ABSTRACT

DE, ANKAN. Device Characterization, Hardware Implementation and System Analysis of Soft switched AC/AC Converters. (Under the direction of Dr. Subhashish Bhattacharya).

Conventional AC-to-DC rectification topology using nonlinear devices, for example diode or thyristor bridges, causes input current harmonics and unwanted reactive power. This effectively deteriorates the voltage and current waveform of the utility grid. Owing to hard switched operation these converters have high switching loss, low frequency of operation, high device stress and are bulky in size. A lot of research has been carried out in the last two decades towards high frequency link dc-dc and dc-ac converters. Various AC-AC converters have also been proposed in the form of cycloconverters and matrix converters. These converters are attributed with complicated controller design, limited buck and boost operation, considerable amount of switching losses and non-favorable frequency changing operation.

The understudied research investigates soft-switching high frequency link AC/AC converters. A number of proposed converters are presented which overcomes the various shortcomings of conventional AC Link schemes. The switching operations occur at zero voltage instants thus lowering the switching losses. The input and output current is harmonic free and the controller also allows setting of desired power factor with buck and boost operations and bi-directional power flow capability.

The work further involves a new kind of device testing to study the unique behavior of current switches under various switching conditions. An attempt has been made to demonstrate the behavior of several devices working under Reverse voltage commutation, hard switched and zero current turn off condition. A new form of switching characteristic has

been noticed and presented. The main motivation of this part of the work is to make a fair judgment on device selection for various soft-switch based topologies.

An in-depth analysis has been done to study optimized module design for series connection of switch and diode. The modules are 3D printed to offer low cost testing of modules. They have been tested up to 4kV in voltage and 100A in current. A DC-DC converter has been built using these modules. The system was stable at full VA rating of the devices.

A modified Steinmetz equation based optimization study has been conducted to analyses magnetics design for DynaC and Partial Resonant converters. The effectiveness of these designs have been shown with corresponding hardware test. The designs showed improvement in efficiency and thermal stability.

A modified version of the understudied converter can function like a Dynamic VAR Compensator (DVC). A system level study has been carried out to study advantages of these fast volt-VAR devices in IEEE-34 BUS system with time varying load and high PV penetration. The work done identifies the various power fluctuations caused by intermittent PV output which can cause unacceptable voltage variations on the feeder. Simulations performed on a prototype feeder indicate that the DVCs are quite effective in smoothing out even the fast voltage variations caused by cloud cover on the PV systems.

Device Characterization, Hardware Implementation and System Analysis of Soft switched AC/AC Converters

by
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DEDICATION

To my parents.

BIOGRAPHY

Ankan De received his Bachelor of Technology degree in Energy Engineering under the Department of Electrical Engineering from Indian Institute of Technology, Kharagpur in 2009. After graduation, he worked in IBM-ISL as an Associate Software Engineer from Jan, 2010 till June, 2010.

He joined the FREEDM Systems Center as an Integrated PhD student at NC State University in Fall, 2010. He received Student Exchange Fellowship to conduct research in ETH-Zurich in 2013. He was awarded the IEEE SUOZZI Intelec Fellowship for the year of 2013 in Hamburg, Germany. He also received Travel fellowship to attend T&D 2014 Conference in Chicago and InterPACK 2015 in San Francisco. He started working in Texas Instruments in Bethlehem, PA from Feb, 16 onwards.

His research interests include Power Electronics, High Frequency Magnetics and High Voltage Packaging. He specializes in AC/AC, resonant and soft switched Converters.

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I would like to thank the rest of my thesis committee members: Dr. Mesut Baran, Dr. Jayant Baliga and Prof. Xiangwu Zhang for their patience and guidance.

My sincere thanks goes to all the staff and students at NSF FREEDM Systems Center at North Carolina State University who kept the center running and thus, facilitated my research work. I am especially thankful to my colleague, Dr. S. Roy, who greatly assisted me in building and implementing some of the more complicated portions of my research. I would also like to thank Adam Morgan for his support both in and outside the work place.

On a personal note, none of this would have been a reality without my parents. I would like to thank them for giving me several second chances all throughout my life. I feel profoundly indebted to their love and trust.

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CHAPTER 1

INTRODUCTION

1.1 Context

Electrical power conversion is undoubtedly the major driving force in all industrial sectors. Electrical power control, process automation and system protection are ubiquitous in most modern industrial, domestic, military or aerospace application today. Switched Mode Power Converters have become standard at these applications on account of their operational efficiency. They combine power control, process automation as well as system protection in a convenient way.

The utility provides ac voltage at constant amplitude and frequency. However, many industrial applications require voltage at variable amplitude and frequency at various power levels. This has to be achieved through power electronic converters which accept power from the utility in a fixed from and deliver power in other forms as required by the loads. While the pulse width modulated voltage source converter (PWM-VSC) configuration has been industry's work horse for over 30 years, significant advances in power semiconductor device technology has resulted in a number of cheaper, compact and more efficient power converters [1] - [3]. In general, the following characteristics can be considered desirable in power converters used as interface converters in the high frequency link systems:

- Bidirectional Power flow
- Unity input power factor
- High Efficiency with Compact size and low weight
- Galvanic Isolation

1.2 Overview Of Various AC/AC Converters

1.2.1 Back-to-Back Voltage Source Converters

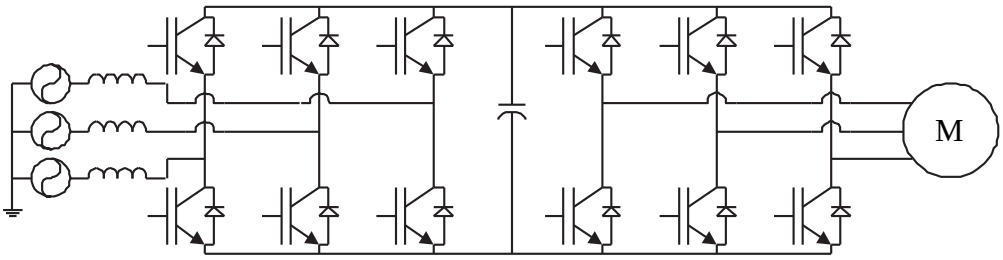


Figure 1.1: Back-to-Back Voltage Source Converters for AC/AC Power Conversion

Figure 1.1 shows the circuit schematic of a typical back-to-back Voltage Source Converter [4]. The front-end Voltage Source Rextifier performs ac-dc power conversion as well as draws sinusoidal current waveforms from the utility. Cascaded Voltage Source Inverter converts DC voltage to AC of required voltage and frequency.

Advantages: Bidirectional, Simple Controller, Low Conduction Losses, Less number of passive components, Compact.

Disadvantages: Usage of Electrolytic capacitor, High Switching loss/stress, High dv/dt, Usage of snubbers, Lacks Galvanic Isolation, Low Frequency Operation, Bulky passive components.

1.2.2 Matrix Converter

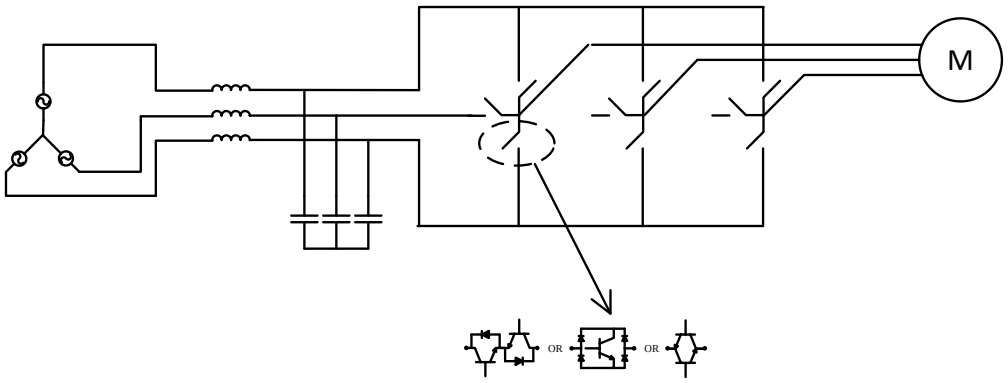


Figure 1.2: Circuit Schematic of a Matrix Converter

Figure 1.2 shows the basic circuit schematic of Matrix Converter [5]. The matrix converter is a direct ac-ac power converter, which connects supply ac utility to output ac load through only controlled bi-directional switches. The output ac signals with adjustable magnitude and frequency are constructed by single- stage power conversion process. The direct ac-ac power conversion principle of the matrix converter leads to the distinct structure with no large dc-link energy storage components. Consequently, the matrix converter topology can be implemented with compact size and volume compared with the diode rectifier based PWM-VSI, where the dc-link capacitor generally occupies 30 to 50 % of the entire converter size and volume.

Advantages: Compact, low Weight/Size, Bidirectional, High Temperature Operation Capability - due to lack of electrolytic capacitor.

Disadvantages: Complicated Control Algorithm, inferior input/output transfer ratio (~86%), limited frequency changing capability, High Switching loss/stress, High dv/dt, Usage of snubbers, Lacks Galvanic Isolation, Low Frequency Operation, Bulky passive components.

1.2.3 Integral Solid State Transformer (SST) Structure

Figure 1.3 shows the basic structure of a typical SST [6]. As compared to Case 1.2.1, here an addition DC/DC Converter is added primarily for isolation. Preferably, as soft switched DC/DC converter are used.

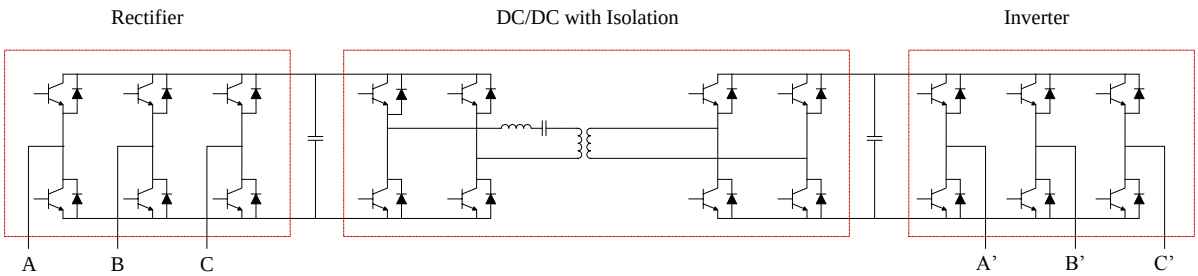


Figure 1.3: Solid State Transformer Structure

This way the frequency of operation can be increased and the magnetics size can be considerably reduced.

Advantages: Bidirectional, Simple Controller, High Frequency Operation, Involves Galvanic Isolation.

Disadvantages: Usage of Electrolytic capacitor, High Switching loss/stress (Rectifier/inverter side), High dv/dt, Usage of snubbers, Low Frequency Operation (Rectifier/inverter side), Bulky filters.

1.2.4 Resonant AC-Link Converter

Fig. 1.4 shows the basic structure of this topology [7]. This is a resonant converter which incorporates soft-switching feature and is characterized by negligible switch turn on and low turn off losses [7]-[10]. It follows a two cycle operation. First, a desired charge is drawn from each phase of a power supply to charge an energy storage element. Second, the charge of the energy storage element is discharged through the output of the same. Through repetitive cycles of the above mentioned operation, charge can be extracted from the power source and injected to the output. Since the AC-Link switching losses are almost negligible, due to the soft switching characteristic, the AC-Link can operate at relatively higher switching frequency.

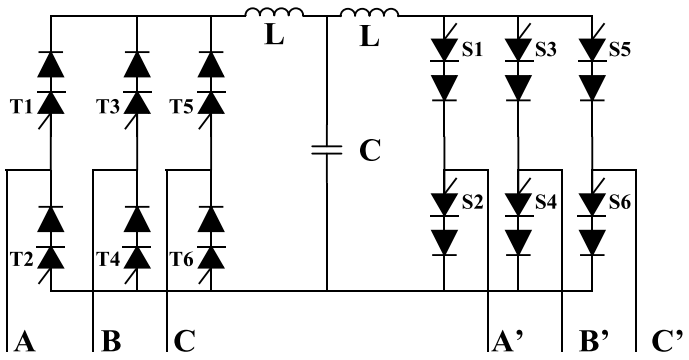


Figure 1.4: Resonant AC-Link Converter

This not only reduces the physical size and complexity but also significantly reduces the losses. It also permits the use of high frequency transformers.

Advantages: Low Loss, Galvanic Isolation, High Frequency Operation, Harmonic Free Input Current.

Disadvantages: High Device Blocking Voltage Stress (Due to resonance, the capacitor charges to a voltage twice the input line-line voltage), Complicated Control Algorithm, Limited Buck-Boost and Frequency Change Capability.

1.2.5 Isolated Dynamic Current Converters (DynaC)

Fig. 1.5 shows the basic schematic of this topology. In this converter, at first the phases with maximum voltage are connected to the transformer first (but turning on the appropriate switches). The turn on duration is set such that the average current in the phases meet the set reference. Then the phases with second highest voltage are turned on till the phase currents meet the desired reference. After this stage of operation, similar sets of operation are conducted to discharge the transferred power from the transformer to the output grid. Through repetitive cycles of the above mentioned operation, charge can be extracted from the power source and injected to the output.

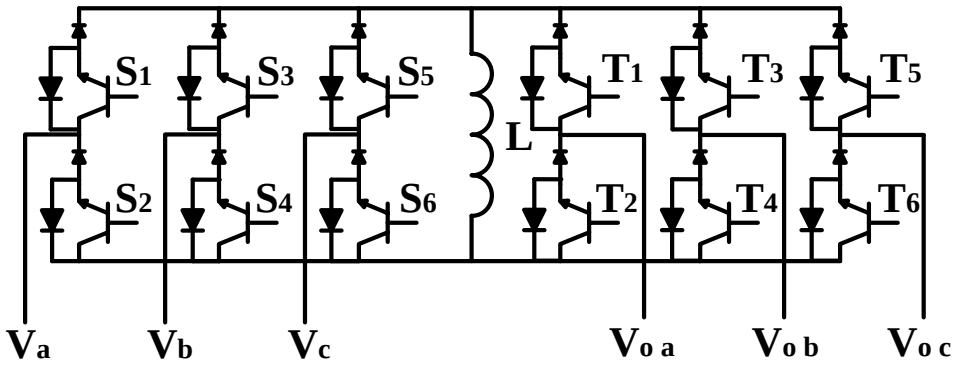


Figure 1.5: Circuit schematic of Isolated Dynamic Current Converters

Advantages: Galvanic Isolation, High Frequency Operation, Harmonic Free Input Current, Simple Controller, Wide Buck Boost and Frequency Capability.

Disadvantages: Need of Snubbers, Hard-Switched Operating states, Reverse Recovery Loss, High Conduction Loss.

1.2.6 Partial Resonant Link Converter

Figure 1.6 shows the basic schematic of this topology [11]. This soft-switched converter uses 12 bidirectional switches and overcomes the various shortcomings of conventional AC Link schemes. The switching operations occur at zero voltage instants thus lowering the switching losses. The input and output current is harmonic free and the controller also allows setting of desired power factor. It can perform buck and boost operations and has bi-directional power flow capability. As the converter operates at high switching frequency, it offers both improved performance and considerable reduction of volume, weight and cost.

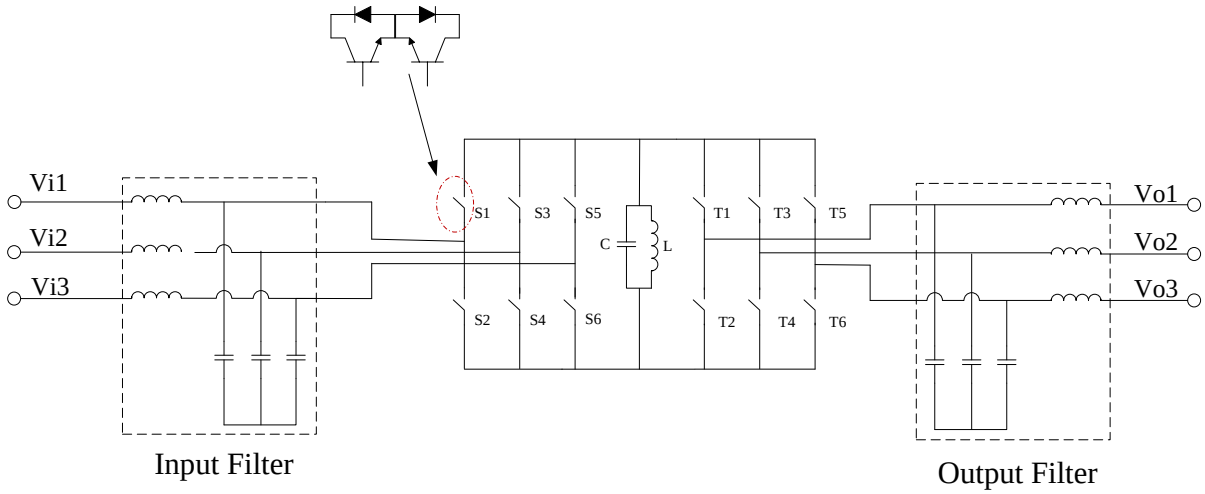


Figure 1.6: Partial Resonant Link Converter Structure

Advantages: Galvanic Isolation, High Frequency Operation, Harmonic Free Input Current, Wide Buck Boost and Frequency Capability, Snubberless, Soft Switched.

Disadvantages: Complex Controller Design, High Conduction Loss.

1.2.7 Converter Based Research Focus

The prime focus of this thesis will be on DynaC and Partial Resonant Link Converter as mentioned in section 1.2.5 and 1.2.6 respectively. Detailed circuit analysis will be presented in subsequent chapters with various modifications to overcome some of the disadvantages of the system. A number of proposed converters will be presented with simulation and hardware results.

1.3 Current Switch Device Characterization

Over the last couple of decades, a lot of work has been done on converters based on Soft Switching techniques [12-14]. The science behind the typical Zero Voltage Switching (ZVS) characteristics has been presented and an in-depth study has been shown [15]. As most available devices are designed for hard switching applications, very little data is available in the literature on device behavior under Current Switch (series connected switch and diode) based soft switching conditions. The application of current-switch inverters such as the High Frequency Link inverter is being actively considered by many manufacturers [16-18]. As current-switch technology matures, designers push the performance envelope for their circuits until the device once again becomes the limiting factor.

Diode reverse recovery is notorious for increasing switching losses in current stiff converters. A lot of effort has been made over the years to mitigate the reverse recovery losses. However, there exists ways to use this feature to achieve zero voltage transition in the same converter thereby, mitigating the loss incurred as compared to hard switched turn off. An attempt has been made to demonstrate the behavior of current switch constructed with different combinations of 1200V devices and 1200V diodes (e.g. Si IGBT in series with Si Diode, Si-IGBT with SiC JBS diode, SiC MOSFET with SiC JBS diode). The switch

behavior under reverse voltage commutation, hard switched and zero current turn off condition at various dc voltage levels are presented. A test circuit has been built and tested with various series connected device combinations, viz. (a) Si-IGBT and Si-Diode, (b) Si-IGBT and SiC-JBS Diode, (c) SiC-MOSFET and SiC-JBS Diode, and (d) Custom Made Package. This work done presents the following device characterizations - (a) Comparison of reverse-recovery losses; (b) Comparison of turn-on Voltage spike (a new form of switching characteristics) for Si-IGBT with SiC-JBS Diode and SiC-MOSFET with SiC-JBS Diode, and (c) Hard Switching loss comparison. The main motivation of this part of the work is to find the best combination of devices to minimize losses and device stress under generic current source converter conditions.

A unique series resonant testing circuit has also been proposed to characterize a 6.5kV SiC Thyristor (GA040TH65). The device has been tested in several soft and hard turn on and off transitions. Conceptual simulation and hardware results have been presented. It has been shown that SiC Thyristor exhibit fast turn-on transitions (~200ns). This coupled with the fact that SiC-JBS Diode (connected in series) has fast reverse voltage commutation leads to an efficient and robust switch combination for a high voltage, high power and high frequency converter. The collected data has been used to estimate overall device losses of a high voltage and high power resonant soft-switched converter.

The main motivation of this work is to evaluate performance and characteristics of a 6.5kV SiC Thyristor based current switch. The device has been tested in: (a) Turn-on : Non-Zero Current + Non-Zero Voltage, (b) Turn-on : Zero Current + Non-Zero Voltage, (c) Turn Off: Zero Current + Zero Voltage and (d) Turn Off: Non-Zero Current + Zero Voltage. These

readings have been enumerated in a Look-Up Table for a converter simulation. The overall switch-losses have been plotted as a function of power for a particular frequency rating.

1.4 Optimum Module Design

As these switches are not widely available in market as a unified package, researchers are forced to use series connected discrete switches to form a current switch. Figure 1.7 shows a schematic of such an arrangement.

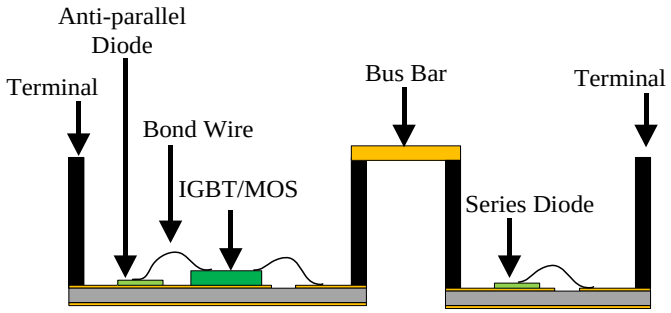


Figure 1.7: Package Schematic of Series Connected Discrete Module

Figure 1.7: shows few permutations of this switch.

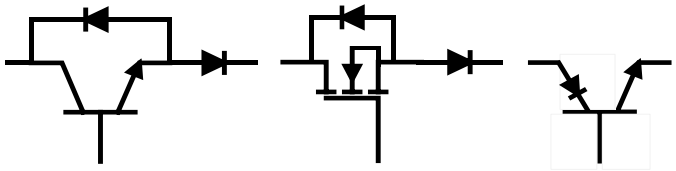


Figure 1.8: IGBT+Diode (left), MOS+Diode (middle) and RB-IGBT (right)

During turn-on mode, current flows from the left Terminal (top to down), through the IGBT/MOS (bottom to top), bondwire connected on the right side of IGBT/MOS toward the BusBar (left to right), to the Series Diode (bottom to top) and finally through the bondwire towards the right Terminal. It should be noted that during this operation, two sets of bondwire comes in series with a Bus Bar. These bondwires usually lead to unwanted parasitic inductances in the circuit. This increases turn off duration and losses and are usually

the primary cause of malfunctioning of packages. Reducing the number of necessary bond wires is an important design goal to make the system more robust and efficient.

ANSYS Q3D/MAXWELL software have been used to analyze and extract parasitic inductance and capacitances in the package along with electromagnetic fields, electric potentials, and current density distributions throughout the package for variable parameters. SIMPLIS-SIMETRIX is used to simulate typical switch behavior for different parasitic parameters under hard switched conditions. Various simulation results have then been used to redesign and justify the optimized package structure for the final current switch design. The thermal behavior of such a package is also conducted in COMSOL in order to ensure that the thermal ratings of the power devices is not exceeded, and to understand where potentially harmful hotspots could arise and estimate the maximum attainable frequency of operation. Hardware setup has been made to characterize the device in unit and continuous pulse tests. The main motivation of this work is to enumerate detailed design considerations for packing a high voltage current switch package.

1.5 Optimized Magnetics Design

One of the primary design constraints of high frequency converters is the magnetic component. The main motivation of this work is to come up with an optimized inductor structure which best matches the required specifications. An accurate derivation of Steinmetz parameter is required for sound prediction of Core Loss. An optimized winding structure has been proposed for minimum core size/weight. The inductor parameters (number of turns and air gap length) are varied and the various losses (copper and core) are tabulated. Two Inductor structures have been proposed: - (a) Low Weight + Moderate Loss and (b) Low Loss + Moderate Weight.

A variable permeability core has also been analyzed. A variable permeability based core as opposed to conventional cores is the fact that the entire core volume is fully utilized to the maximum field strength. This leads to higher inductance for the same/similar volume of the structure. This feature can be used to optimize the size and weight of high frequency magnetics. For transformers, this would result in higher magnetizing inductance thereby reducing the frequency of operation without affecting the size of the converter. For gapped magnetics design, it is shown that certain configuration of permeability variation leads to lower fringing flux which can greatly reduce the overall loss.

1.6 Dynamic VAR Compensator

Utilities try to keep the voltages on a distribution feeder within a target range, and the common practice in United States is to follow the ANSI C84.1 [19] which specifies the range for both service voltage and utilization voltage. On a conventional radial distribution feeder, the common devices employed for voltage control are voltage regulators (VRs) and capacitors. With proper placement of, and coordination between, these Volt-VAR compensators, voltages along a feeder can be kept within acceptable limits under typical load conditions.

Recent interest in connecting small scale renewable energy based generation systems to distribution feeders, partly spurred by the adoption of Renewable Portfolio Standards [20], poses challenges to the conventional Volt-VAR control (VVC) schemes [21]. Connection of large amount of residential scale PV in particular is a challenging case, as it can introduce a highly fluctuating power swing on a distribution feeder [22].

Main impacts of large amount of PV on a feeder include increased voltage variation (voltage rise and voltage fluctuation) along the feeder, negative impact on VRs and Capacitors

operation (voltage control logic, excessive tap movements of VRs and Load Tap Changers, LTCs), and coordination between protection devices [23].

Conventional devices (substation LTC, VRs and Capacitor Banks) employed for VVC on a distribution system act on local information and they are slow acting devices. Hence, these devices respond poorly to voltage variations caused by fast power variations from PVs during a cloudy day. Recently, power electronics based VAR compensators have been proposed to address these challenges, as they can respond to voltage variations much faster and thus provide much more effective VAR compensation on a distribution system [24-25].

In this part of the work, voltage variation issues on a distribution feeder with high PV penetration have been presented first in section II. In section III, the effectiveness of deploying a new type of VAR Compensator, Dynamic VAR Compensator (DVC), in mitigating the voltage variation problems caused by high PV penetration is presented. Section IV provides the conclusions.

1.7 Chapter Outline

Chapter 1 introduces the basic theme of the thesis. Various prior art based power electronic converters are mentioned and a brief introduction of the understudy is mentioned. Reverse Blocking Device characterization is mentioned to show the basic need for this study. One of the section deals with the Dynamic VAR Compensator which may be considered as an immediate practical implementation of the understudied converters.

Chapter 2 presents a new genre of Current Source based AC/AC converter, DynaC. The working principle, simulation and hardware results of the full system have been presented. A slight modification of the topology has been proposed to include battery interface. Hardware results of the same have been presented showing bi-directional power flow. A cascaded

version of this topology has also been proposed. Working principle and hardware results of the same has been presented in details. A sparse AC/DC converter has been proposed with hardware results to confirm the various advantages.

Chapter 3 presents a novel bi-directional soft-switched AC/AC converter. The working principle, simulation and hardware results of the full system have been presented. A sparse AC/DC rectifier has been proposed for Data Center based application. Hardware results of the same have been presented. A brief guide has been given for device selection.

Chapter 4 deals with reverse blocking device characterization. Reverse Voltage Commutation, Switch Overlap Characteristics, Hard Switched, and Forward characteristics of various suitable devices have been tested and studied. The loss data has been used in a look-up table based circuit simulator to predict the total device losses. Both DynaC and Soft Switched AC/AC (as mentioned in Chapter 3) have been simulated showing the appropriate choice of device for each. A new method of characterizing non-turn off Thyristor has been proposed. A 6.5kV SiC Thyristor has been characterized and maximum power efficiency curves have been presented.

Chapter 5 and 6 deals with optimized module and magnetics design. Several hardware and FEM based software results are reported.

Chapter 7 focuses on Dynamic VAR Compensation. The power electronic converter working principle and initial hardware results have been presented. An extensive study has been carried out to show the various advantages of fast Volt-Var Control in an IEEE-34 Bus system. A high PV penetration system has also been studied with and without the DVC. It has been shown that even the fast changing and unpredictable cloud shadowing effect can be mitigated with the use of DVC.

Chapter 8 forms the base for a new kind of SST based study. Voltage stress occurring in different sections of the converter has been studied and presented. A new optimized control system has been presented which effectively reduces this stress. Dielectric heating concept has been reviewed and a test setup has been proposed to study the effect of mixed frequency voltage stress on dielectrics.

In Chapter 9, the thesis is concluded comparing various results and presenting several viewpoints.

CHAPTER 2

DYNAMIC CURRENT (DYNAC) BASED CONVERTER SYSTEM

2.1 Introduction

Conventional Solid State Transformers (SST) are usually realized by a series (back-to-back) connection of AC/DC conversion stage, followed by a DC/DC converter with high-frequency isolation, which is then followed by a DC/AC inverter stage [26]-[30]. Fig. 2.1 shows a circuit schematic of such a topology. These configurations lead to high switch counts which results in additional gate drives, sensors and heat sinks. These are expensive, large, and complex, and have poor efficiency due to multiple devices in the current conduction path. As these technologies are generally developed with voltage-source topologies, bulky energy storage in the form of electrolytic capacitors are typically employed that lower the life and reliability of the product. While film capacitors can be used as an alternative, they come with a significant cost and size penalty. Various AC-AC converters have also been proposed in the form of cycloconverters and matrix converters [31]-[32]. These converters are attributed with complicated controller design, limited buck and boost capability, considerable amount of switching losses and non-favorable frequency changing operation.

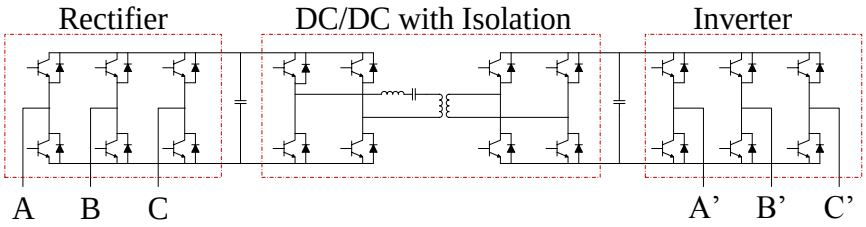


Figure 2.1: Circuit Schematic of a Conventional SST

A more recent invention, Dynamic Current (Dyna-C) Converter presents a novel multi-port, bi-directional, isolated, and compact SST technology based on a current-source topology

with two power conversion stages where each stage is comprised of a standard current-source converter [33]. Fig. 2.2 shows the circuit schematic of this converter. As it can be seen, the convertor consists of much fewer number of devices thereby reducing the overall loss, complexity and size of the system. Furthermore, input/output regulation can be achieved on a switching cycle-by-cycle across all the phases which results in a smaller passive component size. However, it should be noted that it is primarily a hard-switched converter. In one of the transition, a free-wheeling switch+diode leg is commuted which leads to significant amount of reverse recovery loss. Further, as the current in the link inductor needs to be nearly constant, a considerably large magnetic component is required for power transfer.

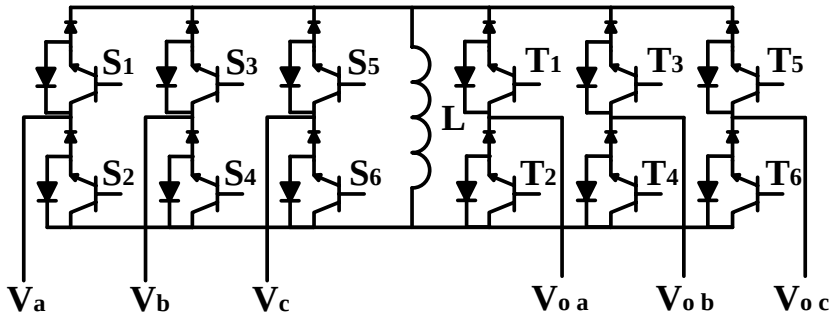


Figure 2.2: Circuit Schematic of Dyna-C.

The proposed controller forces a discontinuous mode of operation. This results in zero current turn on and turn off both at the starting and ending of the switching cycle. The switching scheme is so arranged that the series diode always turns off at zero voltage thereby reducing the reverse recovery losses and device stress. As the converter works under discontinuous mode, there are no freewheeling states. This further makes sure that the diode never undergoes forced reverse voltage commutation. Due to the inherent advantage of switch overlap, the turn on of all the switches (other than the first turn on which occurs at zero current), occur at zero voltage.

These features result in overall lower device stress and high efficiency. As the inductor current follows a triangular trajectory, the value of inductance can be much lower as compared to conventional current source converters. A detailed principle of operation, simulation and hardware test results and a converter/device based comparison has been shown in the later sections.

This converter topology has also been modified to interface with battery to fit in UPS based applications. A cascaded version of this converter has been shown to connect to High Voltage applications. A sparse unidirectional rectifier topology has also been proposed which greatly reduces the number of active switches as compared to conventional converters.

2.2 Principle Of Operation

The principle of operation is explained in this subsection. For simplification, identical (in terms of voltage level and frequency) input and output grid is considered. For other cases, similar procedure can be used to achieve harmonic free power transfer without sacrificing any of the promised advantages. The operating condition is for unity power factor under balanced input and output voltages. This makes voltage and current bear a linear relation (eg. $V_a/I_a = V_b/I_b = V_c/I_c$ = constant). The input (and output) voltage/current waveform can be divided into several 30° sectors.

For this case, the sector where $V_a>0>V_c>V_b$ (which also means $I_a>0>I_c>I_b$) is studied as shown in Figure 2.3. Owing to the symmetric nature of three phase sinusoidal system, similar procedures can be applied in all other sectors for the desired goal of power transfer under soft switched condition.

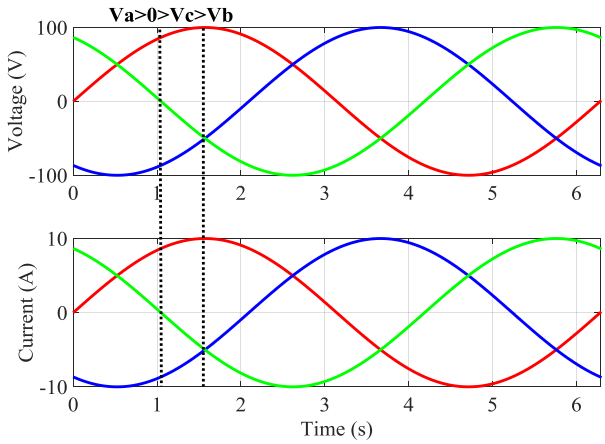


Figure 2.3: Three Phase sinusoidal Input V-I waveform divided into six sectors where A=Red, B=Blue and C=Green. In this illustration, the current is leading the supply voltage.

The switching operation can be divided into five modes of operation:-

Mode 1: Starting from the input side, the link is connected to the input lines having the highest line-line voltage (V_a-V_b in this case). To achieve this, S1, S4 and S6 are turned on. It should be noted that even though S6 is turned on, it would not conduct as the series connected diode is reverse biased. The main motive of turning on S6 is to provide a necessary switch overlap which will be explained in the next mode of operation. With S1 and S4 turned on, the link is charged till the average value of one of the line current (I_b in this case) is equal to the reference set by the controller. This turn-on duration can be calculated using the following formula: -

$$t_1 = \sqrt{\frac{2I_b L}{F(V_a - V_b)}};$$ where 'F' is the Switching Frequency of operation

Figure 2.4 and Figure 2.5 shows the active switches (in red) and the corresponding link voltage and current waveforms.

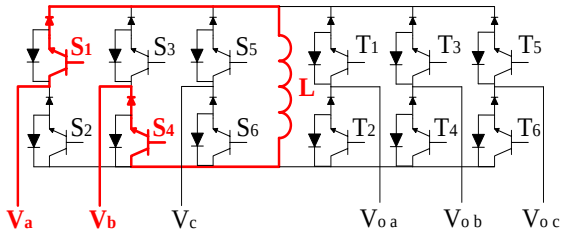


Figure 2.4: Active Switches in Mode 1

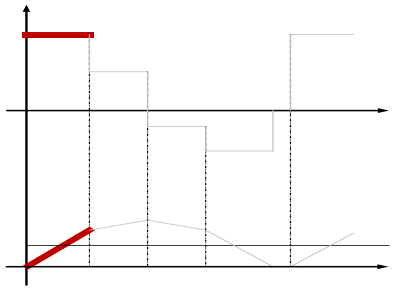


Figure 2.5: Link Voltage and Current

Mode 2: After the end of the previous mode, the switch S4 is turned off. The link inductor current now naturally starts flowing through S1 and S6. The fact that S6 was turned on much before (at the starting of Mode 1) it started conducting, this turn on occurs at near zero voltage. However, the turn-on loss is non-negligible for Si-IGBT [34]-[36]. SiC-MOSFET on the other hand shows a near zero loss in such transition. Further it should be noted that the turn off of series diodes of S4 are under zero voltage thereby reducing the reverse recovery current and stress. Switches T2 and T5 are also turned on (though it would not conduct as the series diodes are reverse biased) during this interval to facilitate zero voltage turn-on in the subsequent Mode. The turn-on duration of S1 and S6 in this mode is:-

$$t_2 = \frac{-b+\sqrt{b^2+4aI_c}}{2a}\text{; where } b=\sqrt{\frac{2(V_a-V_b)I_b}{FL}} \text{ and } a=\frac{(V_a-V_c)}{2L}$$

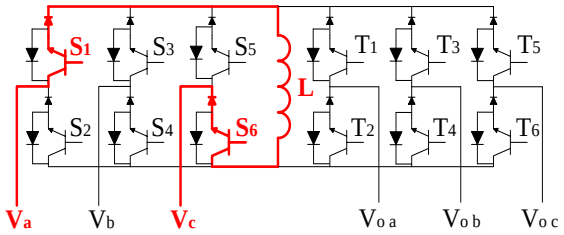


Figure 2.6: Active Switches in Mode 2

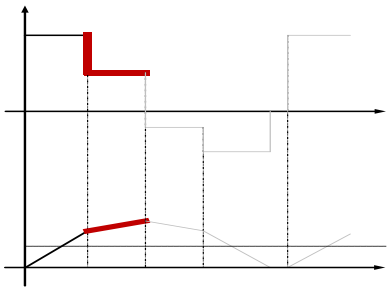


Figure 2.7: Link Voltage and Current

Figure 2.6 and Figure 2.7 shows the active switches (in red) and the corresponding link voltage and current waveforms.

Mode 3: In this mode, the switches S1 and S6 are turned off. This forces the link current to flow through T2 and T5 (which were turned on in mode 2). This transition occurs under zero voltage condition thereby reducing the loss. The turn off of series connected diodes of S1 and S6 are under zero voltage. A negative voltage (V_{oc}-V_{oa}) appears across the inductor which causes the link current to reduce linearly. The duration of turn on time of T2 and T5 is similar to the one mentioned in Mode 2 (the input voltage and current terms should be replaced by the appropriate output voltage and current). The switch T3 is also turned on in this duration (which would not conduct as the series diode is reversed biased). Fig. 2.8 and 2.9 shows the active switches (in red) and the corresponding link voltage and current waveforms.

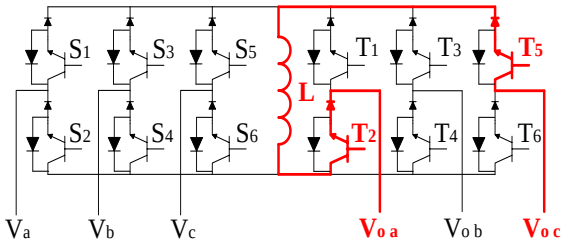


Figure 2.8: Active Switches in Mode 3

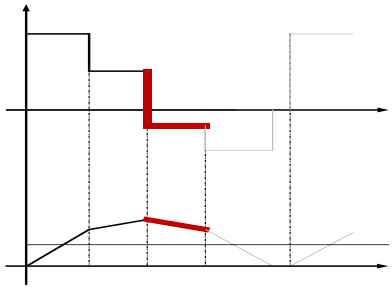


Figure 2.9: Link Voltage and Current

Mode 4: Switch T5 is turned off in this mode forcing the link current to flow through T2 and T3 (which was pre-turned on from the previous mode). This applies a negative voltage (V_b-V_a) across the link inductor causing the link current to further reduce linearly. At some point of time the current through the link will drop to zero. The series diodes of T2 and T3 will then naturally commute off to facilitate zero current turn off. This further reduces the overall losses on the converter. Fig. 2.10 and 2.11 shows the active switches (in red) and the corresponding link voltage and current waveforms.

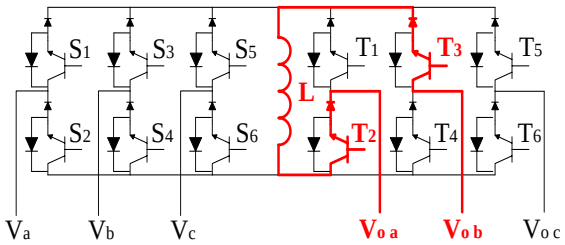


Figure 2.10: Active Switches in Mode 4

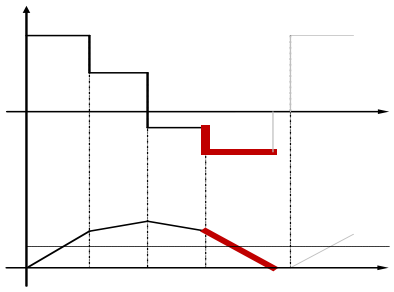


Figure 2.11: Link Voltage and Current

Zero-Vector Mode: After the inductor current reaches zero value and all the switches are soft turned off, the system is allowed to rest till completion of switching time period. As this duration does not directly involve any power transfer, it is denoted as the zero-vector. This is similar to the free-wheeling stage of a conventional current source converter apart from the fact that both voltage and current in the inductor is zero during this mode for the proposed converter. Fig. 2.12 and 2.13 shows the circuit and waveforms during this Mode.

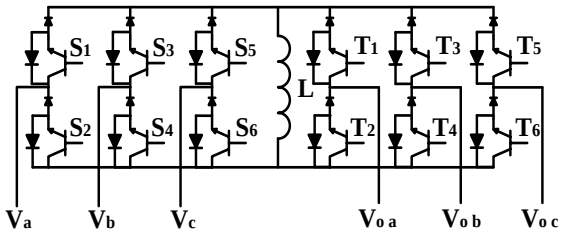


Figure 2.12: In Zero-Vector Mode, all switches are turned off

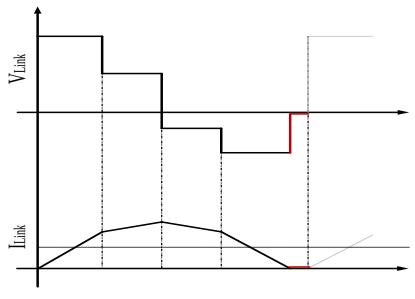


Figure 2.13: The Link voltage and current in Zero-Vector Mode

These modes of operations are repeated thereby transferring power from the input supply to the output grid. In the proposed design, the value of inductor is kept relatively small. This increases the value of conduction dI/dt for the same input voltage level. This results in making the pulsating current triangular as compared to square shaped pulses (in the conventional control scheme) eventually enabling zero current switching.

2.3 Improvement in Reverse Recovery Current

Conventional DynaC and Constant Current Source based converters usually have an inherent issue of high reverse recovery stress. This occurs every switching cycle when the free-wheeling current (during zero-vector mode) flowing through the diode is forced commuted off. As the diode now has to block a significant reverse voltage, the peak reverse recovery current can be notably higher than the rated rms capability of the device [36]. Repeated high current stress operation can lead to device malfunction, unnecessary harmonics and EMI issues. The proposed converter provides a major advantage in this respect. The fact that during the zero-vector mode (when $V_{Link} = 0$), the inductor current is zero owing to discontinuous conduction mode. Therefore, instead of a free-wheeling state, there is a zero current state. As none of the diodes carry any current during this stage, when the circuit goes back to the power transfer mode, there is no reverse recovery.

To further emphasize the logic, a simple mode based comparison study is shown in this section differentiating conventional DynaC and the proposed converter. Fig. 2.14 shows the inductor voltage and current of conventional DynaC. In this case, the inductor current is close to a DC value. As shown in the figure, when the voltage across the inductor is zero (zero-vector mode), the inductor current is constant. Ideally this is achieved by turning on all the switches in a leg (such as S5+S6 or S3+S4 or S1+S2, etc.) to provide freewheeling path to

this current. The diodes in this pole are hence conducting. After the completion of this mode when the power transfer mode (such as turning on S1+S4 like in mode 1) is reinstated, the conducting diodes are forced commuted off by a significantly large reverse voltage. As the value of reverse recovery current is a strong function of conduction current (in this case, it is approximately the DC current flowing through the switches and the inductor), characteristic di/dt of the switch and primarily the reverse blocking voltage, it exhibits a large negative peak current.

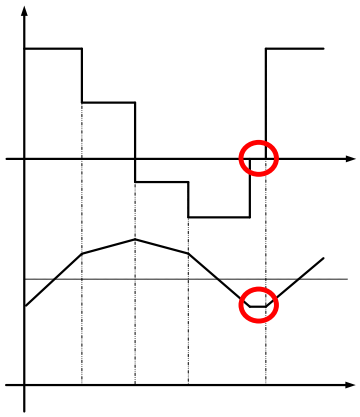


Figure 2.14: The Link voltage (top) and current (bottom) during zero vector mode of Conventional DynaC

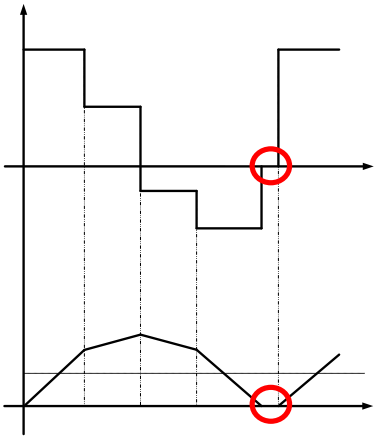


Figure 2.15: The Link voltage (top) and current (bottom) during zero vector mode

This is not witnessed in Mode 1, 2, 3 and 4 as the voltage across diodes remained close to zero during turn off. This effectively reduced the reverse recovery stress. The aforementioned reverse recovery issue in conventional constant current source based converters is unavoidable. The only way to mitigate this phenomenon would be to replace regular Si-Diodes with SiC-JBS Diodes with low reverse recovery losses. This however leads to significantly higher system cost. The inherent discontinuous mode operation in the proposed converter mitigates this problem completely. Fig. 2.15 shows the inductor voltage and current. During the zero-vector mode, the current through the inductor is zero. Hence, all the switches and diodes in the pole are not conducting. When the system shifts from zero-vector to Mode 1, the diodes do not exhibit any reverse recovery current as the conduction current was zero. This effectively lets the designer to use low cost PiN Diodes without the penalty of added switching loss. This also has far reaching consequence in the lifetime of these devices and effectively reduces unwanted harmonics and EMI associated with repeated operation of this.

2.4 Soft Switched Turn-Off Enabled By SiC-JBS Diode

As SiC-JBS Diodes exhibit low reverse recovery current and losses, forced commutation can be used to turn off the diodes before turning off the active switches. This pattern of operation is slightly different from the one mentioned in section 2. For simplicity the same sector where $V_a>0>V_c>V_b$ (which also means $I_a>0>I_c>I_b$) is studied like in Section 2. In this case, during Mode 1, the switches corresponding the second highest line-line voltage is turned on first (S1+S6). When the required amount of charge is drawn from the two phases, S4 is turned on starting Mode 2. As |Vb| > |Vc|, this results in forced reverse voltage commutation of the diode in S6. Hence, S6 stops conducting before the active switch in S6 (IGBT/MOS) is

turned off. Once the current through S6 is close to zero, the active switch can be turned off at zero current. This effectively reduces the turn off losses of the switches. As the reverse recovery current is low, the turn on loss of S4 is significantly low. This operation can be iterated during changeover from Mode 3 to 4 as well. The only hard turn off loss would occur during the transition from Mode 2 to 3 where the active switch has to be turned off to continue the power transfer operation.

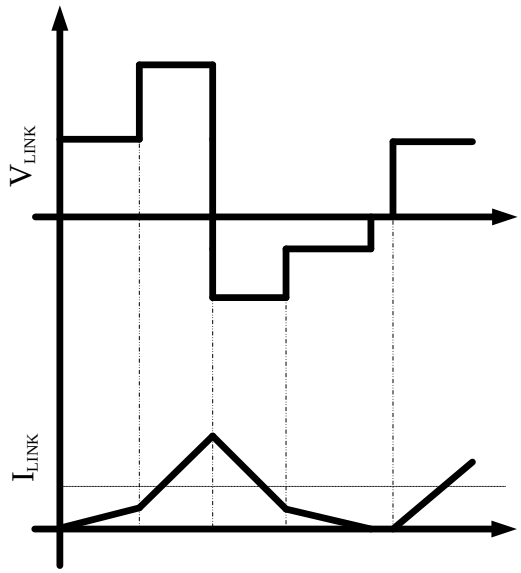


Figure 2.16: The Link voltage and current for alternative control scheme

Fig. 2.16 shows the inductor voltage and current for this switching pattern. This algorithm should not be applied while using Si-PiN Diode as it exhibits large reverse recovery loss. It can be shown that overall efficiency of the converter is highly penalized when Si-PiN Diodes are used with this algorithm. It would be shown in the later section that the overall estimated efficiency of the converter with Si-PiN Diode (using the pattern discussed in Section II) is almost comparable to the one with SiC-JBS Diode (following the aforementioned pattern). As mentioned in the previous section, the price and availability of SiC-JBS Diodes at present

are not comparable to Si-PiN Diodes. This makes Si-PiN the affordable and highly efficient choice for understudied converter.

2.5 System Dynamic Equations

In this section the dynamic equations of the system are derived. It is mentioned in the previous section that the inductor current has four sections in a periodic interval. The dynamic equations are derived for each of the intervals. In this case the source1 (connected to converter 1) is acting as a source of power and the source 2 (connected to converter 2) is acting as a sink of power.

The source 1 voltages are expressed as,

$$v_{a1} = V_{m1} * \sin(\omega_1 t)$$
$$v_{b1} = V_{m1} * \sin(\omega_1 t - 2\pi / 3)$$
$$v_{c1} = V_{m1} * \sin(\omega_1 t + 2\pi / 3)$$

Similarly, the source 2 voltages are expressed as,

$$v_{a2} = V_{m2} * \sin(\omega_2 t + \theta_v)$$
$$v_{b2} = V_{m2} * \sin(\omega_2 t - 2\pi / 3 + \theta_v)$$
$$v_{c2} = V_{m2} * \sin(\omega_2 t + 2\pi / 3 + \theta_v)$$

Interval 1: The inductor current in this duration can be expressed as,

$$i_L = \frac{1}{L}\int_0^{T_1} (v_{a1} + v_{b1})dt$$

where, absolute value of all the voltages are considered.

It is mentioned earlier that in this duration, phase A and B of source 1 are conducting while the other phase is not. Therefore, this is the current expression for phase A and B (the direction of flow is not same).

At the instant T1, the value of the inductor current (denoted as I0) can be expressed as,

$$I_0 = \frac{v_{a1} + v_{b1}}{L} T_1$$

The average value of A-phase current in a periodic interval (switching interval) is expressed as,

$$I_{a1,avg} = \frac{T_1 I_0}{2T}$$

For any given power factor angle θ1 in the converter 1 side we can write following expression,

$$I_{a1,avg} = k_1 V_{m1} \sin(\omega_1 T_1 + \theta_1) = \frac{T_1 I_0}{2T}$$

where k1 is the scaling factor between voltage and current peak magnitudes, i.e., k1 = Im1/Vm1

Interval 2: In this duration, the phases B and C of the source 1 are the conducting phases and other phases are remaining idle. Similar to the earlier case, the inductor current can be expressed as (this is same as the absolute value of the phase B and phase C instantaneous currents),

$$i_L = |i_{b1}| = |i_{c1}| = \frac{1}{L} \int_{T_1}^{T_2} (v_{b1} + v_{c1}) dt + I_0$$

Let us denote the inductor current at the instant T2 as I1. So,

$$I_1 = I_0 + \frac{v_{b1} + v_{c1}}{L} (T_2 - T_1)$$

The C-phase of the source 1 carries current only in this duration (in a switching cycle). So, the average C-phase current in a switching period can be expressed as,

$$I_{c1,avg} = \frac{T_2 - T_1}{2T} (I_1 + I_0)$$

The power factor angle of the C-phase current is given as θ_1. Therefore, we can write the following expression,

$$I_{c1,avg} = k_1 V_{m1} \sin(\omega_1 T_2 + 2\pi/3 + \theta_1) = \frac{T_2 - T_1}{2T}(I_1 + I_0)$$

From the above equations,

$$\frac{\sin(\omega_1 T_2 + 2\pi/3 + \theta_1)}{\sin(\omega_1 T_1 + \theta_1)} = \frac{T_2 - T_1}{T_1} * \frac{I_1 + I_0}{I_0}$$

Replacing I_1 and I_0 in the above equation and then rearranging it,

$$\left(\frac{T_2 - T_1}{T_1}\right)^2 * \frac{v_{b1} + v_{c1}}{v_{a1} + v_{b1}} + 2\left(\frac{T_2 - T_1}{T_1}\right) - \frac{\sin(\omega_1 T_2 + 2\pi/3 + \theta_1)}{\sin(\omega_1 T_1 + \theta_1)} = 0$$

Solving this equation,

$$\frac{T_2}{T_1} = 1 - \frac{v_{a1} + v_{b1}}{v_{b1} + v_{c1}} * \left(1 \mp \sqrt{1 + \frac{v_{b1} + v_{c1}}{v_{a1} + v_{b1}} * \frac{\sin(\omega_1 T_2 + 2\pi/3 + \theta_1)}{\sin(\omega_1 T_1 + \theta_1)}}\right)$$

Interval 3: In this mode the extraction of stored energy from the inductor is initiated. As shown in Fig. 2.4, the phases C and B of the source 2 starts conducting at the instant T2. The instantaneous value of the inductor current can be expressed as (this is also the expression of B and C-phase currents of source 2),

$$i_L = -\frac{1}{L}\int_{T_2}^{T_3} (v_{b2} + v_{c2})dt + I_1$$

So,

$$I_2 = -\frac{v_{b2} + v_{c2}}{L}(T_3 - T_2) + I_1$$

where, I2 is the value of the inductor current at the instant T3. It is shown in Fig. 2.4 that the C-phase of source 2 conducts only in this duration (for a switching period T). Therefore, the average value of C-phase current within the time period T is,

$$I_{c2,avg} = \frac{T_3 - T_2}{2T}(I_1 + I_2)$$

For a given power angle θ_2 at the source 2 side, the above equation can be written as,

$$I_{c2,avg} = k_2 V_{m2} \sin\left(\omega_2 T_3 + 2\pi/3 + \theta_v + \theta_2\right) = \frac{T_3 - T_2}{2T}(I_1 + I_2)$$

Interval 4: This is the interval where the remaining stored energy in the inductor is extracted. Similar to previous cases, the current through the inductor secondary winding can be expressed as,

$$i_L = -\frac{1}{L}\int_{T_3}^{T_4}(v_{a2} + v_{b2})dt + I_2$$

It is ensured that the inductor current becomes zero at the end of this interval. So, at t = T4,

$$i_L = 0 = I_2 - \frac{v_{a2} + v_{b2}}{L}(T_4 - T_3)$$

Therefore,

$$I_2 = \frac{v_{a2} + v_{b2}}{L}(T_4 - T_3)$$

In this duration, the inductor current is same as the absolute magnitude of A and B-phase currents of the source 2. The A-phase of source 2 conducts only in this duration (considering only a switching cycle). Therefore, the average value of A-phase current for this small duration (switching period T) is,

$$I_{a2} = \frac{T_4 - T_3}{2T} I_2$$

For the same given power factor angle q2 at this source side we can express the average current (for a small duration T) as,

$$I_{a2} = k_2 V_{m2} \sin(\omega_2 T_4 + \theta_v + \theta_2) = \frac{T_4 - T_3}{2T} I_2$$

Considering the above equations,

$$\frac{\sin(\omega_2 T_3 + 2\pi/3 + \theta_v + \theta_2)}{\sin(\omega_2 T_4 + \theta_v + \theta_2)} = \frac{T_3 - T_2}{T_4 - T_3} * \left(\frac{I_1 + I_0}{I_0} \right)$$

Rearranging the above equation,

$$= \frac{T_3 - T_2}{T_4 - T_3} * \left(2 + \frac{v_{b2} + v_{c2}}{v_{a2} + v_{b2}} * \frac{T_3 - T_2}{T_4 - T_3} \right)$$

$$\left(\frac{T_3 - T_2}{T_4 - T_3} \right)^2 * \frac{v_{b2} + v_{c2}}{v_{a2} + v_{b2}} + 2 * \frac{T_3 - T_2}{T_4 - T_3} - \frac{\sin(\omega_2 T_3 + 2\pi/3 + \theta_v + \theta_2)}{\sin(\omega_2 T_4 + \theta_v + \theta_2)} = 0$$

Therefore,

$$\frac{T_3 - T_2}{T_4 - T_3} = -\frac{v_{a2} + v_{b2}}{v_{b2} + v_{c2}} * \left(1 \mp \sqrt{1 + \frac{v_{b2} + v_{c2}}{v_{a2} + v_{b2}} * \frac{\sin(\omega_2 T_3 + 2\pi/3 + \theta_v + \theta_2)}{\sin(\omega_2 T_4 + \theta_v + \theta_2)}} \right)$$

And,

$$\frac{v_{a2} + v_{b2}}{L} * (T_4 - T_3) = I_1 - \frac{v_{b2} + v_{c2}}{L} * (T_3 - T_2)$$

Replacing I1 in the above equation,

$$T_1(v_{a1} - v_{c1}) + T_2(v_{b1} + v_{c1} + v_{b2} + v_{c2}) + T_3(v_{a2} - v_{c2}) - T_4(v_{a2} + v_{b2}) = 0$$

2.6 Governing Equations and Controller Block Diagram

It is shown in the previous section that there are three main governing equations of the system in different zones of a periodic interval. These equations are repeated below.

$$\frac{T_2}{T_1} = 1 - \frac{v_{a1} + v_{b1}}{v_{b1} + v_{c1}} * \left(1 \mp \sqrt{1 + \frac{v_{b1} + v_{c1}}{v_{a1} + v_{b1}} * \frac{\sin(\omega_1 T_2 + 2\pi/3 + \theta_1)}{\sin(\omega_1 T_1 + \theta_1)}} \right)$$

$$\frac{T_3 - T_2}{T_4 - T_3} = -\frac{v_{a2} + v_{b2}}{v_{b2} + v_{c2}} * \left(1 \mp \sqrt{1 + \frac{v_{b2} + v_{c2}}{v_{a2} + v_{b2}} * \frac{\sin(\omega_2 T_3 + 2\pi/3 + \theta_v + \theta_2)}{\sin(\omega_2 T_4 + \theta_v + \theta_2)}} \right)$$

$$T_1(v_{a1} - v_{c1}) + T_2(v_{b1} + v_{c1} + v_{b2} + v_{c2}) + T_3(v_{a2} - v_{c2}) - T_4(v_{a2} + v_{b2}) = 0$$

Looking at these equations above, there are three unknowns (T1, T2 and T3). Here, T4 is a known quantity. It is derived from the power flow demand between the converters. As the time period (T) is known, T4 decides the dead time (comes from the power flow demand)

between the converters (see Fig. 2.4). The value of the switching intervals T1, T2 and T3 are found out from the above equations for a given power flow demand.

The block diagram of the controller for the system is as shown in Fig. 2.17.

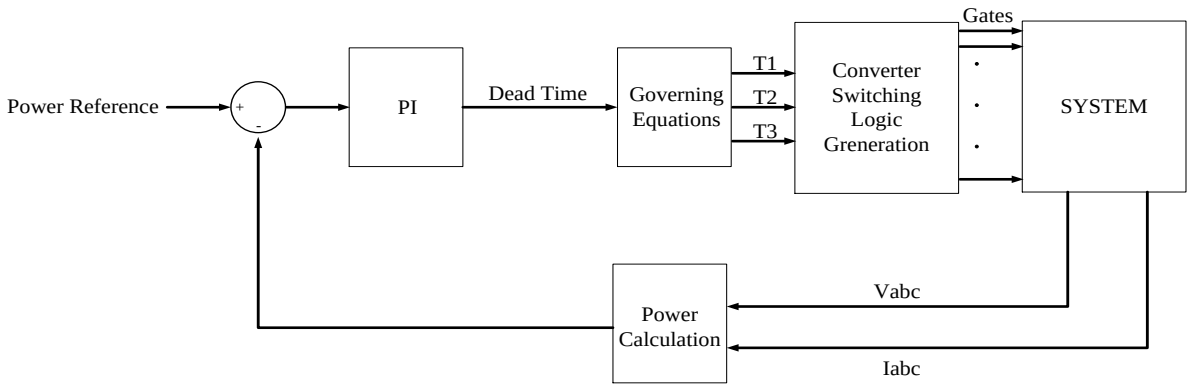


Figure 2.17: Block diagram of the closed loop system

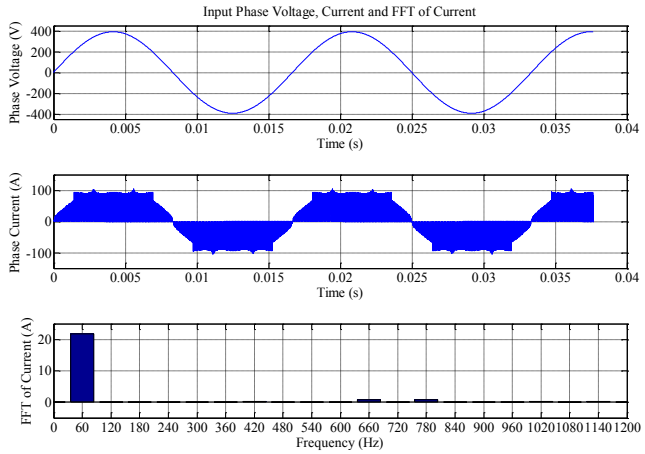
2.7 Simulation Results

The system has been simulated with series connected IGBT and Diode. The switching frequency has been selected to be 20 kHz and the cut off frequency of the filter is around 2 kHz. This is done to verify if the control scheme is effective in drawing harmonic free input current. The section is divided into the following subparts:-

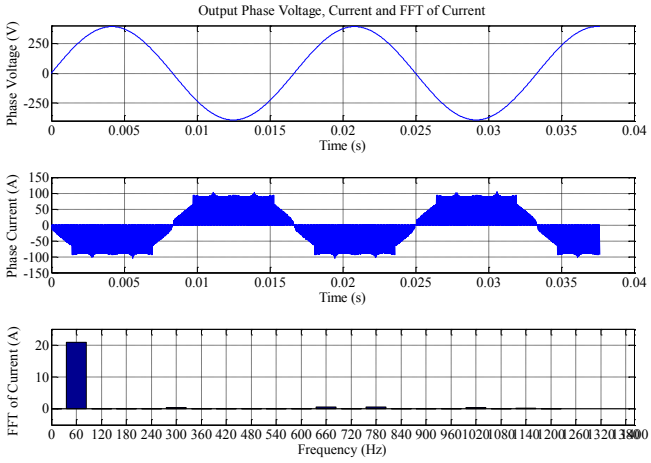
(a) Unity power factor operation (both input and output); (b) Frequency Changer Operation; and (c) Voltage Boost Operation.

(a) Unity power factor operation in Identical Grid

In this case, power is being transferred between two identical grids ($V_{LL,Rms}$=480V,60Hz). Fig. 2.18 (a) and (b) show the phase voltage, unfiltered line current and the harmonics in the line current for input and output phase respectively. As mentioned in the previous section of the chapter, it draws harmonic-free current from input and also the load consumes harmonic-free current. This confirms the effectiveness of the controller and the switching algorithm.



(a)

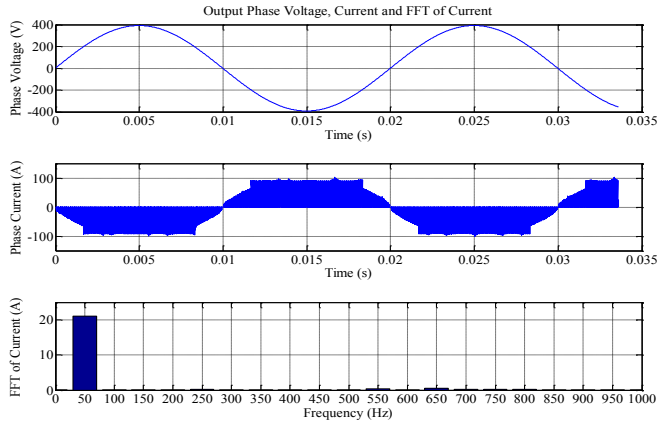


(b)

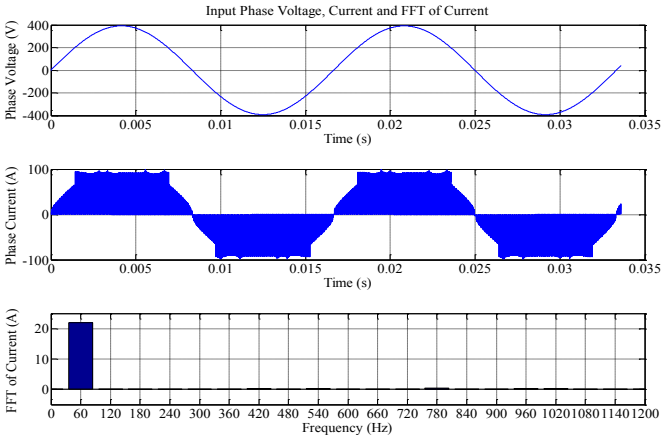
Figure 2.18: (a) Input Phase Profile, (b) Output Phase Profile

(b) Frequency Changer Operation

In this case, power is being transferred between two grids with different frequency of operation ($V_{LL,Rms}$=480V,60Hz and $V_{LL,Rms}$=480V,50Hz). Fig. 2.19 (a) and (b) show the phase voltage, line current and the harmonics in the line current for input and output phase respectively. As seen in the figure, both input and output current are harmonic-free. It can be seen in the figure that the power drawn and dissipated is still in unity power factor.



(a)

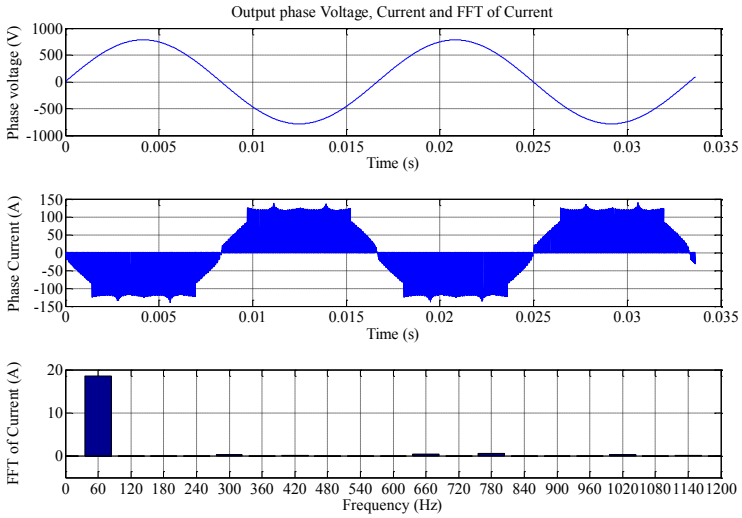


(b)

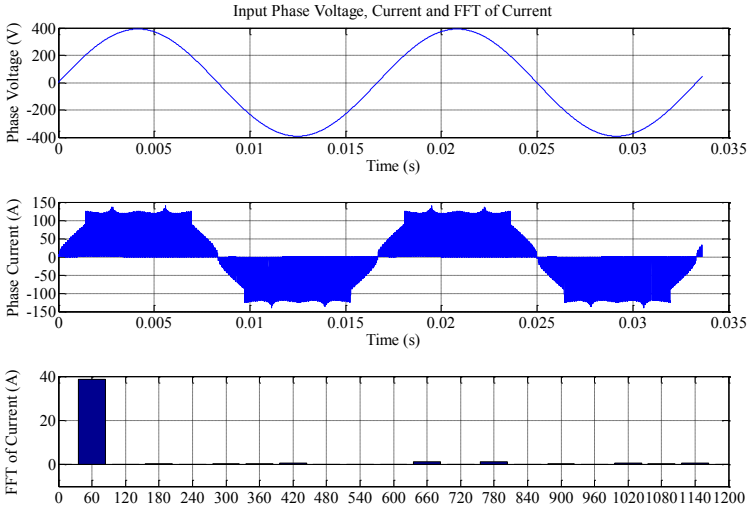
Figure 2.19(a): Input Phase Profile, (b) Output Phase Profile

(c) Voltage Boost Operation

In this case, power is being transferred between two grids with different voltage levels ($V_{LL,Rms}$=480V,60Hz and $V_{LL,Rms}$=960V,50Hz). Fig. 2.20 (a) and (b) show the phase voltage, line current and the harmonics in the line current for input and output phase respectively. As expected, it draws harmonic-free current from input and also the load consumes harmonic-free current. This case shows that this topology can function well in boost operation. A low power (3kVA) hardware prototype has been built as seen in Fig. 2.21. The topology has been tested with various sets of devices – both 1200V Si-IGBTs and 1200V SiC MOSFETs.



(a)



(b)

Figure 2.20(a) Input Phase Profile, (b) Output Phase Profile

2.8 Experimental Results

The above mentioned converter operation is experimentally verified as shown below. The control logic is implemented using a DSP platform (TMS320F2812). Gate pulses are generated for the IGBTs corresponding to the maximum and minimum phase voltages as explained in the above section. The voltage of the transformer primary winding is shown in -

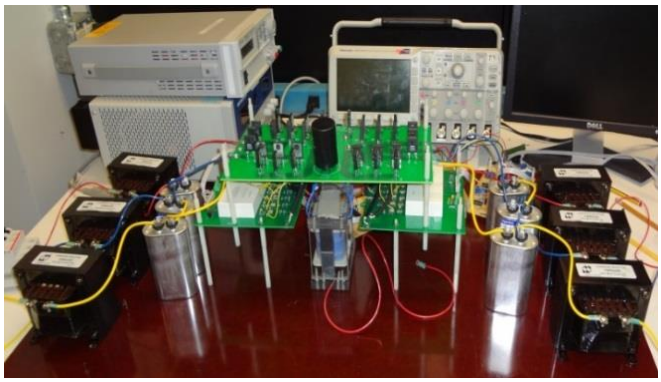


Figure 2.21: Hardware Testing Setup

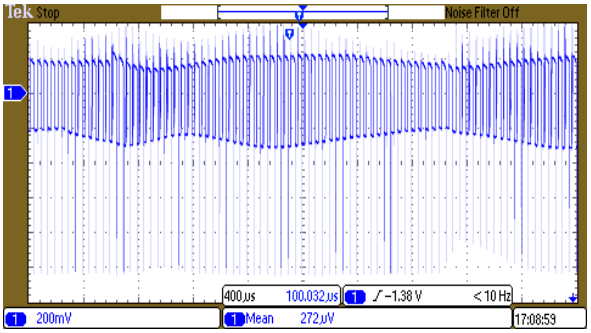


Figure 2.22: Primary winding voltage of the fly-back transformer under steady state operation

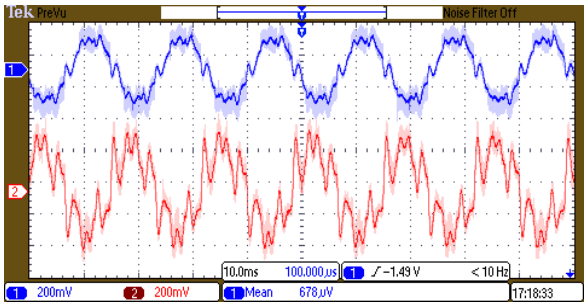


Figure 2.23: Input phase voltage and current for simplified controller

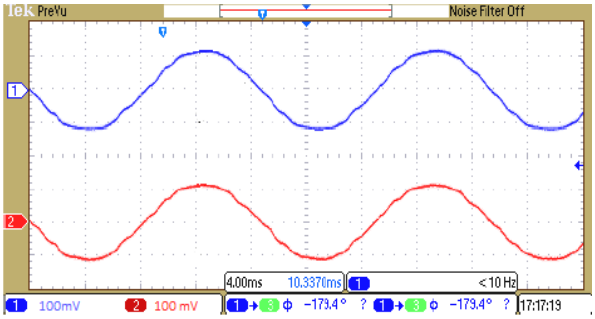


Figure 2.24: Input phase voltage and current for Harmonic Free controller

Fig. 2.22. Similarly, Fig. 2.23 shows the input phase voltage and current for the simplified controller where only the phases corresponding to the maximum line-line voltages are chosen for power transfer. As expected, this results in high THD and therefore is not acceptable. Fig. 2.24 shows the input phase voltage and current corresponding to the controller explained in the previous section. As it can be seen, this results in nearly zero THD in current with negligible common coupling voltage distortion.

2.9 Converter System with Integrated Battery Storage

The AC to AC converter structure shown in Fig. 2.25 is modified to integrate a battery storage system with it. The purpose of this is to integrate a number of renewable energy sources within the system. A series of lithium ion batteries are connected and the battery charger is connected via a bidirectional converter so that energy can be drawn from the grid to charge the battery and during energy crisis the same energy can be fed back to the grid.

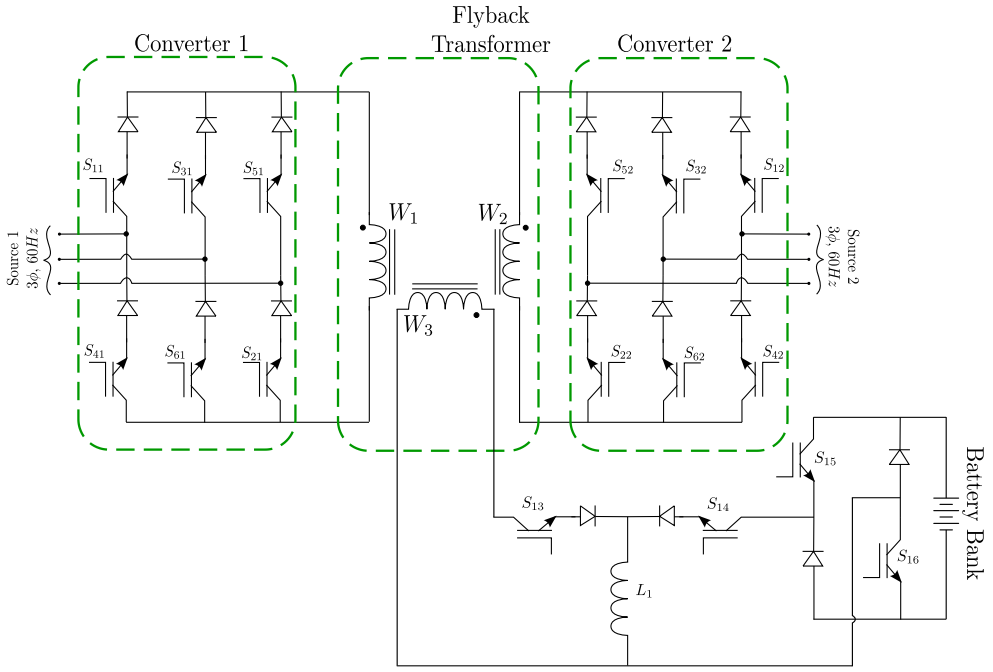


Figure 2.25: Converter structure with the integrated battery energy storage system

2.9.1 Experimental results

The functionality of the system with the integrated battery energy storage is experimentally verified for both charging and discharging mode of the battery. Two series connected 12Volt lithium ion batteries are connected as shown in Fig. 2.25.

The laboratory prototype is built for the following specifications:-

Power Rating: 2kW

Voltage Rating: 300V

Inductance of the main fly-back inductor: 300uH

Number of turns of the three winding fly-back inductor: 40:40:10 (N1 : N2 : N3)

Inductance of the battery charger inductor (L1): 700mH

Part No of the switches: IGBT (IXA12IF1200HB); Diode (ISL9R30120G2)

Fig. 2.26 shows the voltage and current through the inductor (L1 as shown in Fig. 2.25). In this case a 500W load resistance is connected in place of the battery bank. This is to verify the operation of the bidirectional DC-DC converter. The voltage across the primary winding (W1 as shown in Fig. 2.25) and current through it are shown in Fig. 2.27 with the battery bank connected to the circuit. Fig. 2.28 shows the same winding voltage and current while the DC load is not connected.

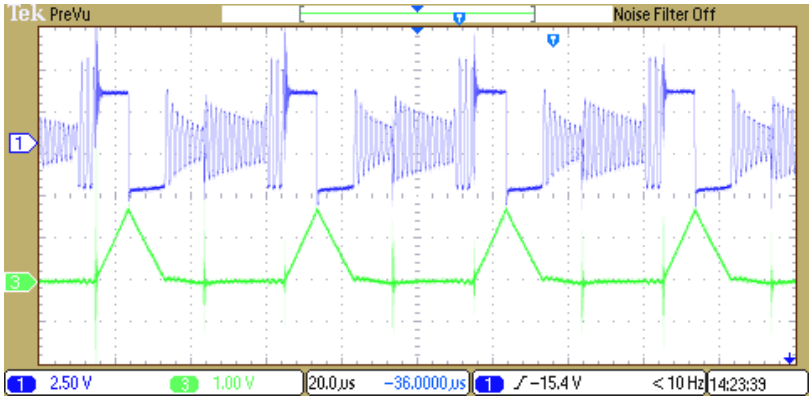


Figure 2.26: DC inductor (L1) voltage and current at steady state

It can be easily seen that the W1 winding current has two different slopes when the battery bank connected to the system. Initially, current is flowing to store energy in the fly-back transformer air-gap as well as to store energy in the DC inductor air-gap. The moment the DC inductor is in discharging mode, it gets isolated from the main inductor and the slope of the main inductor current changes.

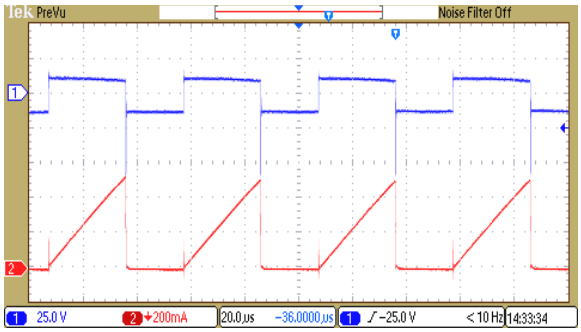


Figure 2.27: Voltage and current of the winding W1 while the DC load is not connected.

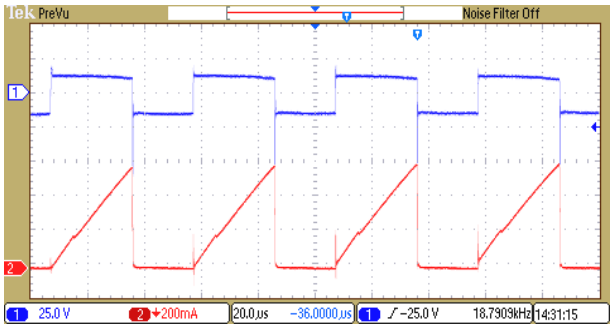


Figure 2.28: Voltage and current of the windingW1 while energy is extracted to supply the DC load.

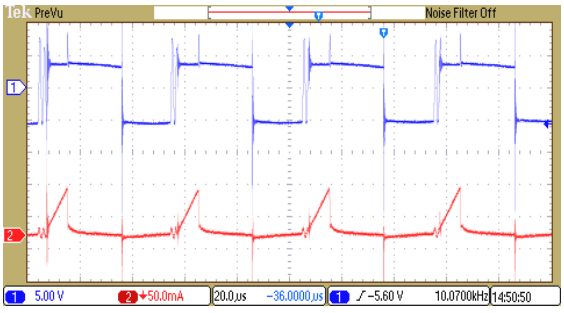


Figure 2.29: Voltage and current of the windingW3 while the DC load and the battery bank are connected.

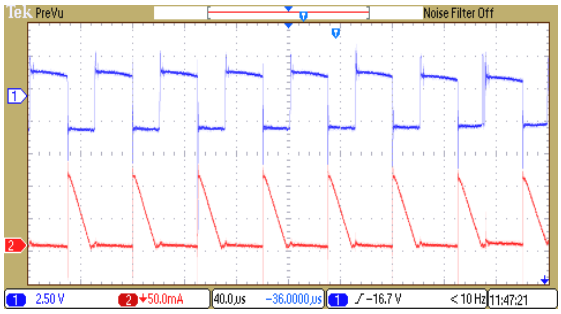


Figure 2.30: Voltage and current of the winding W3 while the battery bank is in discharging mode.

Fig. 2.29 shows the winding W3 voltage and current while the battery bank is connected to the system. The same winding voltage and current are shown in Fig. 2.30 while the battery is in discharging mode.

2.10 CSI Based Cascaded Solid State Transformer for Railway Traction Application

The conventional power converter in the railway traction system requires a line frequency transformer at the front end. Fig. 2.31 shows the structure of the conventional converter system with the bulky line frequency transformer. With the invention of solid state transformer, the bulky and heavy line frequency transformer can be replaced with the compact high frequency one just to increase the available space for passengers. The problem in selecting high switching frequency for the transformer is the unavailability of suitable devices at that high voltage. Therefore, the line frequency transformer has been replaced with medium frequency transformer first. Now research is going on to replace the medium frequency transformer with the high frequency one. [37]- [38] have shown a cascaded converter topology with a medium frequency transformer. The converter topology with high frequency transformer is discussed in [39]. Here also cascaded converters are used to distribute the catenary voltage among the sections. Here the front end converters are connected in series and the rear end converters are connected in parallel. This rear end

produces the required DC bus voltage for the motor control converter. The topology is based on voltage source converters. [40]-[41] discuss about basic power electronic based high frequency transformer concept which can be used to replace the bulky line frequency transformer. These topologies can also be used for railway applications. In this section, a cascaded converter based topology with high frequency transformer is proposed where current source converters are used. It is well known that in medium and high voltage applications current source converters are preferred compared to the voltage source converters. It is because of the fact that current source converters have better control on the short circuit current during fault conditions.

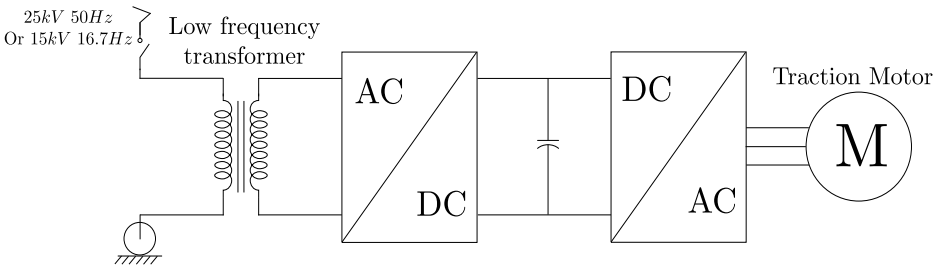


Figure 2.31: Conventional railway traction motor drive system

2.10.1 Converter Topology

Fig. 2.32 shows the proposed cascaded CSI based converter topology for the railway traction drive system. Each of the converter section consists of two cascaded full-bridge inverters and a high frequency fly-back inductor. The fly-back inductor with two windings provides electrical isolation between the sources. It also allows to step-down the catenary voltage to the specified level. The input side full bridges are connected in series to distribute the catenary voltage among the sections. This allows the use of low voltage devices for the converters. The output sections of each cascaded converters are connected in parallel as shown in Fig. 2.20. This allows the low voltage and low current devices to be used in the rear

end converter of each cascaded sections. Filter capacitors are connected at the input as well as the output side. The input side AC capacitors are connected in series to distribute the catenary voltage to each of the cascaded sections. The switching scheme of the cascaded sections is same. Therefore, the current in the series connected front end converters will differ and the catenary voltage distribution will not be equal. The series connected capacitors should be able to handle the small mismatch in the current of the front end converters. The design and fabrication of the inductors should be identical to extent it is possible. The rest will be taken care by the capacitors. The output sections of the cascaded converters are connected in parallel to the output DC bus capacitor. Therefore, any mismatch in the secondary side of the fly-back inductors current should not lead to much problem. The problem can arise due to the mismatch in the series connected front end converter side inductors. The series connected capacitors should be able to handle this mismatch in individual currents. The control of individual converter sections should take care of the input capacitor voltage balancing along with controlling the output capacitor voltage. As shown in Fig. 2.32, suitable resistances are connected across each series connected capacitor to have proper distribution of the catenary voltage.

2.10.2 Principle of Operation

Fig. 2.33 shows a section of the cascaded converter discussed above. It consists of three parts as (i) front end converter, (ii) fly-back inductor and (iii) rear end converter. The front end converter is used to store energy in the fly-back inductor depending on the front and rear end capacitor voltages. The direction of current flow in the fly-back inductor remains always same. The converter switches to be turned ON are selected so as to make the inductor current always positive. Therefore, switches which can carry unidirectional current are chosen for

this application. For a particular instant switches corresponding to the positive current in the primary winding of the fly-back inductor are turned ON. This allows some energy to get stored in the air gap of the fly-back inductor. During this charging time, the rear end converter remains in sleeping mode.

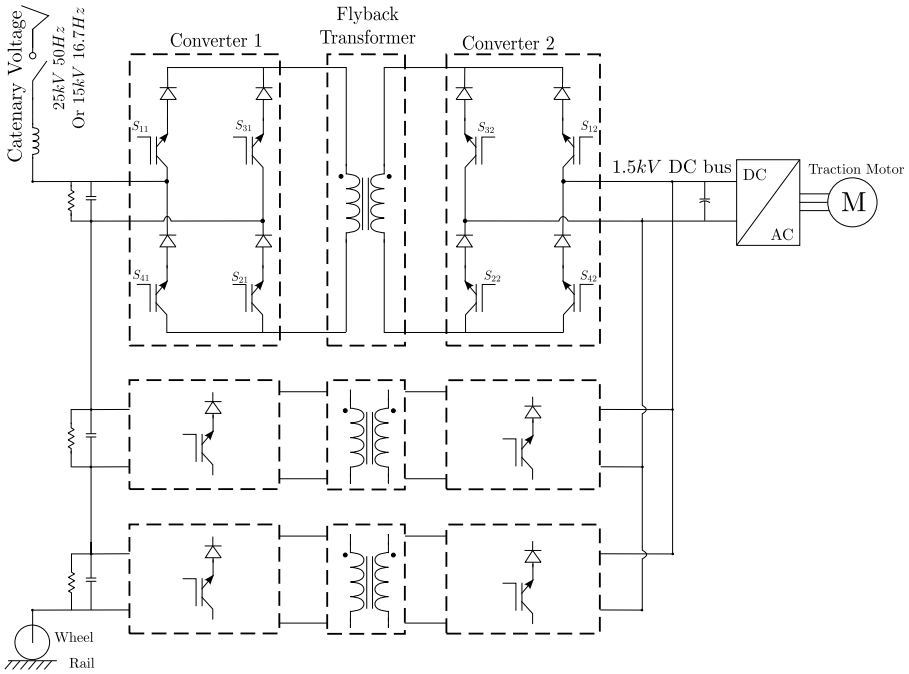


Figure 2.32: Proposed cascaded converter topology for the railway traction drive system

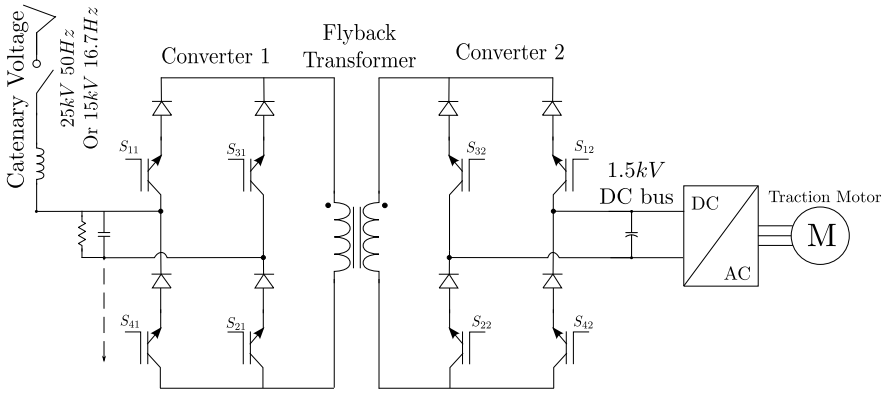


Figure 2.33: A section of the cascaded converter

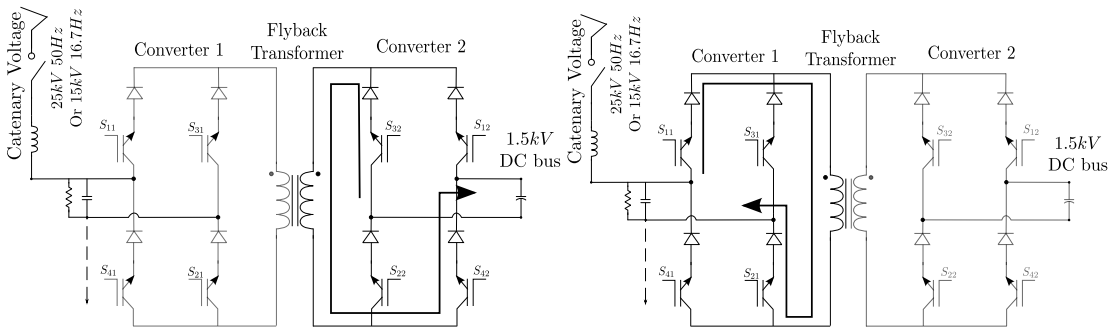


Figure 2.34: Fly-back inductor Charging (left) and Discharging (right) of the cascaded converter

The rear end converter switches are turned ON and the front end pairs are turned OFF when the inductor current reaches a specified value. The switches are so selected that the energy stored in the air gap is dumped into the output capacitor. During this mode the front end converter goes to sleeping mode like the rear end converter in inductor charging mode. Fig. 2.34(a) and (b) show the possible inductor charging and discharging current paths respectively. In practice, there should be an overlapping time between the two converters to avoid voltage spike due to high Ldi/dt. This charging and discharging of the inductor is performed within a short period compared to the fundamental period of the source voltage. The fly-back transformer size and weight depends on the selected frequency of this charging and discharging cycle. The switching sequence of the cascaded converters remains same. This equalizes the voltage sharing of the series connected capacitors at the input side. However, there may be difference in the switching characteristics of the IGBTs and the fly-back inductors may not be identical. This will lead to unequal voltage distribution in the input capacitors. The control of the converters should be able to take care of this unequal voltage distribution at steady state.

2.10.3 Experimental Results

The functionality of the proposed cascaded converter has been experimentally verified on a laboratory prototype. The prototype is built with three series connected converter sections at the input side. The output sides are connected in parallel as mentioned in the above paragraphs. In practice, the number of cascaded sections can be decided based on the available IGBT voltage rating. The rear end converter devices are selected on the basis of available device current ratings and number of cascaded sections. The input of the prototype is fed from normal single phase utility supply (120V; 60Hz). A resistive load (40W) is connected at the output side.

The following are the design specifications of the laboratory prototype built in FREEDM system center:

- Input supply- 120V, 60Hz single phase supply.
- Fly-back inductance- 256mH (top one), 324mH (middle one) and 280mH (bottom one).
- Input side (ac side) capacitors: 10mF, 370 Volt AC capacitors.
- Output side capacitors: 470mF, 500V DC capacitors.
- Load resistance- 40W
- AC side filter inductor- 5mH

It is discussed in the earlier sections that using similar fly-back inductors for the cascaded sections is needed in order to keep the voltages of the input side capacitors balanced under steady state. This ensures similar voltage stress on the devices of the front end converter. However, there can be some sort of mismatch in the fly-back inductor values. This results in unequal voltage distribution on the input side capacitors and therefore unequal voltage stress

on the devices. In order to avoid this, the cascaded front-end converters are controlled separately so as to make the capacitor voltages balanced. In the following paragraphs the experimental results are shown to justify the functioning of the converter.

Fig. 2.35 shows the fly-back transformer primary winding voltages (top and middle converter) with and without the input capacitor voltage balancing algorithm working respectively. The primary winding voltages of the top and bottom converter are shown in Fig. 2.36. Fig. 2.37 shows the top fly-back transformer primary voltage and the DC output voltage of the converter.

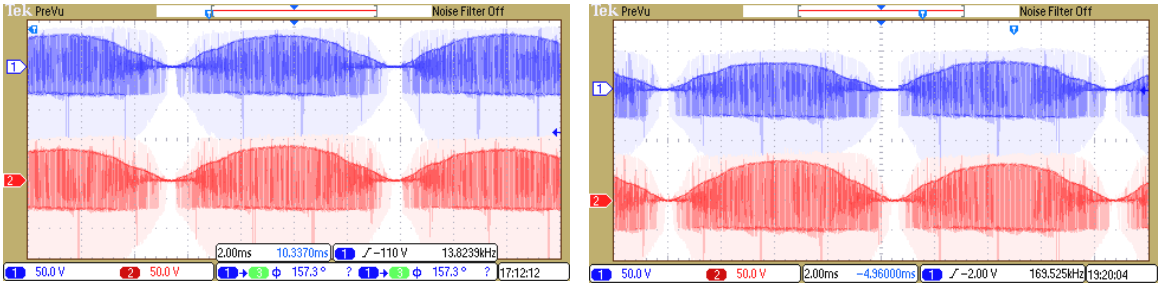


Figure 2.35: Primary winding voltages of the top (ch1) and middle (ch2) fly-back transformers with (left) and without (right) the voltage balancing algorithm of the input capacitors working

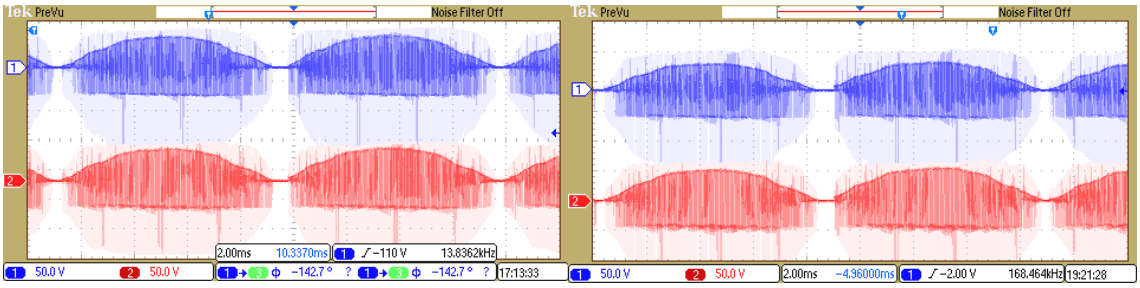


Figure 2.36: Primary winding voltages of the top (ch1) and bottom (ch2) fly-back transformers without the voltage balancing algorithm of the input capacitors working

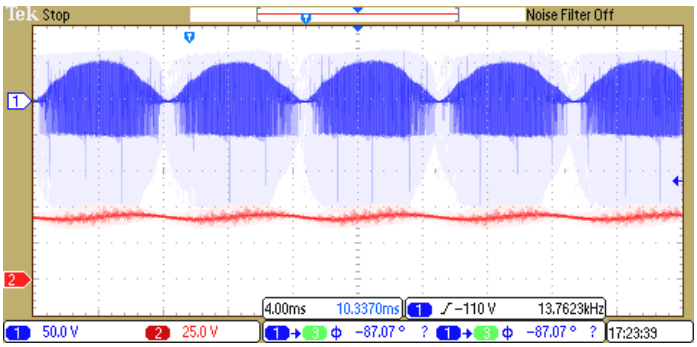


Figure 2.37: Top fly-back transformer primary voltage (ch 1) and the DC output voltage (ch 2) of the converter

2.11 Sparse AC/DC Converter

Conventional AC-to-DC rectification topology using non-linear devices, for example diode or thyristor bridges, causes unwanted input current harmonics and reactive power injection. This effectively deteriorates the voltage and current waveform of the utility grid. Owing to hard switched operation these converters have high switching loss, low frequency of operation, high device stress and are bulky in size.

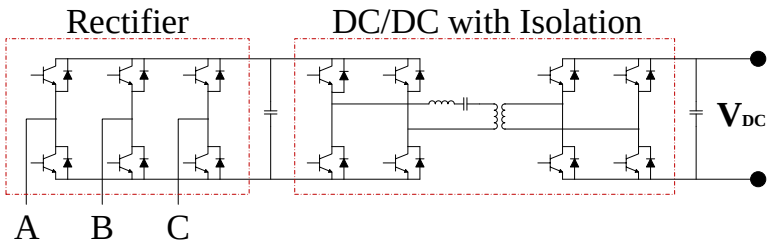


Figure 2.38: Circuit Schematic of a Conventional AC/DC with Isolation

To obtain galvanic isolation, a series connected DC/DC converter is added. Fig. 2.38 shows a circuit schematic of a conventional voltage source based AC/DC converter with galvanic isolation. It should be noted that 14 active switches are used in this topology.

A lot of research has been carried out in the last two decades towards to build high frequency link dc-dc and dc-ac converters [42]- [44]. Various AC-AC converters have also been proposed in the form of cycloconverters and matrix converters [45]- [46]. These converters are attributed with complicated controller design, limited buck and boost operation and has considerable amount of switching losses. A more recent invention, Dynamic Current (Dyna-C) Converter presents a novel multi-port, bi-directional, isolated, and compact SST technology based on a current-source topology with two power conversion stages where each stage is comprised of a standard current-source converter [47]-[50]. The convertor consists of much fewer number of devices thereby reducing the overall loss, complexity and size of the system. Furthermore, input/output regulation can be achieved on a switching cycle-by-cycle basis across all the phases which results in a smaller passive component size. However, it should be noted that it is primarily a hard-switched converter. In one of the transition, a freewheeling diode is reverse voltage commuted which leads to significant amount of reverse recovery loss. Further, as the current in the link inductor needs to be nearly constant, a considerably large magnetic component is required for power transfer. Fig. 2.39 shows an AC/DC version of this converter. As it can be seen, this topology requires 10 active switches to transfer bi-directional power.

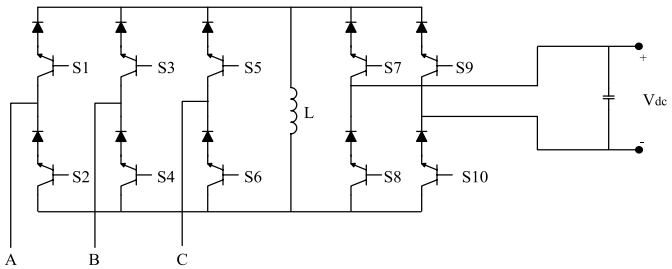


Figure 2.39: Circuit Schematic of AC/DC version of DynaC

Further complexity can be reduced by modifying the input stage of the rectifier to a simple three-switch rectifier topology, with reduced number of utilized active and passive components [51]. Fig. 2.40 shows the schematic of this converter. It should be noted that this converter lacks galvanic isolation.

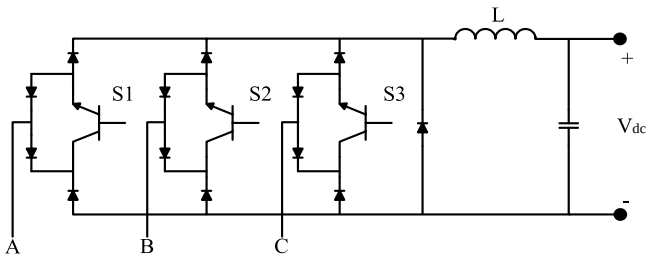


Figure 2.40: Three-Phase Three-Switch Buck Rectifier

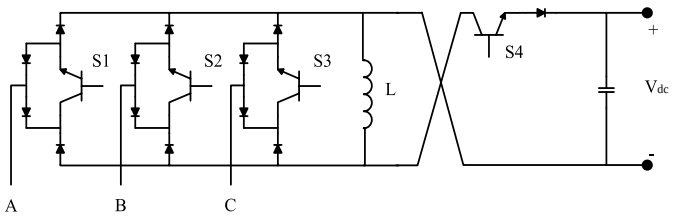


Figure 2.41: Circuit schematic of the proposed Sparse Dyna-C Rectifier

Fig. 2.41 shows the circuit schematic of the proposed topology. A discontinuous mode based non-linear controller has been proposed which results in zero current turn on and turn off both at the starting and ending of the switching cycle. The switching scheme is so arranged that the series diode always turns off at zero voltage thereby reducing the reverse recovery losses and device stresses. As the converter works under discontinuous mode, there are no freewheeling states.

This further makes sure that the diode never undergoes forceful reverse voltage commutation. Due to the inherent advantage of switch overlap, the turn on of all the switches (other than the first turn on which occurs at zero current), occur at zero voltage. These

features result in overall device loss and stress reduction. A detailed principle of operation, simulation and hardware test results and a converter/device based comparison has been shown in the later sections. Overall it uses four active switches to transfer power as compared to 14 switches in conventional VSC based rectifier and 10 switches in Dyna-C AC/DC converter.

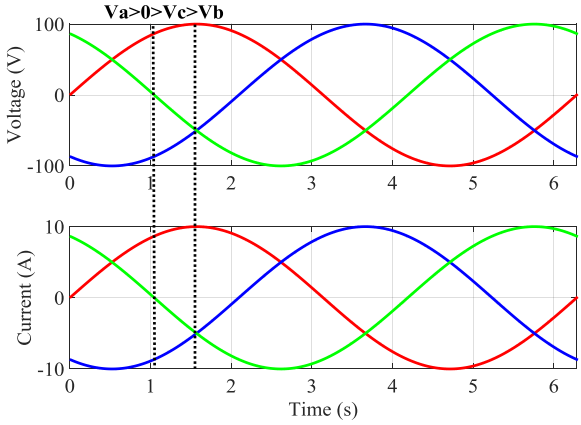


Figure 2.42: Three Phase Sinusoidal Input V-I waveform divided into six sectors where A=Red, B=Blue and C=Green. In this illustration, the current is leading the supply voltage.

2.11.1 Principle Of Operation

The principle of operation is explained in this subsection. The operating condition is for unity power factor under balanced input and output voltages. This makes voltage and current bear a linear relation (eg. Va/Ia = Vb/Ib = Vc/Ic = constant). The input voltage/current waveform can be divided into several 30° sectors. For this case, the sector where Va>0>Vc>Vb (which also means Ia>0>Ic>Ib) as shown in Fig. 2.42 is studied. For all other sectors, similar procedures can be applied for the desired goal of power transfer under soft switched condition. The switching operation can be divided into four modes of operation: -

Mode 1: Starting from the input side, the link is connected to the input lines having the highest line-line voltage (Va-Vb in this case). To achieve this, S1, S2 and S3 are turned on. It

should be noted that even though S3 is turned on, it would not conduct as the diode (connected in series with S3) is reverse biased. The main motive of turning on S3 is to provide a necessary switch overlap as will be explained in the next mode of operation. With S1 and S2 turned on, the link is charged till the average value of one of the line current (Ib in this case) is equal to the reference set by the controller. This turn-on duration can be calculated using the following formula: -

$$t_1 = \sqrt{\frac{2I_b L}{F(V_a - V_b)}};$$ where 'F' is the Switching Frequency of operation

Fig. 2.43 and 2.44 shows the active switches (in red) and the corresponding link voltage and current waveforms.

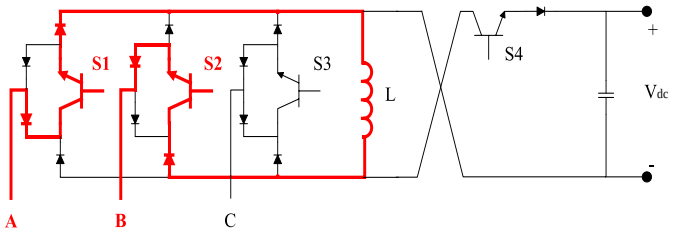


Figure 2.43: In Mode 1, S1 and S2 are the Active conducting switches. 'V_A-V_B' is applied to the Link Inductor 'L'

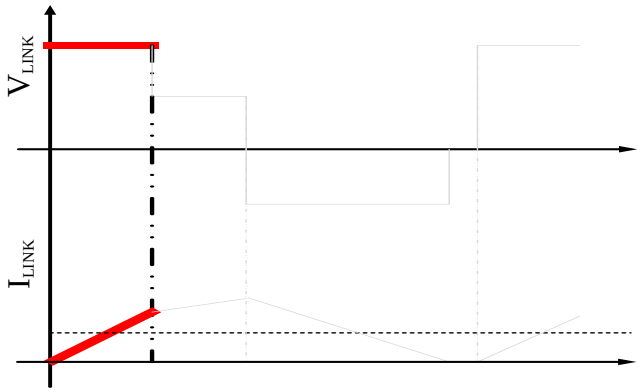


Figure 2.44: The Link voltage and current in Mode 1 (red)

Mode 2: After the end of the previous mode, the switch S2 is turned off. The link inductor current now naturally starts flowing through S1 and S3. The fact that S3 was turned on much

before (at the starting of Mode 1) it started conducting, this turn on occurs at near zero voltage. Further it should be noted that the turn off of series diode of S2 occurs under zero voltage thereby reducing the reverse recovery current and stress. However, the soft turn-on loss is non-negligible for Si-IGBT owing to its forward recovery loss [52]-[54]. SiC-MOSFET however shows a near zero loss in such transition. Switch S4 is also turned on (though it would not conduct as the series diodes are reverse biased) during this interval to facilitate zero voltage turn-on in the subsequent Mode. The turn-on duration of S1 and S3 in this mode is:-

$$t_2 = \frac{-b+\sqrt{b^2+4aI_c}}{2a}; \text{ where } b=\sqrt{\frac{2(V_a-V_b)I_b}{FL}} \text{ and } a=\frac{(V_a-V_c)}{2L}$$

Fig. 2.45 and 2.46 shows the active switches (in red) and the corresponding link voltage and current waveforms.

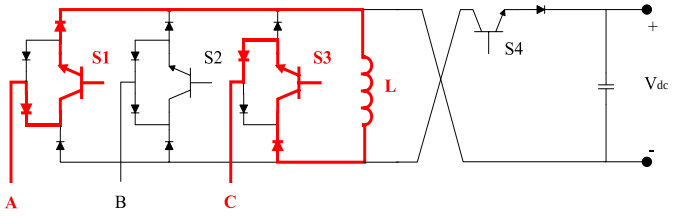


Figure 2.45: In Mode 2, S1 and S3 are the Active conducting switches. 'V_A-V_C' is applied to the Link Inductor 'L'

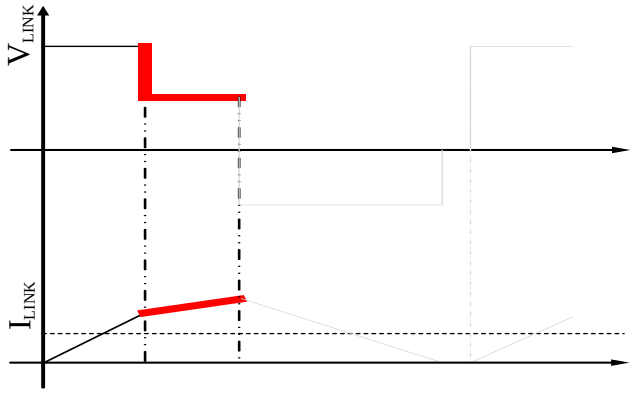


Figure 2.46: The Link voltage and current in Mode 2 (red)

Mode 3: In this mode, the switches S1 and S3 are turned off. This forces the link current to flow through S4 (which was turned on in mode 2). This transition occurs under zero voltage condition thereby reducing the losses. The turn off of series connected diodes of S1 and S3 are under zero voltage. This effectively reduces the device stress and reverses recovery losses.

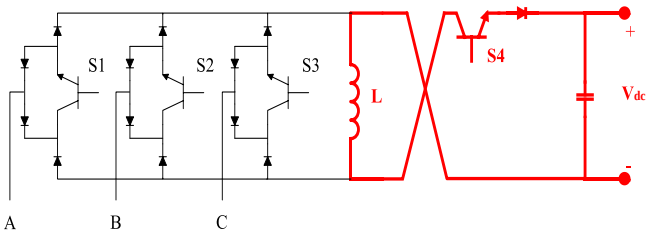


Figure 2.47: In Mode 3, S4 is the only Active conducting switches. '$-V_{DC}$' is applied to the Link Inductor 'L'

A negative voltage ($-V_{DC}$) appears across the inductor which causes the link current to reduce linearly. Fig. 2.47 and 2.48 shows the active switches (in red) and the corresponding link voltage and current waveforms.

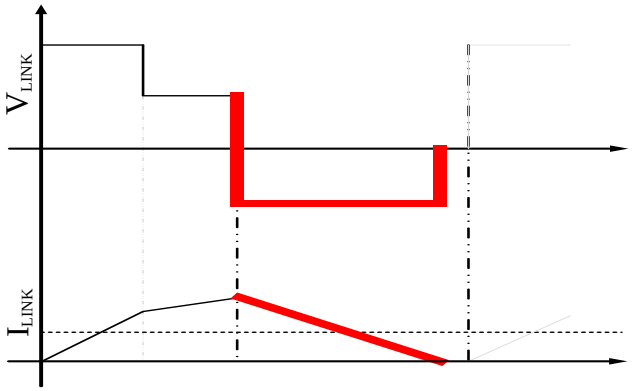


Figure 2.48: The Link voltage and current in Mode 3 (red)

Zero-Vector Mode: After the inductor current reaches zero value and all the switches are soft turned off, the system is allowed to rest till completion of switching time period. As this duration does not directly involve any power transfer, it is denoted as the zero-vector. This is similar to the freewheeling stage of a conventional current source converter apart from the

fact that both voltage and current in the inductor is zero during this mode for the proposed converter. Fig. 2.49 and 2.50 shows the circuit and waveforms during this Mode.

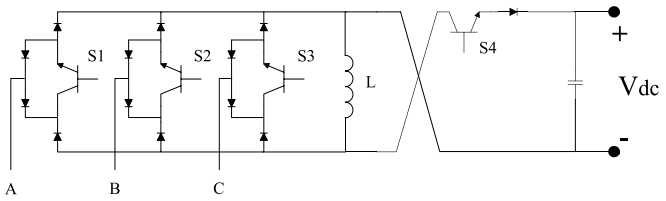


Figure 2.49: In Zero-Vector Mode all the switches are turned off

These modes of operations are repeated thereby transferring power from the input supply to the output grid. In the proposed design, the value of inductor is kept relatively small. This increases the value of conduction dI/dt for the same input voltage level. This results in making the pulsating current triangular as compared to square shaped pulses (in the conventional control scheme) eventually enabling zero current switching.

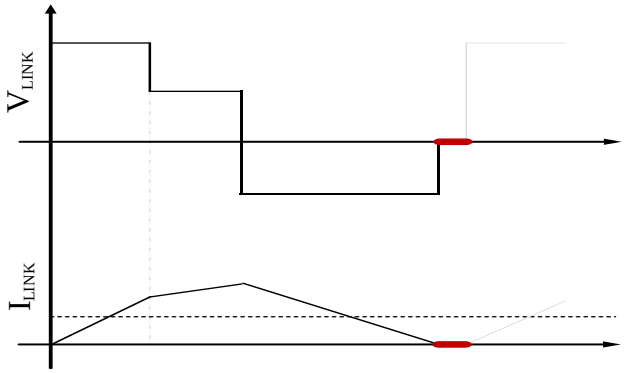


Figure 2.50: The Link voltage and current in Zero-Vector Mode

2.11.2 Device Based Efficiency Comparison

When a pre-turned on switch is forced to conduct a non-zero current, a voltage bump is witnessed. Detailed experimental results have been mentioned in [53]. Fig. 2.51 clearly shows the non-negligible voltage bump. This occurs owing to the forward recovery of the IGBT. This voltage bump is not witnessed when SiC-MOSFET is used as the primary switch

instead of Si-IGBT. Fig. 2.52 shows a typical behavior. It can be seen that voltage bump has been eliminated. This results in significant reduction of switching losses. This makes this transition closer to ideal soft switch. To completely comprehend the losses in the switches, a test circuit was made to evaluate the devices under ZCS turn off. Fig. 2.53 shows a typical zero-current turn-off. As it can be seen from the figure, the overall loss during this transition is negligible.

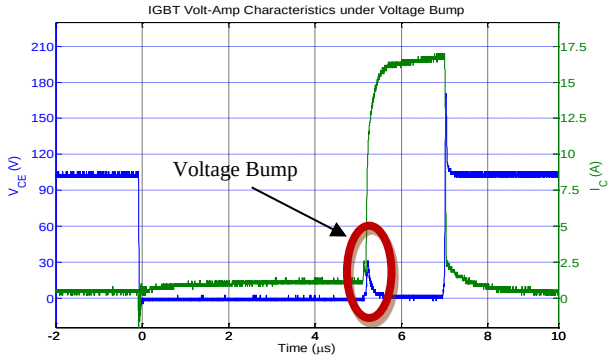


Figure 2.51: Device Test under typical switch overlap condition for Si-IGBT.

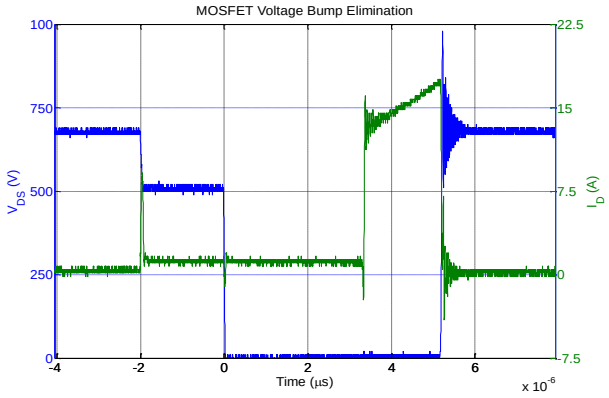


Figure 2.52: Device Test under switch overlap condition for SiC-MOSFET

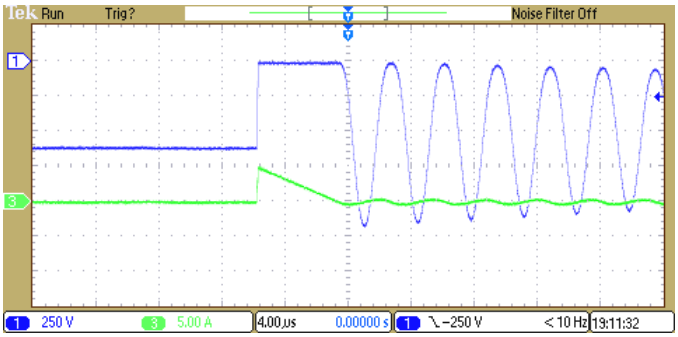


Figure 2.53: Current Switch undergoing ZCS: Diode Voltage (Blue) and Current (Green)

Various switching and conduction loss data collected from a prior characterization study [52]-[54] has been tabulated and fed to a look-up table in PLECS. The system has been simulated for 100kW and 480V supply. The estimated peak inductor current is 400A. The switching frequency is set to 20 kHz. Tab. II shows the estimated switching and conduction losses for various sets of devices in the proposed topology. The main aim of this study is to choose the right pair of devices for this converter. As expected, SiC-MOS (owing to reduction in hard and soft switching losses) + SiC-JBS Diode (owing to reduction in conduction losses) showed significant reduction of overall losses. However, it should be noted that SiC-MOS and low cost Si-PiN Diode also showed comparable efficiency owing to reduced reverse recovery losses.

Table 2: Device based loss comparison of Dyna-C under DCM

Loss	Si-IGBT + Si-Diode	Si-IGBT + SiC JBS Diode	SiC MOS + Si-Diode	SiC MOS + SiC JBS Diode
Conduction	1508 W	1751 W	1580 W	1799 W
Switching	1312 W	1055 W	649 W	421 W
Total	2820 W	2806 W	2229 W	2220 W

2.11.3 Prior Art Comparison

The prior arts shown in Fig. 2.38 and 2.39 have also been analyzed with SiC-MOS and Si-PiN Diode as the primary switching devices under the specifications mentioned in the previous section. Tab. 3 shows the various advantages in terms of switch reduction,

conduction, switching and overall losses of the proposed converter as compared to the previously mentioned prior arts. Prior art 1 and 2 corresponds to the converters shown in Fig. 2.38 and 2.39.

Table 3: Topology based Component/Loss Comparison

Parameters	Prior Art 1	Prior Art 2	Proposed Topology
Active Switches	14	10	4
Passive Switches	14	10	13
Conduction Loss	1231	1603	1580
Switching Loss	1569	854	649
Total Loss	2800	2457	2065

As expected, owing to reduced diode loss and inherent soft-switching, the proposed topology is significantly more efficient.

2.12 Conclusions

This chapter shows the operation principle, simulation results and experimental validation of a current source inverter based multi-port solid state transformer. The battery interface circuit with the conventional circuit adds an interesting feature of adding renewable energy sources to the existing power network. Renewable energy sources with DC output terminal can be connected to the battery terminal via suitable power converter. The extracted energy can be stored in the battery bank and the excess amount can be fed directly to the grid. The stored energy can also be fed to the grid in case of peak power demand. Thus the new era of green energy can be accelerated. In this case an experimental prototype of 2kW has been built to verify the operation of the system. From the experimental results presented in this chapter it is clear that the solid state transformer operates as expected.

The topology for replacing the line frequency transformer with the high frequency one in railway traction drive can be implemented easily with the available 6.5kV IGBTs. There are reverse blocking IGBTS available in the market which can be used in place of the series

connected IGBT and diode. This will reduce the device count further compared to the conventional voltage source converter based topology.

The converter topology is implemented on a laboratory prototype with three cascaded sections. This can easily be extended for real application with more number of cascaded sections. The report also discusses about the voltage balancing of the input side series connected capacitors with non-identical inductors connected to the system.

CHAPTER 3

PARTIAL RESONANT LINK CONVERTER SYSTEM

3.1 Introduction

Conventional AC-to-DC rectification topology using non-linear devices, for example diode or thyristor bridges, causes input current harmonics and reactive power. This effectively deteriorates the voltage and current waveform of the utility grid. Owing to hard switched operation these converters have high switching loss, low frequency of operation, high device stress and are bulky in size. A lot of research has been carried out in the last two decades towards high frequency link dc-dc and dc-ac converters [55]- [57]. Various AC-AC converters have also been proposed in the form of cycloconverters and matrix converters [58]- [59]. These converters are attributed with complicated controller design, limited buck and boost operation, considerable amount of switching losses and non-favorable frequency changing operation. Early soft switching based high frequency converters used Pulse Density Modulation (PDM) as the mean of control [60]. It was noticed that PDM tends to reduce system response and deteriorates power quality due to the usage of integral pulses of current. A resonant DC-Link converter [61], in which a desired charge is drawn from each phase of a power-supply to charge an energy storage element and then the stored energy is fed to the output of the same. Reference [62] proposes a quasi-resonant high frequency link topology with twelve unidirectional switches. As it is built for variable speed drives application, not much importance was given to the current harmonics and power factor control. Reference [63] proposes an improved version using 12 bi-directional switches. Though it has more number of switches, it improves the power density and includes power factor control. The

fact that it uses more number of devices, has 16 modes of operation for power transfer and lesser option for reduction of conduction loss (owing to the usage of AC-switch), gives us a chance to come up with a more cost effective and simpler topology. The work presented in this chapter therefore proposes a modified high frequency link topology which uses 12 unidirectional switches to transfer power from one grid to another. Further complexity can be reduced by modifying the input stage of the buck rectifier to a simple three-switch rectifier topology, with reduced number of utilized active and passive components. An amalgamation of partial resonant link and reduced switched rectifier topology has been presented. The proposed high frequency link topology uses 4 active switches to transfer power from one grid to another. As diode reverse recovery is not an issue, a diode with low conduction loss can be chosen. This gives more freedom on device selection. Usage of RB-IGBT [64] will further reduce the size and conduction loss of the converter.

3.2 Proposed Bidirectional Soft-Switched Sparse AC/AC

Fig. 3.1 shows the schematic of the proposed topology. Each leg of the topology consists of two series connected IGBT and Diode (or RB-IGBT). The converter operates by first charging the inductor from the input supply and then discharging it to the output grid. To draw harmonic-free current from the input, the ratio of the charge drawn from each input phase must be equal to the ratio of the absolute value of the sinusoidal reference of the input phase currents. To ensure this, we need current references for both the input and output. If the output power requirement is known, the output current reference can be set likewise. A simple input current reference predictor can then be implemented so as to minimize the error of the measured output current from the reference. Fig. 3.2(a) shows a typical controller diagram. The switching scheme has been divided into eight subsystems.

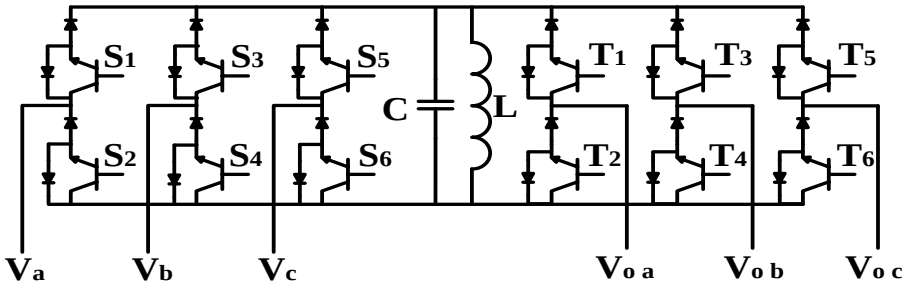
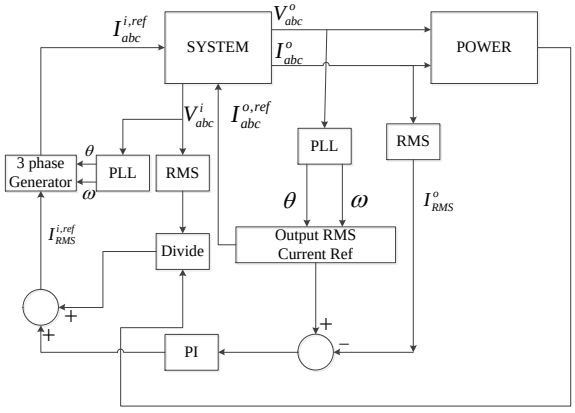
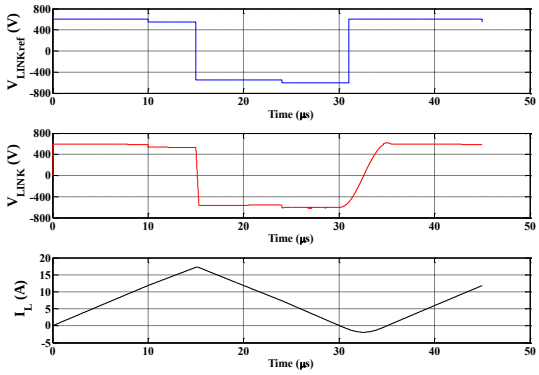


Figure 3.1: Circuit Schematic of the proposed topology

Fig 3.2(b) shows a typical reference link voltage, actual link voltage and inductor current waveform.



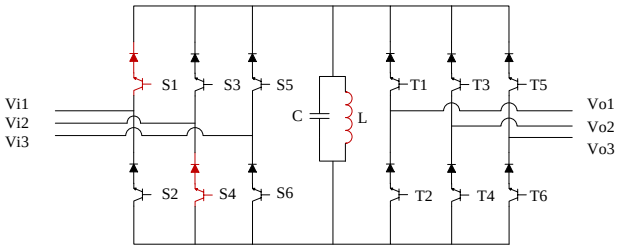
(a)



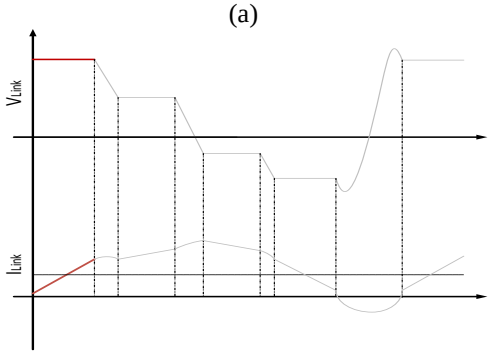
(b)

Figure 3.2 (a): Controller Diagram, (b): Link reference voltage, Link Voltage and Inductor Current

Subsystem 1: Starting from the input side, the link is connected to the input lines having the highest voltage via switches to charge it in the positive direction. The link is charged till the average value of one of the line current is equal to the reference set by the controller. The switches are then turned off. Due to the presence of Capacitor 'C', the voltage across the switch during turn – off is close to zero. This is known as Capacitor buffered soft turn-off. The only loss incurred in the switch would be due to the characteristics IGBT tail bump. This causes some switching loss but is still much less compared to a generic hard-turn off. This also negates the need of additional snubbers in the circuit. If Si-IGBTs are replaced by SiC-MOSFETs, this loss can be considerably mitigated. Fig. 3.3(a) and (b) shows the active switches and the corresponding LC-link voltage and current waveforms.



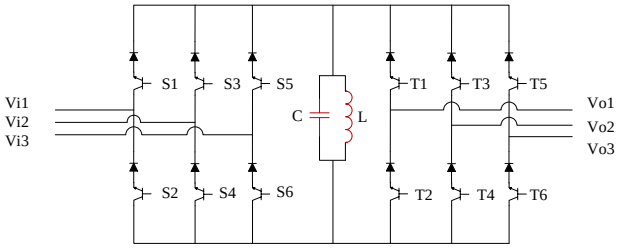
(a)



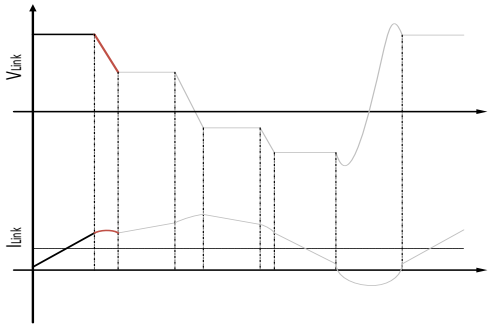
(b)

Figure 3.3: (a) In Subsystem 1, S1 and S4 are the Active conducting switches. 'Vi1-Vi2' is applied to the Link Inductor 'L'; (b) The red portion shows the locus of the Link Voltage during subsystem 1

Subsystem 2: After the switches are turned off, the switch corresponding the second highest line-line voltage are turned on. It should be noted that even though they are turned on, they would still not conduct as the link voltage at present is larger than the second highest line-line voltage. Thus, making the series diode reverse biased. In this subsystem, the link just partially resonates till the link voltage becomes equal to the voltage of the input pair which has the second highest value. Fig. 3.4(a) and (b) shows the active switches and the corresponding LC-link voltage and current waveforms.



(a)

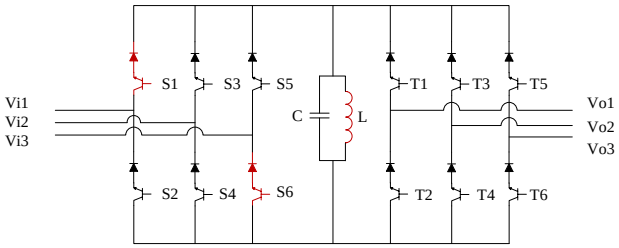


(b)

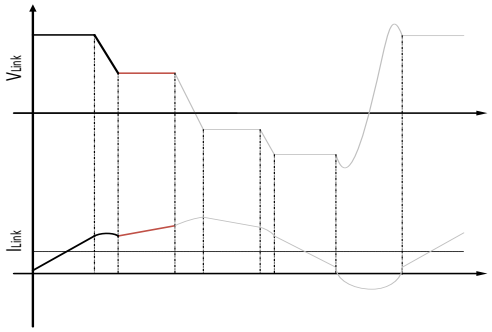
Figure 3.3: (a) In Subsystem 2, the Link 'LC' partially resonated; (b) The red portion shows the locus of the Link Voltage during subsystem 2

Subsystem 3: At this point, the series diodes are naturally turned on and the link once again continues to get charged from the input section. This results in zero-voltage turn on. The only loss incurred in this operation (provided Si-IGBT is used as the switch) is due to a unique

voltage bump that appears across an IGBT when a non-zero current is forced to pass through a pre-turned on device. This causes some switching loss but is still much less compared to a generic hard-turn on. If Si-IGBTs are replaced by SiC-MOSFETs, this loss can be considerably mitigated. This is continued till the line current becomes equal to the reference current and then the switches are turned off. Fig. 3.5 (a) and (b) shows the active switches and the corresponding LC-link voltage and current waveforms.



(a)

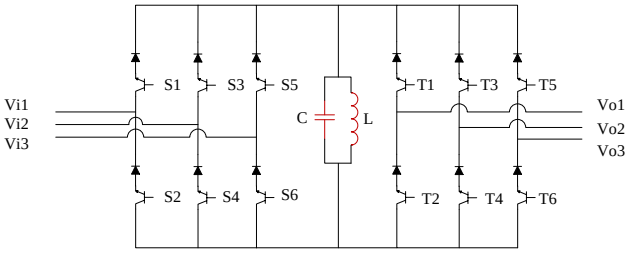


(b)

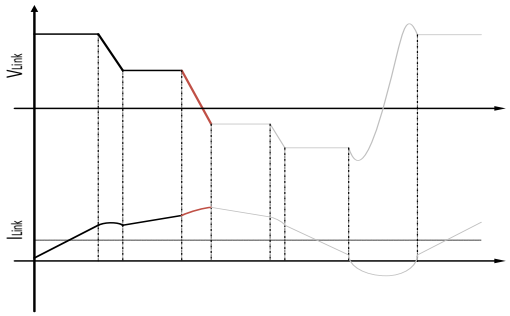
Figure 3.4: (a) In Subsystem 3, S1 and S6 are the Active conducting switches. 'Vi1-Vi3' is applied to the Link Inductor 'L'; (b) The red portion shows the locus of the Link Voltage during subsystem 3

Subsystem 4: After the switches are turned off, the switches corresponding the negative of second highest voltage of the output is turned on. Like Subsystem 2, even though the switches are turned on, they would not conduct instantaneously as the link voltage at present is larger than the negative of second highest line-line voltage of the output. Thus, making the

series diode reverse biased. In this subsystem, the link resonates till the link voltage becomes equal to the negative of the second highest voltage pair of the output grid. Fig. 3.6(a) and (b) shows the active switches and the corresponding LC-link voltage and current waveforms.



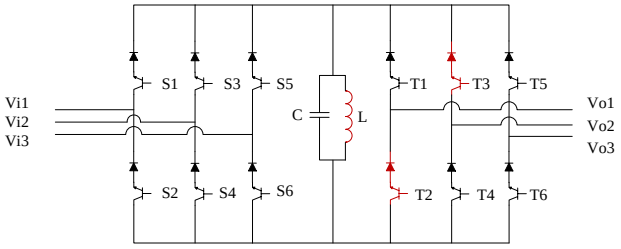
(a)



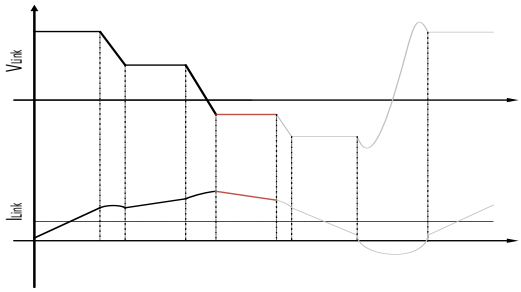
(b)

Figure 3.5: (a) In Subsystem 4, the Link 'LC' partially resonated; (b) The red portion shows the locus of the Link Voltage during subsystem 4

Subsystem 5: The diode now naturally turns on and a negative voltage is applied to the link thereby discharging the stored energy from the link to the output grid. This is continued till the line current becomes equal to the reference current and then the switches are turned off. Both turn-on and turn-off is soft as in the above odd numbered subsystems. Fig. 3.7(a) and (b) shows the active switches and the corresponding LC-link voltage and current waveforms.



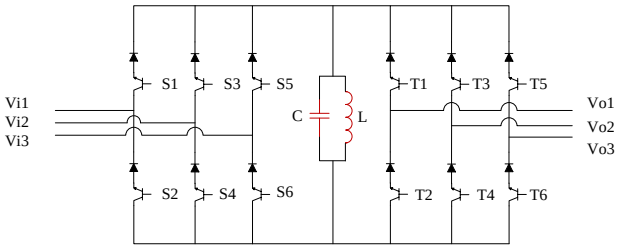
(a)



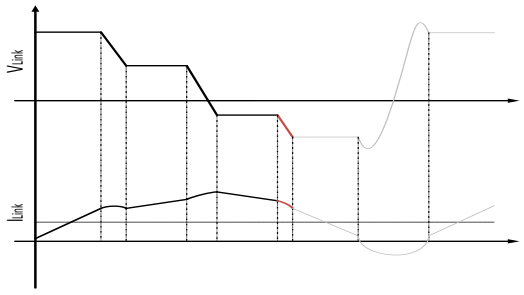
(b)

Figure 3.6: (a) In Subsystem 5, T2 and T3 are the Active conducting switches. Negative of 'Vo1-Vo2' is applied to the Link Inductor 'L'; (b) The red portion shows the locus of the Link Voltage during subsystem 5

Subsystem 6: The switches corresponding to the highest negative voltage of the output pair are turned on. The link partially resonates till the link voltage becomes equal to the highest negative voltage of the output pair. Fig. 3.8(a) and (b) shows the active switches and the corresponding LC-link voltage and current waveforms.



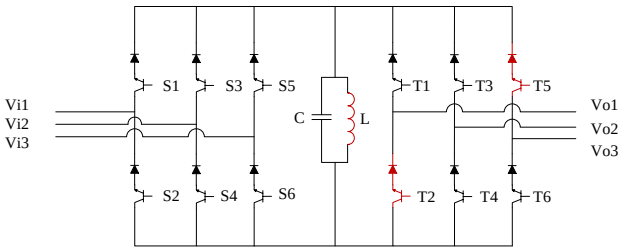
(a)



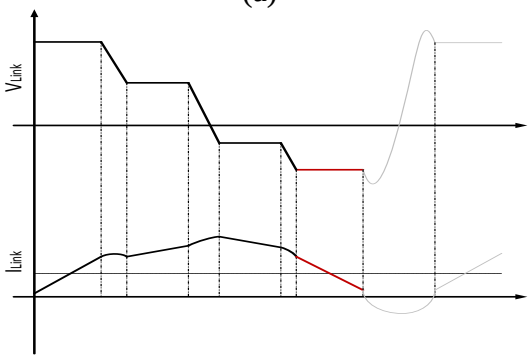
(b)

Figure 3.7: (a) In Subsystem 6, the Link 'LC' partially resonated; (b) The red portion shows the locus of the Link Voltage during subsystem 6

Subsystem 7: Corresponding diodes are now naturally turned on and the link continues to discharge. This is continued till the line current becomes equal to the reference current set by the controller. Fig. 3.9(a) and (b) shows the active switches and the corresponding LC-link voltage and current waveforms.



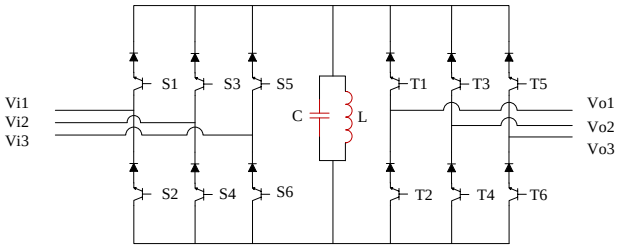
(a)



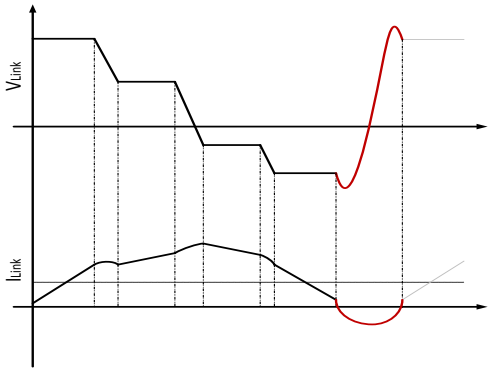
(b)

Figure 3.8: (a) In Subsystem 7, T2 and T5 are the Active conducting switches. Negative of 'Vo1-Vo3' is applied to the Link Inductor 'L'; (b) The red portion shows the locus of the Link Voltage during subsystem 7

Subsystem 8: The link partially resonates back to positive voltage. In this subsystem unlike the previous ones, the link voltage needs to be monitored by sensors. The link continues to resonate till the link voltage is equal to the highest line-line voltage of the input grid. At this point of time, subsystem 1 criterion is satisfied and the input phases continue to power the link. Fig. 3.10(a) and (b) shows the active switches and the corresponding LC-link voltage and current waveforms.



(a)



(b)

Figure 3.9: (a) In Subsystem 6, the Link 'LC' partially resonated; (b) The red portion shows the locus of the Link Voltage during subsystem 8

These sets of operations are repeated thereby transferring power from the input supply to the output grid.

3.3 Hardware Test

A low power (3kVA) hardware prototype has been built. The converter hardware has been tested for proof of concept and verification of soft switching intervals. Tab. 1 shows the specifications of the test.

Table 1: Hardware Specifications

Specifications	Value
Nominal Input / Output Grid Voltages	208V (L-L,rms)
Reference Input Current	25A (rms)
Link Inductance	50µH
Link Capacitance	0.15µF

Fig. 3.11 shows the link voltage and current when the output voltages are close to crossover (approximately equal in voltage). Fig. 3.12 shows a general link voltage and current profile in the boost operation. Fig. 3.13 shows the input phase voltage and current when the controller is simplified to maximum phase to phase power transfer. Fig. 3.14 shows the input phase (A) voltage and current with harmonic free controller algorithm.

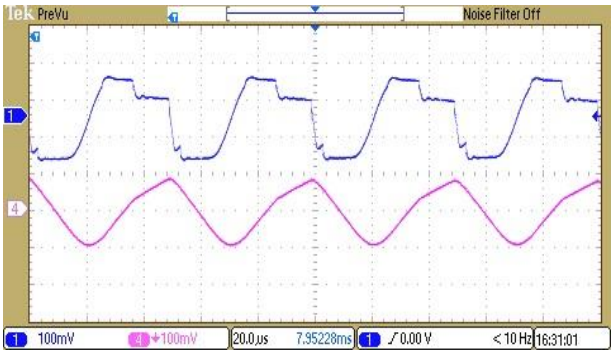


Figure 3.10: Link Voltage and current during voltage crossover

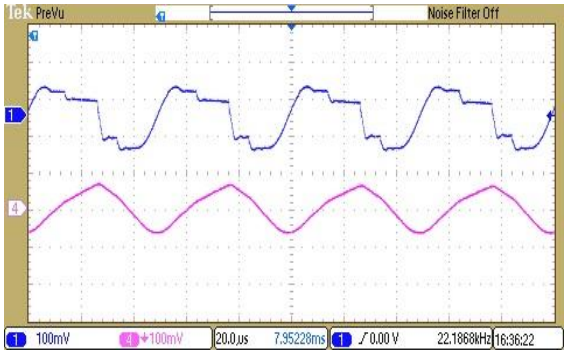


Figure 3.11: Link Voltage and Current during boost operation

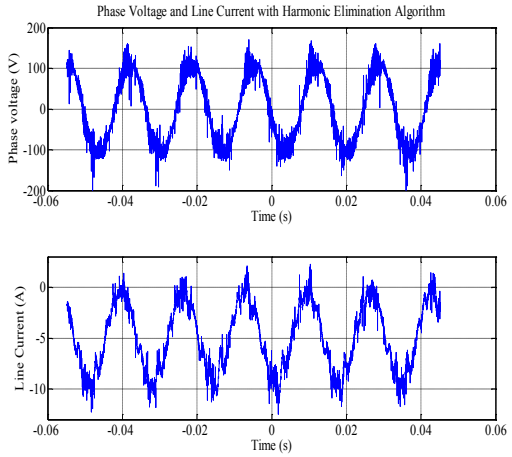


Figure 3.13: Phase Voltage and Current with simplified controller

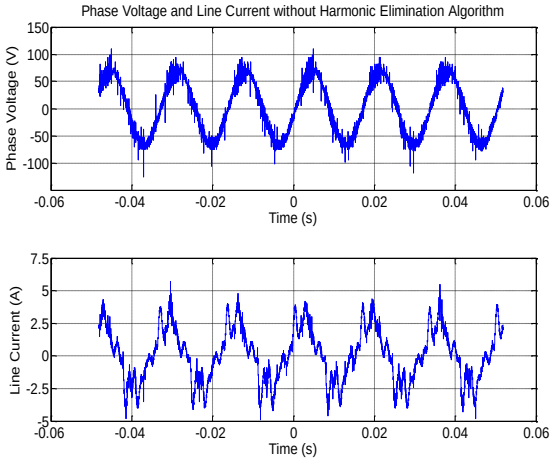


Figure 3.14: Phase Voltage and Current with non-linear controller

3.4 Device Performance and Selection

This section deals with the specific device losses incurred in this converter. Fig. 3.15 shows a conventional hard turn off of the device which incurs huge loss during transition. Fig. 3.16 shows the soft switching characteristics specific to this topology. It clearly shows the distinct current tail bump when the system undergoes ZVS. Comparing both the figures, it is easy to say that with this topology, there will be a considerable amount of reduction of switching loss.

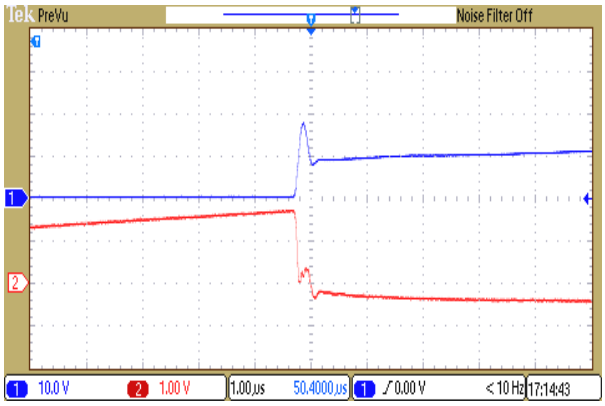


Figure 3.12: Switch Characteristics during Hard Transition

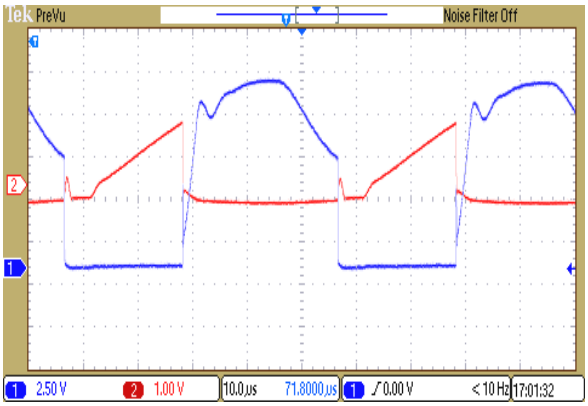


Figure 3.13: Switch Characteristics during Soft Transition

When a pre-turned on switch is forced to conduct a non-zero current, a voltage bump is witnessed. Detailed experimental results have been mentioned in [65]. Fig. 3.17 clearly shows the non-negligible voltage bump. This occurs owing to the forward recovery of the IGBT. This voltage bump is not witnessed when SiC-MOSFET is used as the primary switch instead of Si-IGBT. Fig. 3.18 shows a typical behavior. It can be seen that voltage bump has been eliminated. This results in significant reducing of switching losses. This makes this transition closer to ideal soft switch.

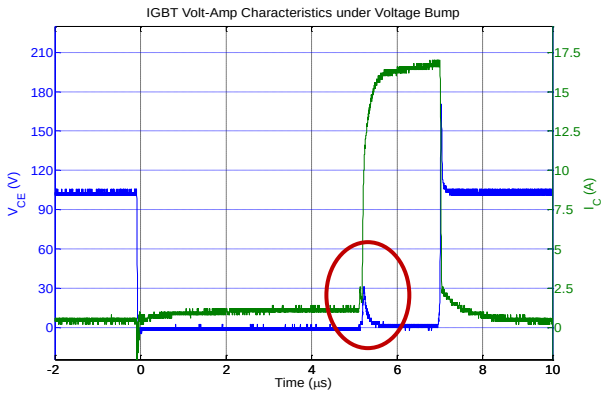


Figure 3.17: Forward recovery of Si-IGBT

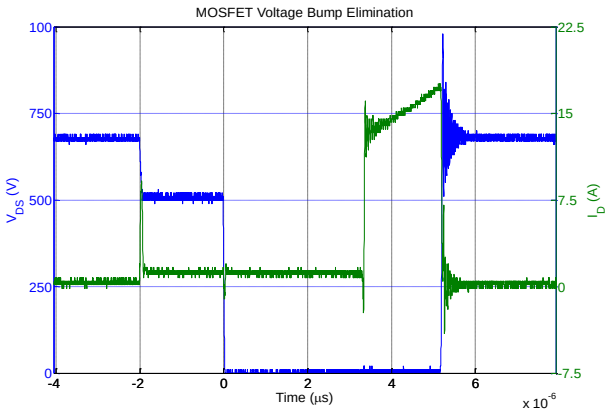


Figure 3.18: Soft turn on of SiC-MOSFET

3.5 Three-Phase Four-Switch Soft Switched Rectifier with High Frequency Isolation

This part of the chapter investigates a soft-switching partial-resonant link AC/DC converter. The proposed converter uses 4 active switches and overcomes the various shortcomings of conventional resonant AC Link schemes such as the need for a four-quadrant ac switch. The switching operations occur at zero voltage instants thus lowering the switching losses. The input current is harmonic free. It can perform buck and boost operations and provides galvanic isolation. As the converter requires less number of switches and operates at high switching frequency, it offers both improved performance and considerable reduction of volume, weight and cost. A prototype converter system has been built and tested. The topology is expected to offer compact, fast, efficient and inexpensive solution to the present AC/DC power conversion requirements.

3.5.1 Proposed topology

Fig. 3.19 shows the schematic of the proposed topology. Each leg of the topology consists of one IGBT and four Diodes. The converter operates by first charging the inductor from the input supply and then discharging it to the output grid. If the output power requirement is known, the input current reference can be set likewise. A simple input current reference predictor can then be implemented so as to minimize the error of the measured output power from the reference. Fig. 3.20 shows a typical controller for this application.

The principle of operation is explained in this sub-section. The operating condition is for unity power factor under balanced input voltages. This makes voltage and current bear a linear relation (eg. $V_a/I_a = V_b/I_b = V_c/I_c$ = constant). The input voltage/current waveform can be divided into several 30^0 sectors. For this case, the sector where $V_a>0>V_c>V_b$ (which also

means $I_a>0>I_c>I_b$) is studied. For all other sectors, similar procedures can be applied for the desired goal of power transfer under soft switched condition can be achieved.

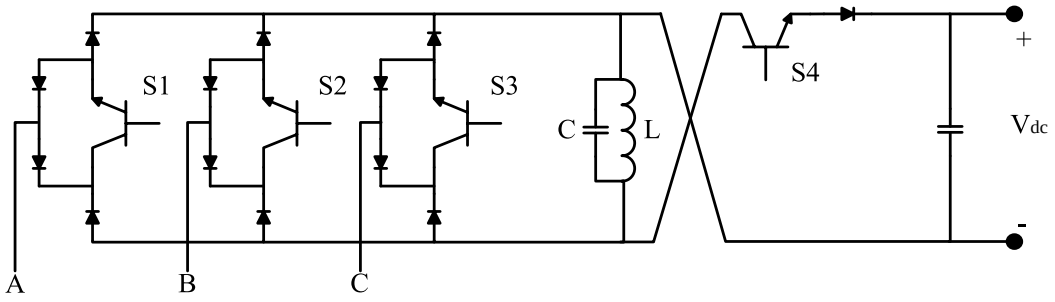


Figure 3.19: Circuit Schematic of the proposed topology

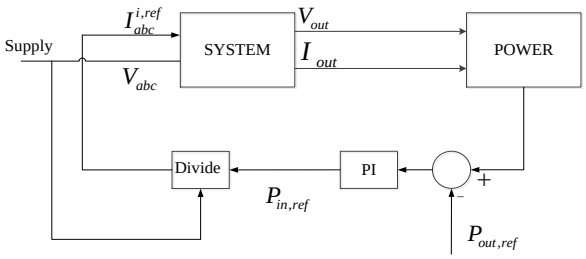


Figure 3.20: Controller - Input Current Reference Predictor

The switching operation can be divided into six modes of operation: -

Mode 1: Starting from the input side, the link is connected to the input lines having the highest line-line voltage (V_a-V_b in this case) via appropriate switches to charge it in the positive direction. The link is charged till the average value of one of the line current (I_b in this case) is equal to the reference set by the controller. The switches are then turned off. Due to the presence of Capacitor 'C', the voltage across the switch during turn – off is close to zero and the value of dv/dt is limited by the resonant sinusoidal of LC. This is known as Capacitor buffered soft turn-off. The only loss incurred in the switch would be due to the characteristics IGBT tail bump as mentioned in [66]. This causes noticeable switching loss

but not-comparable to a generic hard-turn off. This also negates the need of additional snubbers in the circuit. If Si-IGBTs are replaced by SiC-MOSFETs, this loss can be considerably mitigated [67]. Fig. 3.21 and 3.22 shows the active switches (in red) and the corresponding LC-link voltage and current waveforms.

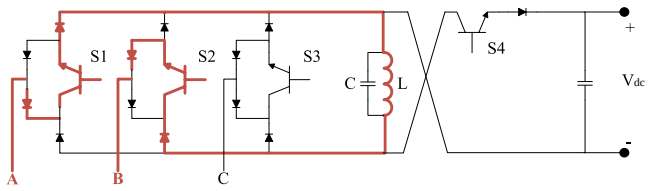


Figure 3.21: In Mode 1, S1 and S2 are the Active conducting switches. 'V_A-V_B' is applied to the Link Inductor 'L'

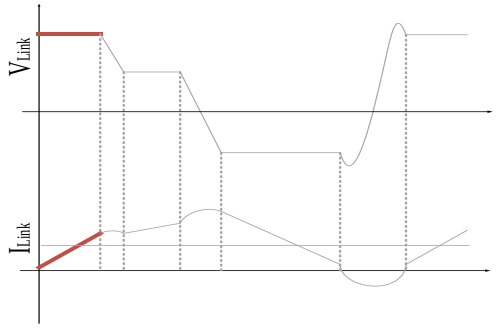


Figure 3.22: Link Voltage and Inductor Current in Mode 1

Mode 2: After the switches are turned off, the switch corresponding the second highest line-line voltage are turned on (V_a-V_c in this case). It should be noted that even though they are turned on, they would still not conduct as the link voltage at present is larger than the second highest line-line voltage. Thus, making the series diode reverse biased. In this subsystem, the link just partially resonates till the link voltage becomes equal to the voltage of the input pair which has the second highest value. Fig. 3.23 and 3.24 shows the active switches (in red) and the corresponding LC-link voltage and current waveforms.

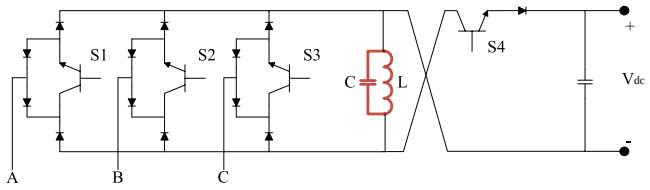


Figure 3.23: In Mode 2, the Link 'LC' resonates partially

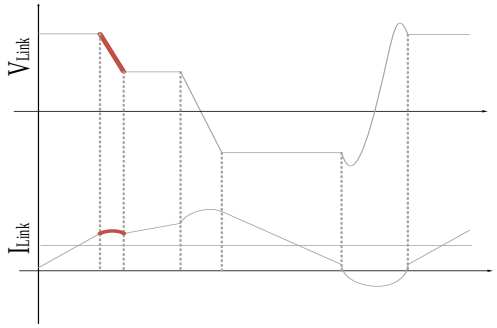


Figure 3.24: Link Voltage and Inductor Current in Mode 2

Mode 3: At this point, the series diodes are naturally turned on and the link once again continues to get charged from the input section. This results in zero-voltage turn on. The only loss incurred in this operation (provided Si-IGBT is used as the switch) is due to a unique voltage bump that appears across an IGBT when a non-zero current is forced to pass through a pre-turned on device [67]. This causes noticeable switching loss but not-comparable to a generic hard-turn on. If Si-IGBTs are replaced by SiC-MOSFETs, this loss can be considerably mitigated. This is continued till the line current (I_c in this case) becomes equal to the reference current and then the switches are turned off. Fig. 3.25 and 3.26 shows the active switches (in red) and the corresponding LC-link voltage and current waveforms. It should be noted that under balanced condition, if references of I_b and I_c are met, this automatically ensures I_a to meet its set reference.

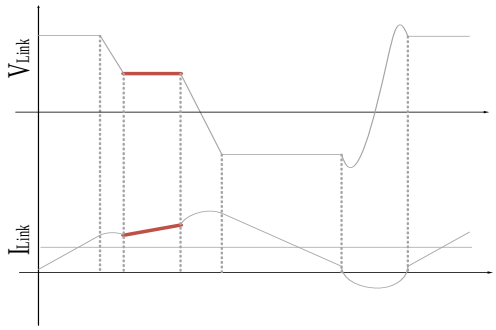


Figure 3.25: In Mode 3, S1 and S3 are the Active conducting switches. 'V_A-V_C' is applied to the Link Inductor 'L'

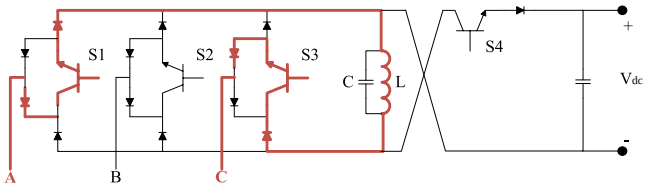


Figure 3.26: Link Voltage and Inductor Current in Mode 3

Mode 4: After the switches are turned off, the switch in series with the output is turned on. Like Subsystem 2, even though the switches are turned on, it would not conduct instantaneously as the link voltage at present is larger than the negative of the output voltage. Thus, making the series diode reverse biased. In this subsystem, the link resonates till the link voltage becomes equal to the negative of the output grid voltage. Fig. 3.27 and 3.28 shows the active switches (in red) and the corresponding LC-link voltage and current waveforms.

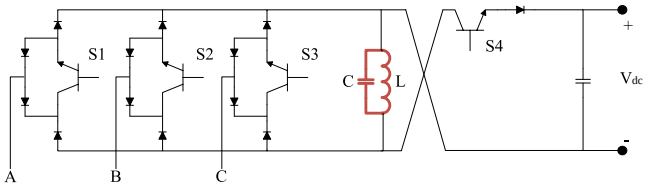


Figure 3.27: In Mode 4, the Link 'LC' resonates partially

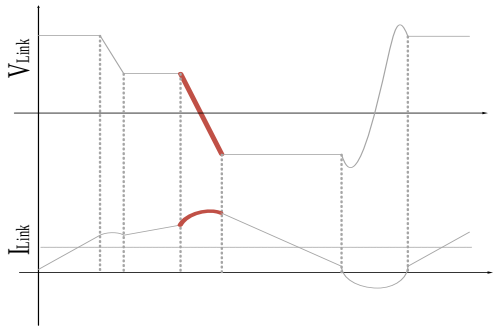


Figure 3.28: Link Voltage and Inductor Current in Mode 4

Mode 5: Once the link voltage is equal to the negative of output DC voltage, the link starts to discharge its energy to the output grid. Fig.3.29 and 3.30 shows the active switches (in red) and the corresponding LC-link voltage and current waveforms.

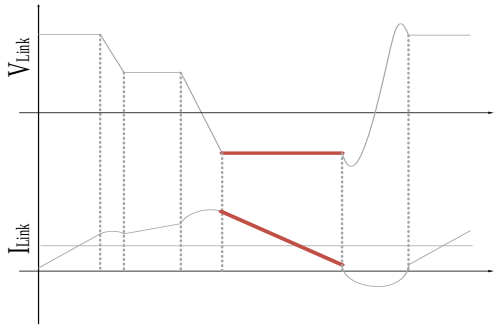


Figure 3.29: In Mode 5, T is the Active conducting switches. Negative of 'Vdc' is applied to the Link Inductor 'L'

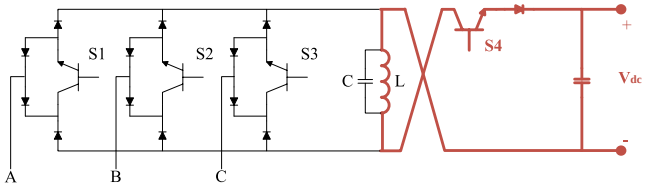


Figure 3.30: Link Voltage and Inductor Current in Mode 5

Mode 6: after the output current/voltage reference has been met, all the switches are turned off and the link is allowed to resonate back to the maximum line-line input voltage. These

sets of operations are repeated thereby transferring power from the input supply to the output grid.

3.5.2 Hardware Test

A low power (3kVA) hardware prototype has been built. The converter hardware has been tested for proof of concept and verification of soft switching intervals. Fig. 3.31 shows a typical link voltage and current profile when the converter is acting in boost (rectifier) operation.

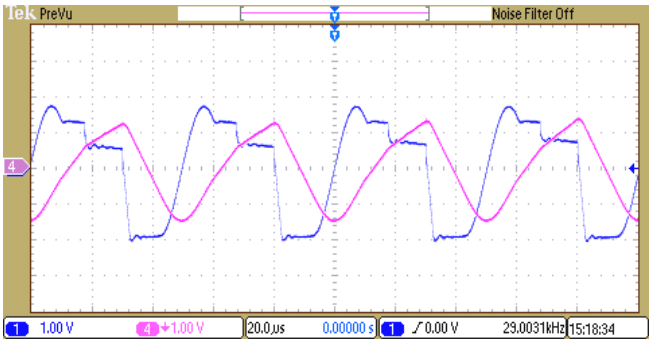


Figure 3.31: Snapshot of Link Voltage (blue) and Inductor Current (purple)

3.5.3 Prior Art Comparison

The prior arts shown in Fig. 2.38 and 2.39 (with parallel Capacitor) have also been analyzed with SiC-MOS and Si-PiN Diode as the primary switching devices under the specifications mentioned in the previous section. Tab. 2 shows the various advantages in terms of switch reduction, conduction, switching and overall losses of the proposed converter as compared to the previously mentioned prior arts. Prior art 1 and 2 corresponds to the converters shown in Fig. 2.38 and 2.39.

Table 2: Topology based Component/Loss Comparison

Parameters	Prior Art 1	Prior Art 2	Proposed Topology
Active Switches	10	3	4
Passive Switches	10	12	13
Conduction Loss	1651	1294	1488
Switching Loss	796	1054	577
Total Loss	2447	2348	2065

3.6 Conclusions

The proposed topology can be used in various AC/AC, AC/DC, DC/DC and DC/AC applications. The main switching losses in this topology are conduction loss; turn off tail current losses of IGBT and turn-on voltage bump loss. Specific diodes with low conduction losses can be used and IGBTs can be replaced with SiC-MOSFETs. The link inductor can be replaced with a transformer to provide galvanic isolation. This makes this converter topology sparse, soft-switched and galvanic isolated rectifier with buck-boost capability. The topology is expected to offer compact, fast, efficient and inexpensive solution to the present AC/DC power conversion requirements.

CHAPTER 4

PERFORMANCE COMPARISON, CHARACTERIZATION AND DESIGN OPTIMIZATION OF CURRENT SWITCH

4.1 Introduction

Diode reverse recovery is notorious for increasing switching losses in current stiff converters. A lot of effort has been made over the years to mitigate the diode reverse recovery losses. However, there exists ways to use this feature to achieve zero-voltage current transition in the same converter thereby, mitigating the loss incurred as compared to hard switched turn off. Significant research works have been carried out over the last couple of years on converters based on soft switching techniques. The typical zero voltage switching (ZVS) has characteristics been well studied and presented in. Most of the available devices are designed for hard switching applications. Sufficient data is not available on the device behavior for Reverse Voltage Blocking or current switch configuration (IGBT/MOSFET in series with diode). The current switch has found its application in current source based converters where thyristors with external commutation circuits are typically used, albeit at low switching frequency. As most available devices are designed for hard switching applications, very little data is available in the literature on device behavior under Current Switch (series connected switch and diode) based soft switching conditions. The application of current-switch inverters such as the High Frequency Link inverter is being actively considered by many manufacturers. In this part of the work, an attempt has been made to demonstrate the behavior of several devices working under reverse voltage commutation, hard switched and switch overlap condition at various voltage and current levels. A test circuit has been built and tested with various series connected device combinations, viz. (a) Si-IGBT and Si-Diode, (b) Si-

IGBT and SiC-JBS Diode, (c) SiC-MOSFET and SiC-JBS Diode, (d) Custom Made Package, and (e) RB-IGBTs. The forward characteristics of the devices were tested using a Curve Tracer. The switching and conduction loss data was then fed to a look up table based circuit simulator (PLECS). The topology under study is the Partial Resonant High Frequency Link Converter. All the above mentioned switching characteristics can be witnessed in this converter. The main motivation of the work is to find the best combination of devices to minimize losses and device stress.

4.2 Reverse Voltage Commutation

Reverse Voltage Commutation occurs when the voltage polarity of a conducting diode either naturally changes or is forcefully changed to negative. This forces the diode to stop conducting. This has specific advantage in current stiff converters as the conducting switch in series with the diode now does not need to be turned off. This is a preferred mode of soft turn off as it reduces loss in the converter. Fig. 4.1 shows the test circuit schematic. The circuit has been so chosen to accommodate several characteristic functions of a typical current switch. Fig. 4.2 shows possible realization of the current switch by series connection of switch and diode, RB-IGBT and custom made SiC-MOSFET/SiC-JBS Diode package.

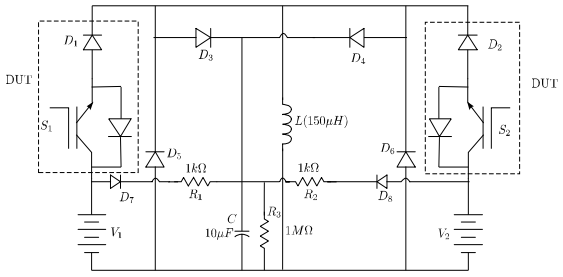


Figure 4.1: Device Test Circuit Schematic

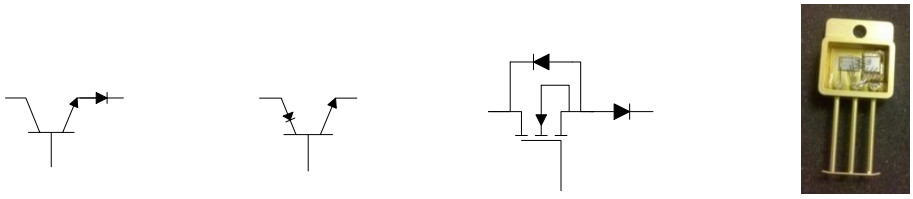


Figure 4.2: Possible Current Switch Configurations (a) IGBT+Diode, (b) RB-IGBT, (c) MOS+Diode, and (d) Custom made current switch package

Series Connection of Switch and Diode has long been used to realize soft switched current stiff converters. Though there are several advantages of these topologies, conduction losses owing to increased device count limits the maximum attainable efficiency. In this context, reverse blocking IGBTs (RB-IGBTs) may show better overall performance for soft switched current source rectifiers and inverters. The main motivation of moving from series connected discrete switch to compact custom made package (SiC-MOS + SiC JBS Diode) was to minimize leakage inductances in the circuit. This effectively reduces device stress, voltage/current overshoot/ringing and switching losses. This would give it a noticeable advantage in hard switched converters.

Fig. 4.3 shows the switching sequence of S1 and S2. At first the right hand side DC voltage (V2) is set to a higher value than the left hand side DC voltage (V1). The switch S1 is turned on first and the device (S1+D1) current starts to rise linearly. At time t=2μs, S2 is turned on. This makes the diode, D1 reverse biased and it naturally commutes off. This results in soft turn off of Si-IGBT at the low voltage side as the voltage across the switch remains close to zero throughout the operation. Fig. 4.4 and 4.5 shows the device (Si- IGBT and Si-Diode & RB-IGBT) characteristics of the side with lower voltage.

The above experiment is repeated by fixing V2 at 800V and varying V1 from 100V to 700V. This is done to find a relation between voltage and energy loss incurred due to commutation.

Similar tests have been conducted with the custom made device. Fig. 4.6 shows the comparison of loss between Si-Diode, SiC-JBS Diode, RB-IGBT and custom made device. It shows significant reduction of loss for both SiC-JBS Diode and custom made device.

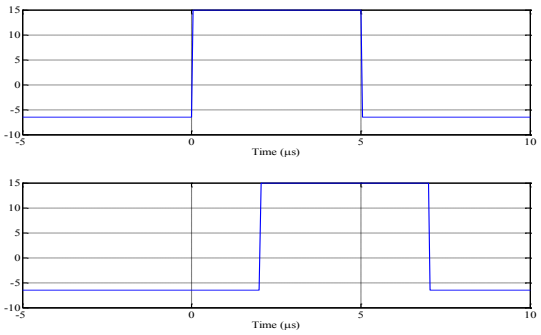


Figure 4.3: Switching sequence of S1 and S2

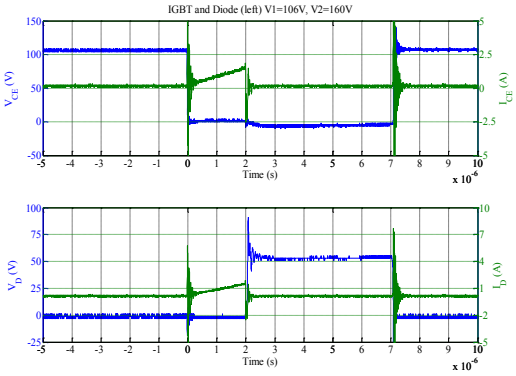


Figure 4.4: Switching Characteristics of Si-IGBT and Si-Diode under RVC

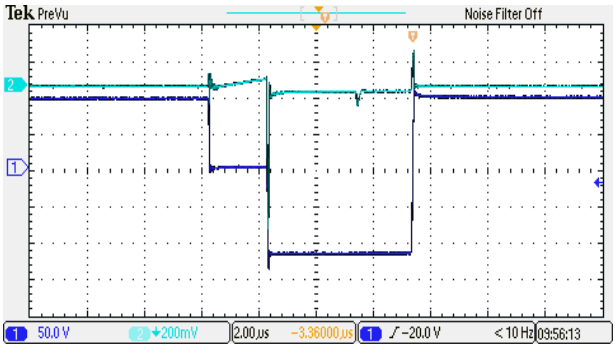


Figure 4.5: Switching Characteristics of RB-IGBT

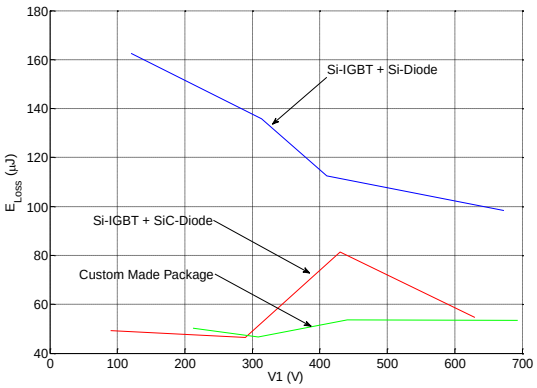


Figure 4.6: Comparison of loss between Si-Diode, SiC-JBS Diode, RB-IGBT and custom made device

The results clearly shows the reduction of commutation losses when the custom made device package is used.

4.3 Switch Overlap Loss Analysis

A new kind of switching characteristics is discovered with a modified switching scheme. A unique Voltage bump appears at non-zero turn-on current while transferring power from higher voltage to lower voltage. In this case the switch corresponding to higher voltage is turned on first. Consequently, the device current starts rising linearly and after some point of time, the switch corresponding to the lower voltage is turned on. In this case, no reverse voltage appears across the switch corresponding to higher voltage and therefore, it continues conducting. The conducting switch is then gated off and the non-conducting switch starts conducting. This is when a voltage bump appears across the IGBT corresponding to the leg with lower voltage. This system has been tested with Si-IGBT in series with SiC-JBS Diode. Fig. 4.7 shows the typical characteristics depicting the voltage bump in Si-IGBT. The RB-IGBT has also been tested under the same condition as shown in Fig. 4.8 below. The system has also been tested with SiC-MOSFET in series with SiC-JBS Diode. Fig. 4.9 shows the characteristics depicting no voltage bump for the SiC MOSFET. The device was tested at

various voltages but did not show any voltage bump. This reduces the corresponding loss and also avoids the voltage spike which might cause device failure.

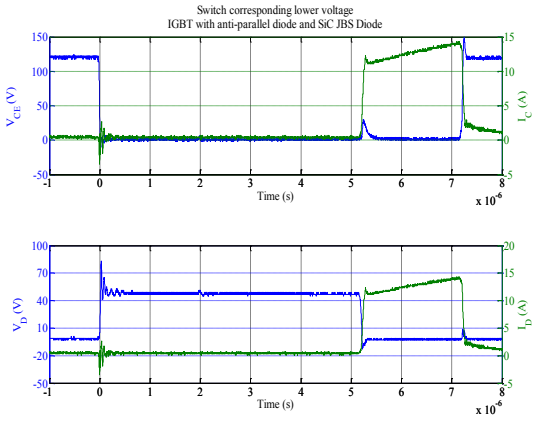


Figure 4.7: Device characteristics of the leg with lower voltage for Si-IGBT

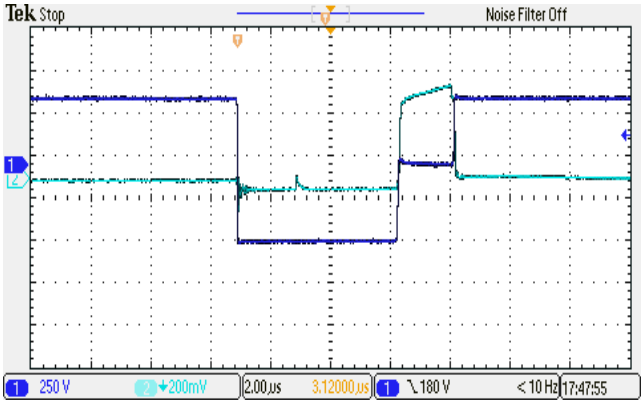


Figure 4.8: Device characteristics of the leg with lower voltage for RB-IGBT

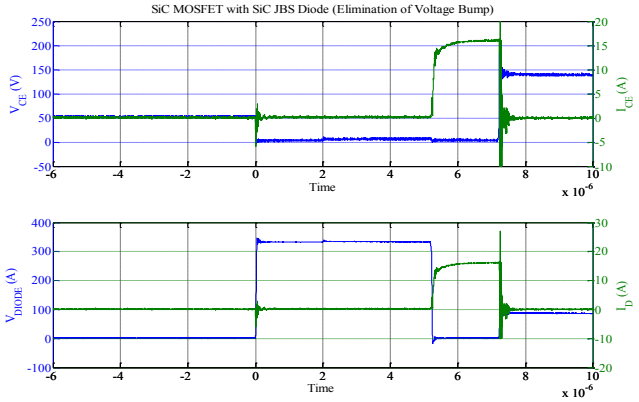


Figure 4.9: Device characteristics of the leg with lower voltage for SiC-MOS

Fig. 4.10 and 4.11 shows the variation of voltage bump peak in Si-IGBT and total Energy Loss as a function of V1.

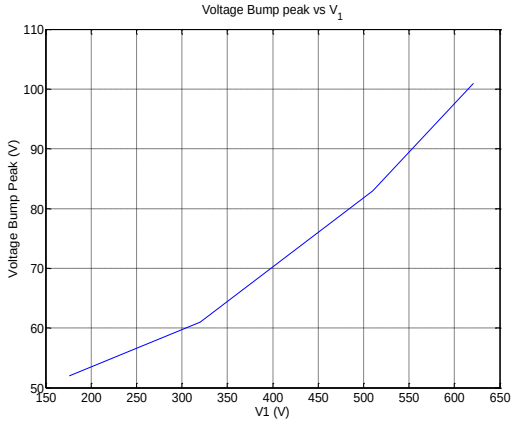


Figure 4.10: Variation of Voltage Bump as a function of Blocking Voltage

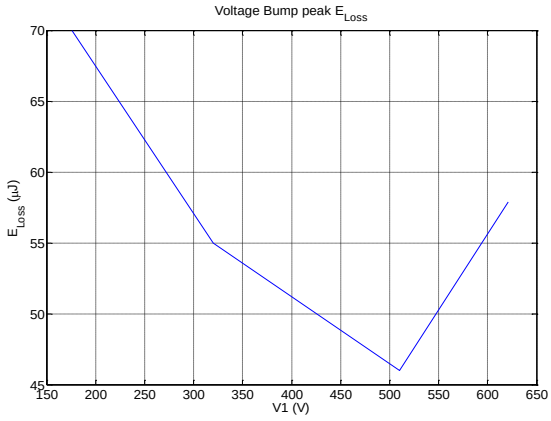
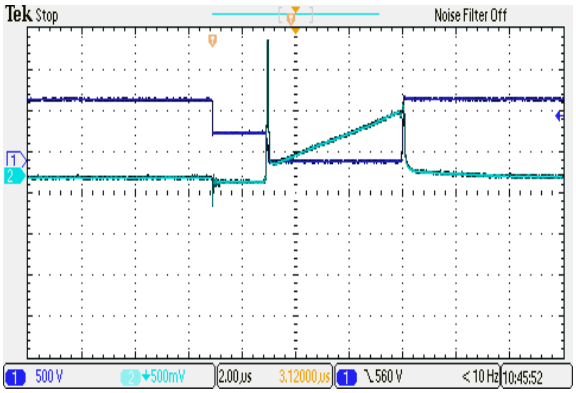


Figure 4.11: Variation of E_{LOSS} as a function of Blocking Voltage

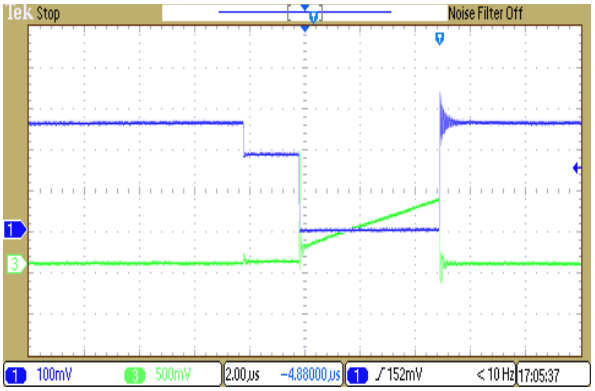
4.4 Hard Switch Test

As mentioned in previous sections, most of the switching in current stiff converters is based on self/forced commutation. However, some instants may still have hard switch turn-on and off. To address this issue, the circuit has been tested under hard switched conditions. In this test, V2 is set to 800V and V1 is varied from 150 to 700 V. At first S1 is turned on and consequently, the inductor current rises linearly. At some point of time S2 is turned on making D1 reverse biased and as a result the current now starts flowing through the switch

combination S2+D2. This results in hard turn on of the switch S2. After some point of time S2 is gated off. It brings hard turn off for S2. Fig. 4.12 (a) and (b) shows the hard turn on and off characteristics of the understudied RB-IGBT and Si-IGBT+Si-Diode respectively.



(a)



(b)

Figure 4.12: (a) Hard Switch Characteristics of RB-IGBT; (b) Hard Switch Characteristics of Si-IGBT

This test has been repeated for the remaining sets of devices. Fig. 4.13 and 4.14 show the comparison of turn on and off losses. The results show the benefit of using SiC-MOSFET as compared to Si-IGBT. It reduces both losses and duration of high device stress. Fig. 4.15 shows the experimental setup.

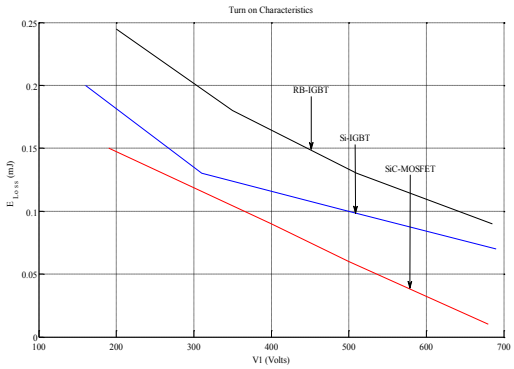


Figure 4.13: Variation of E_{OFF} as a function of Blocking Voltage

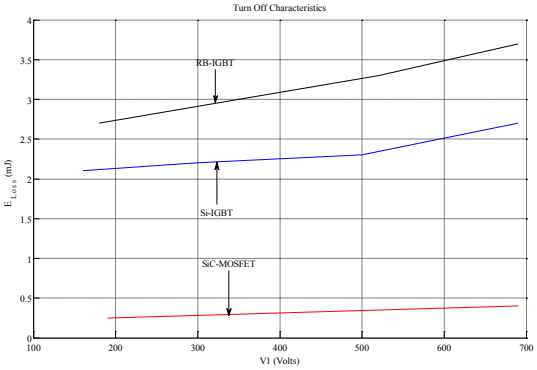


Figure 4.14: Variation of E_{ON} as a function of Blocking Voltage

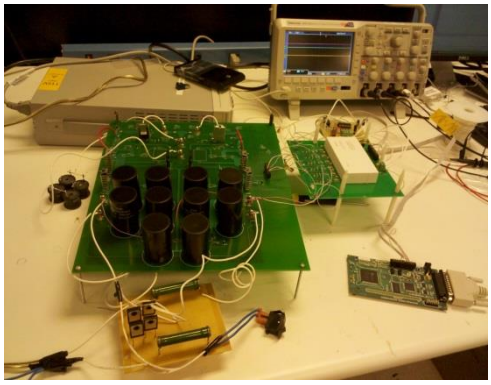


Figure 4.15: Double Pulse Test Setup

4.5 Forward Characteristics

In order to make a fair judgment on the overall device performance, it is essential to study the forward characteristics of the individual devices. The forward characteristics govern the overall conduction losses in a circuit. In this section, RB-IGBT is compared with Si-

IGBT+Si-Diode, Si-IGBT+SiC JBS Diode, SiC-Mosfet+Si-Diode, SiC-Mosfet+ SiC JBS Diode and the custom made package. Fig. 4.16 shows the various forward characteristics of the above mentioned devices.

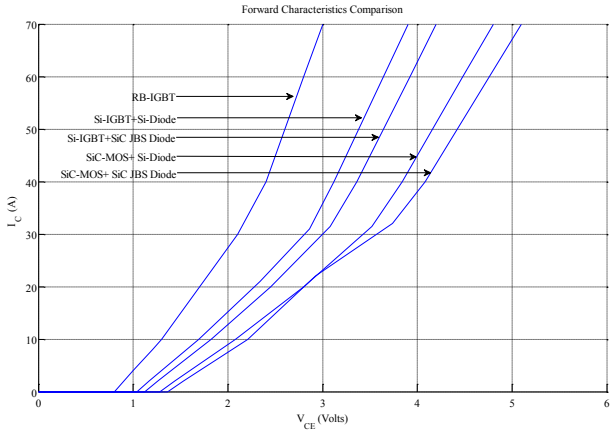


Figure 4.16: Forward Characteristics Comparison

Interestingly it is observed that even though RB-IGBT has worse switching loss characteristics than both Si-IGBT and SiC-MOSFET, it still demonstrates better forward characteristics than all combinations of series connected switch and diodes. This gives it a unique advantage in soft switched converters where conduction loss dominates over the switching loss.

4.6 Converter Test

This section deals with the switching and conduction loss break-up of DynaC and High Frequency Link Converter. The system has been simulated for 100kW, 480V, 3 phase system. The switching frequency is set to 20kHz. The estimated peak inductor current is 400A. The following kind of switching/conduction loss takes place in this converter:-

1) Mild turn on loss (owing to turn on at non-zero current and parasitic capacitance of the inductor/transformer).

2) Reverse Voltage Commutation.

3) Hard turn off (inter grid).

4) Conduction Loss.

As the peak current requirement is higher than the current rating of the devices, appropriate number of individual devices is connected in parallel to support the current. In order to get realistic values of forward characteristics, each of the devices were tested using a Conduction Loss Curve Tracer. The tracer provided the forward characteristics of each of the devices. The various switching and conduction loss data collected from the switching loss and forward characteristic test has been tabulated and fed to a look-up table in PLECS. Fig. 4.17 shows a typical LUT.

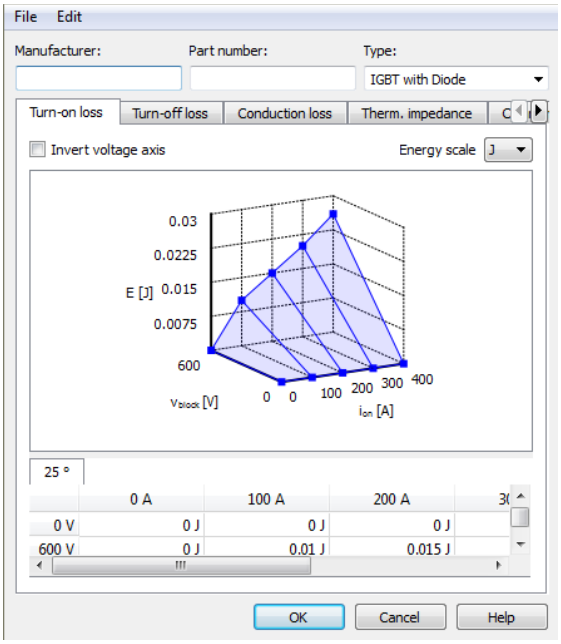


Figure 4.17: Typical LUT in PLECS

Table 1: Device Loss Comparison in DynaC

Loss	Si-IGBT + Si-Diode	Si-IGBT + SiC JBS Diode	SiC MOS + Si-Diode	SiC MOS + SiC JBS Diode	Custom made Package	RB-IGBT
Total Conduction	1565 W	1718 W	1591 W	1743 W	1715 W	960 W
Total Switching	679 W	603 W	267W	197 W	183 W	792 W
Total	2244 W	2321 W	1858 W	1940 W	1898 W	1752 W

The same test has been carried out for Partial Resonant Link Converter. Among the chosen devices, RB-IGBT shows better forward characteristics and thus contributed to lower conduction loss. Even though RB-IGBT witnessed considerably high switching losses, it resulted in the best overall performance. This shows the effective selection of RB-IGBT in soft switched converters where conduction loss dominates over the other losses. Tab. 2 shows the loss comparison.

Table 2: Device Loss Comparison in Partial Resonant Link

Loss	Si-IGBT + Si-Diode	Si-IGBT + SiC JBS Diode	SiC MOS + Si-Diode	SiC MOS + SiC JBS Diode	Custom made Package	RB-IGBT
Total Conduction	1436 W	1668 W	1505 W	1713 W	1698 W	924 W
Total Switching	1544 W	1242 W	764 W	496 W	425 W	1803 W
Total	2980 W	2910 W	2269 W	2209 W	2123 W	2727 W

4.7 Performance Evaluation and Characterization of 6500 V Asymmetric SiC NPNP Thyristor based Current Switch

SiC-based Thyristors as offer 10X higher voltage, 100X faster switching frequencies and higher-temperature operation compared with conventional Silicon-based Thyristors. Targeted research applications include general-purpose medium-voltage power conversion (MVDC), grid-tied solar inverters, wind-power inverters, pulsed power, weapon systems, ignition control, and trigger control. Ultra-high-voltage (>10 kV) SiC device technology will play a revolutionary role in the next-generation utility grid. SiC-based Thyristors also offer the best chance of early adoption due to their similarities to conventional power grid elements. Deploying these power semiconductor technologies could provide as much as a 25–30% reduction in electricity consumption through increased efficiencies in the delivery of electrical power [68].

The main motivation of this work is to evaluate performance and characteristics of a 6.5kV SiC Thyristor (GA040TH65) based current switch. The device has been tested in: (a) Turn-on : Non-Zero Current + Non-Zero Voltage, (b) Turn-on : Zero Current + Non-Zero Voltage, (c) Turn Off: Zero Current + Zero Voltage and (d) Turn Off: Non-Zero Current + Zero Voltage. These readings have been enumerated in a Look-Up Table for a converter simulation. The overall switch-losses have been plotted as a function of power for a particular frequency rating.

4.7.1 Test Circuit And Principle of Operation

Fig. 4.18 shows the circuit schematic of one of the proposed test setup. When the Thyristor 'T' is triggered on, input voltage V_{in} gets applied to the L-C resonant tank. The device turns on at zero current and non-zero voltage. The current rises and falls back to zero following a sinusoidal trajectory. The series connected diode, 'D' gets reverse biased as the current crosses zero value thereby turning T off under zero voltage and zero-current.

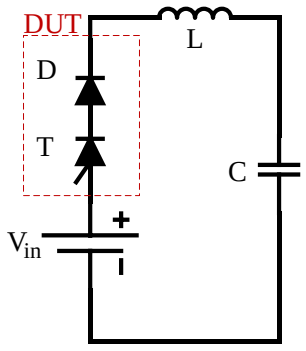


Figure 4.18: Test Circuit for ZCS Characterization

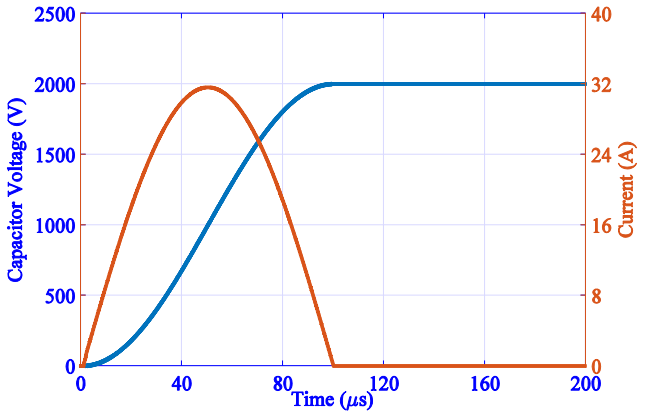


Figure 4.19: Capacitor Voltage and Current for Vin=1000V

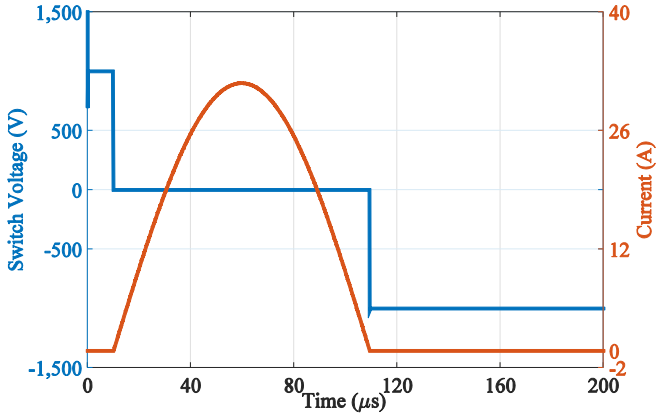


Figure 4.20: Switch Voltage and Current under ZCS turn on and off

When the device is turned on, the circuit equation can be described as:-

$$V_{in} = L\frac{dI}{dt} + \frac{\int Idt}{C}$$

The solution of this equation leads to sinusoidal current and co-sinusoidal voltage waveform:-

$$I = \frac{V_{in}}{\sqrt{L/C}}\sin(\omega t) \text{ and } V_c = V_{in}(1-\cos(\omega t))$$

where,

$$\omega = \frac{1}{\sqrt{LC}}$$

Fig. 4.19 and 4.20 shows the simulation result of this pulse test. The switch voltage in Fig. 4.20 is equal to the input voltage (1000V in this case) before the switch is turned on. During conduction, it falls close to 0V and after the series diode gets reverse biased, blocks a negative voltage. This voltage is the difference between input and capacitor voltage. The capacitor voltage at this time is close to twice the value of Vin. Therefore, the blocking voltage of the device is close to –Vin (-1000V in this case). It should be noted that both turn-on and turn-off occurs close to zero current. During turn-on, the thyristor voltage changes from Vin to zero while the Diode voltage is close to zero throughout. During turn-off, the thyristor voltage remains zero but the diode voltage changes from zero to –Vin as shown in Fig. 4.20. The main motivation of this test is to characterize the device under different voltage stresses.

Fig. 4.21 shows a modified version of the test circuit to characterize the device under hard switched condition. The value of voltage V2 is kept higher than that of V1. At first T1 is turned on, the current as the previous case rises in a sinusoidal manner. After sometime, T2 is turned on. As V2>V1, this operation forces the series connected diode (with T1) to turn off and the resonant line is now connected to V2. The system goes on to complete the characteristic sinusoidal trajectory with a different amplitude.

Fig. 4.22 shows the capacitor voltage and current during this transition. Fig. 4.23 and 4.24 shows the switch voltage and current of T1 and T2. This facilitates Non-Zero Current + Non-Zero Voltage turn on of T2 whereas Non-Zero Current + Zero Voltage turn off of T1.

Characterizing this under different voltage and current would give us valuable overview of how the device behaves under hard switching condition. Hardware results have been shown in the following section.

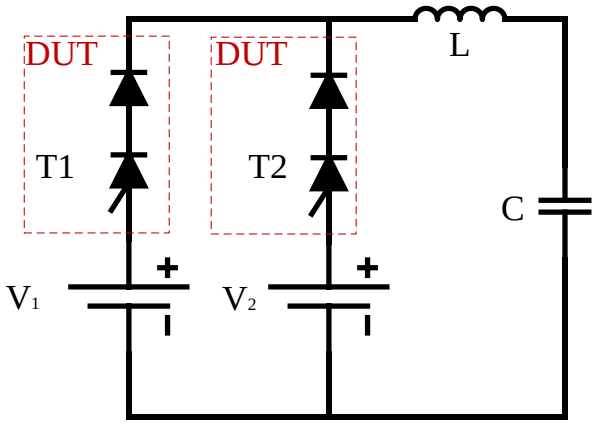


Figure 4.21: Test Circuit for Hard Switched Characterization

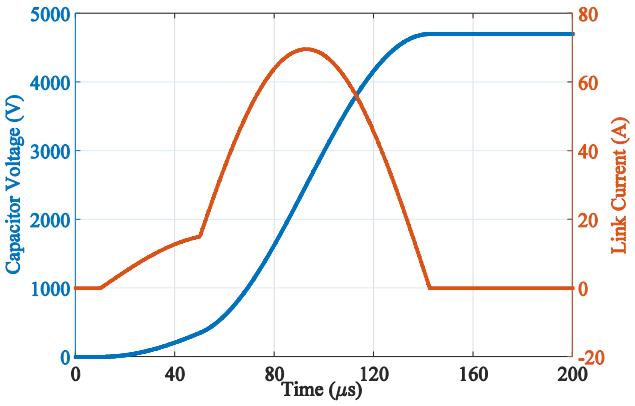


Figure 4.22: Capacitor Voltage and Current for V1 = 500V and V2 = 2500V

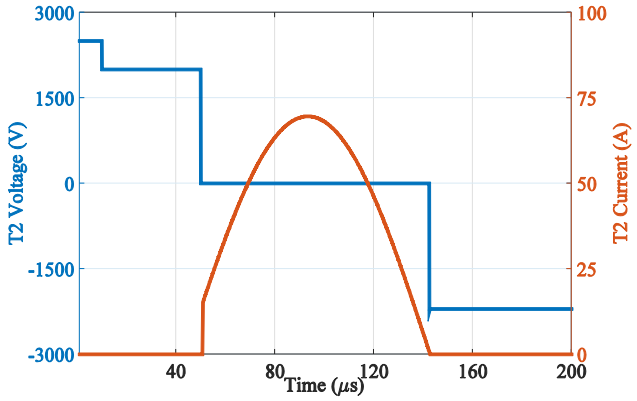


Figure 4.23: Switch (T2) Voltage and Current under hard switched turn-on condition

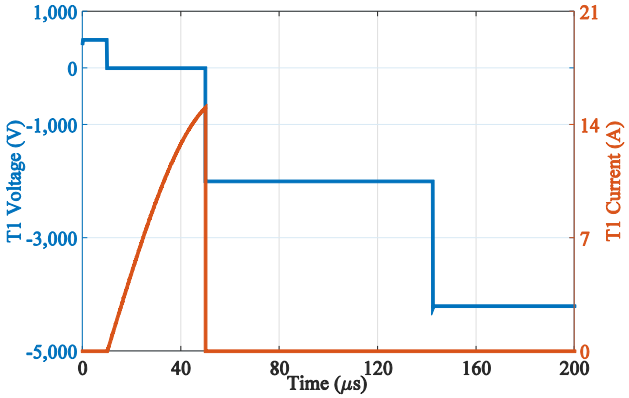


Figure 4.24: Switch (T1) Voltage and Current under hard switched turn-off condition

4.7.2 Hardware Test Results

A hardware setup was assembled to carry out the tests mentioned in the previous section. At first the switch was tested under ZCS as mentioned in Fig. 4.18. The input voltage has been varied from 200V to 1000V. This resulted the maximum voltage of the capacitor to be close to 2000V. Fig. 4.25 to 4.27 shows the device current and voltage waveforms as the input voltage is varied.

Fig. 4.28 shows the zoomed-in view of the turn-off portion of Fig. 10. It can be seen the device blocking voltage undergoes some ringing. While turning off, the diode stored charge

in the vicinity of the diode junction becomes zero, and making it reverse biased. The inductor current is now slightly negative, and must flow through the diode leakage capacitor. The inductor (L) and this leakage capacitor then form a series resonant circuit, which rings with decaying sinusoidal amplitude as shown. This ringing is eventually damped out by the parasitic loss elements of the circuit, such as the inductor winding resistance, inductor core loss, and capacitor equivalent series resistance. With the increase of input voltage, Vin the magnitude of oscillation increases. As the switch is connected in series with an inductor and capacitor, use of busbars (used to minimize stray inductance) can be avoided.

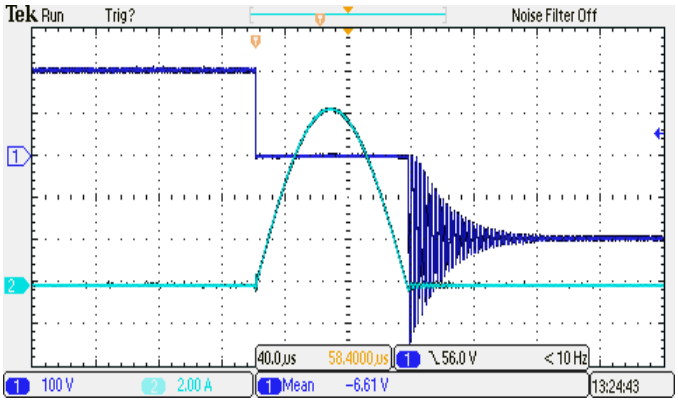


Figure 4.25: Switch Voltage and Current under zero current switched turn on and off condition for Vin=200V

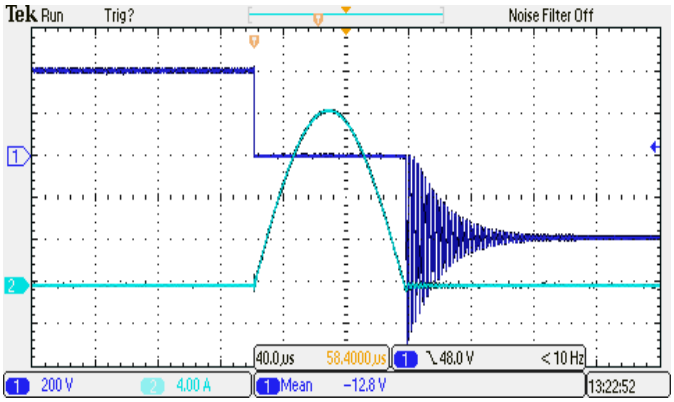


Figure 4.26: Switch Voltage and Current under zero current switched turn on and off condition for Vin=400V

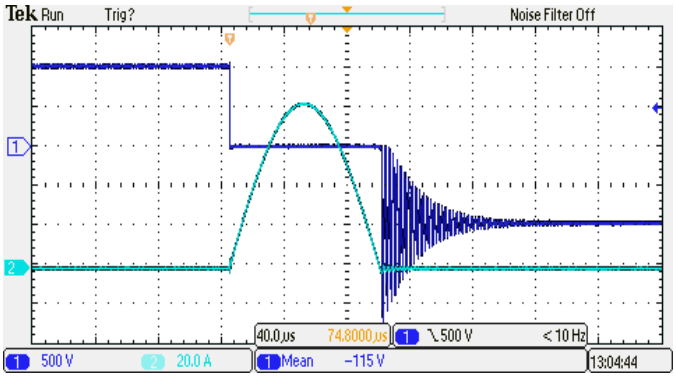


Figure 4.27: Switch Voltage and Current under zero current switched turn on and off condition for Vin=1000V

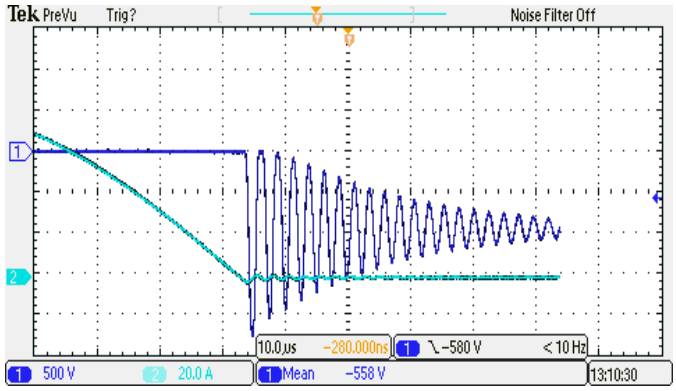


Figure 4.28: Zoomed-in view of the Switch Voltage and Current under zero current switched turn on and off condition for Vin=1000V

The hardware test setup was re-assembled to accommodate two devices for the hard switch characterization. For this setup, special care was taken to reduce stray inductance by introducing busbars connecting the two devices and the input capacitor. This is done to get accurate turn on and off characteristics of the switch under non-zero voltage stress. The circuit has been tested from 200V to 1000V input. Fig. 4.29 and 4.30 shows the characteristic transitions of switch T1 (as referred in Fig. 4). Fig. 4.31 shows a zoomed in version of the hard switching transient of Fig. 4.30. As it can be seen, the duration of this transient is lower than 200ns.

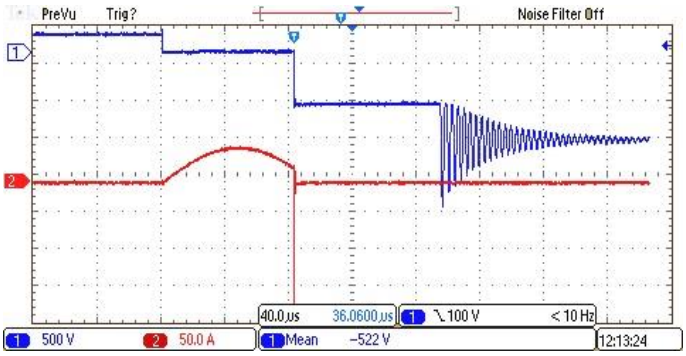


Figure 4.29: Switch (T1) Voltage and Current under non-zero current switched turn off condition for V1=250V and V2=1000V

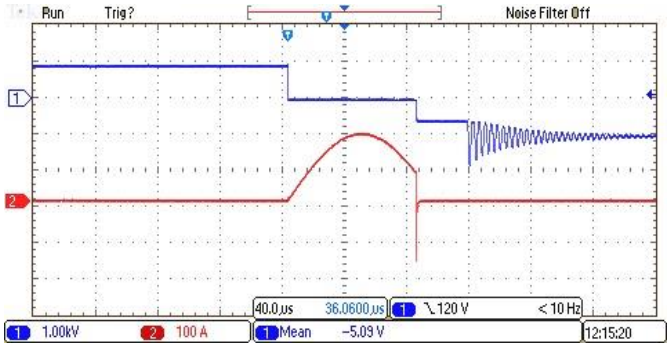


Figure 4.30: Switch (T1) Voltage and Current under non-zero current switched turn off condition for V1=1000V and V2=1500V

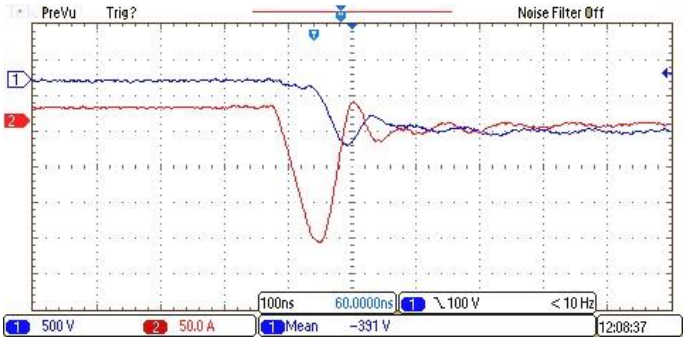


Figure 4.31: Zoomed-in Waveform of Switch (T1) Voltage and Current under non-zero current switched turn off condition for V1=1kV and V2=1.5kV

Fig. 4.32 and 4.33 shows the characteristic transitions of switch T2 (as referred in Fig. 4). Fig. 4.34 shows a zoomed in version of the hard switching transient of Fig. 4.33. As it can be seen, the duration of this transient is close to 250ns.

It should be noted that these fast transitions are attributed to the usage of SiC Thyristor (during turn on) and SiC JBS Diode (during turn off). Si-based devices of this voltage rating usually takes in excess of 15us to turn on. This switch combination reduces the losses by a significant margin thereby making thyristors suitable for high voltage, high frequency and high power converters.

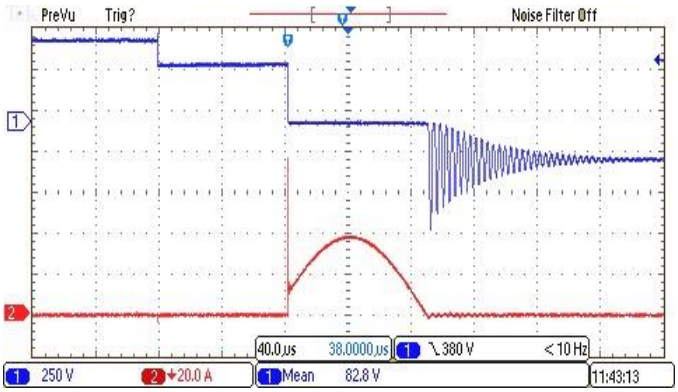


Figure 4.32: Switch (T2) Voltage and Current under non-zero current switched turn off condition for V1=200V and V2=500V

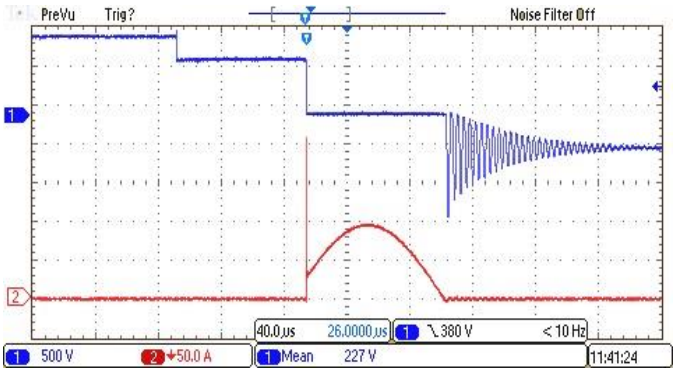


Figure 4.33: Switch (T2) Voltage and Current under non-zero current switched turn off condition for V1=250V and V2=1000V

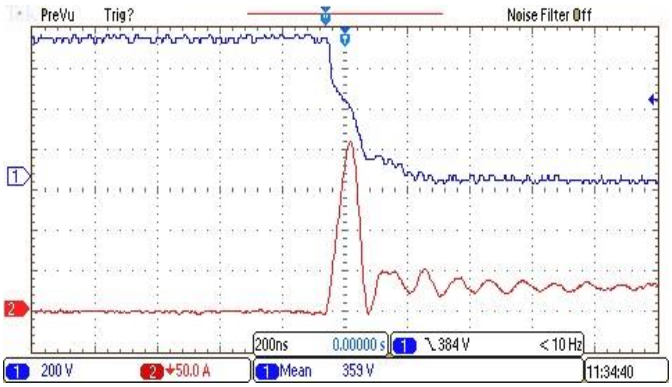


Figure 4.34: Zoomed-in Waveform of Switch (T2) Voltage and Current under non-zero current switched turn off condition for V1=250V and V2=1kV

As thyristors and diodes can be designed to be much more rugged than IGBTs and MOSFETs, this would form a suitable replacement for the same.

4.7.3 Basic Principle Of Operation Of Resonant AC-Link Converter

As thyristors cannot turn off using a gate signal, the converter of choice should have provision for natural or forced commutation. One such converter is the Resonant AC-Link Converter [69]. A simplified circuit schematic of the AC/AC topology is shown in Fig. 4.35. The basic idea is to connect the input phases to the resonant link, this makes the current follow a sinusoidal trajectory which assists in self turn-off of the devices once it reaches back to zero. At this point the capacitor voltage reaches close to twice the value of input phase-phase voltage. This stored energy is then dissipated to the output grid in a similar auto turn-off fashion. This operation is repeated at high frequency to transfer required amount of power from input grid to output grid. This is a universal converter system as it can transfer power from DC/AC, DC/DC, AC/DC, AC/AC with and without transformer isolation. For this part of the work, this converter has been used as a benchmark to assess the performance of the

understudied thyristor switches. This section will deal briefly with the principle of operation of the converter.

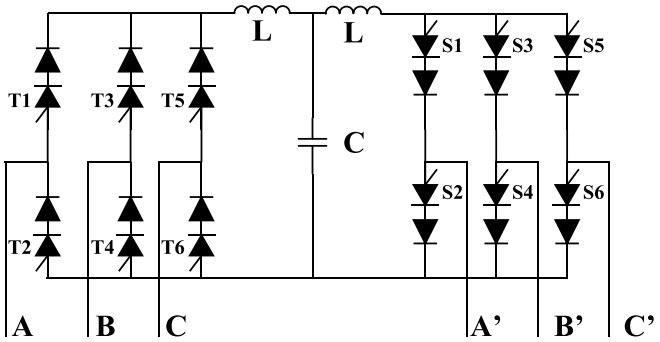


Figure 4.35: Circuit Schematic of the understudied Resonant AC-Link Converter

In order to understand the modes of operation, a balanced three-phase system with instantaneous input voltages as, Va=386V, Vb=-252V and Vc=-134V is studied. At first the switches (on the rectifier side) corresponding to the second highest input line-line voltage will be triggered on (T1 and T6 in this case). The initial current and voltage of the inductor (left) and Capacitor is zero. As the second highest line-line voltage (Vac) is applied to the inductor (left) and capacitor, the current starts rising sinusoidally and the capacitor voltage starts rising as shown in Section II. In order to make sure that input phase currents are harmonic-free, the ratio of overall charge drawn from the phases and switching time period should be equal to the one set by the controller. A non-linear charge control function hence can be implemented [69]. Once the desired amount of charge has been drawn from the input phases (A and C in this case), the switch corresponding to the highest line-line voltage is triggered (T1 and T4 – as T1 is already on, only T4 is triggered). This makes the series connected diode in T6 reverse biased hence turning the leg off while forcing a non-zero current to flow through T4. It should be noted that during this transition, the thyristor (T6) is

turned off under zero voltage as the series diode blocks the reverse voltage. The turn-on however occurs under hard-switching condition. Once T4 is turned on, the new link voltage is Vab. This forces the LC network to change its trajectory to a different sinusoidal. The link is allowed to follow this state space till the current falls back to zero when the series connected diode turns the devices off under zero-current. The link capacitor now stores the entire energy transferred from the input grid. This energy can be dissipated using the same algorithm to the output grid. Fig. 4.36 shows a typical voltage/current characteristics of the link capacitor during charging (when current is positive) and discharging (when current is negative).

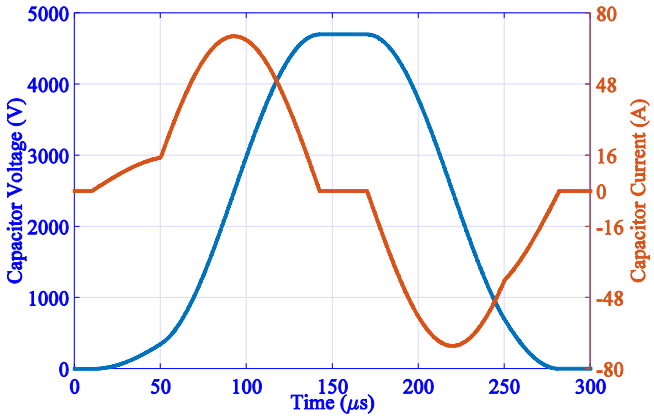


Figure 4.36: Typical voltage and current transitions of the link capacitor during one switching time period

These sets of operations are repeated at high frequency to transfer power from one grid to another while maintaining soft switching and harmonic–free input and output grid currents.

4.7.4 Switch Loss Estimation Of Resonant AC-Link Converter

Fig. 4.37 and 4.38 shows the hard-switched turn on and off losses of the device as a function of voltage and current. The Forward Characteristics of 6.5kV/80A SiC-Thyristor and 10kV/10A SiC-JBS Diode is shown in Fig. 4.39 and 4.40.

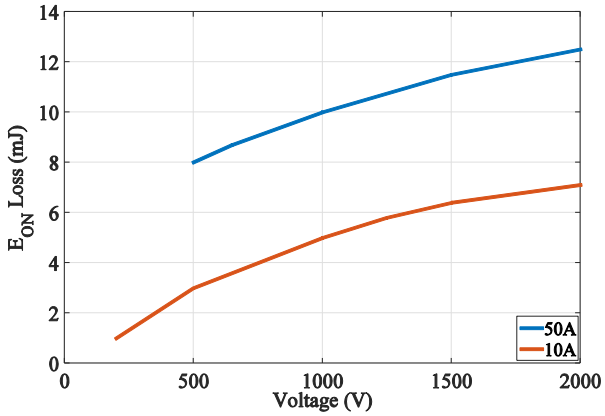


Figure 4.37: Variation of Turn-On Loss of SiC-Thyristor + SiCJBS Diode switch combination as a function of Voltage and Current

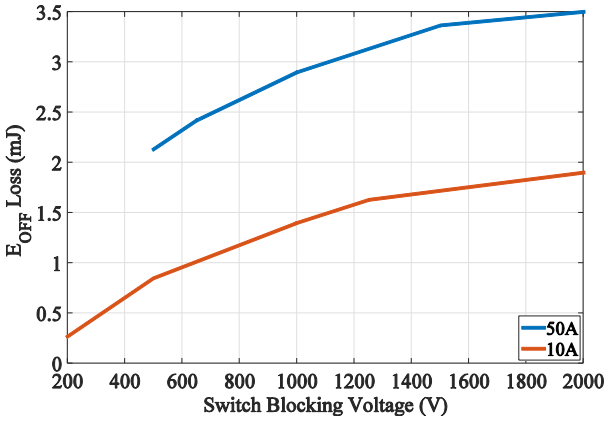


Figure 4.38: Variation of Turn-Off Loss of SiC-Thyristor + SiCJBS Diode switch combination as a function of Voltage and Current

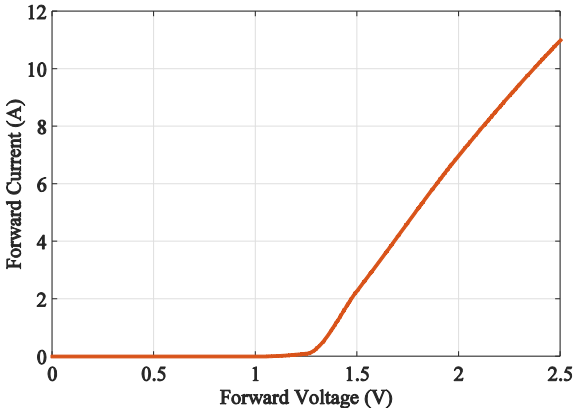


Figure 4.39: Forward Characteristics of 10kV/10A SiC-JBS Diode

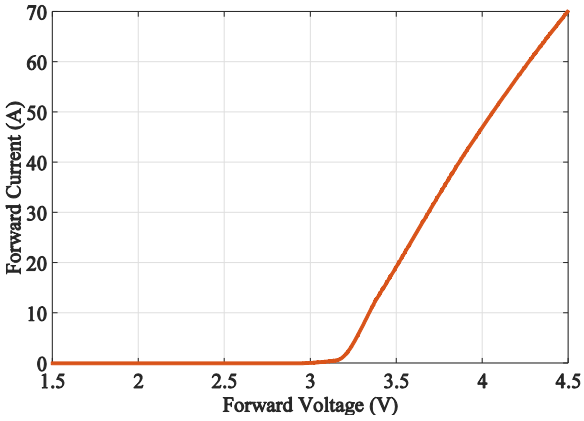


Figure 4.40: Forward Characteristics of 6.5kV/40A SiC Thyristor

Table 3: Specifications of Converter Simulation for Switch Loss Estimation

Parameters	**Values**		
Grid Voltage (l-l, kV, rms)	2	2	2
Phase Current (A, rms)	10	20	30
Total Power (kW)	34.64	69.28	103.9
Inductance (uH)	50		
Capacitance (uF)	5		
Frequency (kHz)	8		

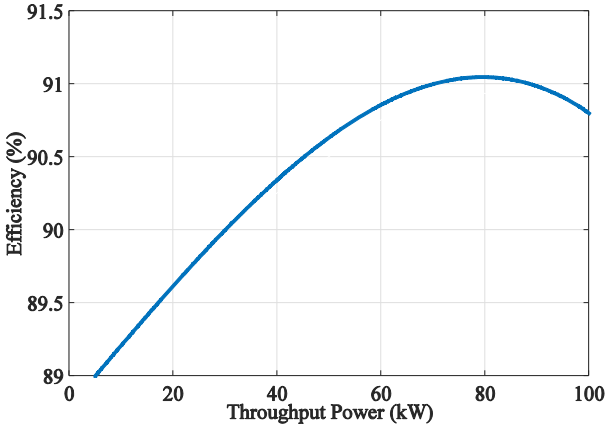


Figure 4.41: Converter Efficiency as a function of throughput power at 8 kHz switching frequency

These data have been populated in the loss look-up table in the understudied PLECS simulation. Tab. 3 shows the specifications of the understudied converter. The system has

been simulated for different phase current requirements. Fig. 4.41 shows the variation of converter efficiency (ignoring the losses of passive components) as a function of throughput power.

4.8 Conclusion

This chapter presents comparison of diode reverse recovery loss of Si-Diode, SiC-JBS diode and RB-IGBT (acting as a diode). SiC-JBS diode shows a considerable reduction of loss. A new form of switching characteristics is reported for Si-IGBT. This was not present when the same experiment was conducted with SiC MOSFET thus reducing the effective loss. In order to make sense out of the various characterizations, a High Frequency Link converter is simulated with the loss data collected from the various experiments. SiC based devices in general showed significant reduction of loss when tested under hard switched conditions. The custom made compact device consisting of SiC-MOSFET and SiC-JBS Diode show significant reduction of losses. RB-IGBT though having high switching losses, shows impressive reduction of overall losses in soft switched converters. The prime motivation of this work is to propose test methods to evaluate performance and characteristics of a 6.5kV SiC Thyristor based current switch (series connected active switch and diode). The device has been tested under ZCS and hard turn on and off transitions. Conceptual simulation and hardware results have been presented. It has been shown that SiC Thyristor with SiC JBS Diode exhibit fast turn-on and off transitions (~200ns). The collected data has been used to estimate overall device losses of a high voltage high power resonant soft-switched converter. It has been shown that the expected efficiency of the converter (ignoring the passive losses) can reach as high as 92%. This switch combination is expected to form a robust system for high voltage, high power and high frequency converter.

CHAPTER 5

DESIGN CONSIDERATIONS OF PACKAGING A HIGH VOLTAGE CURRENT SWITCH

5.1 Introduction

The current switch (series connected switch and diode) has found its application in various current source based converters [70] - [74]. The main advantages of using current-source based topologies can be linked to the fact that these converters usually use less number of active switches, have a more rugged natural protection (owing to the series diode), are well suited for zero-current and zero-voltage based soft switching, etc [75]- [76]. These converters are usually made using thyristors with external commutation circuits, albeit at low switching frequency. The frequency of operation can be pushed to significantly higher values by using faster devices, like IGBTs. With the advent of Silicon-Carbide Devices, singular power electronic devices can now operate beyond 10kV-15kV levels [77] - [80]. This effectively reduces the number of series connected components in the circuit, but drastically increases the dielectric and thermal stresses that develop within the power module. The non-sinusoidal nature of this stress, punctuated with high dV/dt and dI/dt, leads to several steep constraints in terms of parasitic series inductance, shunt stray capacitance, capacitive coupling, thermal conduction, etc [81].

As previously mentioned, the current switch has an additional diode in series with the regular active switch. Packaging this structure comes with an inherent problem of dealing with peak positive (owing to the switch) and negative (owing to the diode) voltage stress within a span of less than 100μs. This is considerably larger than regular switches for the same terminal voltage rating. In order to fully understand how these non-conventional stresses, affect the

current switch packaging, and therefore the overall switch operation, multi-physics simulations have been performed for various layouts of this series diode and regular switch topology based on a material selection that is capable of the required dielectric strength. Physics based, accurate device models have been studied with estimated parasitic parameters in SIMPLIS-SIMETRIX. Various cross simulation results have then been used in an iterative fashion to redesign and analyze the optimized package structure for the final current switch design.

The chapter has been divided into several subparts. First, the basic structure and common testing practices of current switch are enumerated. Two different approaches of fabrication are discussed. Various advantages and disadvantages of both approaches are shown. MAXWELL and Q3D based simulations depicting the voltage/current distribution in the module and extraction of various parasitic parameters are then studied. A parametric sweep is also done to show the appropriate design constraints to fulfil most of the parasitic parameters while operating in the safe operating area. Thermal analysis and maximum attainable frequency calculation is shown in the final analysis part of the chapter. Finally, the work is concluded depicting the major critical design parameters and proposed design considerations.

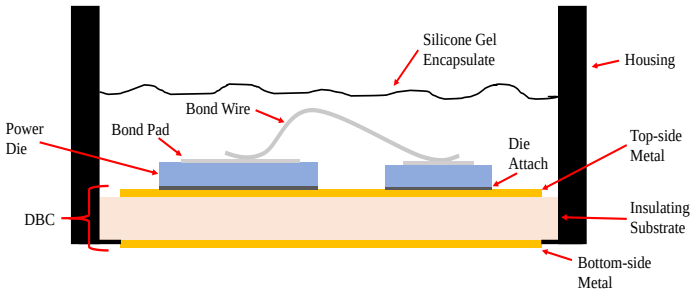


Figure 5.1: General Structure and components of a typical package

Fig. 5.1 shows various packaging components of a standard power module which will be used in the following sections for reference.

5.2 Principle Stress And Operations Of Current Switch

This part of the chapter has been further divided into three subparts: (A) Basic Switching Operation, (B) The effects of parasitic inductance and capacitance and (C) General specifications and design constraints. The main motivation is to put forward a simplified stress analysis that a typical current switch would undergo in a converter. Accurate physics based device models have been used for this simulations for high accuracy/resolution of the transitioning waveforms. SIMPLIS/SIMETRIC software has been used for this section.

(A) Basic Switching Operation

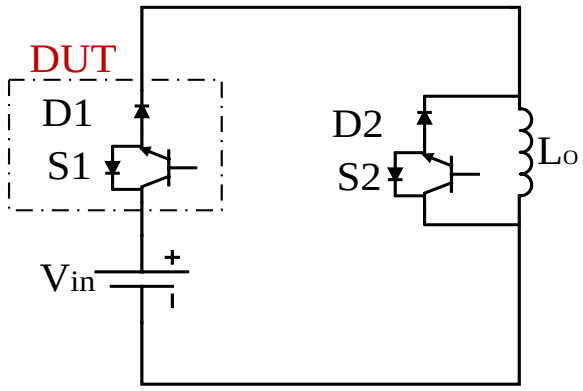


Figure 5.2: Test Circuit Schematic with minimal parasitic inductance

As in most power electronic circuits, the switches usually undergo hard-switching states. In hard switching transitions, the device undergoes a state when both its voltage and current are non-negligible. This state can last for as low as sub 100ns to as high as above 100us. This leads to increased amount of power loss in the device and the overall converter. It is therefore essential to study the ill-effects of this stress in the package. The main motivation of this part

of the work is to demonstrate the typical stress in terms of turn-on and turn-off voltage and current as seen in the device during such hard switching conditions. Fig. 5.2 shows the test circuit schematic. In this test, Vin is set to 1000V. At first S1 is turned on and consequently, the inductor (Lo) current rises linearly. At some point of time S2 is turned on. As the series connected diode (D2) is reverse biased, S1 continues to conduct.

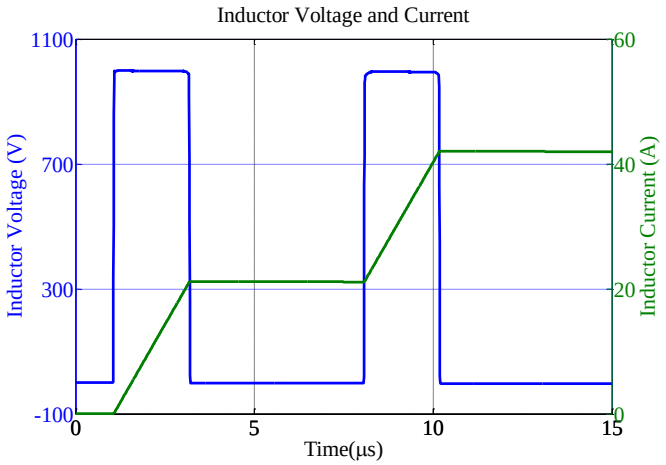


Figure 5.3: Inductor Voltage and Current for the Test setup shown in Figure 2

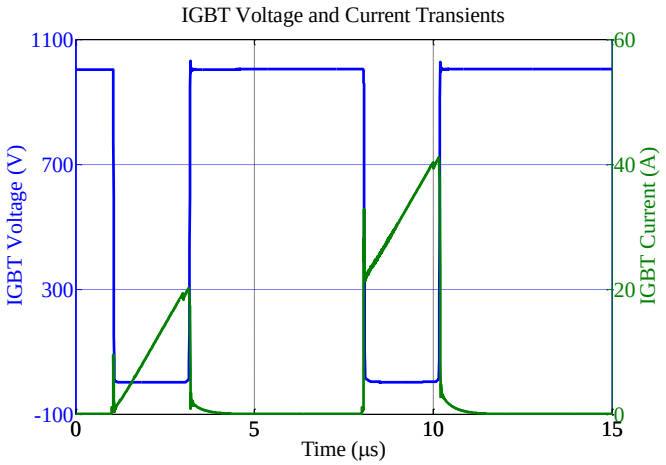


Figure 5.4: IGBT Voltage and Current Transient for the Test setup

At a following point in time, S1 is turned off and the non-zero inductor current is forced to flow through S2 and D2. A similar gating-pulse is again passed through S1 and S2. This

forms a complete double pulse test. Overall, this results in hard turn-on and turn-off of the switch S1. Fig. 5.3 shows the inductor voltage and current. As expected, during the intervals switch S1 is turned on, the inductor current rises linearly. During the turned-off state, the inductor current free-wheels via S2+D2. Fig. 5.4 shows the voltage and current across S1. As it can be clearly seen from the figure, the device undergoes dual non-zero voltage and current stresses during hard switching transient. To insure basic operation, the parasitic parameters have been set to a minimum value. It should be noted that the anti-parallel diode present across the IGBT is a necessary element even though it does not appear in the regular conduction path. During certain transitions, when the series diode is forced commuted off, it exhibits a reverse recovery current in negative direction (to the regular conduction path). If this current is forced to pass through the IGBT, it might push its operation into unsafe operating region. Several hardware testing proves that a switch is susceptible to malfunction during this transition. It is therefore necessary to place an anti-parallel diode to make sure this negative current gets a low resistance path. This would avoid IGBT experiencing a negative current hence leading to a more rugged system. A detailed analysis of low voltage hardware testing for current switch and various hard and soft switching stresses has been recently presented [82]- [85].

(B) Effects of Series Parasitic Inductance and Shunt Capacitance

The packaging of these devices usually adds some additional parasitic components which may lead to unwanted voltage/current overshoot. This increases device stress, losses, EMI, etc and might lead to a dysfunctional system. The dominating series parasitic inductance is due to bond wires used to form interconnects between the contact pads of the semiconductor

devices and the Cu pads of the Direct Bond Copper (DBC) substrate owing to their slender structure.

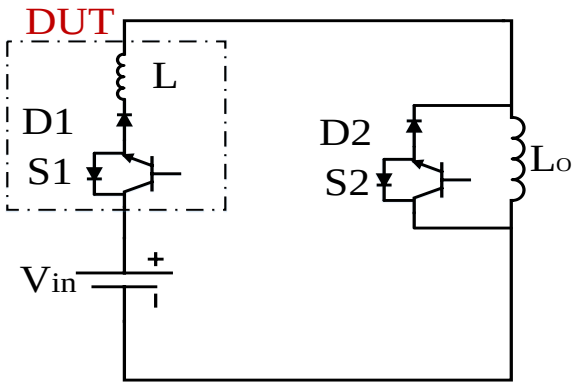


Figure 5.5: Test Circuit incorporating series parasitic inductance

Fig. 5.5 shows the modified circuit schematic depicting series inductance (L) inside the device package. It should be noted that this additional inductance can appear anywhere in the conduction path of the package. For simplicity, this inductance is shown in series with the cathode of the diode. It will be shown in a later section that this can appear both in peripheral and in between the devices. As the function of the anti-parallel diode is just for safety, the parasitic inductance between the IGBT and this diode has been neglected for simplicity. Fig. 5.6 shows a typical increase in overshoot voltage as the parasitic inductance parameter is increased. It should be noted that this increased peak voltage can go beyond the rated blocking voltage of the device. Continuous over voltage operation can lead to eventual device malfunction. The values of parasitic inductances used are 80nH and 160 nH. These values are chosen specifically to mimic a practical scenario as mentioned in later sections.

Similarly, the additional parasitic capacitance of the module can adversely affect the peak switching current seen by the device. Fig. 5.7 shows the modified circuit schematic depicting shunt capacitance inside the device package.

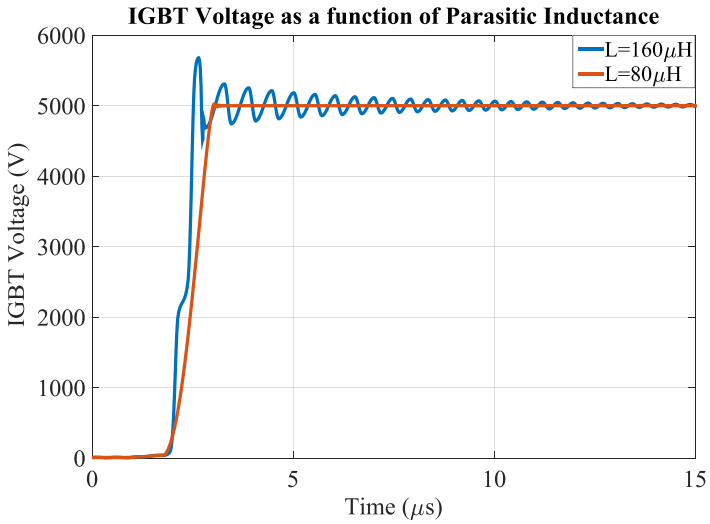


Figure 5.6: IGBT Voltage corresponding to test-setup shown in Figure 5.5 for L=80nH and 160nH

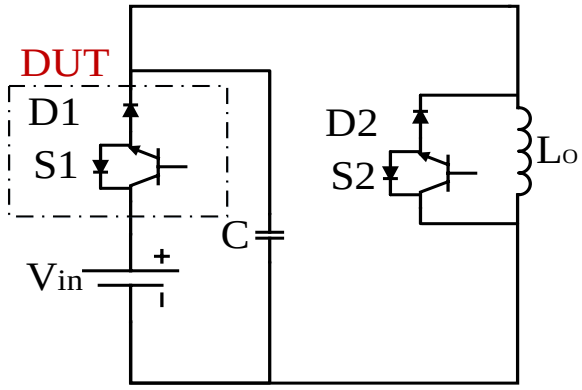


Figure 5.7: Test Circuit incorporating parallel parasitic capacitance

As shown in Fig. 5.8, the overshoot current at C=300pF is larger than the rated current of the understudied device. Continuous operation of the device under similar stress can lead to premature failure and reduction of efficiency

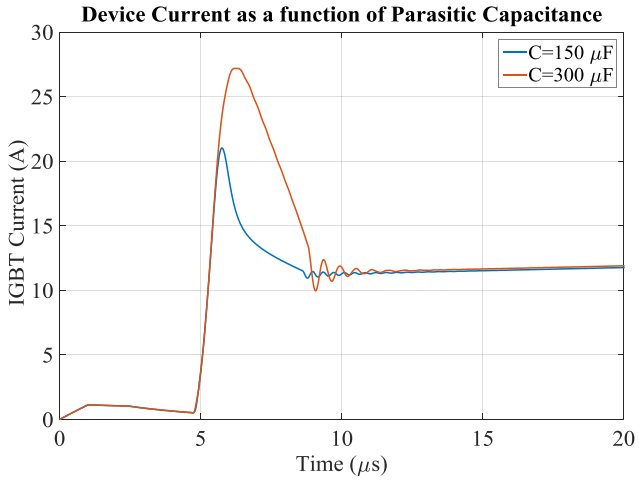


Figure 5.8: IGBT Current corresponding to test-setup shown in Figure 5.7 for C=150pF & 300pF

(C) Module Specifications

As shown in the previous subparts, various regular operation modes and specific parasitic based issues were presented. It is therefore necessary to define safe operating specifications to facilitate a robust and efficient design. For this, a parametric sweep analysis is conducted and threshold values for parasitic parameters were selected. Table 1 shows the general specs and design goals of the understudied system. A lab manufactured 6500V/25A SiC Diode has been used along with commercially available 6500V/25A Si-IGBT Die (5SMX 12M6500).

Table 1: General Specifications and Design Goals

Parameters	**Specifications**
Voltage	+/− 4000V
Current	20A
Parasitic Inductance	80nH (max. overall series)
Parasitic Capacitance	150pF (max. overall parallel)

5.3 Primary Topologies of current switch

The arrangements of series connection of IGBT and Diode can be done in two broad ways. The Cathode of the diode can be connected to the collector of the IGBT or the emitter of the

IGBT can be connected to the anode of the diode. As shown in the prior section, the series parasitic inductance in this package usually leads to unwanted stress, thereby leading to unreliable operation.

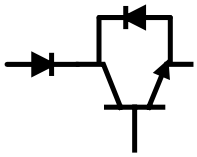


Figure 5.9 (a): Schematic of Cathode-Collector Connected Current Switch

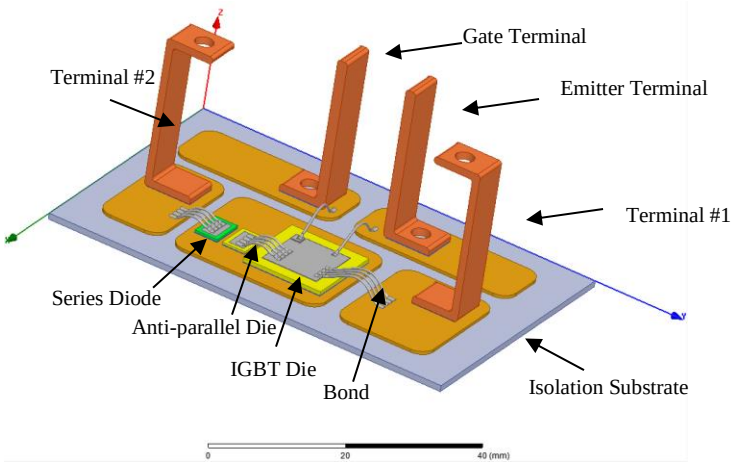


Figure 5.9 (b): ANSOFT Q3D rendering of Cathode-Collector Connected Model

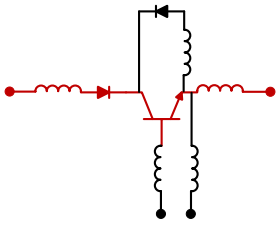


Figure 5.9 (c): Circuit schematic of the Cathode-Collector connected configuration incorporating parasitic non-idealities

It should be noted that the cathode-collector connected design leads to two distinct bond wire bridges in the conduction path, thereby considerably increasing the parasitic inductance (~160 nH) and resistance of the design. This would also lead to increased probability of

module failure in the case of current magnitudes greater than or equal to the fusing currents necessary to burn open the bond wires. The only possible advantage would be owing to the fact that this structure has separate isolated islands for the terminals. This would result in a somewhat more rugged package. Fig. 5.9 shows the fundamental circuit schematic, 3D Model and schematic with extracted parasitic.

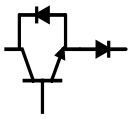


Figure 5.10(a): Schematic of Emitter-Anode Connected Current Switch

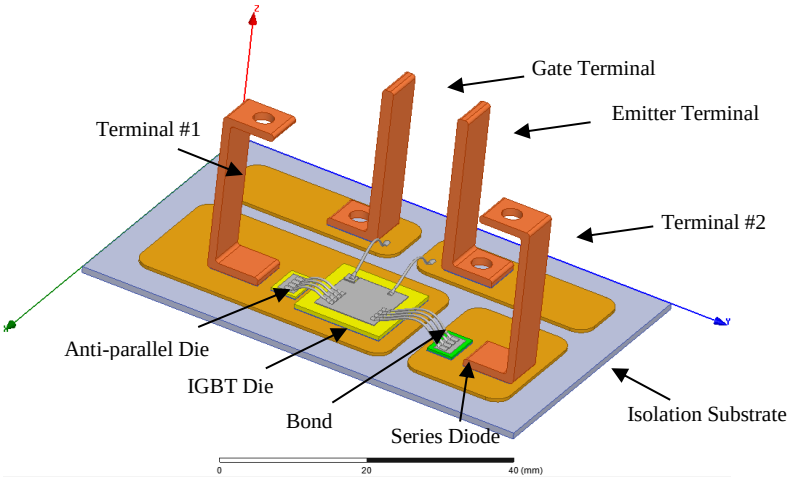


Figure 5.10(b): ANSOFT Q3D rendering of Emitter-Anode Connected Model

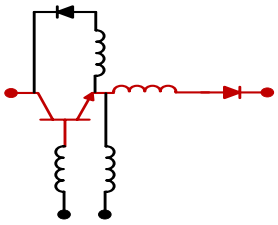


Figure 5.10(c): Circuit schematic of the Emitter-Anode connected configuration incorporating parasitic non-idealities

Emitter-Anode connected designs on the other hand leads to a more compact design with just one series connected bond Wire Bridge. This considerably reduces the parasitic parameters (~80nH) and has safer operating conditions as compared to the previous design. Fig. 5.10 shows the 3D Model depicting the preferred locations of the dies and bond wires for this configuration. From next section onwards, only the configuration shown in Fig. 5.10 is considered.

5.4 Parasitic Extraction

In this part of the work, various parasitic capacitances, inductances and resistances are studied. Parametric variations of these components are studied as a function of substrate width, leads spacing, and bond wire material.

The capacitances of interest are $C_{C,BP}$ (between Collector and Base Plate), $C_{E,BP}$ (between Emitter and Base Plate) and $C_{CAT,BP}$ (between Cathode of the Diode and Base Plate). The base plate is usually attached to a heat sink which is often grounded to facilitate safe high voltage testing/application. These capacitances therefore become essential parameters which effectively sets the functional limit of the package in general. Fig. 5.11 shows the variation of these capacitances as a function of substrate thickness. The terminals in the module are also swept across the upper copper plate of the DBC. However, it was seen that the variation of the value of series parasitic inductance was not significant enough. The value of Capacitance too remained steady in this parametric sweep provided the minimum creepage distance was maintained for safe operation. It should be noted that the capacitance, $C_{BP,E}$ is of much lower value.

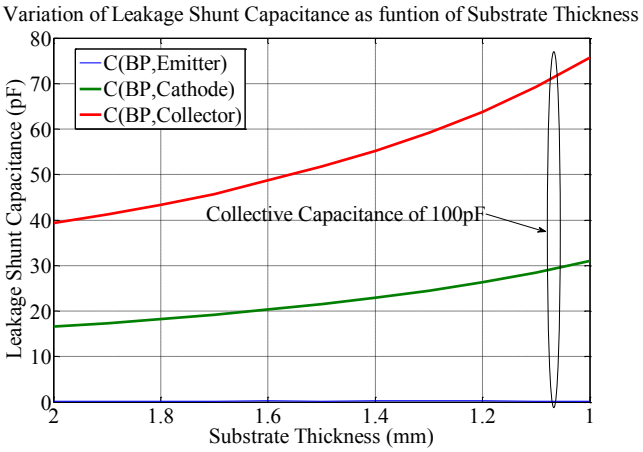


Figure 5.11: Variation of CC,BP , CE,BP and CCAT,BP as a function of DBC substrate thickness

This is due to the fact that the metallic contact at the surface of emitter is considerably smaller than that at the surface of collector. This leads to lower capacitance in series with the one between baseplate and emitter effectively making the overall capacitance. The bond wires' conductance is also varied and the effect on overall series resistance is shown in Table 2. However, it should be noted that Aluminum is still the preferred option owing to its low cost and ease of use.

Table2: Variation of resistance as a function of bond wire material

Material	**Resistance (Ohm)**
Aluminum	0.099614
Copper	0.093246
Gold	0.098347
Silver	0.092457

5.5 Current And Electric Field Distribution

Figure 5.12 shows the current distribution of the 3D model of the low parasitic package. As expected the current density is high and critical in the bond wires and surrounding area. This is to re-affirm the initial logic of using as few series connected bond wires as possible. It should be noted that only one set of bond wires conduct during regular operation.

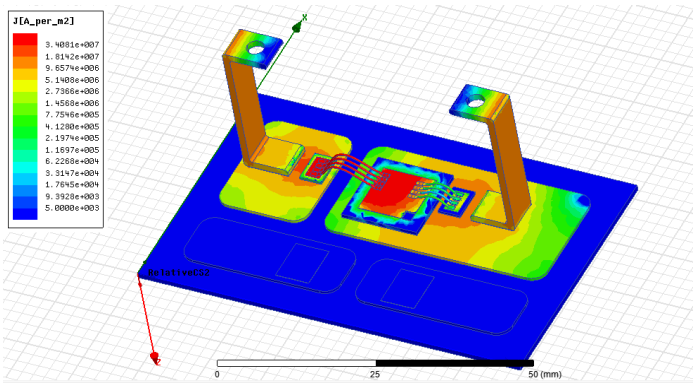


Figure 5.12: Current Distribution in the package

To simplify the FEM simulation, the current excitation has been set to a constant value at the terminals. Fig. 5.13 shows the electric field distribution of the package. As the terminals used have right angular boundaries, the electric field intensity is stronger at the edges.

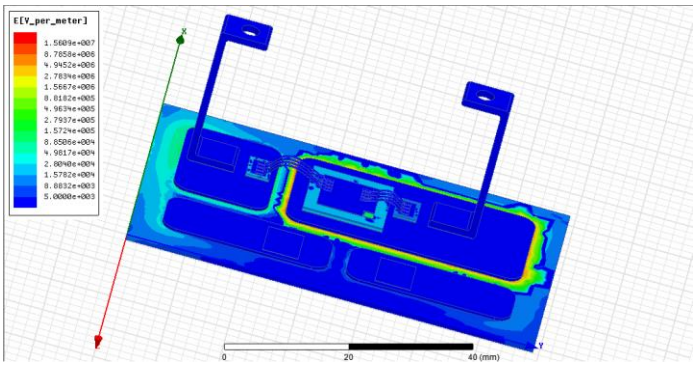


Figure 5.13: Voltage Distribution in the package

These FEM based Magneto-static and Electrostatic simulations have been done in ANSOFT MAXWELL.

5.6 Thermal Study

In order to obtain a basic understanding of initial thermal constraints of the package design, a Heat Transfer in Solids (conduction) study was done using COMSOL Multi-physics software. The thermal simulation analyzed the total power loss of the series current switch

package based on the summation of the typical, rated conduction loss and switching loss of both the Si-IGBT and SiC-Diode and I^2R losses of the DBC, as portrayed by Table 3.

Based on the total power dissipation conditions and the planar cross-sectional areas of the Si-IGBT and series SiC-Diode, appropriate heat source boundary conditions were established for the power die within the package. The Si-IGBT die has a planar cross-sectional area of 13.56mm x 13.56mm, and a die thickness of 0.670mm. The series SiC-Diode die has a cross-sectional area of 3.94mm x 5.70 mm, and a die thickness of 0.387mm. Therefore, specific heat flow rates were calculated for these die dimensions depending on the operating point of study as a function of switching frequency. The frequency dependent heat flow rates for each die were calculated based on the loss data of Table 3 and Equations 1 and 2 below.

*Si-IGBT Loss (f_{sw}) = (Total Rated Switching Loss + Conduction Power Loss)/(Si-IGBT die area) = (0.125J * f_{sw} + 105 W)/(13.56mm x 13.56mm) [W/m^2]* *(1)*

*SiC-Diode Loss (f_{sw}) = (Total Rated Switching Loss + Conduction Power Loss)/(SiC-Diode die area) = (0.01J * f_{sw} + 40 W)/(3.94mm x 5.70mm) [W/m^2]* *(2)*

It was assumed that the ambient temperature on the back-side of the DBC, where a cold-plate would be mounted, has a safe operating temperature of 45℃. During the package fabrication process, a silicone gel will be used as an encapsulate material to cover the top-side of the DBC substrate along with the power semiconductor die, the bottom third of the terminals, and the wire bonds. The silicone gel used in the simulation (Silopren* Gel 6209) has a thermal conductivity of 0.17 W/m-K and a thickness of 2.0 cm in order to electrically isolate the devices and interconnects up past the height of the wire bond loops. The thermal resistance of the silicone gel was calculated to be 0.09375 m^2K/W. This resistive boundary layer was taken into consideration within the thermal simulation as well, and was applied to

all top-side surfaces within the package that comes into contact with the encapsulate material. Simulations were also done without the silicone gel, simply using the thermal conductivity of air for all exposed top-side surface boundary conditions, and a negligible difference in thermal performance was observed. It should also be noted that the wire bond interconnects were removed from the 3D CAD model within COMSOL due to their negligible effect on the heat transfer compared to the entirety of the package.

5.7 Maximum Attainable Frequency

The thermal simulation is swept as a function of the overall loss in Si-IGBT and SiC-Diode at different frequencies for different isolation substrate materials. This will enable the maximum attainable frequency constraint for which the loss is same as that which leads to a peak internal temperature of 150℃.

Table 3: Typical loss data as a function of rated Current and Voltage at 150 °C

Parameters	**Value**
Conduction Power Loss of Si-IGBT	105 W
Total Switching Loss of Si-IGBT	$1.5e\text{-}4*I_C^2+1.8e\text{-}3*I_c+0.03$ J
Total Switching Loss of Si-IGBT (@ V=3600V and I_c=20A)	0.125J
Total Switching Loss of SiC-Diode (@ V=3600V and I_c=20A)	0.01J
Conduction Power Loss of SiC-Diode	40 W
I^2R Losses (using Aluminum Bond Wires)	36 W

According to the data sheets, typical loss data as a function of rated current and voltage is shown in Table 3. Using this table, the overall loss of IGBT and Diode is estimated as a function of frequency, as previously described in (1) and (2). All calculations have been done at V = 3600V and I_c = 20A. These loss data at different frequencies are used as boundary condition inputs to the COMSOL thermal model of the design.

Table 4: Material properties of the studied substrates [86]

Material	Thermal Conductivity [W/m*K]	Heat Capacity [J/kg*K]	Density [kg/m^3]
Alumina	27	765	3970
AlN	165	745	3260
BeO	270	1047	3000

The maximum temperature for each simulation is noted, and the maximum frequency for which the peak temperature is about 150 °C is tabulated. The isolation substrates studied were Alumina, AlN, and BeO. Table 4 shows the material properties of these substrates. Fig. 5.14-5.16 show the simulation results of the package at the maximum permissible frequency for Alumina, AlN and BeO substrates, respectively. As expected, the package with BeO as the insulation substrate limited the peak temperature to about 150℃ at a reasonably higher frequency compared to the Alumina and AlN substrates.

Table 5 shows the maximum attainable switching frequencies of the structure using these materials for which the maximum device temperature is held to approximately 150℃. Fig. 5.17 shows the variation of Peak Temperature as a function of switching frequency.

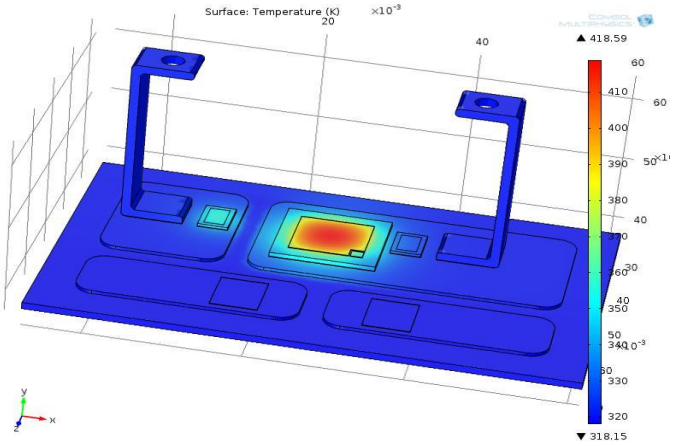


Figure 5.14: Temperature Distribution in the package with Alumina Substrate

This data can be further used for an optimum converter design. The size and efficiency of an overall converter comprising of power modules, magnetic components like inductors and transformers, and capacitors varies as a function of frequency. Higher frequency operation is preferred as it reduces the size of passive components. The data presented in this section can hence be used to model a high density power converter of desirable efficiency.

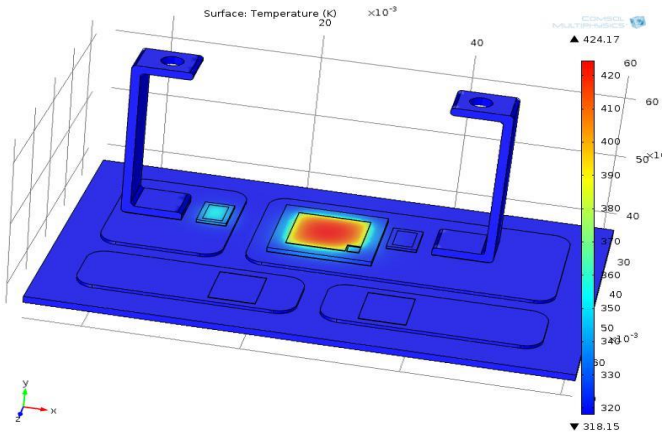


Figure 5.15: Temperature Distribution in the package with AlN Substrate

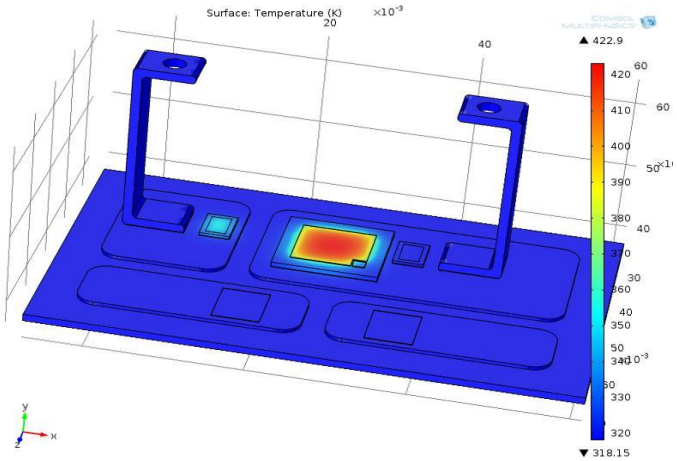


Figure 5.16: Temperature Distribution in the package with BeO Substrate

Table 5: Maximum attainable Switching Frequency

Material	Maximum Frequency (Hz)
Alumina	4000
AlN	10500
BeO	12000

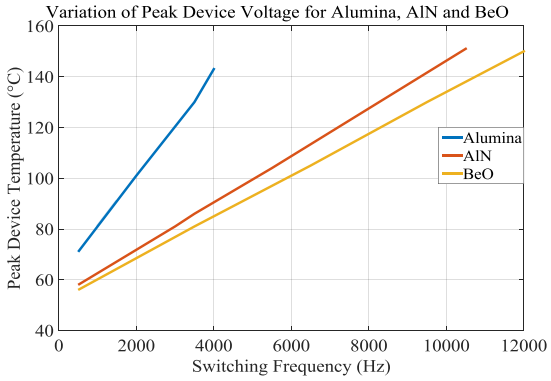


Figure 5.17: Peak Package Temperature as a funtion of Overall Loss of IGBT+Diode

5.8 Stacked Bond Wire Topology

Power semiconductor devices have top side metallization pads that do not always allow for the easy accommodation of multiple bond wires which are necessary to achieve the required current carrying capability and provide redundancy. With the advent of SiC and GaN devices, the accessible area has considerably shrunk reducing the cost of material and size of package. Due to the fast dI/dt transitions of these devices, the parasitic constraints are also stringent. One way of handling this is to add stacked bondwires one on top of other. This helps in better utilization of the pad area by providing reduction of inductance, resistance and leads to better thermal performance.

Fig. 5.18 shows a Q3D model of a single stacked bondwire. The value of inductance as a function of frequency is computed for single, double and triple bondwires connected in parallel to get a good understanding of the advantages in terms of reduction of inductance. As

shown in Tab. 6, the reduction of inductance can range from 14%-25% for these cases. Fig. 5.19 shows the physical manifestation of a stacked bondwire connected to a diode of small metallization area.

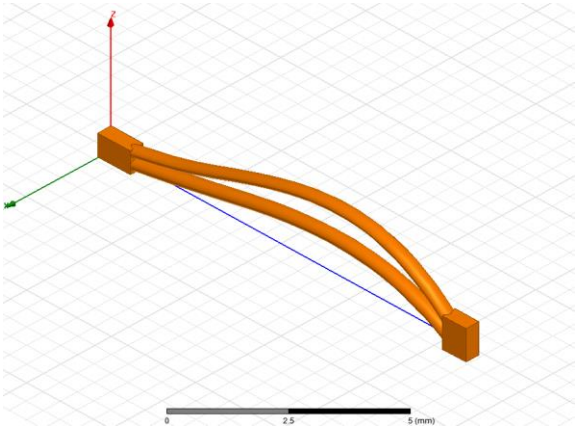


Figure 5.18: ANSYS Q3D single stacked bond wire (N=1)

Table 6: Wire bond inductance vs. frequency

Freq. (kHz)	**N=1**		**N=2**		**N=3**	
	Single	**Stacked**	**Single**	**Stacked**	**Single**	**Stacked**
0.1	8.3168	6.8123	5.9029	4.4167	4.7835	3.3936
100	8.268	6.6409	5.6564	3.7335	4.3419	2.6049
500	7.9685	6.2499	5.2933	3.4867	4.0324	2.4341
1000	7.7992	6.1103	5.1797	3.4250	3.9492	2.3926

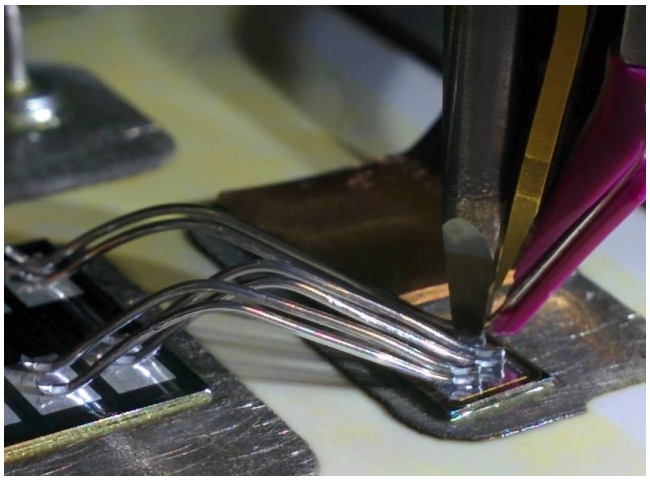


Figure 5.19: Stacked 15mil Al wire bonds from IGBT to diode

5.9 Hardware Testing Results

Hard-switching tests were performed on the custom, fabricated CSCSP. Fig. 5.20 shows the initial structure of the package. The outer casing is 3D printed for optimized terminal positions. Double Pulse Test has been conducted up to 4000V. Fig. 5.21 shows the hardware test setup. Special care has been taken to make sure the loop inductance of the circuit is as low as possible. The gate driver power supply has high voltage isolation for high side gating.

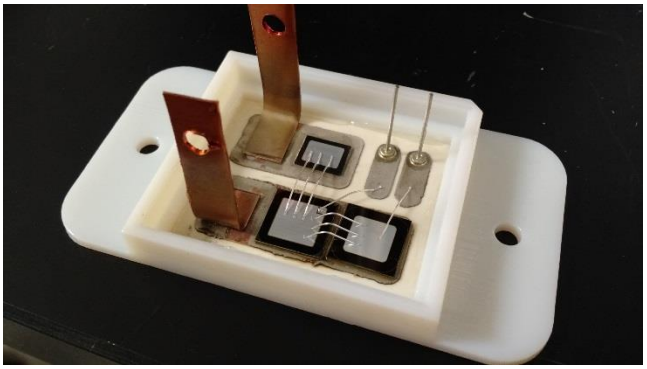


Figure 5.20: Custom, fabricated CSCSP – DBC based

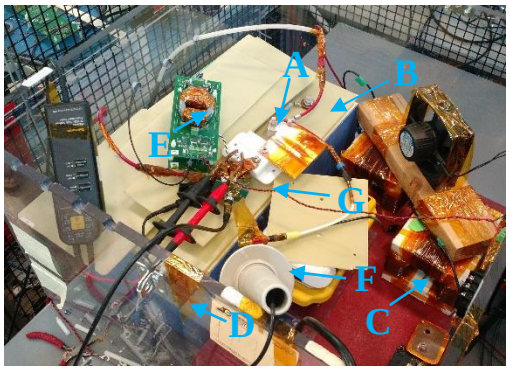


Figure 5.21: High-V double pulse test setup of CSCSP (A: CSCSP module, B: 10kV/10A SiC JBS diode, C: 8mH inductor, D: 250μF capacitor bank, E: gate driver, F: high-V probe, G: high-BW current probe)

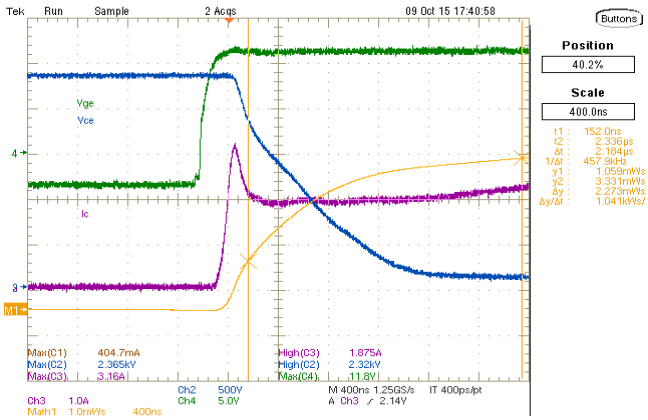


Figure 5.22: Turn-on transition of CSCSP at 2300V

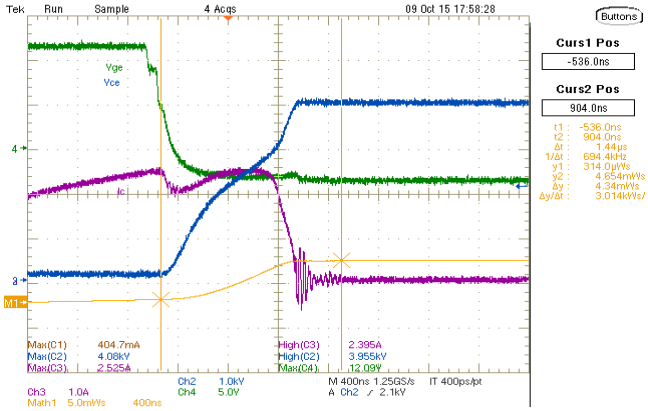


Figure 5.23: Turn-off transition of CSCSP at 4000V

Figure 5.22 and 5.23 shows double pulse test results (turn-on, turn-off transitions, respectively) at 2300V and 4000V. As it can be seen, the transitions were smooth with low overshoot voltage and current.

5.10 Conclusion

The main motive of the work is to demonstrate various package design considerations to accommodate series connection of high voltage Si-IGBT (6500V/25A Die) and SiC-Diode (6500V/25A die). Fundamental hard switching simulation results have been enumerated. Various ill effects of parasitic parameters have been listed. It has been shown that the series parasitic inductance leads to increased over-shoot voltage. The stray shunt capacitance on the

other hand leads to increased current spikes. The advantages of connecting the emitter to the anode, as opposed to cathode to collector, are shown in terms of effective series parasitic inductance. Variations of parasitic parameters as a function of substrate thickness, material, and terminal positions have been studied. Various critical crossover parameters have been shown graphically. The variation of series resistance is also noted as a function of bond wire material for completeness. FEM based current distribution in the package clearly showed the bond wire as the critical high current density hotspot. This further re-instated the assumption of minimizing the overall series parasitic inductance by minimizing the number of essential wire bond bridges. The heat transfer simulation provided useful thermal limit operating conditions based on allowable peak die temperatures. For this simplistic, non-heat sink case, the maximum attainable switching frequency is calculated for a safe operating internal temperature. However, during physical fabrication, an appropriate heat sink design should be used to ensure this safe operating condition. The main motivation of this work is to therefore put forward a set of detailed design considerations for packaging a high voltage current switch.

CHAPTER 6

MAGNETICS DESIGN

6.1 Introduction

Magnetic components are usually the bulkiest and most lossy elements in a current stiff converter. The fact that the inductor (or magnetising inductance of a transformer) is the primary power storage/tranfer element in the previously proposed converters, it tends to be the most critical design constraint in the circuit. Usually these magnetic components require high current carrying capability leading to high saturation limit and the high frequency current sweep capability leading to higher core losses. As we saw in both ZCS based Dyna-C and PRL converters in previous chapters, the peak current and the current sweep are considerably higher than other conventional converters. Therefore, an optimized magnetic design is required to make sure the overall converter efficiency and size is of the desired range.

To accommodate high peak current, usually a magnetic core with high Bsat is chosen. However, as the current sweep is also significantly higher (than conventional systems), a component with lower per-unit core loss is preferred. Nano-crystalline materials owing to high characteristic Bsat (~1.2T) therefore lead to highly efficient designs with smaller foot print. In the following subsections, modified Steinmetz equation has been used to design an efficient inductor. Variable permeability based designs are also studied to better utilize the overallvolume of the design. As for highly conductive magnetic materials, the eddy current loss due to fringging flux is non-negligible, two methods have been proposed to counter it.

The main motive of this chapter is to propose designs that lead to a more optimized magnetics system.

6.2 Loss Prediction and Inductor Proposal

The primary focus of this work is to come up with an optimized inductor structure which best matches the required specifications. An accurate derivation of Steinmetz parameter is required for sound prediction of Core Loss. An optimized winding structure has been proposed for minimum core size/weight. The inductor parameters (number of turns and air gap length) are varied and the various losses (copper and core) are tabulated. Two Inductor structures have been proposed: - (a) Low Weight + Moderate Loss and (b) Low Loss + Moderate Weight.

6.3 Derivation of Steinmetz Parameters

An effort has been made to accurately derive the Steinmetz parameters. The value of power loss has been raised by 10% to make sure that the equivalent model does not lead to an unreasonably optimistic power loss prediction. Fig. 6.1 shows the Core Loss curve for Nanocrystalline Core (www.magmet.com).

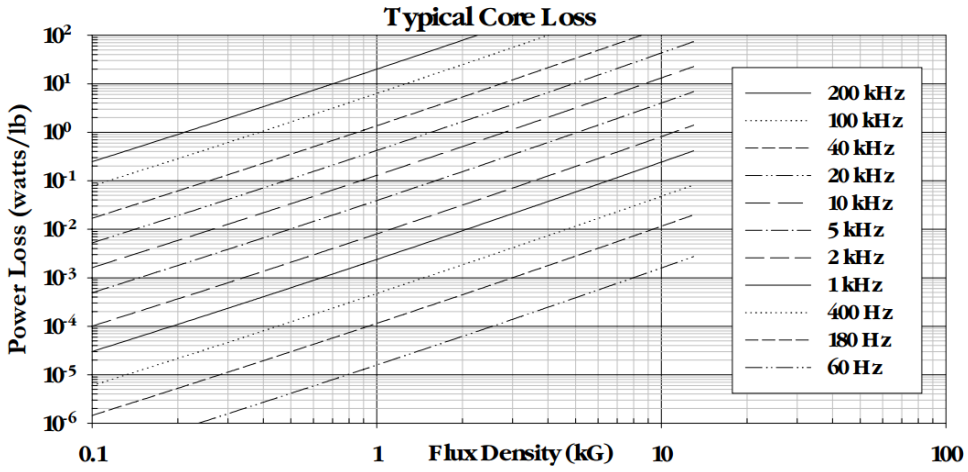


Figure 6.1: Typical Core Loss as a function of Flux Density

As it can be seen, the total number of data points are quite large. Therefore, a regression based method has been applied to find an average curve fitted set of parameter values. The Steinmetz equation for sinusoidal waveform is:

$$P = kf^{\alpha}B^{\beta}$$

$$\log(\mathrm{P}) = \log(\mathrm{k}) + \alpha\log(\mathrm{f}) + \beta\log(\mathrm{B})$$

Where P is the Power Loss in Watts/Lb, f is the frequency of excitation, B is the maximum Flux Density, and α, β and k are the constants for a given material. For different data points, a matrix structure can be made out of the above equation.

$$\begin{bmatrix} \log(P_1) \\ \log(P_2) \\ . \\ . \\ \log(P_n) \end{bmatrix} = \begin{bmatrix} 1 & \log(\mathrm{f}_1) & \log(B_1) \\ 1 & \log(\mathrm{f}_2) & \log(B_2) \\ . & . & . \\ . & . & . \\ 1 & \log(\mathrm{f}_n) & \log(B_n) \end{bmatrix} . \begin{bmatrix} \log(k) \\ \alpha \\ \beta \end{bmatrix}$$

$$\log\mathrm{P} = \mathrm{A} \,.\, \mathrm{X}$$

Here, logP is the matric on the left, A is the 2-D matrix and X is the parameters matrix. As A is not a square matrix, we cannot take direct inverse to get the parameters matrix. Therefore a regression based formula is used to get an averaged parameter matrix:-

$$\mathrm{X} = (\mathrm{A}^{\mathrm{T}} \,.\, \mathrm{A})^{-1} \,.\, \mathrm{A}^{\mathrm{T}} \,.\, \log\mathrm{P}$$

Following are the values of the parameters derived from 50 data points:-

$$\alpha = 1.7515$$

$$\beta = 2.037$$

$$\mathrm{k} = 1.3547\mathrm{e}{-6}$$

6.4 Preferred Core Geometries

It is important to select an optimized core geometry to meet the minimum weight and loss requirement. A simple structure as shown in Fig. 6.2 is selected for this application. The number of windings are divided in to ‘M’ rows and ‘N’ columns thereby making the number of windings equal to M*N. As an example a 6*5 and 5*5 winded inductors are shown in Fig. 6.3.

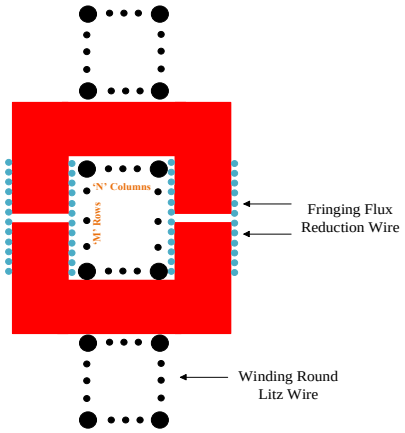


Figure 6.2: A generic inductor structure.

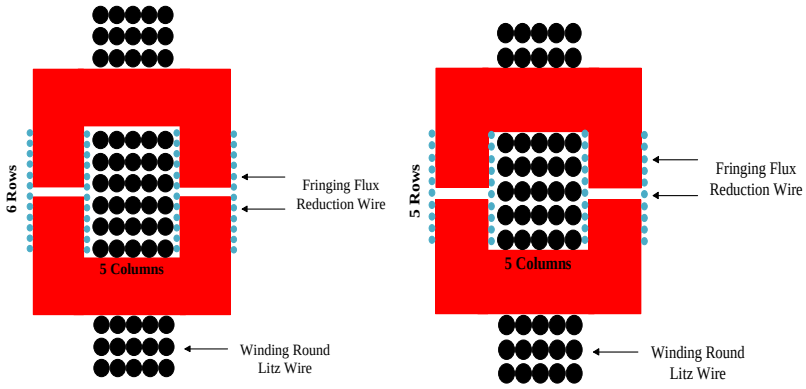


Figure 6.3: (a) A 30 turns Inductor structure (b) 25 turns Inductor structure

For different number of turns an optimized arrangement (values of M and N) is shown in Tab. 1. This is to ensure minimum magnetic material usage which leads to minimum core size, weight and volume and minimum core loss.

Table 1: The value of number of rows and columns of the winding structure

Number of Turns (X)	M	N
6,7,8,10	2	X/2
9	3	3
11,12	3	4
13,14,15,16	4	4
17,18,19,20	4	5
21,22,23,24,25	5	5

6.5 Variation of Weight and Losses as a function of Inductor Parameters

The number of turns and air gap length has been varied to find the variation of weight and loss for the corresponding inductor. The main motive of this study is to find the parameters which would lead to optimum inductor design. Fig. 6.4 and 6.5 shows the graphical representation of this variation in terms of Weight and Power loss.

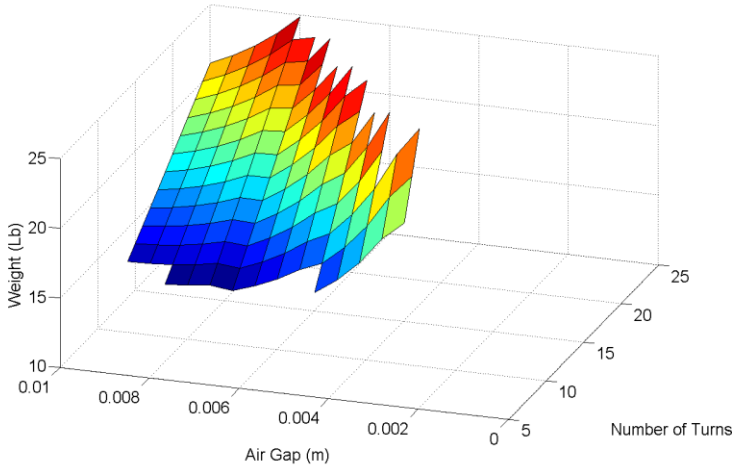


Figure 6.4: Overall Weight in Lb as a function of number of turns and air gap length

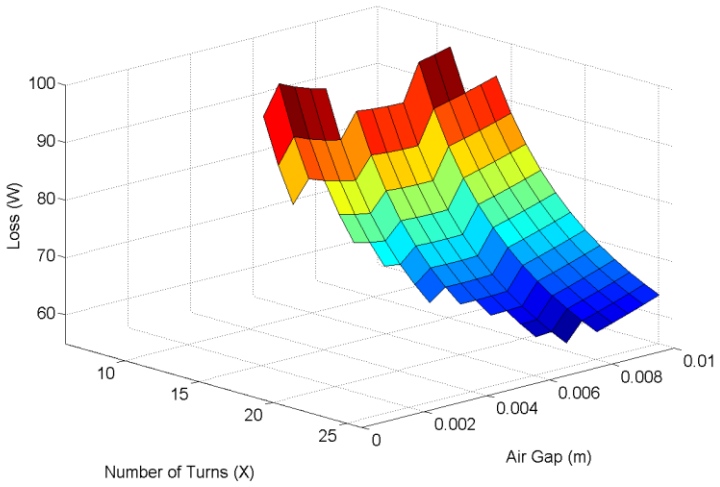


Figure 6.5: Overall Power Loss in Watts as a function of number of turns and air gap length

Only the data points which leads to an overall loss lower than 100W have been plotted. The weight constraint has been relaxed to show a continuous trend. Tab. 2 shows the preferred tabulation of all the data points which resulted in under 100W and under 15lb.

Table 2: Variation of Loss and Weight as a function of number of turns and air gap

Turns	**Air Gap**	**Core Weight (Lb)**	**Wire Weight (Lb)**	**Core Loss (W)**	**Copper Loss (W)**	**Total Weight (Lb)**	**Total Loss (W)**
15	0.0035	9.466068	4.792294	80.98822	15.86415	14.25836	96.85237
16	0.0035	8.142155	5.031387	79.44858	16.65562	13.17354	96.1042
16	0.004	9.51557	5.202692	70.73786	17.2227	14.71826	87.96057
17	0.004	8.952563	5.122994	75.30028	16.95888	14.07556	92.25916
18	0.004	7.850975	5.362087	74.18881	17.75036	13.21306	91.93917
18	0.0045	8.988373	5.52298	66.81873	18.28297	14.51135	85.1017
19	0.004	6.938304	5.601179	73.19799	18.54184	12.53948	91.73982
19	0.0045	7.938256	5.762073	65.88298	19.07445	13.70033	84.95743
19	0.005	8.959703	5.914249	59.99758	19.5782	14.87395	79.57579
20	**0.004**	**6.174096**	**5.840272**	**72.30964**	**19.33331**	**12.01437**	**91.64295**
20	0.0045	7.059601	6.001165	65.04371	19.86593	13.06077	84.90963
20	**0.005**	**7.963535**	**6.153342**	**59.20018**	**20.36968**	**14.11688**	**79.56987**
21	0.004	5.982353	6.238759	77.38512	20.65244	12.22111	98.03757
21	0.0045	6.828402	6.399653	69.48753	21.18506	13.22806	90.67259
21	0.005	7.690372	6.551829	63.14327	21.68881	14.2422	84.83209

22	0.004	5.391232	6.637247	76.6704	21.97158	12.02848	98.64198
22	0.0045	6.150593	6.79814	68.81118	22.50419	12.94873	91.31537
22	0.005	6.9238	6.950317	62.49979	23.00795	13.87412	85.50773
22	0.0055	7.710141	7.095057	57.31647	23.48708	14.8052	80.80356
23	**0.004**	**4.882806**	**7.035734**	**76.02105**	**23.29071**	**11.91854**	**99.31175**
23	0.0045	5.567945	7.196628	68.19642	23.82332	12.76457	92.01974
23	0.005	6.265201	7.348804	61.91469	24.32708	13.61401	86.24176
23	0.0055	6.973952	7.493544	56.75716	24.80622	14.4675	81.56338
24	0.0045	5.063575	7.595115	67.63549	25.14245	12.65869	92.77794
24	0.005	5.69537	7.747292	61.38062	25.64621	13.44266	87.02683
24	0.0055	6.33728	7.892032	56.24648	26.12535	14.22931	82.37183
25	0.0045	4.624163	7.993603	67.12185	26.46158	12.61777	93.58344
25	0.005	5.19916	8.14578	60.89141	26.96534	13.34494	87.85675
25	0.0055	5.783108	8.290519	55.77855	27.44448	14.07363	83.22303
25	**0.006**	**6.375588**	**8.428816**	**51.50518**	**27.90229**	**14.8044**	**79.40747**

The weight constraint was relaxed to find the most power efficient case. A set of noteworthy results is mentioned in the next section.

6.6 Proposed Inductor Structures

Out of the various results, few structures stood out: -

Table 3: Preferred Design Set

Turns	**Air Gap**	**Core Weight (Lb)**	**Wire Weight (Lb)**	**Core Loss (W)**	**Copper Loss (W)**	**Total Weight (Lb)**	**Total Loss (W)**
20	0.004	6.174096	5.840272	72.30964	19.33331	12.01437	91.64295
20	0.005	7.963535	6.153342	59.20018	20.36968	14.11688	79.56987
23	**0.004**	**4.882806**	**7.035734**	**76.02105**	**23.29071**	**11.91854**	**99.31175**
25	**0.006**	**6.375588**	**8.428816**	**51.50518**	**27.90229**	**14.8044**	**79.40747**
20	**0.0075**	**12.73056**	**6.81981**	**41.43496**	**22.57592**	**19.55037**	**64.01088**

The conclusion of this report therefore is a proposal to build two inductors out of the above mentioned specifications: -

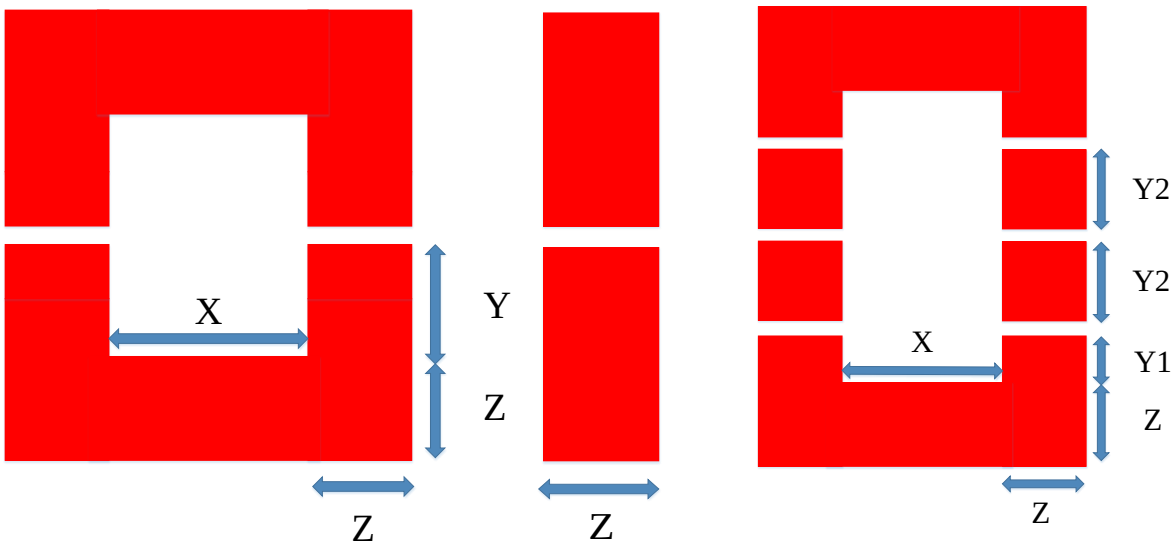


Figure 6.6(a): Design #1: Front View, (b): Design #1: Side View, (c) Design #2: C-Core with distributed Air Gaps

Design	X (in inches)	Y (in inches)	Z (in inches)
1	4.2	4.2	1

Design	X (in inches)	Y1 (in inches)	Y2 (in inches)	Z (in inches)
2	3.36	1.1	1	1.6

6.7 Uniform Flux Magnetics Design using non-uniform Magnetic Material

6.7.1 Introduction

The design of inductors/transformers used in high frequency converters has been very popular in recent years because it plays an important role in increasing the power density and in improving the efficiency. One of the most important concerns in high-frequency high-power conversion is the design of magnetic components. In conventional high frequency converters, the inductors are usually constructed with high permeability commercial magnetic cores and copper litz wires. It has been well studied that these uniform magnetic

materials have non-uniform flux distribution. This is true for both torioidal and rectangular (C/E/I type) cores. This results in the magnetic material closer to the conductor becoming saturated while the magnetic material far away from the conductor is still not fully utilized. This inevitably leads to insufficient utilization of magnetic material space/volume.

It is also important to obtain very low leakage inductance values, while simultaneously ensuring that the leakage flux is not concentrated in a small section of the core used. Further, transformer designs which feature an analytically calculated leakage inductance are appealing for use in soft switching circuits in which the leakage inductance is a useful circuit component. The use of coaxial transformers for high-frequency, high power converters effectively suit these applications. The design of such coaxial transformers is considerably different from that of conventional transformer structures.

6.7.2 Applications

Non-Air Gap Cores

When toroidal cores are used, the core flux distribution is well defined and controlled. Essentially none of the leakage flux finds its way into the core. The core flux distribution is, however as previously mentioned, non-uniformly spread across the radius of the core, and indicates that core loss depends on the ratio of the toroidal core inner and outer radii. Fig. 6.7 shows this un-even flux distribution. Maxwell 2D simulation was used to study this effect. It can be easily derived that the value of this field as, $B = \frac{\mu_r \mu_0 NI}{2\pi r}$. Hence the total inductance can be derived as $L = N^2 h \int_{Ri}^{Ro} \frac{\mu_r . \mu_0}{2\pi r} * dr$, where R_O and R_i are the outer and inner radii of the toroid and 'h' is the height of the core.

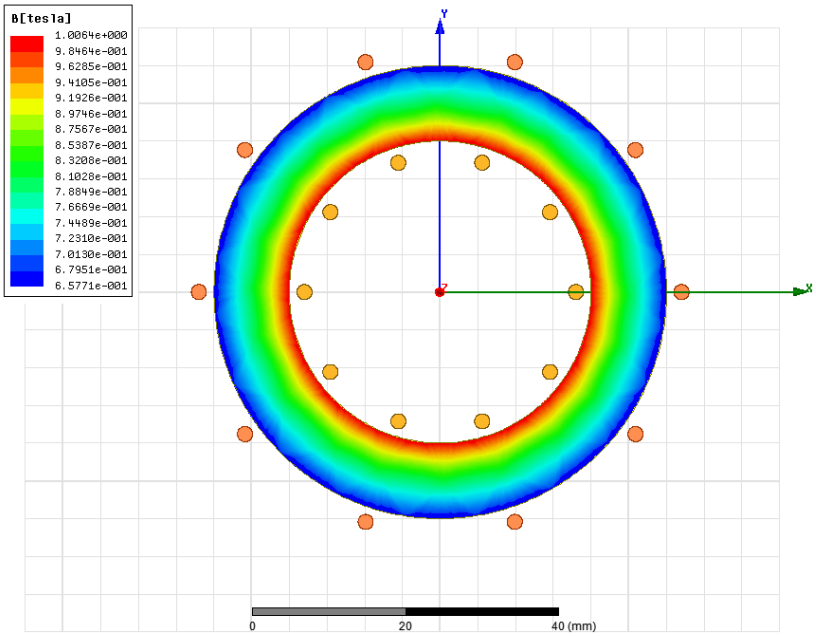


Figure 6.7: Uneven Distribution of Magnetic Field in uniform Toroidal Core

The same concept can be extended to co-axial transformers where the field distribution is non-uniform. Fig. 6.8 shows the 3D model of the understudied transformer and Fig. 6.9 shows the magnetic field distribution. As expected, the field distribution is non-uniform.

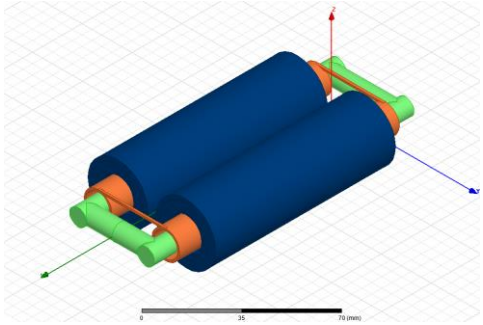


Figure 6.8: 3D model of the Co-axial Transformer

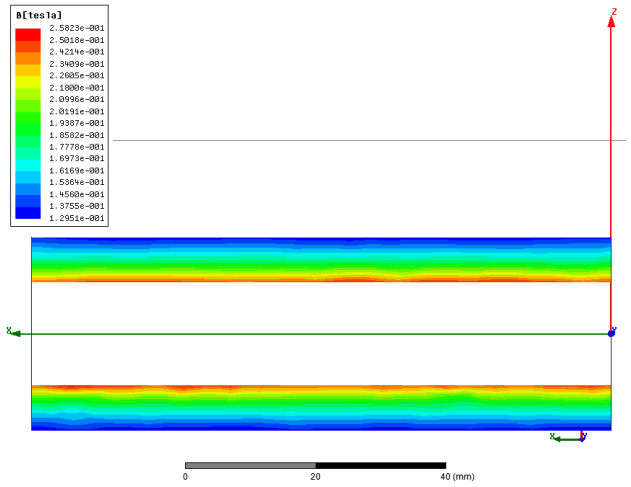


Figure 6.9: Magnetic Field Distribution in the toroidal cores of the Co-axial Transformer mentioned in Figure 3

It can be easily seen that the value of magnetic field is a strong function of relative permeability and radius 'r'. If the value of this relative permeability is varied as a function of 'r', the flux distribution can be set to our requirement. The value of this field is $B = \frac{\mu_r(\mathrm{r})\mu_0 NI}{2\pi r}$ and therefore the value of overall inductance can also be expressed as $L = N^2 h \int_{Ri}^{Ro} \frac{\mu_r(\mathrm{r}).\mu_0}{2\pi r} * dr$. For uniform flux, the distribution of $\mu_r(\mathrm{r})$ can be so chosen to nullify the decaying effect of $\frac{1}{r}$. This can be easily achieved by linearly increasing the μ_r as a function of 'r'. To study this, the 2D simulation of a simple toroidal inductor was modified. Two configurations have been studied. The uniform core was first divided into two and then into ten subsections with linearly varying relative permeability. Fig. 6.10 shows the flux distribution of this configuration of the case with two and Fig. 6.11 shows the distribution of the case with 10 subdivided cores.

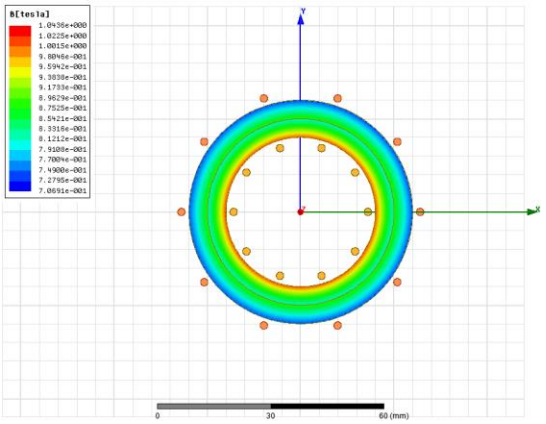


Figure 6.10: Distribution of Magnetic Field in non-uniform Toroidal Core. It uses two different concentric cores of proportionally adjusted relative permeability

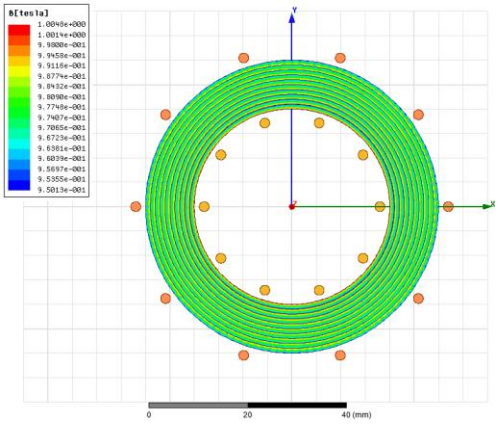


Figure 6.11: Distribution of Magnetic Field in non-uniform Toroidal Core. It uses ten different concentric cores of proportionally adjusted relative permeability

This clearly shows that as the granularity of the concentric cores are increased; the distribution becomes more and more uniform. This also affects the net inductance value. With the uniform distribution, the value of B is set to uniformly high value throughout the core. An estimated increase of inductance can be derived as $k = \frac{\frac{r_o}{r_i} - 1}{\ln\left(\frac{r_o}{r_i}\right)}$. For all values of $\frac{r_o}{r_i}$

which are greater than 1, the value of ‘k’ is greater than 1. The same logic can be used in the case of co-axial winding transformer. Fig. 6.12 shows field distribution of non-uniform core in co-axial winding transformer.

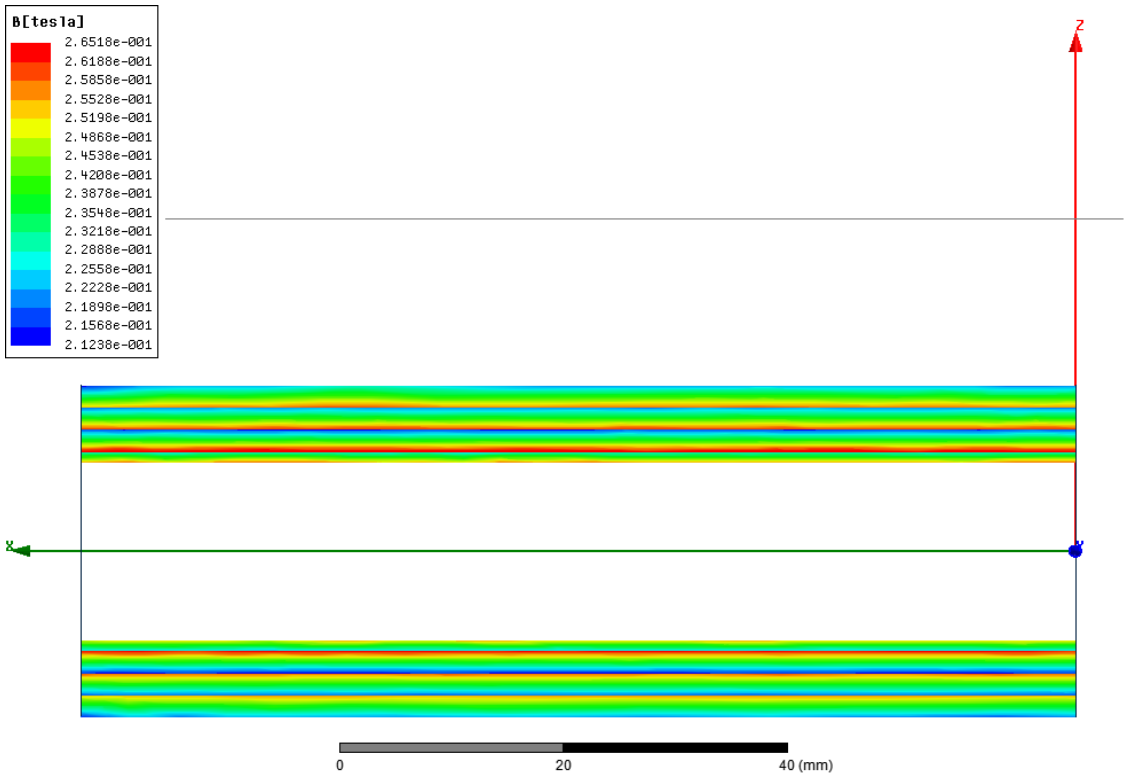


Figure 6.12: Magnetic Field Distribution in the toroidal cores of the Co-axial Transformer. The core can been divided into three concentric hollow cylinders of linearly increased relative permeability

6.7.3 Gapped Cores

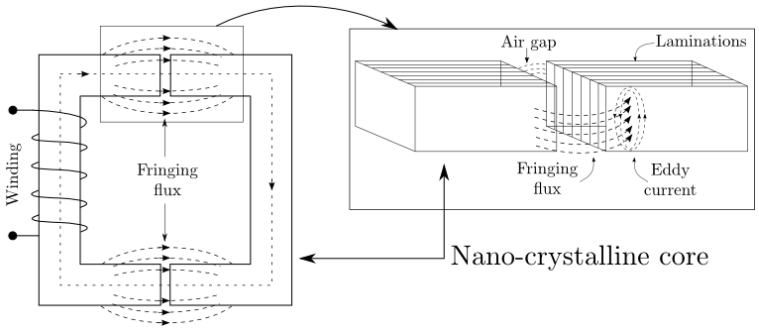


Figure 6.13: Air gap losses due to fringing flux in an inductor

High frequency high power converters, usually requires inductors with large saturation current capability. To accommodate this, large values of air-gaps are needed. This however raises a major concern in case of high conductive cores as it leads to high air gap losses caused by the fringing flux. These cores come with thin laminations as shown in Fig. 6.13. The fringing flux in the air gap hits the core almost perpendicularly. This causes huge eddy current and losses in the core material.

It can be shown that an appropriate variable permeability configuration can help reduce this problem. Preliminary FEM simulations show that if the permeability is higher at the edges as compared to the middle of the core, the overall fringing flux reduces. Fig. 6.14 shows three configurations: (a) Core with lower permeability at the outer layers and higher towards the middle, (b) Core with uniform permeability and (c) Core with higher permeability at the outer layers and lower in the middle. The fringing flux for (a) was more widespread than (b) and (b) was more widespread than (c).

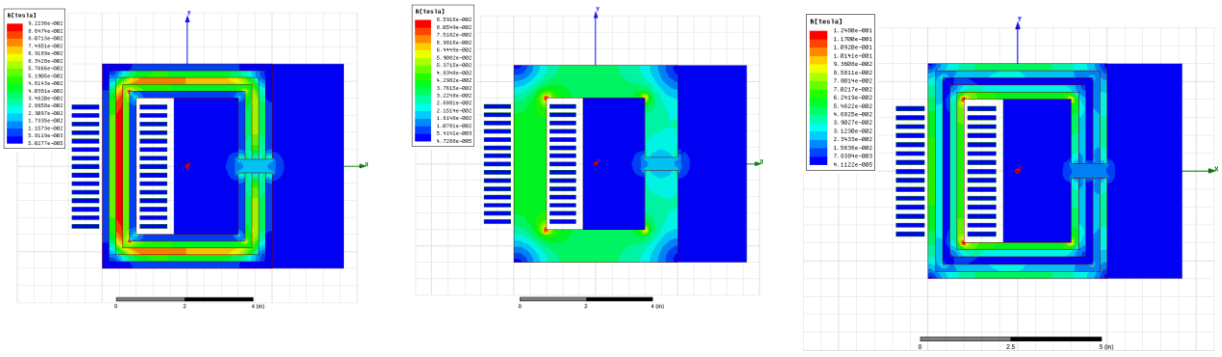


Figure 6.14:(a) [Left] Core with lower permeability at the outer layers and higher towards the middle, (b) [Middle] Core with uniform permeability and (c) [Right] Core with higher permeability at the outer layers and lower in the middle.

6.8 Conclusion

The main advantage of using a variable permeability based core as opposed to conventional cores is the fact that the entire core volume is fully utilized to the maximum field strength. This leads to higher inductance for the same/similar volume of the structure. This feature can be used to optimize the size and weight of high frequency magnetics. For transformers, this would result in higher magnetizing inductance thereby reducing the frequency of operation without affecting the size of the converter. For gapped magnetics design, it is shown that certain configuration of permeability variation leads to lower fringing flux which can greatly reduce the overall loss.

CHAPTER 7

DVC MODELLING AND VOLT-VAR CONTROL FOR DISTRIBUTION FEEDERS**

7.1 Introduction

One of utilities important function is to maintain the voltages on a distribution feeder within a target range, and the common practice in United States is to follow the ANSI C84.1 [89] which specifies the range for both service voltage and utilization voltage. On a conventional radial distribution feeder, the common devices employed for voltage control are voltage regulators (VRs) and capacitors. With proper placement of, and coordination between, these Volt-VAR compensators, voltages along a feeder can be kept within acceptable limits under typical load conditions.

Recent interest in connecting small scale renewable energy based generation systems to distribution feeders, partly spurred by the adoption of Renewable Portfolio Standards [90], poses challenges to the conventional Volt-VAR control (VVC) schemes [91]. Connection of large amount of residential scale PV in particular is a challenging case, as it can introduce a highly fluctuating power swing on a distribution feeder [92].

Main impacts of large amount of PV on a feeder include increased voltage variation (voltage rise and voltage fluctuation) along the feeder, negative impact on VRs and Capacitors operation (voltage control logic, excessive tap movements of VRs and Load Tap Changers, LTCs), and coordination between protection devices.

Conventional devices (substation LTC, VRs and Capacitor Banks) employed for VVC on a distribution system act on local information and they are slow acting devices. Hence, these devices respond poorly to voltage variations caused by fast power variations from PVs

**The IEEE-34 BUS Feeder simulation and all of system based work was done by Wenbo Zhang. The impact of DVC in IEEE-34 BUS Feeder system was a collaborative work done by myself and Wenbo. The work presented in this chapter primarily constitute the modelling of DVC (average dynamical) and its impact in the IEEE-34 BUS system [75].

during a cloudy day. Recently, power electronics based VAR compensators have been proposed to address these challenges, as they can respond to voltage variations much faster and thus provide much more effective VAR compensation on a distribution system [93]-[94]. This report discusses the design and performance of a Dynamic VAR Compensator (DVC) in an IEEE-34 Bus Feeder system. At first a PSCAD based DVC model is established to simulate its dynamic behavior. A PSCAD based IEEE-34 Bus Feeder model is then made and tested without any compensator, with shunt-capacitor compensator and with DVC. Next, a PSCAD based model is made which incorporates a time varying load profile. The system is studied paying close attention to voltage profile at several nodes and voltage at a specific node over a period of time. This has further been extended by adding a PV in the PSCAD based system but without the DVC. The main motive of the chapter is to make a fair judgment on the performance of DVC in both static and time varying load system, discuss the design specification and simulate the effect of DVC in the feeder with time varying load profile. Thus, the work presented in this report will form the base of further exploitation of the topic. The co-ordination between the DVCs will be established for decision-making and the combined performance will then be studied.

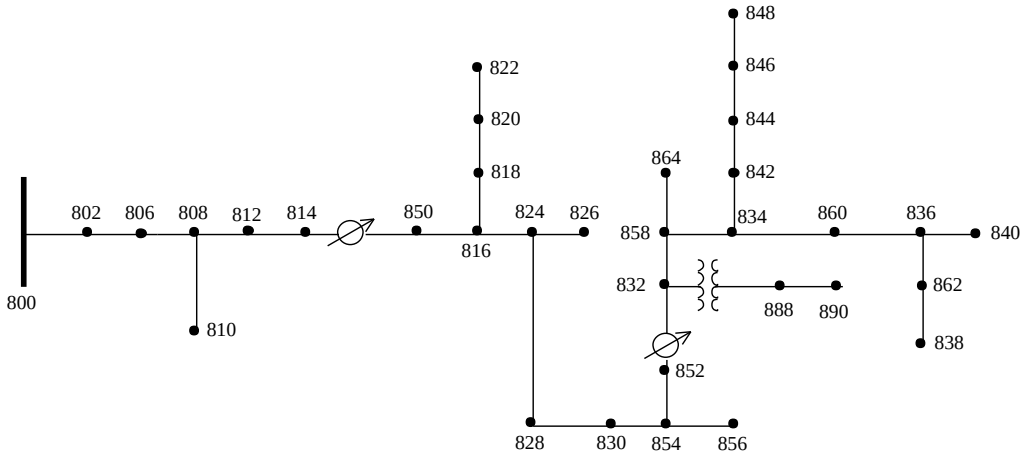


Figure 7.1: IEEE-34 Bus Feeder

7.2 The Feeder Model

The single line diagram of the IEEE-34 Bus feeder is shown in Fig. 7.1. The system has unbalanced circuit parameters and unbalanced loads. The basic feeder has been modeled in both MATLAB and PSCAD. The MATLAB model has already been presented. This report will mostly concentrate in the PSCAD implementation. A time-varying load has been implemented in the system. There are two Voltage Regulators (tap-changers) in the system which ramps up the voltage profile at certain nodes. This ensures that the Voltage Profile of the nodes from left to right and through the branches may not always be monotonically decreasing.

7.3 Proposed Power Electronic DVC

Fig. 7.2 shows the basic structure of the proposed Dynamic VAR Compensator (DVC). As it can be seen it contains six unidirectional switches.

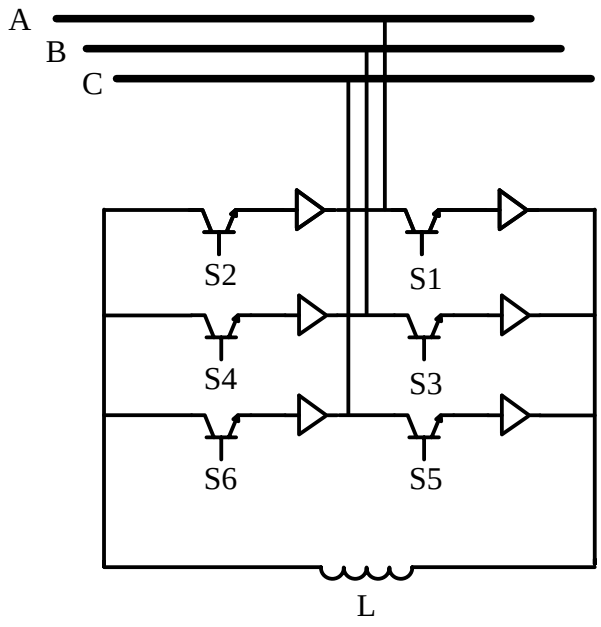


Figure 7.2: Circuit schematic of DVC

The proposed VAR compensator can provide both capacitive and inductive reactive power as and when required by the system. It usually takes just one switching time period to provide required reactive power to the system.

7.3.1 Principle Of Operation

The current reference can be generated such that the expected VAR compensation meets the reference and the phase difference between phase voltage and current is $\pi/2$ (positive or negative depending inductive or capacitive compensation requirements). For simplicity, we would consider the inductive compensation case. The capacitive compensation algorithm is exactly same but with reverse current/voltage orientation.

Once the current reference has been set (lagging voltage by $\pi/2$), depending on the voltage sector as shown in Fig. 7.3 and Fig. 7.4, a particular switching sequence is followed.

At first, depending on the particular sector, the current with maximum magnitude is identified. For example, in sector 1, $|I_c|$ is greater than both $|I_a|$ and $|I_b|$. Now, depending on the sign of I_c (i.e. the current with maximum absolute value) preferred corresponding switch are turned on (S6 – as I_c is negative in sector 1). The voltage applied to the inductor can be either V_a-V_c or V_b-V_c depending on the choice of complementary switch (to be turned on simultaneously with S6). As Va-Vc is positive in sector 1, S1 is turned on with S6. Once the S1-S6 pair is turned on, the inductor current starts rising at the rate of $(V_a$-$V_c)/L$ as shown in Fig. 7.5. The duration of conduction can be determined by equating the average of this triangular current wave to the reference current.

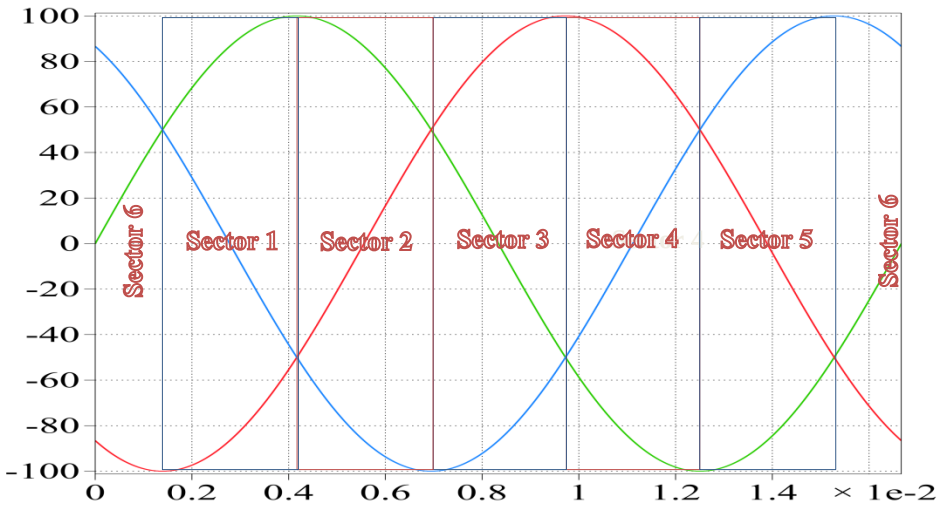


Figure 7.3: Three Phase sinusoidal Input Voltage divided into six sectors (green: A, red: B and blue: C)

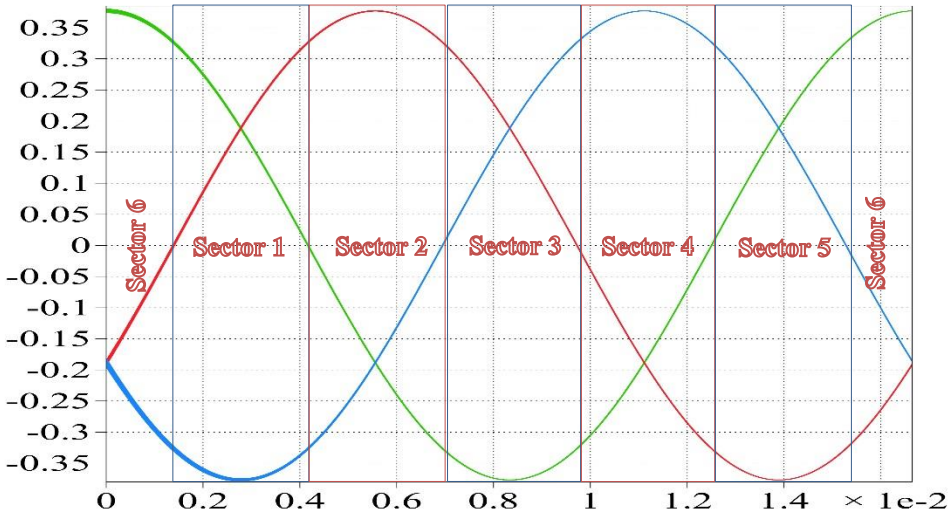


Figure 7.4: Three Phase sinusoidal I/P Reference Current divided into six sectors (green: A, red: B and blue: C)

If the Time Period is 'T',

$$<|I_C|> = 0.5 * t^2 * (V_a - V_c) / (L * T) \ldots \text{(i)}$$

Therefore, the preferred value of 't' derived from (i) is:

$$t = \sqrt{\frac{2 * I_c * T * L}{(V_a - V_c)}} \ldots \text{(ii)}$$

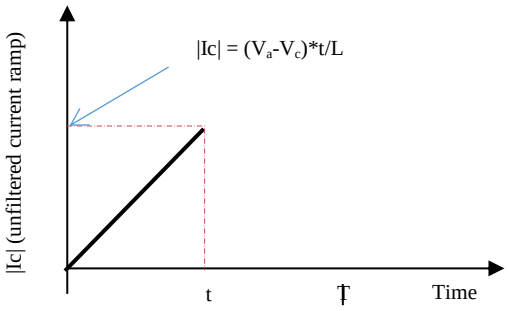


Figure 7.5: Triangular shaped current of Phase C in sector 1

Just before the system reaches time ‘t’, switches S2-S3 are turned on. Though pair S2-S3 is turned on, they would not conduct as the series connected diodes are in reverse biased condition. After time ‘t’, when switches S1-S6 are turned off, S2-S3 starts conducting. During this operation, a negative voltage is applied to the inductor and it starts discharging back to the grid till it reaches zero current. This would naturally commute the series connected diodes off thereby mitigating the losses. This operation is repeated cycle by cycle thereby providing reactive power to the grid. The preferred switching sequence is mentioned in Tab. 1.

Table 1: Switching scheme

Sector	Switched First	Switched Second
1	S1,S6	S2,S3
2	S3,S6	S2,S5
3	S2,S3	S4,S5
4	S5,S2	S1,S4
5	S4,S5	S1,S6
6	S1,S4	S3,S6

7.3.2 Simulation Results And Initial Hardware Results

This system has been simulated. Fig. 7.6 shows the input phase voltage and unfiltered phase current. A hardware setup has been built to verify its operation. Various sectors of operations have been verified using a DSP controller. The converter works under simplified controller (an equivalent polynomial fit for the non-linear calculation of ‘t’. Fig. 7.7 shows an initial

test result. To get harmonic free input current, a look-up table based approach is presently being investigated.

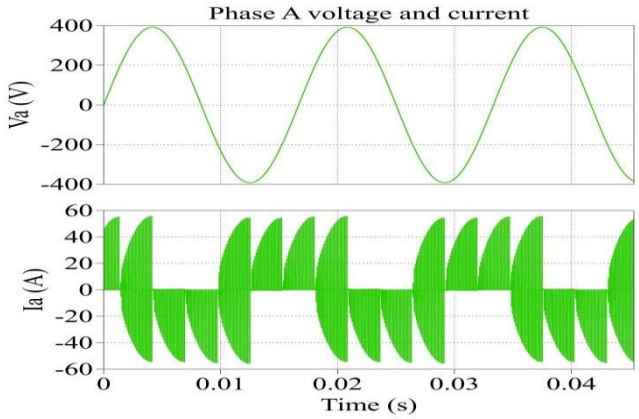


Figure 7.6: Phase Voltage and unfiltered phase current

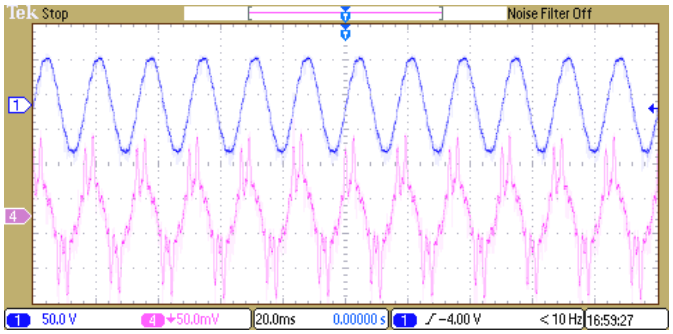


Figure 7.7: Hardware test result; (blue): voltage; (pink): current

7.4 Dynamic Model of DVC

Figure 7.8 shows an equivalent DVC model built in PSCAD to simulate its dynamic behavior when interfaced with the grid. Instead of detailed switching model, the topology is realized by controlled voltage and current sources on both AC input and DC output side. The controller calculates three phase reference voltage and sends it back to the three phase controlled voltage sources. Figure 7.8(b) shows the vector control algorithm adopted for regulating the power flow. The initial few results are controlled in open loop condition. Iq_ref has been manually fed to the system. DVC provides larger reactive power when Iq_ref is set to a larger value. This trend is then utilized to close the loop using the grid voltage

mismatch compared to a set value of 1p.u. These models are made in PSCAD and integrated with the IEEE-34 Bus feeder.

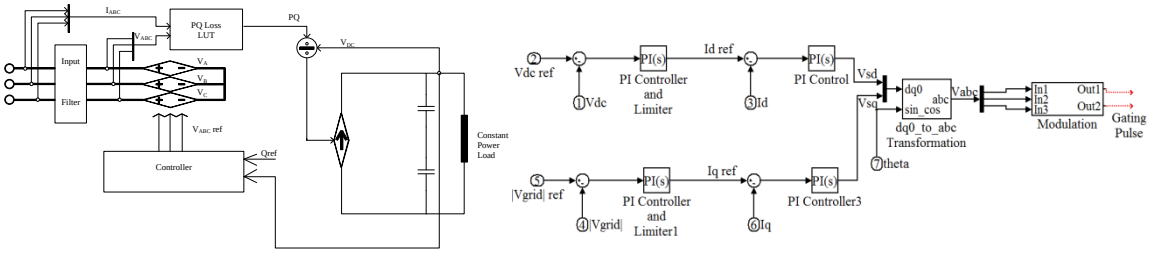


Figure 7.8: (a) DVC Dynamic Model; (b) DVC Control (simplified)

7.5 Study cases

7.5.1 Time-invariant Load with VRs

Base case

In this study case, capacitor banks or DVCs are not integrated in the system. The simulation runs under peak load condition. As we can see in Fig. 7.9, Node 890 has a major voltage violation. Other nodes with similar problems are not connected with any load (eg:-814,812,etc). Fig. 7.10 shows the TAP number as a function of time. As it can be seen there exists an obvious problem as the TAP number hits the max allowed position. This signifies the need of an external compensator to minimize the number of required TAP changes.

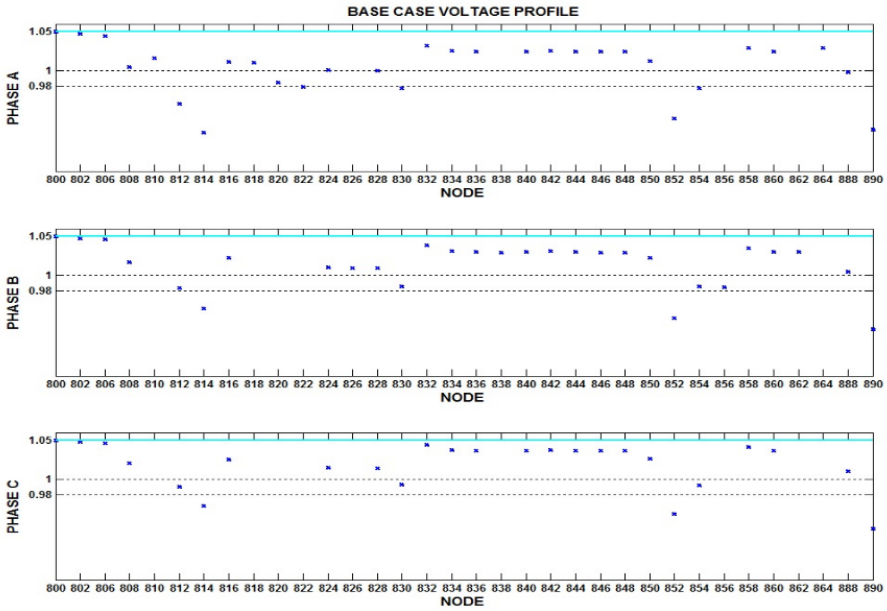


Figure 7.9: Voltage Profile for the Base Feeder at Peak Load Condition

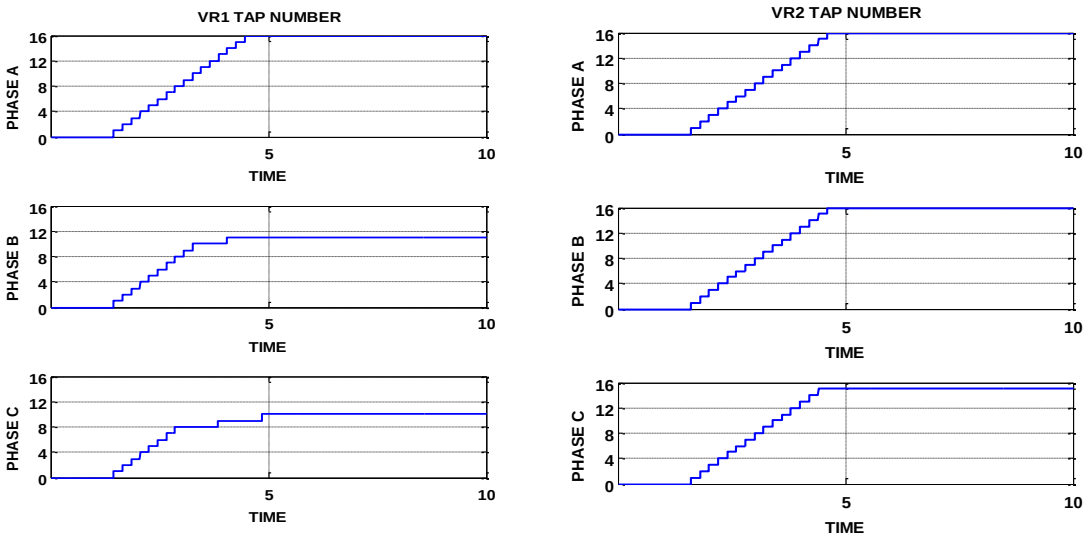


Figure 7.10: (a) Voltage Regulator 2 Tap change Profile, (b) Voltage Regulator 1 Tap change Profile

Shunt Capacitor at Node 848

A three phase shunt Capacitor is added to Node 848. It shifts the level of few of the nodes up as compared to the Base Feeder case. Node 890 continues to be a concern. Fig. 5.11 shows the TAP number as a function of time. Fig. 5.12 shows the Voltage profile of the feeder under peak load condition. Now, the peak TAP number (13) is less than the maximum allowed (16). This signified a stable system.

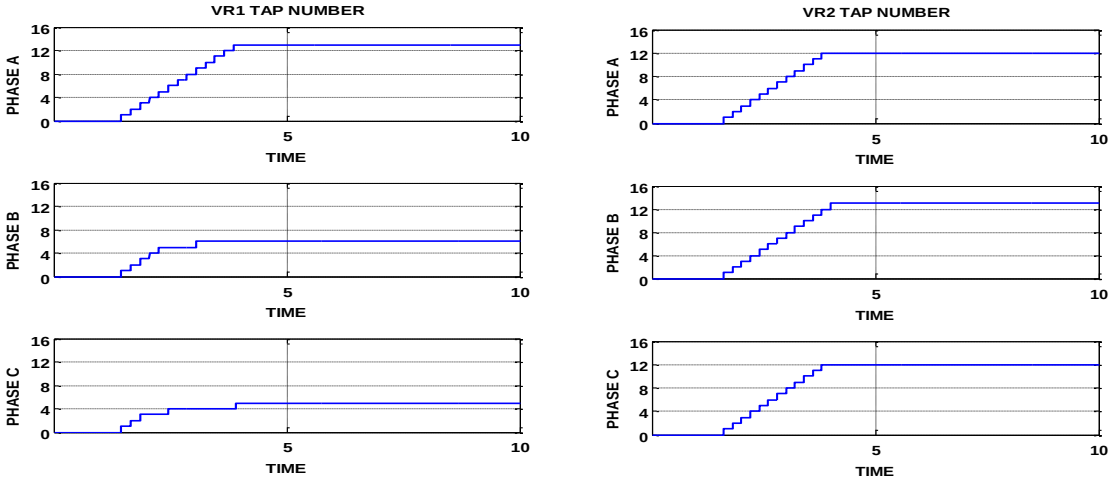


Figure 7.11: (a) Voltage Regulator 2 Tap change Profile, (b) Voltage Regulator 1 Tap change Profile

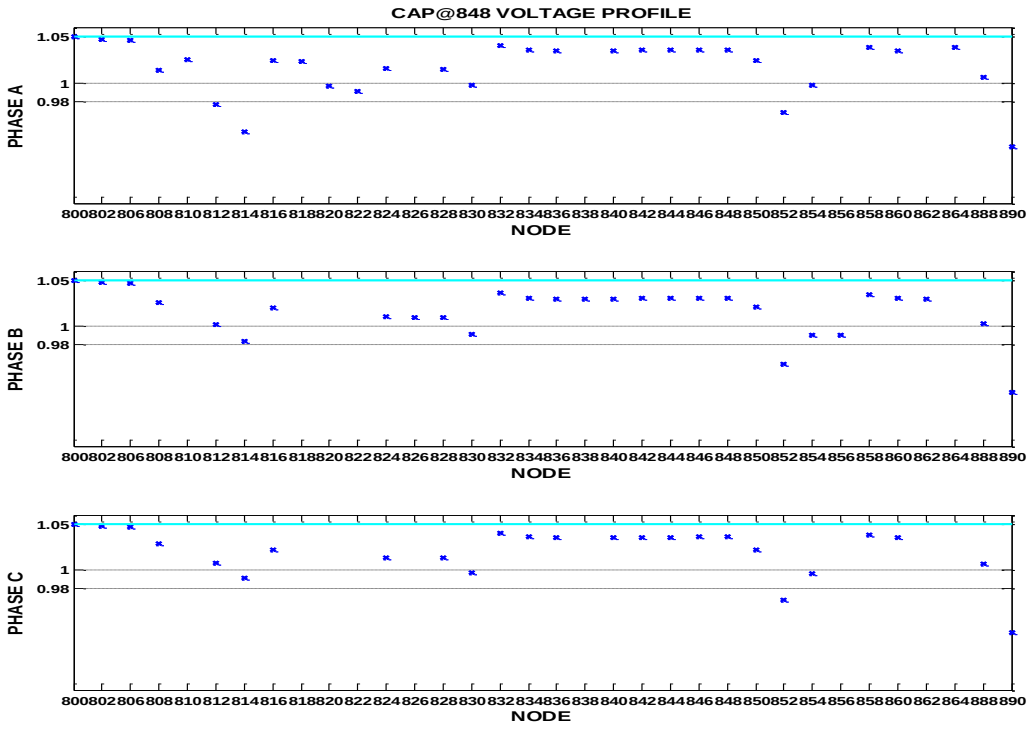


Figure 7.12: Voltage Profile for the Base Feeder with Shunt Capacitor at 848 in Peak Load Condition

DVC at node 848

In this case, the shunt capacitor is replaced by DVC at 848. This test is done just to verify the functionality of DVC in a big system. The internal DC bus voltage and command following Iq waveform confirmed a stable system.

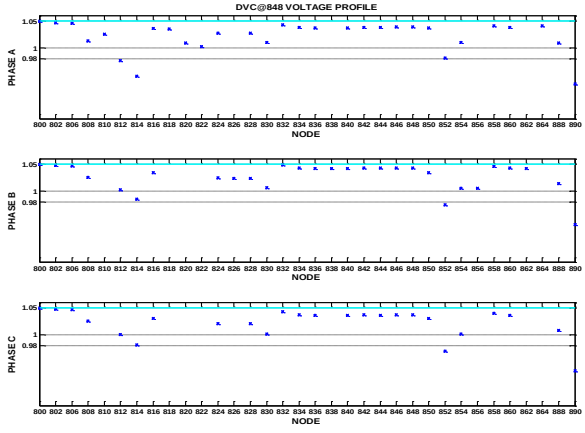


Figure 7.13: Voltage Profile for the Base Feeder DVC at 848 in Peak Load Condition

Fig. 7.13 shows the TAP number as a function of time. The DVC is switched on at TIME=5s. It shifts the equilibrium to a lower value (12). Fig. 7.14 shows the voltage profile of the feeder in this system.

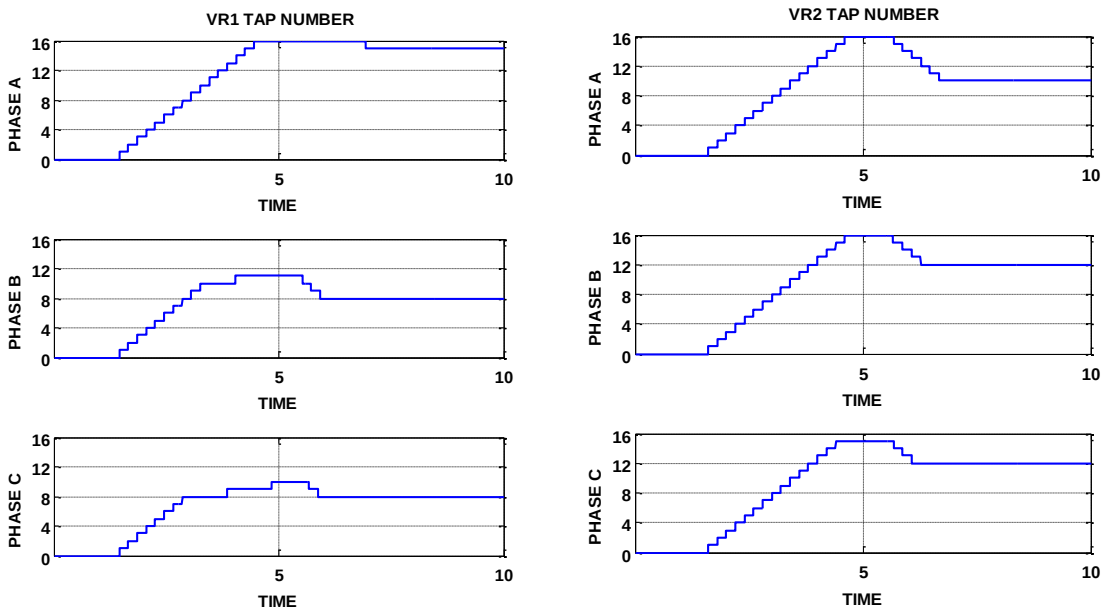


Figure 7.14: (a) Voltage Regulator 2 Tap change Profile, (b) Voltage Regulator 1 Tap change Profile

Comparison

As we can see in Fig. 7.15, both DVC and shunt Capacitor were successful in pushing the voltage to some extent.

This study was done just to verify the functionality of DVC in this system. As noted before, Node 890 has the worst case of voltage violation. DVC placed at 890 has also been studied and presented in the next section. Also, the fact that DVC can provide varied amount of reactive charge at any given time, has been exploited in a time-varying load system. At first the Base Feeder has been simulated and then the DVC has been incorporated and the comparisons have been reported. Fig. 7.16 shows the comparison of Tap Change.

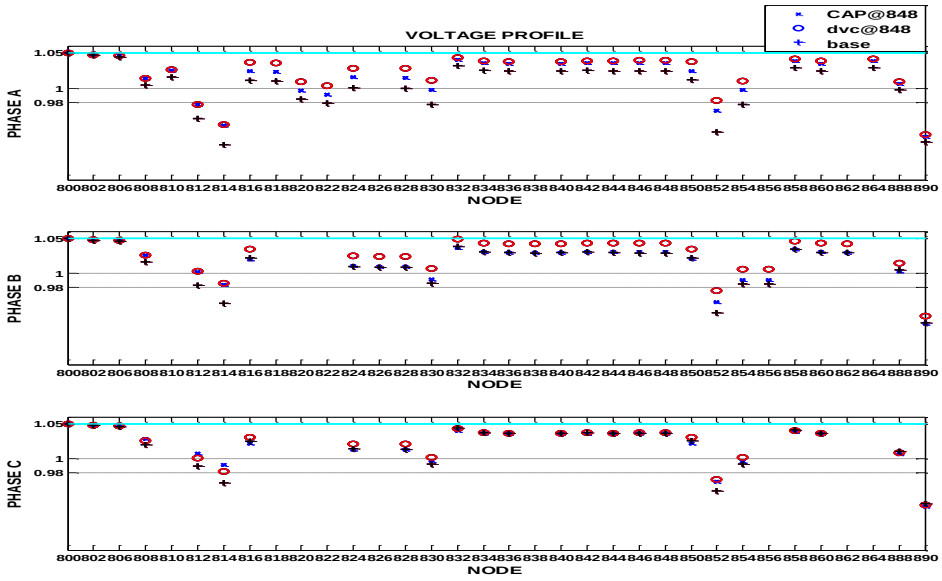


Figure 7.15: Voltage Profile Comparison in Peak Load Condition

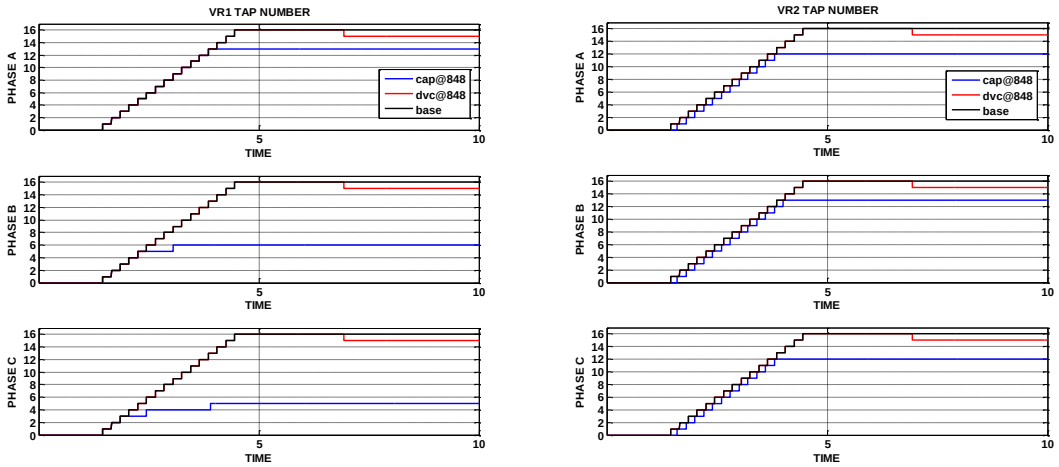


Figure 7.16: TAP Change Profile Comparison in Peak Load Condition of Voltage Regulator 1 (left) and 2 (right)

7.5.2 Time-variant Load with DVC at node 890 and VRs

At, 12:30 the Load requirement is considered low and most of the Nodes are out of violation zone. Here, both the Base Feeder and DVC based system have similar profile (Fig. 7.17). Fig. 7.18 shows the Voltage Profile of the system with and without DVC at 10:30 AM, which is set as a high Load condition. It can be seen that Node 890 is no more in the violation zone

when the system has DVC connected at 890. This gives us a good idea of the functionality of DVC and a way to formulate closing the loop of the controller to get 1p.u. voltage at desired nodes.

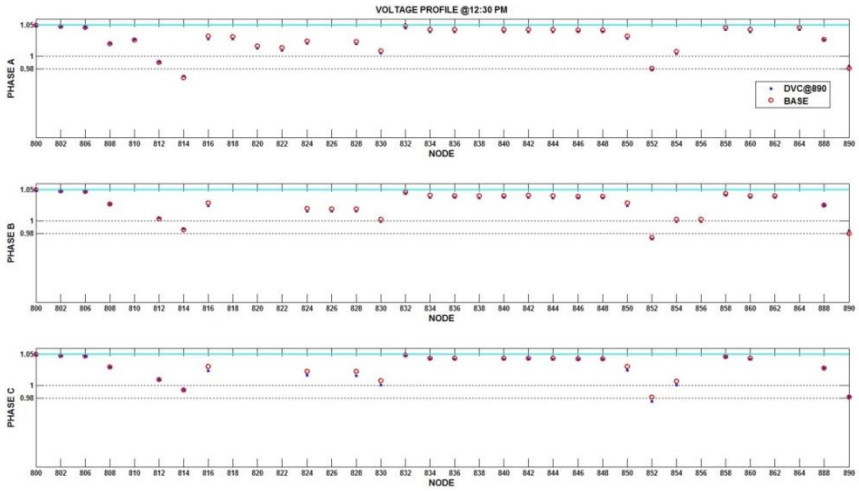


Figure 7.17: Voltage Profile Comparison at 12:30 PM (Low Load)

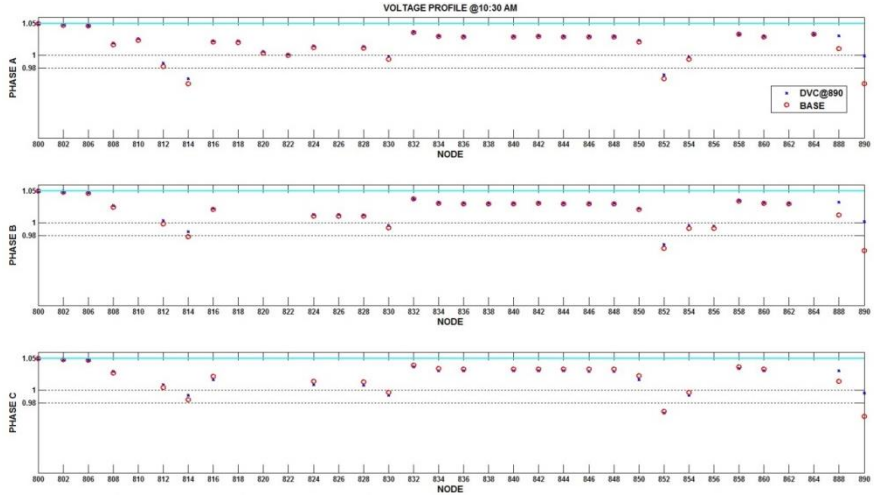


Figure 7.18: Voltage Profile Comparison at 10:30 AM (High Load)

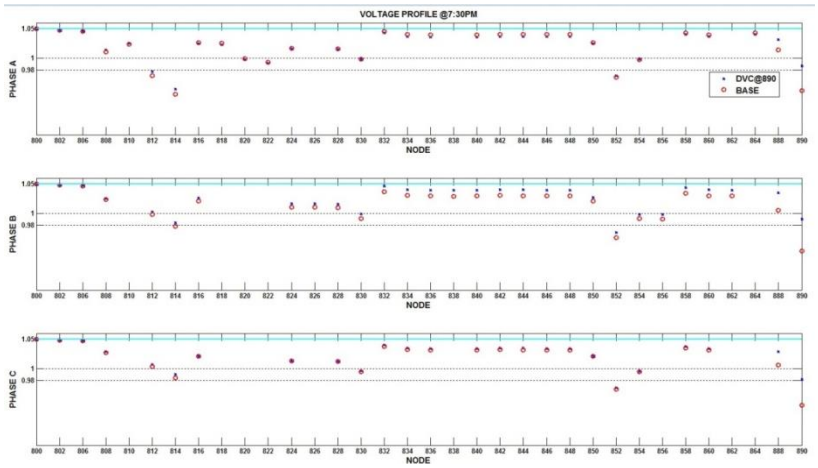


Figure 7.19: Voltage Profile Comparison at 7:30 PM (Peak Load)

Fig. 7.19 shows the Voltage Profile of the system with and without DVC at 7:30 PM, which is set as the peak Load condition. It can be seen that Node 890 is not in the violation zone when the system has DVC connected at 890. There are two ways to control DVC. One is use step change Iq_ref input, and the other one is closed- loop control. Fig. 7.20 shows the voltage waveform at 890 the feeder with and without DVC. The step input command given to DVC were discrete and chosen such that voltage violation be avoided at high load condition. Thus, Iq_ref was set to a low value when the system is under low load and higher value when it is under high load. This has been further extended by closing the loop with grid voltage as a feedback.

Fig. 7.21 shows a successful implementation of closed loop control to fix the Node voltage at 1p.u. At some time, the maximum reactive power providing capability was not enough to bring the node to 1p.u. but for most of the time, the algorithm worked. If the main task of the DVC is to regulate the node voltage, it can be argued that a simple voltage feedback would also serve the purpose thus eliminating the cost of system administration and power flow calculation.

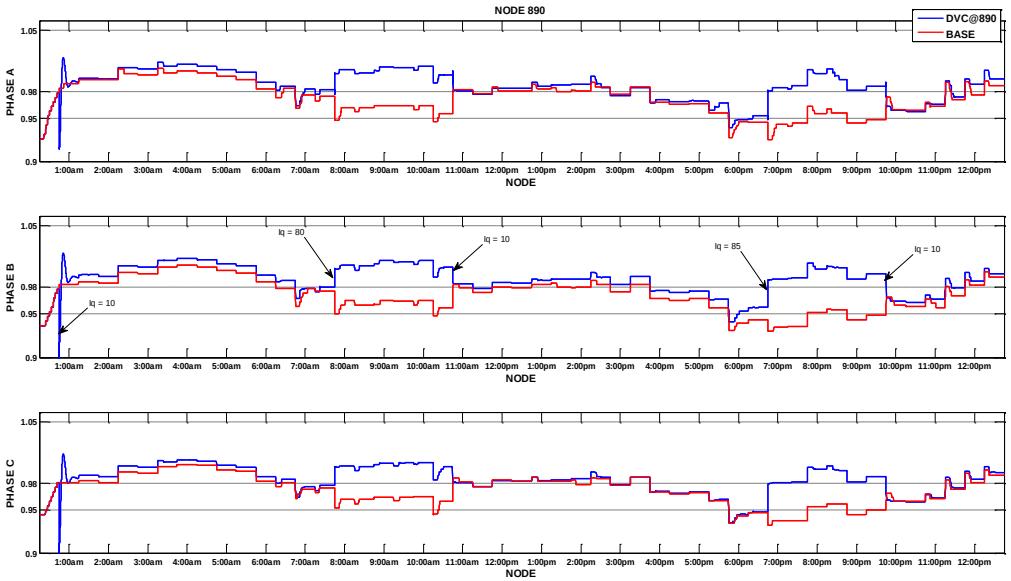


Figure 7.20: Voltage waveform at 890 throughout the day with step change input DVC

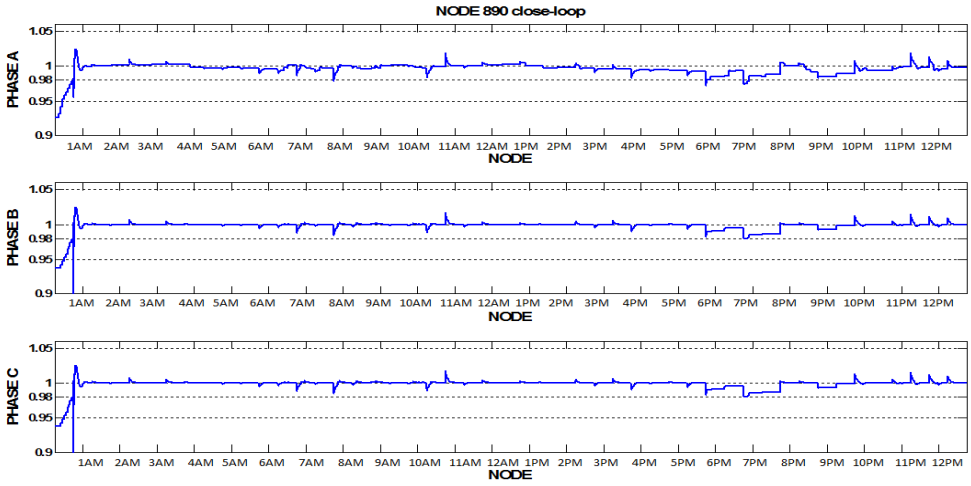


Figure 7.21: Voltage waveform at 890 with closed loop DVC

7.5.3 No VRs

Base case

The base feeder in this study has no VRs, capacitor banks or DVCs. The simulation is run under peak load condition. As we can see in Fig. 7.22, most nodes have voltage violation. Node 890 suffers a serious voltage problem. Thus we need to mitigate these problems by adding DVC into the system.

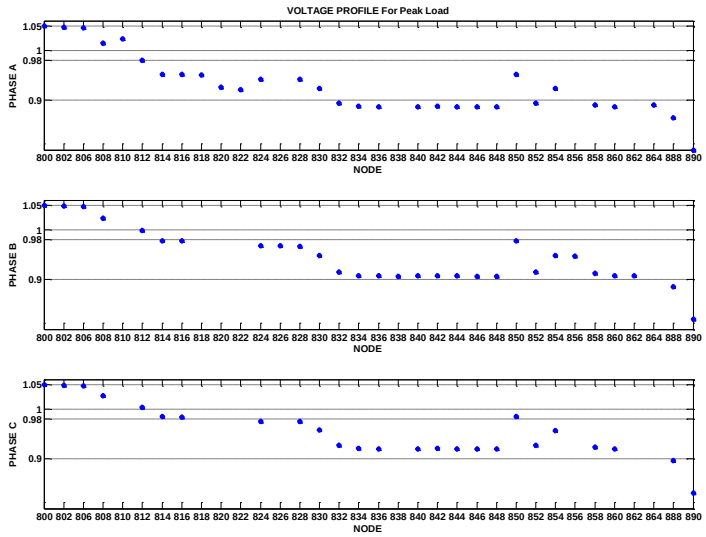


Figure 7.22: Voltage Profile for the Base Feeder at Peak Load Condition without VRs

DVC at node 832, 850, 890

In this study, we are trying compare a system with 2 Voltage regulators (at 850 and 832) and 1 DVC (at 890) with a system with three DVCs (at 850, 832 and 890). With a line drop compensator integrated in the VRs, it regulates two remote nodes (node 850 and node 832). In this study, we are trying to verify whether we could use DVC to realize the functionality of VRs. So we use two closed-loop DVCs to regulate these two nodes at certain voltages which are the same as voltage regulator's reference voltages. As we can see in Fig. 7.23, DVCs at node 832 and 850 boost the voltage to a high value which allows the voltage drop along the feeder behind the node. The significant voltages improve are shown in Fig. 7.24. Node 890 which is a big concern in the previous study also has no voltage violation.

Fig. 7.25 shows a comparison voltage waveform with VRs and DVC at node 850. DVC is working to regulate phase B at the same voltage as reference voltage in VR. This figure could clearly show us DVC could completely replace VR in the system.

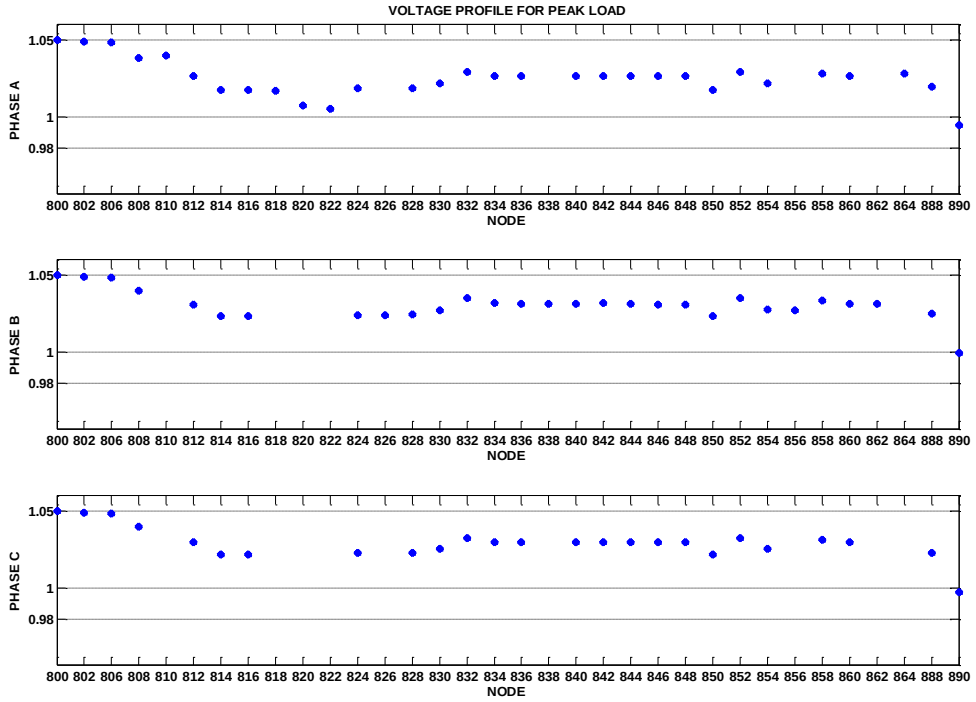


Figure 7.23: Voltage Profile for 3 DVC under Peak Load Condition

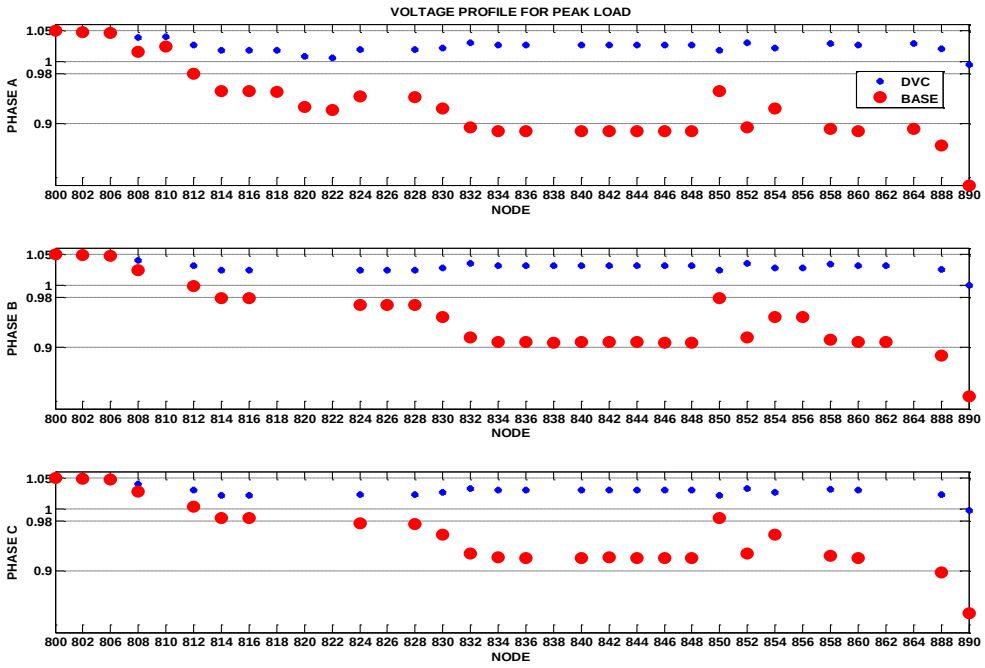


Figure 7.24: Voltage Profile Comparison for 3 DVC under Peak Load Condition

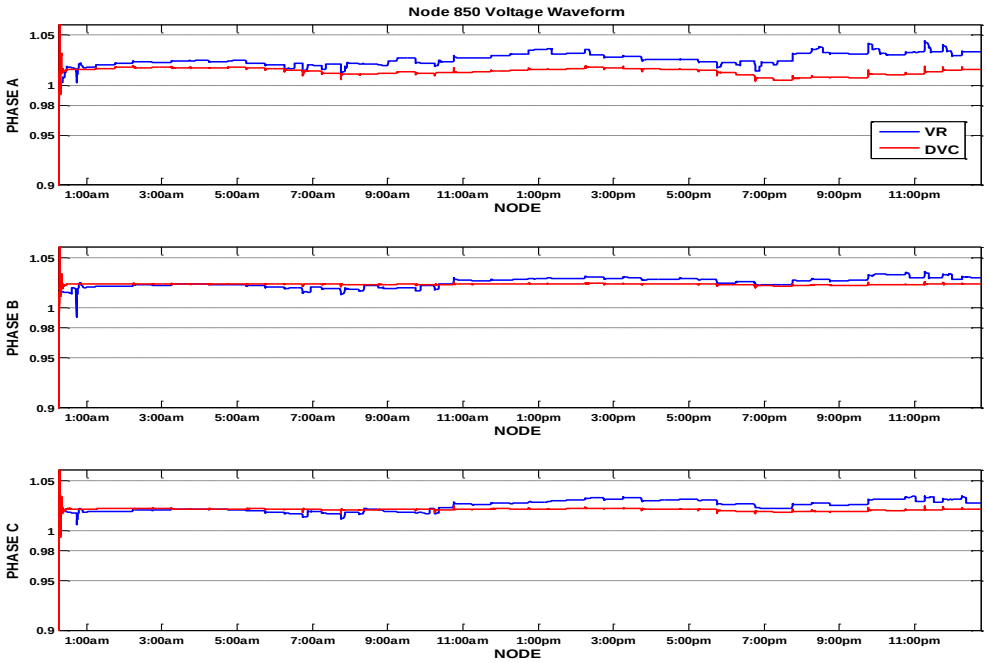


Figure 7.25: Voltage Waveform comparison at node 850

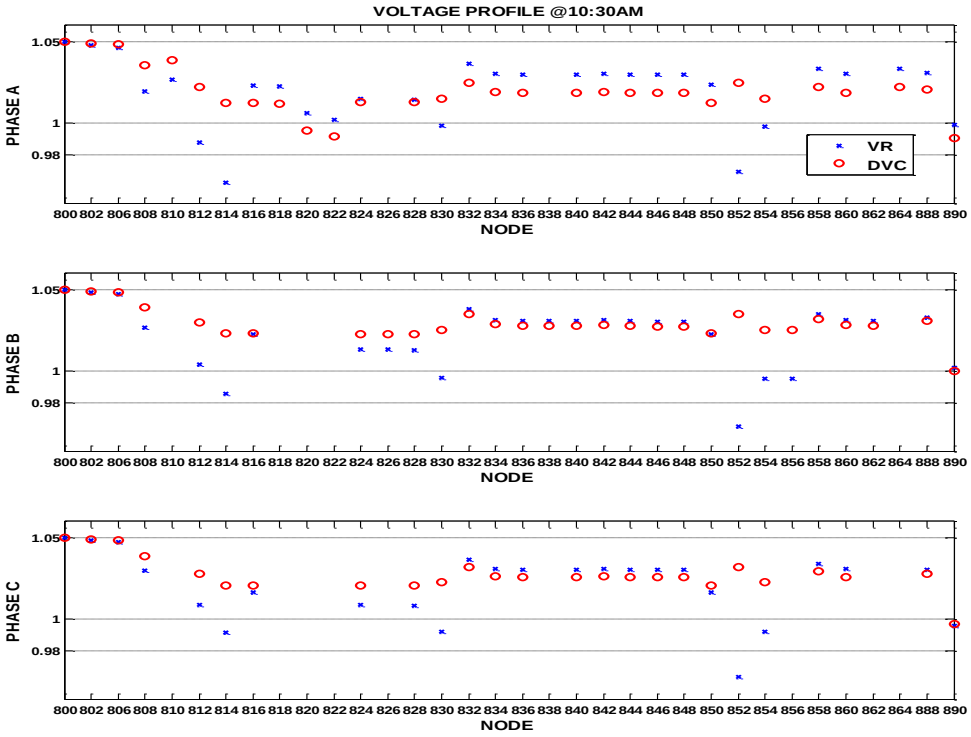


Figure 7.26: Voltage Profile Comparison at 10:30 AM (High Load)

Fig. 7.26 shows the voltage profile comparison of with DVC and with VR. The voltage of phase B at node 850 and 832 are exactly the same in both cases, which prove that DVCs could replace VRs. We can also see that DVCs help improve the voltage at node 814,812, 852, 854 which have voltage violation when VRs are used in the system.

5 DVC

The objective of this study is to make the voltage profile flat. Five DVCs were installed in the system to realize this goal. And the source voltage is also set to 1.0 pu. From the previous study, we found that the lowest voltage among three phases is phase A, so in this study phase A is regulated. Another reason to regulator phase A is that there is a lateral in phase A (Node 816, 818, 820, 822) which has a large load connected to it. If we regulate other phases, like phase B, voltage at node 822 will have voltage violation.

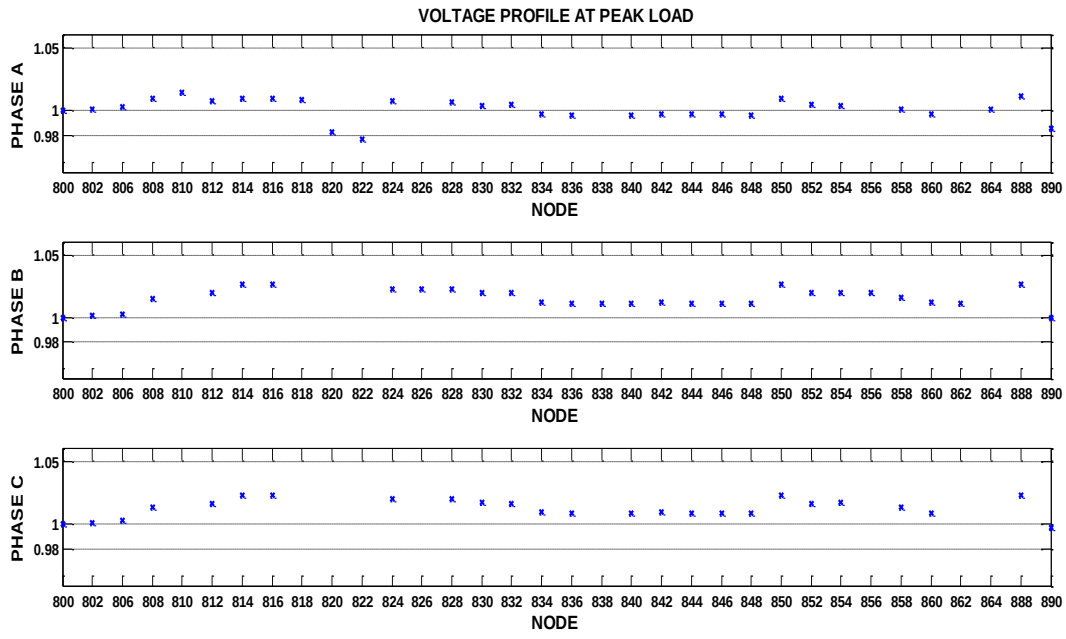


Figure 7.26: Voltage Profile under Peak Load

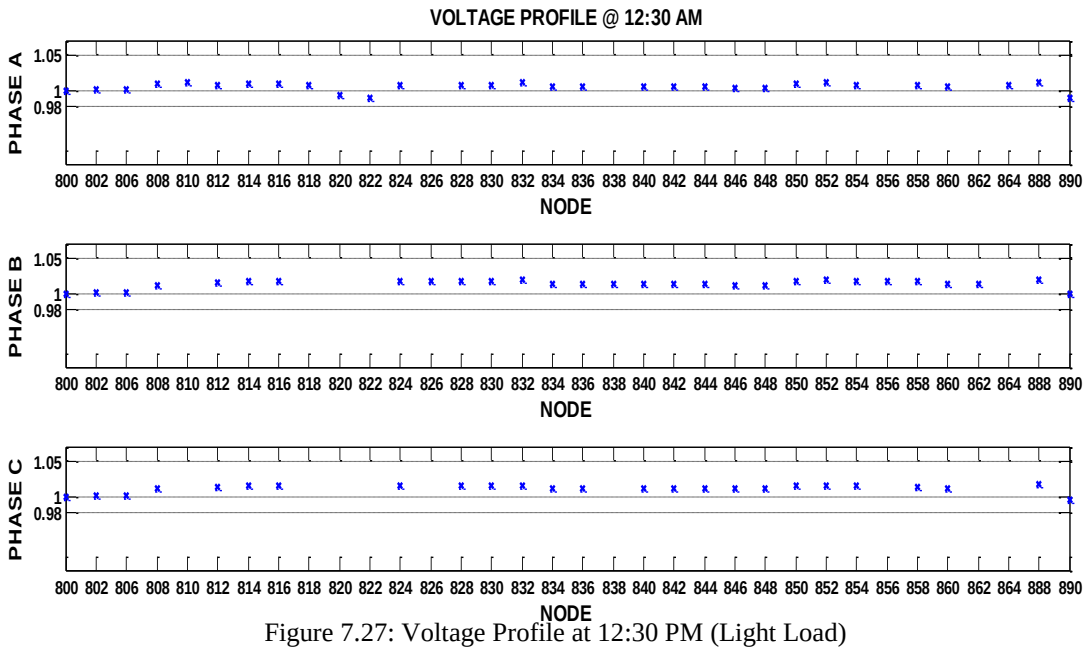


Figure 7.27: Voltage Profile at 12:30 PM (Light Load)

As Fig. 7.27 shows, the voltage at node 822 has a very low voltage compare to other node. There is a heavy load connected at node 822. However we do not have single phase DVC, what we could do is boosting the voltage at node 808 to 1.01 pu instead of 1.00 pu. Similar thing happens at node 890. If we keep node 850 at 1.0 pu, the voltage at node 890 can hardly reach 0.98 pu. Therefore, we boost the voltage at node 850 to 1.02 pu. Although this is peak load which is the worst situation during a day, the voltage profile in Fig. 21 still looks well. The voltage profiles at 12:30 PM (Fig. 7.27), another high load and at 10:30 PM (Fig. 7.28), a light load, look better than peak load.

For further analysis, the voltage waveform at 850, 832 (nodes where DVCs replaces VR) and 890 were recorded. Fig. 7.30 and 7.31 show the voltage waveform at 832 and 850 respectively. Phase B is regulated for 832 and Phase A is regulated for 850.

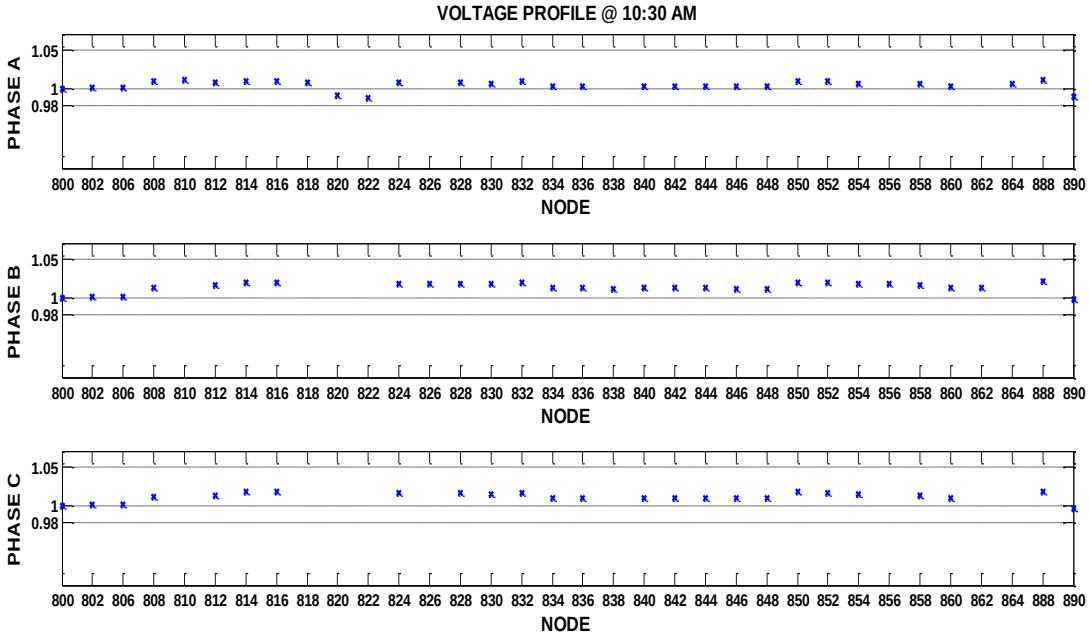


Figure 7.28: Voltage Profile at 10:30 (High Load)

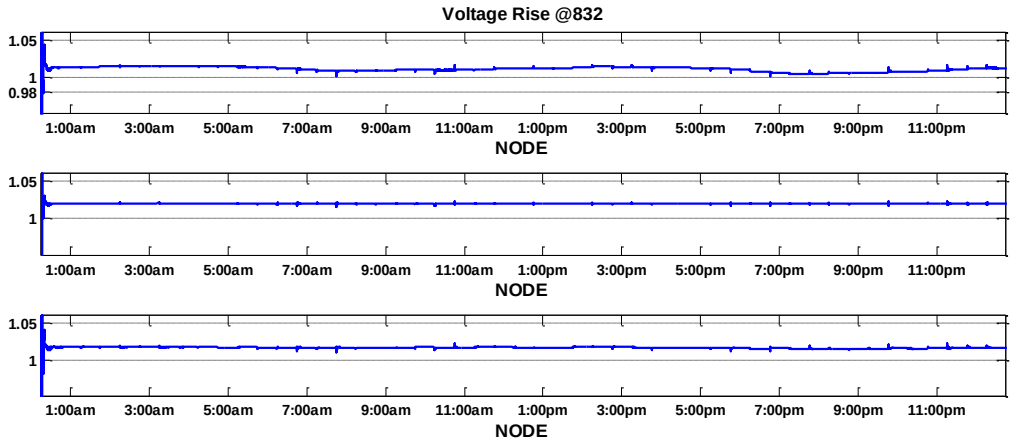


Figure 7.29: Voltage Waveform at 832

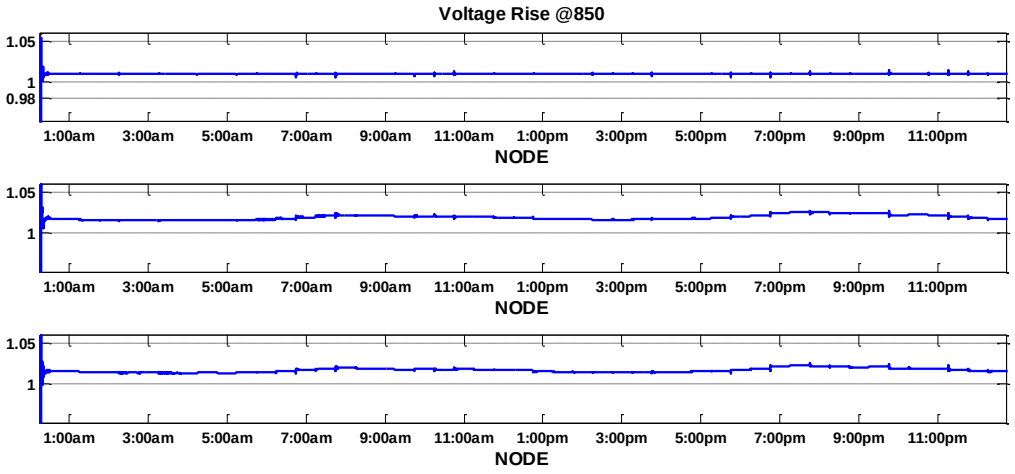


Figure 7.30: Voltage Waveform at 850

The figures confirm the functionality of DVCs is voltage regulators. The voltage waveform of the corresponding regulated phases was flat and did not respond to time varying load. Fig. 7.32 shows the voltage waveform of 890. In this case, phase B is regulated.

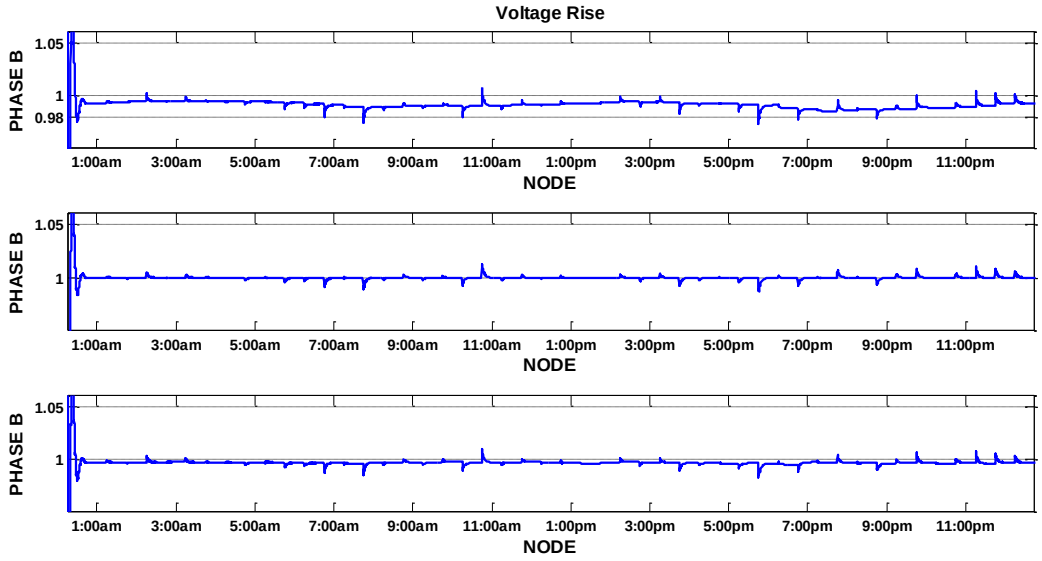


Figure 7.31: Voltage Waveform at 890

7.6 PV Impact on a Distribution System

In this study the distribution system considered is a residential distribution feeder with high penetration of PV – a feeder on which most of residential customers have rooftop PV systems. The main issues investigated in this section associated with such high penetration of PVs (PV capacity is up to 70% of peak load) include the following:

- Reverse power flow: High penetration of PVs on a feeder can offset the feeder load and can even cause reverse power flow from feeder to the substation. Reverse power flow can negatively affect operation of line voltage regulators, particularly the ones with the Line Drop Compensation (LDC), and cause overvoltage [95].
- Voltage Fluctuations: On a cloudy day PV power output can fluctuate quite a lot and such fast variations cause large and frequent voltage variations. Such fluctuations will also increase the VR operations.
- Voltage and current unbalance: If PVs on a feeder are connected mainly to one phase only, this can cause considerable unbalance on both current and voltage on the feeder. However, if the PVs installed properly, they can reduce the voltage and current unbalance, as they will reduce the loading on the system.
- Power Loss: For low and moderate penetration levels of PV, currents along the feeder will decrease, so power system line losses will decrease. For high penetration levels of PV, which causes reverse power on the feeder, during light load conditions for example, feeder line losses may increase. It is important to note that this can happen within a single day. At noon, the load is light and PV output is high, so the losses may increase; while during the late afternoon, the PV output offsets the load only partially, and thus decreases the power losses.

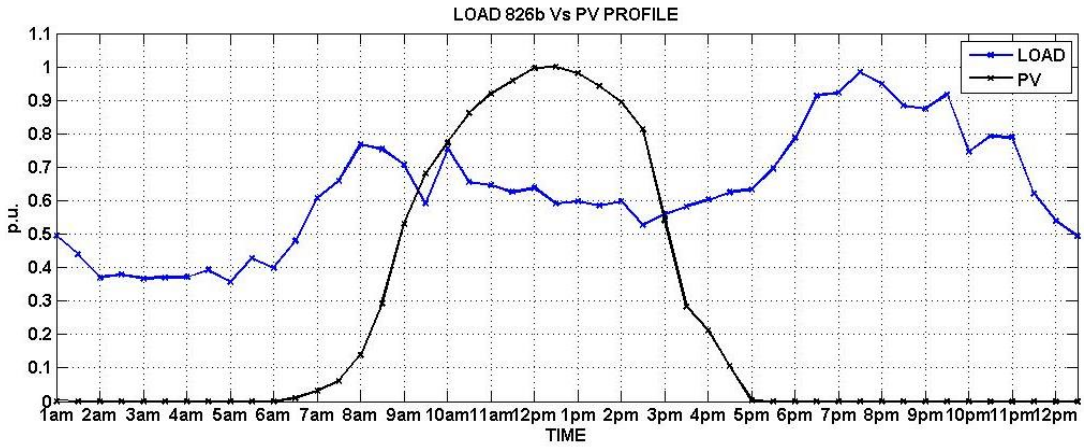


Figure 7.33: Normalized PV and Load profiles

Case 1: Normal Operation

The system is simulated with PV and load profile of Fig. 7.33. Fig. 7.34 compares the voltage profiles at node 890 with and without PV systems. As the figure shows, the voltage at this node is near low limit most of the time without PV, and PVs help boost the voltage at this node when PV output is high, around 10 am – 3 pm. However, during this time the power from PVs cause reverse power flow on the feeder, as PV output is higher than the load, and therefore, it causes the two VRs on the feeder act improperly as will be shown below. As a result, the voltages towards the substation will reach upper limits, as shown in Fig. 7.35. However, PVs do not necessarily raise the voltage at all the nodes, mainly due to VRs response.

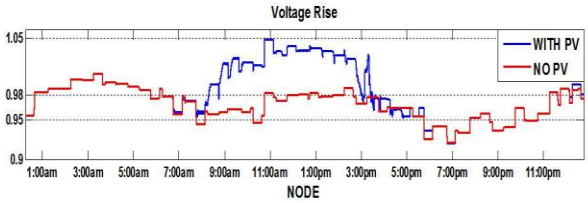


Figure 7.34: Voltage profile at node 890: with or without PV – Case 1

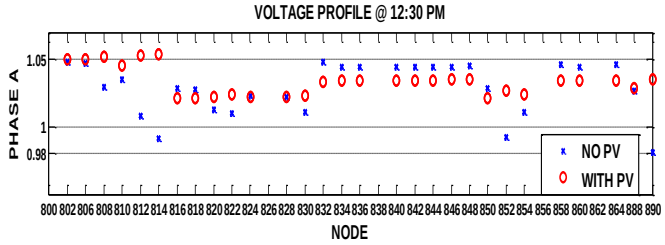


Figure 7.35: Feeder voltage profile at 12:30 pm: with or without PV – Case 1

Case 2: Cloud Cover

PVs are quite susceptible to cloud cover, and PV output can decrease quite fast as a cloud moves over. In this case, a cloud moving over the PVs is simulated by a decrease in solar irradiation from 1000 to 70 W/m2 over a 20 sec, causing PV power output decline in a similar way as shown in Fig. 7.36.

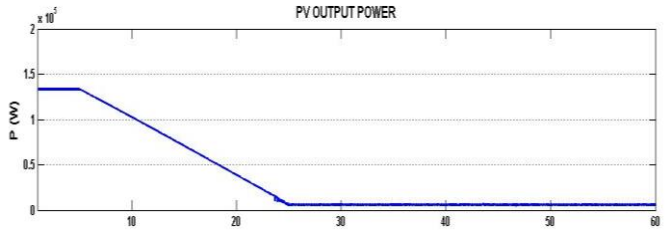


Figure 7.36: PV power changes with sun irradiation – Case 2

Fig. 7.37 shows the voltage variation at node 890, which is the node most severely affected by cloud coverage. As the figure shows, the voltage at the node drops down to 0.89 pu following cloud cover and remains at this low level for about 15 sec until VRs start boosting the voltage.

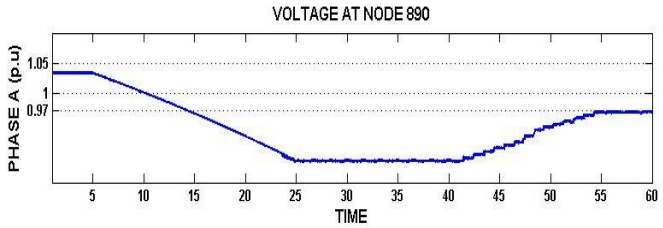


Figure 7.37: Voltage at node 890 following a cloud cover- Case 2

The voltage remaining below low limit of 0.95 pu at a node may affect the loads, especially the dynamic loads such as induction motors. To illustrate this, the loads at 4 nodes, where PVs are connected to, have been simulated as 50% resistive loads and 50% small induction motor loads. Fig. 7.38 shows the operation of motors under the cloud cover condition. We can clearly see that motor at node 890 begins to stall at 12s and motor at node 844 begins to stall at around 20s.

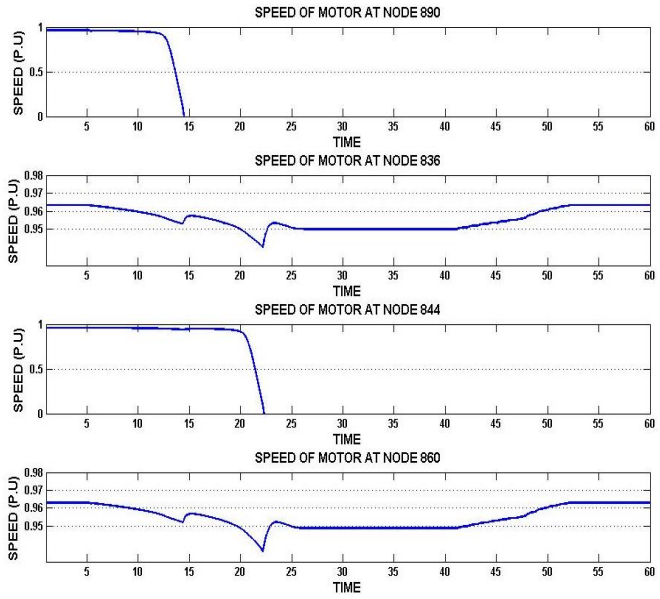


Figure 7.38: Speed of Motors in the system – Case 2

Case 3: DVC at node 890

In this case, we installed a DVC at node 890 to address unacceptably high voltage variation as shown in previous section. We also removed the capacitors at node 844 and node 848 to see whether DVC will still maintain the voltages.

Fig. 7.39 shows the voltage profile at node 890. Voltage remains around 1 pu and no voltage violation occurs throughout the day. This illustrates that the DVC can address the voltage variation at node 890 very effectively. Fig. 7.40 shows the feeder voltage profile during peak load at 7:30 pm, during which there is no PV output. The voltage profile shows that only the node 814 has low voltage violation, and this node has no load, thus this is not a big concern. Hence, this case illustrates the effectiveness of a DVC in improving voltage control locally at a remote end of feeder.

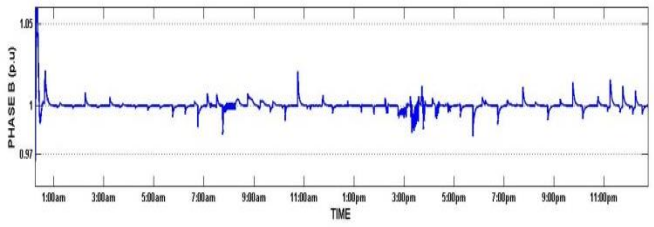


Figure 7.39: Voltage Profile at node 890 with one DVC – Case 3

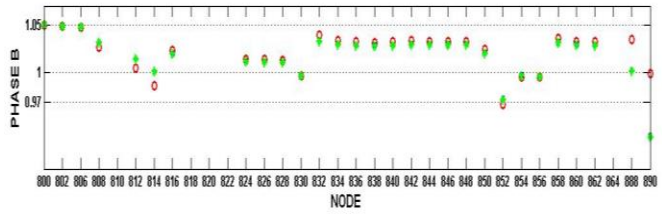


Figure 7.40: Feeder Voltage Profile under Peak Load Condition – Case 3

Case 4: Three DVCs

To improve voltage control more, in this case we considered replacing two VRs on the feeder with two DVCs. Fig. 7.41 compares the feeder profile with DVCs against the voltage profile with VRs. As the figure shows with DVCs there is no voltage rise towards the substation and during high PV output and the voltage profile is all within the acceptable limits.

To illustrate the response of the DVCs during cloud cover, the same cloud cover simulation has been repeated with DVCs also. Fig. 7.42 shows the voltage variation at node 890 following the cloud cover. As we can see, the voltages are almost kept the same for the entire 60s. Fig. 7.43 compares the voltage profile along the feeder. As we can see, the voltages did not change much during the cloud coverage. These results show that indeed the DVCs act quite fast to fast drop in PV power output and provide fast VAR support to keep the voltages smooth even during such high power fluctuations on the feeder.

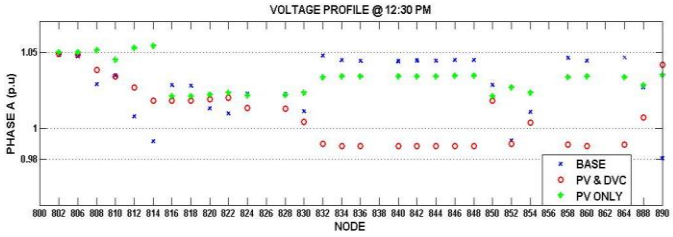


Figure 7.41: Voltage Profile Comparisons at 12:30 PM (Peak PV) - Case 4

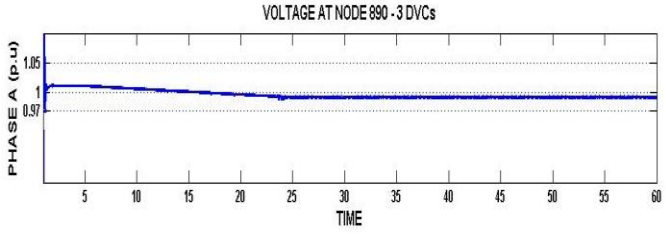


Figure 7.42: Voltage Profile at node 890 with three DVCs – Case 4

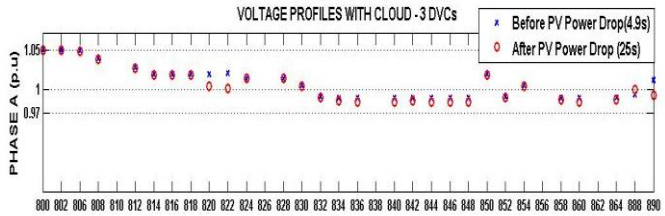


Figure 7.43: Voltage Profiles under cloud condition – Case 4

Finally, the case with the dynamic loads has been repeated here with DVCs. Fig. 7.44 shows the operation of motors in this case. As the figure shows, since there is hardly any voltage variation following the cloud cover, the motors do not see any effect of cloud cover.

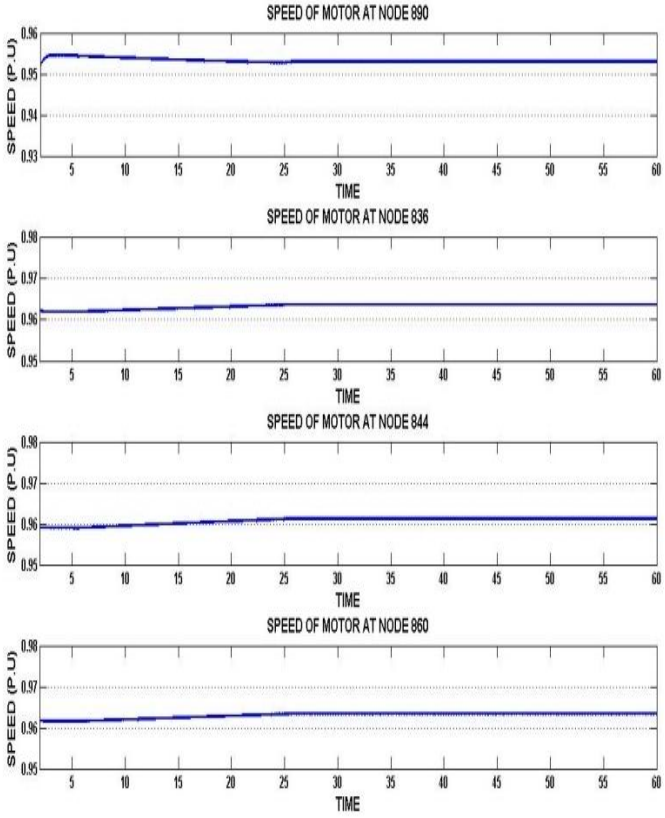


Figure 7.44: Speed of Motors in the system – Case 4

7.7 Conclusions

The work done illustrates a new kind of Dynamic VAR Compensator. Detailed principle of operation and intiail hardware results of the same has been presented. The simulations performed on the IEEE test feeder confirms that high level of PV penetration on a radial feeder can cause considerable voltage variation and affect the operation of Volt-VAR devices on such a feeder, especially if the total power from PVs causes reverse power flow. The main issue in such systems is the power fluctuation from PVs during a cloudy day, as the voltage regulators cannot act fast enough to smooth out the resulting voltage variations. Simulations show that motor type loads will be susceptible to voltage sags during such conditions. The chapter shows that the use of dynamic VAR compensators (DVCs) can address these issues quite effectively, as they can respond fast to voltage variations and provide fast VAR compensation to smooth the fast variations. The chapter shows that DVCs can be either used to replace capacitors to provide voltage boost locally as needed, or they can be used to replace even the voltage regulators to provide a more effective voltage control along the whole feeder. Further studies are needed to determine proper selection and placement of DVCs on a feeder.

CHAPTER 8

DETERMINATION OF ELECTRIC FIELD STRESS DISTRIBUTION IN SOLID STATE TRANSFORMERS AND EVALUATION OF TEST METHODS

8.1 Introduction to Solid State Transformers

The positive attributes of conventional distribution transformers, include low cost, high reliability, and high efficiency. However, these conventional copper-and-iron based transformers possess many undesirable drawbacks. These drawbacks include large size and weight, voltage drop under load, power quality susceptibility, sensitivity to harmonics, environmental concerns when leaks of mineral oil occur, and no DC output or energy-storage capacity. Due to their bulky iron cores and heavy copper windings, conventional transformers are by far one of the heaviest components in an electrical distribution system. The size and weight of the transformer is primarily a function of the saturation flux density of the core material and maximum allowable core and winding temperature rise [96]. The saturation flux density is inversely proportional to frequency, and hence increasing the frequency allows higher utilization of the magnetic core and reduction in transformer size. However, because the operating frequency of commercial power is ordinarily fixed (60 Hz in the U.S. and 50Hz in Europe), the volume and the weight of the distribution transformer cannot be reduced below its definite values

Moreover, with the increased cost in basic materials such as copper and laminated steel, the Solid State Transformer (SST), which uses much less copper, is potentially attractive. This is even more important to the higher power SST because today's 2.7 MVA transformer weighs more than six tons and uses a large amount of copper and steel.

The Solid State Transformer (SST) is a revolutionary power electronics device which will bring a quantum leap in iron-and-copper distribution transformer technology and better facilitate the future smart grid infrastructure. The SST is one of the key elements in the Future Renewable Electric Energy Delivery and Management (FREEDM) Systems [97]. It can act like an energy router to enable active management of DRER, DESD and loads. The SST has the features of instantaneous voltage regulation, voltage sag compensation, fault isolation, power factor correction, harmonic isolation/reduction and DC output production/regulation [98]-[100]. The SST converts the voltage from AC to AC for step-up or step-down with the function same as the conventional transformer. However, the traditional 60 Hz transformer is replaced by a high frequency transformer to provide isolation and step up/down function. This is the key to achieve size and weight reduction and power quality improvement.

8.2 Modular Cascaded SST

The most commonly used power electronic converter topology is the two-level converter. However, even using the highest available power rating 6.5kV IGBTs, a two-level converter (without series connection of switches) based SST can only interface with 2.4kV AC voltage. In order to apply the silicon based SST to a distribution voltage level 7.2kV-12kV, multi-level converter topology is inevitable [101]-[105]. The cascaded H-Bridge multi-level converter based SST system is shown in Fig. 8.1. By using commercially available low voltage low current devices and components, a standardized, integrated and modularized solid state transformer can be designed. The SST under investigation can transfer required power from 10kV, 60Hz MV Grid to 400V, 60Hz LV grid. The high voltage DC bus of each modular converter can be designed as 1.1kV whereas the low voltage DC bus can be set to

800V. Meanwhile, to share the high output current, all the converter cells are paralleled at the output. The advantages of modular SST is that only low voltage H-Bridges are needed for the entire SST, and the system is easy to upgrade by adding on new modular SST cells.

The topology of this solid state transformer consists of a cascaded multilevel AC/DC rectifier, Series Resonant Converter for DC/DC conversion and isolation with high frequency transformers and a DC/AC inverter.

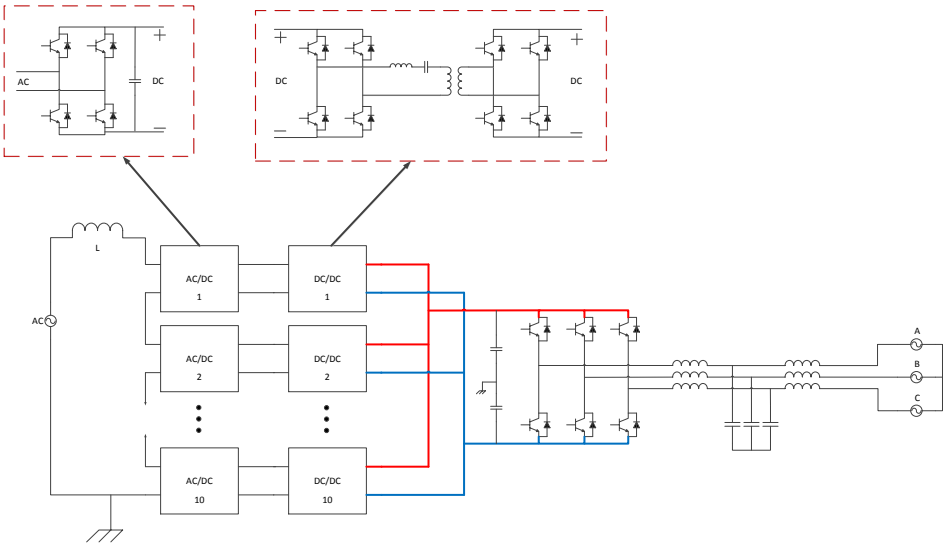


Figure 8.1: Circuit Schematic of the understudied SST

The above mentioned SST can form as the interface device between the distribution system and the electricity consumers in future smart grid systems. It can act like an energy router, with bi-directional energy flow control capability allowing it to control active and reactive power flow and to manage the fault currents on both the low voltage and high voltage sides. Its large control bandwidth provides the plug-and-play feature for distributed resources to rapidly identify and respond to changes in the system. With incorporation of the solid-state technology into the distribution transformer, many new features can be realized through power electronics control and dc bus energy storage [106]-[107].

8.3 Critical Voltage Stress

This chapter deals with the various control algorithms that can be incorporated for transferring power from one grid to another. The various understudied control algorithms are:-

(1) Phase-shifted Multi-level Converter Algorithm with linearly varied carrier wave delay;

(2) Phase -shifted Multi-level Converter Algorithm with alternating carrier wave delay;

(3) Phase -shifted Multi-level Converter Algorithm with alternating carrier wave delay in reverse order;

(4) Optimized module control algorithm; and

(5) Chaotically jittered phase-shifted Multi-level Converter Algorithm.

Various critical stresses have also been presented. These stresses include:-

(1) Inter Module Voltage Stress;

(2) Voltage Stress on Transformer winding with respect to ground;

(3) Voltage difference across middle point of Transformer;

(4) Voltage difference across the top point of Transformer;

(5) Voltage difference across diagonal points of Transformer; and

(6) Voltage of the Collector of the chip with respect to ground.

FFT of voltage difference across the middle point of the transformer of various control algorithm have been compared.

8.4 Phase-shifted Multi-level Converter

As the solid-state switches in an H-bridge module can either be switched laterally to render zero voltage or diagonally to provide $\pm V_{dc}$, the solid-state devices of the same phase of all the converter modules do not have to switch in unison. This freedom allows the phase-shifted triangle carrier technique of the sinusoidal pulsewidth modulation (SPWM) strategy [108]-[109] to be applied in the control of the multiconverter modules. In this technique, the SPWM switching of the same phase of the modules are not simultaneous. Instead, the phase shifted triangle carriers introduce a slight staggering of the switching instants in the individual converters, and this creates the multilevel output voltage waveform. All the excellent properties of the SPWM strategy are found in the array of multiconverter modules, when they operate under the phase-shifted triangle carrier technique [110].

8.4.1 Simulation Results

The Phase-shifted multiconverter system has been simulated in SIMULINK. In this case, the sawtooth carrier fed to module 1 is the most leading wave. The consequent modules are linearly delayed. Thus, the sawtooth waveform fed to module 2 lags the same of module 1 by 1/10th of time period in case of 10 cascaded converter cells. Fig. 8.2 shows the input voltage, input current and staggered rectified output of the system.

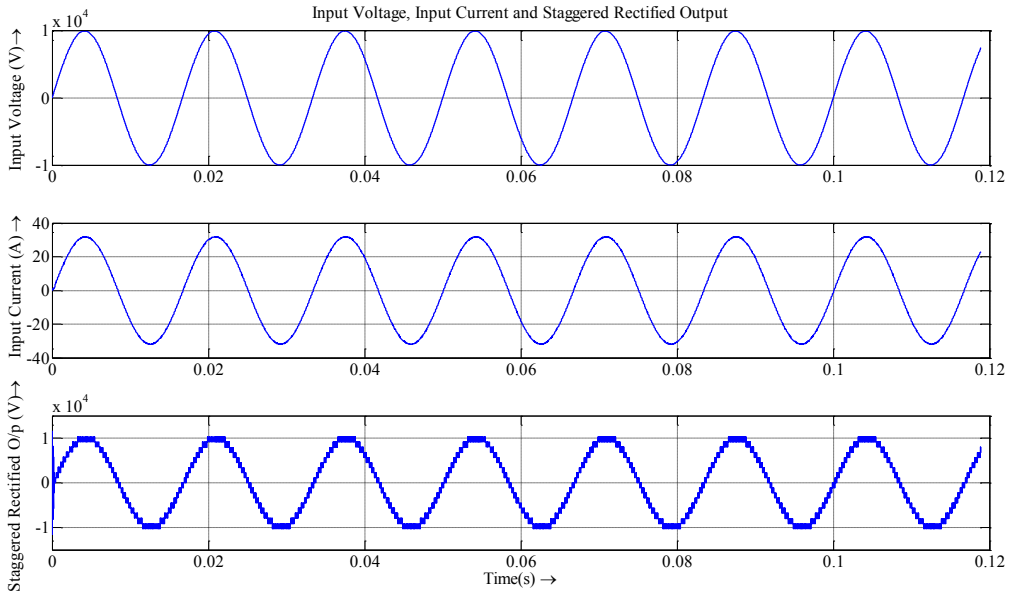


Figure 8.2: Input Voltage, Input Current and Staggered Rectified Output of the system

Tab. 1 shows the voltage rating at various ports of the topology.

Table 1: System Voltage Specifications

Port	Voltage Level	Frequency of Operation
Cascaded Rectifier Output DC Voltage	1.1kV	3kHz (effective : 30kHz)
DC/DC Converter Output Volage	800V	5.5kHz
LV grid	400V, 60Hz (L-L, RMS)	(Inverter) 10kHz
MV grid	10kV, 60Hz (peak)	-

This phase shifted control scheme effectively increases the equivalent switching frequency by ten times (as there are 10 modules) and in addition generates a multilevel output voltage waveform, both of which helps in reduction of the size of passive components. This however has shown a dominant effect in the power spectrum which might lead to dielectric heating. Using this as a base case, a number of stress test monitoring has been done to study the critical voltage stresses in the system. The next few sections will deal with the various stresses witnessed in the system.

8.4.2 Inter Module Voltage Stress

Fig. 8.3 shows two terminals across which voltage is measured. It depicts the inter-module voltage. It was found that the inter module voltage is invariant of the location of modules. Thus, the inter module voltage between module 1 and 2 is same as that between 9 and 10.

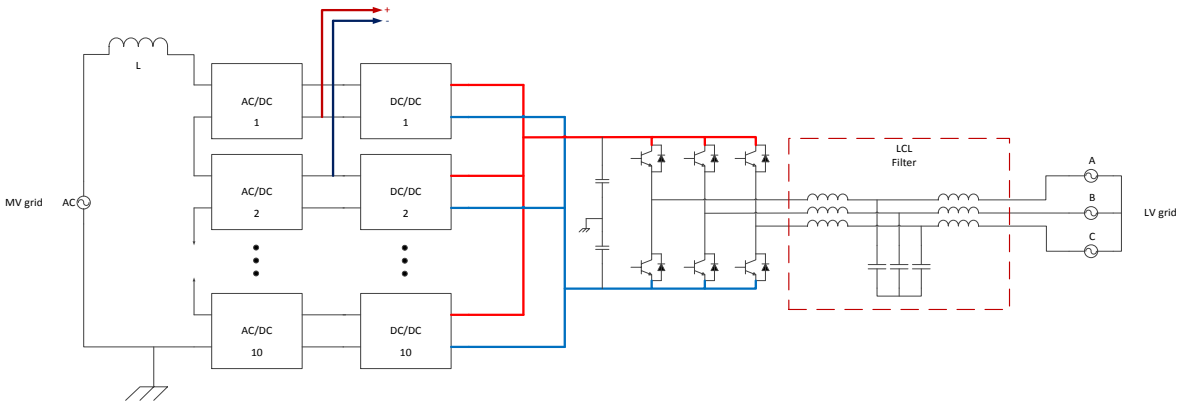


Figure 8.3: Inter Module Voltage Stress Study

Fig. 8.4 shows the voltage measured across the two terminals. As seen, the polarity of the voltage does not change with time. The high frequency switching occurs at 3kHz and low frequency voltage step occurs at 60Hz.

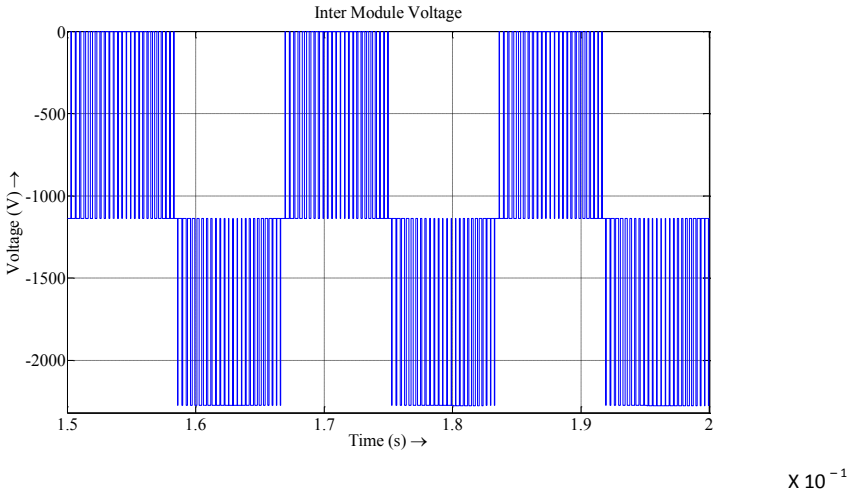


Figure 8.4: Inter Module Voltage Stress

8.4.3 Voltage Stress on Transformer winding with respect to ground

Fig. 8.5 shows two terminals across which voltage is measured. It depicts the transformer terminal voltage with respect to ground.

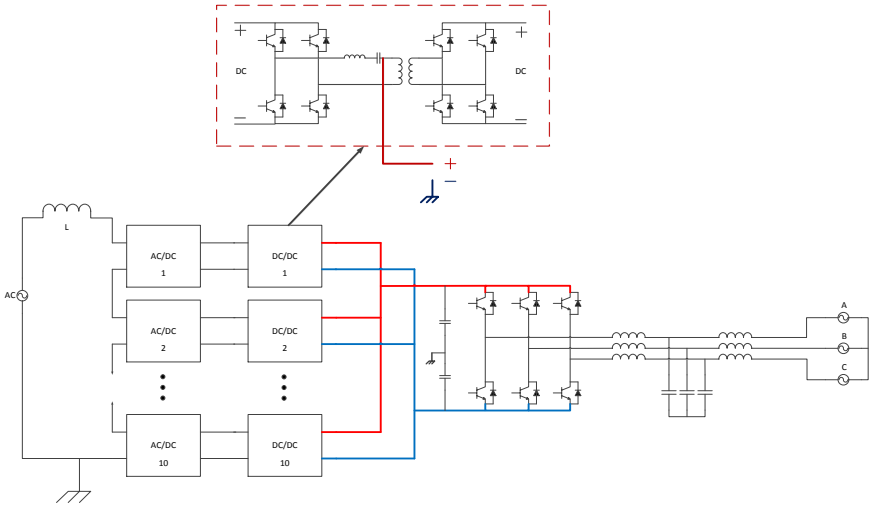


Figure 8.5: Terminals chosen to study Voltage Stress on Transformer winding with respect to ground

This voltage stress varies depending on the location of the module. Fig. 8.6 shows the maximum stress witnessed. It occurs in Module – 1. The voltage stresses in all other modules are shown in the next page.

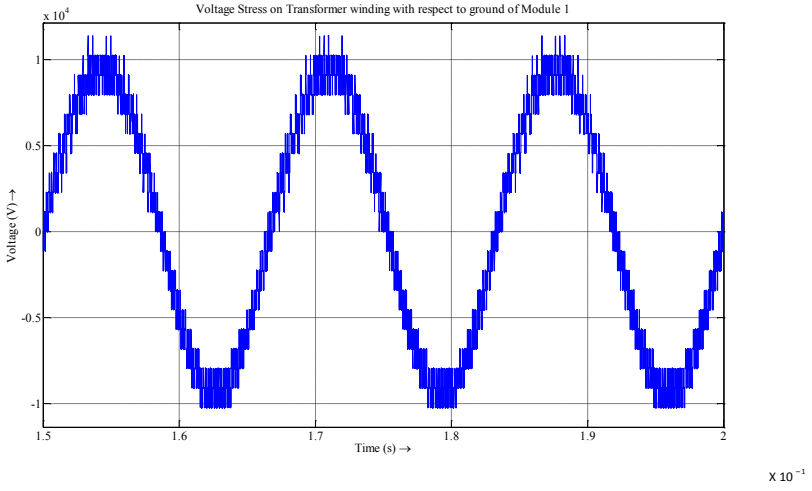


Figure 8.6: Voltage Stress on Transformer winding with respect to ground

8.4.4 Voltage difference across middle point of Transformer

Fig. 8.7 shows two terminals across which voltage is measured. It depicts the voltage difference across middle point of the transformer windings.

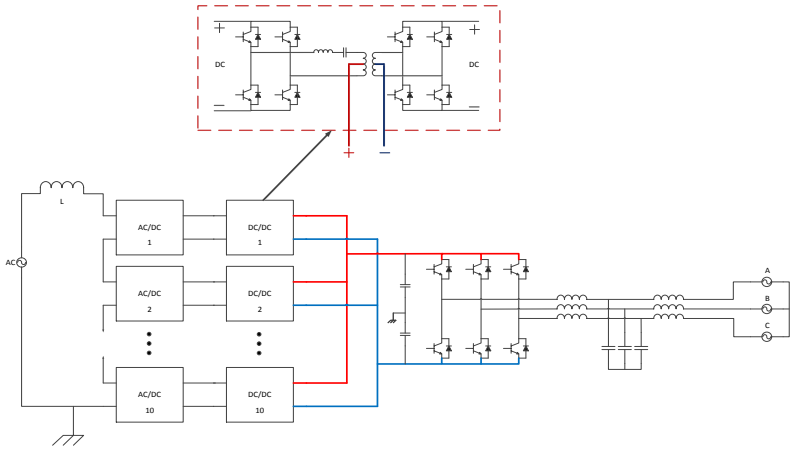


Figure 8.7: Choice of terminals to study the voltage difference across middle point of Transformer

Fig. 8.8 shows the maximum stress witnessed across these terminals. This maximum stress occurs in Module 1. The stresses reduce as we go from Module 1 to 10, which is similar to the case mentioned in 8.3.3.

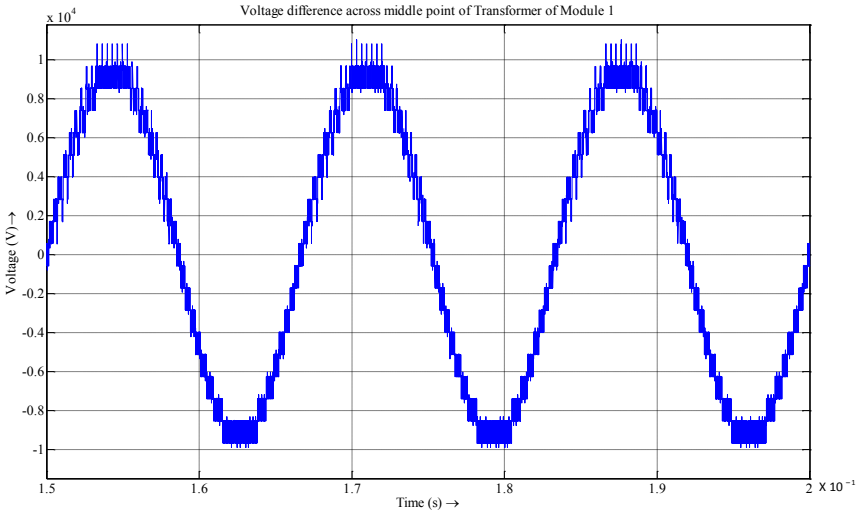


Figure 8.8: Voltage difference across middle point of Transformer

8.4.5 Voltage difference across the top point of Transformer

Fig. 8.9 shows two terminals across which voltage is measured. It depicts the voltage difference across the top point of the transformer windings.

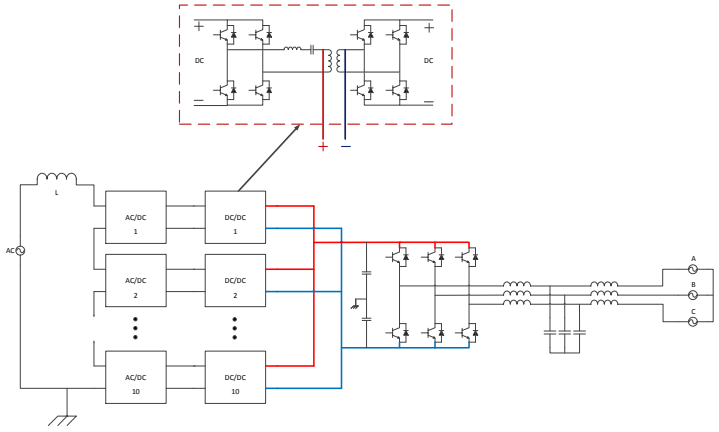


Figure 8.9: Chosen Terminals to study the voltage difference across the top point of Transformer

Fig. 8.10 shows the maximum stress witnessed across these terminals. This maximum stress occurs in Module 1. The stresses reduce as we go from Module 1 to 10, which is similar to the case mentioned in 8.2.3.

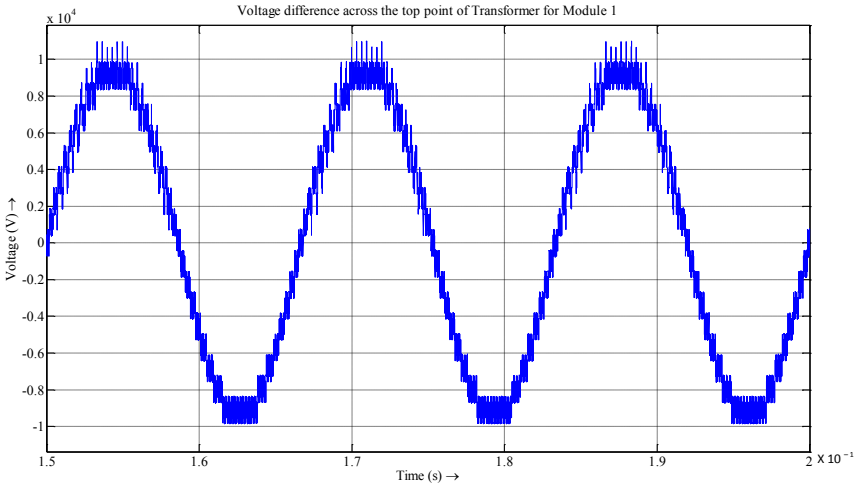


Figure 8.10: Voltage difference across the top point of Transformer

8.4.6 Voltage difference across diagonal points of Transformer

Fig. 8.11 shows two terminals across which voltage is measured. It depicts the voltage difference across the diagonal points of the transformer windings.

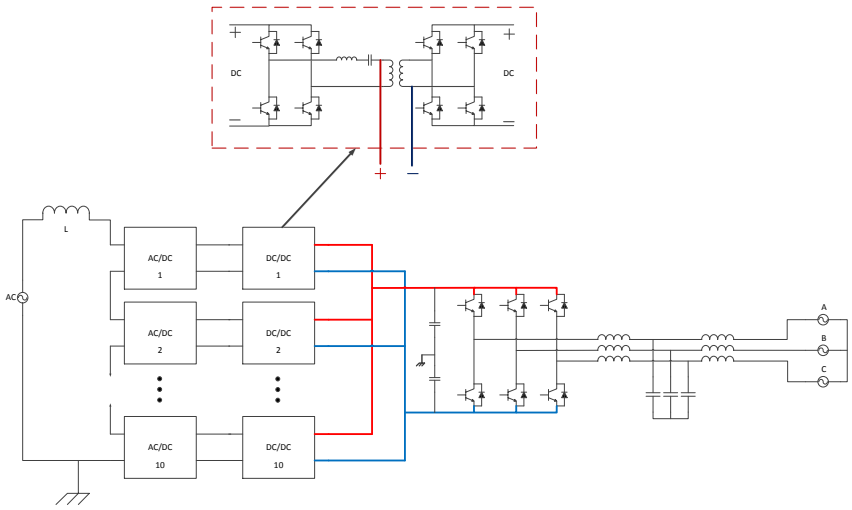


Figure 8.11: Choice of terminals to depict the voltage difference across diagonal points of Transformer

Fig. 8.12 shows the maximum stress witnessed across these terminals. This maximum stress occurs in Module 1. The stresses reduce as we go from Module 1 to 10, which is similar to the case mentioned in 8.2.3.

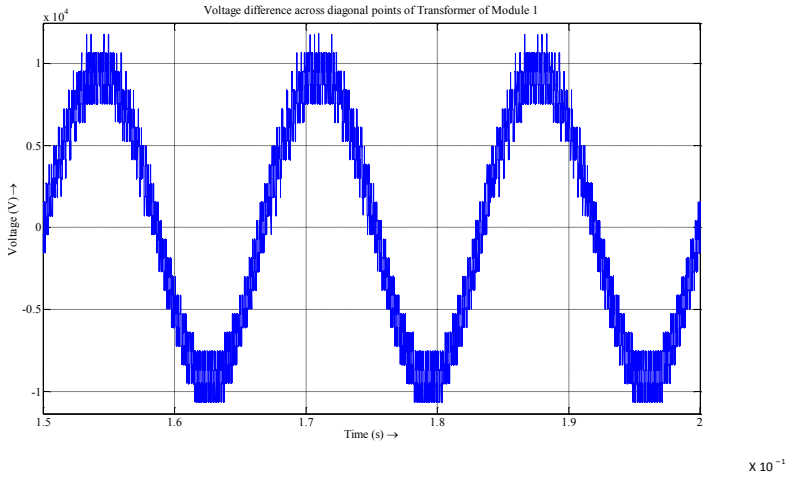


Figure 8.12: Voltage difference across diagonal points of Transformer

8.4.7 Voltage difference across diagonal points of Transformer

Fig. 8.13 shows two terminals across which voltage is measured. It depicts the voltage difference across the diagonal points of the transformer windings (opposite orientation).

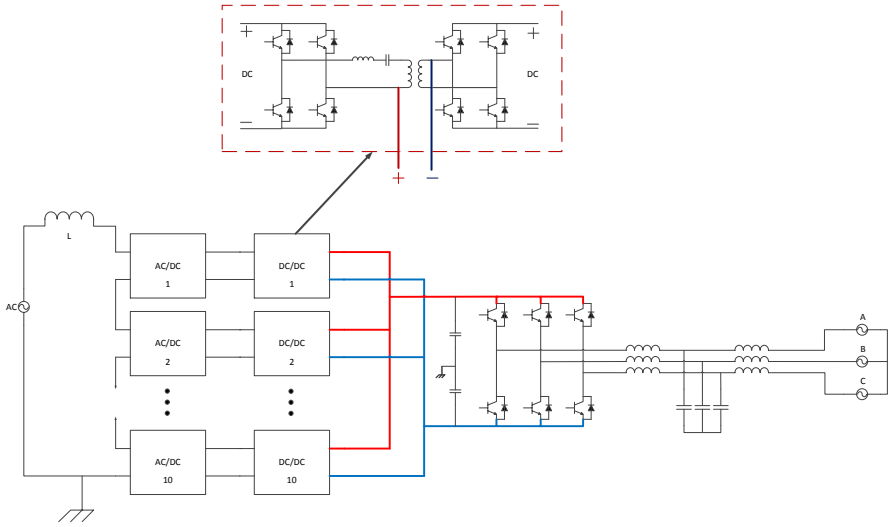


Figure 8.13: Voltage difference across diagonal points of Transformer (negative orientation)

Fig. 8.14 shows the maximum stress witnessed across these terminals. This maximum stress occurs in Module 1. This voltage is 180 degrees phase shifted from the previous case. The stresses follow the same trend moving down the modules as mentioned in the previous case.

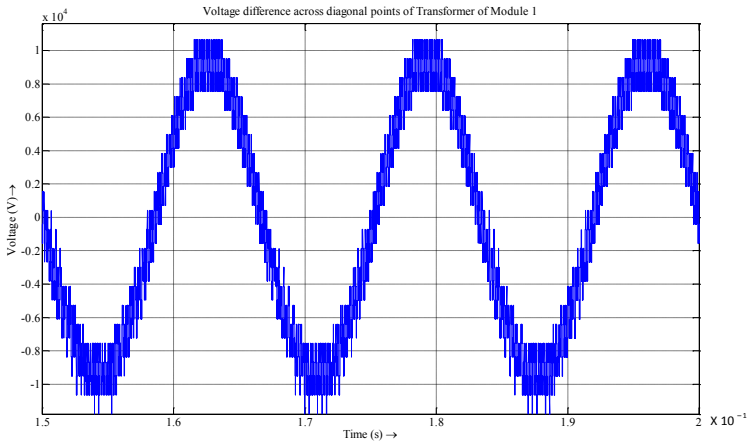


Figure 8.14: Voltage difference across diagonal points of Transformer

8.5 Optimized module control algorithm

In this case, depending on the control output signal of the rectifier stage, a particular module switches while the rest retain a steady state position (i.e. either shorted or series connected with capacitor). Similarly, depending on the control signal voltage level, only a handful of DC/DC converter would be active. This way, we would reduce both switching and conduction loss of the converter.

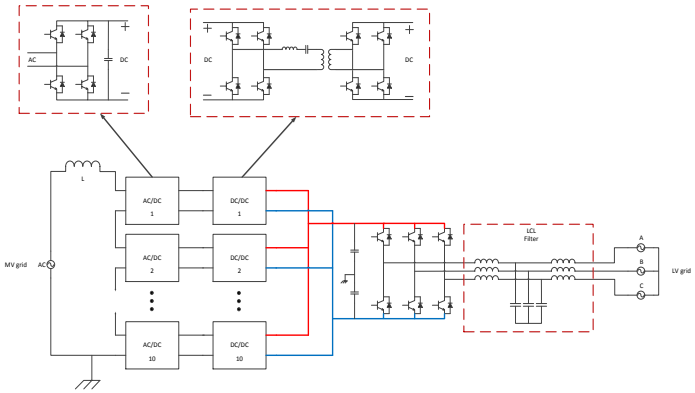


Figure 8.15: Circuit Schematic of the understudied SST

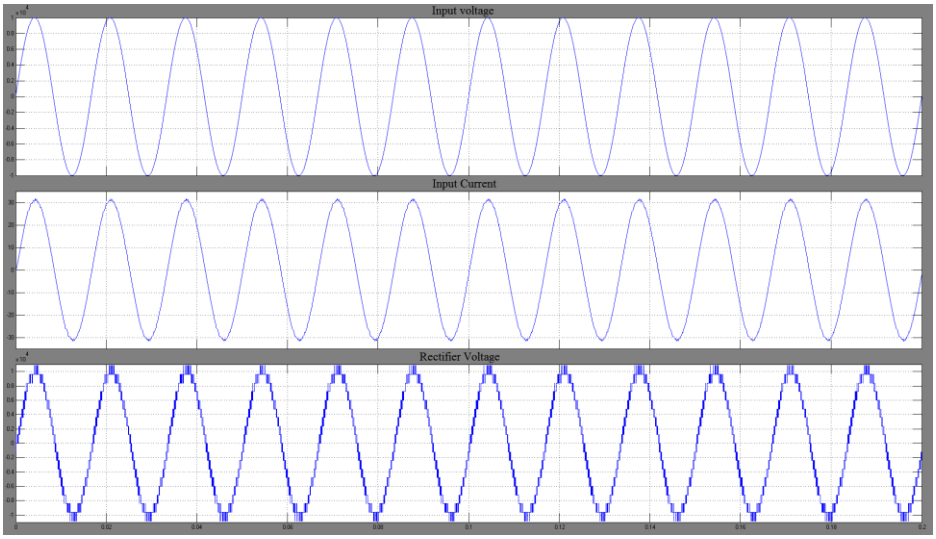


Figure 8.16: Input Voltage, Input Current and Rectifier (Input) Voltage

This however would require a larger input filter to give the same results (input current waveform) as the previous cases. Fig. 8.16 shows the input voltage and current characteristics.

8.6 Voltage Stress on Transformer as a function of Control Algorithm

This part of the report primarily contains the inter-winding voltage stresses in frequency domain. The main aim of this work is to show the variation of these stresses as we change the control algorithm. The work has been divided into four different cases depicting the voltage difference across middle point of Transformer. The various cases are:-

(1) Linear Delay: The sawtooth wave fed to module 1 is the most leading wave. The consequent modules are linearly delayed. Thus, the sawtooth waveform fed to module 2 lags the same of module 1 by 1/10th of time period.

(2) Zig-zag Delay: The sawtooth wave fed to module 10 is the most leading wave. The consequent modules are delayed in a zig-zag order. Thus, the sawtooth waveform fed to module 1 lags the same of module 10 by 1/10th of time period. So, the order of sawtooth wave propagation is : 1,10,2,9,3,8,4,7,5,6,1…

(3) Reverse Zig-zag Delay: In this case the order of the sawtooth wave propagation is : 10,1,9,2,8,3,7,4,6,5,10…

(4) Optimized module control algorithm - In this case, the control has been modified completely. Depending on the voltage requirement (set by the controller for unity power factor), only one of the rectifier module switches (at 3 kHz). Though the effective frequency at the rectifier stage is low (as compared to previous cases ~30 kHz), this would effectively reduce both switching and conduction loss of the overall

converter. Further, the magnitude/power spectrum would not contain any significant value at higher frequencies (~ 30 kHz, 60 kHz, etc.).

8.6.1 Linear Delay

(1) Line Frequency Component

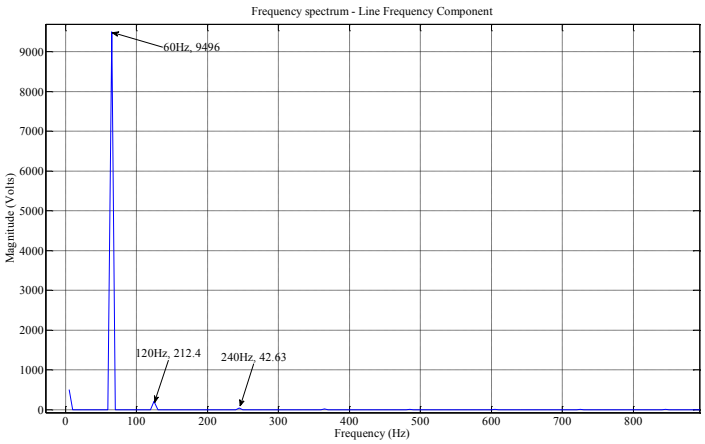


Figure 8.17: Frequency spectrum depicting Line Frequency Components

(2) Switching Frequency Component

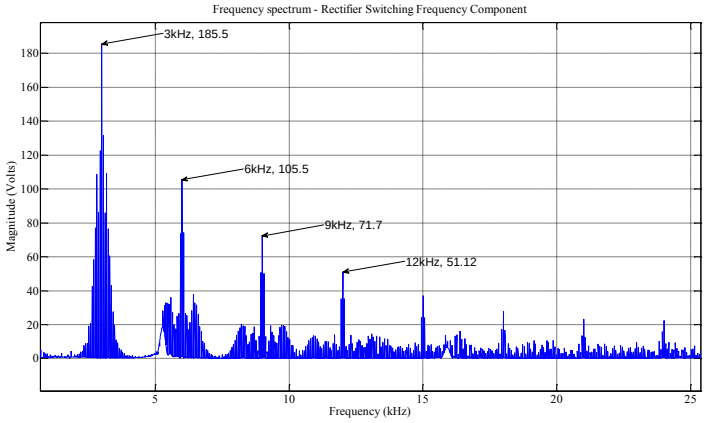


Figure 8.18: Frequency spectrum depicting Rectifier Switching Frequency Components

(3) Effective Switching Frequency Component

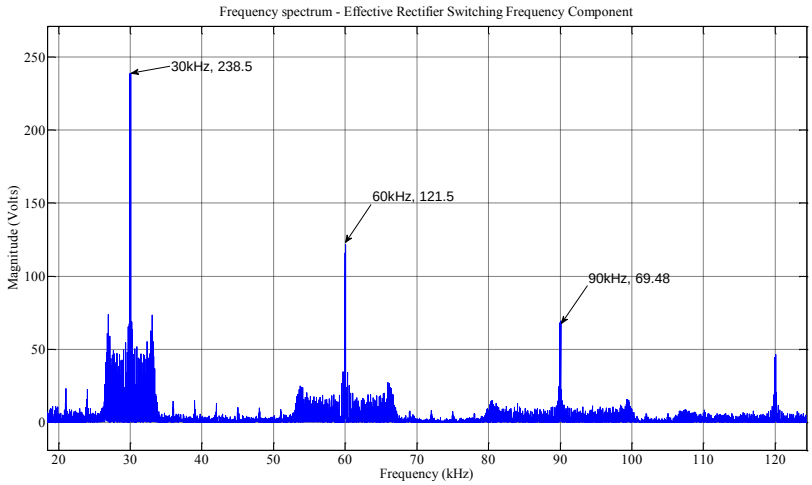


Figure 8.19: Frequency spectrum depicting Effective Rectifier Switching Frequency Components

8.6.2 Zig-zag Delay

(1) Line Frequency Component

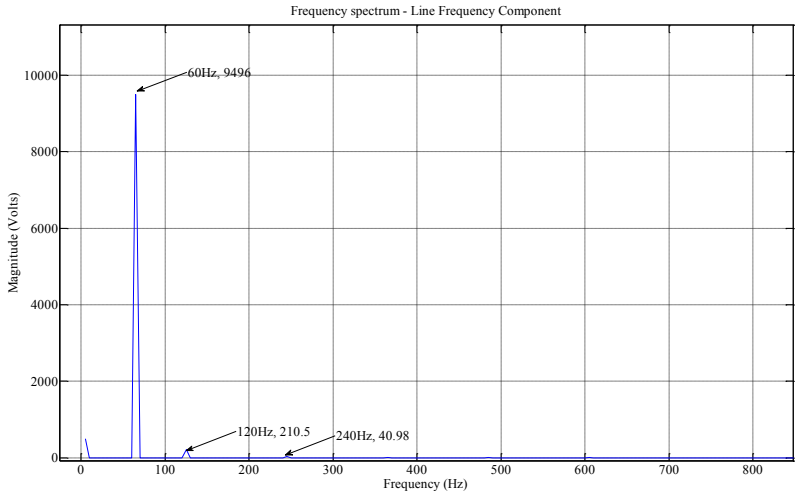


Figure 8.20: Frequency spectrum depicting Line Frequency Components

(2) Switching Frequency Component

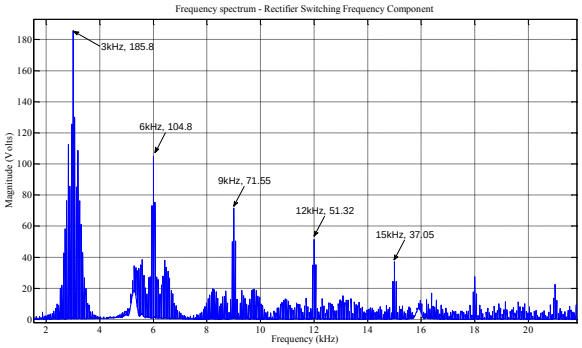


Figure 8.21: Frequency spectrum depicting Rectifier Switching Frequency Components

(3) Effective Switching Frequency Component

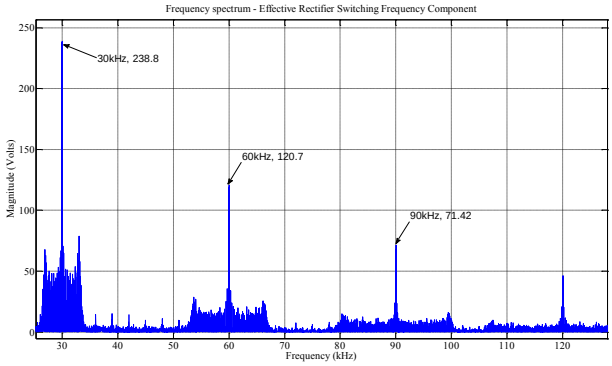


Figure 8.22: Frequency spectrum depicting Effective Rectifier Switching Frequency Components

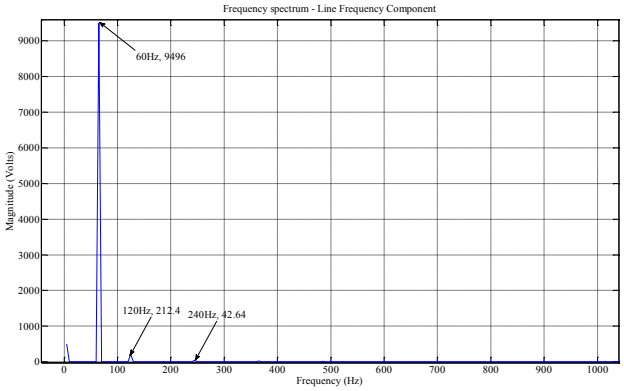


Figure 8.23: Frequency spectrum depicting Line Frequency Components of Section 8.6.3

8.6.3 Reverse Zig-zag Delay

(1) Line Frequency Component

(2) Switching Frequency Component

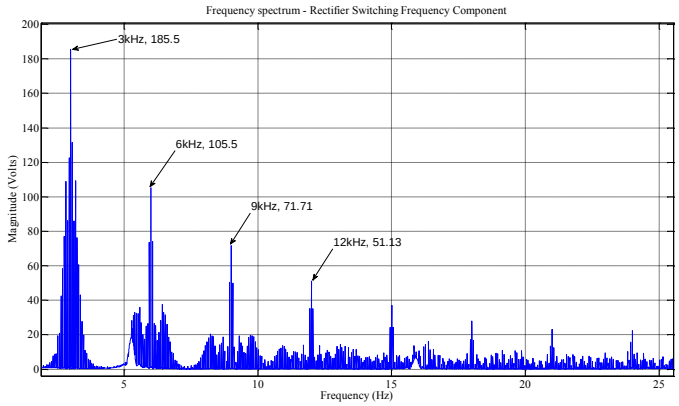


Figure 8.24: Frequency spectrum depicting Rectifier Switching Frequency Components

(3) Effective Switching Frequency Component

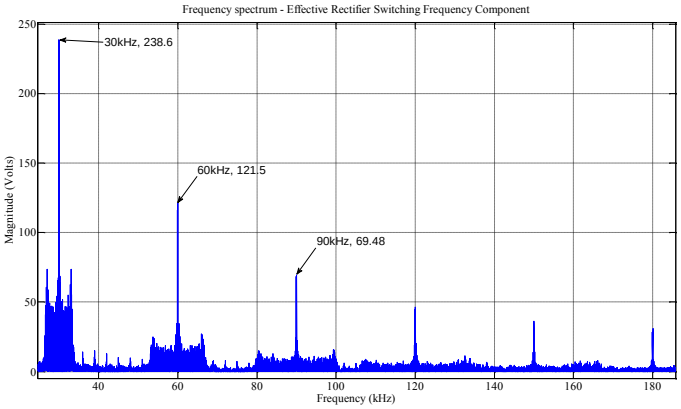


Figure 8.25: Frequency spectrum depicting Effective Rectifier Switching Frequency Components

8.6.4 Optimized module control algorithm

(1) Line Frequency Component

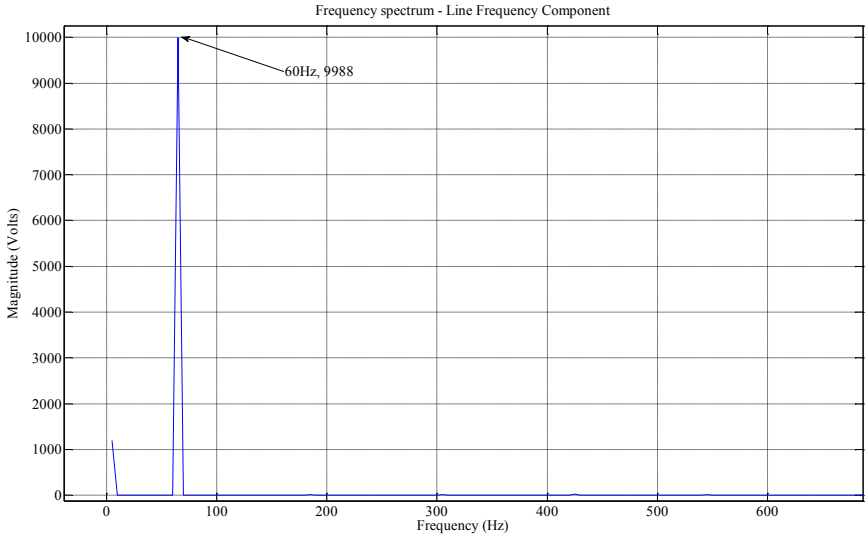


Figure 8.26: Frequency spectrum depicting Line Frequency Components

(2) Switching Frequency Component

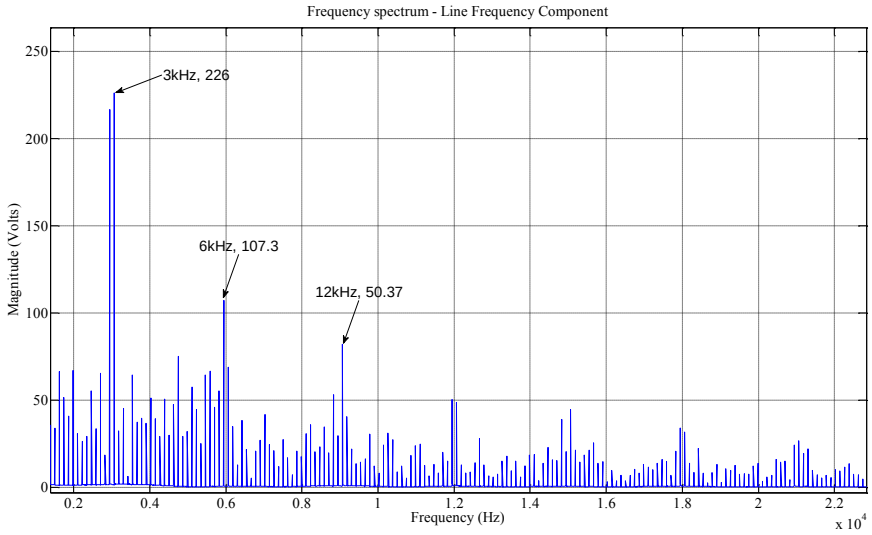


Figure 8.27: Frequency spectrum depicting Rectifier Switching Frequency Components

8.6.5 FFT Comparison

Tab. 5 shows the various frequency components of the Inter-winding voltage stress as a function of different previously mentioned cases.

Table 5: frequency components of the Inter-winding voltage stress of various cases

Frequency	Case #1	Case #2	Case #3	Case #4
60 Hz	9496	9496	9496	9988
120 Hz	212.4	210.5	212.4	-
240 Hz	42.63	40.98	42.64	-
360 Hz	18.38	16.74	18.38	-
3 kHz	185.5	185.8	185.5	226
6 kHz	105.5	104.8	105.5	107.3
9 kHz	71.7	71.55	71.71	82.14
12 kHz	51.12	51.32	51.13	50.37
15 kHz	37.02	37.05	37.03	44.69
30kHz	238.5	238.8	238.6	-
60 kHz	121.5	120.7	121.5	-
90 kHz	69.48	71.42	69.48	-

As expected, Case #4 did not have any 30kHz component. This results in less dielectric heating and less harmonic power factor. For cases #1, 2 and 3, the 30kHz component is higher than the 3kHz component. As we will see in the next chapter, dielectric heating is a strong function of high frequency harmonics. The frequency response shown in the previous section shows that case #4 has negligible component in the lower frequency harmonics, further it has no component in the 30 kHz range as the effective frequency of operation is same as the frequency of the rectifier stage. However, even with this scheme the inter-winding voltage still remain a function of the module location and high voltage stress is unavoidable.

A substantial part of the manufacturing cost of power converters for critical applications involves designing filters to conform to the varying EMI norms for the various domains. In the next part of this chapter, method of EMI reduction using spectral modification through chaotic modulation is proposed.

8.7 Chaotically jittered phase-shifted Multi-level Converter Algorithm

In this scheme, the converter is operated in regular periodic regime, and then the timing signal (the clock or the ramp waveform) is delayed by a random/chaotic number. This can be easily programmed in DSP for runtime implementation. Simulation results show reduction of spectral peaks and consequent spreading of the spectrum — which can be precisely controlled by adjusting the gain of the chaotic waveform. This scheme can thus eliminate filters and screens, or can at least reduce their size significantly [111][64].

The Logistic map has been used to generate these a-periodic/chaotic numbers and correspondingly the ramp waves are phase shifted a-periodically following these numbers. Thus, the time delay of the phase shifted scheme is not a constant.

The basic equation governing the Logistic map is:-

$$x_{n+1} = r * x_n * (1 - x_n)$$

Fig. 8.28 shows the bifurcation diagram of Logistic map as a function of the parameter 'r'.

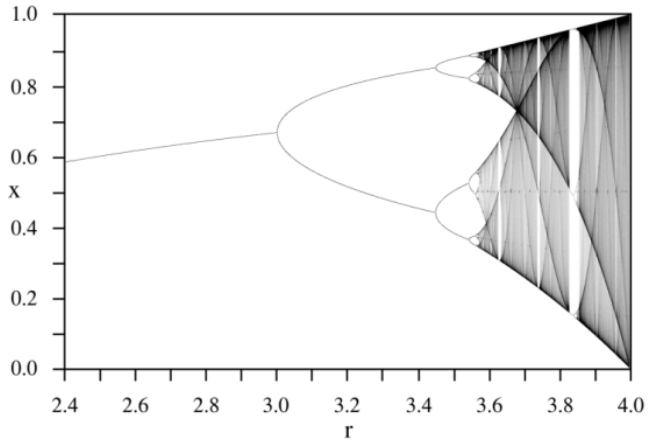


Figure 8.28: Bifurcation diagram of Logistic map

It can be easily seen that the system undergoes chaos when the value of 'r' is close to 3.8. Fig. 8.29 shows the Simulink implementation of this algorithm.

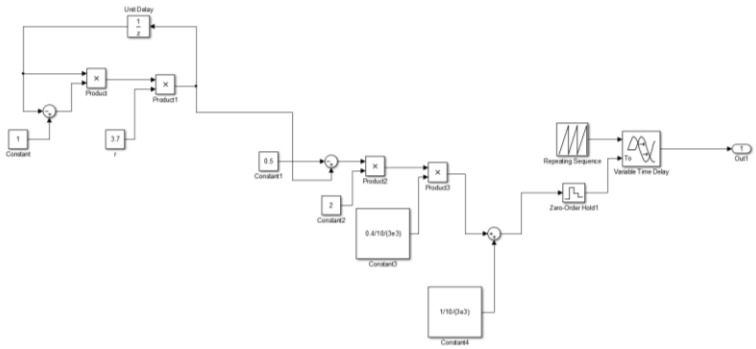


Figure 8.29: Simulink Block Diagram of chaotic number generator

Fig. 8.30 and 8.31 shows the spectral peaks of the regular phase shifted multilevel converter and of chaotically jittered phase shifted multilevel converter respectively. As can be seen in the figures, the spectral peak has now reduced to half of the value (from 0.02674 to 0.01382) when chaos is introduced to the switching.

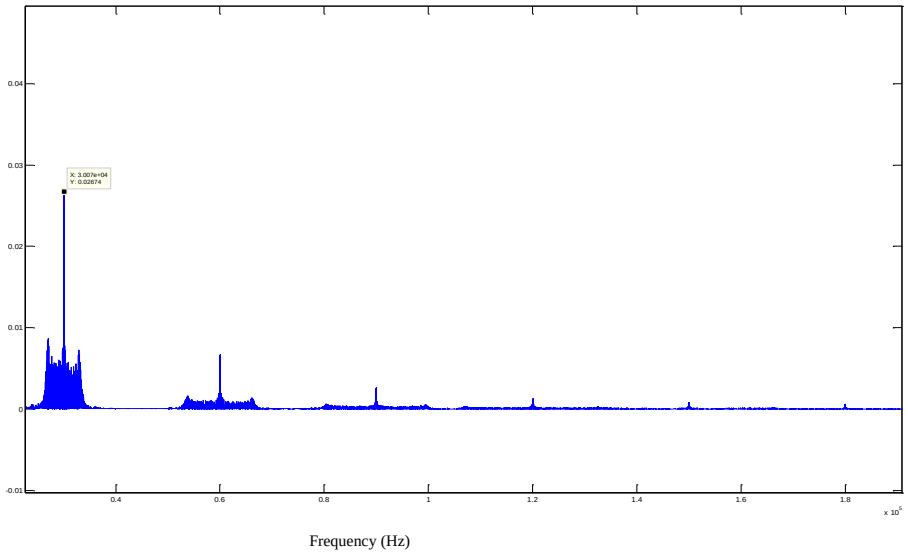


Figure 8.30: Spectral Peaks of Input Current of a generic Phase shifted Multilevel Converter

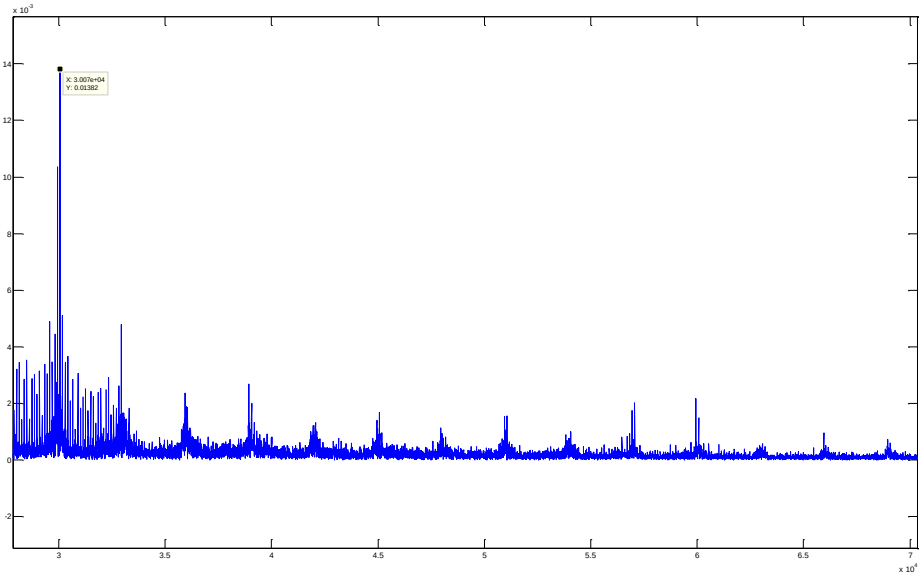


Figure 8.31: Spectral Peaks of Input Current of chaotically jittered Phase shifted Multilevel Converter

8.8 COMSOL Simulation Results

As some crucial nodes of the SST can experience high voltage (~10kV) with respect to ground, the mechanical design and ground placement of the system automatically becomes a big concern. In this part of the chapter, an attempt has been made to study the voltage profile distribution in a typical module. At first a 2D model is made to emulate a power module in a glass framework connected to Aluminium based heat sink. To simplify the system, rectangular structures are chosen to represent both heat sink and the dielectric medium separation Silicon from the heat sink. To this model, a 10kV voltage is applied on the top surface of the dielectric medium with the base of the structure grounded. At first, the heat sink is placed directly on top of the base of the structure. Fig. 8.32 shows this arrangement. Fig. 8.33 shows the simulation result depicting the voltage distribution in the mechanical

structure. It can be easily seen that the dielectric medium has to withstand a large voltage as the heat sink is nearly close to zero potential.

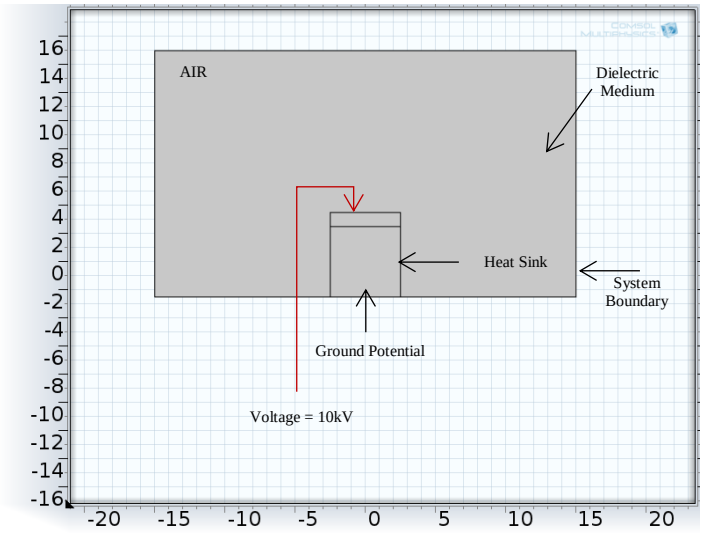


Figure 8.32: COMSOL Geometry

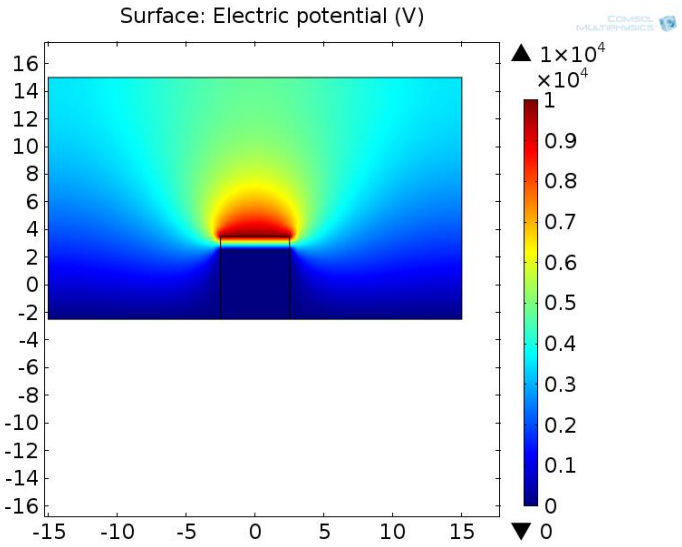


Figure 8.33: COMSOL Space Voltage Distribution

Fig. 8.34 shows the voltage profile distribution along the vertical line passing through the middle of structure. An obvious solution to this problem is to elevate the power module+heat sink stature magnitudes higher than the width of the dielectric medium. In doing so, the voltage of the heatsink will be much closer to the chip voltage. This would result in lower voltage across the dielectric medium.

Fig. 8.35 shows the new structure. Reasonable amount of clearance has been provided between the heat sink and ground. Fig. 8.36 shows the simulation result depicting the voltage distribution in the mechanical structure. Fig. 8.37 confirms an improved voltage profile along the middle line of symmetry.

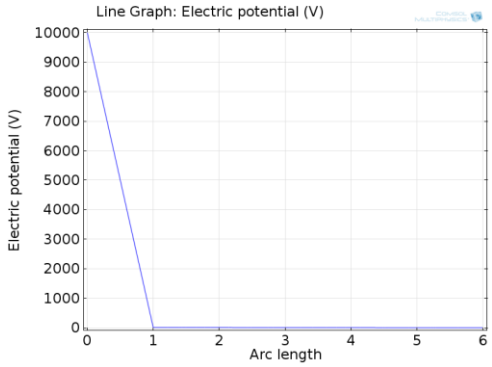


Figure 8.34: Voltage Profile distribution along the vertical line passing through the center of geometry

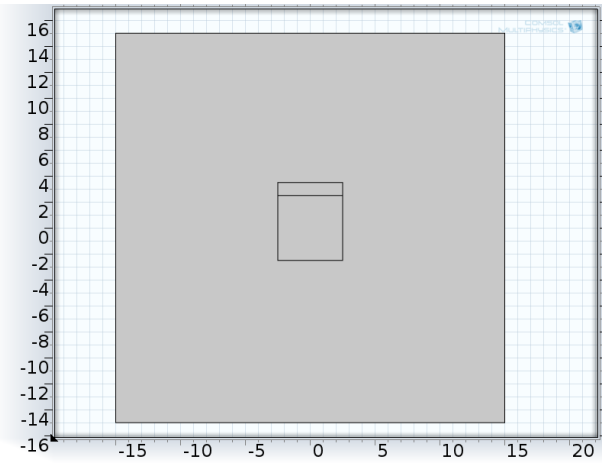


Figure 8.35: COMSOL Geometry with reasonable clearance

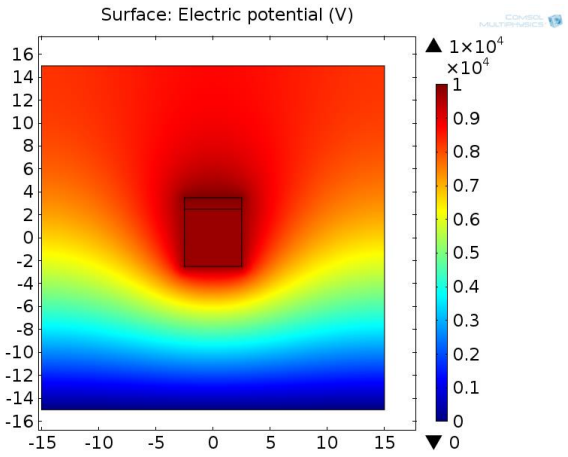


Figure 8.36: COMSOL Space Voltage Distribution

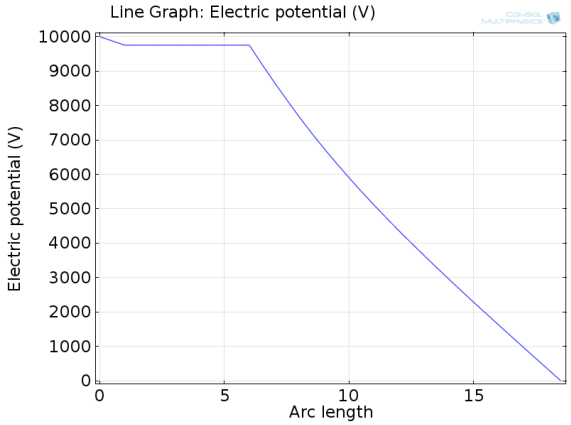


Figure 8.37: Voltage Profile distribution along the vertical line passing through the center of geometry

8.9 Prediction of ageing and material selection

Dielectric heating is one of the main reasons behind aging and breakdown mechanism in materials used for high voltage isolation. When exposed to voltage waveforms containing high amount of harmonics, the heat generation will be larger due to increased power losses as compared with power frequency excitation. This may result in decreased life or even failure of isolation due to the increased operating temperature or thermal runaway.

Presence of high frequency non-sinusoidal (PWM) voltage enhances this loss. In subsequent chapters we will witness the equivalent frequency of operation of the rectifier stage is as high as 30 kHz. This introduces high frequency PWM voltage across the winding of the transformer. A detailed study has thus been made to compare these losses as a function of control algorithm. A hardware test setup has been proposed to see these effects. The main aim of this test will be to choose the best isolation material.

8.10 Introduction to Dielectric Heating

Dielectric heating is one potential aging mechanism active below partial discharge inception voltage in materials used as high voltage insulation. The mechanisms of dielectric heating for sinusoidal voltages containing only one frequency are widely known. Major investigations on a range of insulating materials were performed by Chapman et al already in 1954 [112][65]. The effects of voltage waveforms with high harmonic content have not been examined as carefully yet, although some authors mentioned it as a possible aging factor [113]-[118]. It is important to study the effects of dielectric heating for the study of sub-inception aging and separate among different processes. Dielectric heating accelerates aging but it is not the only process active in sub-inception aging [119]. The influence of power frequency voltage with a single high amplitude superposed harmonic on degradation rate of self-healing polypropylene capacitors was investigated in [114]. RMS voltage levels were found to be the factors influencing the degradation mostly, whereas the influence of the dielectric heating was difficult to separate from the voltage parameters. To describe the power losses at voltages with a plurality of frequencies mathematically, a theoretical approach is presented in [120].

The dielectric losses in a dielectric material for time varying sinusoidal (ac) voltages can be expressed as:

$$P_{ac}(\omega) = U_{RMS}^2 * \omega * C'(\omega) * \tan\delta(\omega)$$

where U_{RMS} is the RMS value of the applied voltage and ω is the angular frequency (rad/s), C'(ω) the real part of the capacitance (F) and tanδ is the dissipation factor.

In its most basic form, the above mentioned equation only considers the contribution to the developed power from a single sinusoidal waveform. When non-sinusoidal waveforms act, the total voltage can be considered as a sum of sinusoidal components, as expressed in:-

$$U(t) = U_{dc} + \mathrm{Re}[\sum_{n=1}^{\infty} \sqrt{2} U_n e^{j\omega_o nt + \varphi_n}]$$

U_n being the RMS voltage of the n^{th} harmonic, θ_n the phase for harmonic n and ω_0 is the fundamental angular frequency. A harmonic and repeatable waveform is thus implicit in this equation. If the term $U_{dc} \neq 0$, the power developed by resistive heating must be taken into account. However, the conductivity of insulating materials is usually very low, making the power developed by resistive heating much lower than the power developed by dielectric heating. Neglecting the resistive part is therefore a reasonable simplification for most insulating materials, leaving us with the following expression:

$$P = \sum_{n=1}^{\infty} U_n^2 * n * \omega_o * C'(n\omega_o) * \tan\delta(n\omega_o)$$

In order to describe the relative increase of power losses due to the harmonic content, the above mentioned expression can be related to losses from a pure sinusoidal voltage with the same fundamental frequency and RMS value as the non-sinusoidal waveform. If the harmonic components are divided with the RMS voltage U_{RMS} of the sinusoidal waveform, a set of dimensionless numbers u_n are obtained.

$$u_n = \frac{U_n}{U_{RMS}}$$

In low frequency range, the change polarization remains almost constant. This further simplifies the expression.

$$\frac{C'(n\omega_o)*\tan\delta(n\omega_o)}{C'(\omega_o)*\tan\delta(\omega_o)} \approx 1$$

Therefore the harmonic power factor (p_{fact}) can be obtained by:-

$$p_{fact} = \frac{P}{P_{ac}(\omega_o)} = \sum_{n=1}^{\infty} u_n^2 * n * \omega_o$$

Thus, knowing the properties of the insulation material and of the waveform, the excess dielectric loss power can be calculated using this. This result can then be related to a conventional dielectric heating calculation for the fundamental frequency in any insulation system.

The quantity of the heat Q of a sample with the mass m and the heat capacity c at a temperature gradient of $\Delta\theta$ is:

$$Q = m * c * \Delta\theta$$

The heat dissipation by convection is

$$Q_c = h * A_c * t * \Delta\theta$$

Where, 'h' is the heat transfer coefficient, A_C is the effective surface for convection and t is time.

In a test set-up with a sample stressed by an electrical field, where heat radiation and heat conduction dissipation mechanisms can be neglected compared to convection, the following equation is valid:

$$P = c * m * \frac{d\Delta\theta}{dt} + \alpha * A_c * \Delta\theta$$

The solution of the differential equation is:

$$\Delta\theta(t) = \frac{P_{DL}}{\alpha * A_c} * \left(1 - e^{-(\frac{hA_c}{mc})t}\right)$$

The temperature curve thus follows a stabilized exponential increase. The steady state is reached, if the generated heat Q is equal to the dissipation heat Qc by convection.

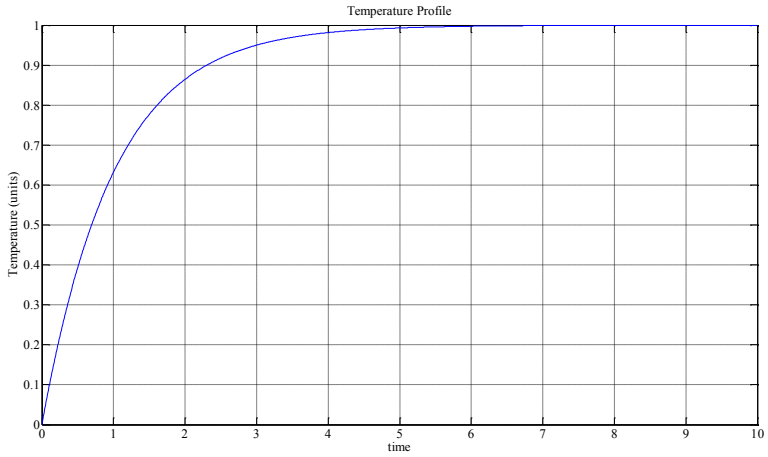


Figure 8.38: Temperature response curve of the heating of a sample considering only internal heating and convection

8.11 Harmonic Power Factor and Total Dielectric Loss

The main aim of this part of the report is to compare the harmonic power factor of the two major control schemes. Table 5 in the previous section showed the various harmonic contents as a function of various control algorithms. The harmonic power factor is thus calculated for Case 1 and 4 as Cases 2 and 3 are quite similar to Case 1. Table 6 shows the corresponding harmonic power factors.

Table 6: Harmonic Power Factor

Case #	Harmonic Power Factor
Case 1	0.61
Case 4	0.05

As indicated in Table 3, even though there are several advantages of Case 1 control scheme, when it comes to dielectric heating, it causes considerable high heat generation. Thus, case 1 control scheme is more susceptible to thermal runaway. If the material testing under superimposed high voltage power frequency sinusoidal with high frequency PWM shows negative results, case 4 control strategy would thus be a better alternative.

From COMSOL Simulation, C = 2 nF

Assuming, $\tan\delta = 0.02$ (very conservative choice)

Total Dielectric Power Loss, $P_{Loss} = U^2 * \omega * C * \tan\delta$

From the previous simulations, the total Dielectric Loss came out to be 2.2W.

8.12 Proposal for Experimental Test Setup

In this part of the chapter, the measuring of dielectric heating of insulating materials stressed by high power-frequency voltages superimposed by high-frequency high-voltages (mixed-voltages) is described. The aim of the proposed work is to make a statement regarding the influence of superimposed high-frequency voltages on the dielectric heating of nonpolar and polar polymers in steady state operation. As shown in Chapter 2, the inter-winding voltage stress seen in some of the modules goes way beyond the terminal voltage levels. Therefore, the design of transformer for a standalone DC/DC converter will be quite different from the DC/DC converter (with same terminal voltage ~1.1kV) of the understudied cascaded system. To ensure a reliable and sustainable electrical system, all components of the systems have to withstand new demands concerning the dielectric stress. Fig. 8.39 shows the proposed test circuit for mixed-frequency voltage generation consisting of a power-frequency voltage and a high-frequency PWM. To protect the elements of the test systems and to ensure a useful voltage distribution in the circuits, decoupling elements are used.

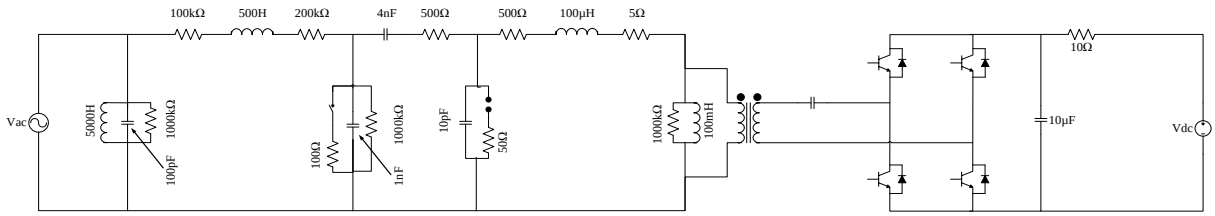


Figure 8.39: Proposed Test Circuit for mixed voltage stress analysis

Here V_{ac} is 10kV, 50Hz sinusoidal wave while V_{dc} is a 1.1kV, 10kHz PWM/square wave. The values are so chosen to emulate a real-world stress which the dielectric medium would experience inside the high frequency transformer.

Fig. 8.40 shows the voltage stress across the dielectric with dielectric and displacement current of the high frequency transformer.

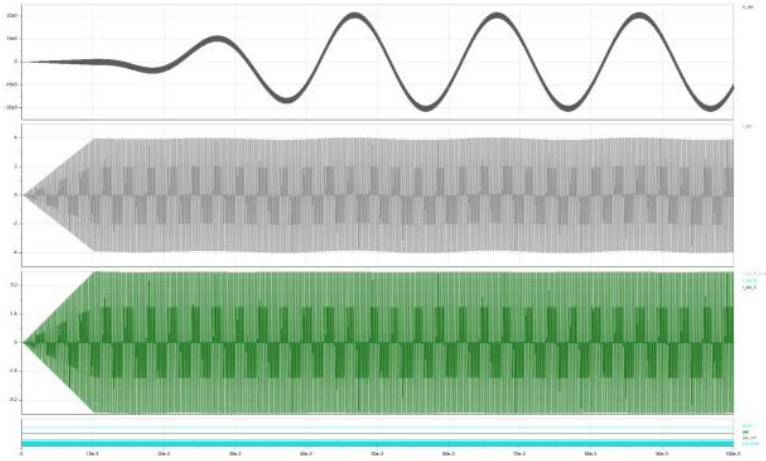


Figure 8.40: Voltage Stress on the Dielectric, Magnetizing and Input Current of High Frequency Transformer

8.13 Choice of Electrode Configuration

The next important step of mixed frequency test is to come up with an appropriate Electrode Configuration which yields uniform Electric field. Various orientations were studied. The advantages and disadvantages of each are mentioned below.

(i) Basic configuration: Fig. 8.41 shows a simplified diagram of this configuration. Simplicity of design is an advantage of this configuration. However, this arrangement would lead to high electric field stress near the round edges of the electrodes.

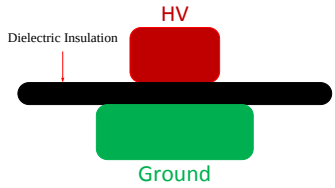


Figure 8.41: Basic Configuration

(ii) Basic Configuration with taped wedges: Fig. 8.42 shows this arrangement. This effectively lowers the electric field stress in the system. One major challenge would be to avoid air gaps between the taped filling, electrode and insulation. This might cause unexpected partial discharge which in turn would bring down the Breakdown Voltage.

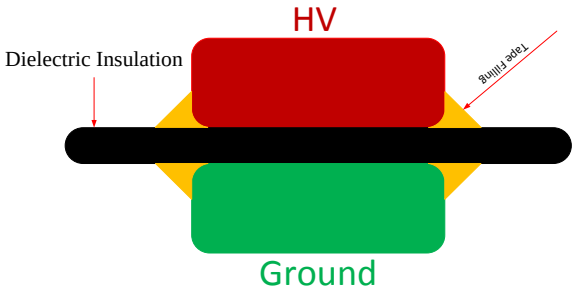


Figure 8.42: Basic Configuration with taped wedges

(iii) Equipotential Electrodes: Fig. 8.43 (a) and (b) shows this configuration. The main advantage is reduction of Electric Field stresses. This is one of the preferred

configuration which is both simple to implement and easy to transform to any of the above configuration if needed.

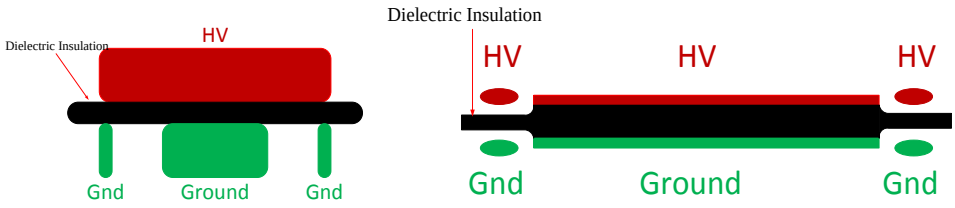


Figure 8.43: (a) Multiple Grounded Electrodes; (b) Multiple symmetric electrodes

(iv) High precision Electrode: Fig. 8.44 shows this configuration. One advantage of this configuration is that now we know the exact location of high electrical field.

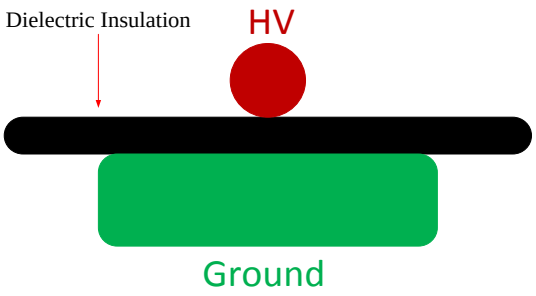


Figure 8.44: High precision Electrode Configuration

(v) Painted shield with soldered Electrode: This configuration is bound to have the least non-uniform electric field stress. This however would be a cumbersome arrangement to deal with in case of failure as the new specimen will have to me reiterated to get this configuration. Fig. 8.45 shows a simplified model of this configuration

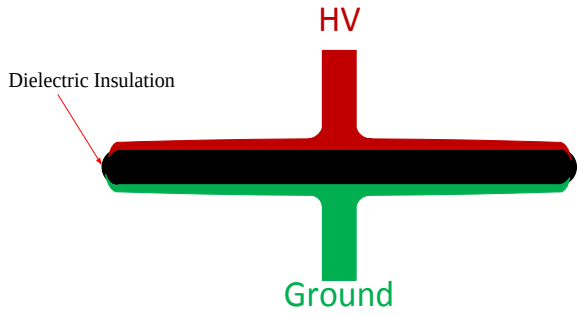


Figure 8.45: Painted shield with soldered Electrode

8.14 COMSOL Simulation of Electrode System with Tapped Wedges

Electrode System with Tapped Wedges (Case (ii)) mentioned in the previous section has been simulated in COMSOL. Fig. 8.46-8.49 shows the Electric Field distribution in the space around the electrode-insulation assembly.

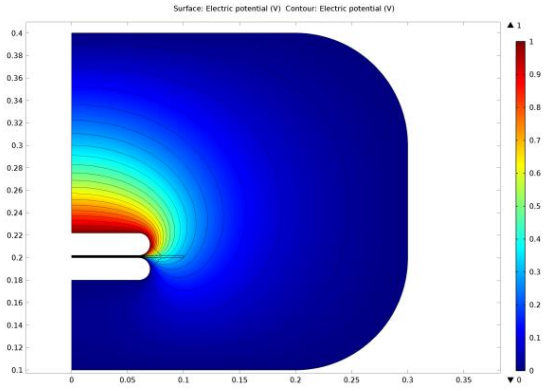


Figure 8.46: Electric Potential Distribution of the tapped wedges

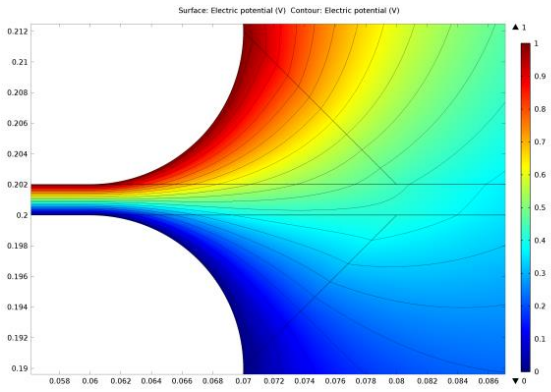


Figure 8.47: Electric Potential Distribution of the system

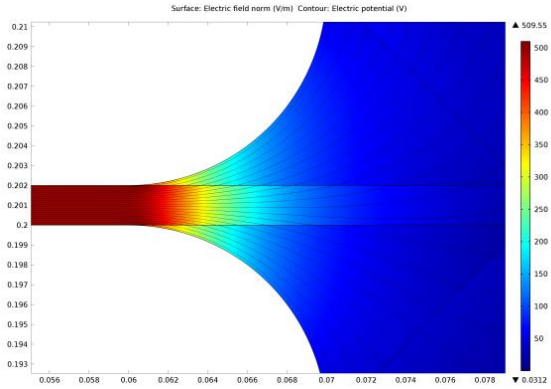


Figure 8.48: Electric Field Distribution of the system without tapped wedges

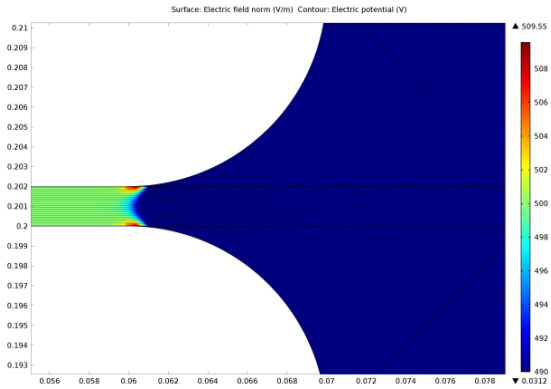


Figure 8.49: Electric Field hotspots of the system without tapped wedges

Fig. 8.49 shows electric field hot spots at the edges. It must be noted that this is still quite less crucial than case (i).

8.15 Conclusion

The basic functionality and usage of solid state transformer (SST) is reviewed. The understudied SST has been simulated with various control algorithm and the advantages and disadvantages of each are mentioned. Due to the asymmetric structure of the SST, the voltage stress experienced by module varies depending on the location of the same. The critical voltage stress witnessed in the topology is mentioned and dielectric heating as a possible cause of thermal runaway is considered. Simulation results of the understudied SST show various stresses occurring in the topology. An effort has been made to witness any reduction of stress as a function of control algorithm. A new control algorithm is introduced which effectively reduces various losses in the converter. It also reduces the high frequency stress and thereby is less susceptible to dielectric heating. A new form of algorithm has also been tried which introduces chaotic jittering in the switching scheme to reduce spectral peaks. This forms an effective low cost method of reducing EMI of the system. The FFT of various waveforms are studied and compared. COMSOL based simulations are also presented depicting voltage distribution in the module. A preferred mechanical design of the modules is also proposed.

The literature review helped in forming a knowledge base of various similar researches. Important material selection for electrode, bushings, etc have been listed. A mathematical formulation of dielectric losses corresponding to the various control algorithms is presented. It is shown that high frequency non sinusoidal components of the voltage waveform causes increased dielectric losses and thereby results in increased heating. A test setup is proposed

to monitor dielectric heating for various materials. Various preferred electrode configurations have been listed. COMSOL simulation of one of the configuration is presented.

Future work would involve hardware testing of the proposed test circuit. It would involve 10kV, 50/60Hz high voltage supply juxtaposed with 1-3kV, 30 kHz PWM/square wave voltage. This mixed frequency voltage will be applied across a material under test. Various materials will be tested and a suitable material apt for the given application will be chosen.

CHAPTER 9

CONCLUSIONS

Chapter 1 introduces the basic theme of the thesis. Various prior art based power electronic converters are mentioned and a brief introduction of the understudy is mentioned. Reverse Blocking Device characterization is mentioned to show the basic need for this study. One of the section deals with the Dynamic VAR Compensator which may be considered as an immediate practical implementation of the understudied converters.

Chapter 2 presents a new genre of Current Source based AC/AC converter, DynaC. The working principle, simulation and hardware results of the full system have been presented. A slight modification of the topology has been proposed to include battery interface. Hardware results of the same have been presented showing bi-directional power flow. A cascaded version of this topology has also been proposed. Working principle and hardware results of the same has been presented in details. The controller used in this work is quite different from the one used by the inventors of this topology. The proposed controller forces the converter to work under DCM. This effectively reduces the loss occurring due to reverse recovery of diode. This also facilitates usage of Si-PiN Diodes which now with this controller would yield similar efficiency as SiC JBS Diode. A sparse rectifier topology has also been proposed and various advantages have been enumerated.

Chapter 3 presents a novel bi-directional soft-switched AC/AC converter. The working principle, simulation and hardware results of the full system have been presented. A sparse AC/DC rectifier has been proposed for Data Center based application. Hardware results of the same have been presented. A brief guide has been given for device selection. The work

presented in this chapter effectively reduces the number of switch requirement for power transfer without changing the power quality or adjusting the frequency of operation. As the dV/dt across the switches are limited by the dV/dt of the resonant sinusoidal, this converter can be used for high voltage converter applications to negate unwanted EMI issues.

Chapter 4 deals with reverse blocking device characterization. Reverse Voltage Commutation, Switch Overlap Characteristics, Hard Switched, and Forward characteristics of various suitable devices have been tested and studied. The loss data has been used in a look-up table based circuit simulator to predict the total device losses. Both DynaC and Soft Switched AC/AC (as mentioned in Chapter 3) have been simulated showing the appropriate choice of device for each. An attempt has been made to test with high voltage (6.5kV) SiC Thyristors. The turn on loss and transition time of the device shows a paradigm shift from conventional silicon based devices. Owing to reduced switching losses, this device can be used for high voltage, high current and high frequency converters.

Chapter 5 deals with optimized module design. Several hardware and FEM based software results are reported. A comprehensive design based study has been shown to fabricate an optimized current switch module. Various experimental results have been shown of the module operating up to 4kV.

Chapter 6 shows optimized designs for the magnetics components of the circuit. Several methods have been proposed to reduce portions of the core losses to better utilize the material and volume of the structure.

Chapter 7 focuses on Dynamic VAR Compensation. The power electronic converter working principle and initial hardware results have been presented. An extensive study has been carried out to show the various advantages of fast Volt-Var Control in an IEEE-34 Bus

system. A high PV penetration system has also been studied with and without the DVC. It has been shown that even the fast changing and unpredictable cloud shadowing effect can be mitigated with the use of DVC.

Chapter 8 forms the base for a new kind of SST based study. Voltage stress occurring in different sections of the converter has been studied and presented. A new optimized control system has been presented which effectively reduces this stress. Dielectric heating concept has been reviewed and a test setup has been proposed to study the effect of mixed frequency voltage stress on dielectrics.

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