ABSTRACT

KASUNAIDU VECHALAPU. Enabling High Efficiency Medium Voltage Converter for High Speed Drives and Other Grid Applications using Low Voltage (LV) and High Voltage (HV) Silicon Carbide (SiC) Devices. (Under the direction of Dr. Subhashish Bhattacharya).

The recent development of Wide Band Gap (WBG) devices such as LV SiC MOSFET devices and HV SiC devices have opened up the scope of research in medium voltage (MV) applications. This dissertation investigates the impact of series connected LV SiC MOSFET devices (such as 1.7 kV SiC MOSFETs) and the recently developed HV SiC devices : 10 kV SiC MOSFET, 15 kV SiC MOSFET, 15 kV SiC IGBT (2 µm & 5 µm buffer layer), on MV power electronic converters to enable (i) MV high – speed motor drive applications; and (ii) HVDC-MVDC or MVDC-LVDC interconnection for DC grid applications.

The MV voltage source Inverter for high-speed drive applications require DC bus ≥ 3.6 kV and switching frequency ≥ 5 kHz to get AC voltage ≥ 2 kV (L-L) with fundamental frequencies ≥ 500 Hz. To meet the high AC output current requirement for >300 kW load high-speed motor drive applications, series connection of low voltage high current 1.7 kV SiC MOSFETs with RC snubber is investigated. Design criteria for selection of RC snubber for series connection is explained and a methodology to find optimal RC snubber for series connection using experimental characterization is presented. Analytical expressions to determine the rating of snubber resistor and snubber resistor losses are presented. A basic building block (one phase leg of three phase converter) with four series connected device (per arm of phase-leg) is designed, fabricated, tested in different converter configurations (such as Full-bridge and Half-bridge Inverter, DC-DC converter) for different operating conditions. Comparison of series connected 1.7 kV SiC MOSFETs with 6.5 kV Si IGBT is presented. The estimated powered density of variable source drive (VSD) section is compared with the US-Department of Energy specifications (DOE).

To evaluate the impact of HV SiC devices in MV power converters, a detailed characterization of 15 kV SiC MOSFET (two parallel dies per module) and demonstration of a DC-DC boost converter (unidirectional and bidirectional configurations) using 15 kV SiC MOSFET in continuous switching mode (endurance test) at different operating conditions is presented. Also, switching characterization of 15 kV SiC IGBT module (two parallel dies per module) is presented. Importance of comparing HV SiC devices (15 kV SiC MOSFET and 15 kV SiC IGBT) at same '*dv/dt'* conditions is discussed. The comparison of total loss for HV SiC modules (10 kV SiC MOSFET, 15 kV SiC MOSFET, 15 kV SiC IGBT) with series connected 1.7 kV SiC MOSFETs is presented.

To enable the operation of HV SiC devices in DC-DC soft switching converters for MV/HV applications at extremely low *dv/dt* values, detailed experimental characterization is explored on (i) the soft switching of HV SiC devices using external snubber and (ii) series connection of HV SiC devices using external snubber. It showed that a low-cost small snubber capacitor across the device makes Punch through (PT) devices (15 kV SiC IGBT) behave like non-punch through (NPT) devices. Series connection of HV SiC devices has been evaluated with external snubber for four separate independent cases: (i) series connection of two 15 kV SiC IGBTs (single die per module, 2µm buffer layer) devices; (ii) series connection of two 15 kV SiC IGBTs (two parallel dies per module, 5µm buffer layer) devices; (iii) Series connection of two 15 kV SiC MOSFET (two parallel dies per module); (iv) Series connection of two 10 kV SiC MOSFET (single die per module) devices. The series connection with small snubber will give a significant reduction in '*dv/dt*' and turn-off losses to enable high power density MV DC-DC transformers or DC-DC soft switching converters with efficiencies > 98 %.

Enabling High Efficiency Medium Voltage Converter for High Speed Drives and Other Grid Applications using Low Voltage (LV) and High Voltage (HV) Silicon Carbide (SiC) Devices

by
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DEDICATION

To my parents Mr. Vechalapu Govinda and Mrs. Vechalapu Mutyalamma, and to my wife Jayasri Pudi and son Jayanshu Kasunaidu. Thank you all for your love.

BIOGRAPHY

Kasunaidu Vechalapu was born in India. He received his B.Tech in Electrical and Electronics Engineering from Jawaharlal Nehru Technological University, Hyderabad, India, in 2005, and the M.Tech. degree in Electrical Engineering from the Indian Institute of Technology, Kanpur, India, in 2007.

From 2008 to 2010, he was with Emerson Network Power Ltd, Mumbai, India, as a Design Engineer in research and development department working on design development of Industrial UPS systems. From 2010 to 2013, he was with ABB Global Industries and Services Ltd, Chennai, India, as an Associate Scientist in Grid system research and development working on HVDC converters and DC grid system.

In Aug, 2013, he joined the Department of Electrical and Computer Engineering at North Carolina State University, Raleigh, North Carolina as a Ph.D. Student. His research interests include Silicon carbide (SiC) devices based Medium Voltage (MV) and High Voltage (HV) power conversion, MVDC and HVDC applications and Solid-State Transformers.

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Chapter 1 Introduction

1.1 Motivation

There are two technology gaps to be addressed for medium voltage (MV) or high voltage (HV) applications. First is "high power density MV converters for high-speed motor drives applications" (as in Fig. 1-1). Second is "efficient MV DC-DC transformers for MVDC to HVDC grid applications" (as in Fig. 1-2).

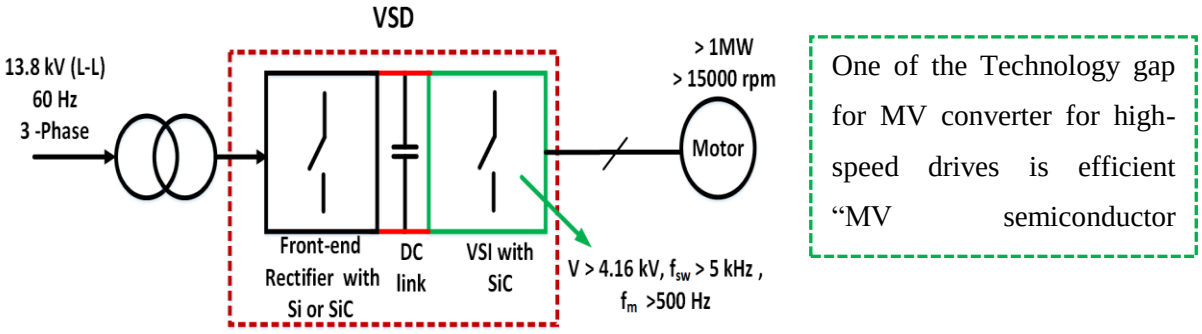


Fig. 1-1: Minimum system requirements for VSD for high-speed applications [1]

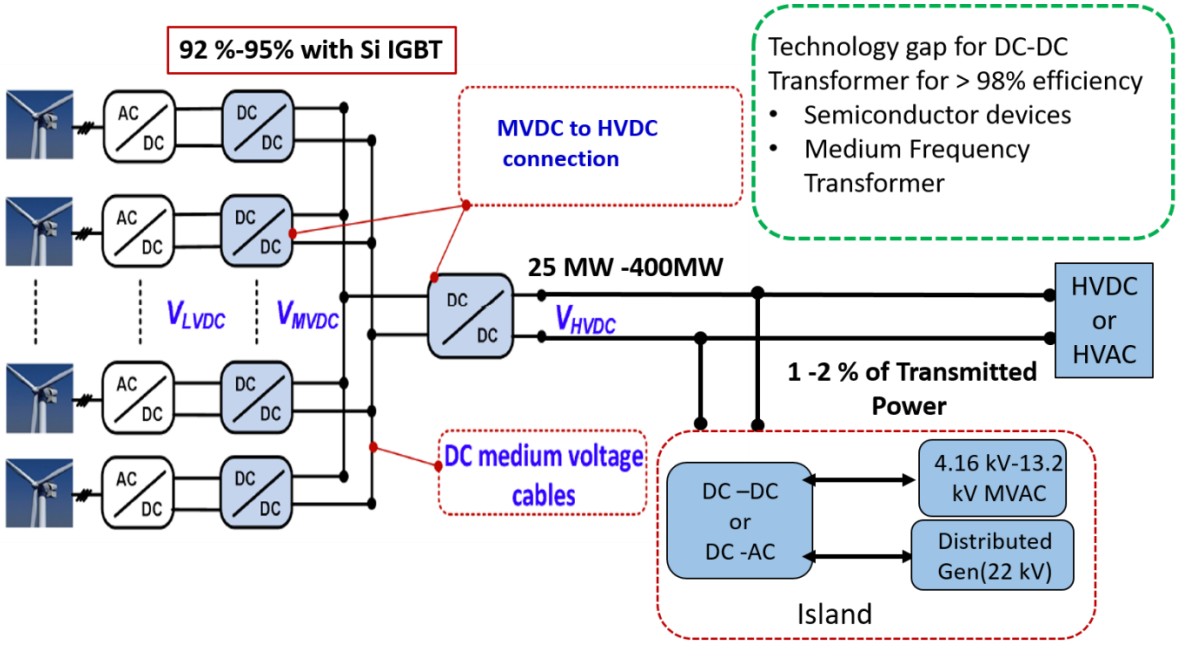


Fig. 1-2: DC-DC transformer application in Wind and Other grid-connected applications

With reference to technology development for high-speed MV drives applications, the U.S Department of Energy (DOE) estimated that the electric motor drive system consumes nearly 68% of total electricity for essential energy handling and material processing and HVAC systems [1]. The motor running at fixed speed or without variable speed drive (VSD) can potentially waste 30% to 80% of energy in mechanical throttles. Therefore, the forecasted energy savings by the deployment of variable speed drive (VSD) for MV motors saves significant energy based on the size of the motor, in applications such as chemical & petroleum refining industries, natural gas infrastructure and general industrial applications as shown in Table 1-1.

Table 1-1: Potential energy savings from VSD [1]

Motor Size	Potential Energy Savings (% of U.S. end-use electricity load)
U.S. industrial motor system (>500 HP, all applications)	1.2% to 3.2 %
U.S. industrial motor system (>1000 HP, all applications)	0.7% to 1.8 %

The power and speed range for some of the selected applications are as shown in Table 1-2 [2]. The majority of all motors with a rating greater than 500 H.P are medium voltage (> 2 kV) class and will require MV drives for operation. However, there is the low adoption of VSD in the medium voltage motors using 4.5 kV to 6.5 kV Si IGBT due to low switching frequency (f_{sw} < 1 kHz), high losses, requirement of gearbox to increase the speed and large footprint of VSD system. The high switching frequencies are required to generate high fundamental frequency (f_m) AC voltages at the motor input and hence achieving high speed at the motor output because the speed of the motor is proportional to 'f_m'.

Table 1-2: Power – Speed range for selected applications [2]

Application	Power	Speed
Oil and Gas	3 MW to 15 MW	5000-15000 rpm
Air Compressor	40 kW to 500 kW	15000-80000 rpm
Microturbine	30 kW to 400 kW	15000-120000 rpm

The converters for MV drives are either two or three level using 4.5 kV-6.5 kV Si IGBT or complex cascaded multilevel converters using low voltage (1.2 -1.7 kV) Si IGBT. The 4.5 kV to 6.5 kV Si IGBTs are highly inefficient if switched above 1 kHz. The cascaded multilevel converter using low voltage Si IGBT can be switched at high switching frequencies (10 kHz) but are complex to implement and low power density due to larger cables size required for low voltage high current operation from each of the building block[3][4].

Therefore, the DOE, academic institutions, and other corporate research centers are focusing on developing the MV power converters for next-generation high-speed drives using Wide Band Gap (WBG) devices such as Silicon Carbide (SiC) devices. The minimum specifications of MV VSD using WBG devices are shown in Fig. 1-1.

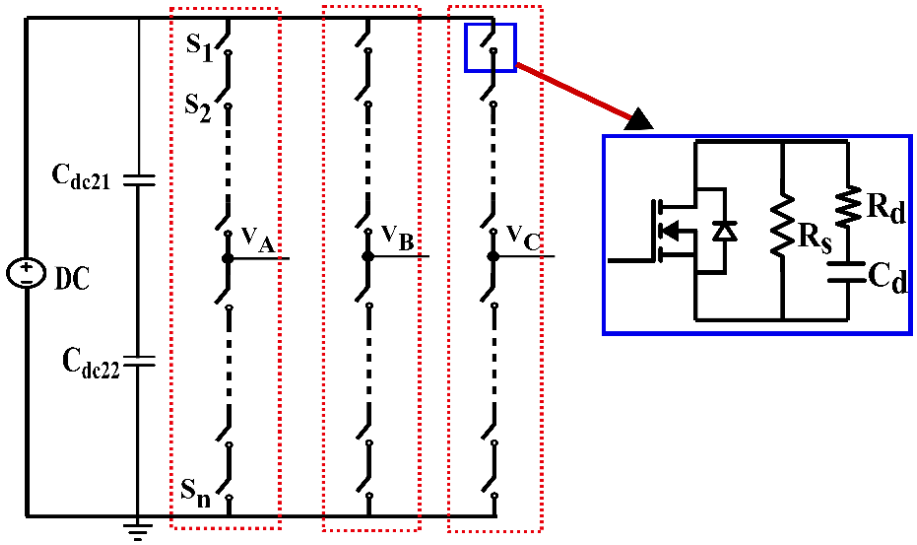


Fig. 1-3: Three phase legs of a two-level converter using the series connection of 'n' 1.7 kV SiC MOSFET devices for MV (>2.0 kV) high- speed drive applications

To realize the MV VSD, the SiC devices are available for both low voltage (1.2-1.7 kV) and medium voltage (10 -15 kV) [5][6][7]. These devices can be switched at higher switching frequencies and lower losses compared to Si IGBT. The medium voltage SiC devices (> 10 kV) are not commercially available for medium voltage high power applications, but available only in research laboratories. It has been reported in [7] about the use of 10 kV SiC MOSFET modules for MV high-speed drive applications with high switching (f_{sw} = 10-20 kHz) and fundamental frequencies (300-1000 Hz). However, the output power from 3-ph converter using 10kV SiC MOSFET modules has been limited to 10-20 kW. It is due to low current rating (10A-15A) of 10 kV SiC MOSFET. Also, the design and operation of the converter using 10 kV SiC MOSFET is more challenging due to high 'dv/dt.' Therefore, the converter operation has been limited from 6 kV to 3 kV dc bus at higher switching frequencies [8]. Recently, Wolf Speed Inc. has developed high current (240 A), 10 kV SiC MOSFET module [9] and they may replace Si-IGBT (4.5 kV, 6.5 kV) in the coming years. However, even if the SiC devices of greater than 10 kV are unavailable due to cost or any other reasons, the LV SiC devices can be used to realize the MV converter. The LV SiC devices are already proven for their robustness and reliability over the recent years. These are available commercially with high current

capability modules. However, to enable MV converter with simple two-level topology, a series connection of LV SiC devices is required (as in Fig. 1-3).

Therefore, one of the focus in this thesis is converter design considerations for series connection of 1.7 kV SiC MOSFETs using RC snubber to enable MV converter for high-speed drive applications.

When coming to MV DC-DC transformer, its significant importance has been increased in the recent years for the state of the art medium voltage DC grid (MVDC grid as shown in Fig. 1-4), with increased penetration of distributed generations such as offshore Wind farms, solar farms and efficient power transmission of DC system over the AC system. The typical application of MV DC-DC transformer is shown in Fig. 1-2, Fig. 1-4 and Fig. 1-5. Reference [10] analyzed different configurations of Wind farm based MVDC grids and different configurations of interfacing converter topologies (AC-DC, DC-DC, DC-AC) to interconnect wind farm to MVDC collection point. The capacity of the Wind farms is 25 MW to 400 MW. Typical AC output voltage of 2 MW to 3 MW Wind turbines are 690 V to 1000 V (Vestas 3 MW 90V turbine generates 1000 V [10]). High power wind turbines such as the M5000 [11], propose a generator voltage of 3.3 kV (5 MW). If the transformation ratio is high enough so that the turbine output voltage reaches 20-40 kV, only a single transformation is used to elevate the voltage to the transmission level of 70 kV-150 kV. If the turbine output voltage after the AC-DC stage is below 5 kV, an additional DC/DC transformer is needed [12]. One typical topology with two transformation steps (MV DC-DC transformer) is shown in Fig. 1-5.

However, the efficiency of MW scale DC-DC converters at medium voltage (MV) transmission/ distribution level with Silicon-based power semiconductor devices is less than conventional AC distribution transformer. The typical efficiency of line frequency (50Hz-60Hz) AC distribution transformer is greater 98%. The efficiency of 5 **MW to 15 MW** DC-DC transformer with different converter topologies using Si IGBT is **92% to 95% [13]**. The frequency of DC-DC transformer is **500 Hz to 1800 Hz** [13]. The efficiency of Wind farm will become poor with an increased number of power conversion stages from Wind turbine output to MVDC collection point. The total losses of AC to DC and DC-DC converter for 40 kV MVDC grid is very high and it is reported to be around **6.5%** [13] The switching frequency of these converters with Si IGBT or Thyristor are reported to be as low as **300 Hz to 1500 Hz** [14]**,** therefore very little impact on converter power density.

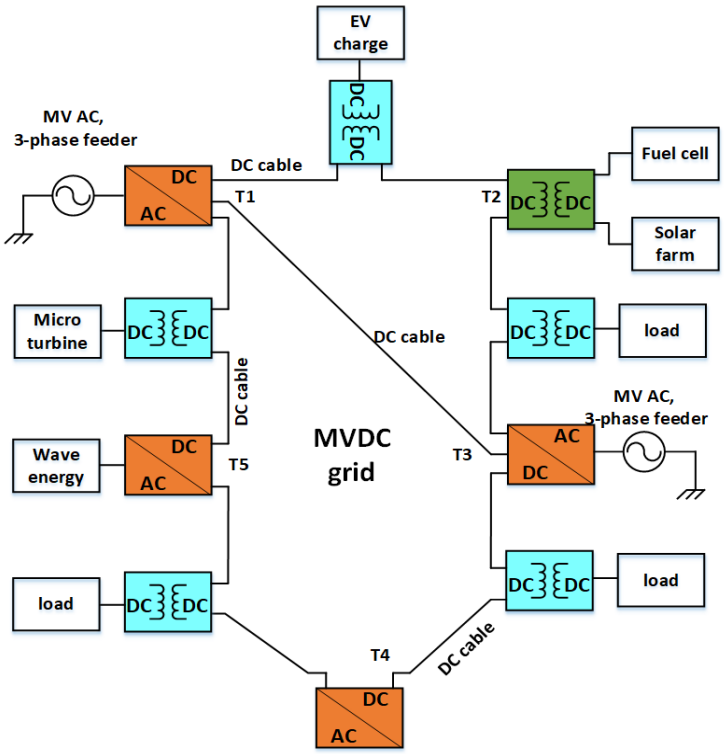


Fig. 1-4: DC-DC transformers applications in MV DC grid

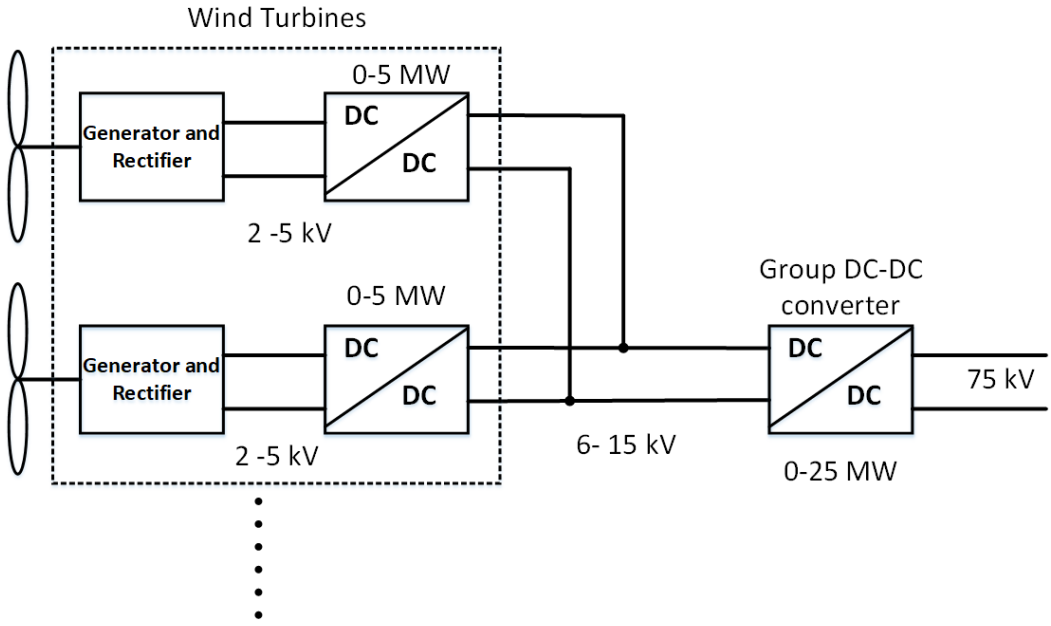


Fig. 1-5: DC-DC Transformer application in MW scale Wind farm with typical input-output voltages [12]

One of the typical DC-DC transformers is shown in Fig. 1-6 and Fig. 1-7. It has three sections: (i) HV side converter; (ii) LV side converter; (iii) high frequency isolation transformer. To increase the power density of isolation transformer, the switching frequency has to be high (>10 kHz). However, unlike low voltage transformers, the size of MV transformer does not decrease with increase in operating frequency. The size of the MV transformer is also a function of insulating material volume. The study shows that the optimal frequency for a high power density of medium frequency transformer (MFT) for MV/HV applications is 4 - 6 kHz, for the 33 kV / 1 kV system, 666 kW as shown in Fig. 1-8[15][16].

Therefore, to realize the DC-DC transformer for MV/HV applications, we do not require semiconductor devices with very high switching frequencies (20 kHz-100 kHz) but require with medium switching frequencies of up to 4- 10 kHz only for both HV side and LV side of the DC-DC transformer. The 4.5-6.5 kV Si- IGBT devices cannot be used on HV side as their switching frequencies are limited to less than 1 kHz. However, LV Si IGBT (1.2-1.7 kV) can be used on the LV side, as their switching frequencies are up to 10 kHz. Therefore, the MV or HV SiC devices such as 10-15 kV can be used on the HV side, and LV side converter could be either with LV Si IGBT or with LV SiC MOSFET. The overall DC-DC transformer for MV/HV application using the basic building blocks is shown in Fig. 1-6. The three configurations of basic building blocks of a DC-DC transformer with Si and SiC devices are shown Fig. 1-7.

Therefore, the second focus of this thesis is to enable DC-DC transformer for MV/HV application by performing (1) the HV SiC devices (10 kV -15 kV) characterization (soft switching and hard switching). (2) The series connection of HV SiC devices (for soft switching applications); (3) Estimating their switching frequency limits, converter design considerations using these devices, evaluation of losses on HV side using these devices and also the efficiency of the DC-DC transformer (for both HV side and LV side). (4) The comparison of HV SiC devices (10-15kV SiC) and a series connection of 1.7kV SiC MOSFET devices and Si –IGBT devices (4.5-6.5 kV) to choose a suitable device for MV converter application.

Based on the previous given reflections and arguments, the objectives of this dissertation are:
(1) Enable High power density medium voltage (MV) converters for high-speed drives using SiC devices (LV and HV)

(2) Enable efficient DC-DC converters (Isolated soft switching) for MV/HV DC grids and Windfarms (HVDC- MVDC) using SiC devices (LV and HV) and Si IGBT (LV).

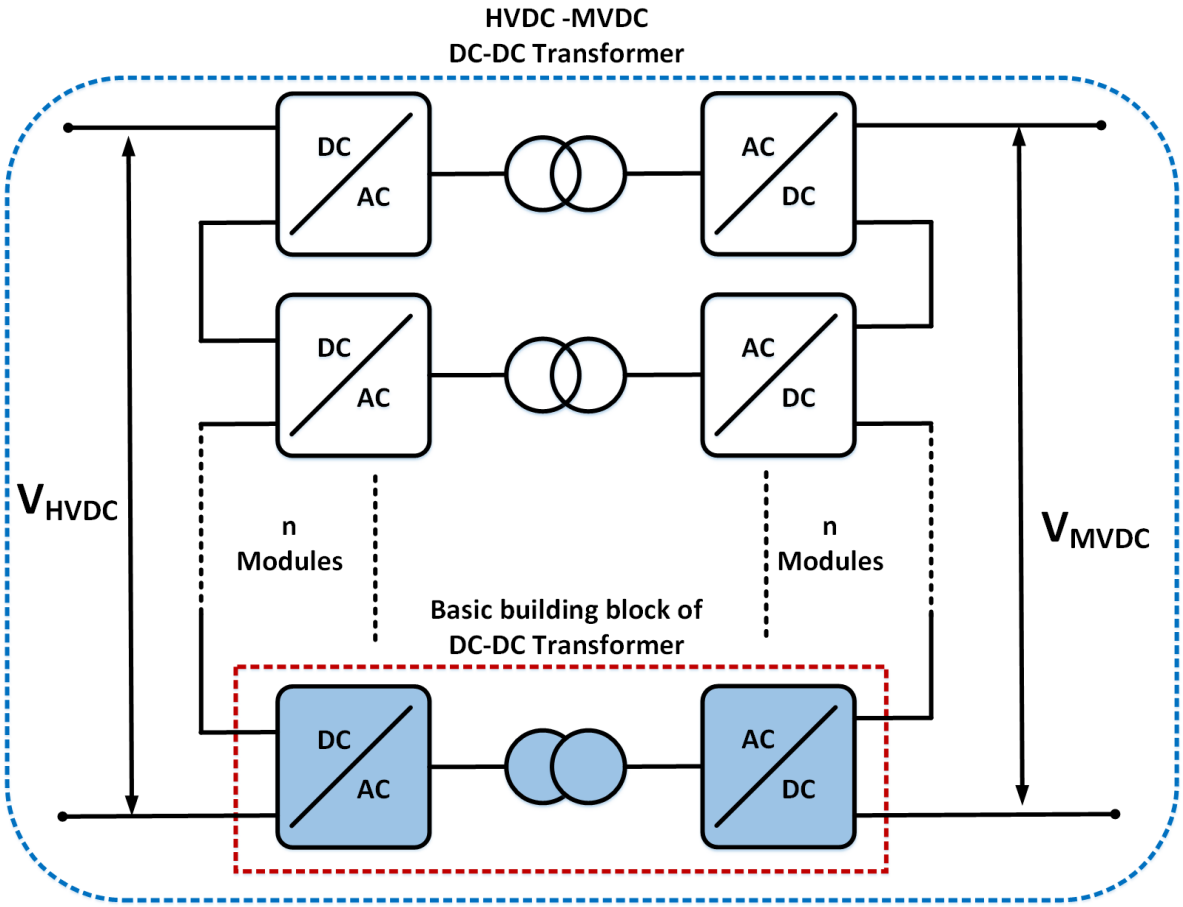


Fig. 1-6: DC-DC transformer for MV/HV application using the basic building blocks

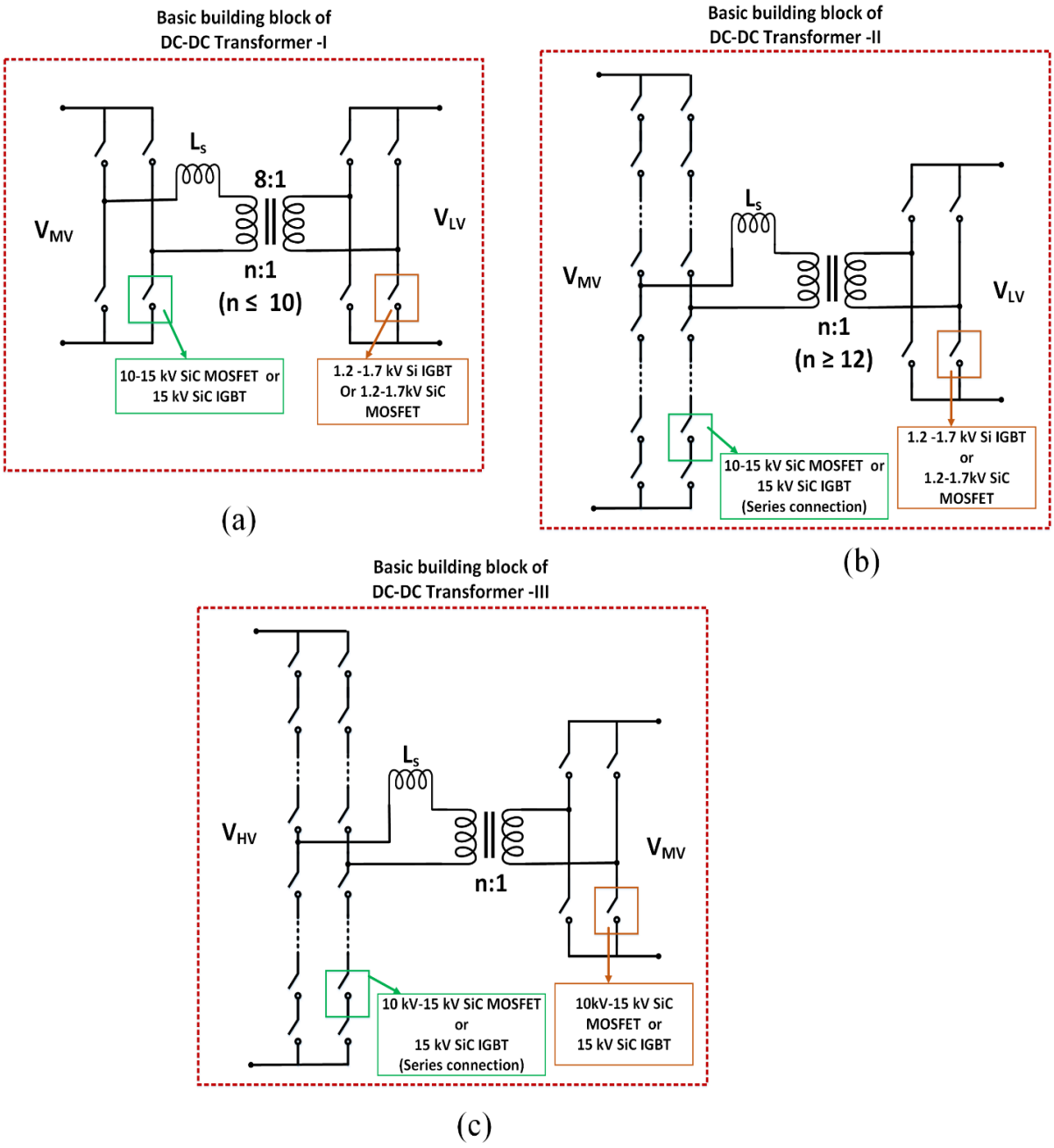


Fig. 1-7: Three configurations of Basic building blocks of DC-DC transformer

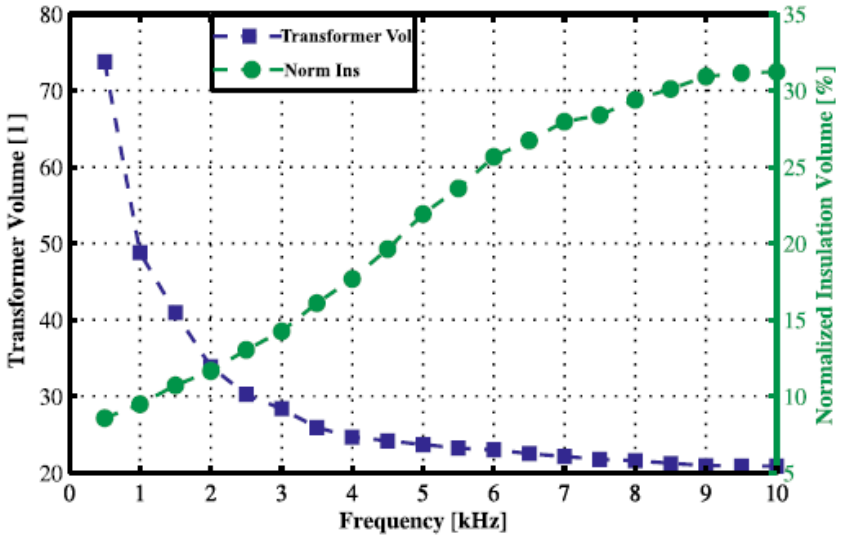


Fig. 1-8: Variation of MV/HV isolation transformer size with switching frequency [15][16]

1.2 Outline of this Dissertation

Section 1.1 outlines the motivation of the dissertation and list of basic converter topologies to enable MV high-speed drives and DC-DC transformer for MV - MW scale applications using low voltage and high voltage SiC devices (1.2 kV to 1.7 kV low voltage SiC devices, and 10 kV to 15 kV high voltage SiC devices).

Chapter 2 explains in detail the design considerations of series connected low voltage SiC devices (1.7 kV SiC MOSFET) to enable medium voltage high power application.

Chapter 3 explains the detailed switching characterization of 15 kV SiC MOSFET and 15 kV SiC IGBT. It covers two different switching characterization double pulse test (DPT) circuit setups and how these DPT test circuits will influence the switching loss characterization. It also covers demonstration of 15 kV SiC MOSFET in dc-dc boost converter at a full working voltage (10 kV DC output) in continuous switching mode and verification of total losses from heat run test and switching characterization. It also introduces the switching loss comparison of 15 kV SiC MOSFET and 15 kV SiC IGBT under same *dv/dt* conditions and comparison of total losses. Finally, switching frequency limits of these 15 kV SiC devices and efficiency of different DC-DC converters (hard switching) and DC-AC inverter (hard switching) using these devices is presented.

Chapter 4 compares the high voltage modules (10 kV to 15 kV SiC devices), and series connected 1.7 kV SiC MOSFETs.

Chapter 5 introduces soft switching and series characterization of HV SiC devices (10-15 kV) to enable DC-DC transformer for MV/HV applications and presents the efficiency of the DC-DC transformer for high power applications.

Chapter 6 presents the conclusions and future work.

Chapter 2 Series Connected Low Voltage SiC devices (1.7 kV SiC MOSFETs) to Enable Medium Voltage High-Speed Drives and Other Grid-Connected Applications

2.1 Introduction

The medium voltage (MV) high-speed drives are required for traction, wind energy, marine, aerospace, oil, and gas compressors applications. The MV converter must be able to switch at higher switching frequencies (> 5 kHz) to generate higher fundamental frequency AC input voltages for the motor (≥ 500 Hz) and thereby achieving high speed at the motor output (≥ 15000 rpm). To develop the VSD as in Fig. 1-1, the high-voltage and high-current SiC devices are not commercially available. Therefore, to meet the immediate need of MV or HV converter applications and to explore the capability of the low voltage SiC devices for medium or high voltage applications, the series connection of 1.7 kV/225 A SiC MOSFET modules has been investigated in this chapter.

In order to reach this objective, it is worth noting that the series connection of multiple devices has the following design challenges that must be addressed: (1) unequal dynamic voltage sharing due to a mismatch in device capacitances, wide-spread in turn-off delay time due to external gate drive signals and mismatch in device turn-off delays. (2) Unequal static voltage sharing of series connected devices due to widespread in device leakage currents among different devices (of identical nominal voltage and current ratings). (3) For a series connection of a high number of devices, the connected bus bars between devices contribute to additional loop inductance (L_s). This increases the device voltage de-rating due to '$L_s \cdot di/dt$' seen by each device during turn-off [17].

Reference [18] demonstrates that the series connected low voltage SiC devices (1.2 kV SiC MOSFET) have high current handling capability, better conduction losses and breakdown voltage compared to a single high voltage device, but it doesn't report any optimization of the RC snubber design for series connection. The feasibility of 3.6 kV/80 A and 10 kV/200 A power module with series and parallel connection of low voltage SiC MOSFET 1200 V/40 A has been reported in [19][20]. It uses a single gate driver unit to turn-on and turn-off the devices in series, which results in an undesired sequential turn-on/off process. During turn-on/turn-off, the closest device from the gate driver unit in the series connection, commutates first and the furthest one will commutate last. Therefore, the switching loss distribution in the devices will be unequal. This switching delay will increase the effective dead band requirement and hence reduces the switching frequency capability. Though they use speeding capacitors in the gate driver to decrease the switching delays between the

devices, it does not improve the turn-off process compared to turn-on. In [19], from the experimental switching characterization, it is clear that the current measurement does not correspond to the actual device current. Hence, true decrease in turn-off losses due to snubber cannot be captured and the total savings in switching losses and heat sink size reduction cannot be evaluated. Therefore it is may not be an effective method for converter development and real-time applications.

Dynamic voltage balancing of the series connection of Si semiconductor devices has been done using various methods, such as (i) Passive RC or RCD snubber [21]-[26]; (ii) Active clamping and Active gate drivers [27]-[29]. Active gate driver method is more complex to implement, and it will be even more challenging for closed-loop control of the fast switching SiC devices for dynamic voltage balancing. In this work, a RC snubber method has been used to evaluate the series connection of LV 1.7 kV SiC MOSFETs to enable MV converters (as in Fig. 1-3)). The static resistance (R_s) and RC snubber (R_dC_d) are selected to reduce the static and dynamic voltage imbalance across the devices and hence to avoid the matching of the devices in the converter design and fabrication.

This chapter is organized as follows: Section 2.2 presents the static characterization and selection of static balancing resistance (R_s). Section 2.3 presents selection procedure of optimum RC snubber (R_dC_d) for series connection of devices. Section 2.4 presents a dynamic characterization of series connected 1.7 kV SiC MOSFET devices. Section 2.5 presents the switching losses per device (E_{sw}) with RC snubber in series connection. Section 2.6 presents the computation of snubber resistor losses (E_{Rd}). Section 2.7 presents an experimental demonstration of series connected devices in different converter configurations. Section 2.8 presents the efficiency of 3-ph MV VSD for different AC voltage (2.1 kV -13.2 kV), Section 2.9 presents the performance comparison of Si –IGBT and series connected 1.7 kV SiC MOSFET devices. Section 2.10 concludes this chapter.

2.2 Static Characterization and Selection of Static Balancing Resistance (R_s)

1.7 kV SiC half-bridge modules device leakage tests are done using Tektronix 370A curve tracer at 1000V and 1200V reverse bias voltages at different junction temperatures (25^0C to 150^0C) for a handful of devices (eight half-bridge modules /sixteen MOSFET devices).

Table 2-1 and Table 2-2 show the characterized device leakage current $\left(I_{ds,\ leakage}\right)$ at 1000V and 1200V respectively. At 1000V, the maximum spread in leakage currents $\left(\Delta I_{ds,leakge}^{max}\right)$ within the module is **9 to 10 μ A** (approx.) and maximum spread in leakage currents between the half bridge -

Table 2-1: Device leakage data at 1000 V

		Leakage current (µA) at 1000 V		
Module no		T=25 ^{0}C	T=125^{0}C	T=150^{0}C
1	Top MOSFET	17	18.5	19.5
	Bottom MOSFET	21.2	25	28
3	Top MOSFET	18.6	20	22
	Bottom MOSFET	21	23.5	28.5
4	Top MOSFET	29.3	32	33.5
	Bottom MOSFET	17	21	24.5
5	Top MOSFET	20.5	22	23.5
	Bottom MOSFET	18.3	22.8	25.5
6	Top MOSFET	36	38.5	40
	Bottom MOSFET	26.2	29.5	32
7	Top MOSFET	18.2	24.5	30
	Bottom MOSFET	17.9	26.5	34
8	Top MOSFET	18.2	20.2	23
	Bottom MOSFET	65.6	127.6	138

Table 2-2: Device leakage data at 1200 V

		Leakage current (µA) at 1200 V		
Module no		T=25 ^{0}C	T=125^{0}C	T=150^{0}C
1	Top MOSFET	24	31.6	35.1
	Bottom MOSFET	33.6	44.4	51.7
3	Top MOSFET	24.8	29	35
	Bottom MOSFET	31.9	40.7	51.7
4	Top MOSFET	42.7	52.6	58.7
	Bottom MOSFET	25.8	38.2	46.3
5	Top MOSFET	27.2	32.5	35
	Bottom MOSFET	28.6	39.8	47.3
6	Top MOSFET	51.4	59.6	66.6
	Bottom MOSFET	38.5	47.8	55.8
7	Top MOSFET	25.6	38.9	49.8
	Bottom MOSFET	24.5	41.7	54.5
8	Top MOSFET	26	32.5	42.2
	Bottom MOSFET	77.9	127.6	162.6

-modules is **20 μ A** (approx.). At 1200V, the maximum spread in leakage currents within the module is **12 μA** (approx.) and maximum spread in leakage currents between the half bridge modules is

30 μ A (approx.). Most of the leakage current values are spread around the average leakage current $\left(I_{ds,leakge}^{avg}\right)$ value of nearly 36 µA, as shown in Fig. 2-1. The static voltage balancing resistor can be designed using (2-1) for a known value of device leakage current and maximum spread in device leakage current. **Static voltage balancing resistor of 0.5 MΩ to 1 MΩ used to limit voltage unbalance within 10%-12% of device nominal operating voltage.**

$$R_s \le \frac{1}{10}\left(\frac{V_{ds}}{\left(I_{ds,leakge}^{avg} + \Delta I_{ds,\ leakage}^{max}\right)}\right) \qquad (2\text{-}1)$$

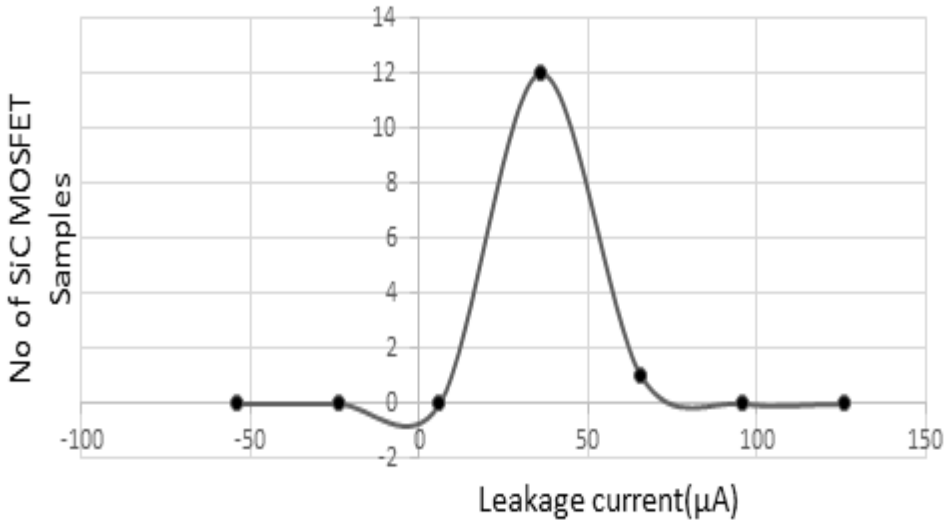
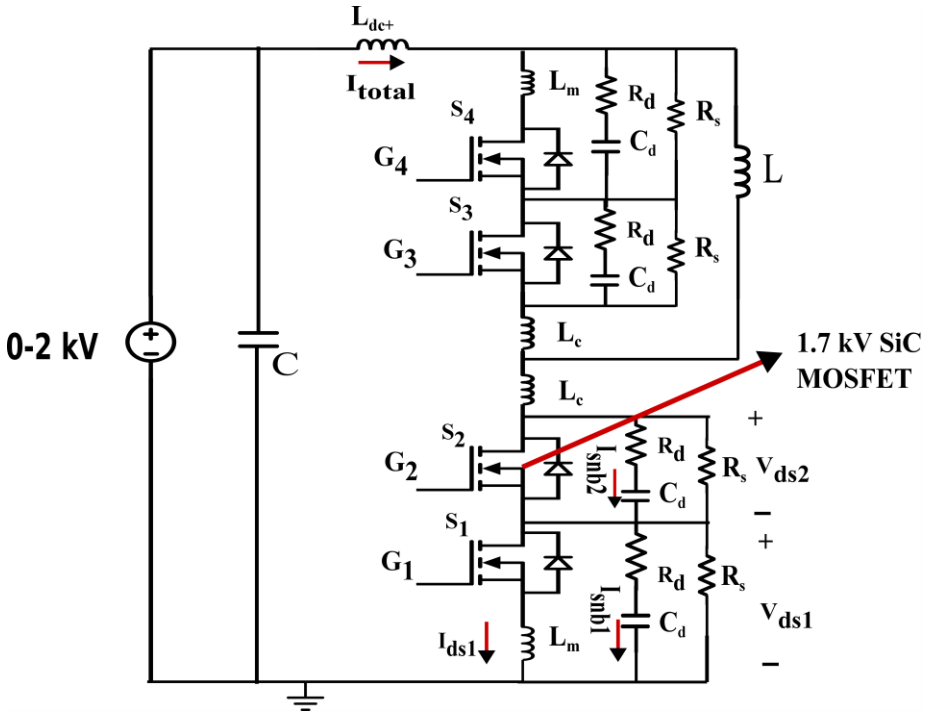
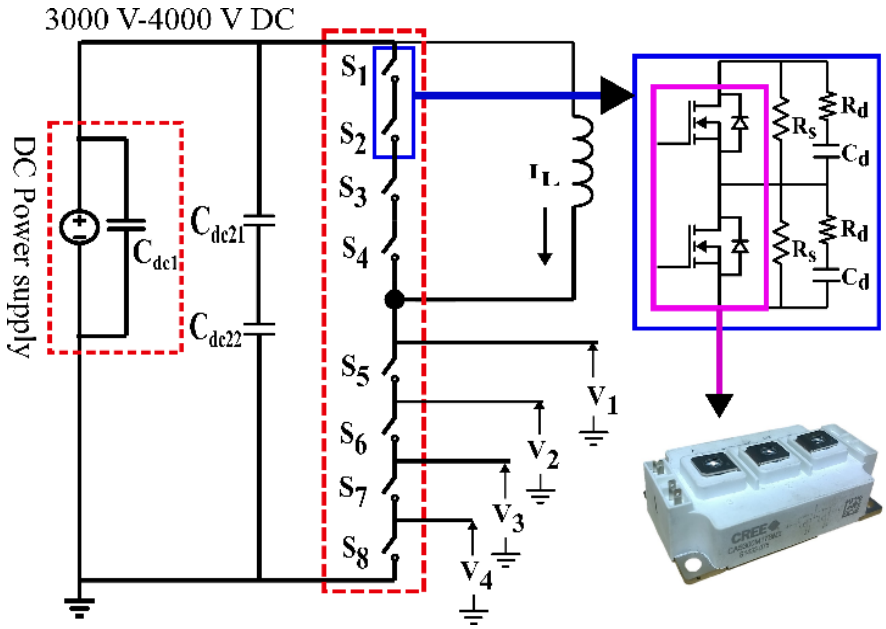


Fig. 2-1: Spread of leakage current from fourteen SiC MOSFET samples

Fig. 2-2: Inductive clamped circuit (a) two series connected 1.7 kV SiC MOSFETs per arm of a phase leg; (b) four series connected 1.7 kV SiC MOSFETs per arm of a phase leg



(a)



(b)

The inductive clamped circuit is shown in Fig. 2-2 (b) has been used for static characterization of four series connected 1.7 kV SiC MOSFET devices. The device gate to source voltages are kept at nearly

-5V, and the DC bus has been increased to 2800V. Fig. 2-3 shows the static voltage across the devices (S_5 to S_8) with respect ground, and the difference in the imbalance between the devices is less than 10% of base rated operating voltage - (i.e.,.V_{dc}/n=2800/4=700V).

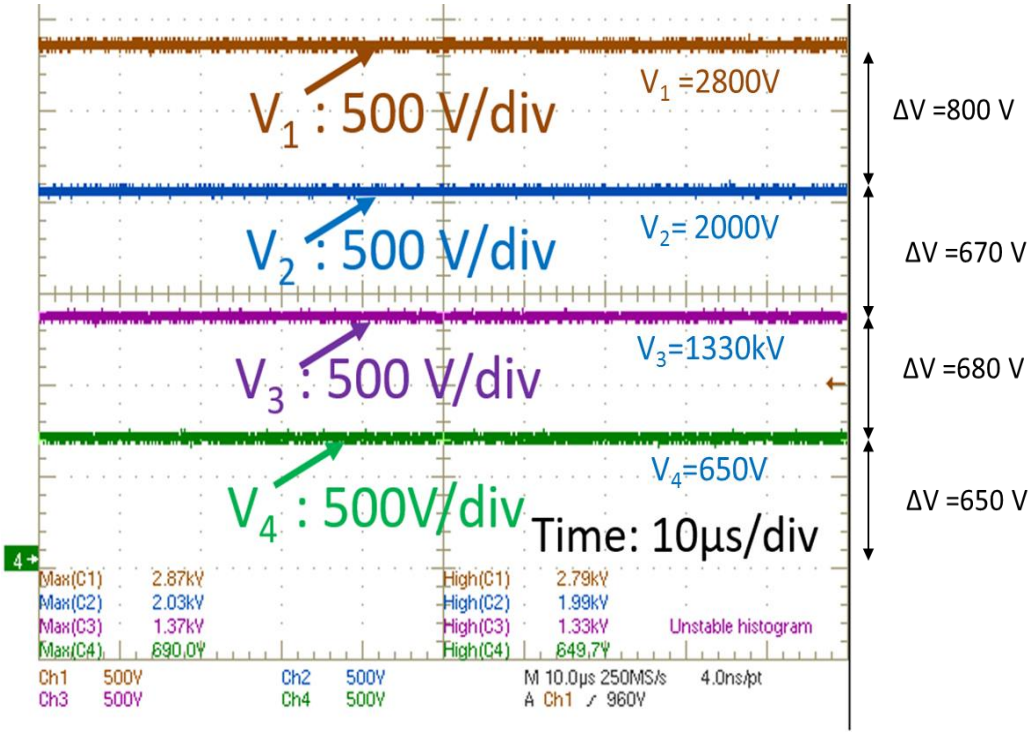


Fig. 2-3: Balanced static voltage of four SiC MOSFET devices in a phase-leg arm (eight devices per phase-leg)

2.3 Selection Procedure of optimum RC snubber (R_dC_d) for series connection of devices

The RC snubber method has been used for series connection of devices. The value of the snubber capacitor (C_d) , snubber resistor (R_d) have been selected such that (i) it limits the dynamic voltage imbalance between the devices within 10-12% of device nominal operating voltage, (ii) it limits the voltage peak overshoot across each device within 10-12% of device nominal operating voltage; (iii) it should be optimal value to reduces the total switching losses; (iv) it should not exceed the peak current into the device more than its repetitive current rating; (v) its discharging time constant ($4R_dC_d$) should be less than device on-state time. Therefore, the optimum value of R_dC_d snubber is the minimum value of R_dC_d snubber given by constraints (2-1).

$$R_d C_d \Big|_{min} = \text{minimize} \left\{ \begin{array}{l} \text{Difference in the dynamic voltage sharing ,} \\ \text{Voltage peakovershoot across the device, and} \\ \text{Total Switching losses in the device at the same time} \end{array} \right\} \quad (2\text{-}1)$$

The snubber capacitor (C_d) contributes to the following four functions: (1) it reduces the unbalance in dynamic voltage sharing between the devices and the rate of rise of voltage across the series connected devices (V_{ds}) (during turn-off, V_{ds} will be nearly equal between the devices, because the snubber capacitor(C_d) is much larger than the device's output capacitance (C_{oss})); (2) it reduces the overall turn-off '*dv/dt*'at AC pole voltage point; (3) it makes the turn-off process in the devices near or partially zero-voltage switching and hence reduces the turn-off losses in the devices; (4) it contributes additional losses during turn-on, because the energy stored in the snubber capacitor during turn-off will be discharged in the series resistor and the device. Hence the total switching losses in the device may increase. Therefore it is essential to find the optimal snubber capacitor value. The flowchart for the selection of the optimal value of R_dC_d for series connection of devices is given in Fig. 2-4. The selection of minimum values of R_dC_d snubber will be carried out mostly by the experimental characterized data from Section 2.4-2.6, using the procedure mentioned in the flowchart shown in Fig. 2-4.

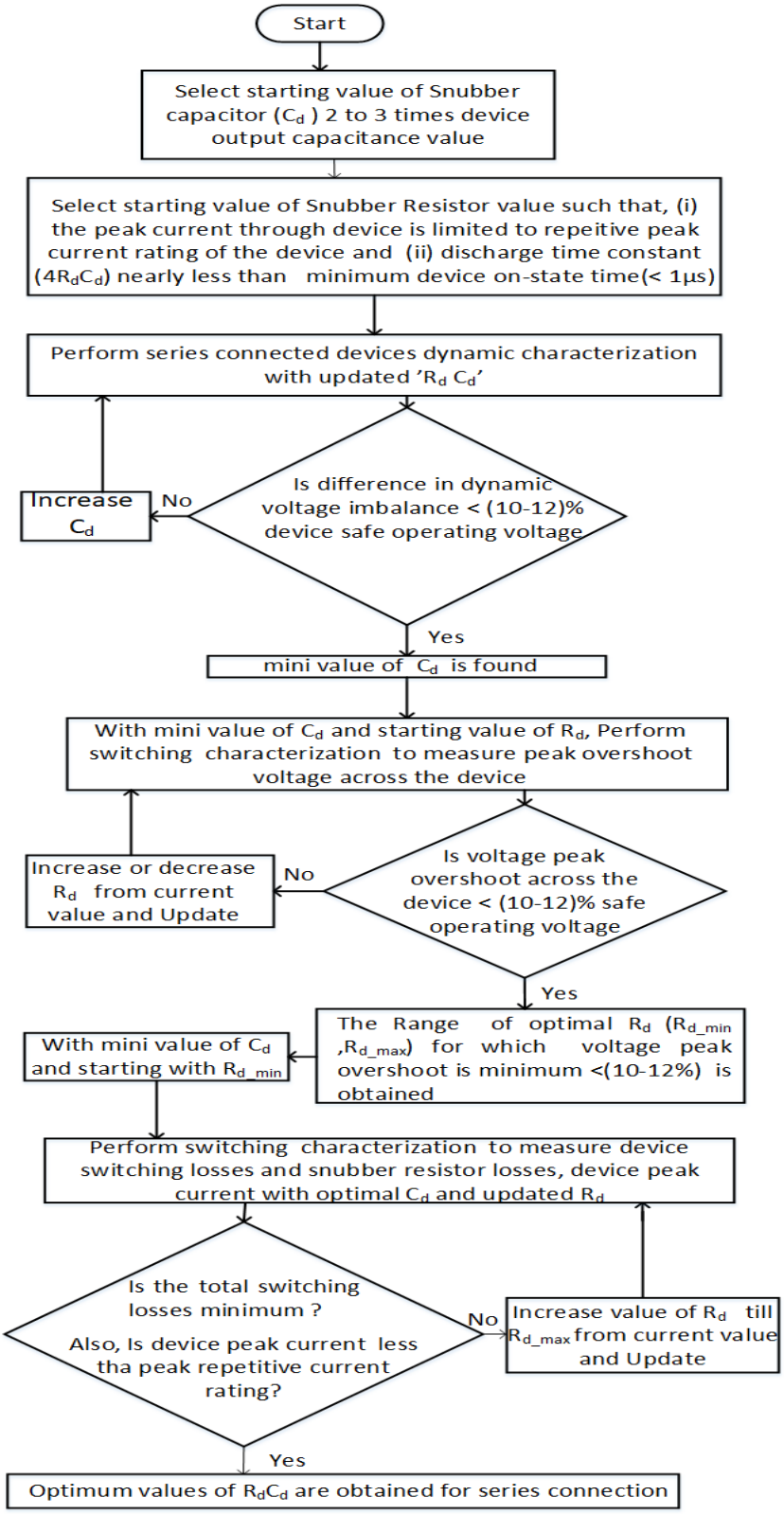


Fig. 2-4: Flowchart for the selection procedure of optimal snubber values for series connection of SiC MOSFET devices

2.4 Dynamic Characterization of Series Connected 1.7 kV SiC MOSFET devices

This section presents the dynamic characterization of series connected 1.7 kV SiC MOSFET devices with (1) two devices per arm (as in Fig. 2-2(a)) (2) four devices per arm (as in Fig. 2-2(b)).

2.4.1 Dynamic Characterization with Two Series Connected 1.7 kV SiC MOSFET devices

Fig. 2-2(a) shows the schematic circuit to verify the dynamic voltage sharing with two devices connected in series. Two half-bridge modules (Wolf Speed CAS300M17BM2 - 1.7 kV SiC MOSFET) are used for switches S_1 to S_4. The stray inductance of the semiconductor module is ~15 nH, and the contribution from bus bars from the DC capacitor to the module and module-to-module interconnection is approximately around 65 nH to 75 nH. Therefore, the effective loop inductance seen per switch position is around 40 nH to 45 nH in the dynamic characterization experiments with two series connected 1.7 kV SiC MOSFET devices.

Fig. 2-5 shows the difference in peak voltage overshoot and the dynamic voltage difference between two series connected devices without snubber during turn-off at 1 kV DC bus voltage and 200 A switching current. The difference in the peak overs shoot (ΔVp-p) is 292 V (30 %), and the dynamic voltage difference (ΔV) is 180 V (20 %). For the safe operating voltage of 900 V, the difference in ΔVp-p and ΔV are nearly 30% and 20% respectively. Increasing the DC bus more than 1 kV without snubber will force the one of the device voltage to go more than safe operating voltage.

Fig. 2-6 shows the peak voltage overshoot difference (ΔV_{p-p}) and dynamic voltage difference (ΔV) between two series connected devices with snubber 33 nF, 4.7 Ω for DC bus voltage of 1.8 kV and switching current of 200 A. It is evident that the dynamic voltage sharing between two series connected devices has been improved significantly with an external snubber.

Table 2-3 shows a summary of difference in voltage sharing between the two devices for different snubber values at gate resistance of 5 Ω for different switching currents. It clear from the table that the **lower bound (minimum value) for snubber capacitor for the dynamic voltage to be less than 10-12% is 22 nF ($C_d \geq 22$nF).**

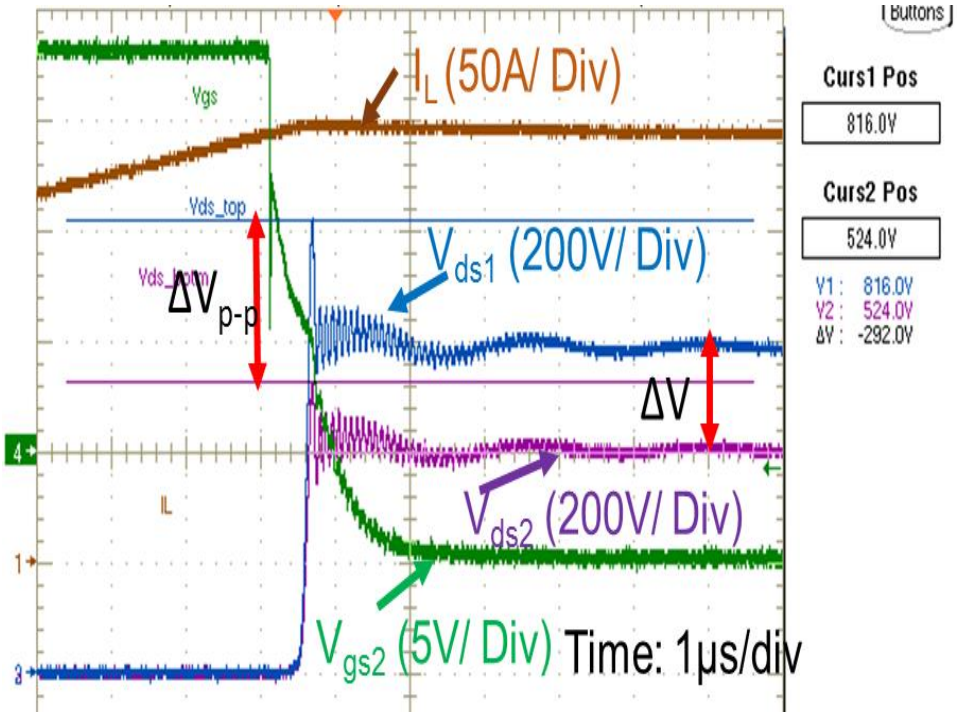


Fig. 2-5: Difference in peak voltage overshoot (ΔV_{p-p}=292 V) and the dynamic voltage difference (ΔV=180 V) between two devices without snubber at 1 kV DC bus voltage, 200 A switching current

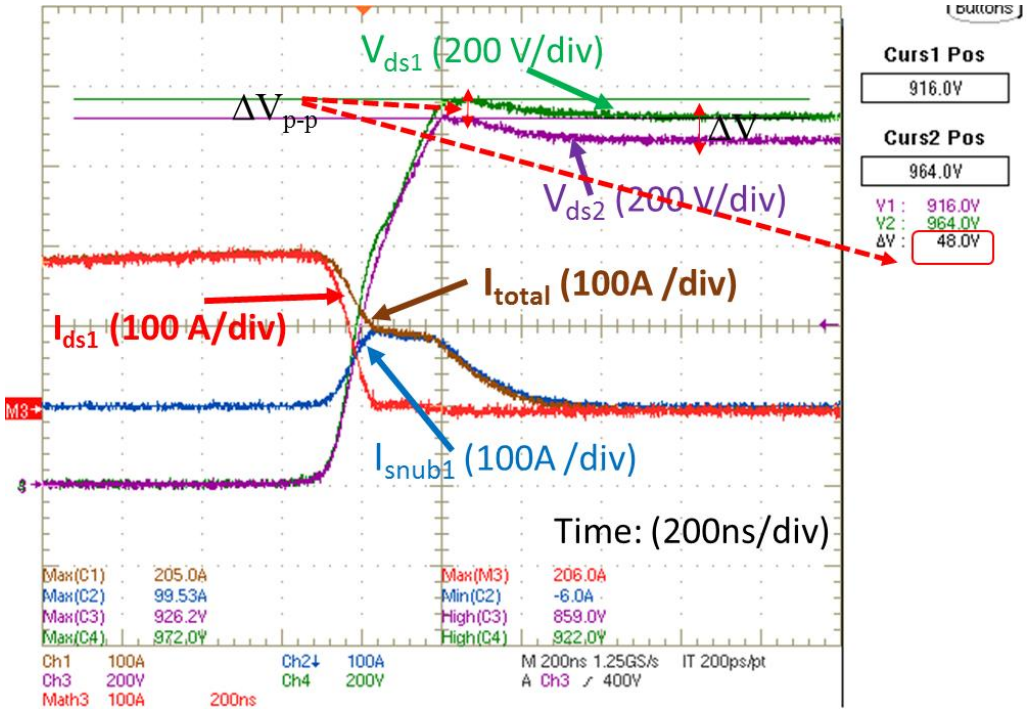


Fig. 2-6: Turn-off transition of two series connected 1.7 kV SiC MOSFETs and transient peak overshoot difference (ΔV_{p-p}=48 V) with R_dC_d =33 nF, 4.7 Ω at 1800 V DC bus, 200 A switching current, R_{goff}=4.7 Ω

The observed turn-off delay difference ($\Delta t_{d(off)}$) between the two devices is less than 10 ns during the dynamic characterization. The analytical expression for turn-off delay ($t_{d(off)}$) for the MOSFET is given by (2-2)[30]. Where C_{gs} : gate to source capacitance; C_{gd} : gate to drain capacitance; $V_{ds(ON)}$: on-state voltage drop; V_{gg} : Gate supply voltage; V_{th} : threshold voltage; I_L : Load current; g_m : Transconductance. Z: Width of MOSFET conduction channel; L: Length of MOSFET conduction channel; C_{ox}: gate oxide capacitance; μ_{ni}: mobility of inversion layer.

Table 2-3: Peak overshoot difference (ΔV_{p-p}) and dynamic voltage difference (ΔV) variation between two SiC MOSFETs with different snubber values

At 1800 V DC bus and $R_{gon} = R_{goff} = 5\ \Omega$						
	at 100 A switching			at 200 A switching		
Snubber values	ΔV_{p-p} (V)	ΔV (V)	%(ΔV_{p-p} or ΔV)	ΔV_{p-p} (V)	ΔV (V)	%(ΔV_{p-p} or ΔV)
10nF,4.7 Ω	125	96	13.88%, 10.66%	302	260	33.55%, 28.89%
22nF,4.7 Ω	48	48	5.33%, 5.33%	92	112	10.22%, 12.45%
33nF,4.7 Ω	32	36	3.55%, 4%	48	56	5.33%, 6.22%
68nF,4.7 Ω	Negligible					

$$t_{d(off)} = R_{goff}[C_{gs} + C_{gd}(V_{ds(ON)}]\ln\left[\frac{V_{gg}}{\left(\frac{I_L}{g_m} + V_{th}\right)}\right] \quad (2\text{-}2)$$

$$g_m = \frac{\mu_{ni} C_{ox} Z}{2L_{CH}}\left[V_{gg} - V_{th}\right]$$

The transconductance (g_m) is dependent on gate oxide thickness, which is process dependent and there could be small variations between the devices. The 'g_m' also dependent on the mobility of inversion layer (μ_{ni}) and threshold voltages. These three parameters will change with temperature, which may effect the 'g_m'. However, based on the 1.7 kV SiC MOSFET datasheet [31], the variation in the transconductance from 25^0C (g_m= 133) to 150^0C (g_m= 131) is very small. Therefore the increase in turn-off delay difference ($\Delta t_{d(off)}$) between the devices is neglected. However, assuming the worst case scenario that the $\Delta t_{d(off)}$ may increase between the devices due to aging in the converter operation with temperature and also the external gate driver delays change with aging and temperature. The increase in $\Delta t_{d(off)}$ will increase the dynamic voltage imbalance difference between the devices. To make the device and the converter more reliable, the selected snubber capacitor has

to keep the difference in dynamic voltage imbalance within 10-12% of safe operating voltage even with the increase in $\Delta t_{d(off)}$.

To emulate the difference in turn-off delays between the two devices and to select the optimal snubber capacitor, the dynamic voltage characterization has been performed with an intentional delay of 40 ns between the two devices. Fig. 2-7 shows the dynamic voltage difference with intentional gate signal delay of 40 ns at 1.8 kV DC bus and 100 A switching current. Table 2-4 shows a summary of dynamic voltage characterization with different snubber cases and with an intentional delay between two gate signals. Therefore, for dynamic voltage imbalance to be less than 100 V (10-12%) for turn-off delay spread of 40 ns, at 100 A switching, the lower bound for the optimal value of snubber capacitor - $C_d \geq 33$ nF. For switching current greater than 100 A and turn-off delay spread greater than 40 ns, the lower bound for snubber capacitor could be in the range of 33 nF < $C_d \leq 68$ nF. However, the turn-off delays for R_{goff}: 2.5 to 5 Ω are nearly 211 ns and 300 ns respectively. The spread in mismatch in turn-off delays ($\Delta t_{d(off)}$) can be assumed nearly 2 % - 5 % of turn-off delay (i.e, $\Delta t_{d(off)}$ = 5 ns -15 ns)[25]. Therefore, the difference in the dynamic voltage less than 10-12% can be achieved with 22 nF $\leq C_d \leq$33 nF for turn-off delay spread of 15 ns. With the endurance test (heat run test with continuous switching mode) of series connected devices in section 2.7, it has been verified that the increase in turn-off delay spread with temperature is negligible. It is observed that, with C_d = 33 nF, the dynamic voltage imbalance between two devices has been within 10-12% of rated operating voltage at 150 A peak current, the heat sink temperature near the module base plate is near 62^0C, and at the junction temperature is early 143^0C. This indicates the negligible increase in the turn-off delays spread between the 1.7 kV SiC MOSFET devices with an increase in junction temperature. Therefore, an optimal snubber capacitor value 22 nF to 33 nF can be used for the series connection of 1.7 kV SiC MOSFETs.

Table 2-4: Peak overshoot difference (ΔV_{p-p}) and dynamic voltage difference (ΔV) variation with intentional gate signal delay to emulate spread in device turn-off delays and gate driver delays

At 1800 V DC bus, 100 A switching current and at $R_{gon} = R_{goff} = 5\ \Omega$				
	Gate Signals Delay:40 ns			
Snubber values	ΔV_{p-p} (V)	ΔV (V)	% ΔV_{p-p}	% ΔV
(33nF,4.7 ohm)	80	92	9.77%	12.5%
(68nF,4.7 ohm)	56	36	6.22%	4.0%

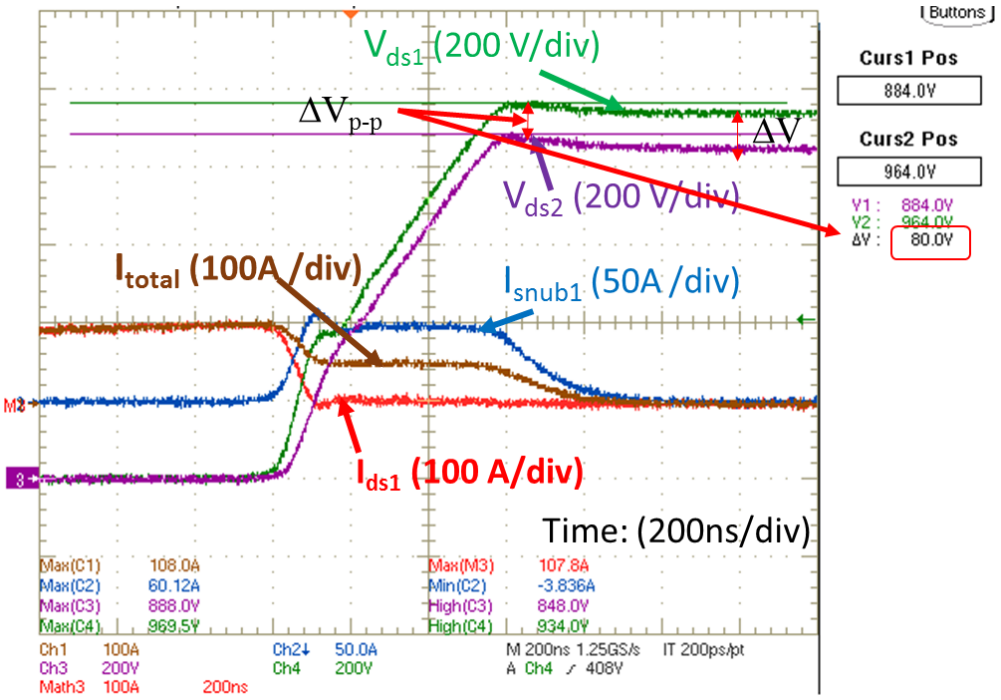
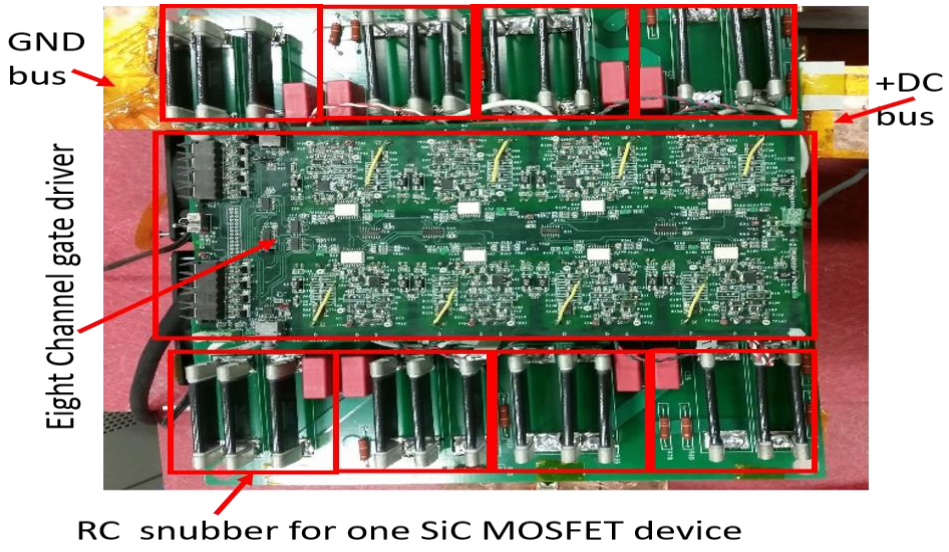


Fig. 2-7: Turn-off transition of two series connected 1.7 kV SiC MOSFETs and the dynamic voltage difference (ΔV_{p-p}=80 V) with Intentional gate signal delay of 40 ns with R_dC_d =33 nF, 4.7 Ω, at 1800V DC bus, 100 A switching current R_{goff}=4.7 Ω

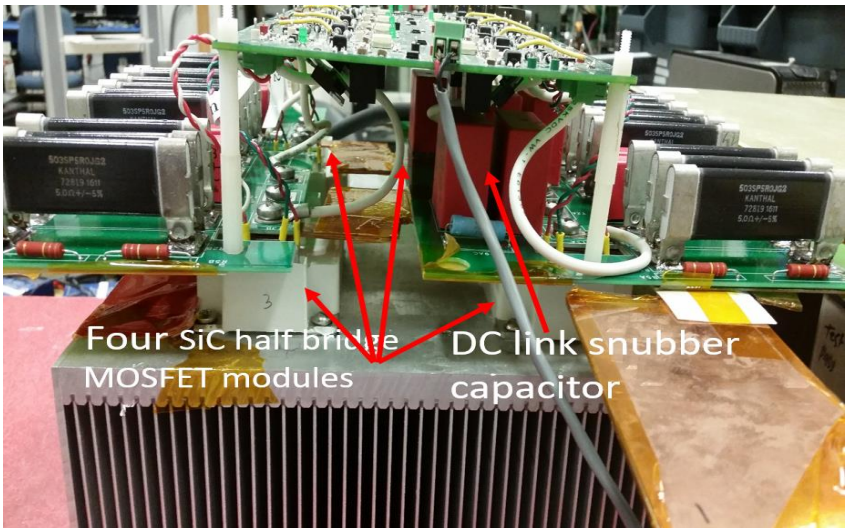
2.4.2 Dynamic Characterization with Four Series Connected 1.7 kV SiC MOSFET devices

Two series connected devices are not enough for building simple two-level MV converter with AC voltage (L-L) of 2 kV and above. Therefore, the demonstration of the **series connection of four 1.7 kV SiC MOSFET devices per arm (eight per leg)** in a "phase leg converter" (one leg or pole of three-phase two-level converter) is required (as in Fig. 2-2(b)). With the demonstration of four series-connected SiC MOSFET devices, it can be generalized for the 'n' number of SiC MOSFET devices can be connected in series for MV converter applications with AC voltages levels of 2 kV to 13.2 kV (L-L) or even HV applications.

Dynamic characterization is performed with four series connected 1.7 kV SiC MOSFET devices per arm of a phase leg. The corresponding experimental prototype is shown in Fig. 2-8. Four half-bridge modules (Wolf Speed CAS300M17BM2 1.7kV SiC MOSFET) are used for the switches S_1 to S_8 in Fig. 2-2(b). The gate to source voltage for the switches S_1 to S_8 are kept at nearly -5 V and a single pulse is applied to S_5 to S_8 at 3000V dc bus.



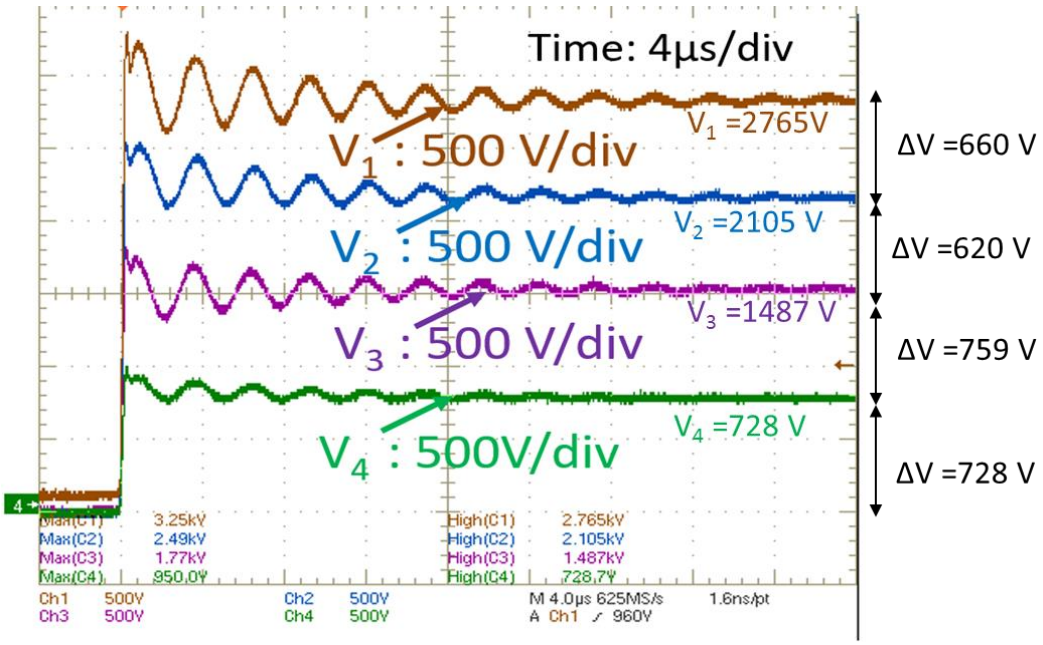
(a)



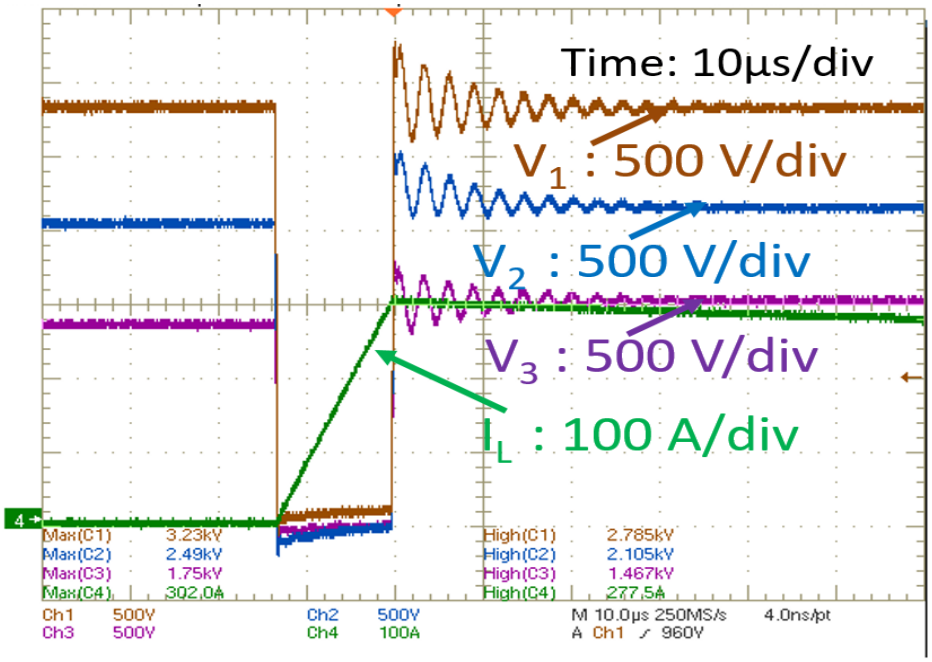
(b)

Fig. 2-8: Experimental setup of one phase-leg with four series-connected SiC MOSFET devices per arm mounted on the heat sink, dc link snubber capacitor, R_dC_d snubber for each device and an eight-channel gate driver; (a) Top View; (b) Side view

Fig. 2-9(a) shows the turn-off dynamic voltage characterization of four series connected 1.7 kV SiC MOSFET devices using optimal snubber capacitor value found from the previous section (C_d=33nF) and at 2800V dc bus, 300A switching current, R_{gon}=R_{goff} = 4.7 Ω, R_d =1.65 Ω, T_j=25^{0}C. The voltage imbalance across the devices is less than 10% of the nominal base operating voltage (V_{dc}/n=2800/4=700V). Fig. 2-9(b) shows that the Inductor current reached 300A before turn-off event, indicating the turn-off dynamic characterization is performed at a switching current of 300A.



(a)



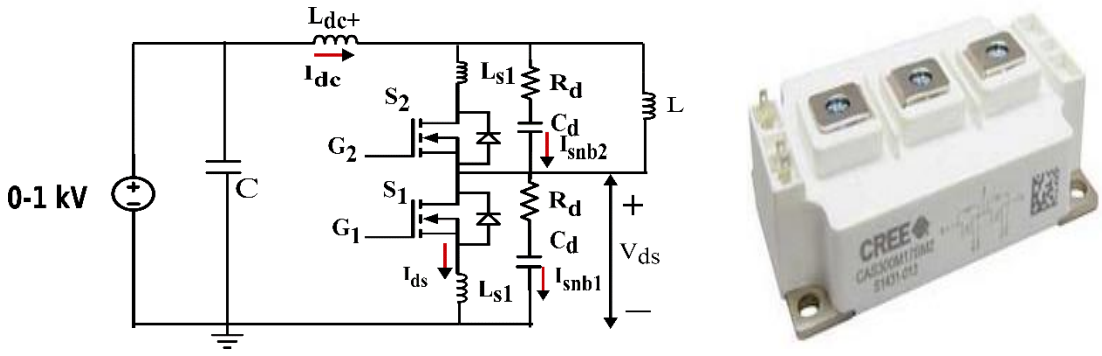
(b)

Fig. 2-9: Turn-off dynamic voltage characterization at 2800 V, 300 A, R_g:4.7Ω, R_dC_d:1.65 Ω, 33 nF, T_j=25^{0}C (a) Turn-off dynamic voltage across four SiC MOSFET devices w.r.t ground in a phase-leg arm; (b) Turn-off dynamic voltage characterization showing the inductor current (i.e., turn-off switch current is 300 A) and the three device voltages with respect to ground

Proper care has to be taken for the selection of correct probe to be used for device voltage measurements in the static and dynamic voltage characterization for the series connection of more than two devices. The input resistance of general LV or MV differential probes is not sufficiently large enough to be used in the series connection experiments. If these differential probes are used, the effective static resistance across each device may not be equal. Hence, the voltage measurements show more imbalance in the voltage sharing of the devices. Therefore, to offset the effect of probe input resistance in the measurements, MV probes with high input resistance (100 MΩ) have to be used. Four high input resistance single ended probes (Tektronix P6015A (20 kV DC, 75 MHz)) have been used in the device voltage measurements in all the experiments.

2.4.3 Influence of switching loop inductance on voltage peak overshoot and selection of snubber resistor (R_d) range

In the previous section 2.4.1, the optimal value of snubber capacitor value for the dynamic voltage to be less than 10-12% has been outlined. This section outlines the effect of different snubber resistors on the voltage peak overshoot during device turn-off for the given snubber capacitor value. In the series connection of SiC MOSFET devices, the peak voltage overshoot across each device during turn-off should be limited. Otherwise, the cumulative addition of dynamic voltage differences and voltage peak overshoot will reduce the voltage safety margin required for the device to operate under step change in loads.



(a) (b)

Fig. 2-10: Switching characterization circuit (1.7 kV SiC MOSFET with RC snubber) (b) 1.7 kV/300A Half Bridge Module (CAS300M17BM2)

To estimate the peak overshoot voltage for each device in the series connection of 'n' devices, a simplified equivalent circuit is required to emulate the nearly similar behavior on per device basis. The phase leg switching characterization setup with snubber across each device using the inductive clamped circuit shown in Fig. 2-10 (a) has been used to estimate the peak overshoot voltage per device. The '*dv/dt*' and '*di/dt*' seen by the device under test device in Fig. 2-10 (a) will be same on a per-device basis in the series connection of 'n' devices. It consists of the DC power supply, DC capacitor bank, inductor, the device under test (S_1) and freewheeling switch (S_2). The switches S_1 and S_2 are realized using half-bridge module shown in Fig. 2-10(b). The total loop inductance per switch is approximately 60 nH (15 nH due to the module, 45 nH due to DC bus). This loop inductance will emulate the similar loop inductance value seen by each switch in series connection due to contribution from module to module interconnection and DC bus connections.

Table 2-5 shows the summary of experimentally measured peak overshoot for different snubber resistor values for the optimal C_d range found in 2.4.1. For a given value of C_d, the peak overshoot increases with a decrease in 'R_d'. To limit the peak voltage overshoot across each device not to exceed 10-12%, the value of 'R_d' has to be within 1.5 Ω to 4.7 Ω. A similar trend has been observed from the 'Simplis/Simtrex' simulation using general SiC MOSFET model and also using analytical method [32]. The Fig. 2-11 shows the peak overshoot with different snubber resistor values and for different switching currents for C_d=33 nF at 900 V dc bus. The peak overshoot increases at extremely lower and higher values snubber resistor. **The range of R_d for which peak overshoot minimum is nearly 1.25 Ω to 4.7 Ω.**

Table 2-5: Experimentally measured voltage peak overshoot with different snubber values

	At 900 V, 100 A	**At 900 V, 150 A**
Snubber value	**% peak overshoot**	**% peak overshoot**
22 nF, 1.56 Ω	7.667	10.222
22 nF, 2.35 Ω	6.833	8.667
22 nF,4.7 Ω	4.889	6.667
33 nF,2.35 Ω	5.878	7.556
33 nF,4.7 Ω	4.056	5.778

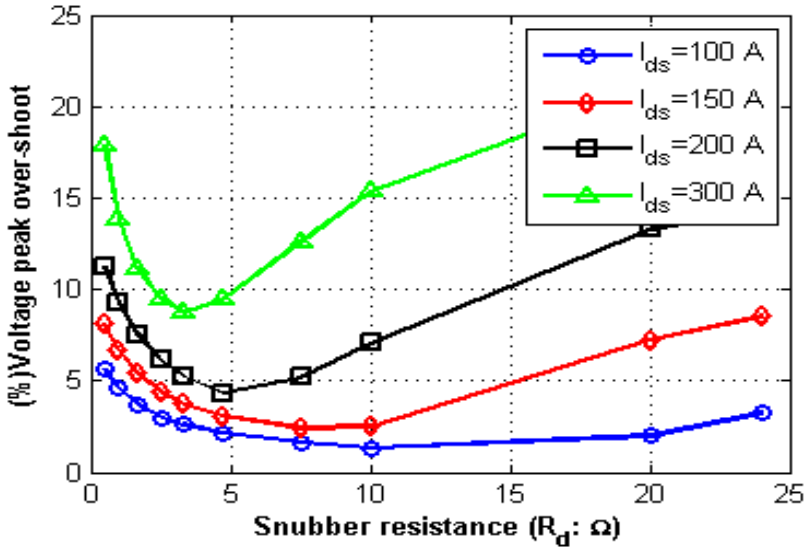


Fig. 2-11: Peak overshoot trend for different snubber resistor values for C_d= 33 nF, Loop inductance of 60 nH and at 900 V dc bus, R_{goff}: 4.7 Ω

2.5 Switching losses per device (E_{sw}) with RC snubber in series connection

The previous section outlines the range of R_d to be used in the series connection to minimize the voltage peak overshoot for a given value of C_d. This section outlines the experimental total switching losses per switch (device switching losses and the snubber resistor switching losses) and concludes the value of R_d to be used in the series connection for a given optimal value of C_d.

2.5.1 Device switching losses with RC snubber in the series connection

To estimate the device switching losses in the series connection of 'n' devices, a simplified equivalent circuit is required to emulate the nearly similar switching behavior on a per-device basis. The phase-leg inductive clamped switching characterization setup with snubber across each device shown in Fig. 2-10(a) has been used to estimate the device switching losses. The switching losses observed in the device under test in Fig. 2-10 (a) will be same on a per-device basis in the series connection of 'n' devices (as in Fig. 1-3). The validation of this simplified circuit is also shown in this section.

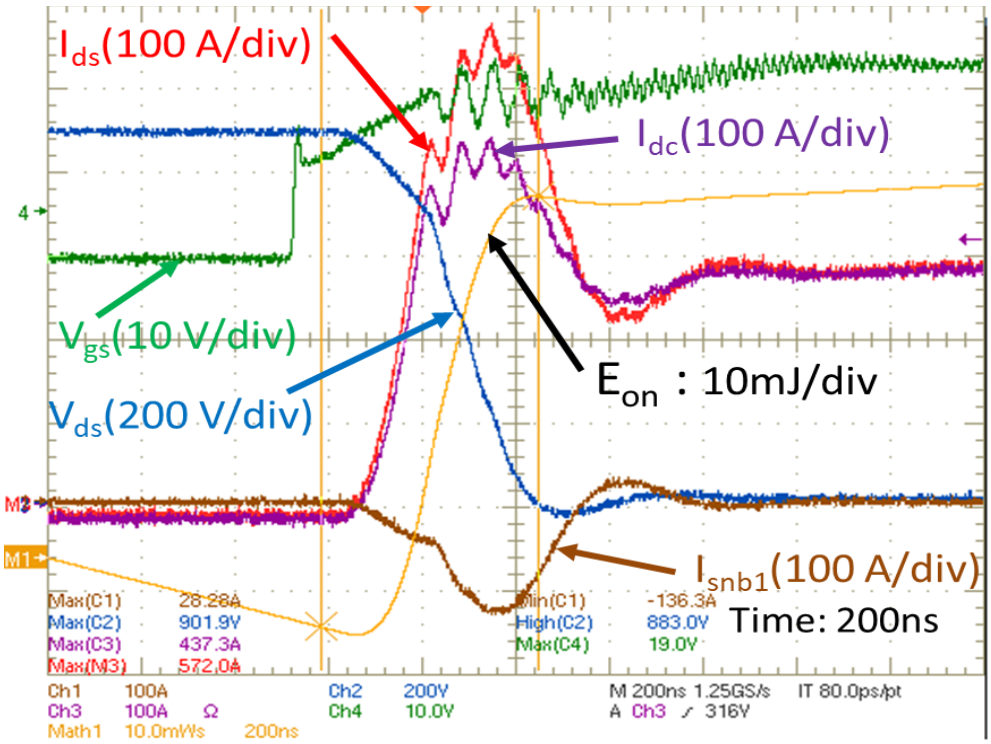


Fig. 2-12: Turn-on switching characterization of 1.7 kV SiC MOSFET with snubber at 900 V, 300 A, R_g=4.7 Ω. R_dC_d=1.56 Ω, 33 nF, T_j=25^{0}C. (Turn-on losses (E_{on}): 52 mJ)

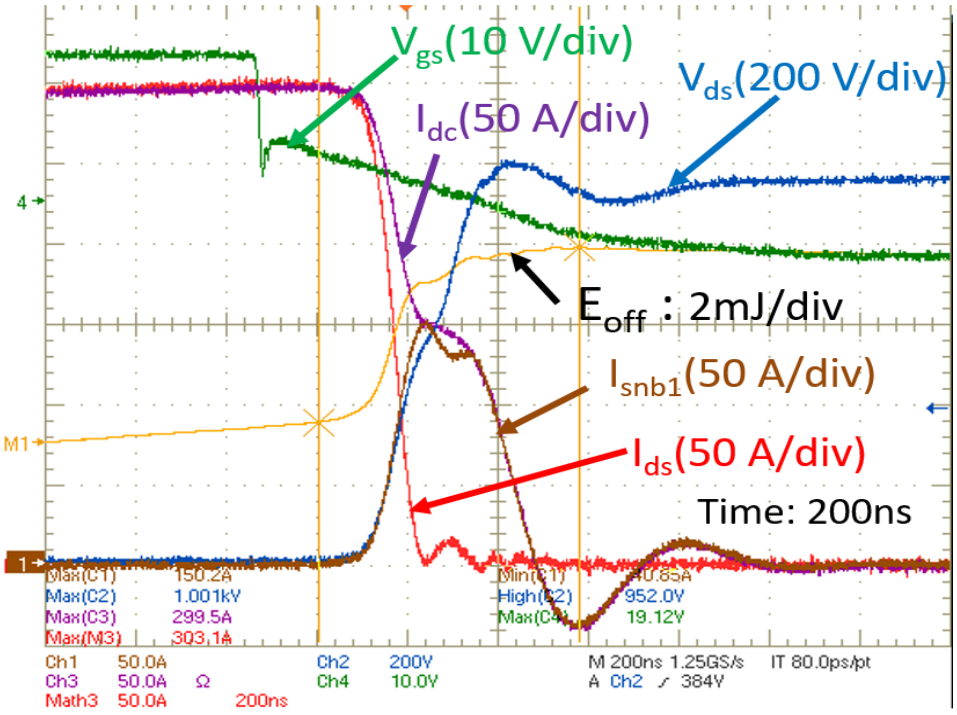


Fig. 2-13: Turn-off switching characterization of 1.7 kV SiC MOSFET with snubber at 900 V, 300 A, R_g=4.7 Ω. R_dC_d=1.56 Ω, 33 nF, T_j=25^{0}C. (Turn-off losses (E_{off}): 4.93 mJ)

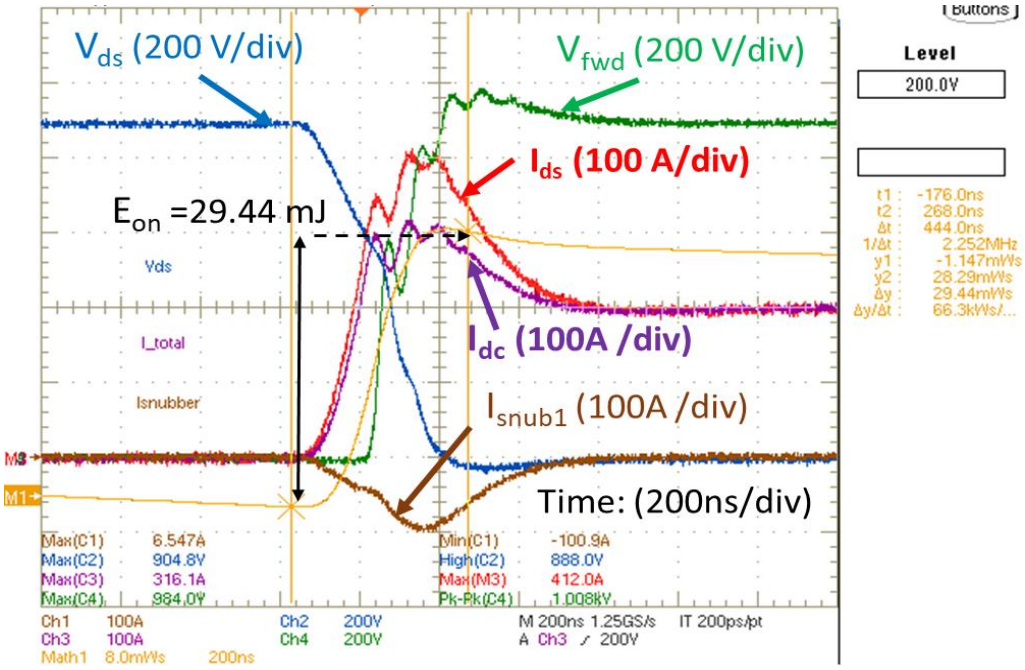


Fig. 2-14: Turn-on switching characterization of 1.7 kV SiC MOSFET with snubber at 900 V, 200 A, R_g=4.7 Ω. R_dC_d=4.7 Ω, 33 nF, T_j=25^{0}C. (Turn-on losses (E_{on}): 29.44 mJ)

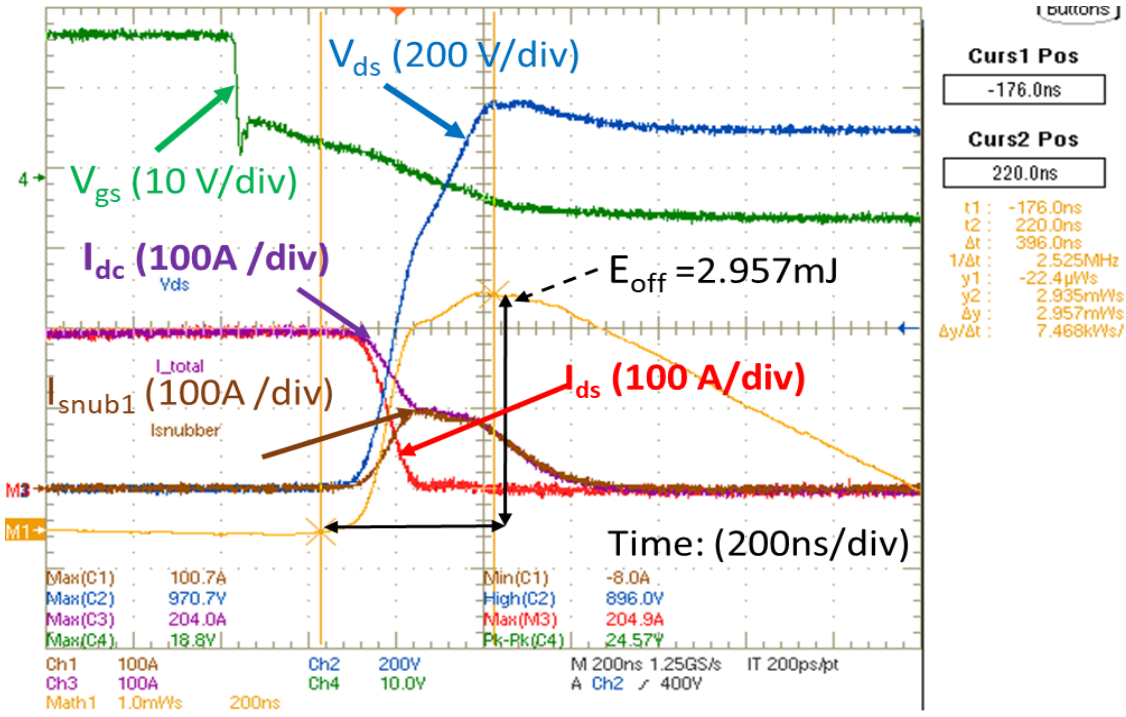


Fig. 2-15: Turn-off switching characterization of 1.7 kV SiC MOSFET with snubber at 900 V, 200 A, R_g=4.7 Ω. R_dC_d=4.7 Ω, 33 nF, T_j=25^{0}C. (Turn-off losses (E_{off}): 2.957 mJ)

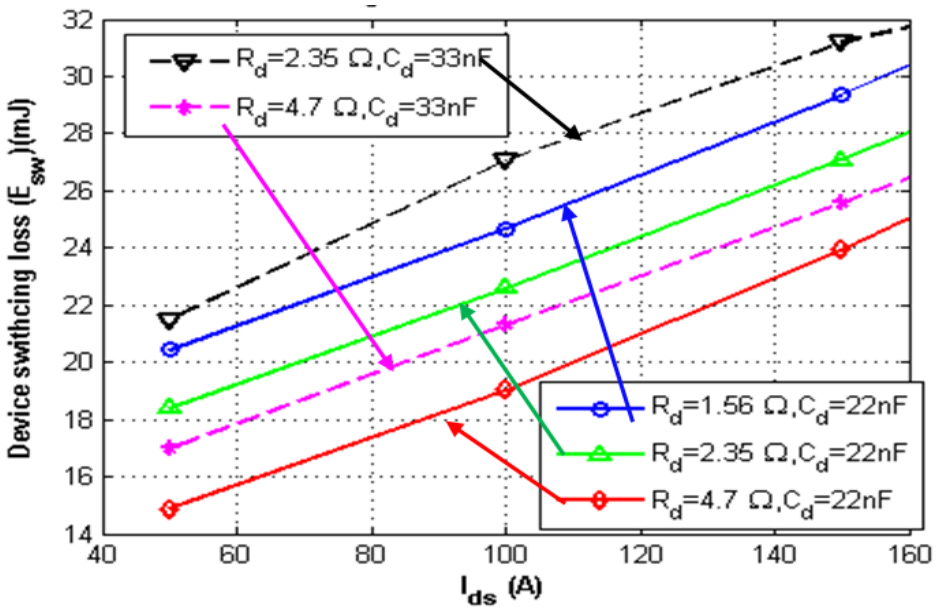


Fig. 2-16: Total device switching loss variation with current for different snubber values at 900 V switching voltage, R_{gon}=R_{goff}=4.7 Ω

The bottom device is the device under test and the top device is used as freewheeling. Fig. 2-12 and Fig. 2-13 show the turn-on and turn-off losses per device at 900 V, 300 A with R_dC_d (1.56 Ω, 33 nF), T_j= 25^{0}C and R_g: 4.7 Ω. Where, V_{ds} (Blue): Voltage across device; I_{ds} (Red): Current through the device; $I_{snubber}$ (Brown): current through Snubber; I_{total} (Magenta): total input current; V_{fwd} (Green): Freewheeling switch (S_2) voltage; M1 (Orange): Switching Energy. Similarly, Fig. 2-12 and Fig. 2-13 show the turn-on and turn-off losses per device at 900 V, 200 A with R_dC_d (4.7 Ω, 33 nF), T_j= 25^{0}C and R_g: 4.7Ω.

Fig. 2-16 shows the total switching loss variation with current for different snubber values (R_dC_d) and without snubber at 900 V switching voltage, R_{gon} =R_{goff} =5 Ω. It is evident from the Fig. 2-16 that the device switching losses (E_{sw}= E_{on}+E_{off}) are increasing with reducing snubber resistor (R_d) for a given value of snubber capacitor (C_d). Therefore, the **optimal series snubber resistor, which minimizes the device switching losses, is R_d =4.7 Ω** can be used for the series connection. This value also keeps the dynamic voltage imbalance and peak overshoot voltage less than 10-12%, for the given optimal snubber value (22 nF-33 nF) as concluded from an earlier section. However, R_d =4.7 Ω does not minimize the total switching losses (E_T= E_{on}+E_{off} +E_{Rd}) (including snubber resistor losses (E_{Rd}) during switching). The details snubber resistor switching losses, total switching losses and selection of 'R_d' are presented in section 2.6.

2.5.2 Validation of characterized device switching loss results with RC snubber for series connection of ‘n’ number of devices

To evaluate the switching loss on a per device in the series connection of ‘n’ devices, it is expensive and not practical to build an inductive clamped circuit with ‘n’ devices in series. A simplified equivalent circuit, which emulates the snubber behavior same as a series connection with ‘n’ devices shown in Fig. 2-10(a) has been used in the earlier section 2.5.1. The switching losses evaluation and peak overshoot mitigation using RC snubber across SiC MOSFET in a phase leg configuration are mentioned in [34]. It uses the RC snubber across the device under test (low side switching device) but not across the freewheeling device (high side device). This circuit will give pessimistic (lower than actual) turn-on losses because it does not include the turn-on current charging current contribution from the upper snubber capacitor during turn-on of low side device or vice-versa. Since the series connected devices have RC snubber in both lower and upper arm of the phase-leg converter. Therefore, it is important to validate the method employed shown in Fig. 2-10(a) to calculate the switching loss per device in the series connection. Hence, the inductive clamped circuit with two devices per arm in series connection shown in Fig. 2-2(a) has been used, and the switching losses are measured in two devices (S_1 and S_2) with S_3 and S_4 acting as freewheeling diodes. The switching losses measured are compared with results obtained using simplified test setup (Fig. 2-10(a)).

Fig. 2-17 and Fig. 2-18 show the turn-on and turn-off losses in the device –S_2 using series connection setup in Fig. 2-2(a). Comparing Fig. 2-17-Fig. 2-18 with Fig. 2-14-Fig. 2-15, it is evident that the current through the snubbers and device measured using series connection setup nearly matches with results obtained using simplified setup (Fig. 2-10(a)) during both turn-on and turn-off transitions. Also, the fall times, rise times of voltage across each device and the turn-on, turn-off losses per device measured using series connection setup nearly matches with switching losses measured using the simplified setup.

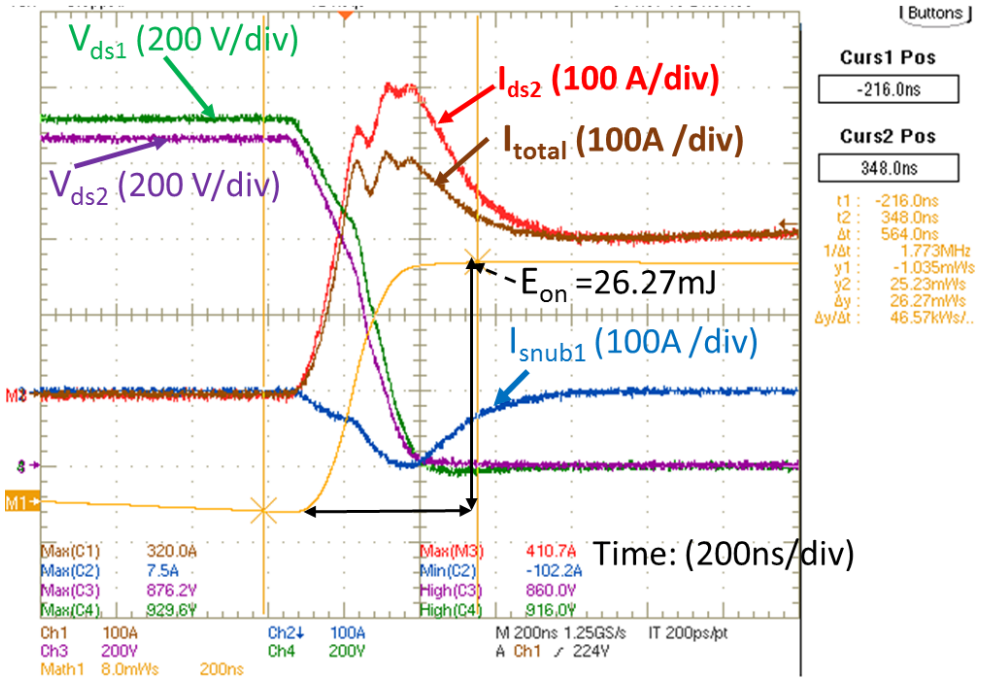


Fig. 2-17: Turn-on losses in MOSFET – S_2 (26.27 mJ) at 900 V, 200 A, T_j:25^{0}C, R_{gon} =5 Ω and at 1800 V DC bus using series connection with R_dC_d (33 nF, 4.7 Ω)

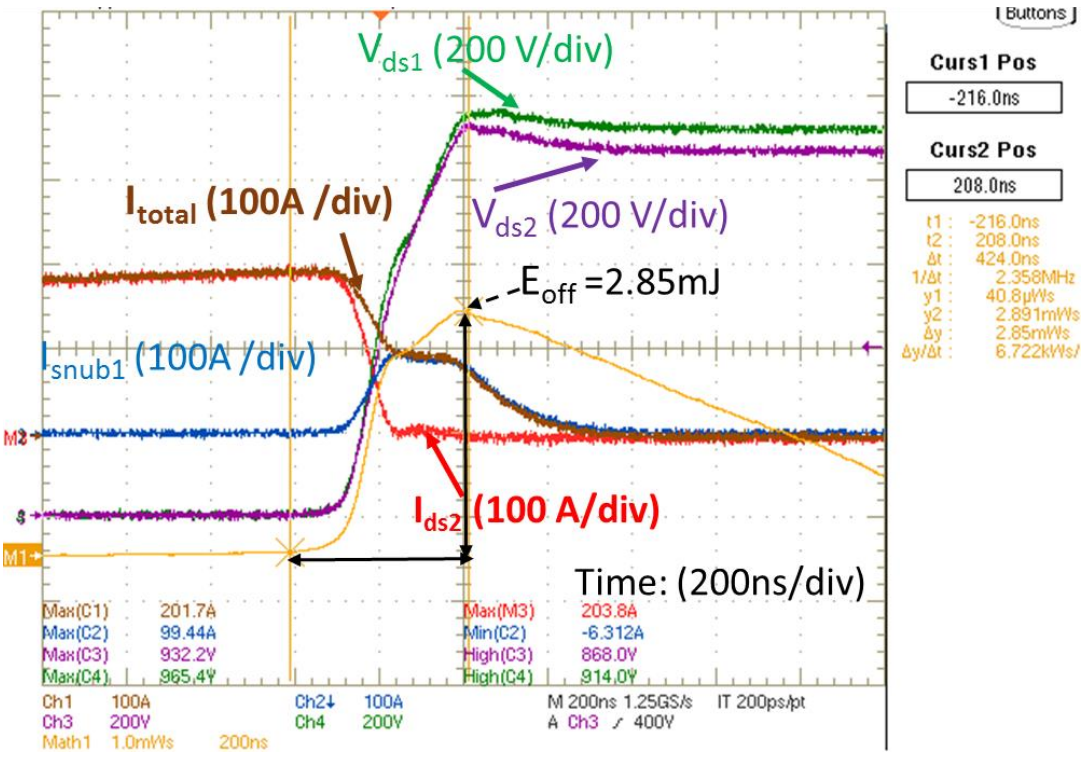


Fig. 2-18: Turn-off losses in MOSFET – S_2 (2.85 mJ) at 900 V, 200 A, T_j:25^{0}C, R_{gon} =4.7 Ω and at 1800 V DC bus using series connection with R_dC_d (33 nF, 4.7 Ω)

Table 2-6 shows the summary of total switching loss comparison measured using two setups at different switching current values. However, there is a small difference in the switching; losses within two MOSFETs measured using series connection setup, due to the difference in dynamic voltage differences. On an average, the total device losses measured using series connection setup nearly matches with the simplified circuit. Therefore a simplified setup is shown in Fig. 2-10 (a) can be used to evaluate the switching losses per device with different snubber values, instead of building expensive and complex phase leg with 'n' devices connected in series. Hence, the total switching loss with 'n' number of the series connected device is 'n' times the switching loss per device computed using setup –Fig. 2-10 (a).

Table 2-6: Comparison of total device switching loss ($E_{sw}= E_{on}+E_{off}$) measured with two setups, at $R_{gon}=R_{goff}=4.7\ \Omega$

Switching current	RC snubber	E_{sw} using series connection setup-Fig. 2-2(a) At 1800 V dc bus		Esw using setup-Fig. 2-10(a) At 900 V dc bus
(A)		MOSFET-S_1 (mJ)	MOSFET-S_2 (mJ)	MOSFET-S_1 (mJ)
100	33 nF, 4.7 Ω	23.64	20.46	20.9
150		29.92	25.48	26.58
200		37.41	29.12	32.39

2.6 Computation of Snubber resistor losses (E_{Rd})

In the above section 2.5, device switching loss per device with external snubber cases has been evaluated. However, there are additional losses in the overall converter due to power loss in series snubber resistor during turn-on and turn-off transition. Eq (2-3) has been used to compute snubber resistor losses per device (E_{Rd}) in a switching cycle. During turn-off of low side device, load current has been shared between both top and bottom snubber. Similarly, during turn-on of low side switch, some part of the energy stored in the snubber capacitor will be dissipated in both snubber resistors (top& bottom). Therefore, RMS value of both snubber currents is required to compute P_{Rd} or E_{Rd}. The RMS value of the snubber current can be calculated using the measured snubber current from switching characterization. The measured snubber current transition is approximated as shown in Fig. 2-19 to compute the losses in the snubber resistor. Fig. 2-12 -Fig. 2-15 and Fig. 2-20 show the similar wave shape of the snubber current during turn-on and turn-off transition from the experiments, and it validates the approximation. Therefore, the RMS value of snubber current is calculated using eq (2-4), and also the RMS values of snubber currents (top and bottom) are approximately equal. Where T_s ($=1/f_{sw}$) is total switching period, I_{pk1} to I_{pk2} are the values of snubber current during turn-

on and turn-off transition corresponding to time intervals ΔT_1 - ΔT_4 as shown in Fig. 2-19. The RMS value of snubber current can also be calculated using measured snubber current that has been saved in '.csv.' format with enough number of samples from the experimental characterization and using eq (2-5) in MATLAB.

$$P_{Rd} = \left(I_{snb1}^{rms}\right)^2 \cdot R_d + \left(I_{snb2}^{rms}\right)^2 \cdot R_d;$$
$$E_{Rd} = P_{Rd} \cdot f_{sw} \qquad (2\text{-}3)$$
$$E_{Rd} = 2\left(\frac{\Delta T_1}{3} I_{pk1}^2 + \frac{\Delta T_2}{3} I_{pk2}^2 + \frac{\Delta T_3}{3} I_{pk3}^2 + \Delta T_4 I_{pk3}^2 + \frac{\Delta T_5}{3} I_{pk3}^2 + \frac{\Delta T_6}{3} I_{pk4}^2\right) R_d$$

$$I_{snb}^{rms} = \sqrt{\left(\frac{\Delta T_1}{3T_s} I_{pk1}^2 + \frac{\Delta T_2}{3T_s} I_{pk2}^2 + \frac{\Delta T_3}{3T_s} I_{pk3}^2 + \frac{\Delta T_4}{T_s} I_{pk3}^2 + \frac{\Delta T_5}{3T_s} I_{pk3}^2 + \frac{\Delta T_6}{3T_s} I_{pk4}^2\right)};$$
$$I_{snb1}^{rms} = I_{snb2}^{rms} = I_{snb}^{rms};$$
(2-4)

$$I_{snb}^{rms} = \sqrt{\left(\frac{1}{N}\sum_{n=1}^{N}\left(I_{snb1}^{rms}(n)\right)^2 + \left(I_{snb2}^{rms}(n)\right)^2\right)};$$
$$N = \frac{f_{sample}}{f_{sw}}; \quad I_{snb1}^{rms} = I_{snb2}^{rms} = I_{snb}^{rms}; \qquad (2\text{-}5)$$

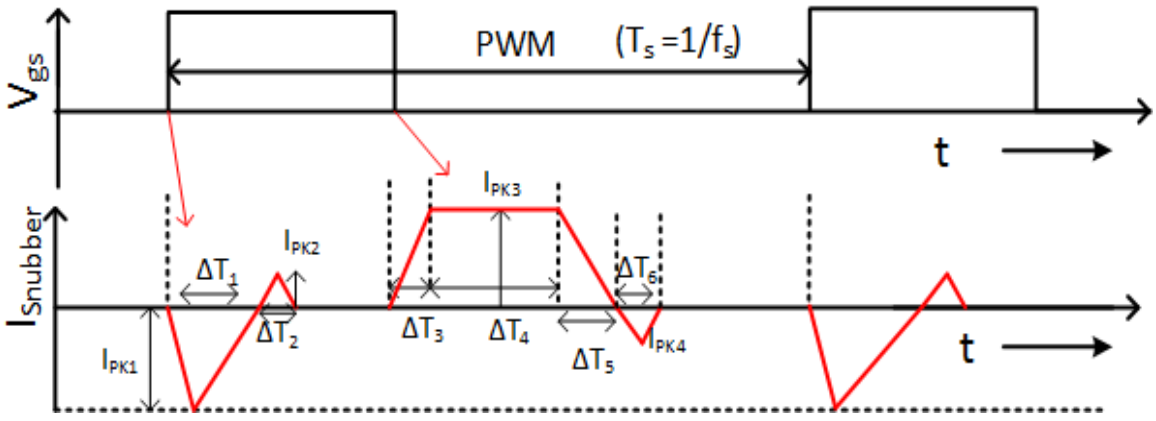
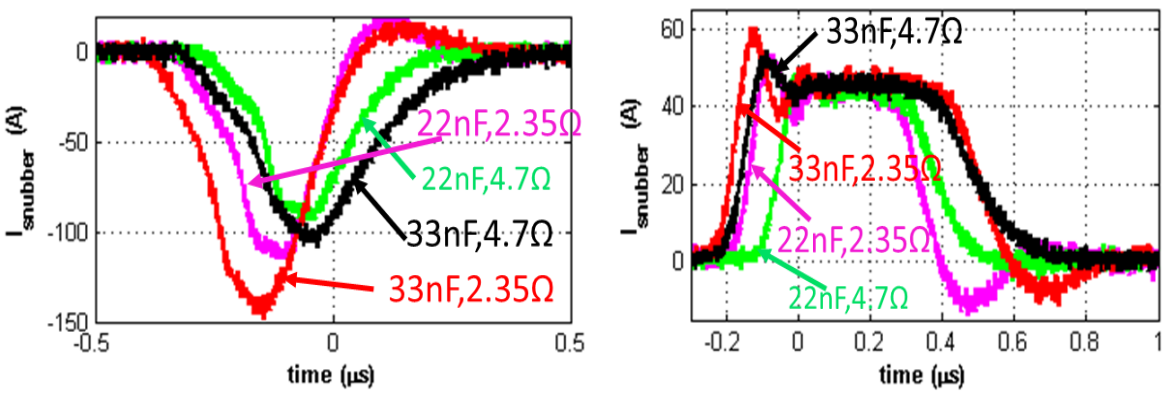


Fig. 2-19: Approximation of Snubber current during turn-on and turn-off



(a) (b)

Fig. 2-20: The wave shape of current through RC Snubber at 900 V, 100 A switching current (a) during turn-on (b) during turn-off

Fig. 2-21 and Fig. 2-22 show the energy loss in snubber resistor losses per device (E_{Rd}) and total switching loss per device (E_T) for different snubber values and different switching currents at 900 V switching voltage, R_g=4.7 Ω. Where $E_T = E_{sw} + E_{rd}$; E_T is total switching loss per device, E_{sw} is device switching loss, and E_{rd} is snubber switching losses per device.

It clear from Fig. 2-21 that the snubber resistor losses are increasing with increase in snubber resistor value for a given snubber capacitor. It increases the total switching loss per device (as shown in Fig. 2-22) and reduces the overall converter efficiency. Therefore to minimize the total switching losses and to increase the converter efficiency, the value of the series resistor (R_d) has to be < 4.7 Ω. But 'R_d' cannot be as low as zero or lower than 1.25 Ω, because the peak overshoot will increase at the very low value of snubber resistor (R_d) for a given value of snubber capacitor (C_d:22 nF to 33 nF)) and switch loop inductance (L_p) as concluded in the section 2.4.3 . **Therefore, the optimal values of R_dC_d for series connection which satisfies the constraints mentioned in the flowchart are 22 nF ≤ C_d ≤ 33 nF and R_d =1.25 Ω to 1.5 Ω.** The switching losses corresponding to optimal snubber values of 33 nF, 1.56 Ω are shown in Fig. 2-23. The Fig. 2-23 shows summary of the Turn-on loss (E_{on}), Turn-off loss (E_{off}), Device switching loss ($E_{sw} = E_{on}+E_{off}$), Snubber resistor switching loss (E_{Rd}), Total switching losses per device ($E_T = E_{on} + E_{off} + E_{Rd}$) at different switching currents and at switching voltage of 900 V, R_g=4.7 Ω and R_dC_d=1.56 Ω. Since the total switching losses per device are known, this information will be useful for power electronic engineers to evaluate the efficiency of power converters realized using the series connection of 'n' devices.

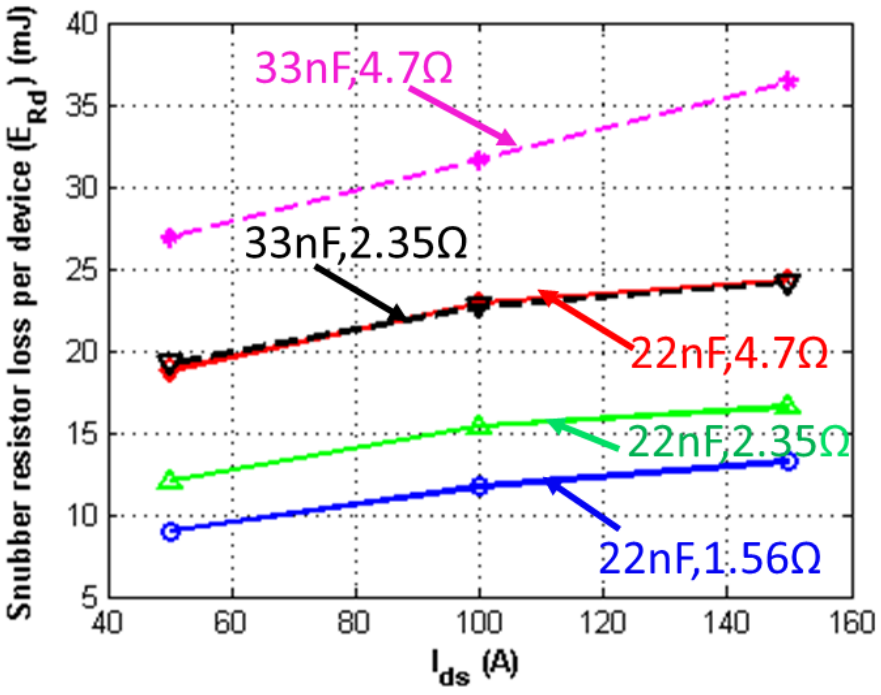


Fig. 2-21: Energy losses in Snubber resistor per device (E_{Rd}) at 900 V, R_g=4.7 Ω

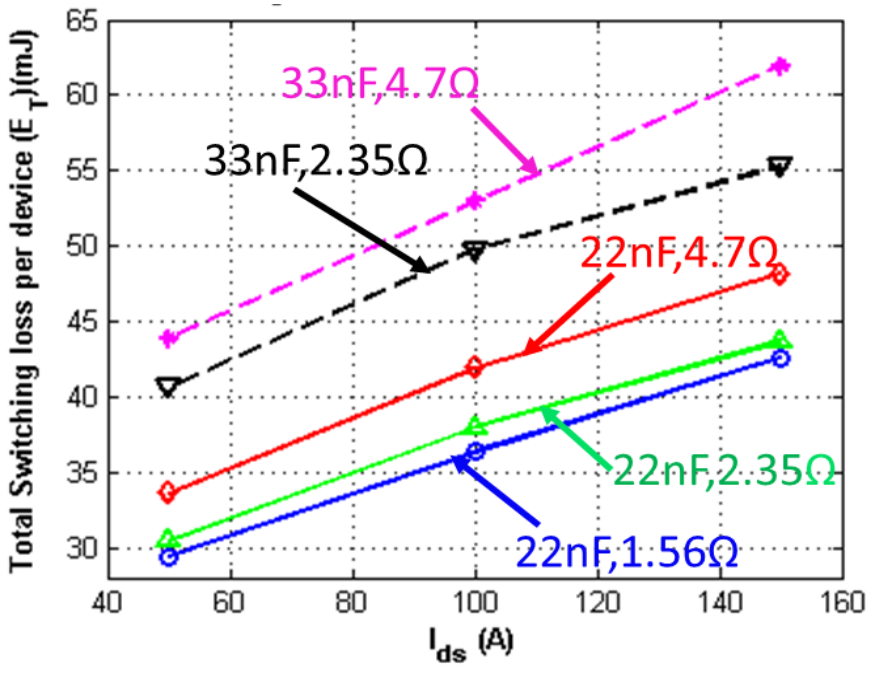


Fig. 2-22: Total switching loss per device (E_T) at 900 V, R_g=4.7 Ω

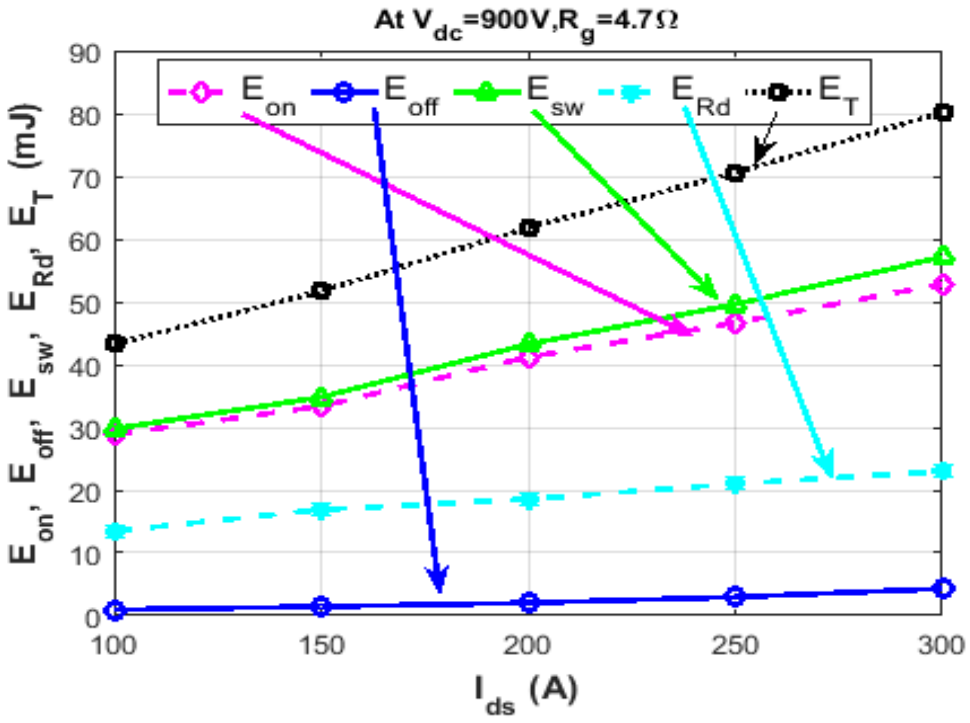


Fig. 2-23: The variation of different switching loss components w.r.t switching current and at switching voltage 900 V, R_g=4.7 Ω, R_dC_d=1.56 Ω, 33 nF

2.6.1 Analytical expression for snubber current in a phase leg converter to compute Snubber resistor losses

In the above section, snubber resistor losses computation from experimentally measured snubber current has been shown. In this subsection, the analysis of a phase leg converter with snubber has been carried out to derive the snubber current expressions. These expressions will be useful to compute the analytical RMS value of snubber current, losses in the snubber resistor and it will eliminate the experimental snubber current measurements.

For the analysis of snubber current in a phase-leg configuration circuit, the dc bus parasitic inductance (L_s) and R_dC_d snubber terminal inductances (L_d) have been considered, whereas the parasitic parameters of the device are neglected to reduce the complexity. The following cases have been considered for deriving the snubber current in a phase leg configuration. Most of the derived equations for this analysis are kept in Appendix Chapter.

Case 1: Snubber current contribution from RC snubber connected across the DUT during turn-on.

Case 2: Snubber current contribution from RC snubber connected across the freewheeling device into DUT during turn-on.

Case 3: Snubber current flowing into the RC snubber connected across the DUT and Freewheeling device during turn-off.

2.6.1.1 Case 1: Snubber current contribution from snubber connected across the DUT during turn-on

It has been assumed that the device S_1 is the DUT, S_2 is the freewheeling device for the analysis and also let T_r is the rise time for the current, T_f is the voltage fall time during turn-on. Fig. 2-24(a)-(b) shows the device current contribution due to its own snubber, freewheeling snubber and load current during turn-on for two different time intervals ($0 < t < T_r$, $t > T_r$) during turn-on. When the positive gate to source voltage is applied, the DUT channel will be formed when V_{gs1} more than its threshold voltage and current starts increasing into DUT and reaches load current by $t=T_r$, and freewheeling device current falls zero. Since the freewheeling device is conducting until $t= T_r$, the voltage across the freewheeling device is nearly zero. Therefore, entire dc bus voltage (V_{dc}) is supported by DUT. However, there is a decrease in voltage across the DUT (V_{ds1}) from V_{dc} due to parasitic dc bus inductance coupled with 'di/dt' during $0 < t < T_r$ as shown in Fig. 2-25(a). Due to a decrease in voltage across the DUT, the snubber capacitor V_{Cd1} will start discharging into DUT for $t > 0$, and the increase in snubber current (i_{snb1}) is shown in Fig. 2-25(a). For $t > T_r$, the voltage across the freewheeling device starts supporting voltage, so the voltage across it starts increasing, and DUT voltage starts falling quickly. Therefore the charging current through snubber 'i_{snb2}' starts increasing (Fig. 2-25(b)) and 'i_{snb1}' will further increase as shown in Fig. 2-25(a).

To derive the snubber current (i_{snb1}) during turn-on, KVL is applied to the DUT, and its own RC snubber (Fig. 2-24(a)) and the resultant equations are shown in (2-6), and the DUT voltage (V_{ds1}) is given by(2-7).

$$V_{ds1}(t)+L_d\frac{di_{snb1}(t)}{dt}+R_d\ i_{snb1}(t)+\frac{1}{C_d}\int i_{snb1}(t)\,dt=0\ ;$$
$$\left(sL_d+R_d+\frac{1}{C_d s}\right)i_{snb1}(s)+\frac{V_{Cd1}(0)}{s}=-V_{ds1}(s);\quad V_{Cd1}(0)=V_{dc} \tag{2-6}$$

$$V_{ds1}(t)=\begin{cases}\left(V_{dc}-\dfrac{L_s kt}{T_r}\right) & \text{for } 0\le t<T_r;\\ \left(\dfrac{V_{dc}-L_s k}{T_f-T_r}\right)\left(T_f-t\right) & \text{for } T_r\le t<T_f;\\ 0 \quad t\ge T_f\ ; & \end{cases} \tag{2-7}$$

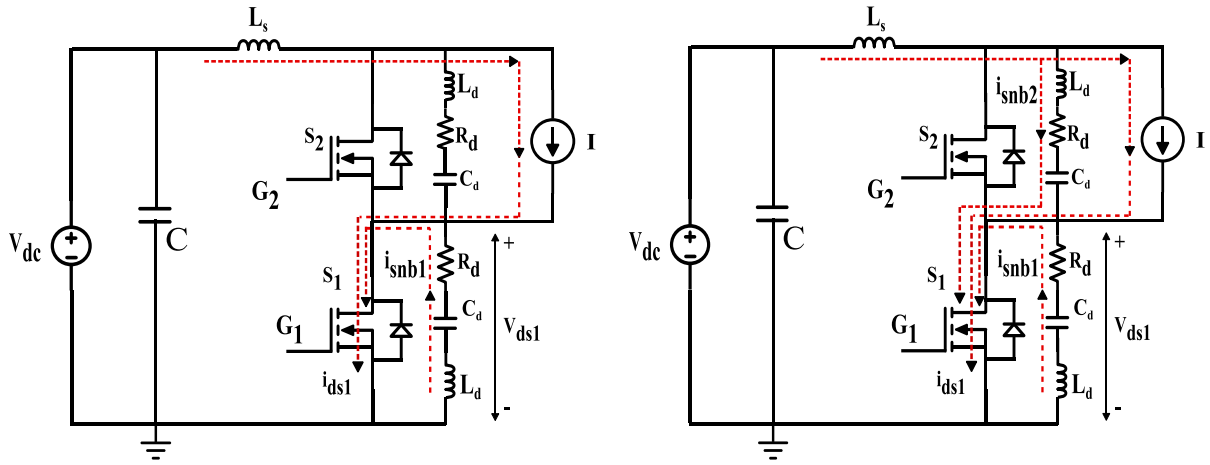


Fig. 2-24: The turn-on device current contribution due to its own snubber and load current for $0<t<T_r$; (b) Shows the turn-on device current contribution due to its own snubber, Freewheeling snubber and load current for $t > T_r$

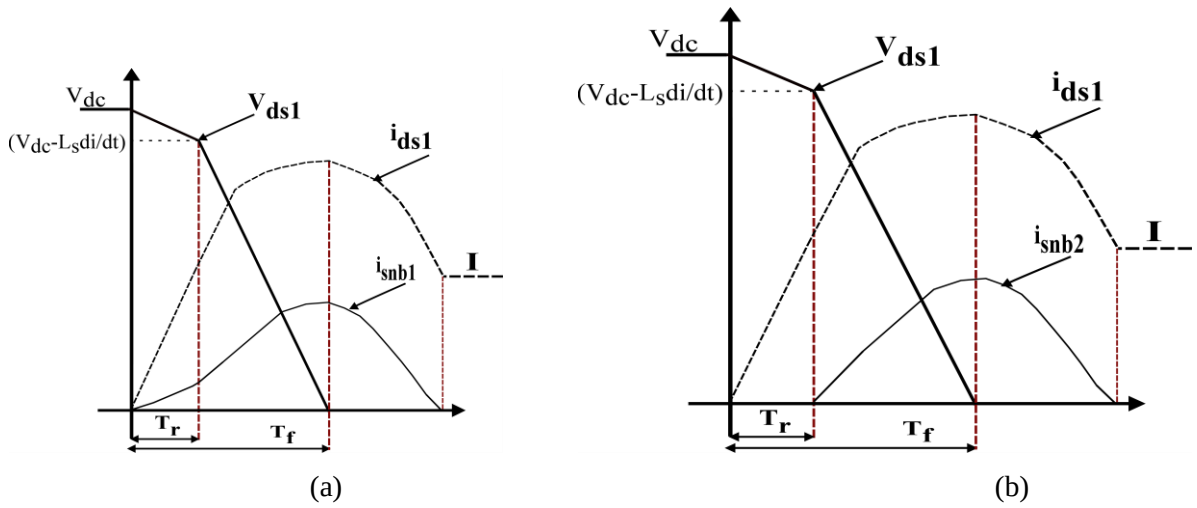


Fig. 2-25: Turn-on switching waveforms with snubber and dc bus parasitic inductance (Approx.); (a): shows the DUT voltage, current, and snubber current from RC snubber connected across DUT; (b) shows the DUT voltage, current, and snubber current from RC snubber connected across Freewheeling device

$$U_{T_r}(t)=\begin{cases}0 & \text{for } t<T_r\\ 1 & t\geq T_r\end{cases};\ U_{T_f}(t)=\begin{cases}0 & \text{for } t<T_f\\ 1 & t\geq T_f\end{cases};\qquad (2\text{-}8)$$

Let $U_{T_r}(t)$, $U_{T_f}(t)$ are step functions defined as shown in (2-8). The $V_{ds1}(t)$ can be written using step functions as shown in (2-9) to (2-11) and the corresponding $V_{ds1}(s)$ is given in(2-12).

$$\left.\begin{aligned}V_{ds1}(t)&=\left(V_{dc}-\frac{L_s kt}{T_r}\right)\left(1-U_{T_r}(t)\right)\\ &=\left(V_{dc}-\frac{L_s kt}{T_r}\right)-\left(V_{dc}-\frac{L_s kt}{T_r}\right)U_{T_r}(t)\\ V_{ds1}(t)&=\left(V_{dc}-\frac{L_s kt}{T_r}\right)-\left(V_{dc}-L_s k\right)U_{T_r}(t)+\frac{L_s k(t-T_r)}{T_r}U_{T_r}(t);\quad \text{for } 0\leq t<T_r;\end{aligned}\right\}\qquad (2\text{-}9)$$

$$\left.\begin{aligned}&V_{ds1}(t)=\left(\frac{V_{dc}-L_s k}{T_f-T_r}\right)(T_f-t)\left(U_{T_r}(t)-U_{T_f}(t)\right);\quad \text{for } T_r\leq t<T_f;\\ &\textit{let } B=\left(\frac{V_{dc}-L_s k}{T_f-T_r}\right);\\ &V_{ds1}(t)=BT_f\left(U_{T_r}(t)-U_{T_f}(t)\right)-B\,t\left(U_{T_r}(t)-U_{T_f}(t)\right)\quad \text{for } T_r\leq t<T_f;\\ &V_{ds1}(t)=BT_f\left(U_{T_r}(t)-U_{T_f}(t)\right)-BT_r U_{T_r}(t)+BT_f U_{T_f}(t)-B(t-T_r)U_{T_r}(t)+B(t-T_f)U_{T_f}(t)\end{aligned}\right\}\qquad (2\text{-}10)$$

$$V_{ds1}(t)=\left\{\begin{aligned}&\left(V_{dc}-\frac{L_s k\,t}{T_r}\right)-\left(V_{dc}-L_s k\right)U_{T_r}(t)+\frac{k\,L_s(t-T_r)}{T_r}U_{T_r}(t)+BT_f\left(U_{T_r}(t)-U_{T_f}(t)\right)-B\,T_r\,U_{T_r}(t)\\ &+B\,T_f\,U_{T_f}(t)-B\,(t-T_r)\,U_{T_r}(t)+B\,(t-T_f)U_{T_f}(t);\quad \text{for } 0\leq t<T_f;\end{aligned}\right\}$$

(2-11)

$$V_{ds1}(s)=\left(\frac{V_{dc}}{s}-\frac{L_s kt}{s^2T_r}\right)-\frac{(V_{dc}-L_s k)}{s}e^{-sT_r}+\frac{L_s k}{T_r s^2}e^{-sT_r}+\frac{B(e^{-sT_f}-e^{-sT_r})}{s^2}+\frac{B(T_f-T_r)}{s}e^{-sT_r};\quad \text{for } 0\leq t<T_f;$$

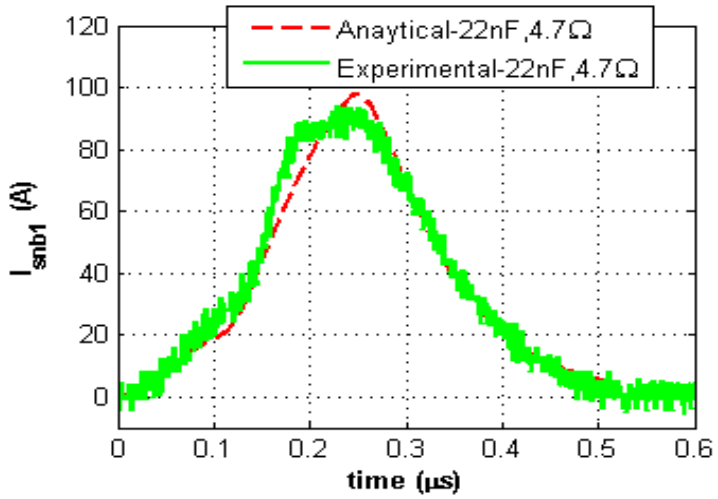
(2-12)

To simplify the analysis, It has been assumed that the 'k' = 'di/dt' is constant for a given value of turn-on gate resistance (R_{gon}) during $0 \le t < T_r$. Substituting (2-12) in (2-6) gives the $i_{snb1}(s)$ is given by (2-13).

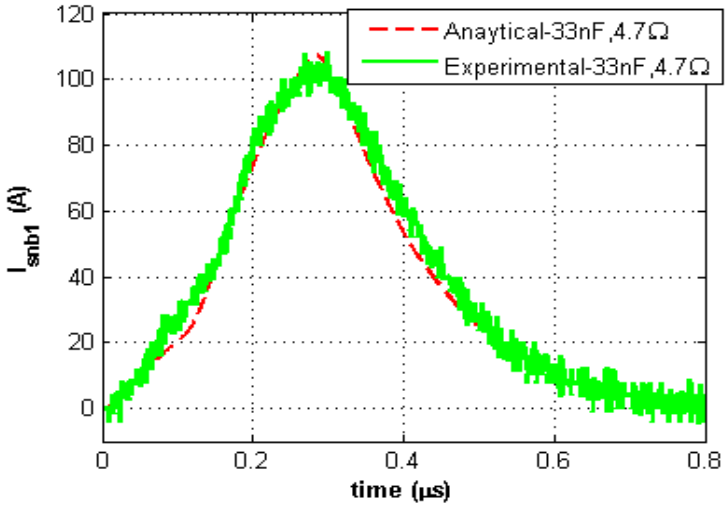
The solution for the snubber current '$i_{snb1}(t)$' is given in (7-1) for $R_d < 2\sqrt{\frac{L_d}{C_d}}$ and in (7-2) $R_d > 2\sqrt{\frac{L_d}{C_d}}$ respectively (in Appendix Chapter). The parameters 'V_{dc}', 'L_s' are known parameters for a given DC bus design and the parameters 'T_r '(current rise time), 'T_f' (voltage fall time), turn-on 'di/dt' are also known for a given value of turn-on gate resistance(R_{gon}) in (7-1) and (7-2). Therefore the snubber current '$I_{snb1}(t)$' ((7-1) and (7-2)) during turn-on and snubber resistor losses can be evaluated for snubber values R_dC_d using MATLAB.

$$\left\{ i_{snb1}(s) = \frac{\left(\frac{L_s k}{T_r L_d}\right)}{s\left(s^2 + \frac{R_d}{L_d}s + \frac{1}{L_d C_d}\right)} + \frac{\left(\frac{(V_{dc} - L_s k)}{L_d}\right)e^{-sT_r}}{\left(s^2 + \frac{R_d}{L_d}s + \frac{1}{L_d C_d}\right)} - \frac{\left(\frac{L_s k}{T_r L_d}\right)e^{-sT_r}}{s\left(s^2 + \frac{R_d}{L_d}s + \frac{1}{L_d C_d}\right)} - \frac{\frac{B}{L_d}\left(e^{-sT_f} - e^{-sT_r}\right)}{s\left(s^2 + \frac{R_d}{L_d}s + \frac{1}{L_d C_d}\right)} - \frac{\frac{B}{L_d}\left(T_f - T_r\right)e^{-sT_r}}{\left(s^2 + \frac{R_d}{L_d}s + \frac{1}{L_d C_d}\right)} \right\} \quad (2\text{-}13)$$

Fig. 2-26- Fig. 2-27 show that the experimentally characterized snubber currents are nearly matching with analytically evaluated snubber currents for different snubber values during turn-on.



(a)



(b)

Fig. 2-26: Analytical and experimental Snubber current contribution from snubber across device under switching $R_d < 2\sqrt{\frac{L_d}{C_d}}$; (a) for R_dC_d: 22 nF,4.7 Ω; (b) for R_dC_d: 33 nF,4.7 Ω

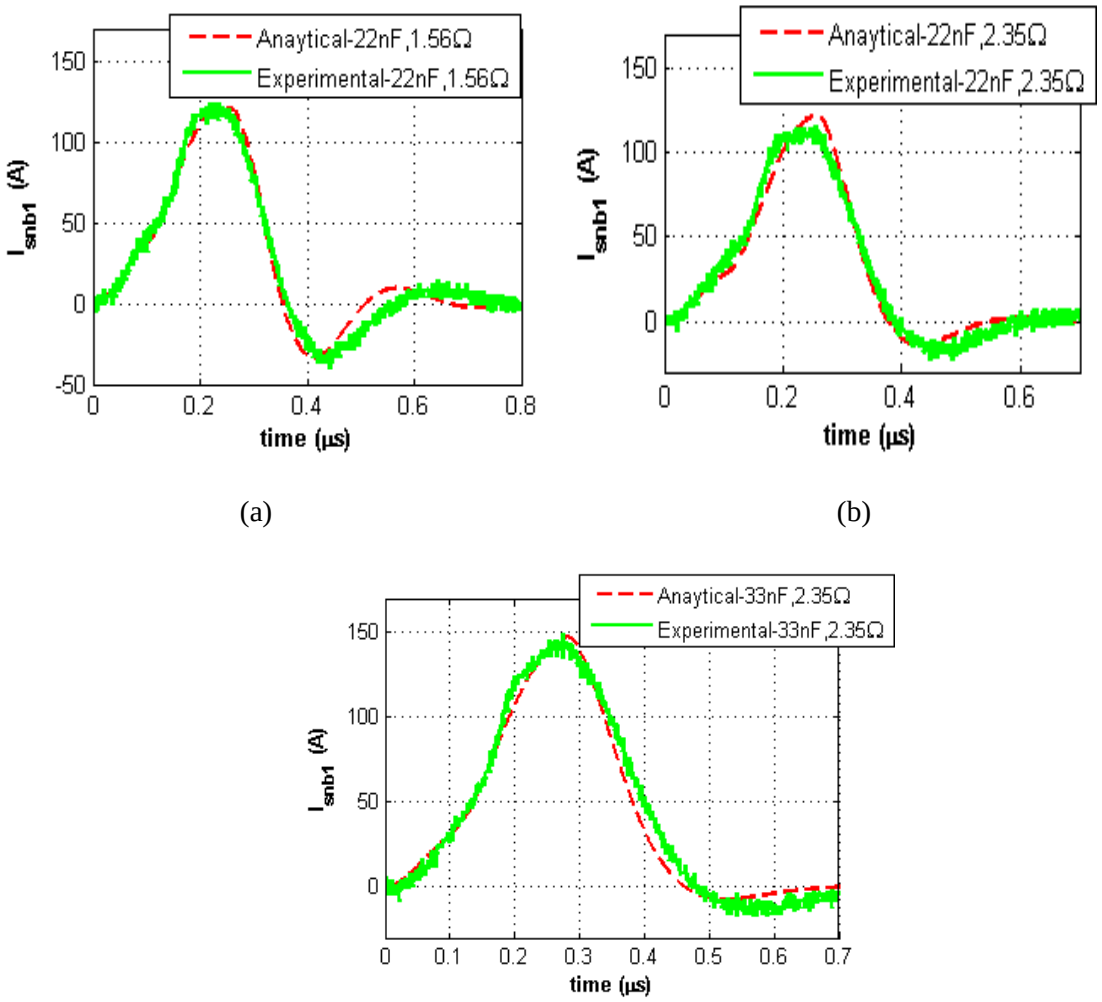


Fig. 2-27: Analytical and experimental Snubber current contribution from snubber across device under switching for $R_d < 2\sqrt{\frac{L_d}{C_d}}$; (a) for R_dC_d: 22 nF, 1.56 Ω; (b) for R_dC_d: 22 nF, 2.35 Ω; (c) for R_dC_d: 33nF, 2.35 Ω

2.6.1.2 Case 2: Snubber current contribution from snubber connected across the freewheeling device into device under switching - during turn-on

To derive the snubber current (i_{snb2}) during turn-on, KVL is applied across the V_{dc} – L_s- freewheeling snubber ($R_dC_dL_d$) - V_{ds1} Fig. 2-24 (b)). The resultant equation is shown in (2-14), and the DUT voltage (V_{ds1}) is given by (2-15). $V_{ds1}(t)$ has been realized using step function in (2-8) and the

corresponding $V_{ds1}(s)$ can be extracted from(2-12) and it is given in (2-16). Substituting (2-16) in (2-14) gives $i_{snb2}(s)$ as shown in (2-17) and $i_{snb2}(t)$ is given in (7-3) (Appendix).

$$\left\{\begin{array}{l} V_{dc}-\left(L_d+L_s\right)\dfrac{di_{snb1}(t)}{dt}\text{-}R_d\ i_{snb2}(t)\text{-}\dfrac{1}{C_d}\int i_{snb2}(t)\,dt\text{-}V_{ds1}(t)=0\ ; \\ \left(sL_{ds}+R_d+\dfrac{1}{C_d s}\right)i_{snb2}(s)+\dfrac{V_{Cd1}(T_r)}{s}=\dfrac{V_{dc}}{s}\text{-}V_{ds1}(s); \\ L_{ds}=\left(L_d+L_s\right);\ i_{snb1}(T_r)=0;\ \text{and}\ V_{Cd1}(T_r)=0, \\ \text{because freewheeling diode conducts until } t=T_r; \end{array}\right\} \quad (2\text{-}14)$$

$$V_{ds1}(t)=\left\{\begin{array}{l} 0 \quad t<T_r\ ; \\ \left(\dfrac{V_{dc}\text{-}L_s k}{T_f\text{-}T_r}\right)\left(T_f\text{-}t\right)\ \text{for}\ T_r\le t<T_f\ ; \\ 0 \quad t\ge T_f\ ; \end{array}\right\} \quad (2\text{-}15)$$

$$\left\{V_{ds1}(s)=\frac{B(e^{-sT_f}\text{-}e^{-sT_r})}{s^2}+\frac{B(T_f\text{-}T_r)}{s}e^{-sT_r};\ B=\left(\frac{V_{dc}\text{-}L_s k}{T_f\text{-}T_r}\right);\right\} \quad (2\text{-}16)$$

$$i_{snb2}(s)=\frac{\dfrac{V_{dc}}{L_{ds}}}{\left(s^2+\dfrac{R_d}{L_{ds}}s+\dfrac{1}{L_{ds}C_d}\right)}-\frac{\dfrac{B}{L_{ds}}\left(e^{-sT_f}\text{-}e^{-sT_r}\right)}{s\left(s^2+\dfrac{R_d}{L_{ds}}s+\dfrac{1}{L_{ds}C_d}\right)}-\frac{\dfrac{B}{L_{ds}}\left(T_f\text{-}T_r\right)e^{-sT_r}}{\left(s^2+\dfrac{R_d}{L_{ds}}s+\dfrac{1}{L_{ds}C_d}\right)} \quad (2\text{-}17)$$

2.6.1.3 Case 3: Snubber current flowing into the snubber connected across the DUT and Freewheeling device during turn-off

To analyze the snubber current during turn-off, the flow of load current through the device and R_dC_d snubber at different sub-intervals have been marked as shown in Fig. 2-28 (a)-(c). The experimental snubber current for different intervals during turn-off is given in Fig. 2-29.

During turn-off, the governing equation of phase leg with snubber are represented by (7-4) to (7-6) using Fig. 2-28(a)-(c) for different sub-intervals ($0\ \le t<T_f$, $T_f\ \le t<T_c$, $t\ge T_c$).

Applying Laplace transform for (7-4) to (7-6) and simplifying gives $i_{snb1}(s)$ (7-7) to (7-9). The corresponding '$i_{snb1}(t)$' is shown in (7-10) to (7-12).

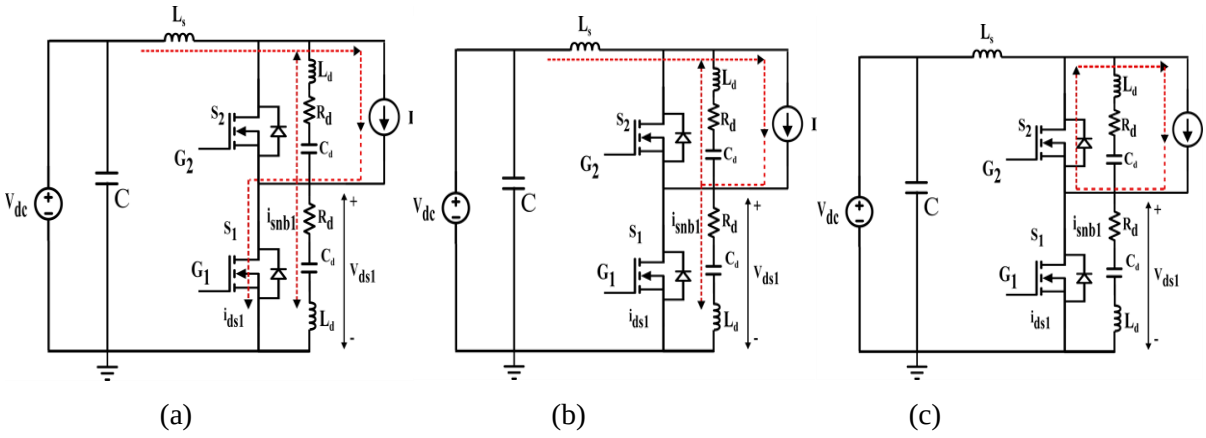


Fig. 2-28: The turn-off device current and snubber for different sub-interval (a) $0 \le t < T_f$; (b) $T_f \le t < T_r$; (c) $t \ge T_c$

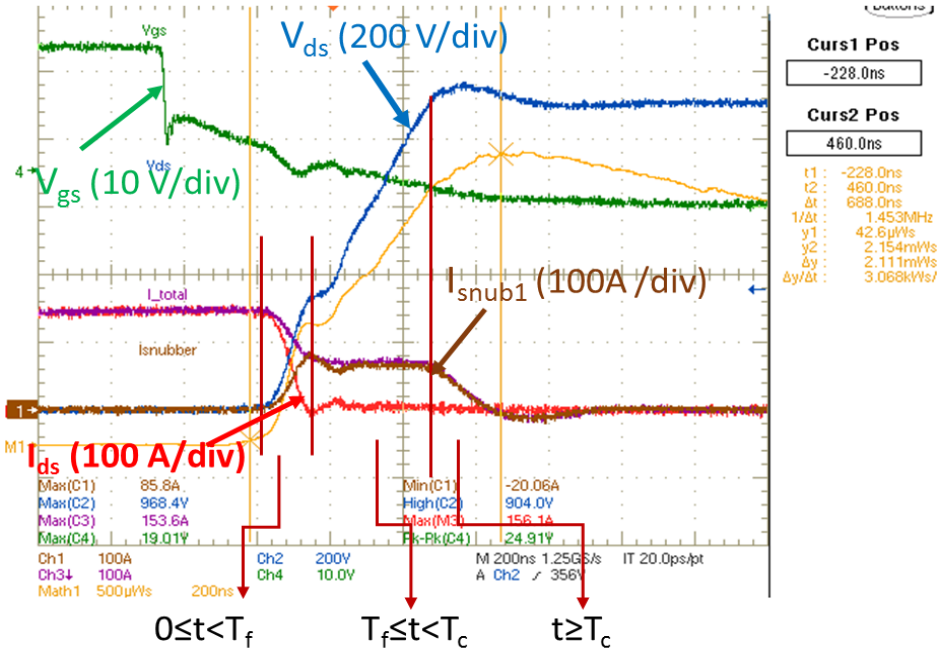


Fig. 2-29: Turn-off transition of 1.7 kV SiC MOSFET showing the snubber current transition at different sub-intervals at 900 V, 150 A, R_g=4.7 Ω

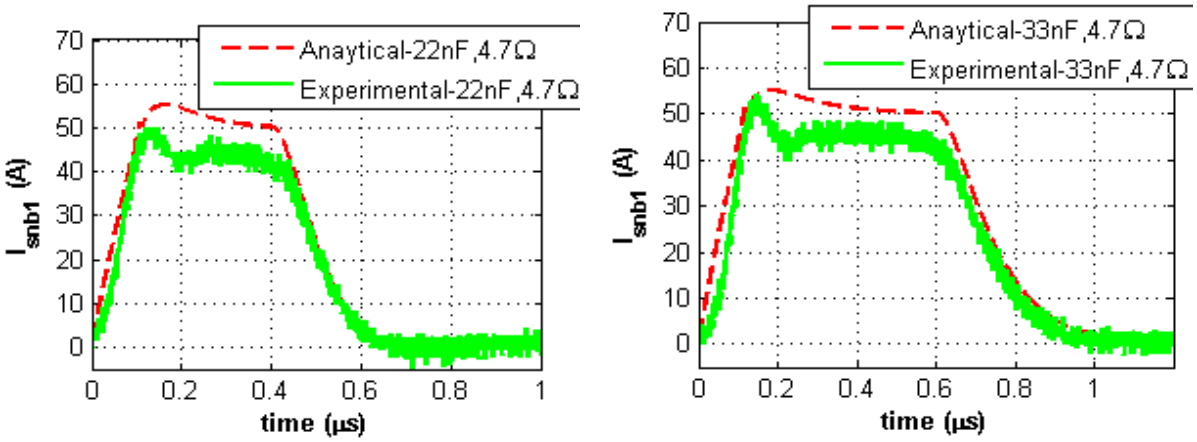
Snubber current '$i_{snb1}(t)$' during turn-off is the sum of sub-interval equations (7-10) to (7-12) and it is given by (2-18).

$$i_{snb1}(t) = i_{snb1}(0 < t < T_f) + i_{snb1}(T_f < t < T_c) + i_{snb1}(t > T_c);$$
$$i_{snb1}(t) = i_{snb2}(t); \quad (2\text{-}18)$$

The parameters I (load current), L_s are known parameters for a given DC bus design and the parameter 'T_f'(current fall time) is also known for a given value of turn-off gate resistance (R_{goff}). The parameter 'T_c' (Charging time (T_c)-Voltage across the snubber to reach 'V_{dc}') is the known value for a given snubber capacitor value and turn-off load current. It is given by (2-19) (parasitic snubber inductance (L_d) has been neglected to reduce the complexity.) Therefore the analytical turn-off snubber current '$I_{snb1}(t)$' given by (2-18) and turn-off snubber resistor losses can be evaluated for different snubber values R_dC_d using MATLAB.

$$T_c = \frac{2C_d V_{dc}}{I} + \frac{T_f}{2} - R_d C_d \quad (2\text{-}19)$$

Fig. 2-30-Fig. 2-31 show that the experimentally characterized snubber currents are nearly matching with analytically evaluated snubber currents for different snubber values during turn-off. The snubber current expression derived in 'case 1- case 3 ' will be useful to determine the RMS value of snubber currents (both DUT snubber, freewheeling snubber) and their corresponding snubber resistor losses.



(a) (b)

Fig. 2-30: Analytical and experimental Snubber current flowing into the snubber across device during turn-off for $R_d > \sqrt{L_{dds}/C_d}$; (a) for R_dC_d: 22 nF, 4.7 Ω; (b) for R_dC_d: 33 nF, 4.7 Ω

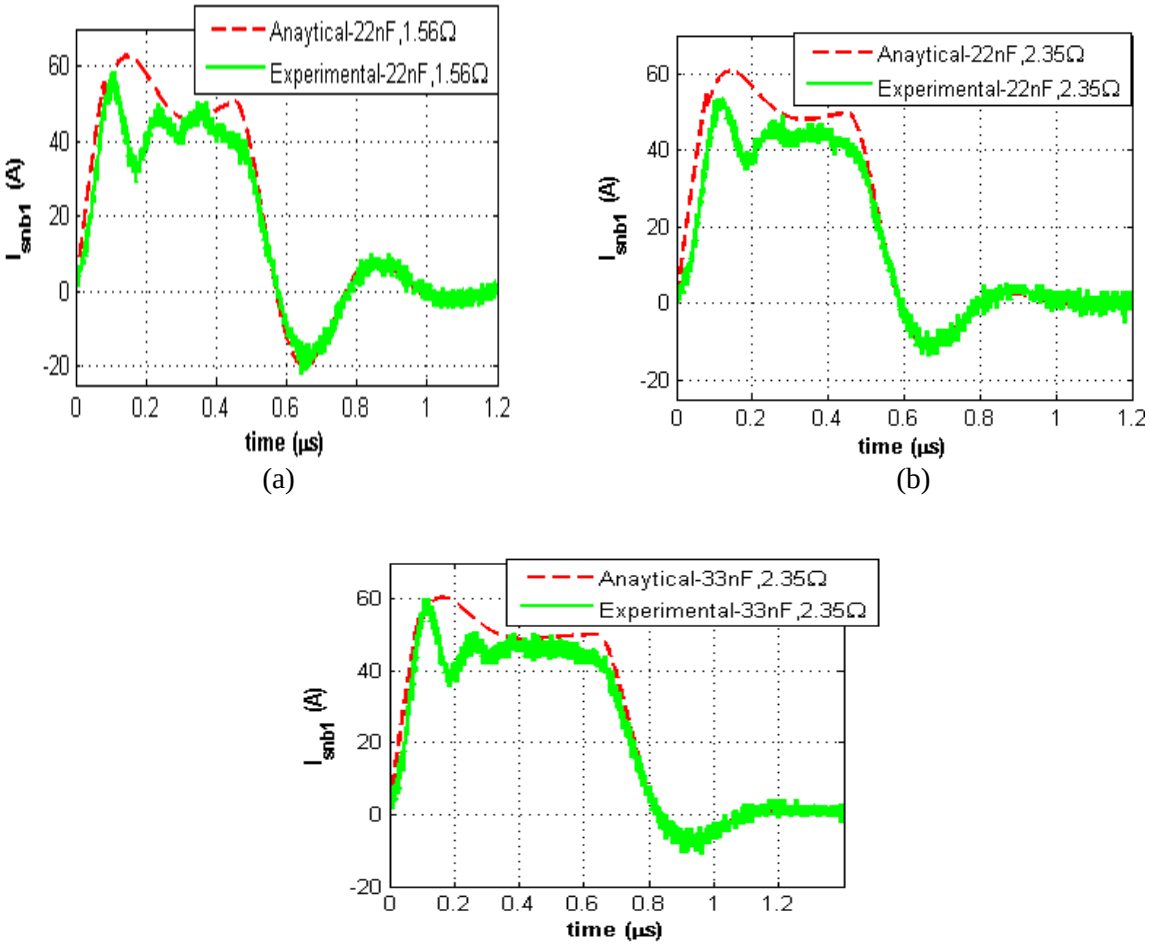


Fig. 2-31: Analytical and experimental Snubber current flowing into the snubber across device during turn-off for $R_d < \sqrt{L_{dds}/C_d}$;(a) for R_dC_d: 22 nF, 1.56 Ω; (b) for R_dC_d: 22 nF, 2.35 Ω; (c) for R_dC_d: 33 nF, 2.35 Ω

2.7 Experimental demonstration of series connected devices

This section presents the experimental results with series connected 1.7 kV SiC MOSFETs in different configurations such as (i) DC –AC full bridge Inverter (two devices per arm); (ii) DC-AC half bridge Inverter (four devices per arm); and (iii) DC-DC buck converter with four devices per arm. The snubber value (R_dC_d) used in all the experiments is 33 nF, 1.56 Ω, and the gate resistance (R_{gon}=R_{goff}) = 4.7Ω. The 1.7 kV SiC modules are mounted on a heat sink (part no: 476400U00220G from Aavid Thermalloy) and forced air-cooling is used. The setup shown in Fig. 2-8 is reconfigurable for performing above experiments.

2.7.1 DC –AC full bridge converter with two 1.7 kV SiC MOSFET devices per arm

The full bridge inverter configuration as shown in Fig. 2-32 with two series connected devices per arm is used with an R-L load. The dc bus has been kept at 1800V such that the devices are loaded with rated nominal operating voltage (900V across each), and the converter is operated at different loads, different switching frequencies and fundamental frequencies. The converter is operated for 10 to 15 min to allow the heat sink temperature to stabilize. The summary of converter operating points, the measured heat sink temperatures (from thermos-couples) and the estimated junction temperature of the modules have been listed in Table 2-7. The junction temperature of modules has been estimated using (2-20); where, the '$R^{th}_{(H-A)}$' is the thermal resistance of heat sink to ambient (0.028^0C/W–from datasheet of heat sink), the '$R^{th}_{(J-C)}$' is the thermal resistance of junction to case(0.07^0C/W– from datasheet of the module) , and the '$R^{th}_{(C-H)}$' is the thermal resistance of case to heat due to thermal interface compound (0.05^0C/W), 'P_{disp}' is the power dissipation in the module, T_A, T_H, T_j are ambient heat sink and junction temperatures respectively.

$$P_{disp} = \frac{T_H - T_A}{R^{th}_{H-A}}; \qquad T_j = \left(P_{disp} \cdot (R^{th}_{J-C} + R^{th}_{C-H})\right) + T_H; \quad (2\text{-}20)$$

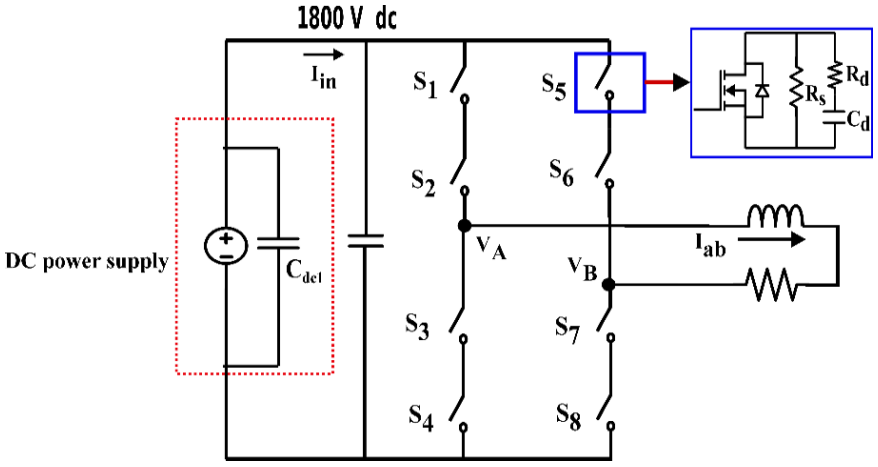


Fig. 2-32: Experimental schematic of DC-AC full bridge inverter

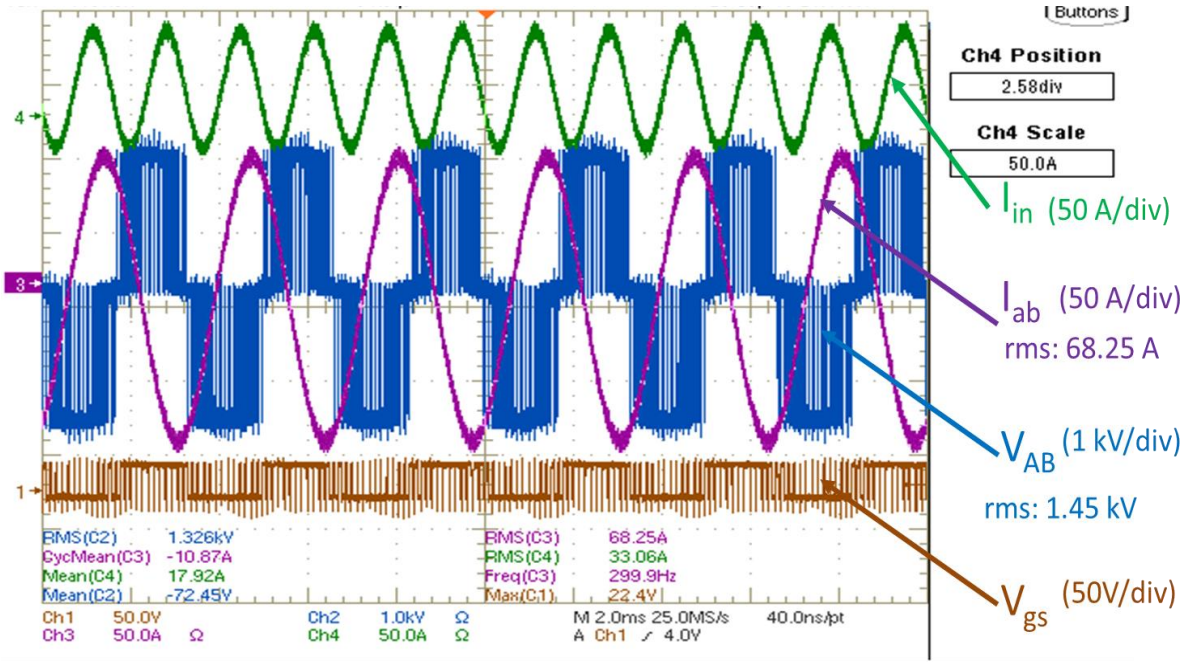
From Table 2-7 the rise in heat sink temperature and the calculated junction temperature (T_j) of the devices in the series connection operation shows that for switching frequencies below 8 kHz, the devices have enough margin for the junction temperature to reach 150^0C and therefore these devices can be loaded up to its rated current of 225 A. However, for switching frequencies $f_{sw} \geq 10$ kHz and

f_m =1kHz, the device junction temperature is very close to the thermal packing limit of 150^0C. Therefore, the devices have to be de-rated with the present snubber values.

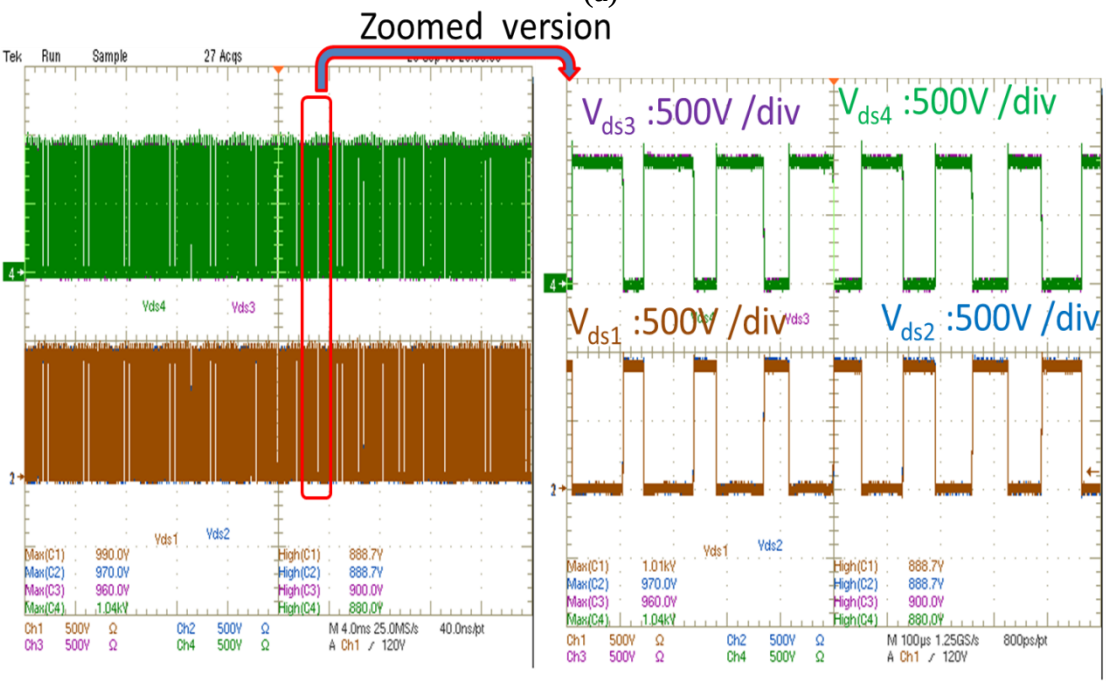
Table 2-7: Summary of full bridge test at different operating conditions with two series 1.7 kV connected devices

V_{dc}	f_s	f_m	m	(I_{ab})	R-L load	S_{out}	T_H	T_A	ΔT_{H-A}	T_j
1.8kV	5 kHz	60Hz	0.45	80 A	7.7mH, 6.25 Ω	45 kVA	^{0}43 C	^{0}27.8 C	^{0}15.2 C	^{0}75.57 C
1.8kV	7.5 kHz	500 Hz	0.9	80 A	3.3 mH, 6.25 Ω	92 kVA	^{0}47.2 C	^{0}23 C	^{0}24.2 C	^{0}99.05 C
1.8kV	8 kHz	720 Hz	0.955	66 A	3.3 mH, 6.25 Ω	80 kVA	46 ^{0}C	22^{0}C	24^{0}C	^{0}97.43 C
1.8kV	10 kHz	1 kHz	0.6	95 A	0.054 mH, 6.25 Ω	76 kVA	^{0}62 C	^{0}24 C	^{0}38 C	^{0}143.42 C

Therefore, the switching frequency limits per device are nearly 7.5 kHz - 8 kHz from the above experiments without derating of the current rating of the devices with C_dR_d:33nF 1.65Ω. These switching frequency limits will be same even if 'n' number of devices are connected in series for MV or HV applications. Fig. 2-33-Fig. 2-34 show the full-bridge experimental results with two series connected devices at f_{sw}=7.5 kHz f_m=300 Hz and 500Hz respectively. Fig. 2-35- Fig. 2-36 show the full-bridge experimental results with two series connected devices at f_{sw}=10 kHz f_m=1000 Hz and f_{sw}=15 kHz f_m=1000 Hz respectively.

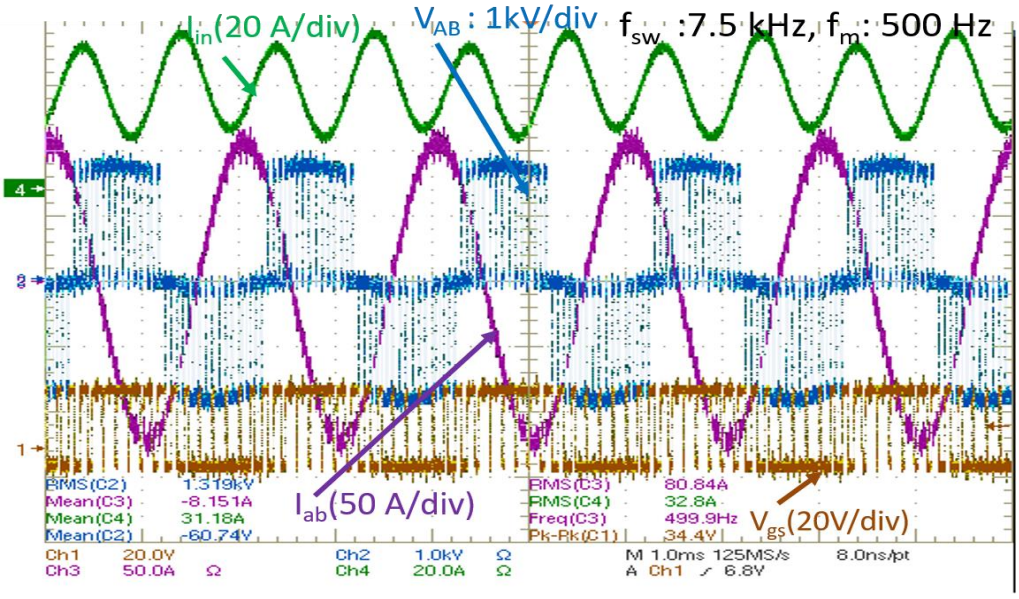


(a)



(b)

Fig. 2-33: (a) Shows the input current (I_{in}), Output AC voltage(V_{AB}), AC current (I_{ab}), and one of low side MOSFET gate voltage in DC-AC operation with two series connected 1.7 kV MOSFET devices per arm of full-bridge at 7.5 kHz, 1800 V input DC, modulation index of 0.9, AC load peak current of 96 A (300 Hz) and nearly 82 kVA load; (b) Shows the voltage across four devices in a phase leg pole; (b) The voltage across four devices in a phase leg pole for the same operating condition



(a)

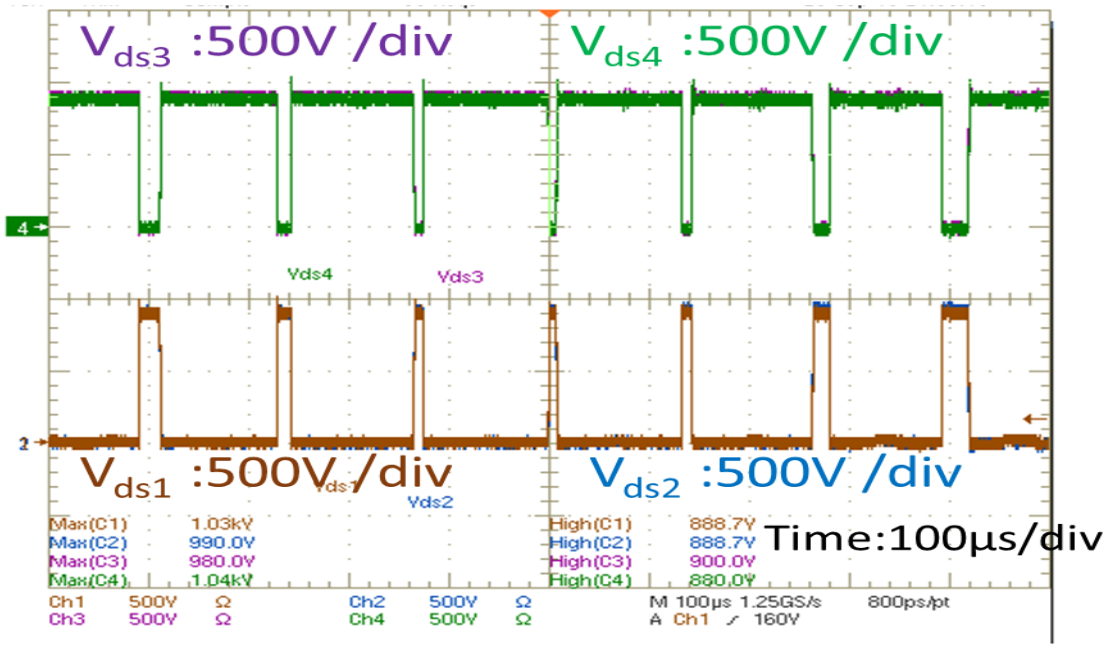
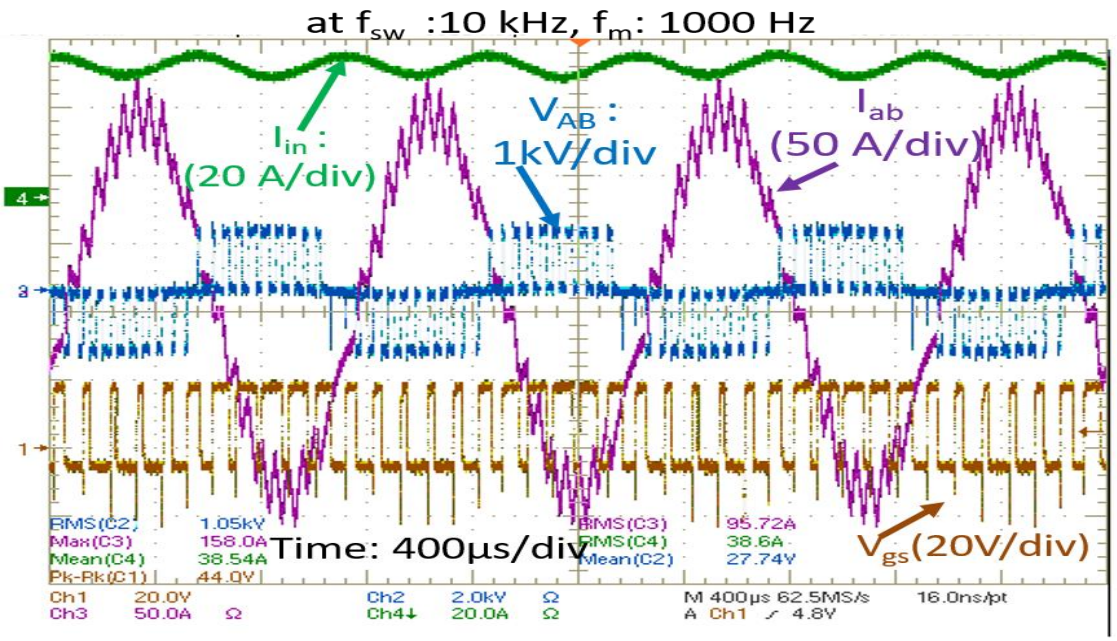
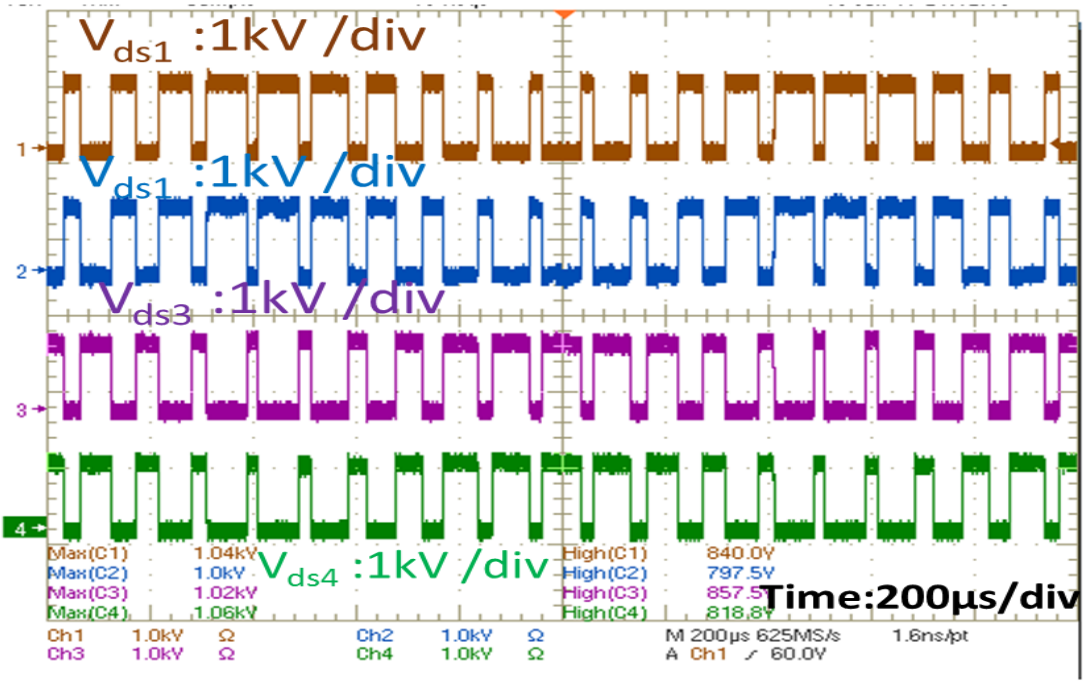


Fig. 2-34: (a) Input current (I_{in}), Output AC voltage(V_{AB}), AC current (I_{ab}), and one of low side MOSFET gate voltage (s_4) in DC-AC operation with two series connected 1.7 kV MOSFET devices per arm of full-bridge at 1800 V input DC, m=0.9, f_{sw} =7.5 kHz, f_m=500 Hz, AC current (I_{ab}) =80 A (rms) and nearly 92 kVA load; (b) The voltage across four devices in a phase leg pole for the same operating condition

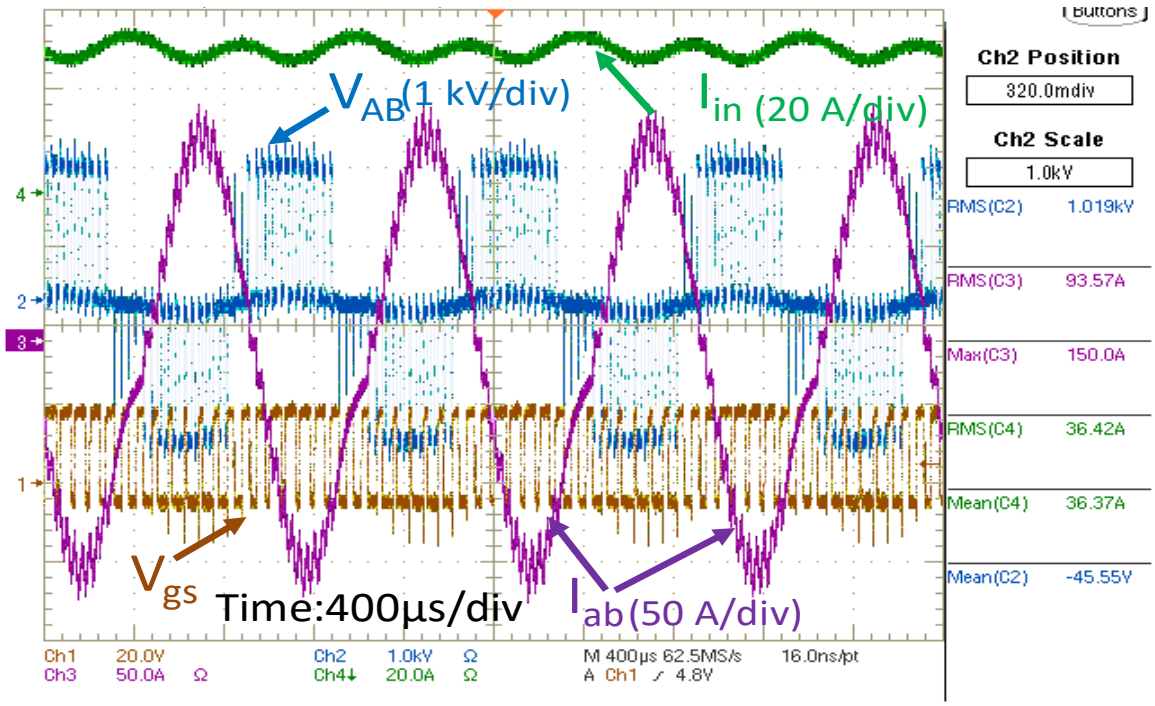


(a)

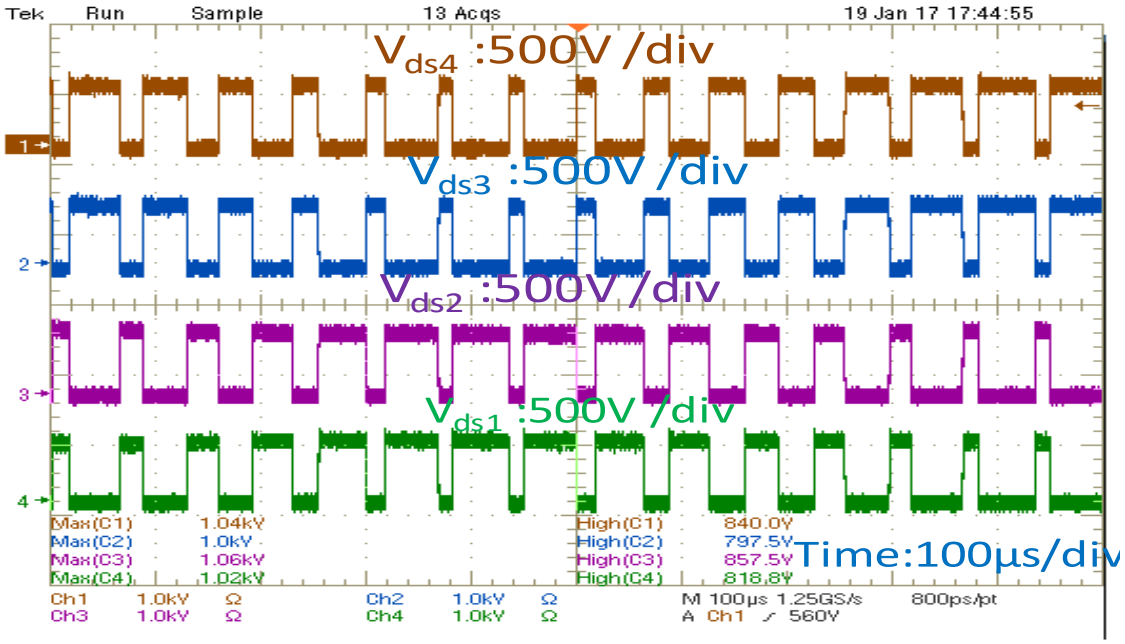


(b)

Fig. 2-35: Input current (I_{in}), Output AC voltage(V_{AB}), AC current (I_{ab}), and one of low side MOSFET gate voltage (s_4) in DC-AC operation with two series connected 1.7 kV MOSFET devices per arm of full-bridge at 10 kHz, 1800 V input DC, m=0.6, f_{sw} =10 kHz, f_m=1000 Hz, AC current (I_{ab}) =95 A (rms) and nearly 76 kVA load; (b) The voltage across four devices in a phase leg pole for the same operating condition



(a)



(b)

Fig. 2-36: (a) Input current (I_{in}), Output AC voltage(V_{AB}), AC current (I_{ab}), and one of low side MOSFET gate voltage (s_4) in n DC-AC operation with two series connected 1.7 kV MOSFET devices per arm of full-bridge at f_{sw} :15 kHz, 1800 V input DC, AC load peak current of 150 A (f_m :1000 Hz) (nearly 76 kVA); (b) V_{ds1},V_{ds2} ,V_{ds3},V_{ds4}: Voltage across series connected devices in one phase leg of H-bridge converter

2.7.2 Experimental results of phase leg in a DC –AC half-bridge converter.

This section presents the experimental results of series connected 1.7 kV SiC MOSFETs in a DC – AC half-bridge converter. The half bridge inverter configured (one-phase leg pole of the three-phase converter) with four series-connected devices per arm shown in Fig. 2-37 with an R-L load. The experimental setup shown in Fig. 2-8 is re-configured for DC-AC half-bridge inverter operation. Since the switching frequency limits of each 1.7 kV SiC MOSFET with external RC snubber has been between 7.5 kHz to 8 kHz from the previous full bridge results. Therefore, the half-bridge experiments have been conducted at 7.5 kHz with different fundamental frequencies but at a higher DC bus (V_{dc}) voltages than the full bridge as listed in Table 2-8. An air core inductor (L) and resistive bank (R) are used for the load to test the converter. The variation of measured load inductance value for the air core inductor with different fundamental frequencies is also shown in Table 2-8.

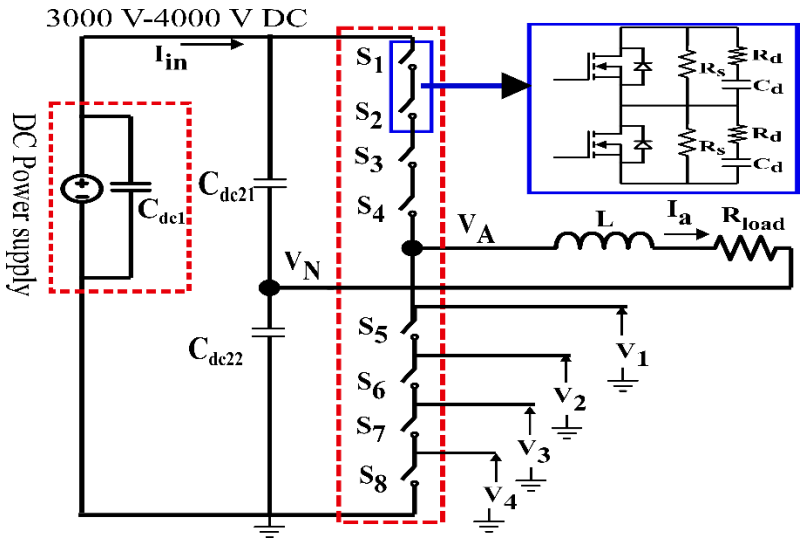


Fig. 2-37: Experimental schematic of DC-AC half-bridge inverter

Table 2-8: Summary of half- bridge tests at different operating conditions with four series 1.7 kV connected devices

V_{dc}	f_{sw}	f_m	m	I_a (rms)	R-L Load	Output power
3 kV	7.5 kHz	60 Hz	0.75	111 A	L=5.8 mH,0.16 Ω R=6.25 Ω	88 kVA
3 kV	7.5 kHz	300 Hz	0.95	78 A	L=5 mH,0.5 Ω R=6.25 Ω	78 kVA
3 kV	7.5 kHz	500 Hz	0.9	48 A	L=4.95 mH,2.3 Ω R=6.25 Ω	45 kVA

Fig. 2-38-Fig. 2-40 show the DC-AC half-bridge inverter operation with four series-connected devices per arm at 3000 V DC bus, f_{sw}=7.5 kHz and at different fundamental frequencies (60Hz-500Hz). Since the R-L load is same for all three cases, the output phase current is less at higher fundamental frequencies. It is because the load inductance offers higher impedance at those fundamental frequencies. The input current (I_{in}) from DC power supply unit contains AC (ripple) component as shown in Fig. 2-38-Fig. 2-40. It is because, the DC capacitor (C_{dc1}) from the power supply also supplies part of reactive current to the load along with external DC film capacitors (C_{dc21}, C_{dc22}).

Fig. 2-41-Fig. 2-42 show voltage across four SiC MOSFET devices w.r.t ground in a phase-leg arm at 3 kV dc bus, f_{sw}=7.5 kHz at f_m=300Hz-500Hz. The voltage imbalance across each device is less than 10% of rated base voltage (V_{dc}/4, i.e=750 V) during the continuous switching operation also.

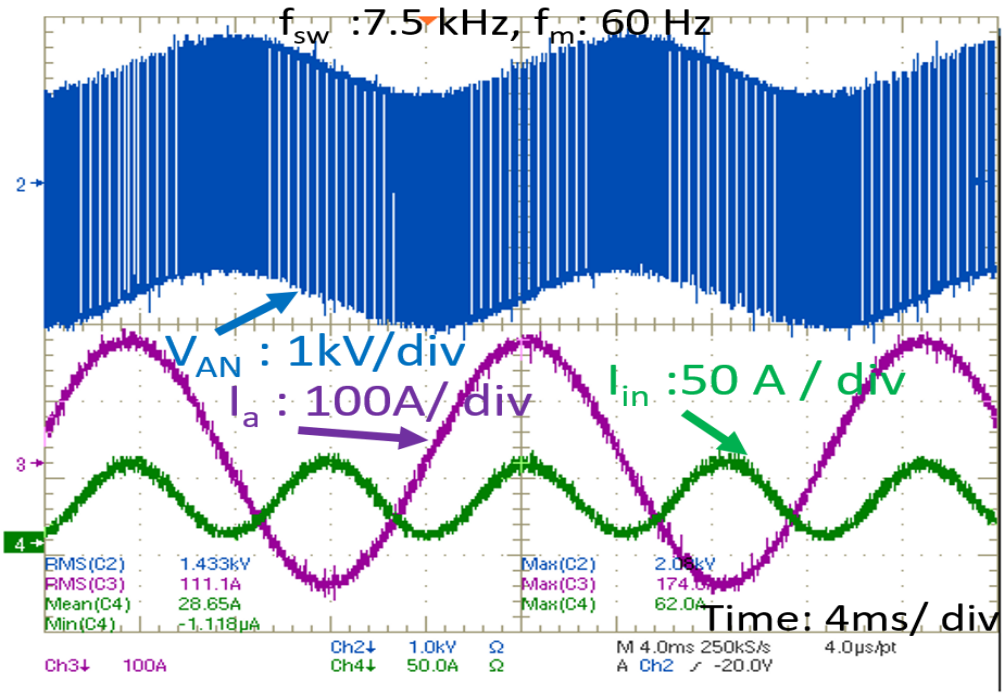


Fig. 2-38: Input current (I_{in}), Output Phase voltage(V_{AN}), Phase current (I_a), with four series-connected 1.7 kV MOSFET devices per arm of half-bridge Inverter at 3000 V input DC, f_{sw}=7.5 kHz, m= 0.75, f_m=60Hz, Phase current (I_a) =111 A (rms) and nearly 88 kVA load

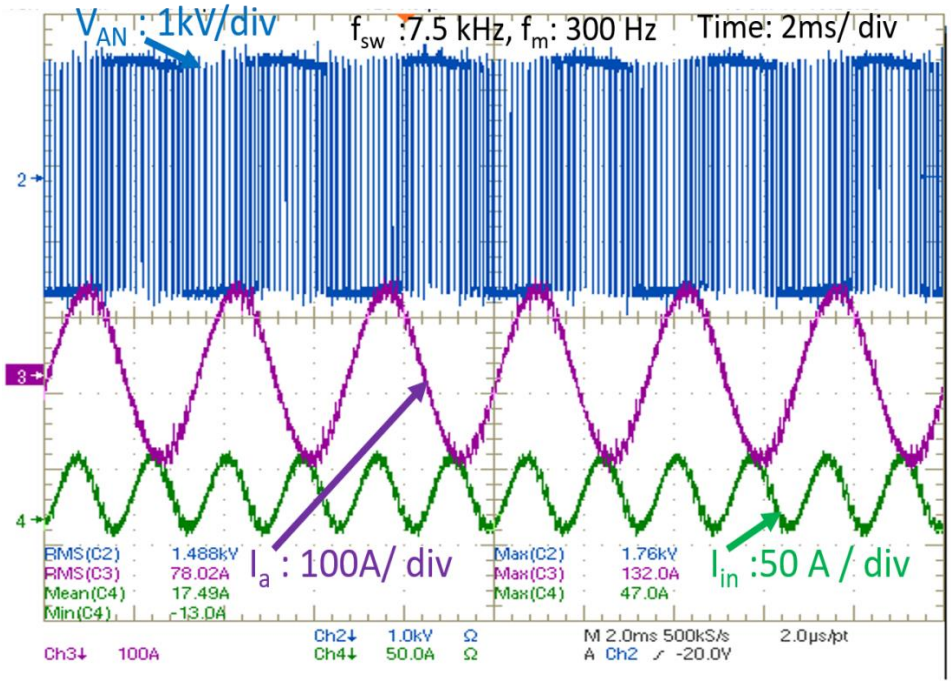


Fig. 2-39: Input current (I_{in}), Output Phase voltage(V_{AN}), Phase current (I_a), with four series-connected 1.7 kV MOSFET devices per arm of half-bridge Inverter at 3000 V input DC, f_{sw}=7.5 kHz, m= 0.95, f_m=300 Hz, Phase current (I_a) =78 A (rms) and nearly 78 kVA load

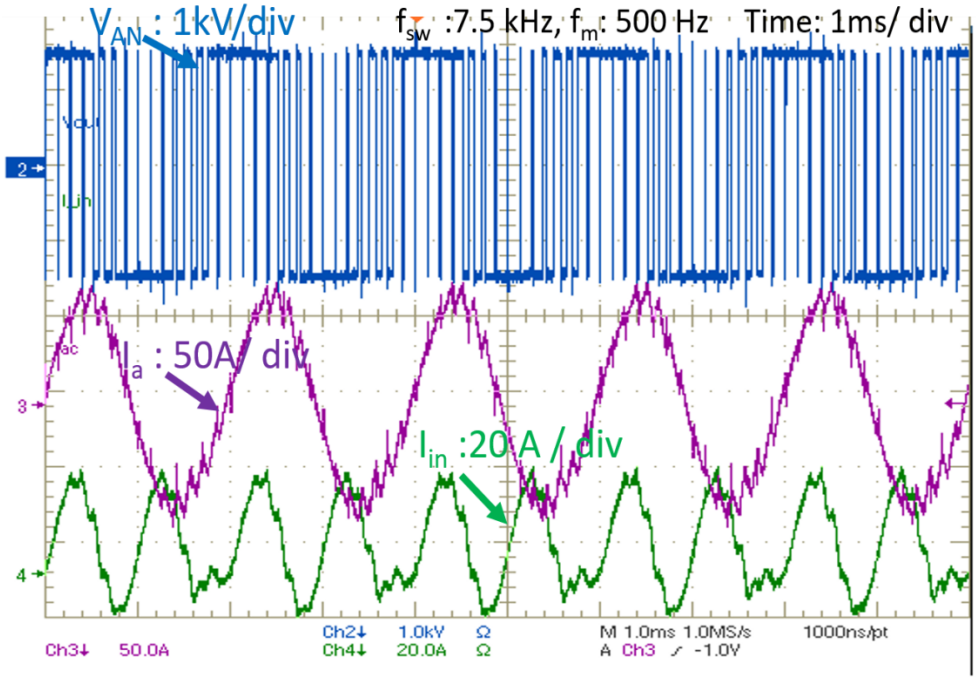


Fig. 2-40: Input current (I_{in}), Output Phase voltage(V_{AN}), Phase current (I_a), with four series-connected 1.7 kV MOSFET devices per arm of half-bridge Inverter at 3000 V input DC, f_{sw}=7.5 kHz, m= 0.9, f_m=500 Hz, Phase current (I_a) =48 A (rms) and nearly 45 kVA load

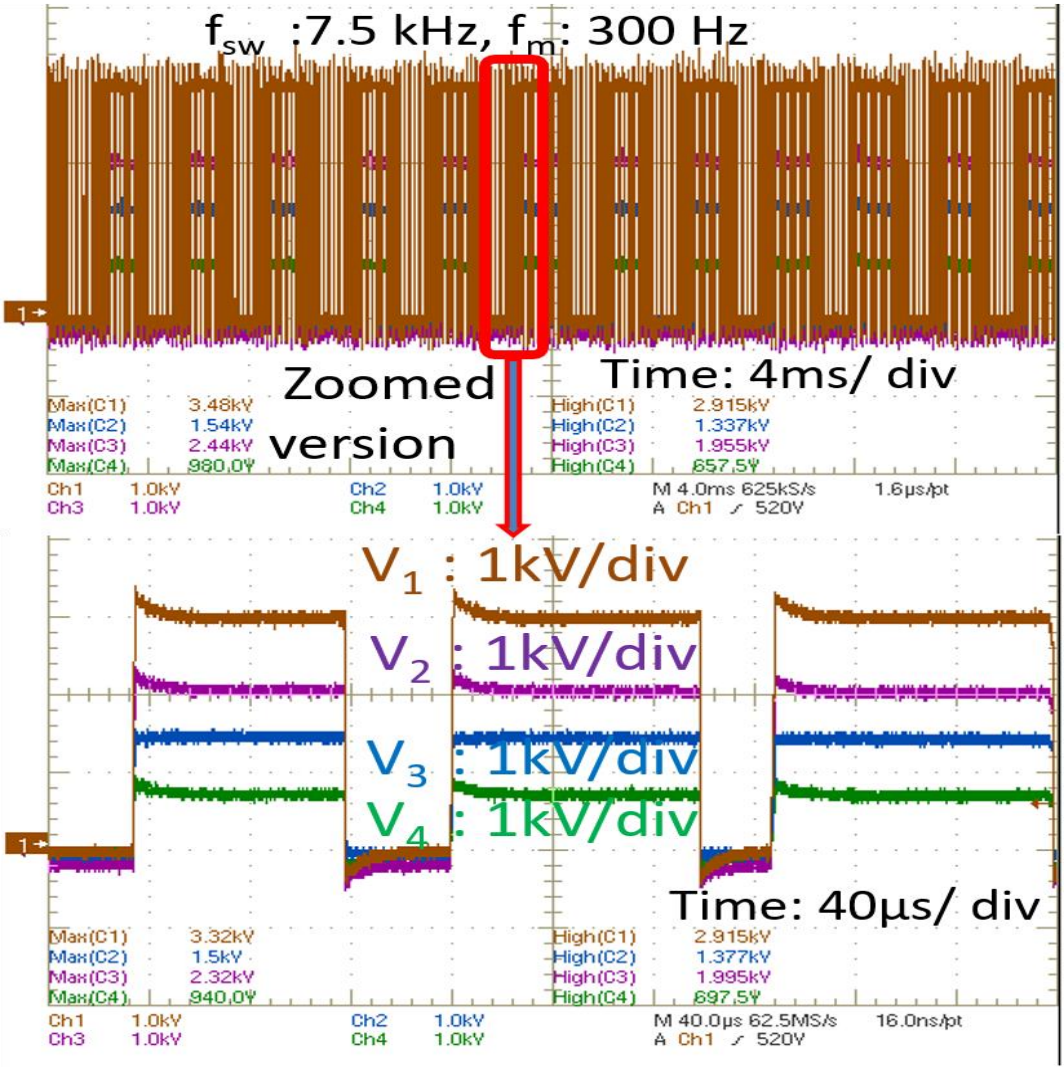


Fig. 2-41: The voltage across four SiC MOSFET devices w.r.t ground in a phase-leg arm at 3 kV dc bus, f_{sw}=7.5 kHz, m= 0.95, f_m=300 Hz, Phase current (I_a) =78 A (rms) and nearly 78 kVA load

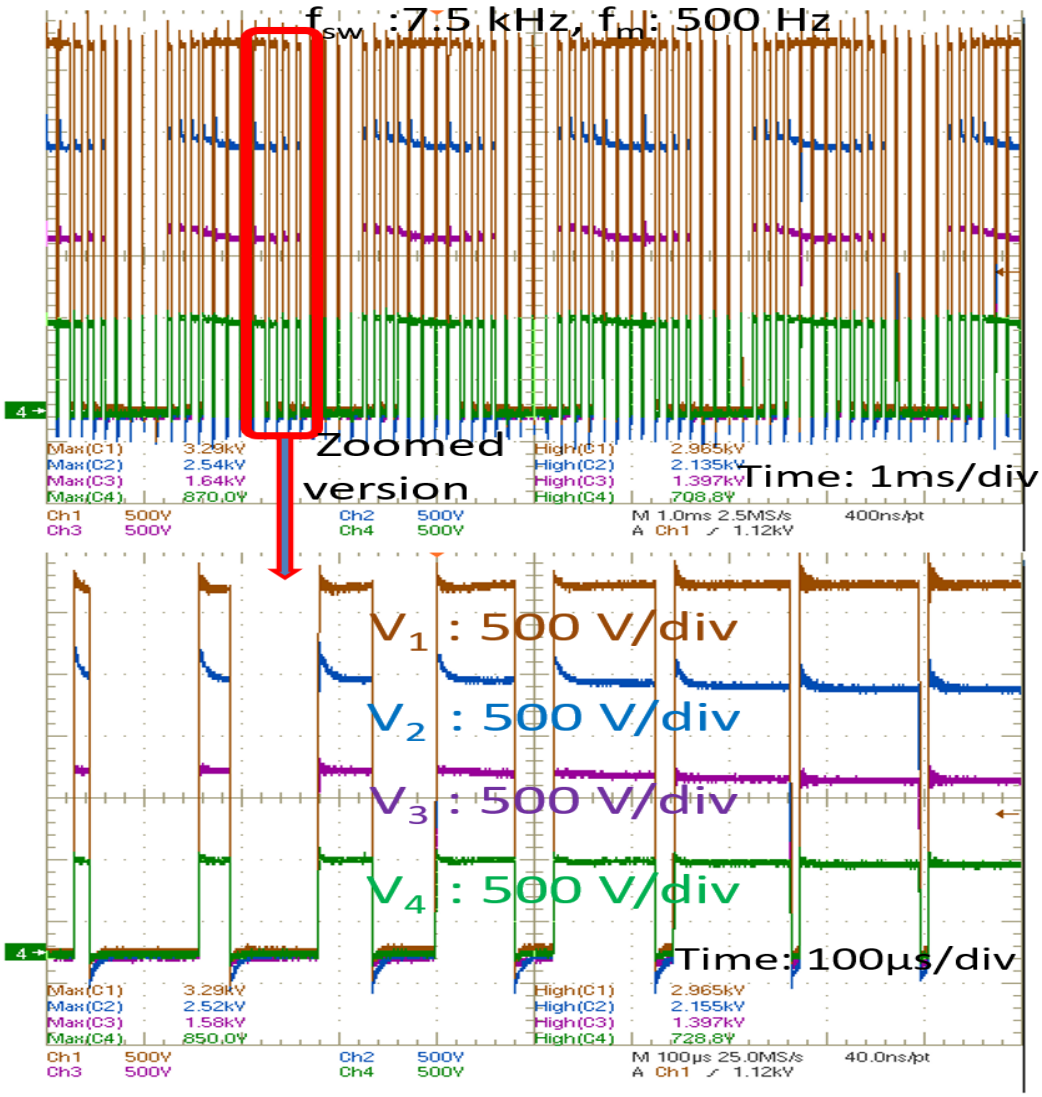


Fig. 2-42: The voltage across four SiC MOSFET devices w.r.t ground in a phase-leg arm at 3 kV dc bus, f_{sw}=7.5 kHz, m= 0.9, f_m=500 Hz, Phase current (I_a) =48 A (rms) and nearly 45kVA load

2.7.3 Endurance test of a phase–leg in a DC-DC converter

The DC-AC full bridge experimental results (from section A) showed the switching frequency limits of each 1.7 kV SiC MOSFET with external snubber can be 7.5kHz-8 kHz at rated operating voltage of 900V across each. However, it has not been tested at full current rating (The device is rated to operate at 225 A at T_{case}=90^{0}C from the datasheet.) due to the limitation of non-availability of AC load at high current in the lab. However, there is a DC load of nearly 100kW at 600V.Therefore an attempt has been made to load the device near to its rated current by configuring phase leg converter

with four series-connected devices per arm as a DC-DC buck converter with input dc bus voltage of 3000V as shown in Fig. 2-43.

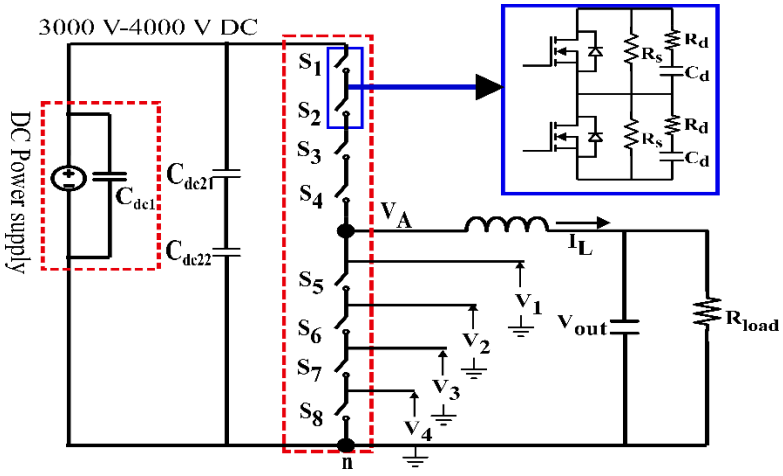


Fig. 2-43: Experimental schematic of DC-DC converter using four series-connected 1.7 kV SiC MOSFET per arm

Fig. 2-44 shows the waveforms of a DC-DC buck converter with four series-connected devices per arm at 3 kV DC, f_{sw}=7.5 kHz, duty ratio (D)= 0.2, I_L =180 A (mean), 200 A (peak) and 100 kW load; The converter has been run for 10 min. The measured heat sink temperature is nearly 60-62^{0}C and the calculated junction temperature is (T_j) ~140^{0}C-143^{0}C. Fig. 2-45 shows the voltage across each device w.r.t ground (for the bottom arm devices) for the same operating condition. The voltage imbalance across the devices is less than 10% of rated base voltage (V_{dc}/n=3000/4=750V across each).

The experiment results from section 2.7.1 to 2.7.3 validates that the 1.7 kV SiC MOSFET with external snubber can be used in series connection to make MV converter with switching frequency of 7.5 kHz without de-rating the voltage and current (rated nominal operating voltage: 900 V, rated current : 225 A). Also, feasibility to generate high fundamental frequencies up to 500 Hz to achieve high-speed operation up to 15000 rpm is shown, which cannot be achieved with the existing 4.5 kV-6.5 kV Si IGBT devices. The four series-connected SiC MOSFET devices can be operated up to 3600V dc bus in a two-level phase leg with nearly 900V across each device. This is equivalent to one single 6.5 kV Si IGBT (their rated nominal voltage: 3600V) with the similar current rating but with much better performance w.r.t switching frequency (f_{sw}) to enable high-speed MV drive applications.

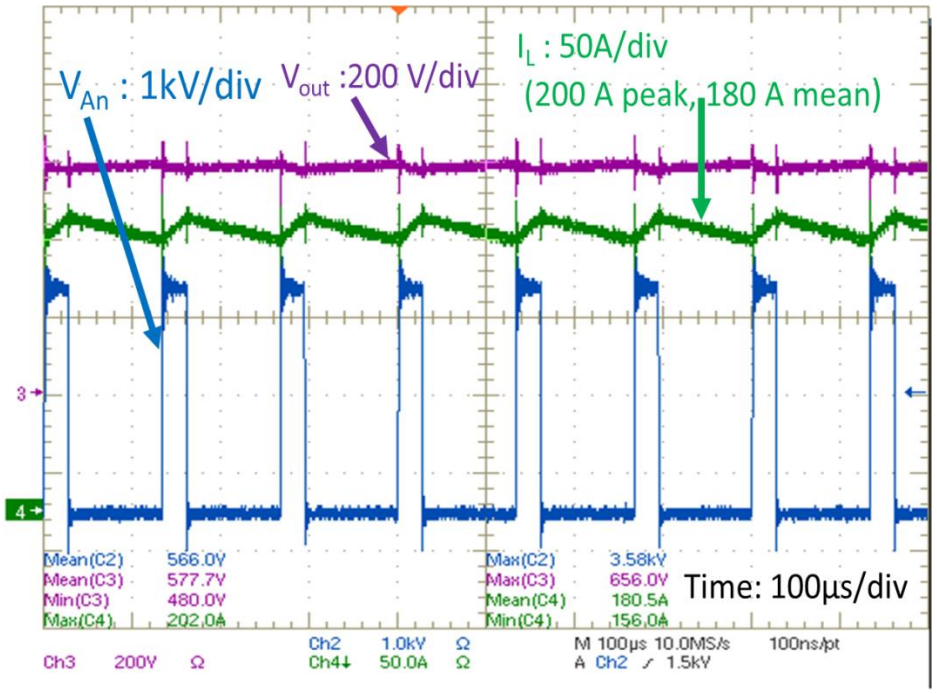


Fig. 2-44: Pole voltage (V_{An}), Inductor current (I_L),Output voltage(V_{out}) with four series-connected 1.7 kV MOSFET devices per arm at 3000 V input DC, f_{sw}=7.5 kHz, duty ratio (D)= 0.2, I_L =180 A (mean), 200 A peak and 100 kW load

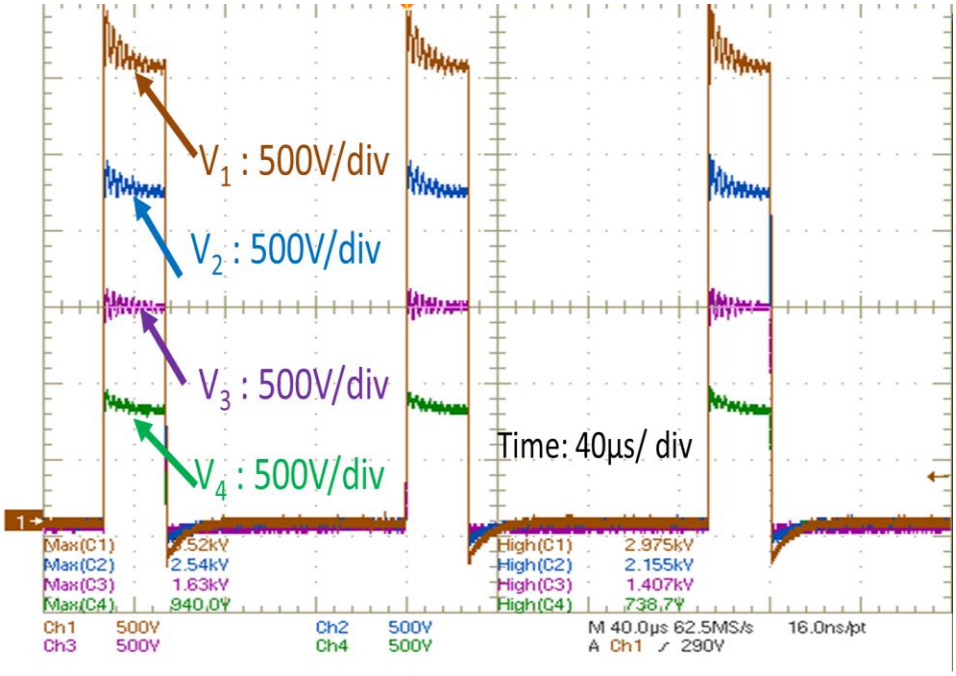


Fig. 2-45: The voltage across four SiC MOSFET devices w.r.t ground in a phase-leg arm at at 3000 V input DC, f_{sw}=7.5 kHz, duty ratio (D)= 0.2, I_L =180 A (mean), 200 A peak and 100 kW load

2.8 Power loss and Efficiency Evaluation of 3-ph MV VSD for different AC voltage (2.1 kV -13.2 kV)

To evaluate the MV converter efficiency using series-connected devices for any other operating conditions, (f_{sw}, V_{dc} (dc bus voltage), phase current, and load power factor, modulation index (m)), along with the switching loss data of SiC MOSFET (with RC snubber), conduction loss data is also required. Fig. 2-23 gives switching loss data per device. The total switching losses of SiC MOSFET do not change with temperature, therefore, the switching loss data shown in Fig. 2-23 can be used to estimate the converter switching losses for T_j=150^{0}C. The on-state resistance (R_{dson}) of SiC MOSFET does not change with external snubber in the series connection. Therefore, the R_{dson} data from the data sheet can be used to evaluate the conduction losses of SiC MOSFET.

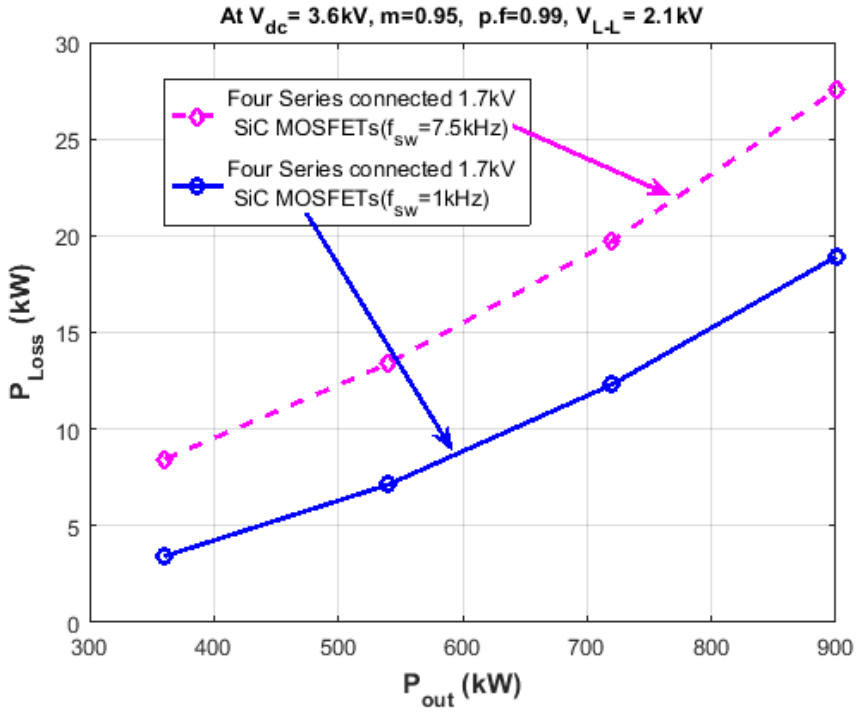


Fig. 2-46: Total loss comparison of MV, 3-ph, two-level VSI with four series-connected of 1.7 kV SiC MOSFETs at different loads at 3.6 kV DC, 2.1 kV AC (L-L)

Using the above switching loss and R_{dson} data in MATLAB/PLECS simulation tool, the total power loss (P_{loss}) of 3-phase, MV two-level voltage source Inverter (VSI) with series connected 1.7 kV SiC MOSFETs (four per arm) at different output power has been evaluated as shown in Fig. 2-46. **The efficiency of the converter at 720 kW load, f_{sw}=7.5 kHz is 97.33%.** The volume of the one phase-leg with four series-connected devices including an eight-channel gate driver, heat sink, fans, RC snubbers and DC link snubber capacitors is **"38.5cmx 36 cm x 24 cm"** (as in Fig. 2-8). **For the per phase**

power of 240 kW at 2.1 kV (L-L), 200 A rms, the power density of per phase-leg is 7.2 MW/m^3 (or 0.138 m^3/MW). The power density of 3-ph converter with such similar phase legs is also expected to same**.** If the same 3-ph converter is used for the front-end rectifier, the overall power density of VSD section (for front-end rectifier and VSI) will be 3.6 MW/m^3 (or 0.277 m^3/MW) excluding the DC bus capacitor size and 2.38 MW/m^3 (or 0.418 m^3/MW) including the DC bus capacitor size. The efficiency of front-end converter will be much higher than Inverter section as the front converter can be switched at lower 'f_{sw}'.

2.9 Comparison of Performance comparison of Si –IGBT and series connected 1.7 kV SiC MOSFET devices

The comparison of series connected 1.7 kV SiC MOSFET devices and 6.5 kV Si-IGBT has been evaluated as shown in Fig. 2-47. The 6.5 Si-IGBT (ABB 6.5kV Si IGBT: 5SNA 0400J6501) [35] has been taken for evaluation. The safe operating voltage of 6.5 kV Si-IGBT is 3600V. Four series connected 1.7 kV SiC MOSFET are required to compare with 6.5 kV Si-IGBT.

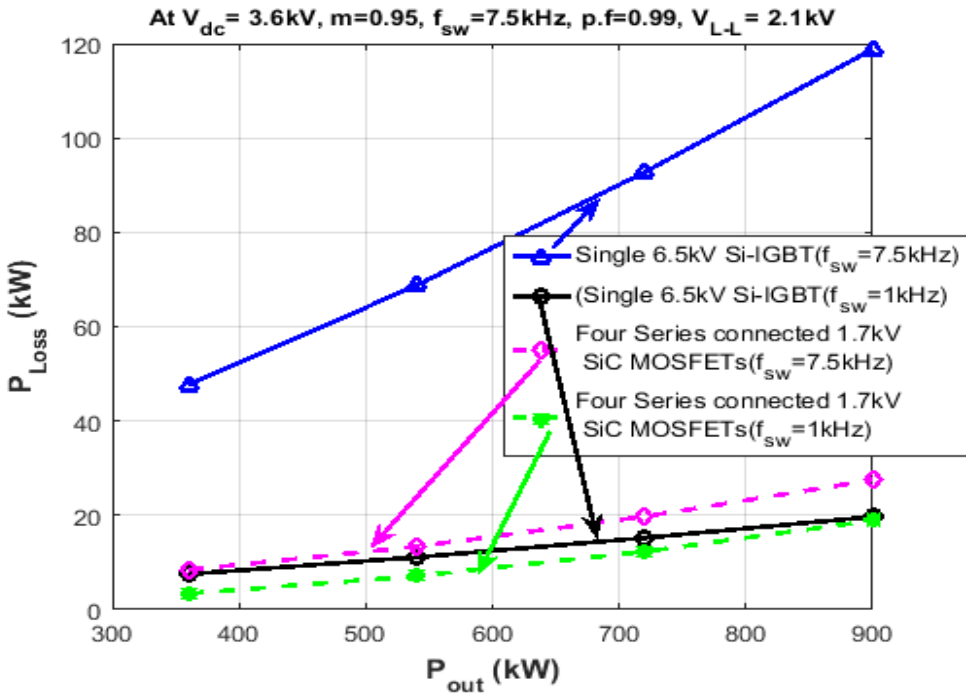


Fig. 2-47: Total loss comparison of 6.5 kV Si-IGBT with four series-connected 1.7 kV SiC MOSFETs at different loads at 3.6 kV DC, 2.1 kV AC (L-L)

Fig. 2-47 shows that the **four series-connected devices (1.7 kV SiC MOSFET) have nearly 4-6 times lower total loss compared to single 6.5 kV Si-IGBT at 7.5 kHz.** For '1 kHz' switching frequency, the total loss for four series-connected devices (1.7 kV SiC MOSFET) is comparable to 6.5 kV Si IGBT at higher output power, but it is **two times lower** at lower output power. Therefore, the series connection of 1.7 kV SiC MOSFETs also makes a significant impact on the efficiency of converter for low switching frequency (~ 1 kHz) applications such as front-end rectifier in the VSD unit. For switching frequencies below 1 kHz, the Si IGBT will be more favorable than the series connection of 1.7 kV SiC MOSFETs. It is because the majority of the total loss contribution is due to conduction losses compared to switching losses at low switching frequencies and the conduction losses for the Si IGBT is much less than series connected SiC MOSFETs due to increased 'R_{dson}' with temperature.

2.10 Conclusions

- A detailed dynamic voltage balancing and switching loss experimental characterization and a method to find the optimal snubber capacitor and snubber resistor for the series connection of 1.7 kV SiC MOSFETs have been presented.
- The analytical expression to determine the rating of snubber resistor and snubber resistor losses have been presented.
- In addition, different configuration of converters (Full bridge, half-bridge, DC-DC phase-leg) have been demonstrated using series 1.7 kV SiC MOSFET devices in continuous switching mode at different operating conditions to showcase (i) the voltage imbalance is within the limit with increase in junction temperature, (ii) enabling MV/HV converter with switching frequencies up to 8 kHz for high-speed drives or grid-connected applications.
- It has been shown that the series connection of 1.7 kV SiC MOSFETs will enable simple two-level MV converter for high-speed MV motor drive applications with higher switching frequencies (up to 7.5 kHz), and fundamental frequencies (up to 500 Hz).
- The series connection of four 1.7 kV SiC MOSFETs has significantly lower total loss compared to single 6.5 kV Si IGBT for the same current rating and $f_{sw} > 1$ kHz.
- The estimated **powered density of** VSD section (both front-end and VSI) is **2.38 MW/m^3**, which is much higher than the "DOE" specifications of next generation high speed drives **0.66 MW/m^3**.

Chapter 3 Characterization of High Voltage 15 kV SiC MOSFET, 15 kV SiC IGBT and their Performance Evaluation

3.1 Introduction

In Chapter 2, the performance of series connected LV SiC MOSFETs has been evaluated to enable two-level converter for MV applications as commercial of HV SiC devices (10-15 kV) are unavailable. However, the power electronics designers in smart grid industry and medium voltage (MV) high power density motor drives industry are interested in understanding the capability of high voltage silicon carbide devices (> 10 kV) in MV converter. There has been tremendous progress in research and development to make 10 kV-15 kV high current SiC modules as shown in Table 3-1 and these modules will become commercially available in the coming years. Therefore, it is important to understand the characteristics of available HV SiC devices (low current or high current), so that some of the converter design issues using these devices can be addressed to enable simple two-level converters for MV applications. This chapter presents the complete switching characterization of 15 kV SiC MOSFET module (with two parallel dies) and its performance with existing 15 kV SiC IGBT (5µm) modules (single and two parallel dies).

Table 3-1: Summary of recently developed HV SiC devices for MV applications

Single chip modules	Multi-chip module
10 kV/10 A SiC MOSFET module single die (Gen-I)[36]	10 kV/120 A SiC MOSFET using 15 dies of Gen I [36]
10 kV/10 A SiC MOSFET module with single die (Gen-II)	10 kV/20 A SiC MOSFET using two dies of Gen-II
10 kV/10 A SiC MOSFET single die (Gen-III)	10 kV/240 A SiC MOSFET using 18 dies of Gen III [9]
15 kV /10 A SiC MOSFET module with single die[6]	15 kV /20 A SiC MOSFET module with two dies
15 kV /20 A SiC IGBT (5µm) module with single die [37][38]	15 kV /40 A SiC IGBT (5µm) module with two dies [39]

The highest blocking voltage reported in state of the art SiC MOSFET is 15 kV [5][6][40] and that for state of the art SiC n-IGBT is 27.5 kV [41]. The first ever demonstration results of a three-phase MV

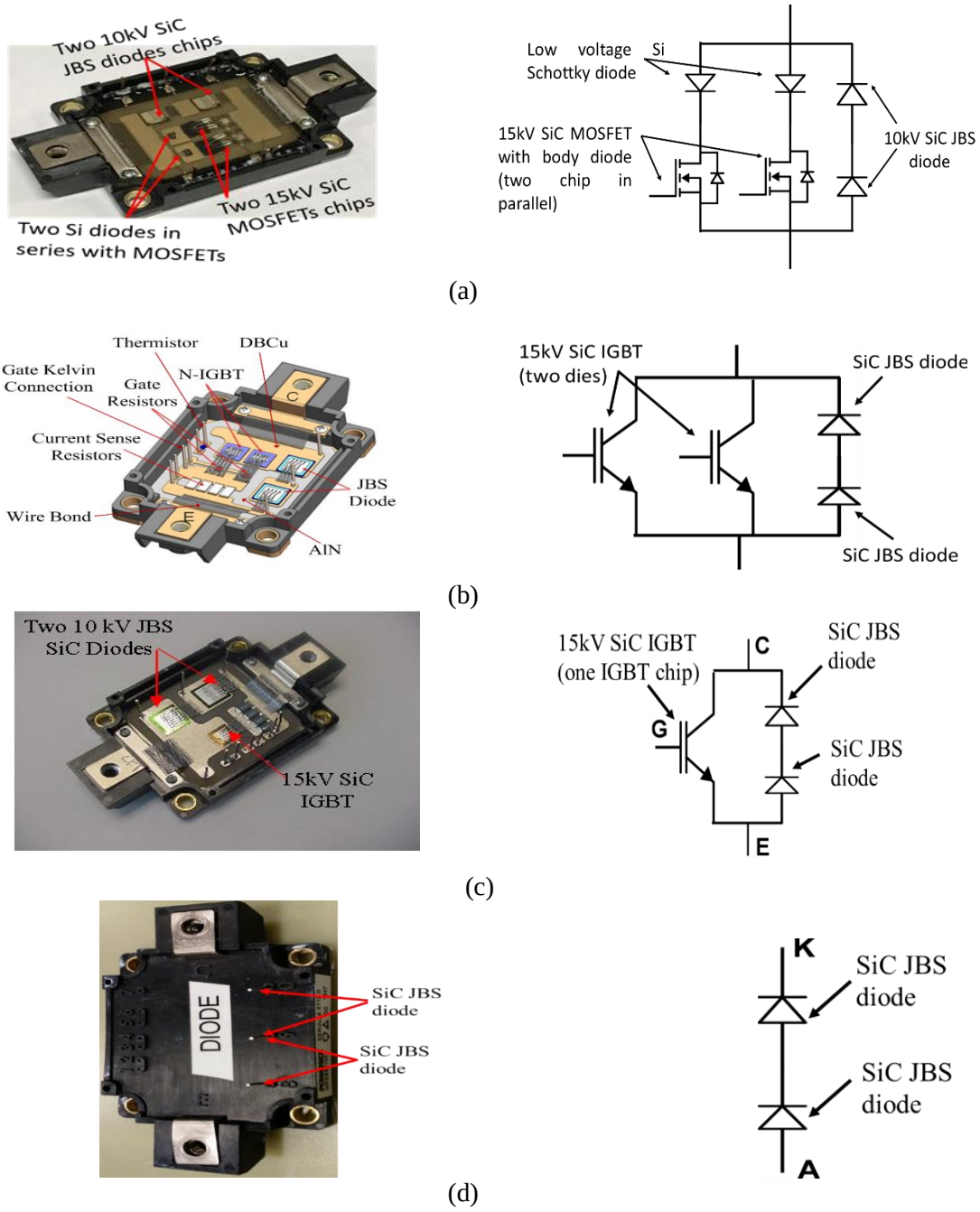


Fig. 3-1: (a)15 kV/ 15 A SiC MOSFET co-pack module package and its Chip layout ; (b) 15 kV /40 A SiC IGBT(5µm buffer layer) co-pack module package and its Chip layout; (c) 15 kV /20 A SiC IGBT (5µm buffer layer) co-pack module package and its Chip layout; (d) 15 kV SiC JBS diode and its Chip layout

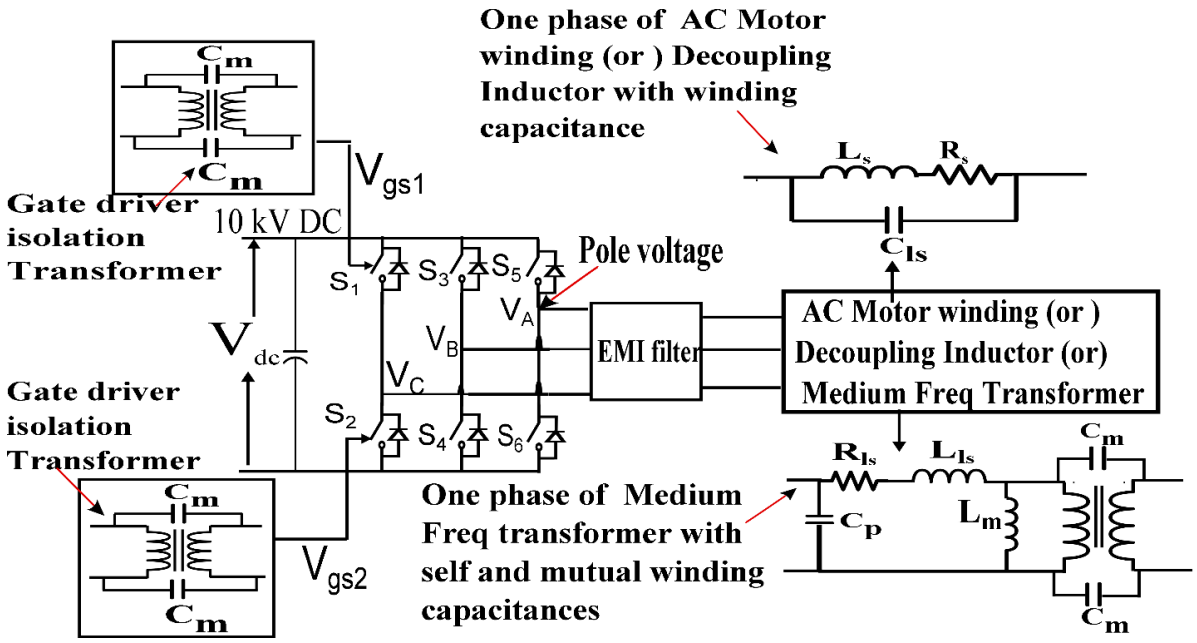
grid-connected 100 kVA Solid State Transformer (SST) enabled by 15 kV SiC n- IGBT has been reported in [42]. The high voltage SiC devices - 15 kV SiC MOSFET (Fig. 3-1(a)) with chip area 8

mm x 8 mm [5][6] and 15 kV SiC IGBT (Fig. 3-1(b)-(c)) with chip area 8.4 mm x 8.4 mm [37][38]- offer simpler medium voltage converter topologies and more efficient power conversion, leading to high power density power converters. Fig. 3-1 (a) and Fig. 3-1(b)-(c) show the 15 kV SiC MOSFET co-pack module, 15 kV SiC IGBT co-pack module designed by Cree Inc., packaged by Powerex and their chip layouts in the respective module. The anti-parallel diode chips in these two modules are made using two series connected 8 kV-10 kV SiC JBS diodes. Fig. 3-1(d) shows the 15 kV SiC JBS diode module made using two 10 kV SiC JBS diode chips and this module has been used as a high side freewheeling switch in the one of the inductive clamped double pulse test (DPT) circuit configuration for characterization of these modules.

This chapter provides a comparative evaluation of 15 kV SiC MOSFET and 15 kV SiC IGBT devices. The performance comparison of these two devices is helpful for designers to choose the right device for their application. These high voltage SiC devices generate high *dv/dt* during switching transitions which generates common mode current through parasitic capacitances. The sources of parasitic coupling capacitances in power converter system could be: (i) device base plate to heat sink; (ii) gate driver isolation transformer parasitic capacitance; (iii) converter filter inductor turn to turn capacitance; (iv) transformer primary to secondary winding capacitances; and (v) motor turn-to-turn winding capacitance. From power electronics designer's point of view, it is desired to compare the performance of these two devices for the same common mode *dv/dt* generated at the switching pole, so that the size and cost of external interfacing components (medium frequency inductor, transformer, and gate driver dv/dt isolation) remain same. The MV DC-AC converter with possible inductive interfacing components and their equivalent circuits with parasitic coupling capacitances are shown in Fig. 3-2(a).

A comparative performance study of high voltage 10 kV SiC MOSFET devices and 15 kV SiC IGBT for medium voltage converter applications have been mentioned in [43]-[46]. In [43]-[45], it is shown that for 1 MW, the 10 kV SiC-MOSFET with SiC-JBS diode can achieve switching frequency limits more than 10 kHz compared to other devices and it is claimed to offer high power density converters than the 15 kV SiC IGBT. In [46], it is shown that 15 kV SiC IGBT has lower total losses than 15 kV SiC MOSFET up to 7 kHz. However, it is not mentioned whether the devices loss data has been computed at same *dv/dt* conditions to evaluate the converter losses. The earlier papers also did not mention the cost saving as a result of a reduction in switching loss due to fast switching as well as size, cost implications due to required EMI filter components to compensate the detrimental effects of fast *dv/dt* transitions at the pole voltages. Hence, the comparison methods reported in the earlier literature are not fully comprehensive to evaluate these devices in power electronics converters.

Therefore, this chapter presents a fair comparison based on same *dv/dt* of the fast switching power electronic devices in a converter application.



(a)

(b) (c)

Fig. 3-2: (a) DC-AC converter with possible inductive interfacing components with equivalent circuits; (b) DC-DC bi-directional converter; (c) DC-DC unidirectional converter

The switching characteristics of 15 kV/20 A SiC IGBT (5µm buffer layer) and its switching frequency limits have been extensively reported in [38]. Whereas, the 15 kV /40 A SiC IGBT (5 µm buffer layer) switching characterization has not been reported at higher dc bus voltages (> 7 kV) and higher junction temperatures (T_j) =150^{0}C. The 15 kV/20 A SiC IGBT data from [48] has been taken for comparison with 15 kV SiC MOSFET. However, 15 kV SiC MOSFET and 15 kV/40 A SiC IGBT

have been extensively characterized in this chapter. The 15 kV SiC MOSFET has not been extensively characterized in the existing literature [5],[6],[40]. References [5], [6] reported the switching loss at ambient temperature (25^0C) and one value of gate resistance. It has not been characterized for higher junction temperatures. The switching frequency limits of 15 kV SiC MOSFET results with boost converter has been evaluated up to 6 kV/ 5A only and were not evaluated at the rated nominal operating voltage (10 kV). Reference [40] reported only static I-V transfer characteristics of 15 kV SiC MOSFET in first and third quadrant operation but not the switching characteristics. The switching characterization reported for 15 kV SiC MOSFET has been tested -

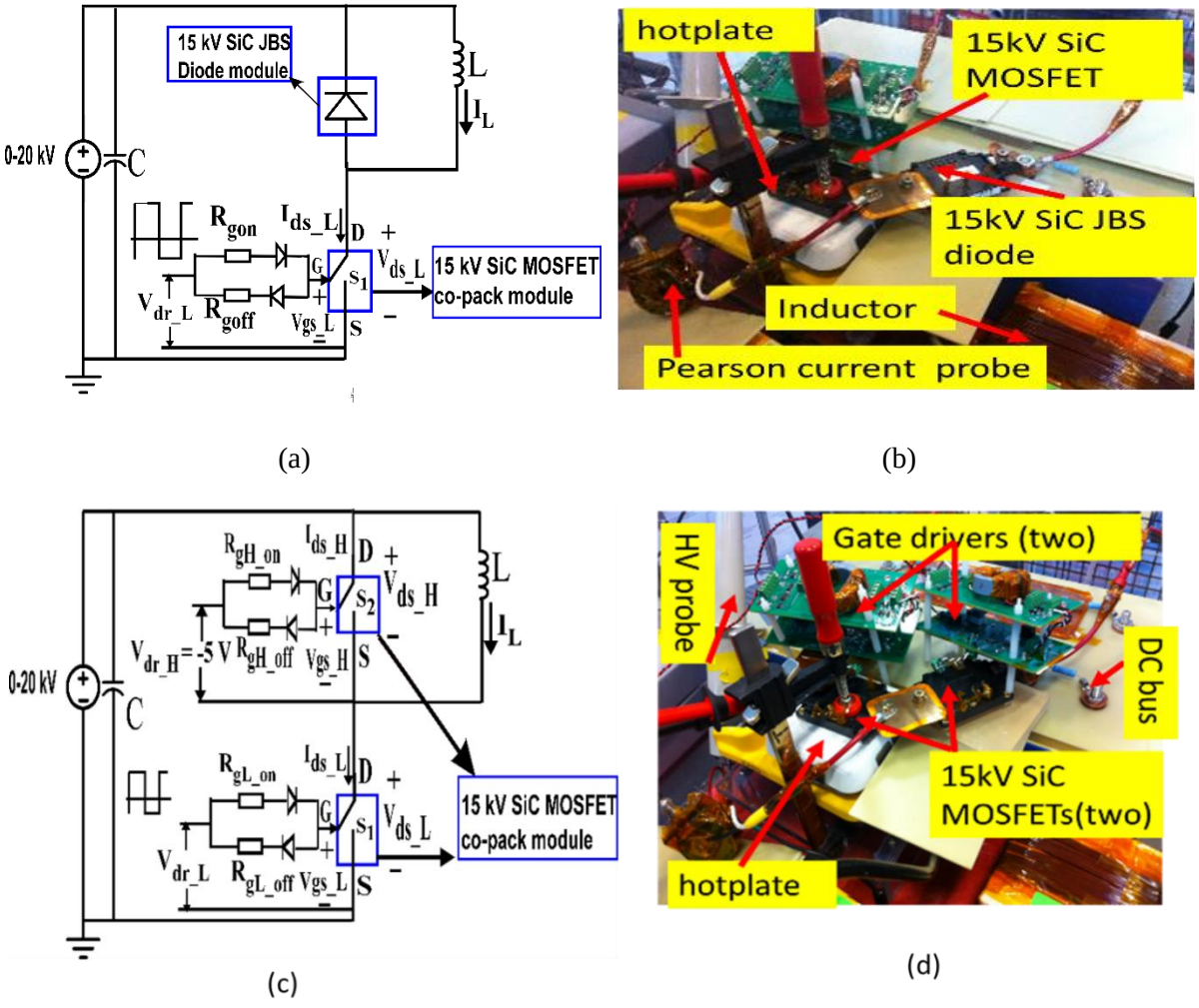


Fig. 3-3: (a) Double pulse test setup with high side SiC JBS Diode and low side MOSFET co-pack module; (b) Experimental test setup with high side Diode and 15 kV SiC MOSFET co-pack module on low side;(c) Double pulse test setup with MOSFET co-pack module on both low side and high side (phase leg configuration);(d) Experimental test setup with MOSFET co-pack module on both low side and high side

-using the Inductive clamped circuit as shown in Fig. 3-3(a) [5][6], but not using phase leg configuration setup (Fig. 3-3(c)). Switching losses characterized using Fig. 3-3 (a) will be slightly lower compared to switching losses characterized using phase leg configuration (Fig. 3-3(c)). It is because, for the same value of DC capacitor and loop inductance (bus bar arrangement and connecting bus bar between the devices), the peak current through the device under test (**DUT**) during the turn-on is different when the high side switch is a JBS diode module as compared to a MOSFET co-pack module. Therefore, the switching characterization results using Fig. 3-3 (a) cannot be used to evaluate the efficiency of DC-AC or AC-DC or DC-DC bidirectional converter as shown in Fig. 3-2(a) & Fig. 3-2(b), but it can only be used in where either high side or low side is freewheeling diode module such as DC-DC converters shown in Fig. 3-2(c). Furthermore, the phase leg configuration setup is more prone to partial shoot- through due to high *dv/dt* -conditions and hence leads to more switching losses in the DUT. This partial shoot- through problem has not been analyzed in 15kV SiC MOSFET devices, though partial shoot through for low voltage (LV) wide band gap devices has been reported in [47].

This chapter is organized as follows:

Section 3.2 presents experimental switching characterization test setup.

Section 3.3 presents the switching characterization of 15 kV SiC MOSFET co-pack module as DUT on low side switch and 15 kV JBS SiC diode module on high side switch in double pulse test (DPT) circuit shown in Fig 3(a).

In section 3.4 presents the switching characterization of 15 kV SiC MOSFET in phase leg configuration (with 15 kV SiC MOSFET co-pack module on both high side and low side as shown in DPT circuit shown in Fig 3(c)). It also presents the influence of *dv/dt* on crosstalk and resultant partial shoot through phenomena.

Section 3.5 presents endurance test (continuous switching mode experimental demonstration) of 15kV SiC MOSFET for different output voltage and loading conditions for both bi-directional and unidirectional DC-DC boost converter.

Section 3.6 presents the switching characterization of 15 kV/40 A SiC IGBT (5µm buffer layer) in phase leg configuration.

Section 3.7 presents a comparison of 15 kV SiC MOSFET and 15 kV SiC IGBT devices. It also presents the analytical power loss evaluation of DC-DC boost converter (unidirectional and

bidirectional configurations) using 15 kV SiC MOSFET and 15 kV SiC IGBT to determine the switching frequency limits and efficiency.

Finally, section 3.8 concludes the chapter.

3.2 Experimental switching characterization test setup

Switching characterization is performed using the well-known inductive clamped circuits shown in Fig. 3-3(a) and Fig. 3-3(c). It consists of DC power supply, DC capacitor bank, inductor and DUT (MOSFET co-pack module (S1) and the freewheeling switch is either JBS diode module (D) or MOSFET co-pack module (S2). The key components are high voltage DC bus, gate driver with high dv/dt isolation, and inductor. The HV DC bus has been designed using four series connected DC film capacitors each rated with 3.5 kV DC, 120 µF with low ESL (<30 nH). The copper bus bar arrangement with sufficient clearance (1.5 cm from the unconnected terminal of DC capacitor) is shown in Fig. 3-4.

The insulation material used between the copper bus bar is a **G-10/FR4 material with a thickness of 0.25 to 0.125 inch**. The dielectric strength of the G-10/FR4 material is **350 kV/inch**. Therefore, the isolation achieved between top copper bus and bottom copper is around 43 kV to 87 kV. The copper bus bar corners are smoothed, and all sides are covered with Kapton tape to avoid corona discharge at high switching voltages. The DC voltage sharing has been achieved using high voltage 5 MΩ resistor connected across each DC capacitor. The design consideration of gate drive design for 15 kV SiC device has been reported [48], and same gate driver has been used in all the experiments. The inductor with low interwinding capacitance (<10 pF) with single layer design reported in [37] has been used. The interconnection from DC capacitor bank to device connections are kept as small as possible with copper plates to minimize the switching loop inductance. The dimension of copper plate from positive DC terminal to the freewheeling device is 4 cm x 4 cm x 0.2 cm and from negative DC terminal to device under test is slightly longer (10 cm x 5 cm x 0.2 cm) to accommodate the Pearson current monitor and thermal hot plate. However, the inductance due to these interconnections has minimal effect on turn-off voltage overshoot and EMI due to very low *di/dt* (≤0.02 kA/µs) values at low switching current amplitudes (10 A to 15 A). The high voltage probe (20 kV, 75 MHz Tektronix P6015 probe**)** with very low output capacitance is used for device voltage measurements, low voltage probe (Tektronix P5200) is used for low side gate voltage measurement, and the current is measured using a 120 MHz Pearson current monitor (model no: 6600). The oscilloscope used for the entire tests is a Tektronix TDS series 500 MHz scope.

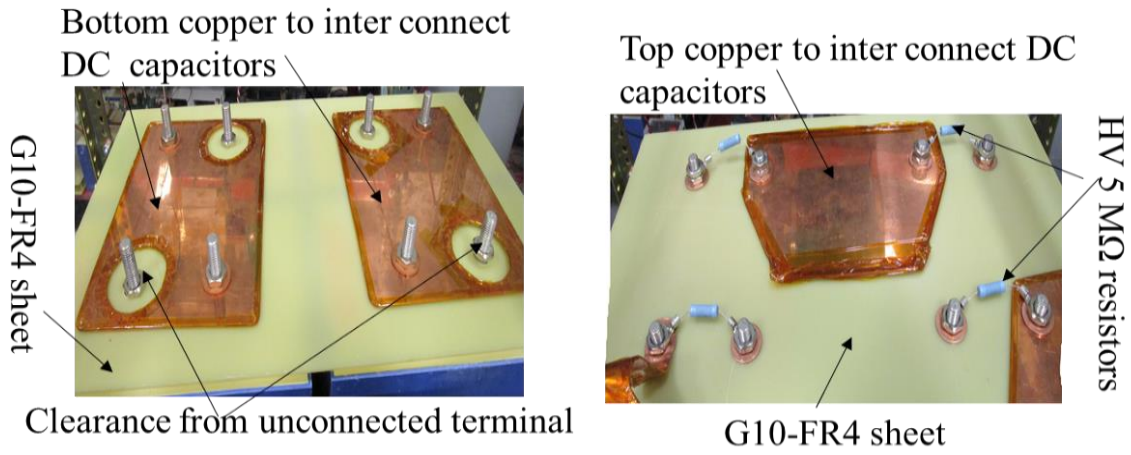


Fig. 3-4: HV DC capacitor bank (rated for 14 kV) used for switching characterization

3.2.1 Static C-V measurements of 15 kV SiC MOSFET, 10 kV JBS diode, 15 kV SiC IGBT per chip

At Cree Inc, the static C-V measurements have been carried out with a single chip 15 kV SiC MOSFET, 10 kV JBS diode and 15 kV SiC IGBT. The corresponding C-V curves are shown in Fig. 3-5, Fig. 3-6, and Fig. **3-7** respectively. The capacitance for co-pack modules and multi-chip co-pack modules as shown in Fig. 3-1 can be estimated from this data. The C-V curve measurements will be useful to understand the relative increase or decrease in switching losses in the DUT using the setup Fig. 3-3(a) and Fig. 3-3 (c).

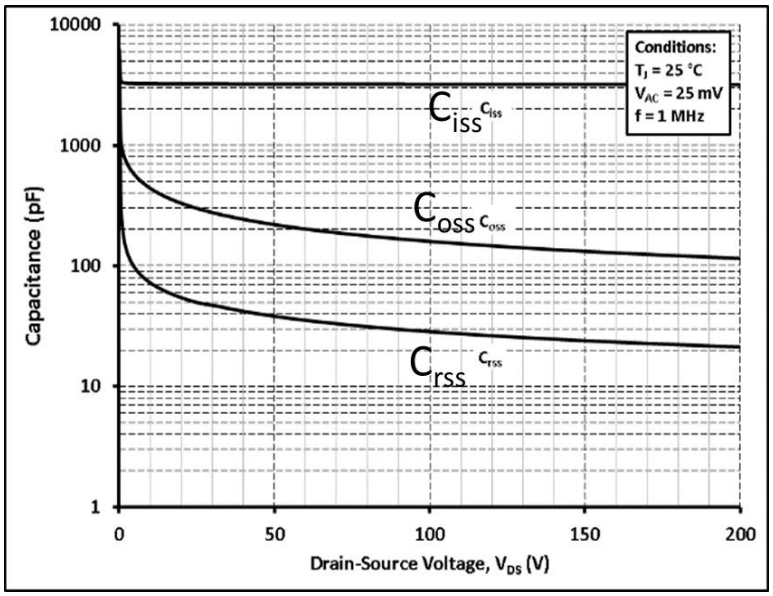


Fig. 3-5: 15 kV SiC MOSFET C-V curve with a single chip

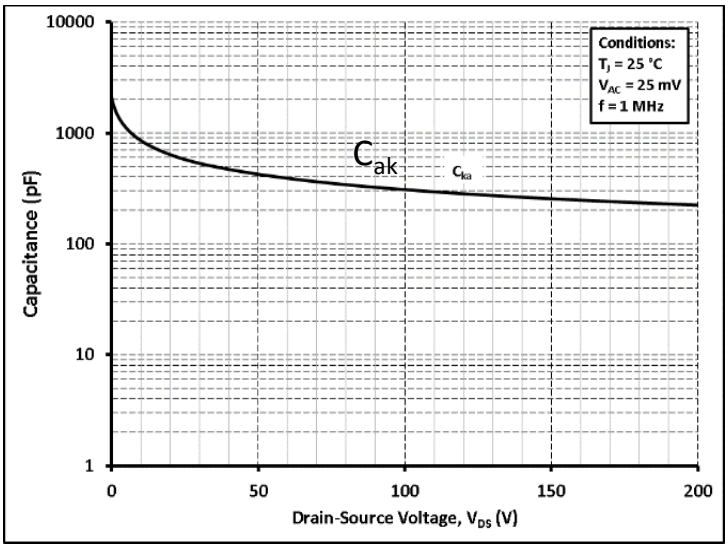


Fig. 3-6: 10 kV SiC JBS diode C-V curve with a single chip

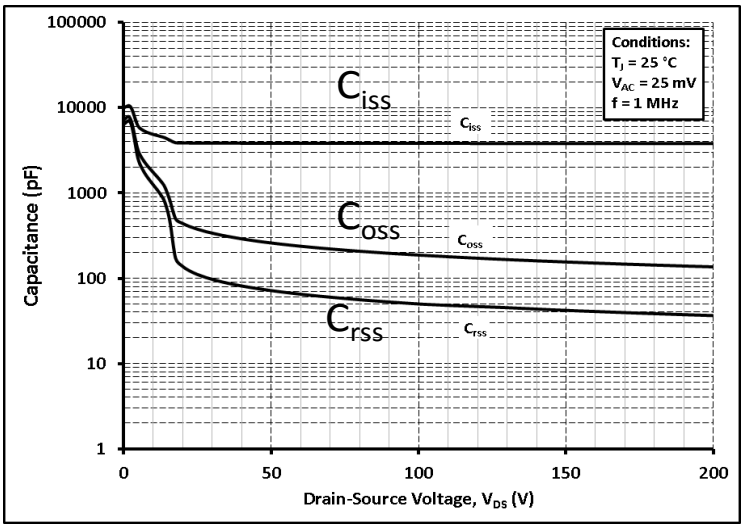


Fig. 3-7: 15 kV SiC IGBT C-V curve with a single chip

3.3 Switching Characterization of 15 kV SiC MOSFET, with Co-pack module as Low side switch and 15 kV JBS SiC diode module as High side switch in Double Pulse Test Circuit

In this section, the result of 15 kV SiC MOSFET switching characteristics are presented using the setup shown in Fig. 3-3 (a) (DUT is 15 kV SiC MOSFET co-pack module on the low side and the

freewheeling switch is 15 kV JBS SiC diode module on the high side). The general double pulse method has been used to characterize the 15 kV SiC MOSFET co-pack module.

3.3.1 Turn-off losses

The Fig. 3-8 shows the turn-off switching transition of 15 kV SiC MOSFET at 12 kV, 10 A and at a junction temperature (T_j) of 125°C. Where, V_{gs_L}: Low side gate to source voltage; V_{ds_L}: Low side voltage across device; I_{ds_L}: Current through low side device; I_L: Inductor current.

Fig. 3-9 shows the turn-off losses with current for different gate resistances at 25°C, at switching voltage of 10 kV and 12 kV respectively. The turn-off losses are nearly same for different values of switching current for lower values of gate resistance. From [49], it is explained that during turn-off event, the transition from plateau region to the threshold is very small. Therefore the channel current will be cut-off quickly by the time voltage across the DUT start rising. Hence, the turn-off loss contributed from actual channel current during voltage rise time is negligible and all the load current will be used to charge capacitances C_{gd} ,C_{ds} and the measured turn-off losses (E_{off}) will be given by (3-1). Where, V_{ds}: Voltage across drain to source; I_{ds}: Current through MOSFET.

$$\int V_{ds} I_{ds}\, dt = \frac{1}{2}(C_{gd} + C_{ds})V_{ds}^2 \qquad (3\text{-}1)$$

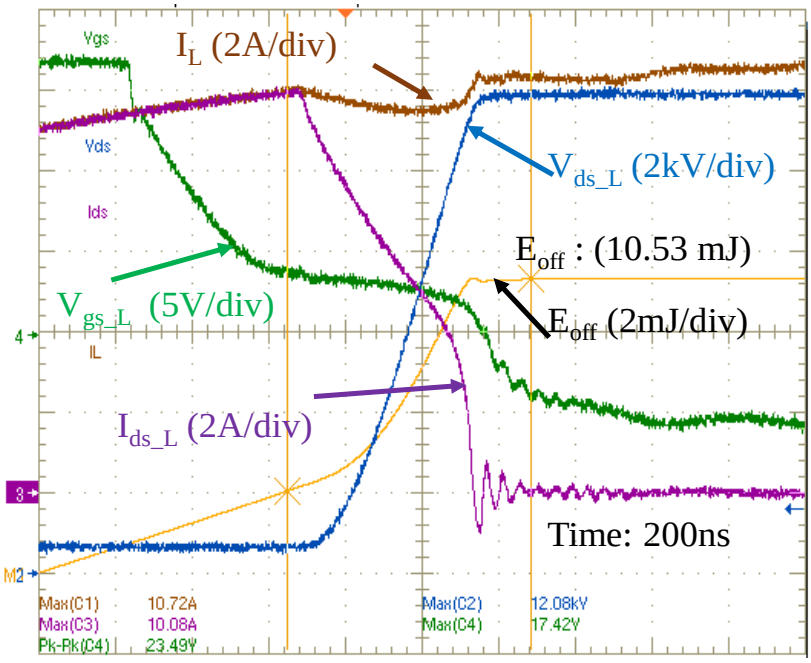


Fig. 3-8: Turn-off loss (10.53 mJ) at 12 kV 10 A at T_j:125°C, R_{goff}: 16.5 Ω

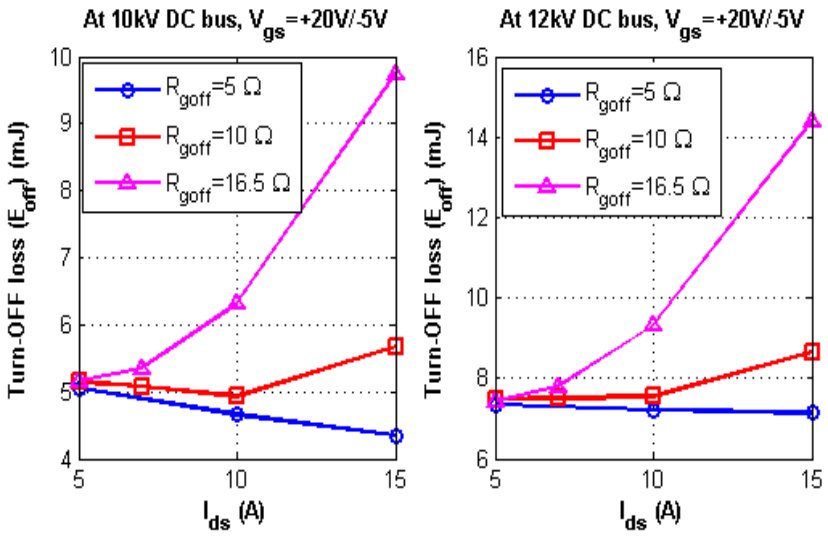


Fig. 3-9: Turn-off losses with device current at 10 kV, 12 kV and T_j: 25^{0}C

Therefore, (3-1) states that the measured turn-off losses are nearly constant with load current for the low value of gate resistances (e.g., R_{goff}: 5 Ω) as shown in Fig. 3-9. However, it is observed that at low gate resistance values (i.e. R_{goff}=5 Ω), there is a slight decrease in turn-off losses (**5.056 mJ** at 10 kV 5 A to **4.352 mJ** at 10 kV 15 A) with an increase in switching current. Fig. 3-10 (a) and Fig. 3-10 (b) show the turn-off loss at 5 A and 15 A respectively at R_{goff}=5 Ω. The turn-off 'dv/dt' is higher for 15 A switching current case compared to 5 A switching current case, because the voltage rise time is inversely proportional to load current [49]. There is a dip in the inductor current during voltage rise time, it is increasing with 'dv/dt' to discharge the parasitic capacitance of Inductor. Therefore, there is a slight decrease in effective load current flowing into the device at 15A turn-off case compared to 5 A turn-off case. Hence, a marginal decrease in turn-off switching losses with the current. Whereas at higher turn-off gate resistances (i.e., R_{goff} =16.5 Ω), the turn-off losses increases with increase in current, following the normal expected trend. For high turn-off gate resistances, the transition from plateau region to threshold limit is not very small. Therefore, the channel current is not cut-off quickly. There is a considerable rise in the drain to source voltage (V_{ds}) before the channel current is cut-off. Therefore, the rise in V_{ds} contributes switching losses before the channel current is cut-off. The loss contribution before the channel current is cut-off increases with increase in current and the total turn-off losses with high gate resistances is the sum of losses in the channel and stored energy given by (3-1). Also due to low turn-off '*dv/dt*' at higher gate resistances, the dip in inductor current is less significant to alter actual device current as shown in Fig. 3-11(a), and Fig. 3-11(b). Therefore, the overall turn-off losses increase with current as shown in Fig. 3-9, Fig. 3-11(a), and Fig. 3-11(b) for high gate resistance case.

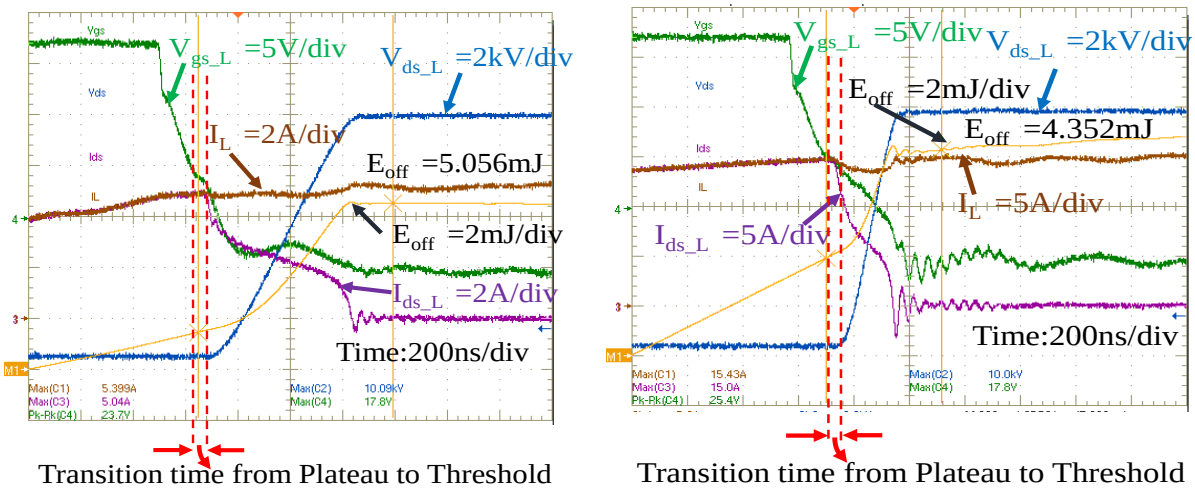


Fig. 3-10: (a) Turn-off transition (E_{off}: 5.056 mJ) at 10 kV 5 A and at T_j:25°C, R_{goff}: 5 Ω ; (b) Turn-off transition (E_{off}: 4.352 mJ) at 10 kV 15 A and at T_j:25°C, R_{goff}: 5 Ω

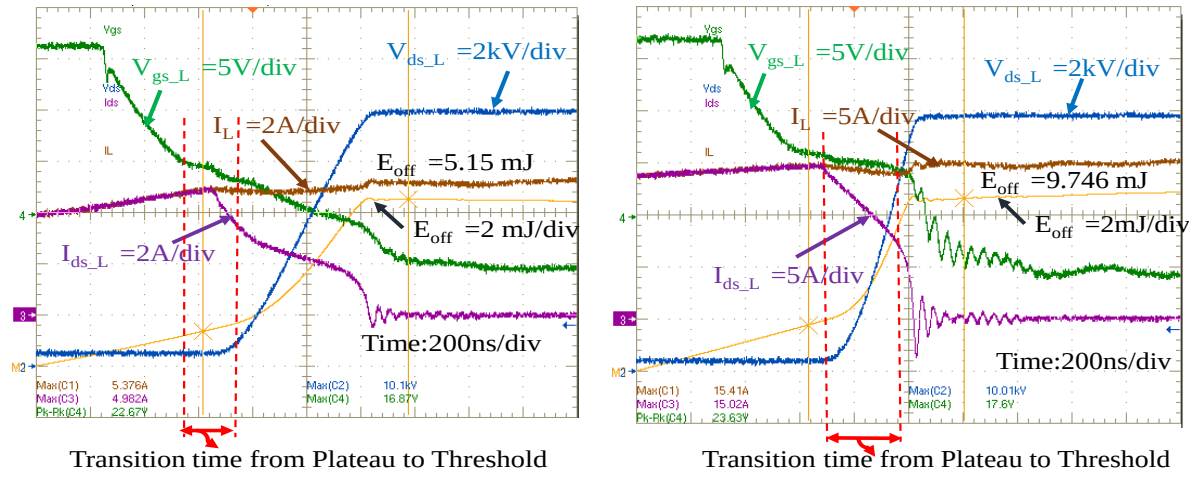


Fig. 3-11: (a) Turn-off transition (E_{off}: 5.152 mJ) at 10 kV 5 A and at T_j:25°C, R_{goff}: 16.5 Ω; (b) Turn-off transition (E_{off}:9.746 mJ) at 10 kV 15 A and at T_j:25°C, R_{goff}: 16.5 Ω

Fig. 3-12 shows the turn-off losses with current at 10 kV and 12 kV switching voltage for different value of junction temperatures (T_j=25°C, 75°C, 125°C) at gate resistances (R_{goff}) of 16.5 Ω. They are nearly constant at lower values of current for T_j=25°C to 125°C and slightly increases with temperature at higher values of current. Threshold voltage measurement with temperature has been done at Cree Inc. The drain current is 2 mA and the drain to source voltage is as low as the gate voltage for the threshold voltage measurement experiment. With the increase of temperature the

threshold voltage reduces as shown in Table 3-2, therefore the transition time from plateau region to threshold limit increases during a turn- off. This will increase switching losses during turn-off slightly. However, the drain to source voltage (V_{ds}) rise is very small during V_{gs} transition from the plateau to the threshold limit and contributing a negligible increase in turn-off losses at a low value of load currents (I_{ds}< 7 A). Fig. 3-12 shows the negligible increase in turn-off losses with the temperature at low load currents. Whereas, at high load currents (I_{ds} > 7 A), the turn-off time is inversely proportional to load current [49].Therefore, the drain to source voltage (V_{ds}) rise is higher compared to low load current scenario during V_{gs} transition from the plateau to the threshold limit. Hence, there is a visible increase in turn-off losses with the temperature at higher currents (I_{ds} >7 A) as shown in Fig. 3-12.

Fig. 3-13 shows turn-off losses with different switching voltages (5 kV-12 kV) at switching current of 5 A, 10 A and gate resistance of R_{goff}: 16.5 Ω. Similarly Fig. 3-14 shows the turn-off losses with different switching voltages for different gate resistances at switching current of 5 A and 10 A respectively.

Table 3-2: 15 kV SiC MOSFET Threshold voltage with temperature at I_{ds}=2 mA

Junction Temperature	25°C	150°C
V_{gs}^{th}	2.466 V	1.868 V

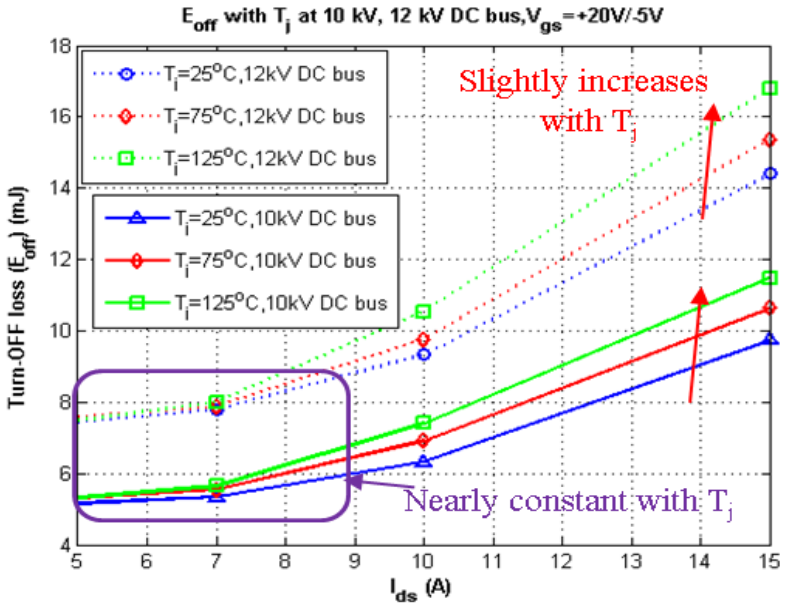


Fig. 3-12: Turn-off losses of 15 kV SiC MOSFET with device current at 10 kV and 12 kV, at different junction temperatures, at R_{goff}: 16.5 Ω

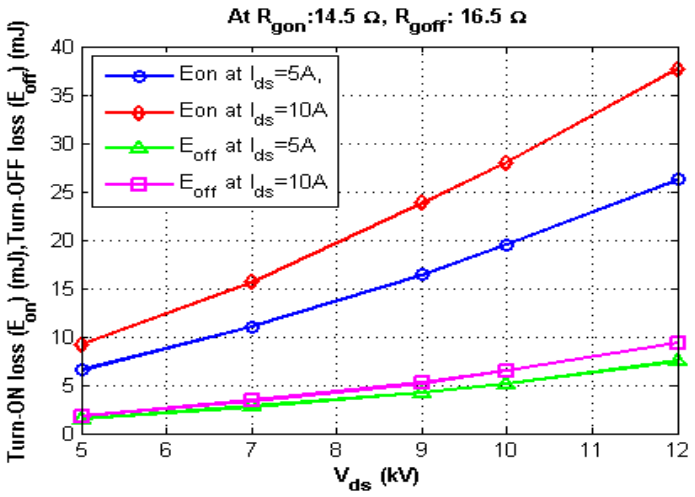


Fig. 3-13: Turn-on and turn-off losses with switching voltage at 5 A and 10 A switching current at gate resistance R_{gon}=14.7 Ω , R_{goff}=16.5 Ω T_j: 25^{0}C

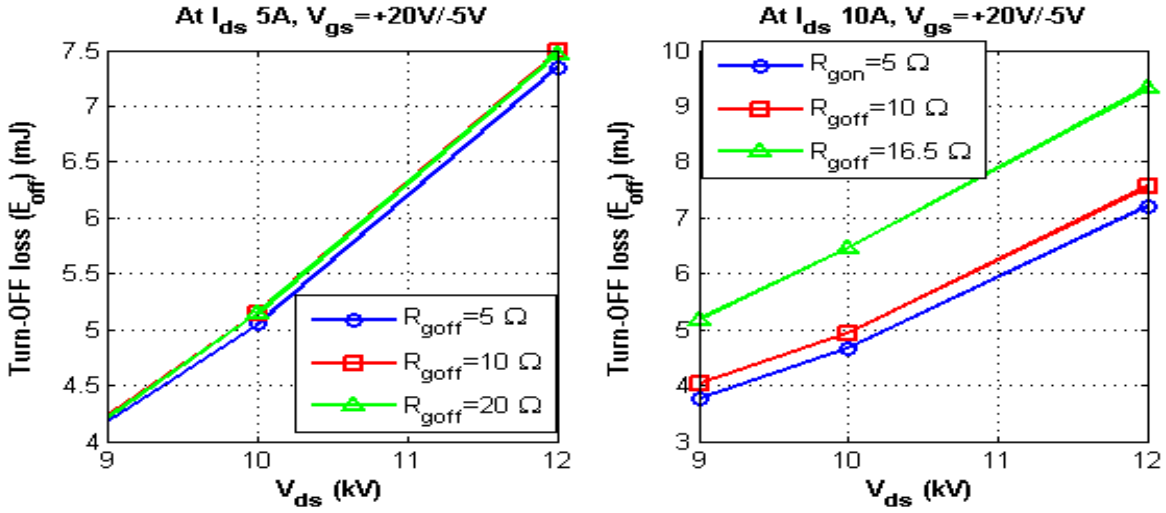


Fig. 3-14: Turn-off losses with switching voltage at 5 A, 10 A switching currents with different gate resistances and at T_j: 25^{0}C

3.3.2 Turn-on losses

The Fig. 3-15 shows the turn-on transition of 15 kV SiC MOSFET at 12 kV, 10 A and at a junction temperature of 125^{o}C. Fig. 3-16 shows the turn-on losses with current for different gate resistances at 25^{o}C, at switching voltage of 10 kV and 12 kV respectively. There is a significant increase in turn-on losses with either increase of device current or increase of DC bus voltage or increase in gate

resistance. Fig. 3-17 shows 15 kV SiC MOSFET turn-on current and voltage at different gate resistances at an ambient temperature of 25°C. The current overshoot during turn-on of low side switch could be due to resonance between parasitic loop inductance and high side JBS junction capacitance and C_{ak} dv/dt (C_{ak}: SiC JBS diode junction capacitance). But it is not from body diode reverse recovery, because the function of the body diode of SiC MOSFET has been eliminated by placing low voltage 'Si' Schottky (break down voltage of the order 50 V to 60 V) in series with 15 kV SiC MOSFET as shown in Fig. 3-1 (a). Therefore, the reverse recovery current from body diode is zero. The reverse recovery of SiC JBS connected across the MOSFET is also negligible.

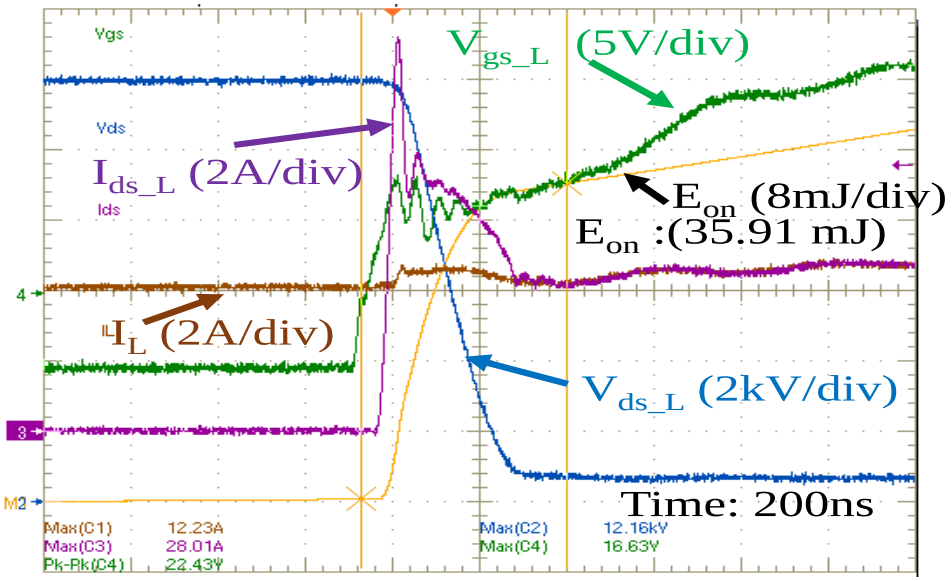


Fig. 3-15: Turn-on loss (35.91 mJ) at 12 kV 10 A at T_j:125^{0}C, R_{gon}:14.7 Ω

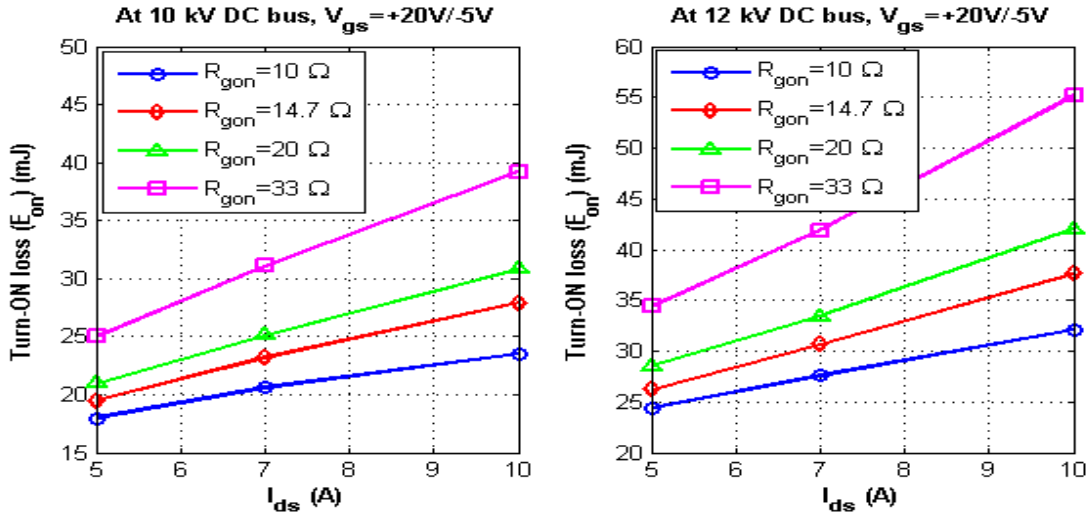


Fig. 3-16: Turn-on losses at 10 kV, 12 kV and at T_j: 25^{0}C

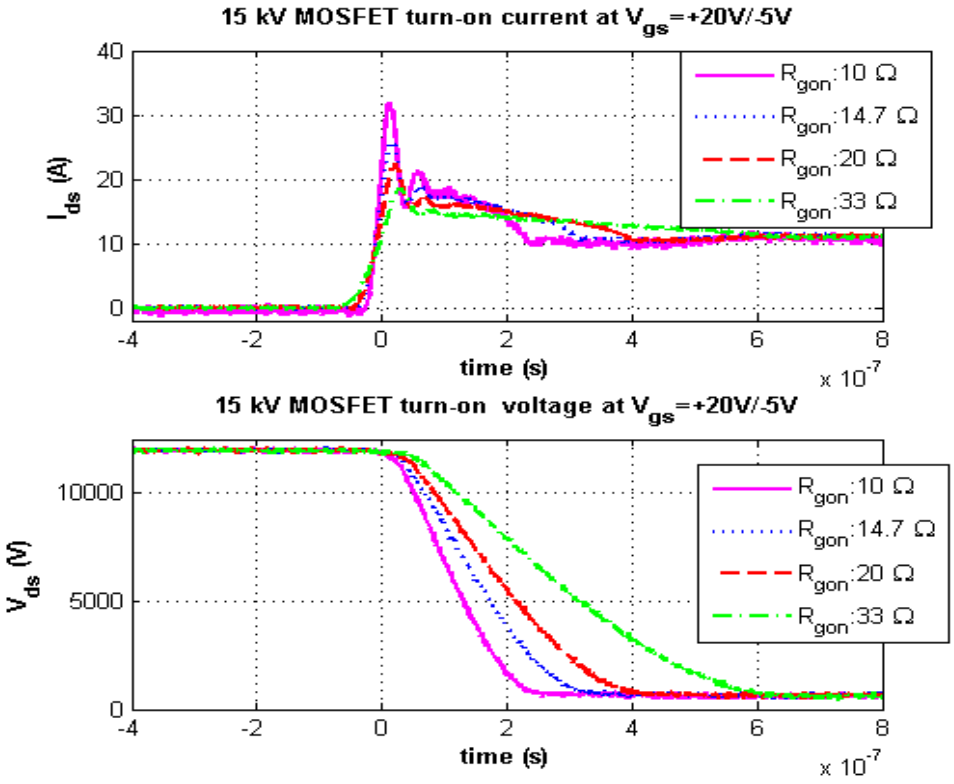


Fig. 3-17: 15 kV SiC MOSFET turn-on current (I_{ds}) and voltage (V_{ds}) at 12 kV 10 A at different gate resistance (R_{gon}) at 25°C with DUT is the co-pack module and the Freewheeling module is JBS diode module in double pulse test

Fig. 3-18 shows the turn-on losses with current at switching voltage of 10 kV and 12 kV DC bus for different values of junction temperatures (T_j=25°C, 75°C, 125°C) at gate resistance (R_{gon}) of 14.7 Ω. The turn-on losses decrease with temperature because the gate threshold voltage will decrease with temperature and hence the switching voltage and current transition times are reduced.

Fig. 3-19 shows the turn-on losses with different switching voltages (9 kV-12 kV) for different gate resistances at switching current of 5 A and 10 A respectively. In addition, Fig. 3-13 shows the turn-on losses with different switching voltages (5 kV-12 kV) at switching current of 5 A, 10 A and gate resistance of R_{gon}: 14.7 Ω.

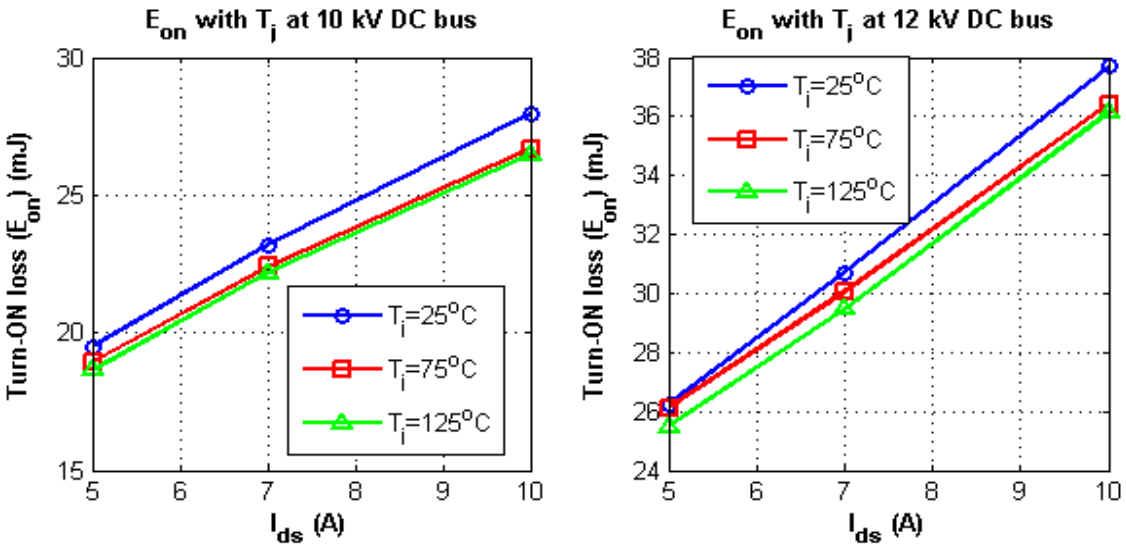


Fig. 3-18: Turn-on losses of 15 kV SiC MOSFET with device current at 10 kV and 12 kV, at different junction temperatures, at R_{gon}: 14.7 Ω

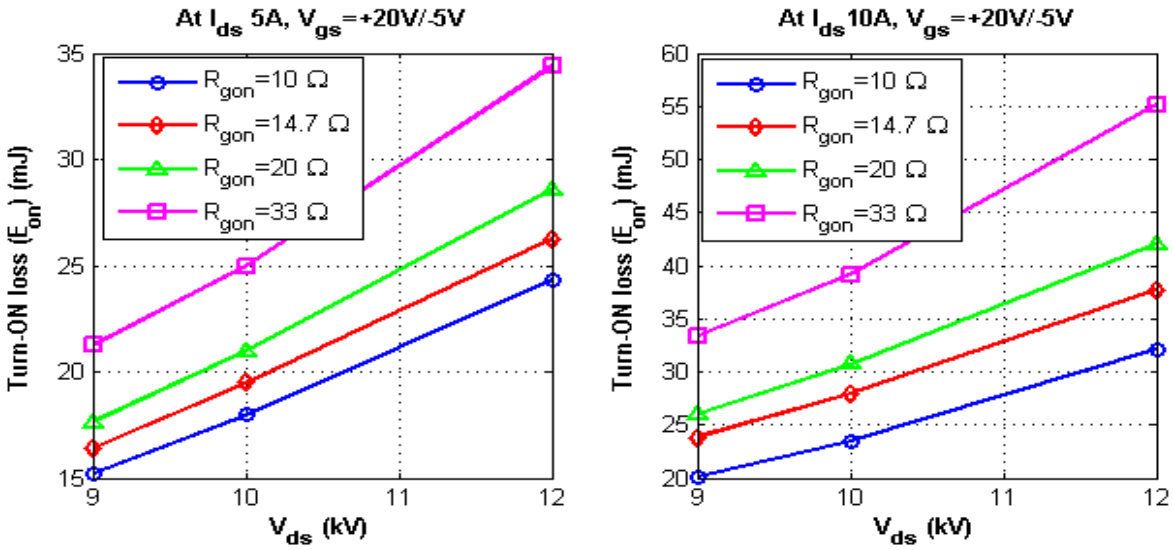


Fig. 3-19: Turn-on losses with different switching voltage, different gate resistances at 5 A, 10 A switching currents and at T_j: 25^{0}C

3.4 Switching characterization of 15 kV SiC MOSFET in phase leg configuration

The 15 kV SiC MOSFET switching loss reported in section 3.3 can only be used for evaluating the unidirectional DC-DC converter or similar converters but cannot give accurate losses for the DC-AC or AC-DC or DC-DC bidirectional converter as shown in Fig. 3-2 (a) or for such similar converters.

Also, SiC devices may have partial shoot through at high turn-on *'dv/dt'* conditions and at certain gate resistances. This will increase the turn-on losses of the device. Therefore, the 15 kV SiC MOSFET switching characterization is performed using the inductive clamped circuit as shown in Fig. 3-3 (c), and it is important for the accurate evaluation of bi-directional converter shown in Fig. 3-2(a) and Fig. 3-2(b) or for such similar converters. The setup is shown in Fig. 3-3(c), it is almost same as Fig. 3-3 (a) except that both high side and low side switches are the same 15kV SiC MOSFET co-pack modules. The gate voltage for the switch S_2 is always maintained at -5V so that only anti-parallel JBS SiC diode in the MOSFET co-pack module conducts during the freewheeling time.

3.4.1 Turn-off losses in Phase leg configuration

Fig. 3-20 shows the turn-off switching characterization at 12 kV, 10 A and at a junction temperature of 125^{0}C, turn-off gate resistance (R_{gL_off}): 4.7 Ω. Fig. 3-21 shows the turn-off losses with current at switching voltage of 10 kV and 12 kV for different gate resistances at 25^{o}C. At lower values of gate resistances, the turn-off losses are nearly same for different values of current, and at higher values of gate resistance it is increasing with the current. The turn-off losses are nearly constant with temperature for a given switching current and voltage.

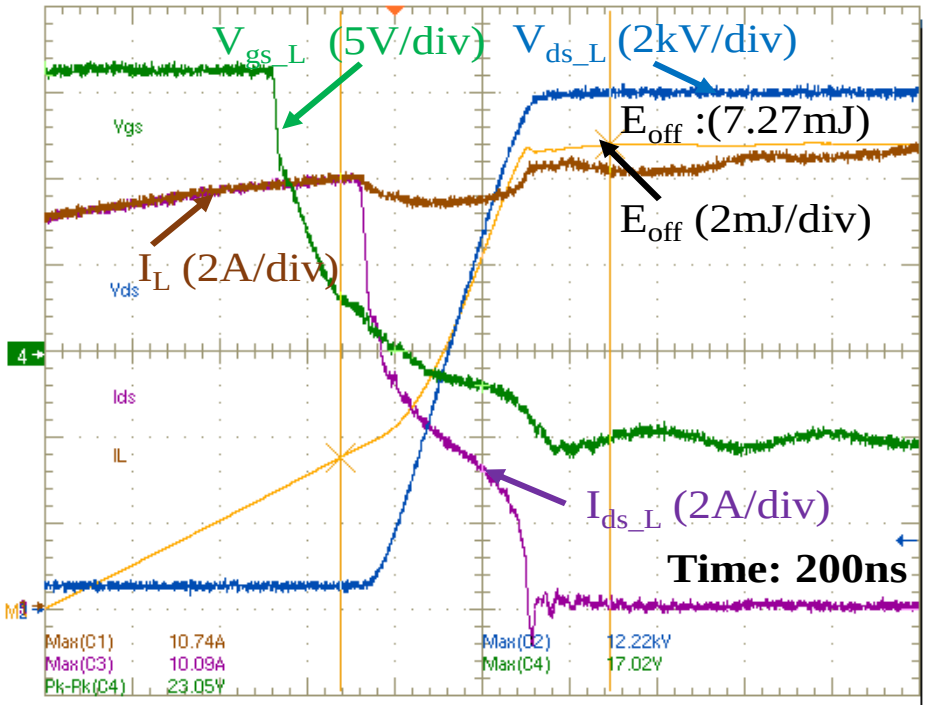


Fig. 3-20: Turn-off losses (7.27 mJ) of 15 kV SiC MOSFET at 12 kV 10 A and at 125^{0}C, R_{gL_off}: 4.7 Ω (with Phase leg configuration)

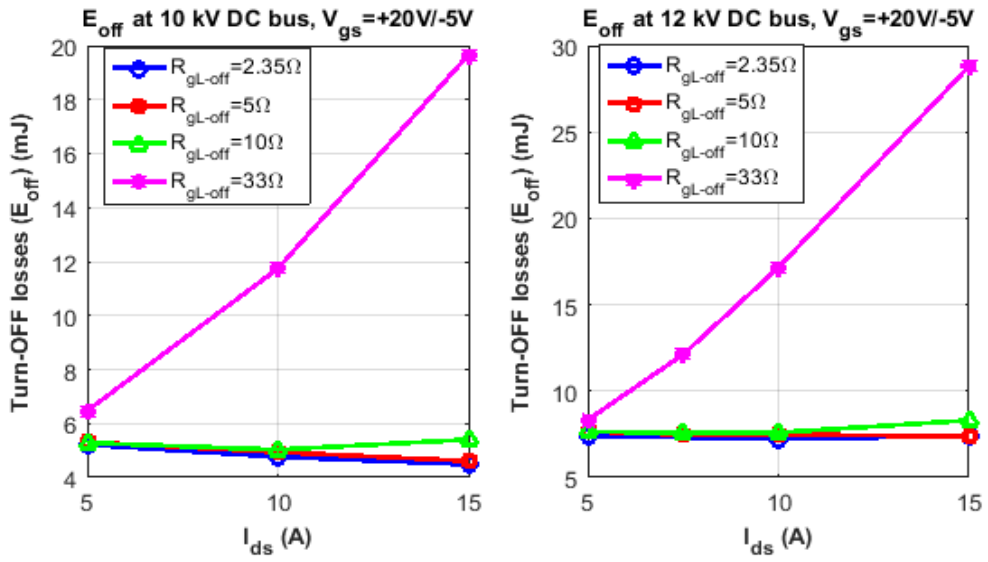
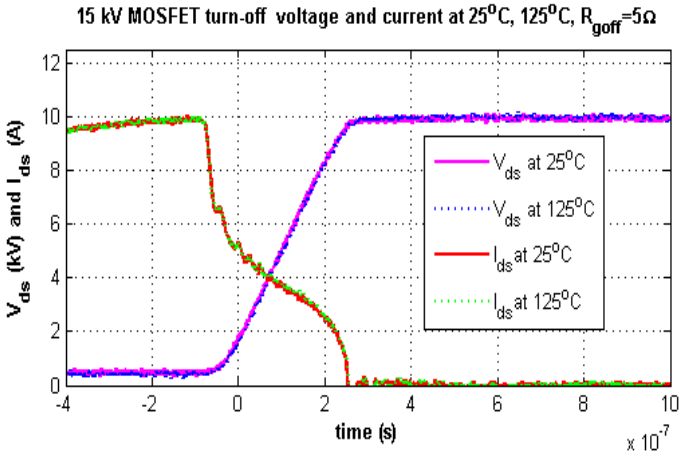


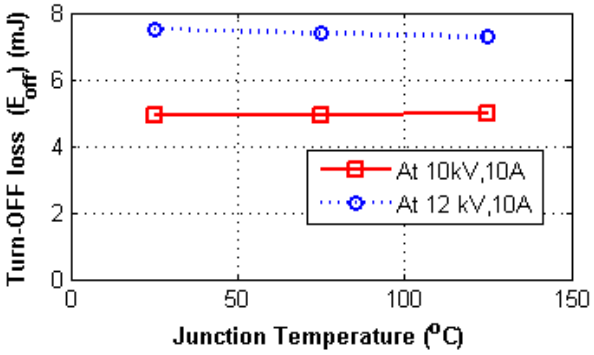
Fig. 3-21: Turn-off losses of 15 kV SiC MOSFET at 10 kV,12 kV and at T_j: 25^{0}C, (with Phase leg configuration)

The Fig. 3-22 (a) shows the turn-off voltage and current at 25^{0}C and 125^{0}C. From Fig 22(a), it is clear that turn-off losses with temperature do not change, as the area under voltage and current are same in both cases. The data from Fig. 3-22 (b) also confirms that turn-off losses are nearly constant with temperature. As explained earlier in section 3.3.1, for smaller turn-off gate resistances, the turn-off losses are nearly same for lower values of gate resistance. In [49], it is also explained that during turn-off event, the transition from plateau region to threshold limit very small, therefore the channel current will be cut-off quickly by the time voltage across the DUT start rising. Hence, the turn-off loss contributed from actual channel current during voltage rise time is negligible and all the load current will be used to charge C_{gd} and C_{ds} and the measured turn-off losses will be given by (3-1). Therefore, from (3-1) the measured turn-off losses are nearly constant with load current for the low value of gate resistances (e.g. : R_{gL_off}: 5 Ω).

With the increase of temperature the threshold voltage reduces, the transition time from plateau region to threshold limit increases during turn-off. This will increase switching losses during turn-off slightly. However, the drain to source voltage (V_{ds}) rise is very small during V_{gs} transition from the plateau to threshold limit and hence there is no appreciable increase in turn-off losses with temperature. However, the turn-off losses may increase slightly with temperature at higher load current and at higher gate resistances as explained in earlier section. Fig. 3-23 shows the turn-off losses with different switching voltages for different gate resistances at switching current of 5 A and 10 A respectively.



(a)



(b)

Fig. 3-22: (a) 15 kV SiC MOSFET turn-off voltage and curent at 25^{0}C and 125^{0}C with R_{gL_off}: 5 Ω. (with Phase leg configuration); (b) Turn-off losses of 15 kV SiC MOSFET at 10 A device switching current, at 10 kV and 12 kV switching voltage, at different junction temperatures at R_{gL_off}: 5 Ω (with Phase leg configuration)

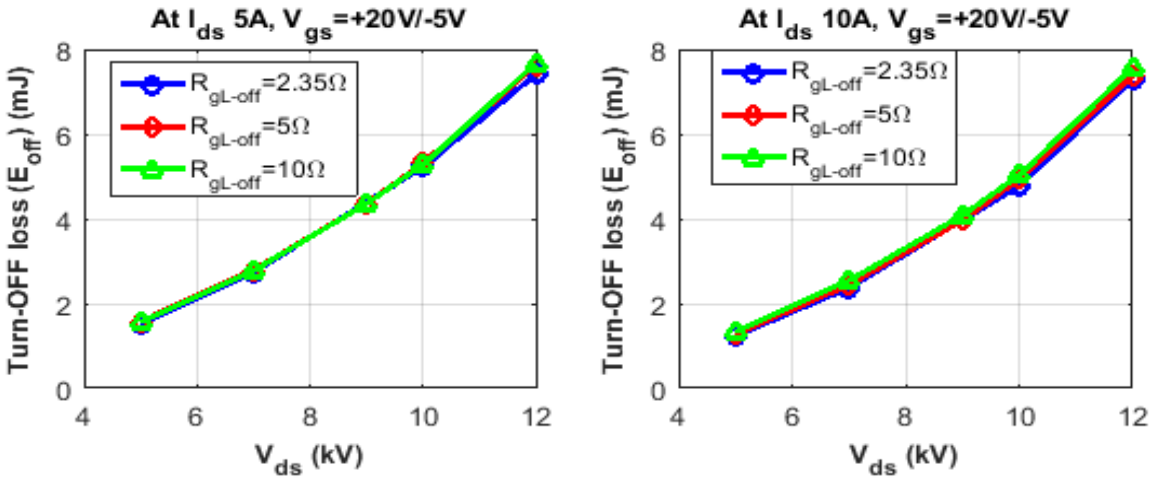


Fig. 3-23: Turn-off losses with switching voltage at 5 A switching current with different gate resistances, T_j: 25^{0}C (with MOSFET co-pack module on both low side and high side switch)

3.4.2 Turn-on losses in Phase leg configuration

Fig. 3-24 shows the turn-on loss at 12 kV, 10 A and at 125^{0}C, R_{gL_on}:33 Ω. Fig. 3-25 shows the turn-on losses with current for different gate resistances at 10 kV, 25^{o}C. Fig. 3-26 show the turn-on losses with different switching voltages for different gate resistances at switching current of 5 A and 10 A respectively.

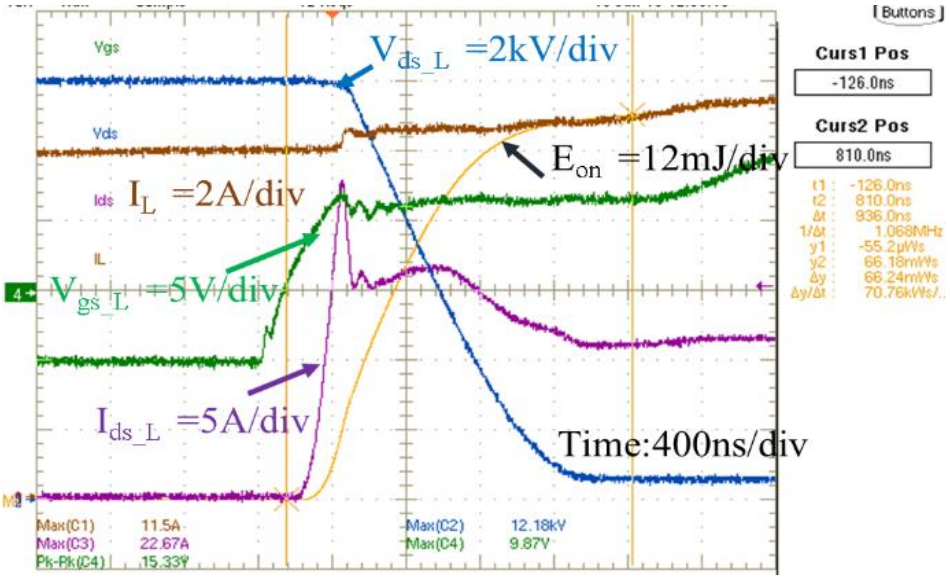


Fig. 3-24: Turn-on losses (66.24 mJ) of 15 kV SiC MOSFET at 12 kV 10A and at 25^{0}C, R_{gL_on}: 33 Ω (with Phase leg configuration)

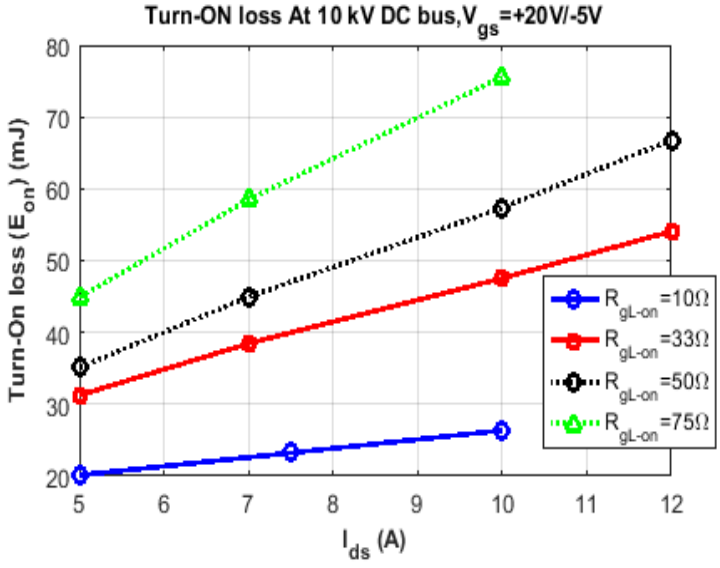


Fig. 3-25: Turn-on losses (E_{on}) of 15 kV SiC MOSFET at 10 kV at 25^{0}C (with Phase leg configuration)

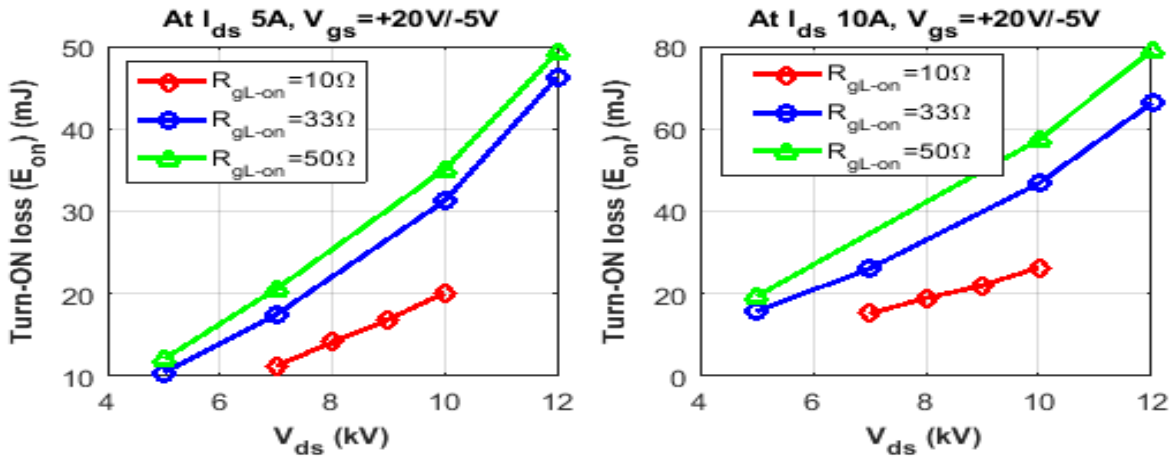


Fig. 3-26: Turn-on losses with switching voltages at 5 A and 10 A switching currents with different gate resistances, T_j: 25^{0}C (with Phase leg configuration)

Table 3-3: Comparison peak current in the device during turn-on

	Phase leg configuration (R_{gL_on} = R_{gL_off} =33Ω, R_{gH_on} = R_{gH_off}=33Ω)	**High side JBS diode and low side SiC MOSFET module (R_{gon}=33Ω)**
Switching voltage and current	**Turn-on Peak current in the device (A)**	**Turn-on Peak current in the device (A)**
10 kV, 5 A	16.2	12.26
10 kV, 7 A	19.0	14.85
10 kV, 10 A	22.42	18.41

For the same turn-on *dv/dt* (21 kV/µs) *and* turn-on gate resistances values (33 Ω), the turn-on losses increase is slightly more (1.2 to 1.25 times approximately) using SiC MOSFET co-pack module on the high side compared to the SiC JBS diode module on the high side, due to high current overshoot. This is mainly due to 15 kV SiC MOSFET co-pack module having a higher output capacitance than the 15 kV JBS diode module, hence more parasitic (loop inductance and output capacitance) resonant current. The comparison of peak current in the device during turn-on for two different configurations is shown in Table 3-3. The C_{oss} and C_{ak} for the 15 kV SiC MOSFET and 10 kV SiC JBS diode are per chip basis as shown in Fig. 3-5 and Fig. 3-6. To get a relative increase in capacitance values between JBS diode module and MOSFET co-pack module, the actual arrangement and number of chips in the module needs to be considered as shown in Fig. 3-1(a) and Fig. 3-1(d). The output capacitance of high side switch in the setup shown in Fig. 3-3(a) is only due to JBS diode module (Fig. 3-1(d)). Whereas output capacitance of the high side switch in the setup shown in Fig. 3-3 (c) is for the MOSFET co-pack module (Fig. 3-1(a)). The MOSFET co-pack module has "two parallel MOSFET chips and across that there is a JBS diode". Therefore, the net output capacitance of the high side

switch using MOSFET co-pack as the high side switch is higher than that only with the JBS diode module. Hence, there is slightly more current overshoot due to the parasitic resonance as mentioned above. However, for low turn-on gate resistances, there is a partial shoot- through problem in phase leg configuration due to crosstalk. Therefore, current overshoot comparison for those cases is not considered in the present work. The effect of crosstalk on current overshoot and turn-on losses is explained in the subsequent section.

3.4.3 Effect of crosstalk on turn-on losses in phase leg configuration

In the phase leg configuration, the turn-on process of low side switch will affect the operation condition of the high side switch and vice-versa. This interaction might increase peak current through the switch and hence switching losses. The interaction between the two-phase leg switches is called crosstalk. The influence of crosstalk has been extensively discussed in low voltage (LV) wide band gap devices and Si devices in [47][50]-[54]. In a phase leg configuration as shown in Fig. 3-3 (c), the high turn-on *dv/dt* of the low side MOSFET module will cause the similar rate of rise of voltage across the high side module (freewheeling module). The *'dv/dt'* across the freewheeling module will cause miller capacitive (C_{gd}.*dv/dt*) current flow into the high side gate resistance. The high side turn-on gate resistance (R_{gH_on}) does not conduct miller capacitive current due to the forward diode, whereas the high side turn-off gate resistance (R_{gH_off}) conducts to miller capacitive current. Therefore, the voltage drop across 'R_{gH_off} 'will increase the 'V_{gs}' of the high side switch. If the 'V_{gs}' of the high side becomes more than its threshold, then both top and bottom modules will conduct simultaneously and leads to increase in current from DC bus. This will increase the peak current and turn-on losses in the low side switch (DUT). The peak value of high side gate voltage for the low side switching is given in (3-2). Similarly, the peak value of the low side gate voltage for the high side switching is given in (3-3) [52] [53].

Fig. 3-27 shows 15 kV SiC MOSFET turn-on current and voltage at different low side gate resistances (R_{gL_on}) at 12 kV and 10 A. The gate resistance of the high side switch (R_{gH_off}) in all these cases is 33 Ω. From Fig. 3-27 it is clear that, for low turn-on gate resistances (R_{gL_on}:4.7 Ω, 10 Ω) the peak current is significantly higher compared to higher turn-on gate resistances (R_{gL_on}:33 Ω, 50 Ω). This could be due to higher turn-on dv/dt at low gate resistances may have increased the voltage drop in the high side gate resistance (R_{gH_off}=33 Ω) and also the overall gate to source voltage more than the threshold voltage during the voltage rise time of the high side switch. This increased V_{gs} across the high side will turn-on the high side SiC MOSFET, resulting in increased peak current in the low side DUT due to the partial shoot through.

$$V_{gs-H(max)} = \frac{dv}{dt} \times R_{gH\_off} C_{gd\_H} \times \left(1 - e^{\left(\frac{-V_{dc}}{\frac{dv}{dt} \times C_{iss\_H} R_{gH\_off}} \right)} \right) \quad (3\text{-}2)$$

$$V_{gs-L(max)} = \frac{dv}{dt} \times R_{gL\_off} C_{gd\_L} \times \left(1 - e^{\left(\frac{-V_{dc}}{\frac{dv}{dt} \times C_{iss\_L} R_{gL\_off}} \right)} \right) \quad (3\text{-}3)$$

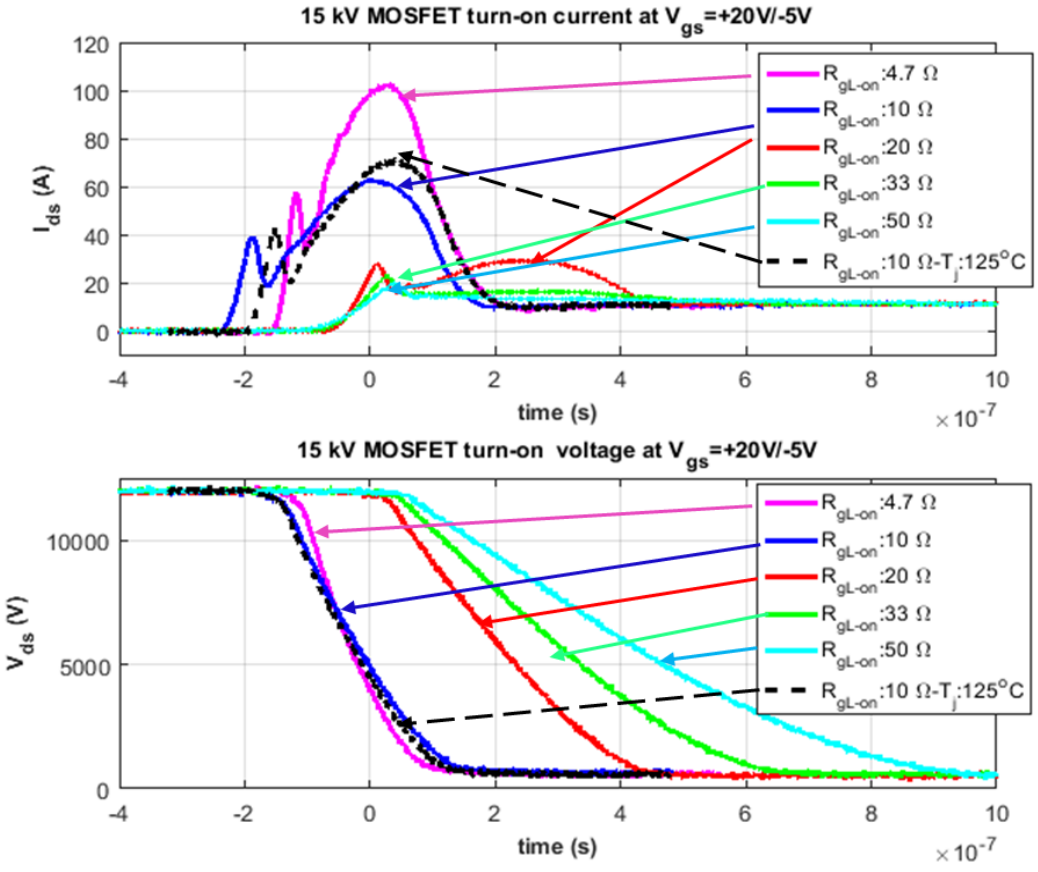


Fig. 3-27: 15 kV SiC MOSFET turn-on current (i_{ds}) and voltage (V_{ds}) at 12 kV 10 A for different R_{gL_on} at 25°C and at 125°C for R_{gL_on} =10 Ω (with Phase leg configuration)

With increasing junction temperature, the SiC MOSFET threshold voltage reduces, hence reducing the turn-on voltage fall time transition. The decreased fall time of V_{ds} (i.e., increased *dv/dt* of V_{ds}) from 25°C to 125°C at R_{gL_on} 10 Ω is shown in Fig. 3-27. This will increase the turn-on *dv/dt*. The increased *dv/dt* draws more 'C_{gd}.*dv/dt*' current from the top freewheeling module's Miller capacitance. Therefore, the increase in V_{gs} in the high side switch will be high at 125^0C compared to that of at 25^0C. This increased 'V_{gs}'- will draws more partial shoot-through current from DC bus. Therefore, the partial shoot through will increase peak current in the low side switch at 125^0C compared to at 25^0C. It is observed that the increased turn-on peak current in the 15 kV SiC MOSFET from 62 A at 25°C to 72 A at 125°C at R_{gL_on}= 10 Ω is shown in Fig. 3-27.

An experiment has been conducted to measure the corresponding increase in 'V_{gs}' threshold at high 'dv/dt' conditions and hence to verify further that the large induced peak current in the MOSFET is due to partial shoot through. With low side MOSFET as DUT as shown in Fig. 3-3 (c), it is extremely difficult to measure the high side floating gate voltage due to non-availability of low voltage probes with high voltage isolation. The available high voltage differential probes (10 kV to 20 kV differential probes) cannot measure low values of the gate to source voltage accurately. Therefore the experiment has been modified with the high side MOSFET co-pack module as DUT and the low side MOSFET co-pack module as the freewheeling device as shown in Fig. 3-28. Hence, the increase in low side gate voltage due to crosstalk from the high side switching can be measured with low voltage probe with high accuracy.

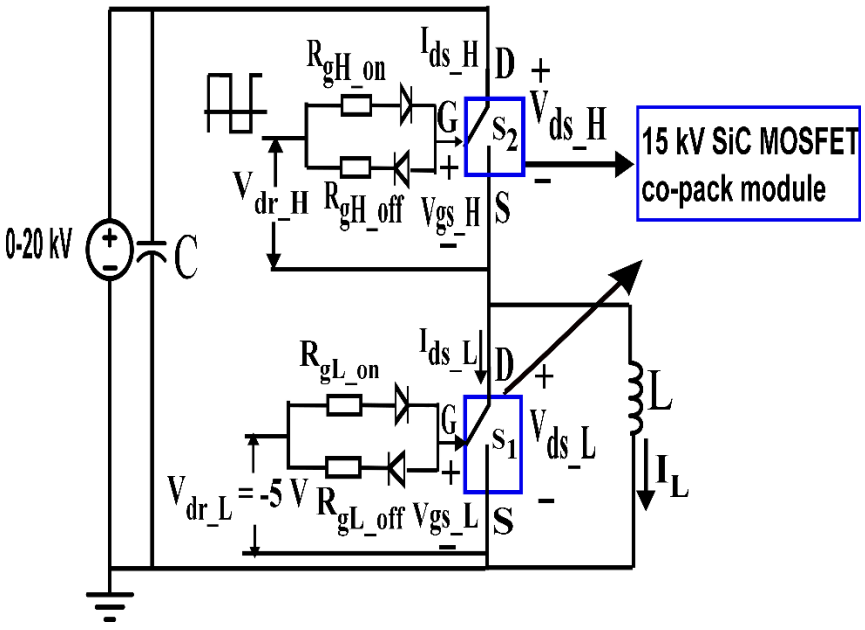


Fig. 3-28: High side switching characterization of 15 kV SiC MOSFET in phase leg configuration

Fig. 3-29 and Fig. 3-30 show the increase in V_{gs} (low side) above the threshold value when high side MOSFET is turning-on at 7 kV, 9 A, R_{gH_on}=4.7Ω, R_{gL_off} =33 Ω and at 9 kV, 9 A, R_{gH_on}=4.7 Ω, R_{gL_off} =4.7 Ω. For the same turn-on high side gate resistance, the V_{gs_L} increases above the threshold value and also its duration is more when the low side gate resistance is R_{gL_off} =33 Ω compared to R_{gL_off} =4.7 Ω. This confirms the significant increase in peak currents at low turn-on gate resistances in Fig. 3-27 are due to partial shoot through.

Fig. 3-32 shows the turn-on loss in high side MOSFET (using setup in Fig. 3-28) at 10 kV, 10 A, R_{gL_on}: 10 Ω, R_{gH_off} =5 Ω. There is a small increase in V_{gs_L} above the threshold, but for the negligible duration and hence a large decrease in peak current compared to Fig. 3-29. Fig. 3-31 shows the turn-on loss in low side MOSFET (using setup in Fig. 3-3 (c)) at 10 kV, 10 A, R_{gL_on}: 10 Ω, R_{gH_off} =33 Ω. From Fig. 3-31and Fig. 3-32, it is clear that for the same turn-on gate resistance, the turn-on losses are reduced nearly **two times** when the partial shoot-through effect is nearly negligible. Therefore proper care should be taken for selection of the turn-on and turn-off gate resistances to prevent partial shoot-through and spurious increases in negative gate voltage, or crosstalk mitigation techniques can be used [55].

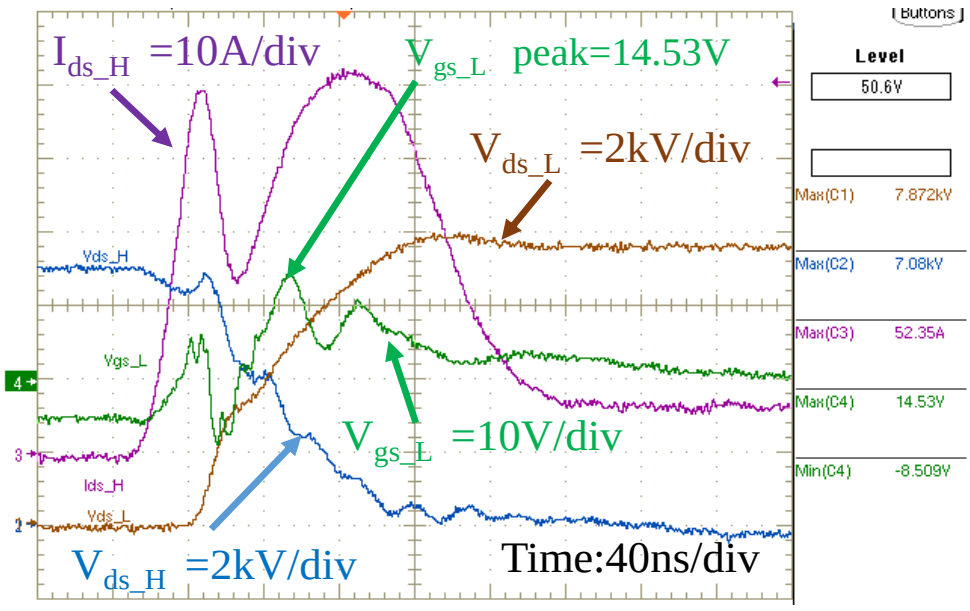


Fig. 3-29: Increase in V_{gs} of low side SiC MOSFET module at 7 kV, 9 A and at R_{gL_on} =R_{gH_on} =4.7 Ω, R_{gH_off} =R_{gL_off} =33 Ω. (high side switching using setup shown in Fig. 3-28)

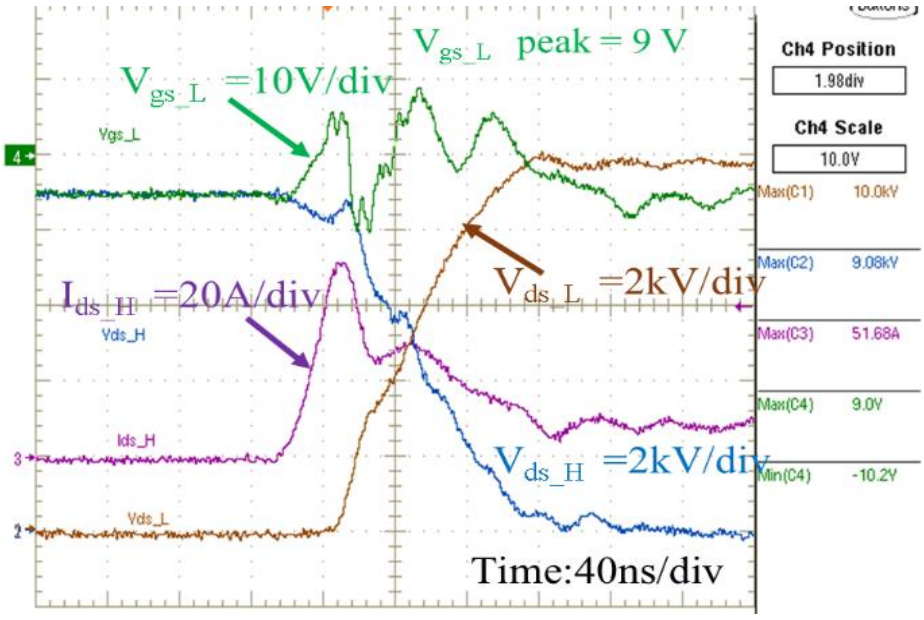


Fig. 3-30: **Increase in V_{gs} of low side SiC MOSFET module at 9 kV, 9 A and at R_{gL_on} =R_{gH_on} =4.7Ω, R_{gH_off} =R_{gL_off}=3.3Ω. (high side switching using setup shown in Fig. 3-28)**

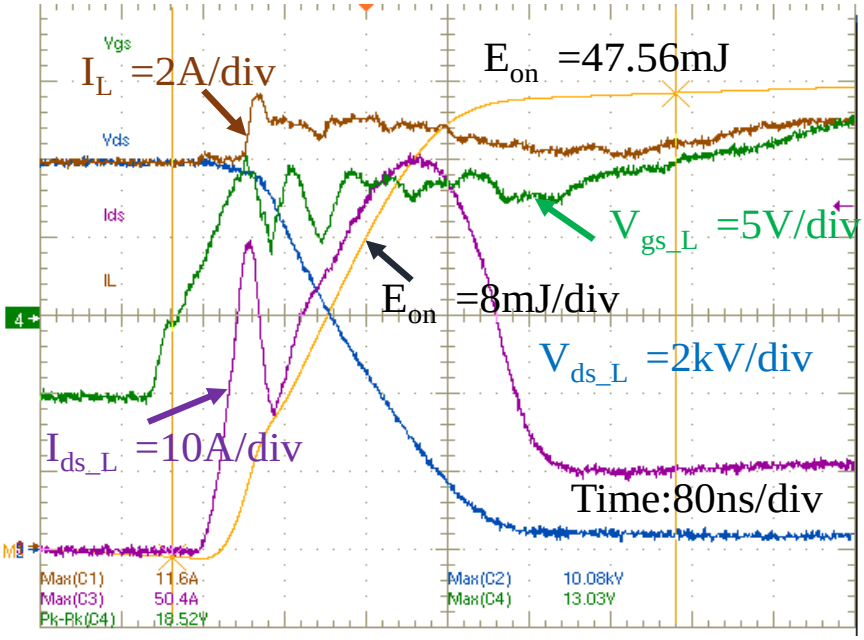


Fig. 3-31: **Turn-on losses (47.56 mJ) of 15 kV SiC MOSFET at 10 kV 10 A, R_{gH_on} =R_{gL_on}= 10 Ω, R_{gH_off} =R_{gL_off} = 33 Ω (low side switching using setup shown in Fig. 3-3 (c))**

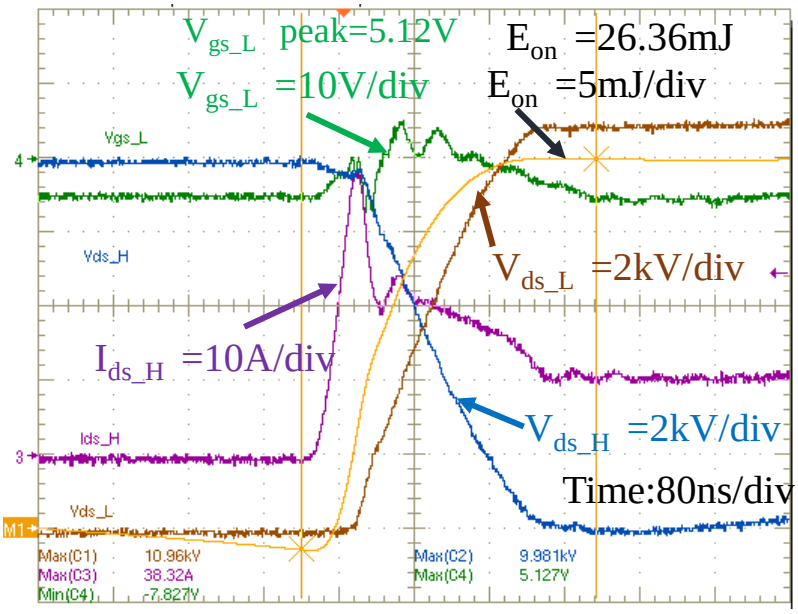


Fig. 3-32: Turn-on losses (26.36 mJ) of 15 kV SiC MOSFET at 10 kV 10 A $R_{gL\_on}=R_{gH\_on}=10\ \Omega$, $R_{gH\_off}=R_{gL\_off}=5\ \Omega$ (high side switching setup shown in Fig. 3-28)

3.5 Endurance test (continuous switching mode experimental demonstration) of 15kV SiC MOSFET in DC-DC converters

This section presents the experimental demonstration of 15 kV SiC MOSFET at 10 kV DC output voltage using DC-DC boost converter. The boost converter circuit is shown in Fig. 3-2 (b)-(c) and experimental setup for boost converter shown in Fig. 3-33. Table 3-4 shows the parameters and experimental testing conditions for both unidirectional and bidirectional DC-DC converters (including operating output voltages, different loading conditions and switching frequencies). The Fig. 3-34 to Fig. 3-36 show the output voltage DC voltage (V_o), low side gate to source voltage (V_{gs}), and inductor current (I_L) for 10 kV to 8 kV output DC voltages at R load of 16 kΩ. Similarly, Fig. 3-37 and Fig. 3-38 show the DC-DC converter operation for 6 kV output voltages and at 5 kHz and 10 kHz switching frequencies respectively.

The heat sink (part no: 392-300AB) with forced air-cooling has been used [57]. The fan arrangement in the experiment is the push-pull type, i.e., one fan at the inlet and one fan at the outlet. The airflow rate of each fan is 0.0542 m^3/s. The heat sink to ambient thermal resistance (R^{th}_{H-A}) is approximately 0.11 $^oC/W$ from the datasheet [57]. The heat sink temperatures measured at the end of 30 minutes are shown in Table 3-5 to Table 3-6. The thermal images for some of the test cases are shown in Fig. 3-39 to Fig. 3-42.

Table 3-4: DC-DC boost converter parameters and experimental testing conditions

	Bi-directional boost	**Unidirectional boost converter**	
Parameter	Value	Value	Value
Input voltage	2.5 kV	1.5 kV	1.5 kV
Output voltages	8 kV, 9 kV,10 kV	6 kV, 9 kV, 10 kV	6 kV
Switching Frequency	5 kHz	5 kHz	10 kHz
Filter Inductor	140 mH	140 mH	140 mH
Output capacitor	30 µF	30 µF	30 µF
Output load conditions	4 kW at 8 kV 5.1 kW at 9 kV 6.4 kW at 10 kV	5.6 kW at 6 kV 5.1 kW at 9 kV 6.4 kW at 10 kV	5.6 kW at 6 kV
Cooling mechanism	Forced air cooling	Forced air cooling	Forced air cooling
Test duration	30 mins	30 mins	30 mins
Mode of operation	CCM	CCM	CCM

Table 3-5: Experimental and analytical Power dissipation comparison of 15 kV SiC MOSFET in unidirectional DC-DC boost converter setup

Output DC voltage	**Switching frequency**	**Gate resistance**	T_A	T_H	P_d^{exp}	P_d^{calc}	T_H^{calc}
10 kV	5 kHz	R_{gLon}=15 Ω R_{gLoff}=15 Ω	23.1°C	32.4°C	84.4 W	78.4 W	31.7°C
9 kV	5 kHz	R_{gLon}=15 Ω R_{gLoff}=15 Ω	23.1 °C	30.2 °C	64.54 W	64.52 W	30.19°C
6 kV	5 kHz	R_{gLon}=33 Ω R_{gLoff}=7.67 Ω	24°C	29.8°C	52.72 W	47.49 W	29.22°C
6 kV	10 kHz	R_{gLon}=33 Ω R_{gLoff}=7.67 Ω	24°C	36.8 °C	116.36 W	103.44 W	35.37°C

Table 3-6: Experimental and analytical Power dissipation comparison of 15 kV SiC MOSFET in bi-directional DC-DC boost converter setup

Output DC voltage	**Switching frequency**	**Gate resistance**	T_A	T_H	P_d^{exp}	P_d^{calc}	T_H^{calc}
10 kV	5 kHz	R_{gLon}=33 Ω R_{gLoff}=7.67 Ω R_{gHon}= 15 Ω R_{gHon}= 15 Ω	25.4 °C	43.8°C	167 W	141.6 W	41.0°C
9 kV	5 kHz		25.4 °C	38.1°C	115.45 W	93.14 W	35.64°C
8 kV	5 kHz		25.4 °C	35°C	87.27 W	87.4 W	35°C

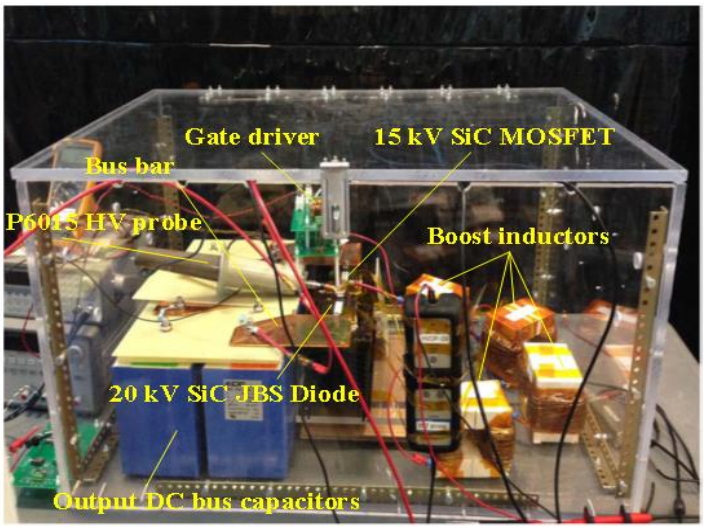


Fig. 3-33: The experimental setup of the 10 kV output DC-DC boost converter

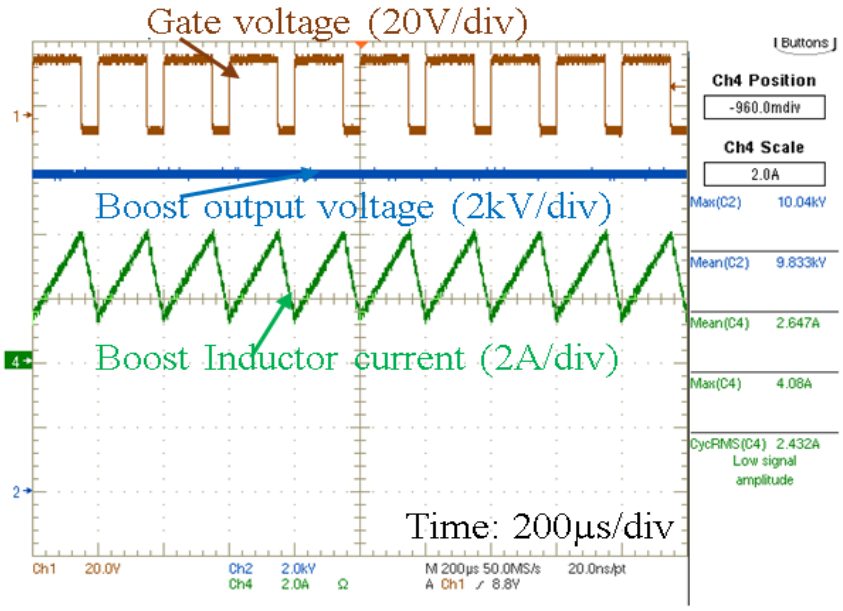


Fig. 3-34: Boost converter operation at 5 kHz, with 2.5 kV input and 10 kV output, at 6.3 kW. (Ch1: V_{gs}, Ch2: Boost output voltage, Ch4: Inductor current)

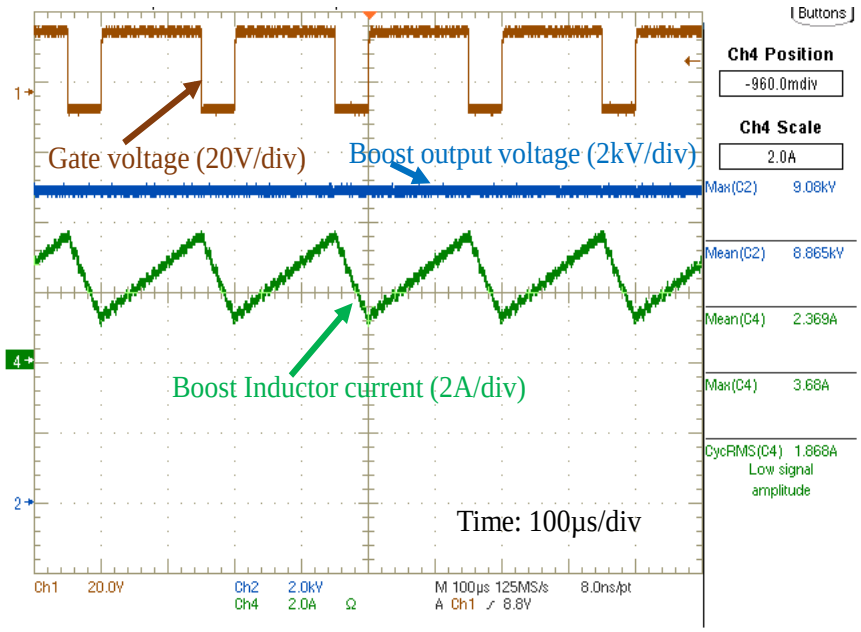


Fig. 3-35: Boost converter operation at 5 kHz, with 2.5 kV input and 9 kV output, at 5.1 kW. (Ch1: V_{gs}, Ch2: Boost output voltage, Ch4: Inductor current)

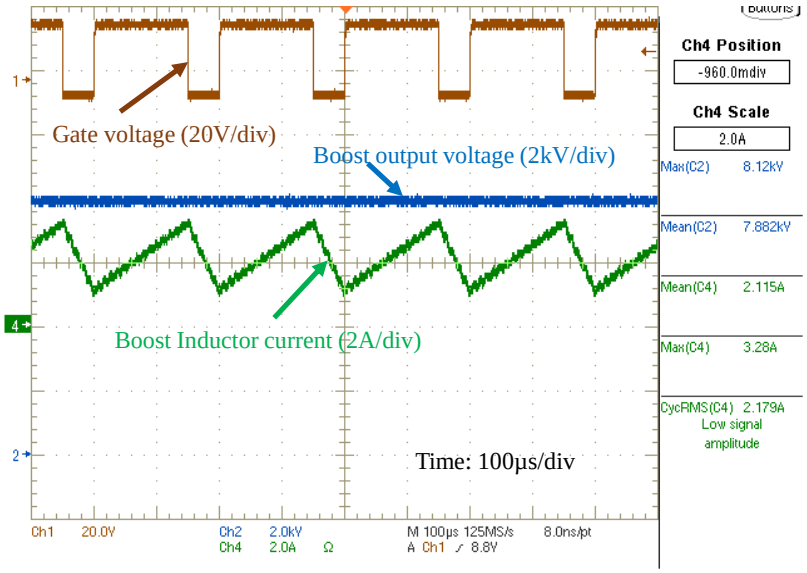


Fig. 3-36: Boost converter operation at 5 kHz, with 2.5 kV input and 8 kV output, at 4 kW. (Ch1: V_{gs}, Ch2: Boost output voltage, Ch4: Inductor current)

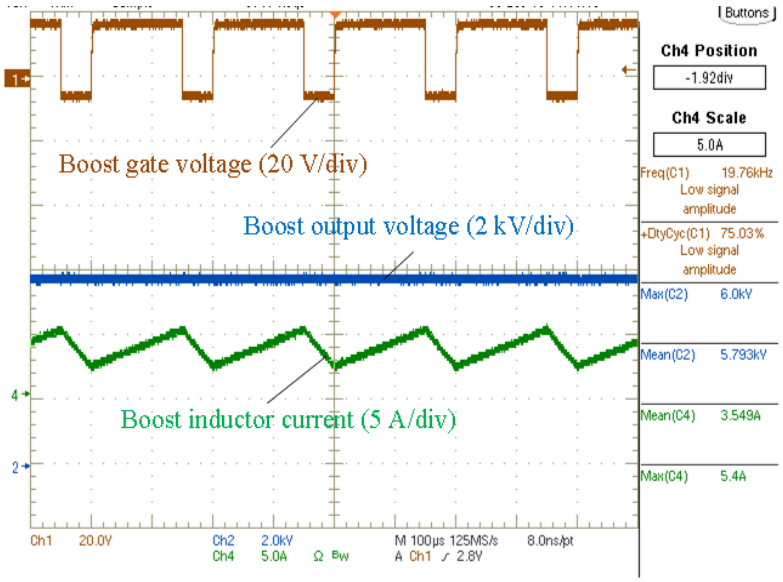


Fig. 3-37: Boost converter operation at 5 kHz, with 1.5 kV input and 6 kV output, at 5.6 kW. (Ch1: V_{gs}, Ch2: Boost output voltage, Ch4: Inductor current)

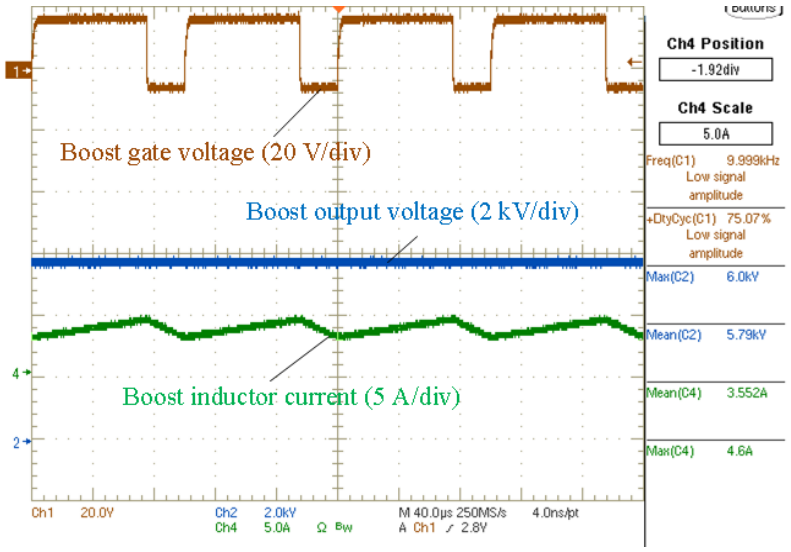


Fig. 3-38: Boost converter operation at 10 kHz, with 1.5 kV input and 6 kV output, at 5.6 kW. (Ch1: V_{gs}, Ch2: Boost output voltage, Ch4: Inductor current)

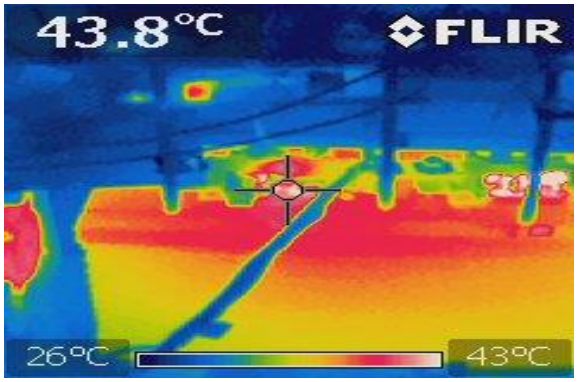


Fig. 3-39: Heat sink temperature near the base plate of 15 kV SiC MOSFET in bi-directional boost setup at 10 kV output voltage, f_{sw}=5 kHz, 6.3 kW load

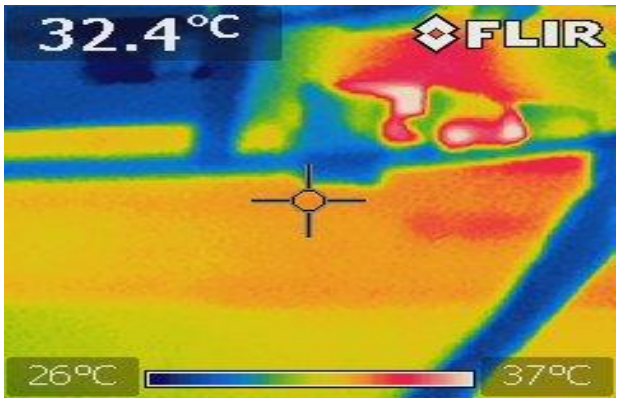


Fig. 3-40: Heat sink temperature near the base plate of 15 kV SiC MOSFET in unidirectional boost setup at 10 kV output voltage, f_{sw} =5 kHz,6.3 kW load

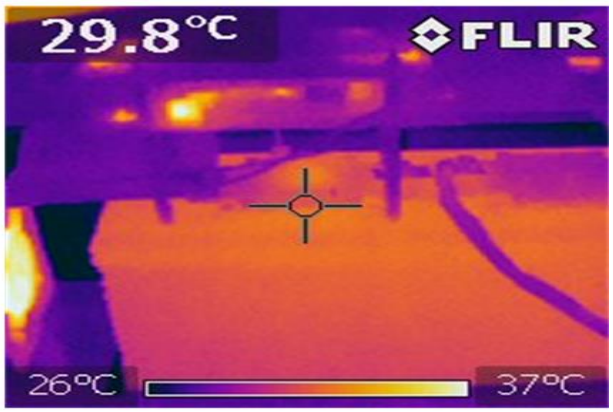


Fig. 3-41: Heat sink temperature near the base plate of 15 kV SiC MOSFET in unidirectional DC-DC boost setup at 6 kV output voltage, f_{sw}=5 kHz, 5.6 kW load

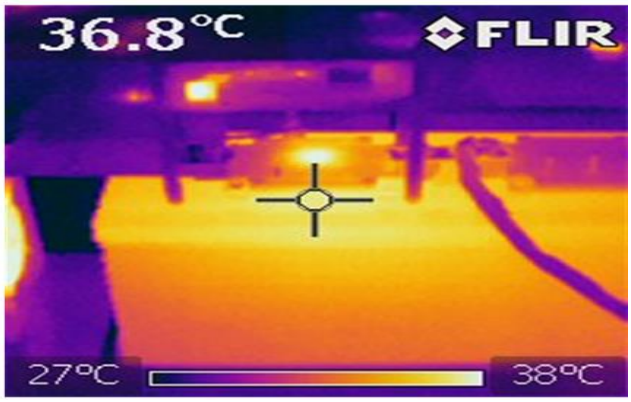


Fig. 3-42: Heat sink temperature near the base plate of 15 kV SiC MOSFET in unidirectional DC-DC boost setup at 6 kV output voltage, f_s=10 kHz, 5.6 kW load

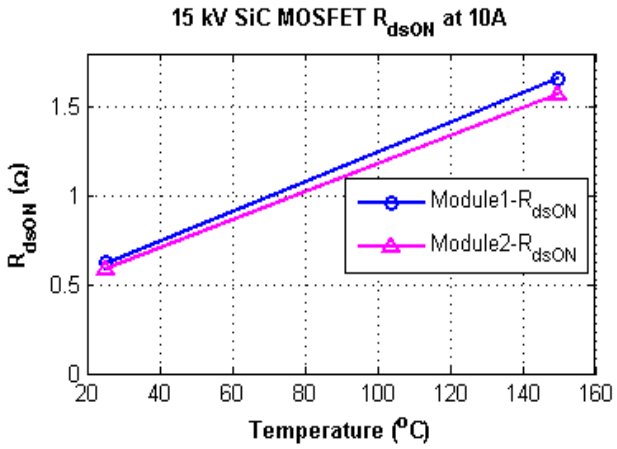


Fig. 3-43: 15 kV SiC MOSFET On-state resistance (R_{dson}) variation with junction temperature (T_j)

The power dissipated in the 15 kV SiC MOSFET module from experiment is calculated using (3-4) from measured heat sink temperature (T_H), ambient temperature (T_A) and heat sink thermal resistance (R^{th}_{H-A}). Theoretical total device power loss (P_d^{calc}) can be computed using (3-5) and characterized switching loss data obtained in earlier sections and on state resistance (R_{dson}) from Fig. 3-43; Where P_{sw}: total switching losses, P_{cond}: conduction losses, I_{sw}: switching current, D: duty ratio.

The theoretical total device power dissipation (P_d^{calc}) and heat sink temperature (T_H^{calc}) computed using the characterized loss data is very close to measured heat sink temperature (T_H) and calculated experimental loss (P_d^{exp}) as shown in Table 3-5 and Table 3-6.

$$(P_d^{exp}) = \frac{\Delta T}{R_{H-A}^{th}} = \frac{T_H - T_A}{R_{H-A}^{th}}; \quad (3\text{-}4)$$

$$\begin{aligned} P_{sw} &= E_{total} \bullet f_s \\ P_{cond} &= V_{fwd} \bullet I_{sw} \bullet D \\ E_{total} &= E_{on} + E_{off} = f(I_{sw}, R_{gon}, R_{goff}, V_{ds}) \\ (P_d^{calc}) &= P_{sw} + P_{cond} \\ T_H^{calc} &= (P_d^{calc} \bullet R_{H-A}^{th}) + T_A \end{aligned} \quad (3\text{-}5)$$

3.6 Characterization of 15 kV SiC IGBT module (two parallel dies)

3.6.1 Characterization of 15 kV/40A SiC IGBT

In order to evaluate the MV converter using 15 kV/40 A SiC IGBT devices (two 20 A IGBT dies in parallel as in Fig. 3-1(b)), the switching characteristics and On-state voltage drop is required. Some of the work related to 15 kV/40 A SiC IGBT is reported in [39] at lower switching voltages (5 kV) and up to 10 A switching current. The reported characterization is also not useful for evaluating MV VSI converter, as the device is not characterized using phase-leg configuration DPT setup as in Fig. 3-3(c), but characterized using DPT setup shown in Fig. 3-3(a). There is a significant difference in measured turn-on losses of the device between these two setups. Therefore, this section presents the switching characterization at higher DC bus voltages (up to 8 kV) and up to 20 A switching current using DPT setup shown in Fig. 3-3(c) In addition, it presents the difference in turn-on losses in the device using these two DPT setups (Fig. 3-3 (a) and Fig. 3-3 (c)).

Table 3-7 shows the comparison of turn-on losses (E_{on}) in 15 kV/40A SiC IGBT using two DPT setups Fig. 3-3 (a), Fig. 3-3(c)). It shows the effect of *dv/dt* and device output capacitance on turn-on loss characterization. There is a significant change in turn-on loss reported for a given dc bus voltage, switching current and gate resistance. Therefore, proper usage of DPT setup is necessary for HV SiC devices operating with high '*dv/dt'* and 'output capacitances'.

To evaluate, MV VSI converter, switching characterization of SiC IGBT using phase leg configuration is the correct DPT setup to be used. Therefore, switching characterization of 15 kV/40 A SiC IGBT is performed at different switching voltages and currents using DPT setup Fig. 3-3 (c). Fig. 3-44 and Fig. 3-45 show the turn-off switching characterization at 8 kV, 15 A and at a junction

temperature of 25^0C and 150^0C, turn-off gate resistance (R_{gH_off} =R_{gL_off}) of 7.5 Ω. Fig. 3-46 shows the turn- off loss (E_{off}) variation with the temperature at different switching current. There is nearly 2.5 to 3 times increase in turn-off losses from T_j=25^0C to T_j=150^0C, for a given dc bus voltage and switching current.

Table 3-7: Comparison of turn-on losses in 15 kV/40 A SiC IGBT using two DPT setups

	Phase leg configuration using setup Fig. 3-3(c) ((R_{gL_on}=R_{gL_off}=33Ω,R_{gH_on} R_{gH_off}=33Ω)		**High side JBS diode and low side 15kV/40A SiC IGBT module using setup Fig. 3-3 (a) (R_{gon}=33Ω)**	
Switching voltage and current	**Turn-on Peak current in the device (A)**	**Turn-on losses (E_{on}) (mJ)**	**Turn-on Peak current in the device (A)**	**Turn-on losses (E_{on}) (mJ)**
8 kV, 5 A	13.01	22.88	9.2	18.25
8 kV, 7 A	15.82	28.36	12.41	24.48
8 kV, 10 A	20.43	38.17	16.06	32.27
8 kV, 12 A	23.3	43.68	19.02	38.2
7 kV, 5 A	12.87	18.23	9.28	14.75
7 kV, 7 A	15.44	22.42	12.25	19.23
7 kV, 10 A	20.13	30.81	16.04	25.73
7 kV, 12 A	22.67	34.69	19.2	30.51

Similarly, turn-on switching characterization is performed. Fig. 3-47 shows the turn-on switching characterization at 8 kV, 15 A and at a junction temperature of 25^0C, turn-on gate resistance is (R_{gH_on} =R_{gL_on}) 33 Ω. The change (decrease) in turn-on losses in SiC IGBT with temperature is very small [38][39] [46]. Therefore, it is reasonable to assume the turn-on losses at 25^0C is nearly equal to turn-on losses at 150^0C. The total switching losses (E_{sw}) of 15kV/40A SiC IGBT are the sum of turn-on losses and turn-off losses are shown in Fig. 3-48 for dc bus voltages of 7 kV and 8 kV for different switching currents at T_j=150^0C.

The on-state voltage drop of 15 kV/40 A SiC IGBT (5μm buffer layer) has been characterized by Wolf speed Inc. Fig. 3-49 shows the variation of on-state voltage (V_{cesat}) drop with temperature for different current values. Therefore, using the characterized switching loss and on-state voltage drop, the total loss and efficiency of MV VSI converter can be evaluated for DC bus voltage of up to 8 kV and AC voltages of 4.6 kV (L-L).

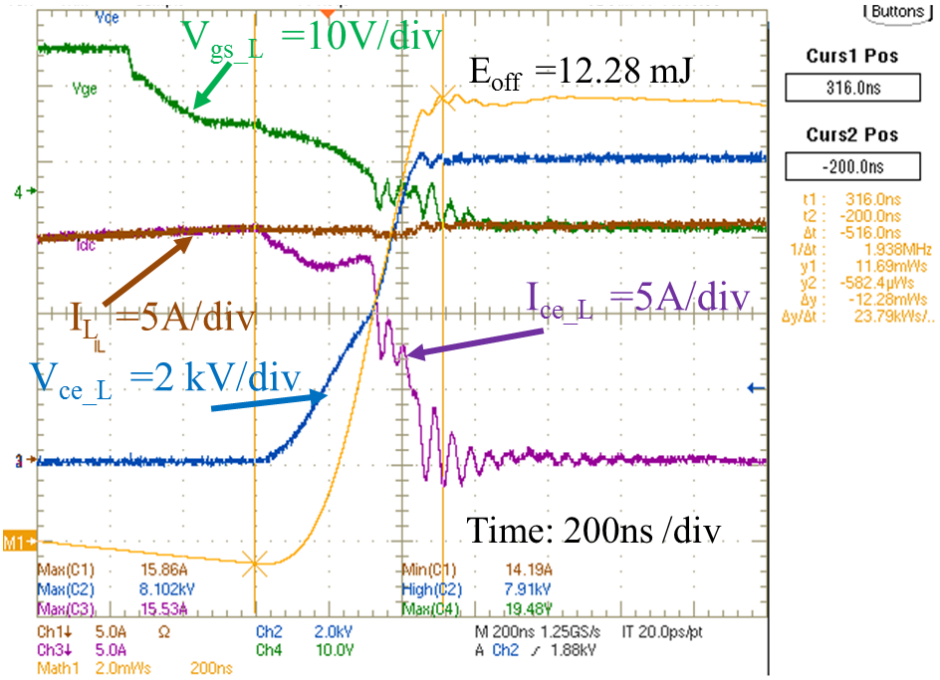


Fig. 3-44: Turn-off losses (12.28 mJ) of 15 kV/40 A SiC IGBT at 8 kV 15 A and at 25^{0}C, R_{gH_of}=R_{gL_off}: 7.5 Ω (with Phase leg configuration)

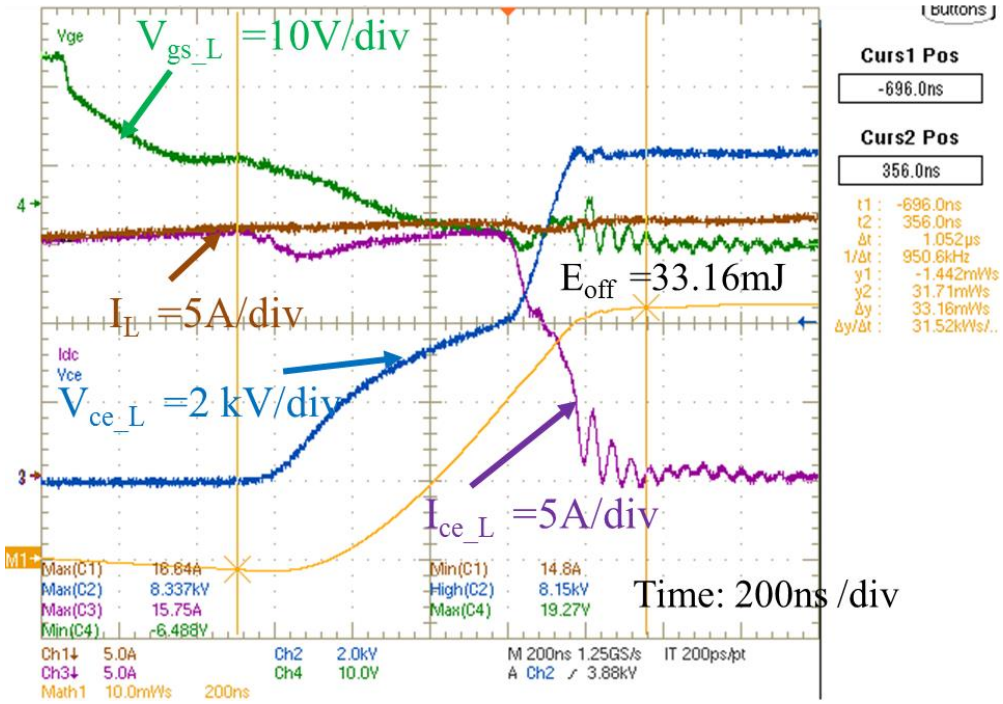


Fig. 3-45: Turn-off losses (33.16 mJ) of 15 kV/40 A SiC IGBT at 8 kV 15 A and at 150^{0}C, R_{gH_of}=R_{gL_off}: 7.5 Ω (with Phase leg configuration)

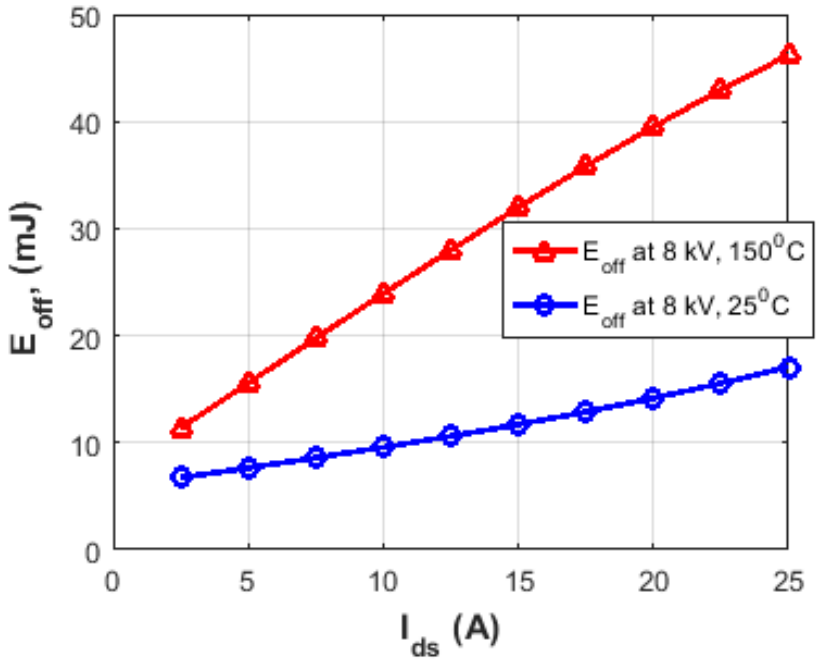


Fig. 3-46: Turn-off loss (E_{off}) variation with temperature for different values of current at 8 kV dc bus, R_{gH_off}= R_{gL_off} =7.5 Ω

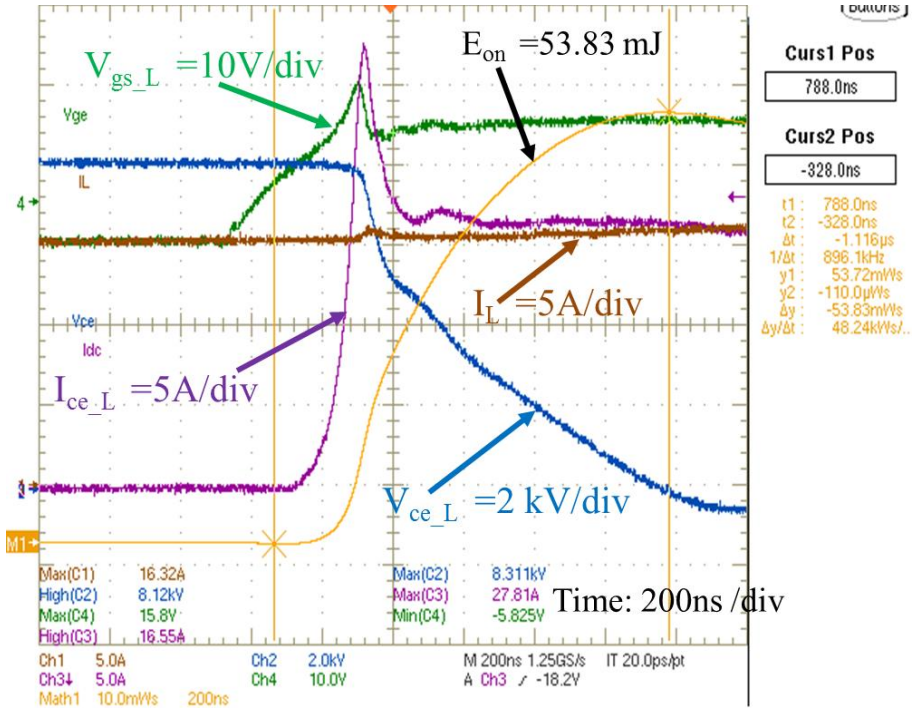


Fig. 3-47: Turn-on losses (53.83 mJ) of 15 kV/40 A SiC IGBT at 8 kV 15 A and at 25^{0}C, R_{gL_on}: 33 Ω (with Phase leg configuration)

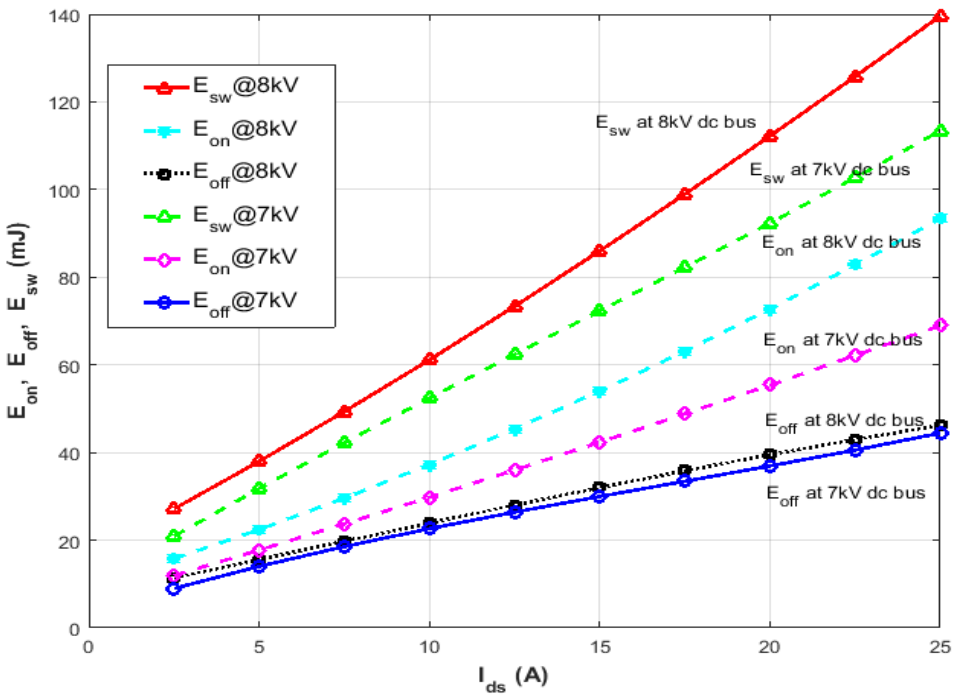


Fig. 3-48: Turn-on loss (E_{on}), Turn-off loss (E_{off}), and Total switching loss (E_{sw}) of 15 kV/40 A SiC IGBT for different switching currents, at T_j=150^{0}C, R_{gH_on}= R_{gL_on} =33 Ω, R_{gH_off}= R_{gL_off} =7.5 Ω

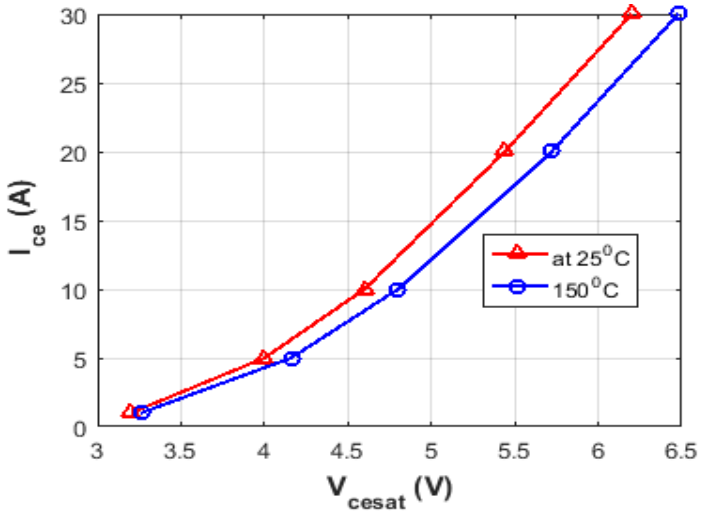


Fig. 3-49: On-state voltage drop of 15 kV/40 A SiC IGBT (5μm)

3.7 Comparison of 15 kV SiC MOSFET and 15 kV SiC IGBT devices and switching frequency limits

This section presents their switching frequency limits using the characterized loss data. Table 3-8 shows the HV SiC devices used for the comparison.

Table 3-8: Chip area of 15 kV SiC MOSFET and 15 kV SiC IGBT devices

HV SiC Module	Total no of parallel chips	Chip area per die	Total chip area
15 kV/15A SiC MOSFET	2	0.64 cm^2 (0.8cm x0.8 cm)	1.28 cm^2
15 kV/20 A SiC IGBT	1	0.7056 cm^2 (0.84 cm x 0.84 cm)	0.7056 cm^2
15 kV/40 A SiC IGBT	2	0.84 cm^2 (0.84 cm x1 cm)	1.68 cm^2

3.7.1 Comparison of 15 kV SiC MOSFET (two dies) and 15 kV SiC IGBT (single die) device

The 15 kV/20A SiC IGBT (single die) device has been characterized in [38] using DPT setup similar to Fig. 3-3 (a). Therefore, the loss data from the reference [38] has been taken to compare with 15 kV SiC MOSFET. For the 15 kV SiC MOSFET, the characterized switching loss data is taken from section 3.3 (using DPT shown in Fig. 3-3 (a).) and on-state resistance data has been taken from section 3.5.

The comparison of 15 kV SiC MOSFET results with 15 kV/20A SiC IGBT is made at same turn-on and turn-off *dv/dt*. The reason for *dv/dt* based comparison is outlined in the introduction section 3.1. The 15 kV SiC IGBT *dv/dt* of turn-on and turn-off are calculated from the switching voltage plots mentioned in [38]. The 15 kV SiC IGBT has two slopes in the voltage transition at turn-on and turn-off due to punch through design. The *dv/dt* of 15 kV SiC IGBT is maximum during the voltage transition in the punch-through region. The turn-on dv/dt at 10 kV 10A is 45 kV/µs and turn-off *dv/dt* is 32 kV/µs during punch-through region. The gate resistances used for 15 kV SiC IGBT characterization are R_{gon} =20 Ω and R_{goff} =10 Ω [38]. Since the 15 kV SiC MOSFET module does not have the same input and output capacitances as that of 15 kV IGBT, hence the same values of gate resistance cannot yield the same *dv/dt* values. So the 15 kV SiC MOSFET has been characterized at different gate resistances in section 3.3 and it has been identified that the gate resistances R_{gon} =14.7

Ω and R_{goff} =16.5 Ω gives the same turn-on and turn-off *dv/dt* as that of 15 kV SiC IGBT using setup shown in Fig. 3-3 (a) for evaluating unidirectional DC-DC converter.

The Fig. 3-50 shows the switching loss comparison of 15 kV SiC MOSFET and 15 kV SiC IGBT at 25°C using the loss data obtained from setup shown in Fig. 3-3(a) in Section 3.2 and from reference [38]. Fig. 3-51 shows the turn-off loss comparison of 15 kV SiC MOSFET and 15 kV SiC IGBT with the temperature at 10 kV, 5A and 10 kV, 10A. The turn-on losses of 15kV SiC IGBT (single die) with temperature is not available in the literature. The turn-on energy loss of 15 kV SiC IGBT slightly decreases with increase in temperature [46][38]. Therefore, the decrease in turn-on loss with temperature is neglected for 15 kV SiC IGBT in this work. This provides the most pessimistic (lowest) switching frequency limit values for the 15 kV SiC IGBT, whereas for the 15 kV SiC MOSFET, the turn-on loss with the variation of temperature is characterized in section 3.2.

At higher junction temperatures, the 15 kV SiC IGBT's (single die) total switching loss (E_{sw}) is more than 15 kV SiC MOSFET as shown in Fig. 3-52. This is due to significant increase in turn-off losses with temperature in 15 kV SiC IGBT compared to 15 kV SiC MOSFET as shown in Fig. 3-51. Table 3-9 shows the summary of switching losses and the on-state voltage drop at 125°C. Using the above-mentioned loss data of 15 kV SiC MOSFET and 15 kV SiC IGBT, the switching frequency limits of 15 kV SiC MOSFET with 15 kV SiC IGBT for unidirectional DC-DC converter and the converter loss analysis is carried out using analytical formulae mentioned in [60] and verified using MATLAB/PLECS simulation.

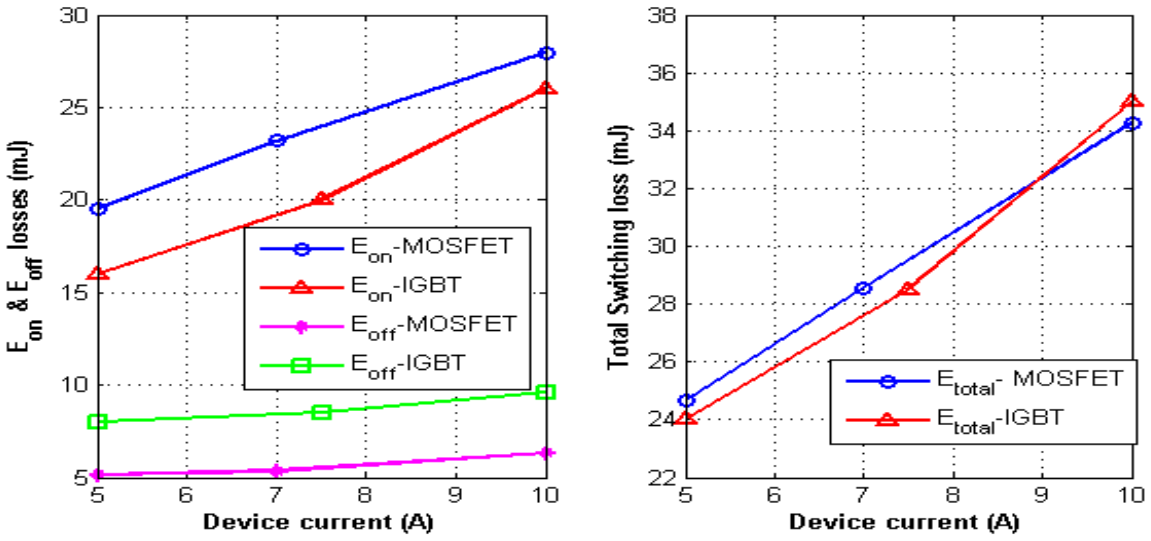


Fig. 3-50: Comparison of Turn-on(E_{on}), Turn-off (E_{off}) and Total switching loss at 10 kV dc bus and at turn on *dv/dt*=45 kV/µs, turn-off *dv/dt* =32 kV/µs (for both MOSFET and IGBT) , T_j= 25°C

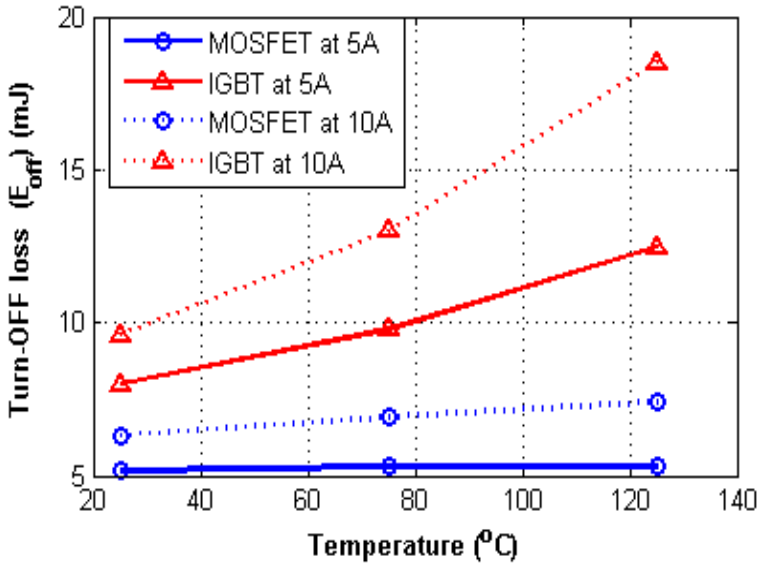


Fig. 3-51: Turn-off loss comparison with temperature at 10 kV dc bus and at turn on *dv/dt*=45 kV/µs, turn-off *dv/dt* =32 kV/µs (for both MOSFET and IGBT)

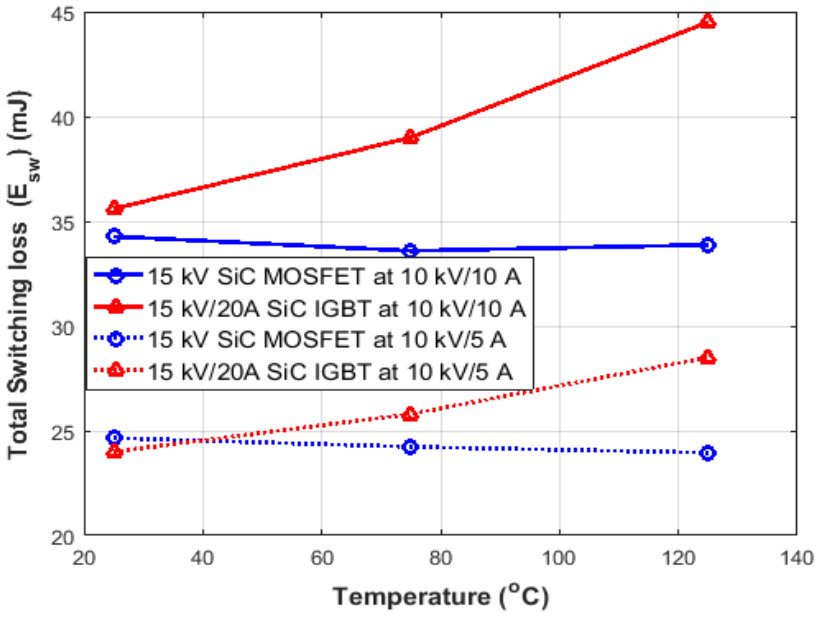


Fig. 3-52: Total switching loss with junction temperature at turn on *dv/dt*=45 kV/µs, turn-off *dv/dt* =32 kV/µs (for both MOSFET and IGBT)

Table 3-9: Comparison of switching loss and ON-state voltage

At 10 kV Switching voltage, T_j: 125^{o}C					
	Device current	E_{on} (mJ)	E_{off} (mJ)	E_{sw} (mJ)	V_{on} (V)
15 kV SiC MOSFET	at 5 A	19.5	5.2	24.7	7.35
15 kV/20 A SiC IGBT		16	12.5	28.5	4.8
15 kV SiC MOSFET	at 10 A	27.9	6.3	34.2	14.7
15kV/20A SiC IGBT		26	18.5	44.5	5.2

The thermal resistance of 15 kV IGBT co-pack module (single IGBT die and anti-parallel JBS diode) from the junction to ambient has been extensively evaluated in [38]. The power dissipation density of 15 kV/20 A SiC IGBT is 550 W/cm^2 with 0.0542 m^3/s forced air cooling, while the thermal resistance of 15 kV SiC IGBT module from the junction to the case has been calculated to be **0.49^{o}C/W**. The 15 kV SiC MOSFET co-pack module is done with the similar thermal package (junction to the isolated base plate) as that of 15 kV SiC IGBT, but there are two number of MOSFET chips in parallel in a module compared to one chip in 15 kV SiC IGBT module. Hence the thermal resistance of 15 kV MOSFET co-pack module from the junction to ambient is estimated from normalized chip areas. The **chip area of 15 kV SiC IGBT is 0.7056 cm^2, the chip area of 15 kV SiC MOSFET is 1.28 cm^2** (two chips with 0.64 cm^2 each). The thermal resistance of 15 kV SiC MOSFET module =0.49x [0.7056/1.28]=**0.27 ^{o}C/W**. It is slightly underestimated value because the thermal duty spread in various layers (Top DBCu, AlN, Bottom DBCu etc.) in a module package from the junction to base plate. The thermal resistance of heat sink to ambient is approximately 0.11 ^{o}C/W [57] and thermal resistance of heat sink to the case (thermal grease) is approximately 0.05 ^{o}C/W. Therefore, the thermal resistance of 15 kV SiC MOSFET module from the junction to the ambient is 0.43 ^{o}C/W (approx.). Assuming the maximum safe junction temperature as 150^{0}C and the ambient temperature at 25^{0}C, the **15 kV SiC MOSFET module can dissipate the total power of 307 W**. Table 3-10 shows the thermal resistance of all the HV SiC modules.

Table 3-10: Thermal resistance of HV SiC modules

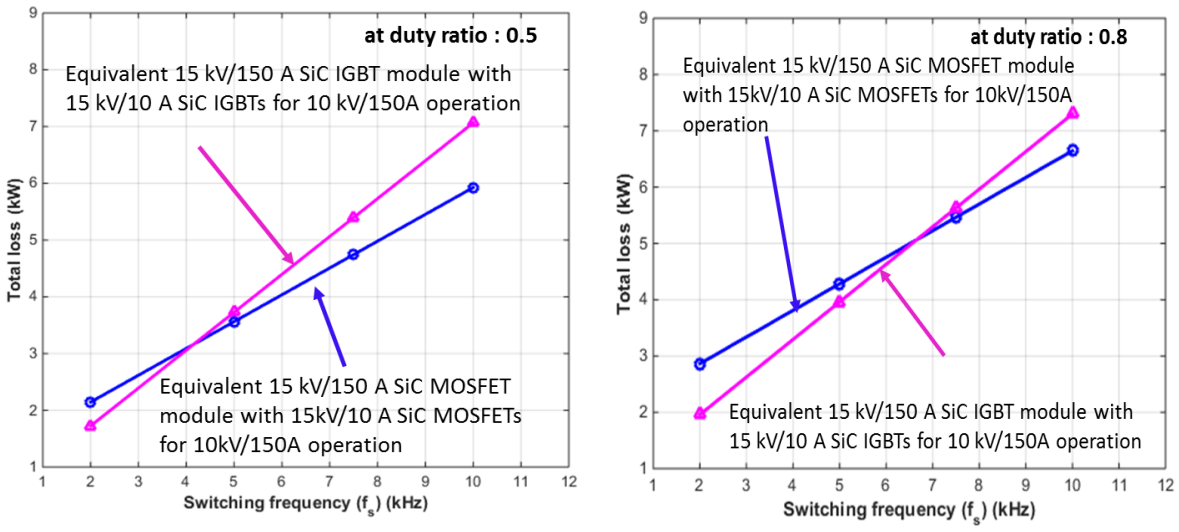
	Thermal resistance			
Module	**junction to Case**	**Case to heat sink**	**Heat sink to ambient**	**Total thermal resistance junction to ambient**
15 kV SiC IGBT (Single die)	0.49 ^{0}C/W	0.05^{0}C/W	0.11^{0}C/W	0.65 ^{0}C/W
15 kV SiC IGBT (Two parallel dies)	0.2058 ^{0}C/W	0.05^{0}C/W	0.11^{0}C/W	0.3658 ^{0}C/W
15 kV SiC MOSFET (Two parallel dies)	0.27 ^{0}C/W	0.05^{0}C/W	0.11^{0}C/W	0.43 ^{0}C/W

Table 3-11 shows the comparison of switching frequency limits for 15 kV SiC MOSFET module (with two parallel dies) and 15 kV SiC IGBT module (with a single die) in unidirectional DC-DC boost converter for output DC voltage 10 kV, input currents of 10 A and 5 A at different duty cycles (D). The switching frequency limits of 15 kV SiC MOSFET before its junction temperature reaches 149.5^{0}C are nearly 5 kHz- 9 kHz for 10 kV,10 A operation and 11 kHz-12 kHz for 10 kV,5 A operation. The widespread of switching frequency limits at 10 kV/10 A operation for different duty ratio (D) is due to a significant share of SiC MOSFET conduction losses in the total losses. For 10 kV/ 5A operation, the conduction losses are much less than switching losses. Therefore, the switching frequency limits are nearly constant for each duty ratio (D). For any operating current and duty ratio, the 15 kV SiC MOSFET is favorable for operating at higher switching frequency compared to 15 kV SiC IGBT for same *dv/dt* conditions.

Table 3-12 shows the efficiency comparison of 15 kV SiC MOSFET and 15 kV SiC IGBT in a unidirectional DC-DC boost converter for 10 kV DC output voltage. In a unidirectional DC-DC converter, for the same input current of 5A, high switching frequency (5 kHz), the 15 kV SiC MOSFET has a lower total loss and higher efficiency than the 15 kV SiC IGBT. However, for an input current of 10 A and low switching frequency (2.9 kHz), the 15 kV SiC IGBT has a lower total loss and higher efficiency than the 15 kV SiC MOSFET.

Table 3-11: Switching frequency limits of 15 kV SiC MOSFET (two parallel dies) and 15 kV SiC IGBT (single die) in Unidirectional DC-DC boost converter for 10 kV output DC voltage for T_j =149.5^{0}C

Unidirectional DC-DC Boost converter	Input current	Output voltage	Input power	Duty ratio (D)	Switching Frequency limit	Switching Losses	Conduction losses
with 15 kV SiC MOSFET	10 A	10kV	20 kW	0.8	5.1 kHz	157.45 W	132 W
	10 A	10 kV	75 kW	0.25	8.1 kHz	248.52 W	41.2 W
	10 A	10 kV	90 kW	0.1	8.85kHz	273.23 W	16.5 W
with 15 kV SiC MOSFET	5 A	10kV	10 kW	0.8	10.7 kHz	256.15 W	33 W
	5 A	10 kV	37.5 kW	0.25	11.7 kHz	280.1 W	10.3 W
	5 A	10 kV	45 kW	0.1	11.9 kHz	284.88 W	4.12 W
With 15 kV/20 A SiC IGBT	10 A	10kV	20 kW	0.8	2.9 kHz	137.85 W	53.2W
	10 A	10 kV	75 kW	0.25	3.7 kHz	178.88W	16.62 W
	10 A	10 kV	90 kW	0.1	3.9 kW	185.39 W	6.65 W
with 15 kV/20 A SiC IGBT	5 A	10kV	10 kW	0.8	5.2 kHz	169 W	22.1W
	5 A	10 kV	37.5 kW	0.25	5.65 kHz	185.25 W	6.9 W
	5 A	10 kV	45 kW	0.1	5.8 kHz	188.5 W	2.76 W



(a) (b)

Fig. 3-53: Comparison of total losses (P_T=P_{sw} + P_{cond}) for equivalent 15 kV/150 A SiC MOSFET and 15 kV/150 A SiC IGBT modules for 10 kV, 150 A operation (assuming 15 parallel modules or dies (15 kV/10 A) connected)

Table 3-12: Efficiency comparison of 15 kV SiC MOSFET(two parallel dies) and 15 kV SiC IGBT(single die per module) in unidirectional DC-DC boost converter

Using loss From Diode and Co-pack module setup				
Unidirectional DC-DC Boost converter	**With 15 kV SiC MOSFET (D=0.8)**		**With 15 kV SiC IGBT (D=0.8)**	
Input current	5 A	10 A	5 A	10 A
Switching Frequency	5.2 kHz	2.9 kHz	5.2 kHz	2.9 kHz
MOSFET or IGBT Switching Losses	124.48 W	89.5 W	169 W	137.8 W
Freewheeling Diode Switching losses	0	0	0	0
MOSFET or IGBT Conduction losses	33 W	132 W	22.1 W	53.2 W
Freewheeling Diode Conduction losses	13.5 W	27 W	13.5 W	27 W
Total loss	170.98 W	248.53 W	204.6 W	218.05 W
Thermal resistance junction to Ambient	0.43^0C/W	0.43^0C/W	0.65^0C/W	0.65^0C/W
Ambient temperature	25 ^{o}C			
Junction temperature (T_j)	92.7 ^{o}C	120.24 ^{o}C	149.2 ^{o}C	149.2 ^{o}C
Efficiency (%)	98.32	98.77	97.99	98.92

Fig. 3-53 shows the comparison of total losses ($P_T=P_{sw} + P_{cond}$) for equivalent 15 kV/150A SiC MOSFET and 15 kV/150 A SiC IGBT modules for 10 kV, 150 A operation (assuming 15 parallel modules or dies of 15 kV/ 10 A connected to scale the current). The breakeven switching frequency is the frequency at which total losses using equivalent 15 kV/150 A SiC IGBT and 15 kV/150 A SiC MOSFET modules are equal. The breakeven switching frequency is nearly 4 kHz and 6.5 kHz at a duty ratio of 0.5 and 0.8 respectively. For switching frequency < 4 kHz, the equivalent 15 kV/150 A SiC IGBT has a lower total loss compared to equivalent 15 kV/150 A SiC MOSFET for the duty ratio of 0.5. Similarly, for switching frequency < 6.5 kHz, the equivalent 15 kV/150 A SiC IGBT has a lower total loss compared to equivalent 15 kV/150 A SiC MOSFET for the duty ratio of 0.8.

3.7.2 Comparison of 15 kV SiC MOSFET (two dies) and 15 kV SiC IGBT (two dies) device

This section presents the comparison of 15 kV SiC MOSFET (two dies) and 15 kV SiC IGBT (two dies) and their switching frequency limits for the bi-directional DC-DC converter. For 15 kV SiC MOSFET, the characterized loss data from section 3.4 - 3.5 is used and for 15 kV SiC IGBT, the characterized loss data from section 3.6 is used. The switching loss data used for both devices is taken for the same gate resistance (R_{gon}=33 Ω and R_{goff}=7.5 Ω). The corresponding turn-on and turn-off '*dv/dt'* values for both devices at 8 kV10 A and at the same gate resistance are shown Table 3-13.

Table 3-13: The turn-on, turn-off dv/dt values of 15 kV SiC MOSFET and 15 kV SiC IGBT(two parallel dies in each module) for the same gate resistance (R_{gon}=33 Ω and R_{goff}=7.5 Ω)

	15 kV SiC MOSFET		15 kV/40 A SiC IGBT	
Switching voltage and current	**Turn-on dv/dt**	**Turn-off dv/dt**	**Turn-on dv/dt**	**Turn-off dv/dt**
8 kV, 10A	20 kV/µs	30 kV/µs	24 kV/µs	36 kV/µs

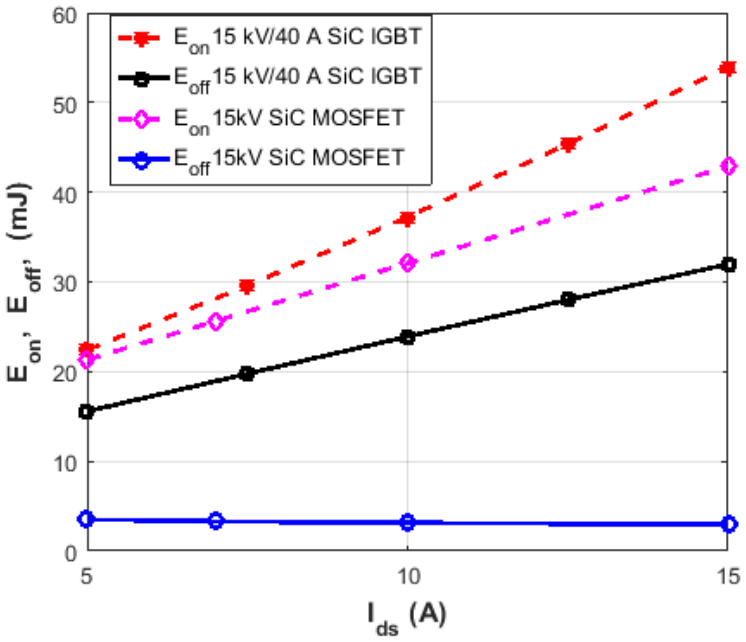


Fig. 3-54: Turn-on and Turn-off loss comparison of 15 kV SiC MOSFET and 15 kV SiC IGBT (two parallel dies in each module) at 8 kV dc bus, for different switching currents and at T_j=150^{0}C, R_{gon}=33 Ω, R_{goff}=7.5 Ω

Fig. 3-54 shows the turn-on and turn-off loss comparison of 15 kV SiC MOSFET module and 15 kV SiC IGBT module at 8 kV dc bus, T_j=150^{0}C using the loss data obtained in sections 3.4 - 3.6. The turn-on losses are comparable to each other, but the turn-off losses in SiC IGBT are much (5 to 7 times) higher compared to SiC MOSFET. The Fig. 3-55 shows the total switching loss comparison of 15 kV SiC MOSFET module (with two parallel dies) and 15 kV SiC IGBT module (with two parallel dies) at 8 kV dc bus, T_j=150^{o}C. There is a significant increase in the total switching loss in SiC IGBT compared to SiC MOSFET. The summary of switching losses and on-state voltage drops are shown in Table 3-14.

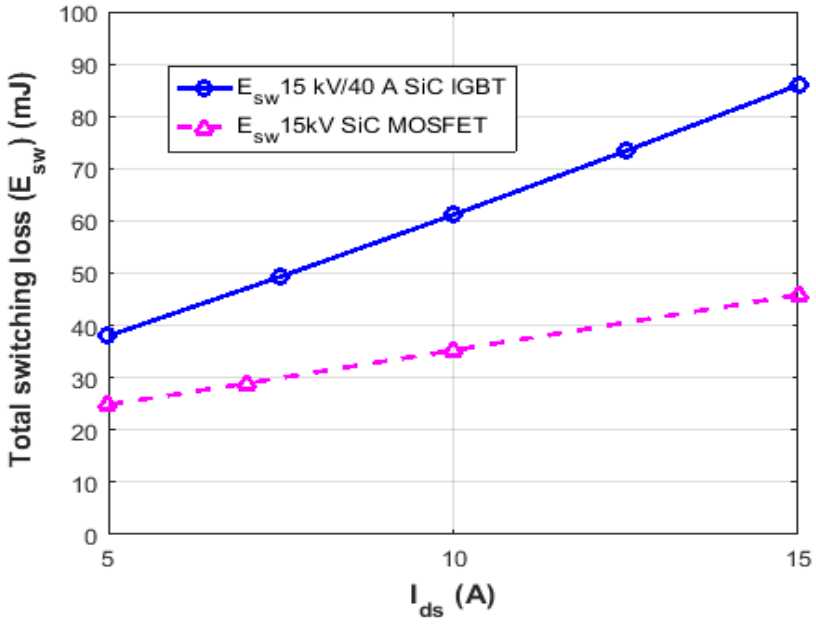


Fig. 3-55: Total switching loss comparison of 15 kV SiC MOSFET and 15 kV SiC IGBT (two parallel dies in each module) at 8 kV dc bus, for different switching currents and at T_j=150^{0}C, R_{gon}=33 Ω and R_{goff}=7.5 Ω

Table 3-14: Comparison of switching loss and ON-state voltage

At 8 kV switching voltage, T_j: 150^{0}C					
	Device current	E_{on} (mJ)	E_{off} (mJ)	E_{sw} (mJ)	V_{on} (V)
15 kV SiC MOSFET	at 5 A	21.31	3.52	24.83	8.25
15 kV/40 A SiC IGBT		22.42	15.56	37.98	4.16
15 kV SiC MOSFET	at 10 A	32.1	3.14	35.24	16.5
15 kV/40 A SiC IGBT		37.23	23.91	61.14	4.8

Similar to the unidirectional DC-DC boost converter evaluation in section 3.7.1, in this section, the evaluation of switching frequency limits of 15 kV SiC MOSFET and 15 kV SiC IGBT for a bi-bidirectional DC-DC converter have been provided for 8 kV dc output voltage using the above loss data (characterized using phase-leg configuration DPT setup).

Table 3-15: Switching frequency limits of 15 kV SiC MOSFET and 15 kV SiC IGBT (two parallel dies in each module) in bi-directional DC-DC boost converter for 8 kV output DC voltage for T_j =149.5^{0}C

Device	Input current	Output voltage	Input power	Duty ratio (D)	Switching Frequency limit	Device switching Losses	Device conduction losses
15 kV SiC MOSFET	10 A	8 kV	4 kW	0.95	3.8 kHz	133.9 W	156.75 W
	10 A	8 kV	16 kW	0.8	4.5 kHz	158.58 W	132 W
	10 A	8 kV	24 kW	0.7	4.96 kHz	174.79 W	115.5 W
	10 A	8 kV	40 kW	0.5	5.9 kHz	207.92 W	82.5 W
	10 A	8 kV	60 kW	0.25	7.05 kHz	248.44 W	41.25 W
	10 A	8 kV	72 kW	0.1	7.75 kHz	273.1 W	16.5 W
15 kV SiC MOSFET	5 A	8 kV	2 kW	0.95	10.1 kHz	250.88 W	39.2 W
	5 A	8 kV	8 kW	0.8	10.3 kHz	258.85 W	33 W
	5 A	8 kV	12 kW	0.7	10.47 kHz	260 W	28.75 W
	5 A	8 kV	20 kW	0.5	10.85 kHz	260.95 W	20.63 W
	5 A	8 kV	30 kW	0.25	11.25 kHz	279.45 W	10.3 W
	5 A	8 kV	36 kW	0.1	11.5 kHz	285.66 W	4.12 W
15 kV/40 A SiC IGBT	10 A	8 kV	4 kW	0.95	4.6 kHz	281.24 W	59.37 W
	10 A	8 kV	16 kW	0.8	4.75 kHz	290.4 W	50 W
	10 A	8 kV	24 kW	0.7	4.85 kHz	296.53W	43.75 W
	10 A	8 kV	40 kW	0.5	5.05 kHz	308.75 W	31.25 W
	10 A	8 kV	60 kW	0.25	5.31 kHz	324.65 W	15.6 W
	10 A	8 kV	72 kW	0.1	5.46 kHz	333.82 W	6.25 W
15 kV/40 A SiC IGBT	5 A	8 kV	2 kW	0.95	8.35 kHz	317.13 W	23 W
	5 A	8 kV	8 kW	0.8	8.45 kHz	320.93 W	19.38 W
	5 A	8 kV	12 kW	0.7	8.51 kHz	323.2 W	16.95 W
	5 A	8 kV	20 kW	0.5	8.65kHz	328.52 W	12.11 W
	5 A	8 kV	30 kW	0.25	8.8 kHz	334.22 W	6.1W
	5 A	8 kV	36 kW	0.1	8.9 kHz	338 W	2.4 W

Table 3-15 shows the comparison of switching frequency limits for 15kV SiC MOSFET module (with two parallel dies) and 15 kV SiC IGBT module (with two parallel dies) in bidirectional DC-DC boost converter for output DC voltage 8 kV, input currents of 10 A and 5 A at different duty cycles (D). The approximate switching frequency limits of 15 kV SiC MOSFET before its junction

temperature reaches 149.5^{0}C are 4 kHz - 8 kHz for 8 kV,10 A operation and 11 kHz-12 kHz for 8 kV,5 A operation. The widespread of switching frequency limits at 10A operation for different duty ratio (D) are due to a significant share of SiC MOSFET conduction losses in the total losses. Whereas, at 5 A operation, the conduction losses are much less than switching losses. Therefore, the switching frequency limits are nearly constant for each duty ratio (D). Similarly, the approximate switching frequency limits of 15 kV SiC IGBT before its junction temperature reaches 149.5^{0}C are 4.5 kHz- 5.5 kHz for 8 kV,10 A operation and 8.3 kHz - 8.9 kHz for 8 kV, 5 A operation. For any operating current and duty ratio, the 15 kV SiC MOSFET is favorable for operating at higher switching frequency compared to 15 kV SiC IGBT for same gate resistance values.

Table 3-16 shows the efficiency comparison of 15 kV SiC MOSFET and 15 kV SiC IGBT in a bidirectional DC-DC boost converter for 8 kV DC output voltage. In a bidirectional DC-DC converter, for high switching frequency and input current of 5 A , the 15 kV SiC MOSFET has a lower total loss and higher efficiency than the 15 kV SiC IGBT. However, for low switching current and input current of 10 A, the 15 kV SiC IGBT total loss is comparable to the 15 kV SiC MOSFET and the difference in the efficiency using 15 kV SiC MOSFET and 15 kV SiC IGBT in a DC-DC boost converter is very small.

Table 3-16: Efficiency comparison of 15 kV SiC MOSFET and 15 kV SiC IGBT (two parallel dies in each module) in Bidirectional DC-DC boost converter

Using loss data from phase-leg configuration setup				
Bidirectional DC-DC Boost converter	**With 15 kV SiC MOSFET (D=0.8)**		**With 15 kV SiC IGBT (D=0.8)**	
Input voltage	1600 V			
Output voltage	8000 V			
Input current	5 A	10 A	5 A	10 A
Switching Frequency	8.1 kHz	4.5 kHz	8.1 kHz	4.5 kHz
MOSFET or IGBT Switching Losses	201.2 W	158.58 W	307.63 W	275.13 W
Freewheeling Diode Switching losses	0	0	0	0
MOSFET or IGBT Conduction losses	33 W	132 W	19.38 W	50 W
Freewheeling Diode Conduction losses	13.5 W	27 W	13.5 W	27 W
Total loss	247.7 W	317.58 W	340.52 W	352.13 W
Thermal resistance junction to Ambient	0.43 ^{0}C/W	0.43 ^{0}C/W	0.3658 ^{0}C/W	0.3658 ^{0}C/W
Ambient temperature	25^{o}C			
Junction temperature (T_j)	125.7 ^{o}C	149.94 ^{o}C	144.6 ^{o}C	143.93 ^{o}C
Efficiency (%)	96.99	98.05	95.91	97.84

3.8 Conclusions

- Detailed experimental hard switching characteristics of 15 kV SiC MOSFET have been evaluated.
- Experimental results with high side module switching have been done to verify the increased 'V_{gs}' above the threshold limit of freewheeling module due to crosstalk.
- In a phase leg configuration, at low turn-on gate resistance (high turn-on dv/dt conditions) and high turn-off gate resistance, the turn-on peak current is significantly more in DUT compared to high side is SiC JBS diode due to the partial shoot-through problem. Therefore, a proper value of gate resistances has to be chosen to avoid partial shoot-through or crosstalk mitigation techniques published in the literature has to be used.
- 15 kV SiC MOSFET switching loses computed using phase leg configuration setup is slightly more compared to JBS SiC diode and SiC MOSFET setup.
- The continuous mode experimental demonstration of 15 kV SiC MOSFET has been presented for both unidirectional and bi-directional DC-DC boost converter for different output voltages loading conditions and switching frequencies. The temperature rise from the ambient to the heat sink is found to be a close match with the experimental values and also with that of analytically computed values.
- Briefly presented the 15 kV/40 A SiC IGBT (two parallel dies) characterization results.
- 15 kV SiC MOSFET comparison with single die 15 kV SiC IGBT has been presented and their switching frequency limits for unidirectional DC-DC converter been evaluated. The 15 kV SiC MOSFET is favorable for operating at higher switching frequency compared to 15 kV SiC IGBT for same *dv/dt* conditions.
- 15 kV SiC MOSFET comparison with 15 kV/40 A SiC IGBT (with two parallel dies) has been presented and their switching frequency limits for a bi-directional DC-DC converter have been evaluated.
- Efficiency comparison of 15 kV SiC MOSFET and 15 kV SiC IGBT in DC-DC boost converter (both unidirectional and bi-directional configuration) has been presented.
- The experimental characterized data showed that for switching frequency < 4 kHz, the equivalent 15 kV SiC IGBT (single die per module) has a lower total loss compared to equivalent 15 kV SiC MOSFET(two dies per module) for duty ratio of 0.5, at 10 kV dc bus and at same *dv/dt* values. Similarly, for switching frequency < 6.5 kHz, the equivalent 15 kV SiC IGBT(single die per module) has a lower total loss compared to equivalent 15 kV

SiC MOSFET(two dies per module) for the duty ratio of 0.8, at 10 kV dc bus and at same *dv/dt* values.

- For DC bus voltage of 8 kV, the 15 kV SiC MOSFET (two parallel dies per module) has a lower total loss and higher efficiency than the 15 kV SiC IGBT (two parallel dies per module) for any current, switching frequency and at same gate resistance values.

Chapter 4 Comparison of series connected 1.7 kV SiC MOSFETs and HV SiC modules (10 kV SiC MOSFET, 15 kV SiC MOSFET, 15 kV SiC IGBT)

4.1 Introduction

One stream of the industry is working towards HV modules with the high current capability to enable medium voltage applications. Whereas, with proven robustness and reliability of low voltage (LV) SiC technology and availability of commercial LV SiC devices in the recent years, another stream of the industry is looking into the series connection of LV SiC MOSFETs for medium voltage, high power applications. Therefore, it is interesting to know the performance of state of the art HV SiC modules (10 kV -15 kV) with series connected LV SiC devices (1.2 kV to 1.7 kV). The LV and HV SiC modules used for comparison are shown in Fig. 4-1 to Fig. 4-5.

So far, it has been discussed (Chapter 2 and Chapter 3) about the series connection of 1.7 kV SiC MOSFET devices and 15 kV SiC devices (MOSFET and IGBT). However, the 10 kV SiC MOSFET device (Gen-I to Gen-III) characterization and loss data have not been discussed to compare with series connected 1.7 kV SiC MOSFET devices. Therefore, this chapter first briefly discuss the characterization 10 kV SiC MOSFET (Gen-I, Gen -II and Gen-III) and then presents the comparison of all HV SiC devices (10 kV SiC MOSFET, 15 kV SiC MOSFET, 15 kV SiC IGBT) with that of series connected 1.7 kV SiC MOSFET devices.

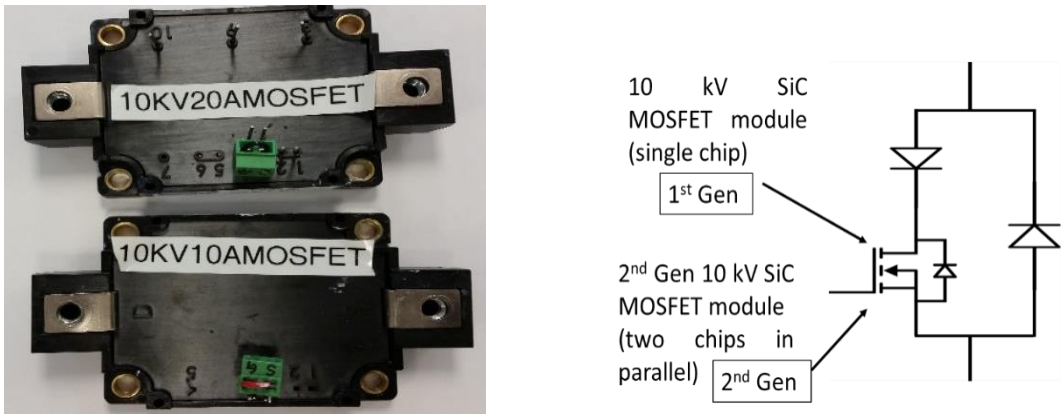


Fig. 4-1: SiC MOSFET - 10 kV/10 A(1st Gen), 10 kV/20 A (2nd Gen)

Fig. 4-2: 10 kV/10 A (3rd Gen) module packages, and their chip layout

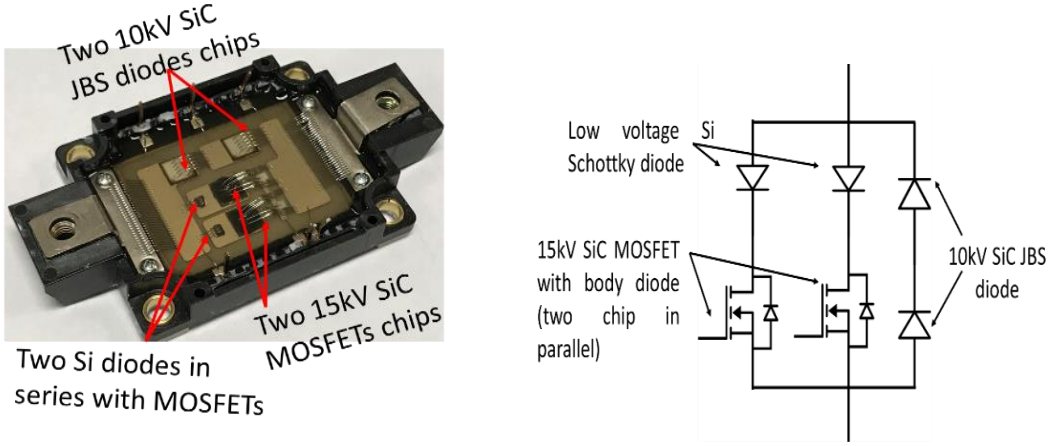


Fig. 4-3: 15 kV/20 A SiC MOSFET module package and its chip layout

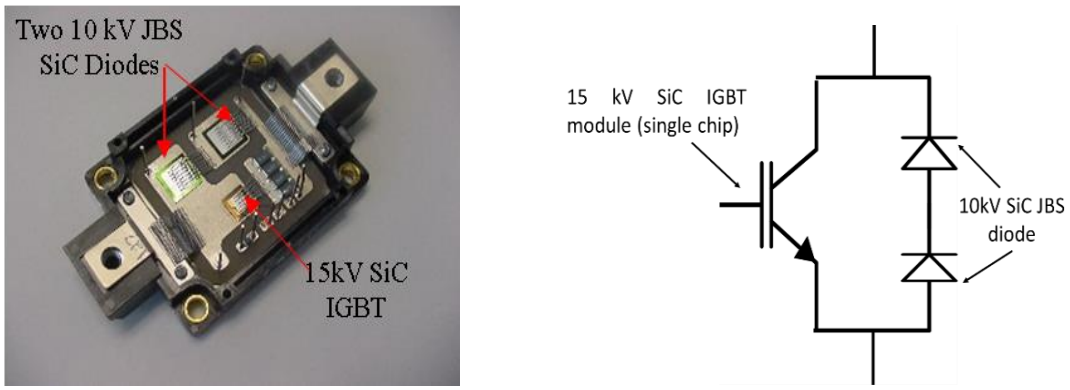


Fig. 4-4: 15 kV/20 A SiC IGBT(5 µm buffer layer) module package and its chip layout

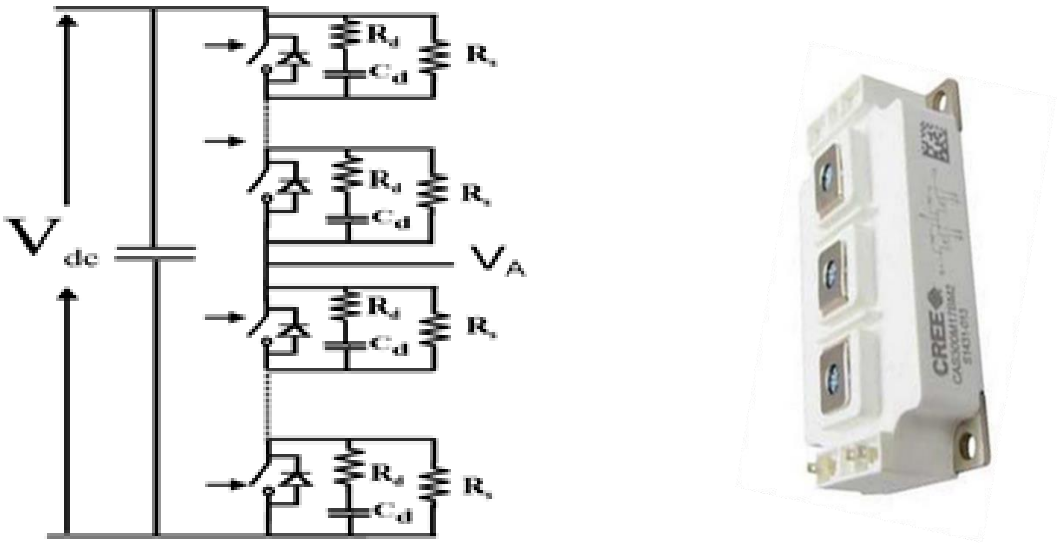


Fig. 4-5: HV SiC Switch using series connected 1.7 kV SiC MOSFET modules

4.2 10 kV SiC MOSFET switching and conduction losses

The typical value of R_{dson} of 1st Gen 10 kV/10 A SiC MOSFET is 0.41 Ω at 25°C [36]. The R_{dson} of 2nd Gen 10 kV/20 A SiC MOSFET (two chips per module) is 0.18 Ω at 25°C [6][8]. Therefore, its per chip R_{dson} will be 0.36 Ω at 25°C. Recently Wolf Speed has developed the third generation (3rd Gen) of 10 kV SiC MOSFET with improved internal body diode performance and eliminated external JBS diodes and series Si diode (as in Fig. 4-2). The per chip R_{dson} will be 0.345 Ω at 25°C [9]. The R_{dson} values of the HV SiC MOSFET devices at 150°C are nearly 2.5 to 3 times at 25°C. Table 4-1 shows the summary of the On-state resistance of 10 kV SiC MOSFET from 1st Gen to 3rd Gen.

Table 4-1: 10 kV SiC MOSFET On-state resistance (R_{dson})

10 kV/10 A SiC MOSFET	R_{dson} at 25°C	R_{dson} at 150°C
1st Gen per chip	0.41 Ω, at 10 A	1.1 Ω, at 10 A
2nd Gen per chip	0.36 Ω, at 10 A	0.9 Ω, at 10 A
3rd Gen per chip	0.35 Ω, at 10 A	0.875 Ω, at 10 A

Switching losses of 10 kV/10 A and 10 kV/20 A devices (with Powerex packing) have been characterized at R_{gon}=R_{goff}=14.5 Ω [8]. Therefore, switching characterization of 3rd Gen 10 kV/10 A SiC MOSFET has also been done at same gate resistance. Fig. 4-6 to Fig. 4-7 show the turn-on and turn-off switching transition of 15 kV SiC MOSFET at 5 kV, 10 A and at a gate resistance of 14.7 Ω junction temperature (T_j) of 25°C. Where V_{gs_L}: Low side gate to source voltage; V_{ds_L}: Low side

voltage across device; I_{ds_L}: Current through low side device; The turn-on and turn-off *dv/dt* values are 32 kV/µs and 58 kV/µs respectively. However, for the gate resistance of 2.2 **Ω**, the turn-on and turn-off *dv/dt* values are nearly 94 kV/µs and 61 kV/µs respectively been seen during characterization and reduction in switching losses.

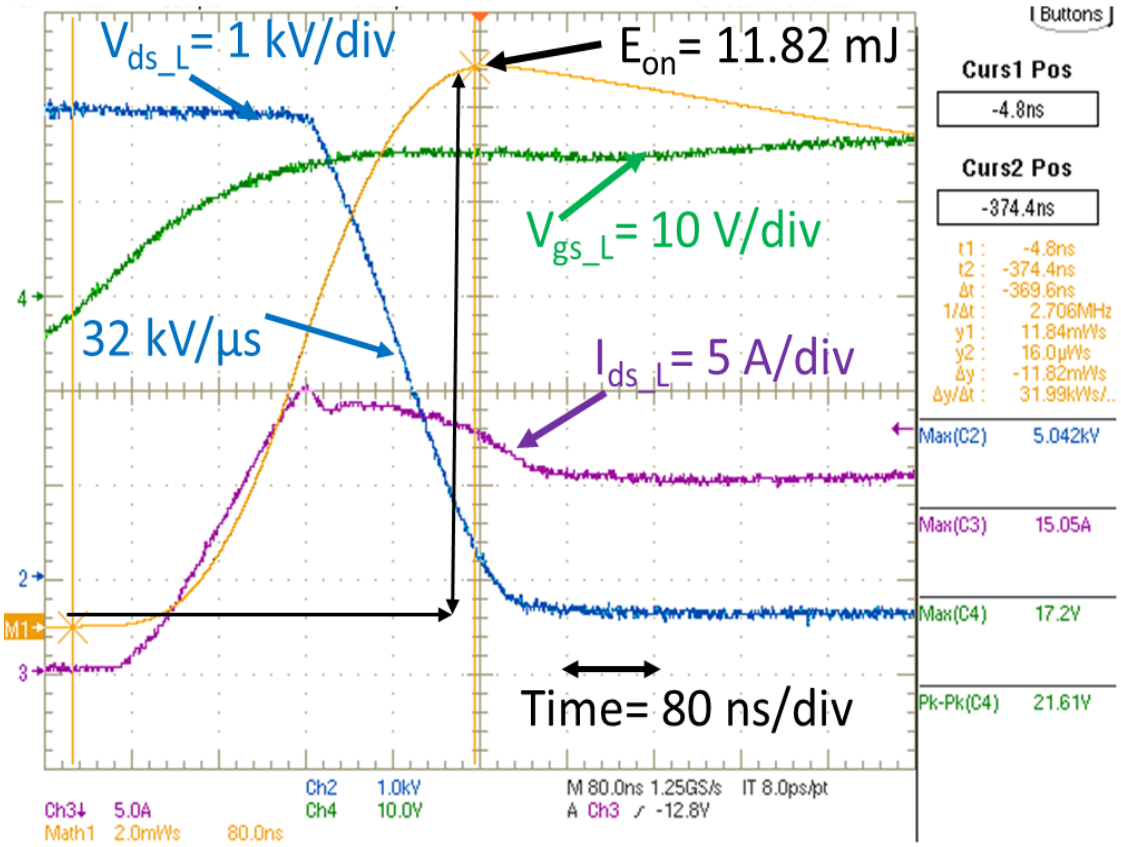


Fig. 4-6: Turn-on loss (11.82 mJ) at 5 kV 10 A at T_j:25^{0}C, R_{gon}:14.7 Ω

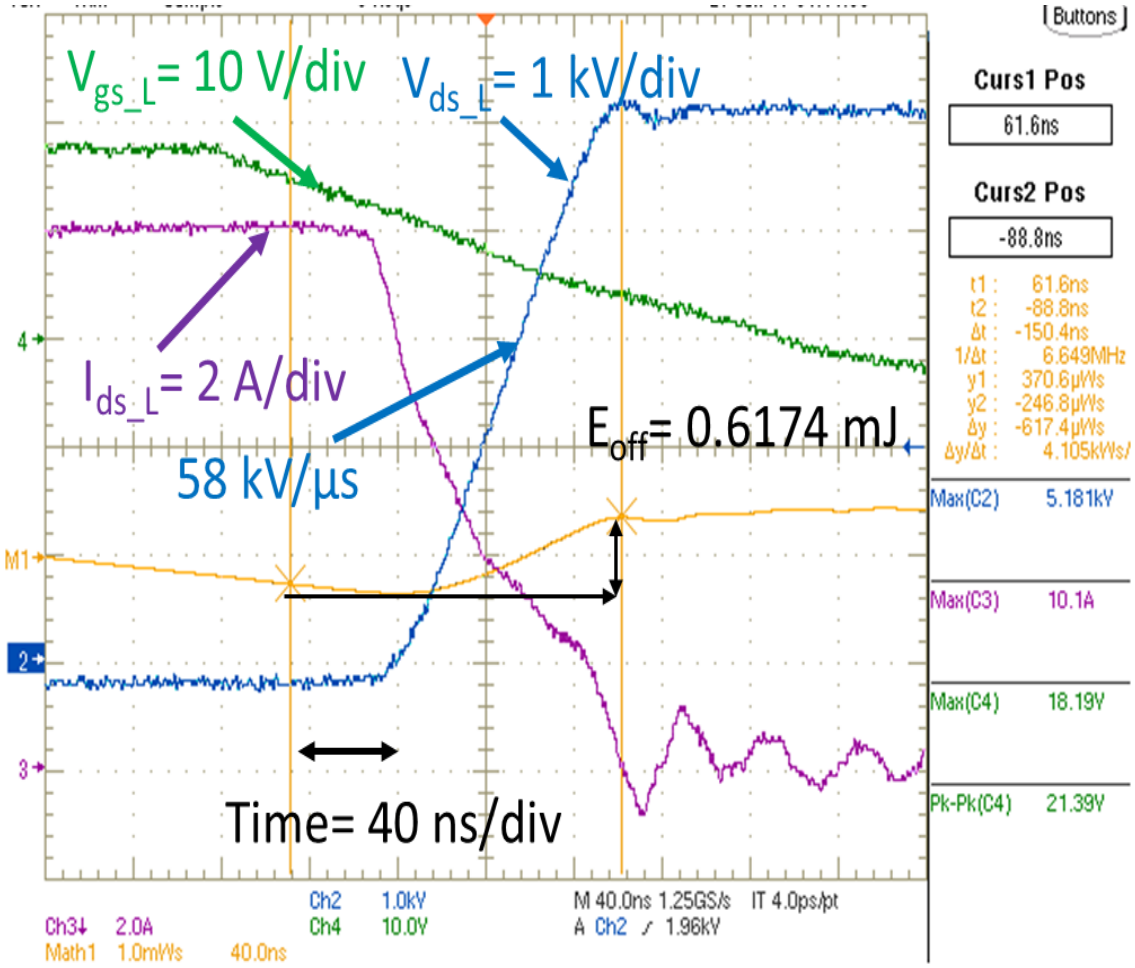
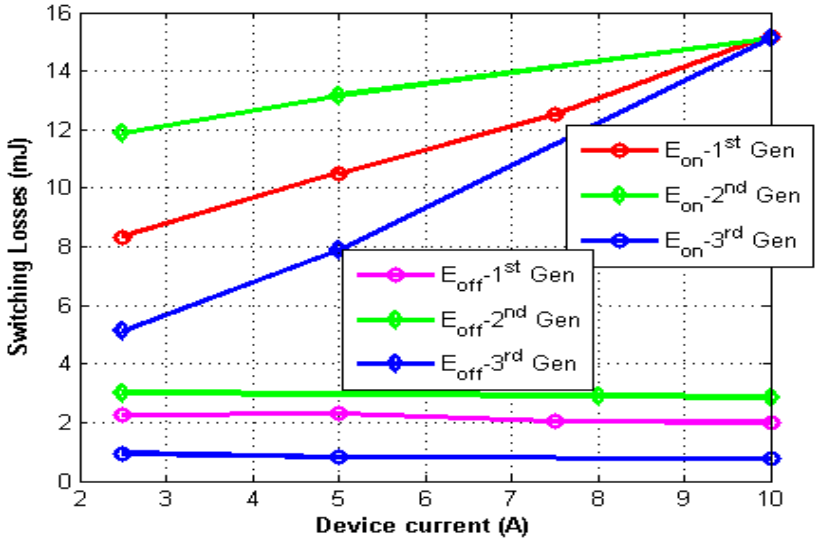
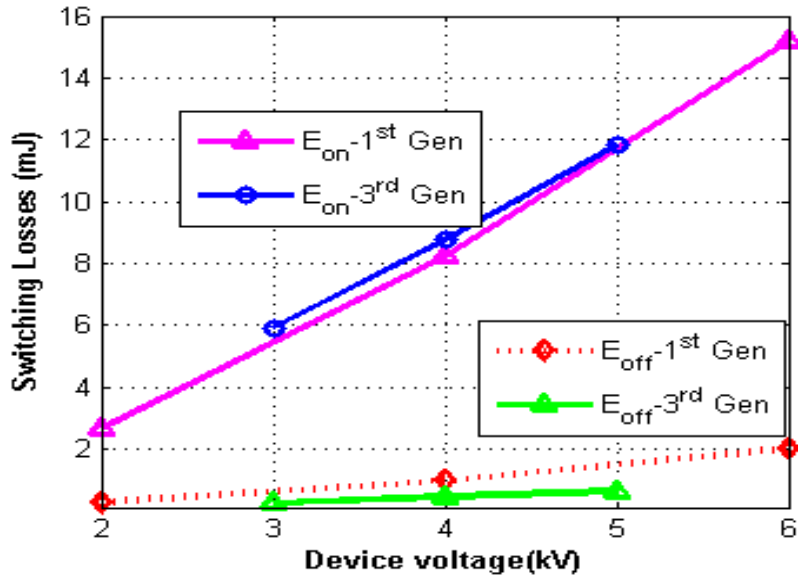


Fig. 4-7: Turn-off loss (0.6174 mJ) at 5 kV 10 A at T_j:25^{0}C, R_{gon}:14.7 Ω

Fig. 4-8(a) shows the comparison of switching loss of 1st, 2nd and 3rd Gen with different switching currents and at 6 kV switching voltage. It illustrates that the total switching loss (E_{sw} =E_{on}+E_{off}) of 3rd Gen is less compared to 1st and 2nd Gen SiC MOSFETs for different switching currents. Fig. 4-8(b) shows that total switching loss of 3rd Gen SiC MOSFET is less compared to 1st Gen SiC MOSFET for different switching voltages and at 10 A switching current. The effect of an increase in junction temperature on total switching loss is negligible from Gen-I, Gen-II experiments [8]. Therefore, the switching losses of 10 kV SiC MOSFET at 25^{0}C can used for converter power loss analysis for the junction temperature of 125^{0}C - 150^{0}C.



(a)



(b)

Fig. 4-8: (a) Turn-on (E_{on}), Turn-off (E_{off}) losses of 1st Gen to 3rd Gen 10 kV SiC MOSFET devices at 6 kV switching voltage with different switching currents; (b) Turn-on (E_{on}), Turn-off (E_{off}) losses of 1st Gen and 3rd Gen 10 kV SiC MOSFET devices at 10 A switching current with different switching voltages

4.3 Comparison of series connection of 1.7 kV SiC MOSFET devices and HV SiC modules

The typical safe operating voltage of 10 kV SiC MOSFET module is around 5 kV to 6 kV, and similarly, for 15 kV SiC MOSFET/IGBT modules, it is around 10 kV. The endurance test of these

HV SiC modules has been demonstrated in a DC-DC boost converter in section 3.5 and references [8][38] at similar operating voltages. Therefore, the series connected 1.7 kV SiC MOSFET devices are compared to the similar operating voltage conditions. But the 1.7 kV SiC MOSFET can operate at higher current (150 to 200 A) compared to HV SiC modules. Therefore, to make these HV SiC modules for 150 A switching operation, it has been assumed that the fifteen number of HV modules (10 kV/10 A or 10 kV/20 A or 15 kV/20 A) connected in parallel or fifteen number of chips are connected in parallel in a module. To support the feasibility of paralleling of HV SiC dies or modules for high current, Wolf Speed Inc. reported the feasibility of HV 10 kV/240 A SiC MOSFET module with parallel chips (3rd Gen) in a single module [9]. The summary of loss data of HV SiC modules (Fig. 4-1 to Fig. 4-5) to be used for scaling of 150 A operation has been shown in Table 4-2.

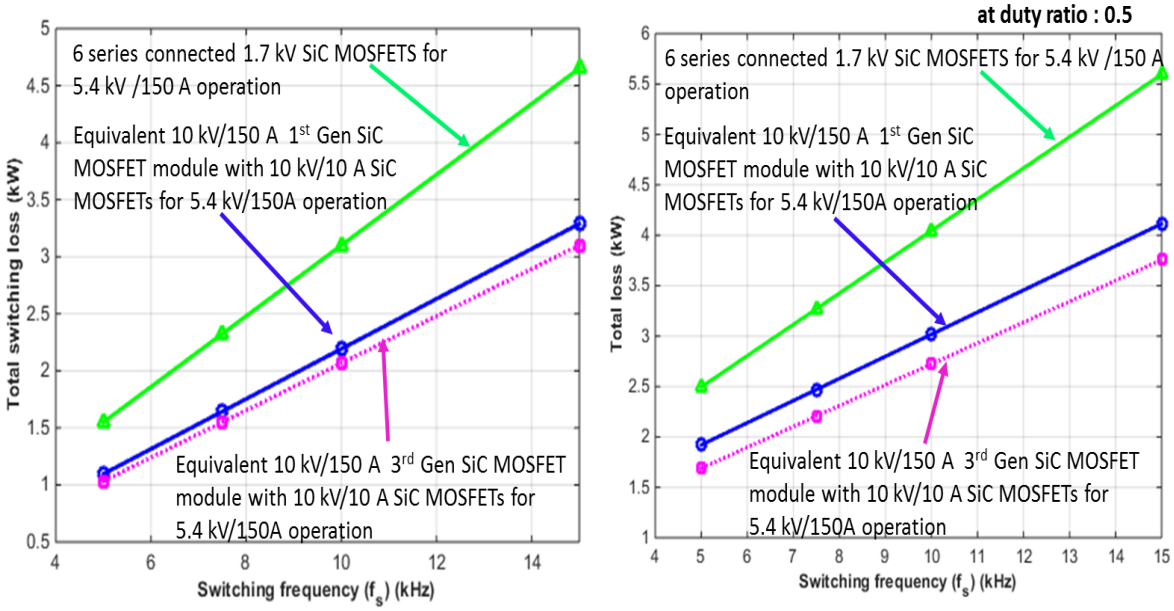
Table 4-2: Switching loss, conduction loss and dv/dt per HV SiC module

Module type	Switching voltage, current	Turn-off *dv/dt* (kV/µs)	Turn-on *dv/dt* (kV/µs)	E_{off} per module (mJ)	E_{on} per module (mJ)	$E_T = (E_{on}+E_{off})$ per module (mJ)	V_f or R_{dson} at T_j=150 ^{0}C	Conduction loss
10kV/10A SiC MOSFET (1st Gen)	5.4kV, 10A	42	20	1.654	12.96	**14.62**	1.1 Ω at 10A	**110 W at 10A**
10kV/20A SiC MOSFET (2nd Gen)	5.4kV, 10A	42	20	2.53	13.59	**16.13**	0.45 Ω at 10A	**45 W at 10A**
10kV/10A SiC MOSFET (3rd Gen)	5.4kV, 10A	58	32	0.678	13.1	**13.78**	0.875 Ω at 10A	**87.5 W at 10A**
15kV/20A SiC MOSFET	10 kV, 10A	32	45	5	26.47	**31.5**	1.6 Ω at 10A	**160 W at 10A**
15 V/20A SiC IGBT	10kV, 10A	32	45	22	25.5	**47.5**	5.2 V	**52 W at 10A**

The thermal resistance of the 15 kV SiC modules (R^{th}_{j-c}) is shown in section 3.7, Table 3-10. 10 kV SiC modules have the same packaging as of that 15 kV SiC modules, so same thermal resistance has been assumed for 10 kV SiC MOSFET modules from chip to base plate case. Therefore, the effective thermal resistance of the equivalent 10 kV/150 A SiC module with fifteen parallel devices of 10 kV/10 A (1st Gen) will be 0.03266^{0}C/W. Similarly, the thermal resistance of the equivalent 10 kV/150 A SiC module with fifteen parallel devices of 10 kV/20 A (2nd Gen) and 15 kV/150 A module with fifteen parallel devices of 15 kV/20 A will be 0.01667^{0}C/W (because each device has two parallel chips). The thermal resistance of 1.7 kV SiC MOSFET device is 0.071^{0}C/W data sheet

[31]. Therefore, the effective thermal resistance with six and eleven series-connected 1.7 kV SiC MOSFET devices will be 0.01167^0C/W and 0.00636^0C/W respectively for making equivalent 10 kV and 15 kV HV SiC series switch.

Fig. 4-9(a)-(b) and Table 4-3 show the comparison of switching losses and total losses for the equivalent 10 kV/150A SiC MOSFET modules and 10 kV SiC switch using series connected 1.7 kV SiC MOSFET devices for 5.4 kV/ 150 A operation. The equivalent 3rd Gen 10 kV/150 A SiC MOSFET module has lower total loss compared 10 kV /150 A SiC switch using the series connection of 1.7 kV SiC MOSFET devices. Total loss of 10 kV/150 A SiC MOSFET switch using series connected 1.7 kV SiC MOSFET(33 nF,1.56 Ω) is nearly 22% more compared to equivalent 3rd Gen 10 kV/150 A SiC MOSFET module at 5 kHz, and it will be much higher at higher switching frequencies due to increased snubber resistor losses with frequency. However, the total loss using equivalent 10 kV/150 A SiC module (2nd Gen) is 9.775 % less compared to that of 10 kV HV switch using series connected 1.7 kV SiC MOSFET this is due to significant reduction of 'R_{dson}' or conduction losses at the cost of "**2x** increased" number of parallel devices or chips compared to equivalent 1st and 3rd Gen SiC MOSFET modules.



(a) (b)

Fig. 4-9: (a) Shows the comparison of switching losses; (b) shows the comparison of Total losses; for 1st, 3rd Gen equivalent 10 kV/150 A SiC MOSFET modules and 10 kV HV SiC switch using series connected 1.7 kV SiC MOSFET devices for 5.4 kV, 150 A operation

Table 4-3 shows the junction temperature rise from base plate case is much less in HV SiC switch using series connected 1.7 kV SiC MOSFET devices compared 10 kV/150 A equivalent HV SiC MOSFET modules(using Gen-I and Gen-III chips). It will increase the switching frequency limits for

series connected 1.7 kV SiC MOSFET devices compared to 10 kV/150 A equivalent HV SiC MOSFET modules made using Gen-I and Gen-III chips. However, the junction temperature rise from base plate case is not significantly more for 10 kV/150 A equivalent HV SiC MOSFET module using Gen –II chips compared to that of HV SiC switch using series connected 1.7 kV SiC MOSFET devices. It is due to decreased total losses and reduced effective thermal resistance of module at the cost of "**2x** increased" no of parallel devices or chips compared to 1st and 3rd generation 10 kV SiC MOSFET modules.

Table 4-3: Junction to case temperature rise comparison of parallel connected 1st to 3rd Gen 10 kV SiC MOSFET devices and five series connected 1.7 kV devices (HV SiC switch),) at 5.4 kV 150 A switching, with a duty ratio of 0.5 for conduction losses

Device	No of devices for series or parallel for 5.4 kV,150A operation	Effective Thermal resistance of module $\left(R_{j\text{-}c}^{th}\right)$	Total losses for 5 kHz	Total losses for 10 kHz	Junction temperature from Case	Junction temperature from Case
10kV/10A SiC MOSFET (1st Gen)	15 devices parallel	0.03266 ^{0}C/W	2746.275	3842.55	89.71^{0}C	125.49^{0}C
10kV/20A SiC MOSFET (2nd Gen)	15 devices parallel or (30 chips in parallel)	0.01634 ^{0}C/W	1884.398	3093.795	30.77^{0}C	50.52^{0}C
10kV/10A SiC MOSFET (3rd Gen)	15 devices parallel	0.03266 ^{0}C/W	2345.895	3379.29	76.63^{0}C	110.36^{0}C
1.7kV SiC MOSFET (33nF, 1.56 Ω)	6 devices in series	0.01167 ^{0}C/W	3440.46	4990.92	34.24^{0}C	46.42^{0}C

Fig. 4-10 and Fig. 4-11 show the comparison of switching losses and total losses for equivalent 15 kV/150 A HV SiC modules and 15 kV/150 A HV switch using series connected 1.7 kV SiC MOSFET devices. The equivalent 15 kV/150 A SiC IGBT module has higher switching losses compared equivalent 15 kV/150 A SiC MOSFET module and the series connection of 1.7 kV SiC MOSFET devices. However, the conduction losses of equivalent 15 kV/150 A SiC IGBT is much lower than other two SiC MOSFET cases as shown in Table 4-4. Therefore, up to certain switching frequency called breakeven switching frequency, the SiC IGBT module will have lower total loss compared to other two MOSFET cases. For the frequency greater than breakeven switching frequency, the switching losses of SiC IGBT will be more dominant compared to increased

conduction losses of MOSFET, which leads to 15 kV SiC MOSFET more efficient compared to 15 kV SiC IGBT at higher switching frequencies. The Fig. 4-11 shows that for the frequency greater than the breakeven switching frequency, the equivalent 15 kV/ 150 A SiC MOSFET module has a lower total loss compared to other two cases (equivalent 15 kV/150 A SiC IGBT and series connection of 1.7 kV SiC MOSFETs).

Table 4-4: Comparison of conduction losses of eleven series connected 1.7 kV devices (HV switch), and fifteen parallel devices of 15 kV/20 A (HV module) for '10 kV 150 A' operation

Device	No of devices for series or parallel for 10 kV, 150 A operation	Conduction losses
15 kV/20 A SiC MOSFET	15 devices/chips in parallel	2.4 kW
1.7 kV SiC MOSFET with 33 nF, 1.56 Ω	11 device in Series	3.465 kW
15 kV/20A SiC IGBT (5µm)	15 devices/chips in parallel	0.78 kW

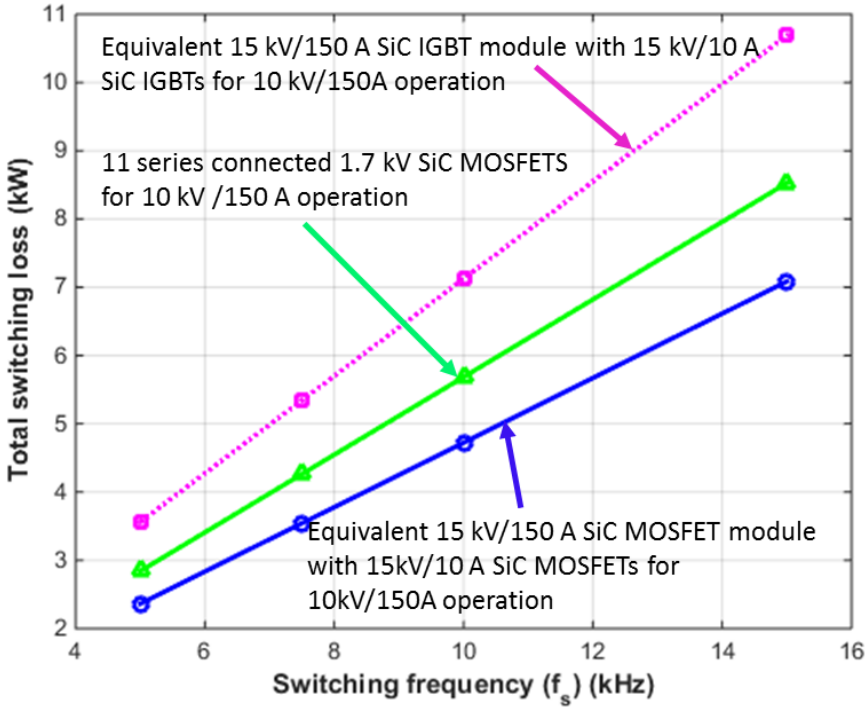
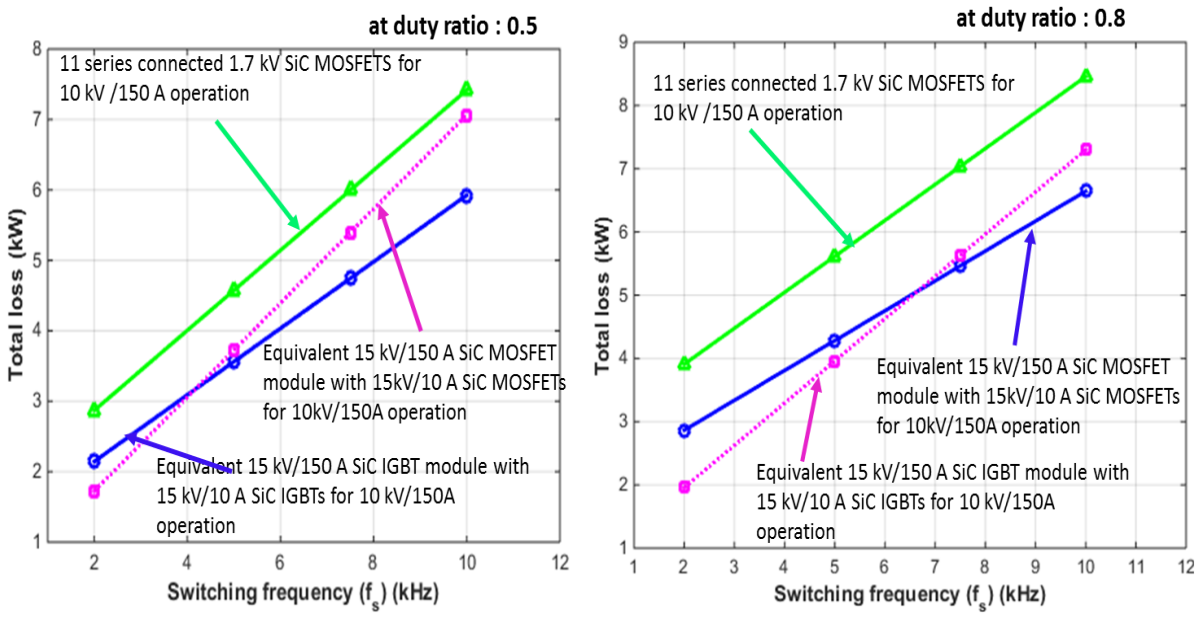


Fig. 4-10: Shows the comparison of switching losses for the equivalent 15 kV/150 A HV modules and 15 kV/150 A HV switch using series connected 1.7 kV SiC MOSFET devices for 10 kV, 150 A operation



(a) (b)

Fig. 4-11: Shows the comparison of Total losses for equivalent 15 kV/150 A HV modules and 15 kV/ 150 A HV switch using series connected 1.7 kV SiC MOSFET devices for 10 kV, 150 A operation

Similar to 10 kV SiC MOSFET module, the 15 kV SiC modules also experience higher junction temperature rise from base plate case due to the higher thermal resistance of modules of compared to 1.7kV SiC MOSFET modules. The module packaging technology is limiting the thermal resistance of HV modules and hence its value is much higher compared to HV SiC switch with series connected 1.7kV SiC MOSFETs.

Therefore, better HV module packaging technologies need to be investigated to further enhance the performance of HV modules compared to that of low voltage series connection. However, until the low-cost HV modules become commercially available, the series connection of low voltage SiC MOSFET will definitely give high efficiency and high switching frequencies up to 10 kHz and become an alternative to replace the existing HV Si-IGBT for MV/HV converter applications.

The comparison of HV SiC switch using series connected 1.7 kV SiC MOSFET devices and HV Si-IGBT has been evaluated as shown in Table 4-5. The Si 3.3 kV Si-IGBT (ABB manufacture part no : 5SNG 0250P330305) and 6.5 kV Si-IGBT(ABB manufacture part no : 5SNA 0400J650100)[35] have been taken for evaluation. The safe operating voltage of 3.3 kV Si-IGBT is 1800 V and that of 6.5 kV Si-IGBT is 3600 V. Two series connected 1.7 kV SiC MOSFET devices are required for to compare with 3.3 kV Si-IGBT and four series connected 1.7 kV SiC MOSFETs are required to compare with

6.5 kV Si-IGBT. Table 4-5 shows that the two series connected devices (1.7 kV SiC MOSFET) has 2 to 3 times lower total losses at 5 kHz and 10 kHz compared to single 3.3 kV Si-IGBT. Similarly, the four series-connected devices (1.7 kV SiC MOSFET) has 5 to 6 times lower total losses at 5 kHz and 10 kHz compared to single 6.5 kV Si-IGBT.

Table 4-5: Total losses comparison of 3.3 kV-6.5 kV SiC switch using series connected of 1.7 kV SiC MOSFETs and Si-IGBT (3.3 kV-6.5 kV)

Device	No of devices	Device switching losses per kHz	Total Snubber Resistor loss per kHz	Total switching losses per kHz	Total conduction losses	Total losses for 5kHz	Total losses for 10kHz
	At 1800V, 100A Switching						
3.3 kV Si IGBT	**1 device**	309 W	0.00 W	309 W	225 W	1.77 kW	3.32 kW
1.7 kV SiC MOSFET (Snubber: 33 nF,2.35 Ω)	**2 devices in series**	52.14 W	45.41 W	97.55 W	280 W	0.77 kW	1.26 kW
	At 3600V, 100A Switching						
6.5 kV Si IGBT	**1 device**	1369W	0.00 W	1369 W	310 W	7.16 kW	14.00 kW
1.7 kV SiC MOSFET (Snubber: 33 nF,2.35 Ω)	**4 devices in series**	104.28 W	90.82 W	195.10 W	560 W	1.54 kW	2.51 kW

4.4 Conclusions

- Total losses of series connected 1.7 kV SiC MOSFETs case is compared with equivalent 10 kV-15 kV /150 A SiC modules. The junction to case temperature rise is more in the equivalent 10-15 kV SiC /150 A modules for a given switching frequency compared to the series connection of 1.7 kV SiC MOSFET devices. The packaging thermal resistance is limiting the performance of HV SiC modules.
- Total losses of the equivalent 10 kV /150 A SiC MOSFET modules (using 1st - 3rd gen dies) are less compared to that of series connected 1.7kV SiC MOSFET devices for 5.4 kV/150 A.
- For switching frequency less than 6.5 kHz and at a duty ratio of 0.8, the equivalent 15 kV/150 A SiC IGBT is more efficient compared to the equivalent 15 kV/150 A SiC MOSFET module and series connected 1.7 kV SiC MOSFETs. For switching frequency greater than 6.5 kHz, the equivalent 15 kV/150 A SiC MOSFET modules are more efficient for 10 kV/150 A operations compared to other two cases. However, the 10-15 kV SiC modules are not

commercially available due to cost or other reasons at present. Therefore the series connection of LV SiC MOSFETs will provide an alternate method for enabling MV converter for high-speed drives or grid connected converters applications.

- Also, the series connected 1.7 kV SiC MOSFET devices is 3- 6 times lower total loss compared to 3.3 kV Si-IGBT and 6.5 kV Si-IGBT.

Chapter 5 Soft switching and Series Connection Characterization of HV SiC Devices (10-15 kV) to Enable Medium Voltage High Power DC-DC Transformer for MV/HV Applications

5.1 Introduction

The objective of this chapter is to enable a medium voltage high power DC-DC soft switching converters Fig. 1-6, Fig. 1-7 (a)-(c) and similar converters. These converters use either single HV SiC device per arm or series connected HV SiC device per arm.

In DC-DC transformer applications using DC-DC dual active bridge converter (DAB), the turn-on losses of devices are nearly zero due to inherent zero voltage switching (ZVS) during turn-on. Therefore, the total losses are due to turn-off switching losses and conduction losses.

5.1.1 DC-DC transformer or DAB using 10-15 kV SIC MOSFET devices

If 10-15 kV SiC MOSFET is used in the DAB converter, the measured turn-off losses of 3rd generation 10 kV SiC MOSFET at 5 kV, 10 A are nearly negligible with 3 W -3.7 W (4.57 W/cm^2 - 5.64 W/cm^2) for 5 to 6 kHz switching frequency unless the switching frequency is very high. The measured dissipation(3 W-3.7 W) is due to (i) power dissipation in the channel and energy stored in the output capacitance. The energy dissipated in the channel is called true turn-off losses and makes the junction temperature to rise. Since the channel will be cut-off quickly for these HV SiC MOSFETs during turn-off and most of the load current is shifted to output capacitance. Therefore true turn-off power dissipated in the channel is negligible out of total measured turn-off losses [49] and the stored energy in the output capacitance will not be dissipated in the device during next turn on, but it will be fed back to DC source in a DAB converter just before next ZVS turn-on. Therefore, the turn-off losses are nearly negligible even if the ZVS turn-off is not achieved using 10 kV-15 kV SiC MOSFET devices in the DC-DC converter applications like DAB unless the switching frequency is very high. Hence, the majority of the total losses are due to conductions losses, and junction temperature of these devices are mostly limited by the on-state resistance (R_{dson}) and RMS current through the device, but the R_{dson} of the SiC MOSFET increases nearly 2.5-3 times for T_j = 25^{0}C to 150^{0}C.

One of the challenges using these devices in DAB is to limit the parasitic coupling capacitive currents due to high *dv/dt* reflected in the pole voltages. These coupling currents deteriorates the gate driver functionality and hence operating converter using these devices will be challenging. Therefore, to reduce the turn-off '*dv/dt*' in a DC-DC transformer application using 10-15 kV SiC MOSFET devices

(single device per arm), an external snubber capacitor is used. The external snubber capacitor gives zero voltage switching during turn-off and the turn-off '*dv/dt*' will be reduced along with a further reduction in turn-off losses. With proper selection of external snubber, a series connection of HV SiC MOSFET devices can also be achieved to enable DC-DC transformer using series connected HV SiC devices per arm.

5.1.2 DC-DC transformer or DAB using 15 kV SIC IGBT devices

If 15 kV SiC IGBT is used in DAB converter, unlike the 10 kV -15 kV SiC MOSFET, the turn-off losses are not negligible in 15 kV SiC IGBT. Therefore the total losses in 15 kV SiC IGBT in soft switching converter are turn-off losses and conductions losses. During turn-off, the measured turn-off losses will contain energy losses due to a significant portion of minority charge in the drift layer compared to energy stored in the device output capacitance [61]. Unlike SiC MOSFET, the On-state voltage does not increase significantly from $T_j=25^0$C to 150^0C.

Similar to HV SiC MOSFET devices, operating DAB converter using 15 kV SiC IGBT is also challenging. It generates high '*dv/dt*' because of punch through design with the field stop buffer layer. The switching voltage across the device has two slopes depending on whether the voltage across the device is below punch through or above punch-through region. From the power electronics converter designer perspective, the high '*dv/dt*' generated at the switching pole is detrimental to external-interfacing inductive circuits such as medium frequency transformer, inductor, and gate driver isolation transformer with parasitic winding capacitance (C) . This is due to large common mode currents (C.*dv/dt*) drawn by parasitic coupling capacitors. The switching '*dv/dt*' and its influence in high voltage high power converter has been reported in [45]. The switching '*dv/dt*' of the 15 kV IGBT with different gate resistances and the need for complex active gate driver is reported in [62]. The three-level DC-DC soft switching converter operation in the Solid-state-transformer (SST) application using 15 kV SiC IGBT with 2 μm field-stop buffer layer was extremely challenging due to high '*dv/dt*' generated by these devices in the punch-through region. Therefore the demonstration of three-level DC-DC converter for Solid State Transformer (SST) application has been done using 15 kV 5 μm SiC IGBT which has relatively lower '*dv/dt*' and turn-off loss compared to 2 μm 15 kV SiC IGBT [42]. However, these demonstrations did not utilize full rating of the device (10 kV) and results were reported till 5 kV only. DC-DC soft switching converter inherently gives zero voltage turn-on. Therefore the punch through turn-on '*dv/dt'* stress can be eliminated. However, the turn-off '*dv/dt*' of the order of 30 to 45 kV/μs is still present in this converter. This high '*dv/dt*' is preventing the operation of the converter at higher dc bus voltage or rated device voltage (10 kV -11 kV).

A typical power electronics MV converter (such as Solid State Transformer) with parasitic coupling capacitances using 15 kV SiC IGBT is shown in Fig. 5-1 [63]. The 35 kVA, 22 kV/800 V, 10 kHz, the medium voltage medium frequency transformer has been used in this application. The transformer impedance has been characterized using Agilent 4294A impedance analyzer [64]. The loading of transformer at 7 kV/500 V, 10 kW has been demonstrated in [63], but this converter used custom-designed inductors (L_{f1}, to $L_{f3,}$ with very low parasitic capacitance) on primary side of transformer and common mode chokes to reduce the coupling currents drawn by parasitic transformer capacitance due to high '*dv/dt*' generated by SiC IGBT devices. The coupling current drawn by the parasitic capacitance of medium frequency transformer and its comparison with respect to rated primary side current of the transformer are summarized in Table 5-1. The typical AC pole voltage '*dv/dt*' seen by the transformer in the Dual active bridge (DAB) shown in Fig. 5-1 is 30-45 kV/µs. If the custom inductors or transformers are not present, then the parasitic capacitive coupling current will be much higher.

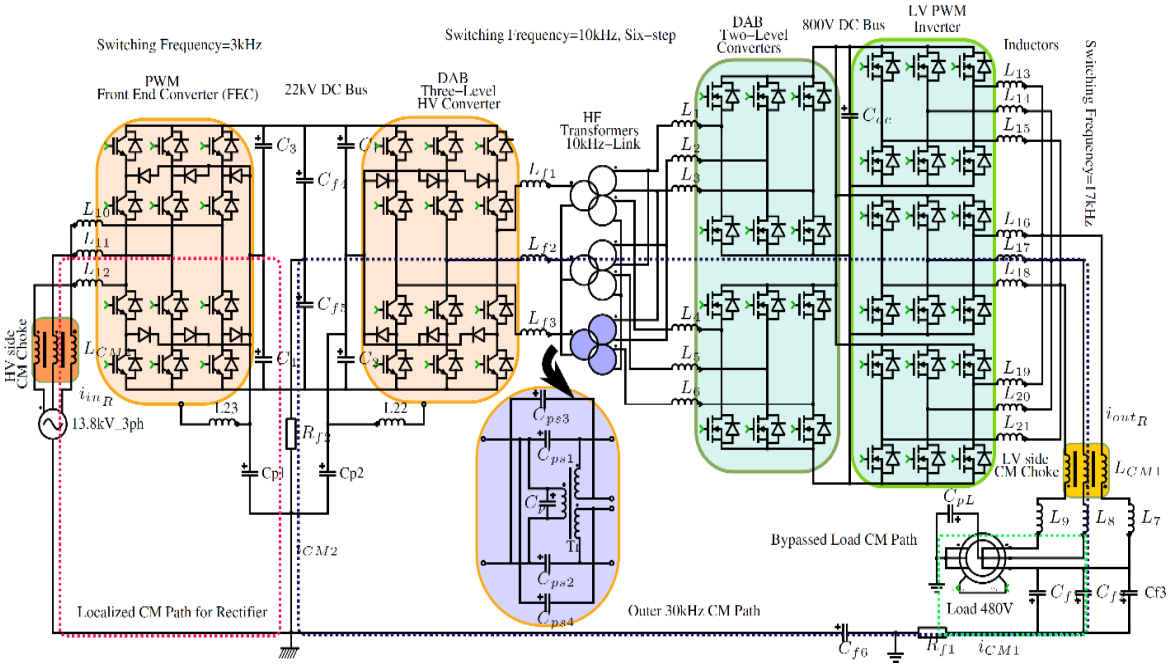


Fig. 5-1: DC-DC soft switching converter (DAB) with medium frequency Transformer and its parasitic capacitances in SST application[63]

Therefore, to reduce the turn-off losses and '*dv/dt*' in a DC-DC transformer application using single 15 kV SiC IGBT device per arm, an external snubber capacitor is used. The external snubber capacitor gives zero voltage switching during turn-off and hence losses in the device reduce along with reduced '*dv/dt*'. With proper selection of external snubber, a series connection of HV SiC

devices can also be achieved to enable DC-DC transformer using series connected HV SiC devices per arm.

In summary, this chapter presents the (i) detailed turn-off characterization of 15 kV SiC IGBT (2 µm and 5 µm buffer layer) devices with and without snubber capacitor; (ii) Series connection characterization of 15 kV SiC IGBT devices, 15 kV SiC MOSFET devices and 10 kV SiC MOSFET devices;

Table 5-1: 35 kVA, 22 kV/ 800 V 10 kHz transformer parasitic current at AC pole voltage *dv/dt* of 30 kV/µs

Transformer parasitic capacitance[5-6]	**Coupling current due to parasitic capacitance(C.dv/dt)**	**Rated current on primary side of DAB at 22 kV/800V, 35 kW**	**% of coupling current w.r.t rated current**
Self-capacitance (C_p) 50pF	1.5 A peak	6 A peak	25%
Mutual capacitance (C_{ps1}) 300pF	9 A peak	6 A peak	150%

This chapter is organized as follows:

Section 5.2 presents turn-off characterization of (i) 15 kV SiC IGBT (single die, 2µm buffer layer) with and without snubber capacitor; (ii) 15 kV SiC IGBT (two parallel dies, 5µm buffer layer) with and without snubber capacitor.

Section 5.3 presents the DC-AC half-bridge soft switching converter demonstration using 15kV/40A SiC IGBT devices (two parallel dies per module, 5µm buffer layer).

Section 5.4.1 presents series connection of 15 kV/20 A SiC IGBT modules (single die per module, 2 µm buffer layer).

Section 5.4.2 presents series connection of 15 kV/40 A SiC IGBT modules (two parallel dies per module, 5 µm buffer layer).

Section 5.4.3 presents series connection of 15 kV/15 A SiC MOSFET modules (two parallel dies per module)

Section 5.4.4 presents series connection of 10 kV/10 A SiC MOSFET modules (single die per module)

5.2 Turn-off Characterization of 15 kV SiC IGBT with and without snubber capacitor

The preliminary results on soft switching behavior of the 12 kV SiC N-IGBTs have been reported up to 7 kV/10 A [61] using DPT shown in Fig. 5-2 This is asymmetrical phase-leg configuration. The characterization results obtained using this setup cannot be used for the performance evaluation of DC-DC converter where the devices are in a phase-leg configuration (as in Fig. 5-3(a)). The asymmetrical DPT setup gives most pessimistic turn-off loss savings (lower than actual) in the device than phase-leg configuration DPT setup.

In this section, using symmetrical phase-leg inductive clamped circuit, the turn-off switching characteristics of the 15 kV SiC IGBT devices (with and without snubber capacitor) have been experimentally evaluated at higher switching voltages (up to 9 kV-10 kV), and at higher switching currents (up to 20 A) for both 2 μm and 5 μm field-stop buffer layer thicknesses.

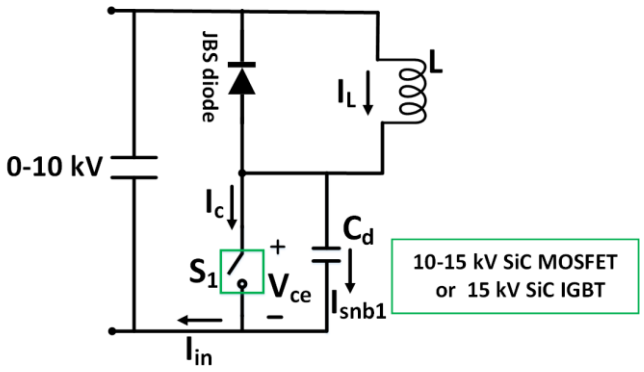


Fig. 5-2: Asymmetrical phase-leg Inductive clamped circuit

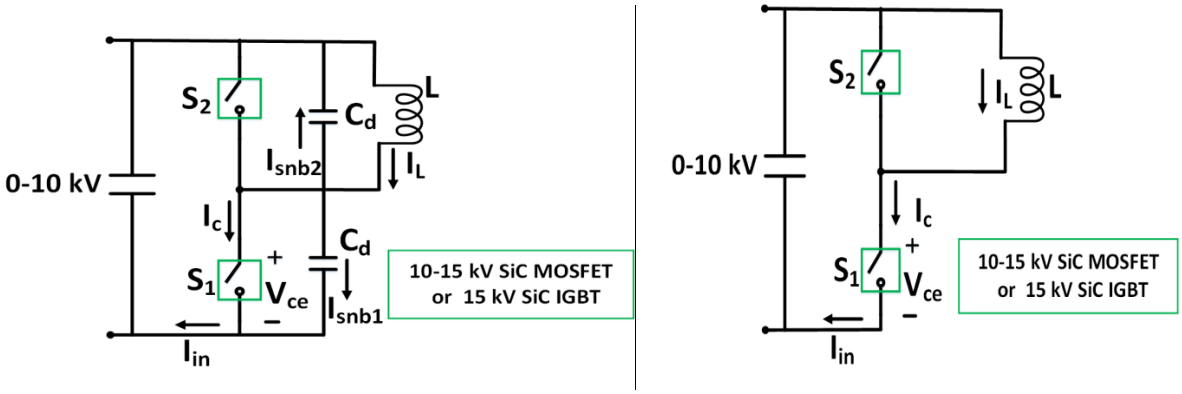


Fig. 5-3: The symmetrical phase-leg Inductive clamped circuit (a) circuit used for turn-off soft switching of an HV SiC device; (b) The circuit used for turn-off hard switching of an HV SiC device

5.2.1 15 kV/20 A SiC IGBT (2 µm field-stop buffer layer)

The turn-off characteristics of 2µm 15 kV/20 A SiC IGBT with and without snubber capacitor are presented in this section. The 15 kV/20 A SiC IGBT (2 µm field-stop buffer layer) turn-off characteristics are obtained through double pulse experiments on the test circuits shown in Fig. 5-3(a) and Fig. 5-3(b). Fig. 5-4 and Fig. 5-5 and show the turn-off losses without external snubber at 25°C and 150°C respectively, where Ch2: voltage across the 15 kV IGBT device (V_{ce}), Ch3: Device current (I_c), Ch1: Inductor current (I_L), Ch4: Gate voltage (V_{ge}). Math1: Energy losses.

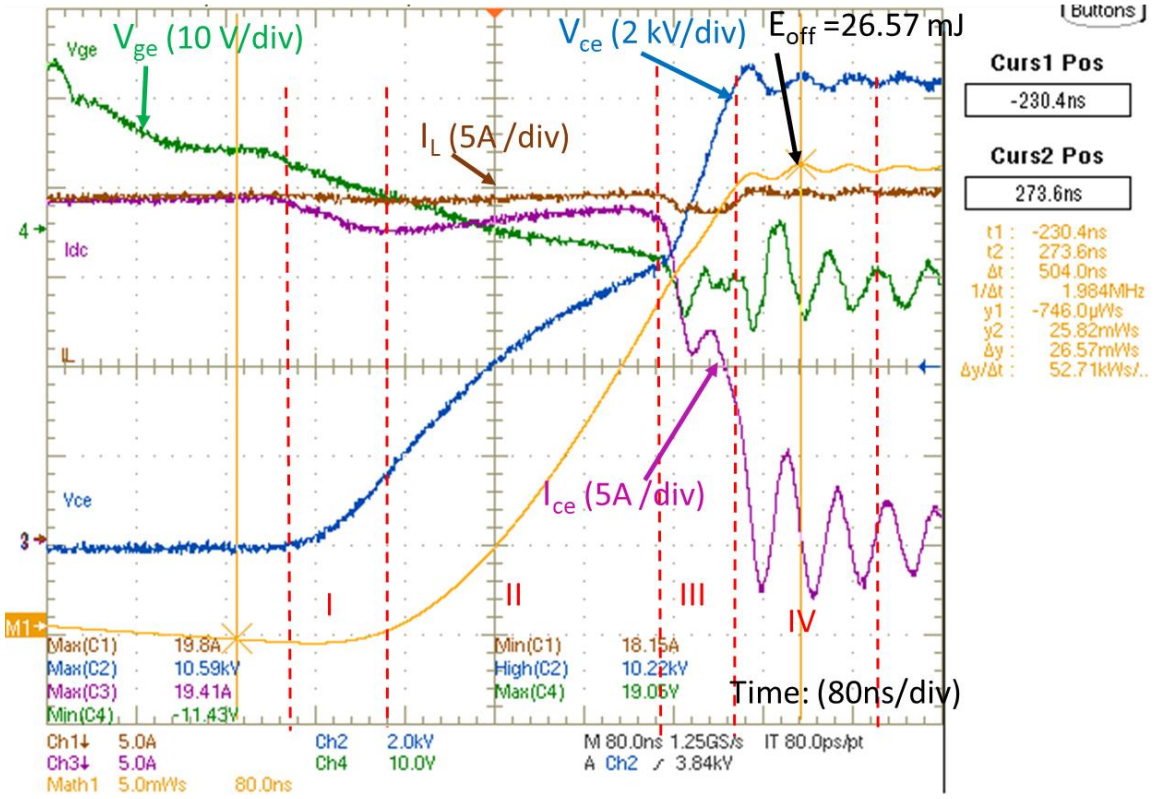


Fig. 5-4: Turn-off losses of 15 kV, 2 µm buffer layer SiC IGBT at 25°C without an external snubber capacitor at 10 kV, 20 A. (E_{off} =26.57 mJ)

As explained in [61], the turn-off current has four different stages during the transition: a dip at the beginning of the transition resulting from transferring load inductor current into the IGBT capacitance (and capacitance of the free-wheeling diode); the current nearly constant until the punch-through voltage (until all the stored charge from drift layer is removed); a slow drop in current from punch-through voltage until the voltage reaches dc-bus voltage of 10 kV; a sudden drop in current once the voltage reached dc-bus value of 10 kV; finally, the current tail resulting from

recombination of the stored charge. At 150^{0}C, the stored charge in the drift layer is more compared to 25^{0}C. Therefore, the duration for the voltage (V_{ce}) to reach punch-through voltage is significantly longer (**2 times longer**) and the resultant turn-off losses also significantly more (**nearly 3 times more**) compared to 25^{0}C.

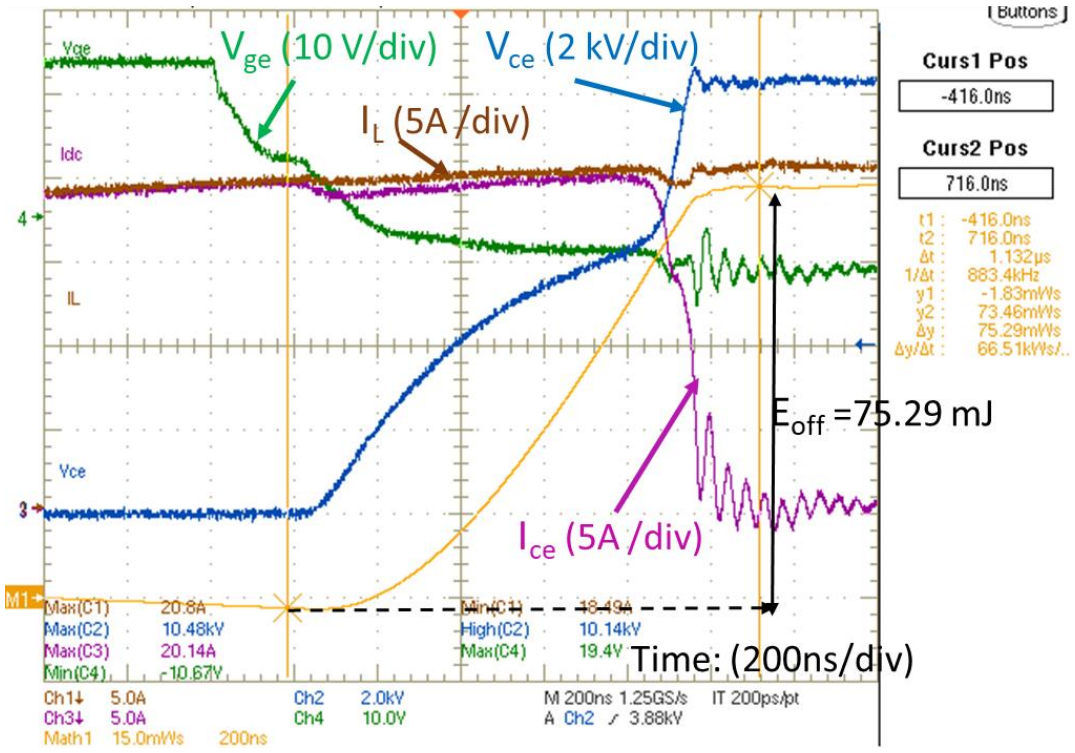


Fig. 5-5: Turn-off losses of 15 kV, 2 µm buffer layer SiC IGBT at 150^{o}C without an external snubber capacitor at 10 kV, 10 A. (E_{off} =75.29 mJ)

Fig. 5-6 shows the turn-off losses with external snubber (2.2nF) at 150^{o}C respectively, where Ch2: voltage across the 15kV SiC IGBT device (V_{ce}), Math3: Device current (I_{ce}), Ch1: Current through external snubber capacitor (I_{snb1}), Ch3: Total current from DC source (I_{in}) Ch4: Gate voltage (V_{ge}). Math1: Energy losses. Fig. 5-5 and Fig. 5-6 show that there is a **nearly 20 mJ (26.43%)** reduction in turn-off losses with snubber compared to without snubber.

Fig. 5-7 and Fig. 5-8 show the turn-off *dv/dt* without and with external snubber at 150^{o}C. The turn-off *dv/dt* with external snubber is reduced significantly (nearly **12 times)** as compared to without snubber. Table 5-2 and Table 5-3 show the comparison of reduction in *dv/dt* and turn-off losses with snubber compared to without snubber at 150^{o}C for different switching voltages and currents.

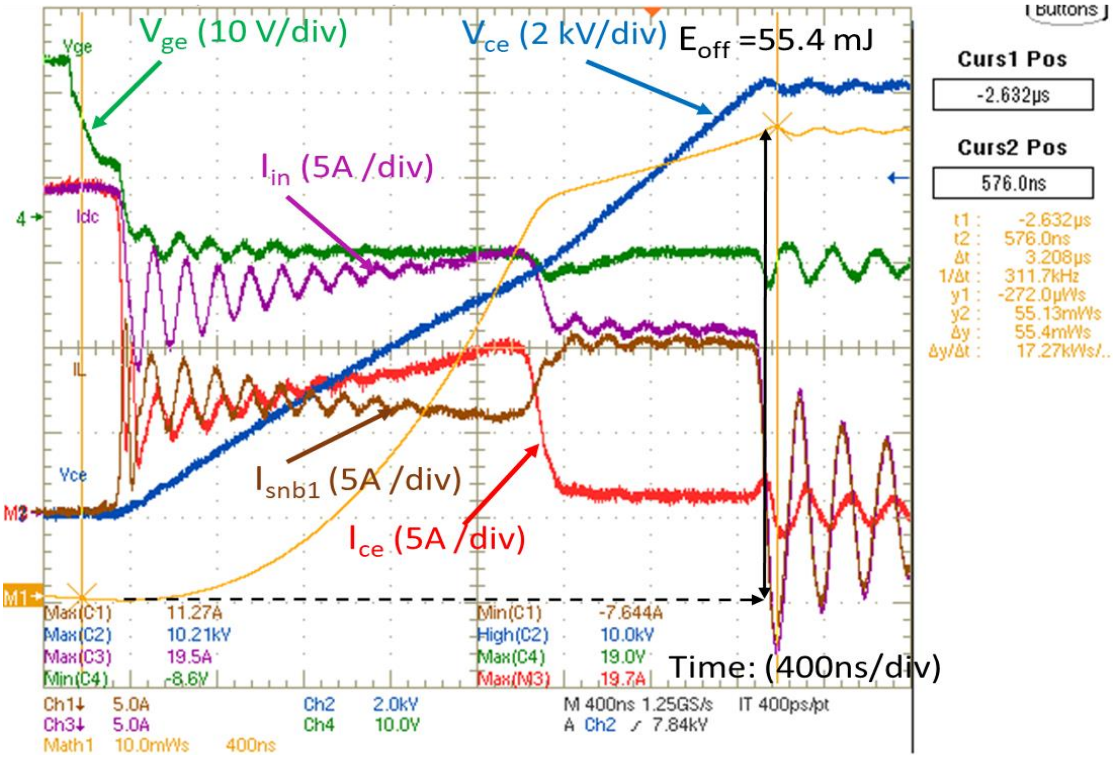


Fig. 5-6: The Turn-off transitions of 15 kV, 2 µm buffer layer SiC IGBT at 150°C with an external snubber capacitor (2.2nF). (E_{off} =55.4 mJ)

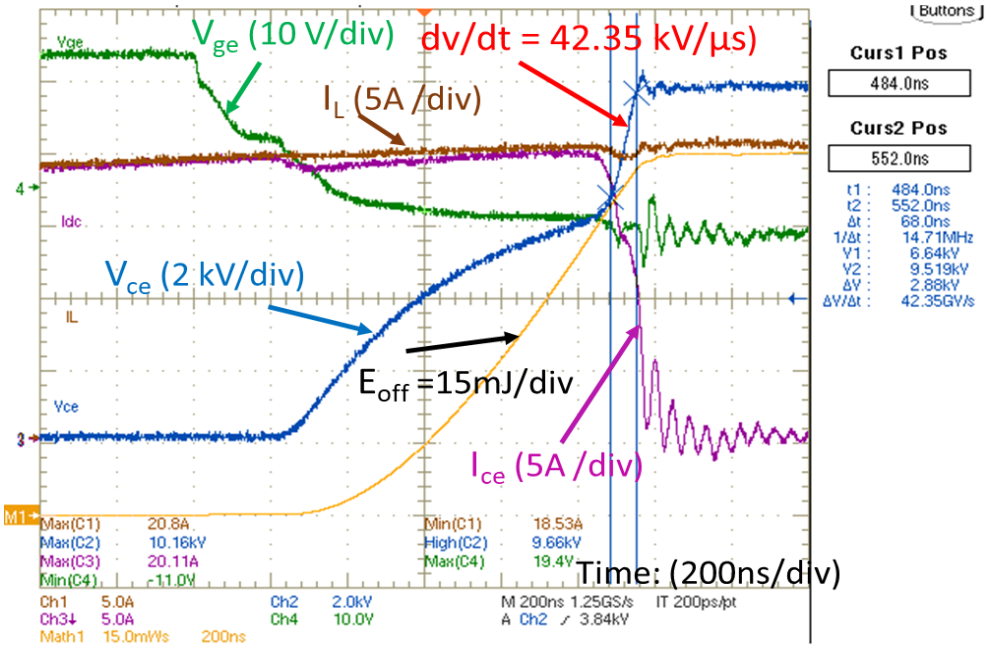


Fig. 5-7: Turn-off *dv/dt*=42.35 kV/µs of 15 kV, 2 µm buffer layer SiC IGBT at 150°C without an external snubber capacitor

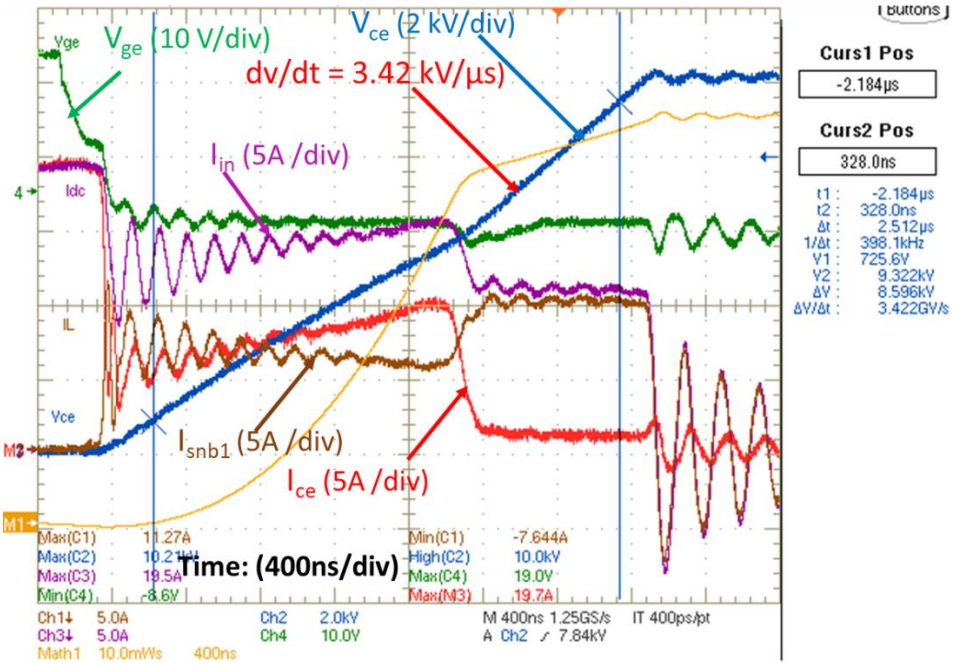


Fig. 5-8: Turn-off *dv/dt*=3.42kV/µs of 15 kV, 2 µm buffer layer SiC IGBT at 150°C with an external snubber capacitor (2.2 nF)

Table 5-2: Comparison of turn-off losses and *dv/dt* for 2 µm 15 kV SiC IGBT with and without snubber at T_j=150°C, 10 kV dc bus

	Turn-off losses (E_{off})			Turn-off '*dv/dt*'		
	Without snubber	**With 2.2 nF Snubber capacitor**	**With 1.1 nF Snubber capacitor**	**Without snubber**	**With 2.2 nF Snubber capacitor**	**With 1.1 nF Snubber capacitor**
10 kV, 5 A	28.78	25.37	27.01	17.14	1.51	2.33
10 kV, 10 A	47.79	35.59	39.87	30.71	2.14	4.77
10 kV,15 A	61.79	45.02	51.75	35.9	2.85	6.3
10 kV, 20 A	75.29	55.44	62.4	42.35	3.42	7.95

Table 5-3: Comparison of turn-off losses and *dv/dt* for 2 µm 15 kV SiC IGBT with and without snubber at T_j=150°C, 9 kV dc bus

	Turn-off losses (E_{off})			Turn-off '*dv/dt*'		
	Without snubber	**With 2.2 nF Snubber capacitor**	**With 1.1 nF Snubber capacitor**	**Without snubber**	**With 2.2 nF Snubber capacitor**	**With 1.1 nF Snubber capacitor**
9 kV, 5 A	28.25	25.38	26.77	15.57	1.42	2.98
9 kV, 10 A	45.67	32.58	36.9	27.34	2.075	4.38
9 kV,15 A	60.16	43.11	49.7	30	2.667	5.96
9 kV, 20 A	73.33	52.86	59.79	36.74	3.34	7.6

5.2.2 15 kV/40 A SiC IGBT (5 µm field-stop buffer layer)

The turn-off characteristics of 5 µm 15 kV/40 A SiC IGBT with and without snubber capacitor have been presented in this section. Fig. 5-9 and Fig. 5-10 show the turn-off losses and '*dv/dt*' without external snubber at 150°C. Fig. 5-11 and Fig. 5-12 show the turn-off losses and '*dv/dt*' with external snubber (2.2 nF) at 150°C.

Fig. 5-9 and Fig. 5-11 show that there is a **nearly 10 mJ (22.73%)** reduction in turn-off losses with snubber compared to without snubber. Similarly, Fig. 5-10 and Fig. 5-12 show that the turnoff '*dv/dt*' with external snubber is **reduced eleven times** compared to without snubber. Table 5-4 and Table 5-5 show the comparison of reduction in '*dv/dt*' and turn-off losses with and without snubber at 150°C for different switching voltages and currents.

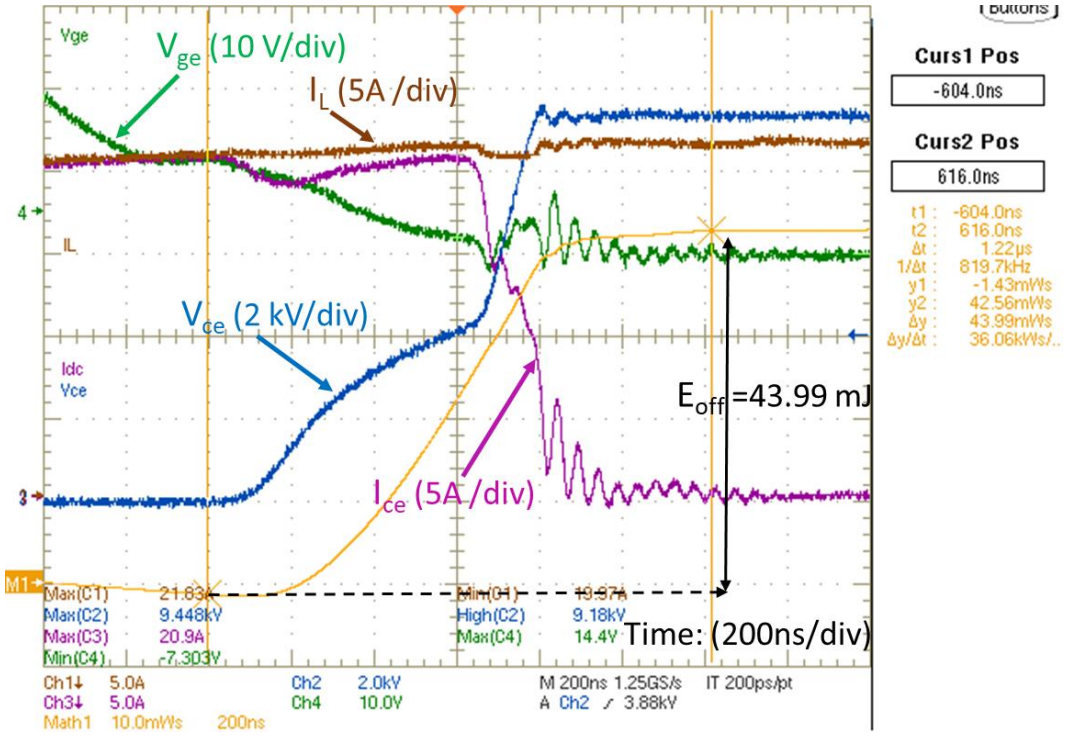


Fig. 5-9: Turn-off transitions of 15 kV, 5 µm buffer layer SiC IGBT at 150°C without an external snubber capacitor at 9 kV, 20 A. (E_{off} =43.99 mJ)

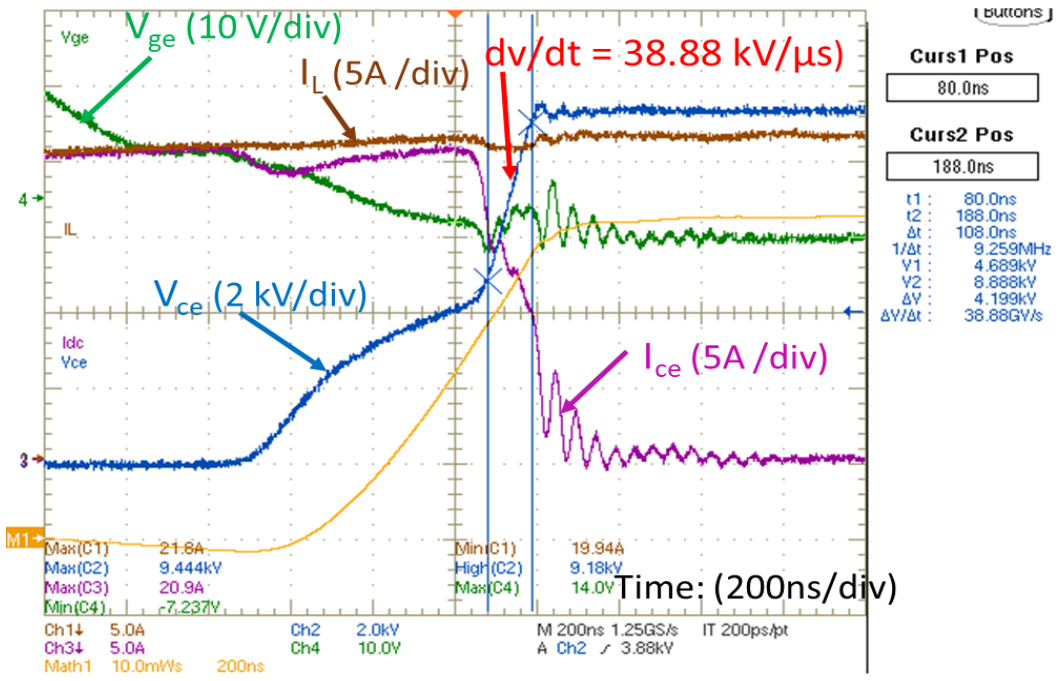


Fig. 5-10: Turn-off dv/dt=38.88 kV/µs of 15 kV, 5 µm buffer layer SiC IGBT at 150°C without an external snubber capacitor at 9 kV, 20 A

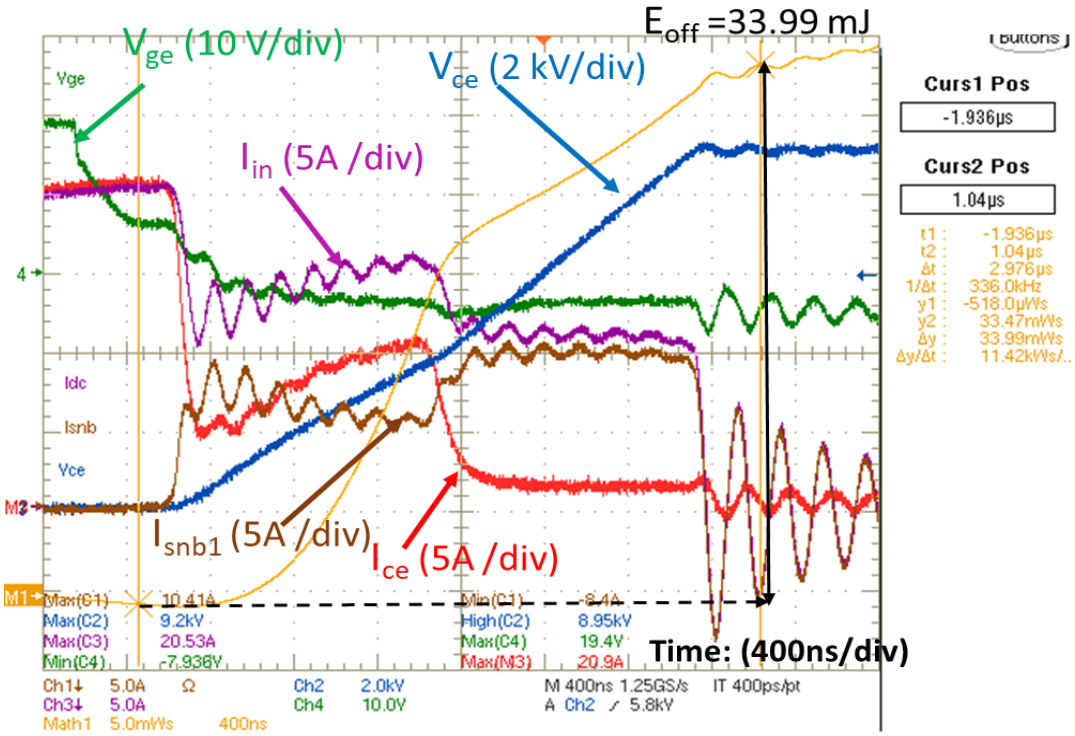


Fig. 5-11: Turn-off losses of 15 kV, 5 µm buffer layer SiC IGBT at 150°C with an external snubber capacitor (2.2nF) at 9 kV, 20 A. (E_{off} =33.99 mJ)

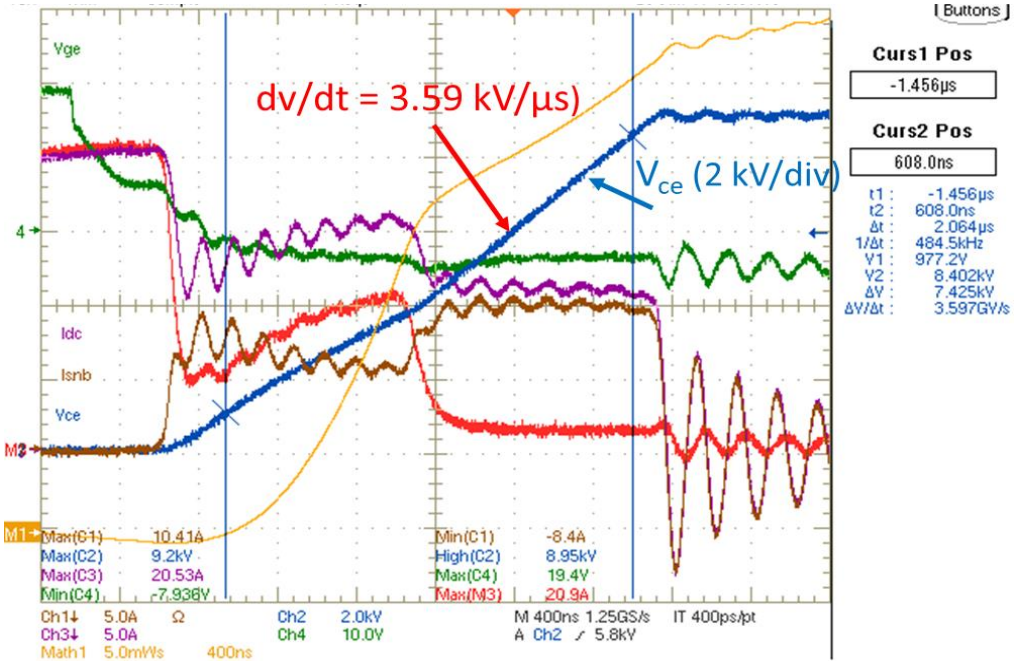


Fig. 5-12: Turn-off *dv/dt*=3.59 kV/µs of 15 kV, 5 µm buffer layer SiC IGBT at 150°C with an external snubber capacitor (2.2nF)

Table 5-4: Comparison of turn-off losses and *dv/dt* for 5 µm 15 kV IGBT with and without snubber at T_j=150°C , 9 kV dc bus

	Turn-off losses (E_{off})		Turn-off '*dv/dt*'	
	Without snubber	**With 2.2 nF**	**Without snubber**	**With 2.2 nF**
9 kV, 5 A	17.45	18.1	14.15	1.57
9 kV, 10 A	27.89	22.85	23.81	2.24
9 kV,15 A	36.17	28.73	31	2.91
9 kV, 20 A	43.99	33.99	38.8	3.597

Table 5-5: Comparison of turn-off losses and *dv/dt* for 5 µm 15 kV IGBT with and without snubber at T_j=150°C, 8 kV dc bus

	Turn-off losses (E_{off})			Turn-off '*dv/dt*'		
	Without snubber	**With 2.2 nF**	**With 0.5 nF**	**Without snubber**	**With 2.2 nF**	**With 0.5 nF**
8 kV, 5A	16.16	14.89	14.26	13.5	1.3	4.47
8 kV, 10A	24.95	20.32	21.53	21.43	2.16	7
8 kV,15 A	33.16	25.94	28.1	29.68	2.92	9.6
8 kV, 20 A	40.34	30.82	34.32	35.14	3.597	12.48

The turn-off losses are shown in Table 5-2 -Table 5-5 contains both minority carrier current and stored energy in the device output capacitance. The energy stored in the device output capacitance is fed back to the source in ZVS converter (such as DAB converter) and only minority carriers contribute to the true turn-off losses. Since the losses evaluated using the ZVS characterization have not been isolated from stored device capacitance energy (though energy stored in the output capacitance can be neglected compared to loss due to minority stored charge), hence the evaluation of IGBT module losses in a ZVS converter will do not yield true losses and results in most pessimistic converter efficiencies (lower than actual values).

5.3 DC-AC half bridge soft switching converter demonstration using 15 kV/40A SiC IGBT devices

This section presents the experimental demonstration of zero voltage switching of DC-AC half-bridge converter using 5 μm 15 kV/40 A IGBT module. The test circuit is shown in Fig. 5-13.

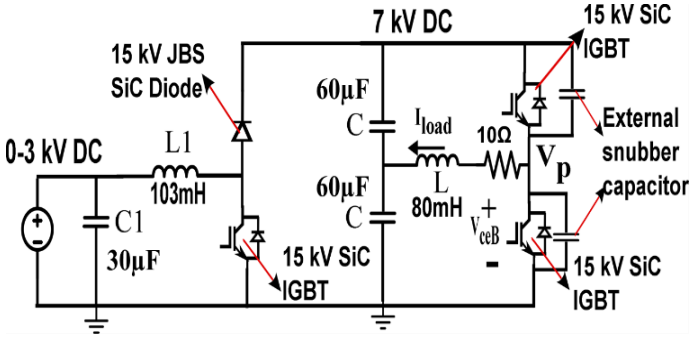


Fig. 5-13: The experimental circuit of dc-dc boost converter and dc- ac half bridge ZVS converter

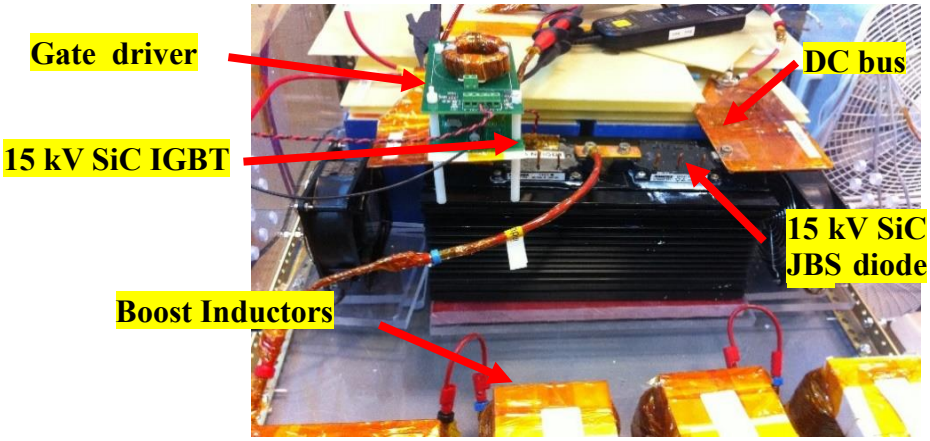


Fig. 5-14: The experimental circuit of DC-DC boost converter

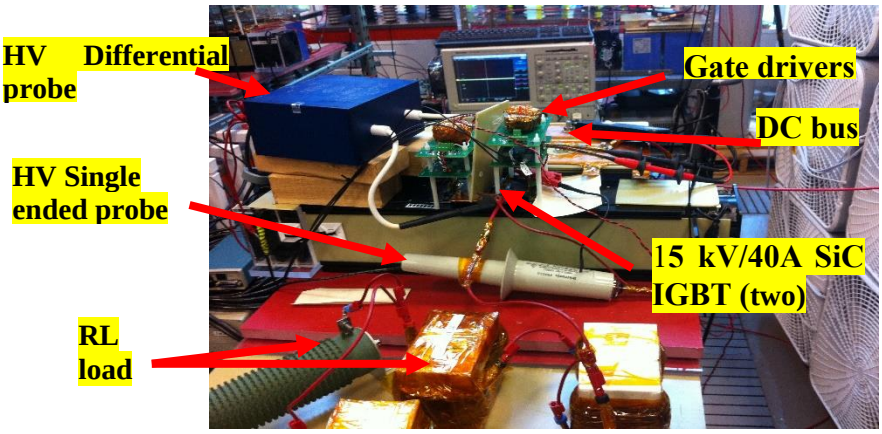


Fig. 5-15: The experimental circuit DC-AC half bridge ZVS converter

The experimental setups for boost converter that boost from 1.75 kV to 7 kV DC and half-bridge converter are shown respectively in Fig. 5-14 and Fig. 5-15. The true total losses of IGBT module can be measured by heat dissipated (heat sink temperature) in the IGBT modules in a half bridge based ZVS converter. The gate resistances R_{gon} of 33 Ω and R_{goff} of 7.5 Ω are used in the gate drivers for all the experiments

5.3.1 Total losses and *dv/dt* of 15 kV SiC IGBT (5 μm field-stop buffer layer) in Half-bridge dc-dc Soft switching converter and without external snubber

The 15 kV SiC IGBT device capacitance is used to achieve the partial ZVS turn-off without any external snubber. The inductive lagging current of the converter discharges the voltage across the incoming turn-on device and then freewheels through anti-parallel diodes during dead-time. This condition achieves the ZVS turn-on. The switching frequency of the half-bridge converter is 5 kHz. The Fig. 5-16 shows the steady state voltage across the bottom IGBT (VceB), Bottom IGBT gate voltage (VgeB), AC Pole voltage(Vp), and load current (Iload) at 7 kV DC bus. The converter is continuously run for 20 minutes. The heat sink temperature measured at the end of 20 minutes is 34.7^{o}C. The ambient temperature is 25.5^{o}C. The heat sink (392-180AB) thermal resistance with forced air-cooling are given in [65] with 1 module and 3 modules on the heat sink. The fan arrangement in the DC-AC experiment is the push-pull type, i.e. one fan at the inlet and one fan at the outlet. The airflow rate of each fan is 115 cfm. The effective airflow rate on the heat sink due to push-pull arrangement is approximately taken as 1.1 to 1.5 times the airflow due to each fan. This is because of difference in pressure drop from inlet to outlet, and there is 18 cm distance between the fan and the heat sink on both inlet and outlet side. From the datasheet, the thermal resistance of heat sink for the forced air convection at 126.5 to 172.5 cfm with 1 module on the heat sink is 0.118-0.1

^{o}C/W and with 3 modules is 0.091-0.08 ^{o}C/W. The half bridge ZVS experiment uses 2 modules so the effective heat thermal resistance range will be 0.1045-0.09 ^{o}C/W (i.e., an average of thermal resistance due to 1 module and 3 modules). The details of the heat sink are mentioned in [65].

The power dissipated in the 15 kV SiC IGBT module is calculated using (5-1); where, T_H= Heat sink temperature. T_A= Ambient temperature.

$$(P_d) = \frac{\Delta T}{R^{th}_{H-A}} = \frac{T_H - T_A}{R^{th}_{H-A}} \qquad (5\text{-}1)$$

Therefore, the total power dissipated in 15 kV SiC IGBT module corresponding to 0.1045-0.09 ^{o}C/W will be P_d=88.04 W to 102.22 W at 7 kV DC bus and Iload=8.2 A. The thermal resistance of 40 A module from junction to heat sink case $(R^{th}_{J\text{-}C})$ is 0.2058^{0}C/W as shown in section 3.7 and Table 3-10. The estimated junction temperature (T_j) using (5-2) for the power dissipation of 88.04 W to 102.22 W will be 52.82^{o}C to 55.73^{o}C.

$$T_j = T_A + P_d \times (R^{th}_{J\text{-}C} + R^{th}_{C\text{-}H} + R^{th}_{H\text{-}A}) \qquad (5\text{-}2)$$

Fig. 5-17 and Fig. 5-18 show the transition of AC Pole voltage (Vp), load current (Iload), the voltage across the bottom IGBT (VceB), Bottom IGBT gate voltage (VgeB), when top IGBT is turning off and bottom IGBT is turning off respectively. The maximum *dv/dt* across the IGBT device or AC pole voltage (in the punch-through region) is 14.5 kV/µs.

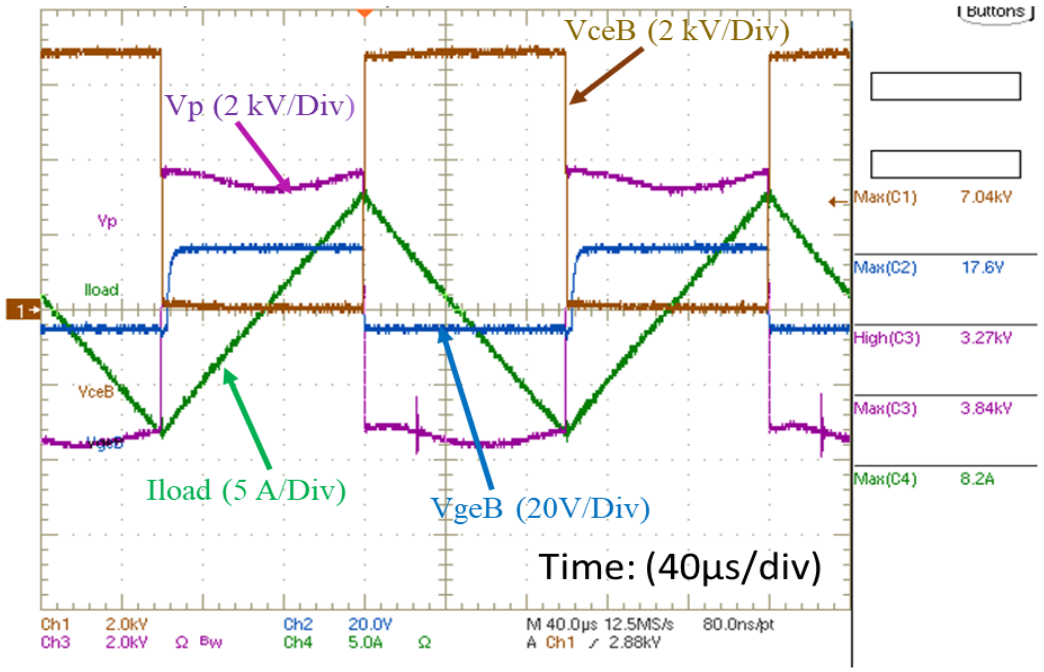


Fig. 5-16: At 7 kV, 8.2 A peak and 5 kHz half bridge ZVS test, the steady state AC Pole Voltage(Vp), load current(Iload), voltage across the bottom IGBT (VceB), Bottom gate IGBT voltage (VgeB)

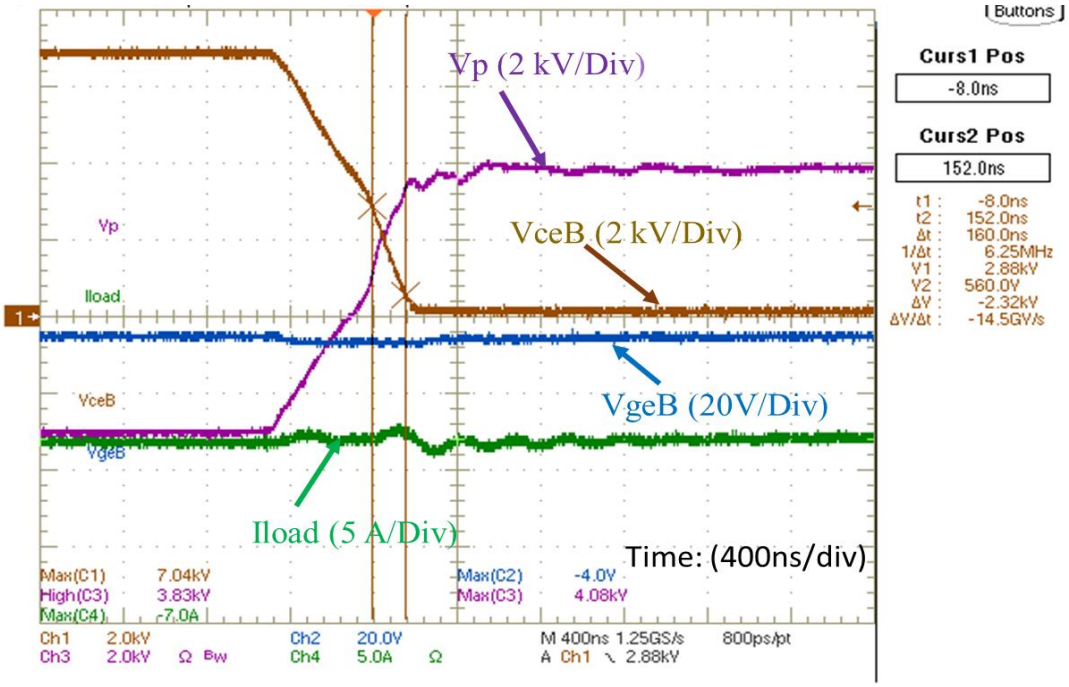


Fig. 5-17: Without external snubber in ZVS half-bridge converter, the maximum *dv/dt* (14.5 kV/µs) voltage across the bottom IGBT when top IGBT is turning-off

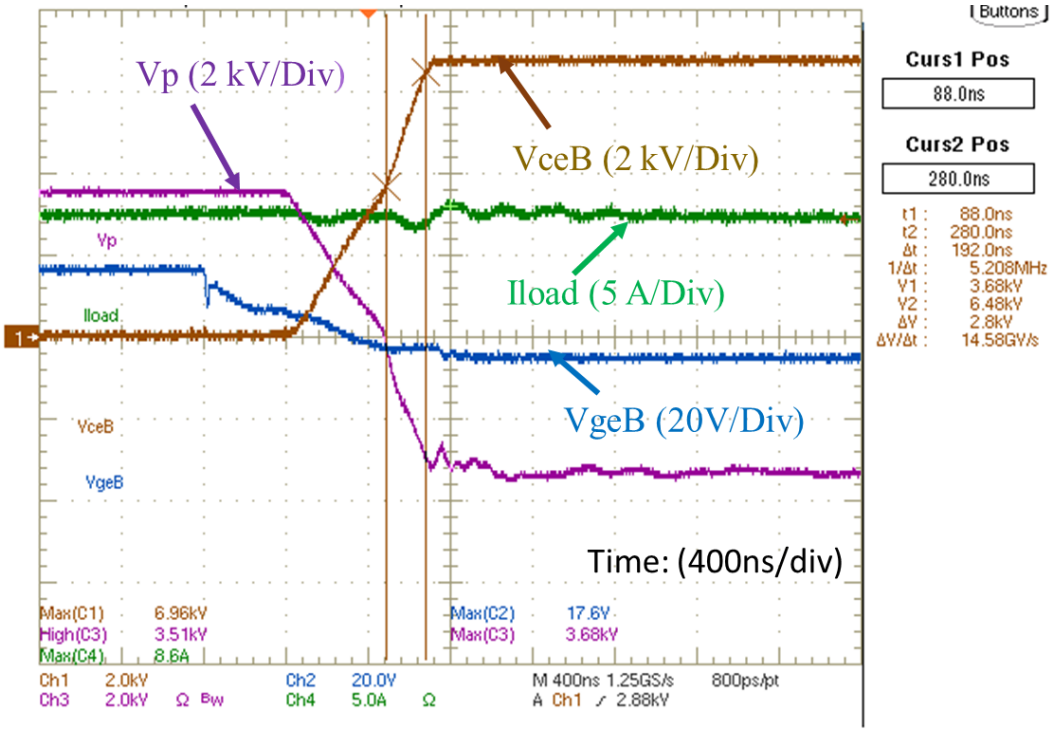


Fig. 5-18: Without external snubber in ZVS half-bridge converter, the maximum *dv/dt* (14.5 kV/μs) across the bottom IGBT during turn-off in the punch-through region

5.3.2 Total losses and *dv/dt* of 15 kV SiC IGBT (5 μm field-stop buffer layer) in Half-bridge DC-AC converter and with external snubber

An external 1.1 nF snubber capacitor is placed across the each of the 15 kV/40 A SiC IGBT in the half-bridge converter to achieve the ZVS turn-on and ZVS turn-off. The switching frequency of the half-bridge converter is 5 kHz. The converter is continuously run for 20 minutes. The heat sink temperature measured at the end of 20 minutes is 32.7^{o}C. The ambient temperature is 25.5^{o}C. The heat sink thermal resistance with forced air cooling is 0.1045-0.09 ^{o}C/W as mentioned in section 5.3.1. The total power dissipated in 15 kV/40 A IGBT module is P_d=68.89 to 80 W at 7 kV DC bus and Iload=8.2 A. With module thermal resistance estimated to be 0.2058 ^{o}C/W in section 5.3.1, the calculated junction temperature for the power dissipation of 68.89 to 80 W will be 46.87^{o}C to 49.16 ^{o}C.

With external 1.1nF snubber capacitor placed across each of the 15 kV/40 A SiC IGBT in the half-bridge converter, Fig. 5-19 and Fig. 5-20 show the transition of the voltage across the bottom IGBT (VceB), Bottom IGBT gate voltage (VgeB), AC Pole Voltage (Vp), load current (Iload) when top IGBT is turning off and bottom IGBT is turning off respectively.

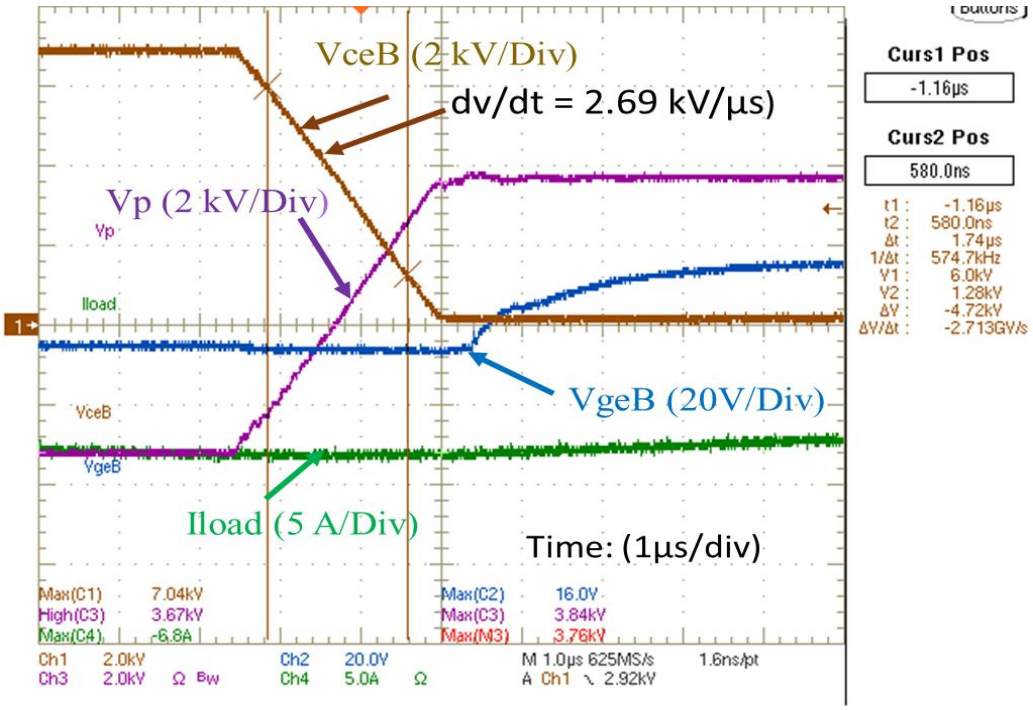


Fig. 5-19: With 1.1 nF snubber in ZVS half-bridge converter, *dv/dt* (2.71 kV/µs) across the bottom IGBT when the top IGBT is turning-off

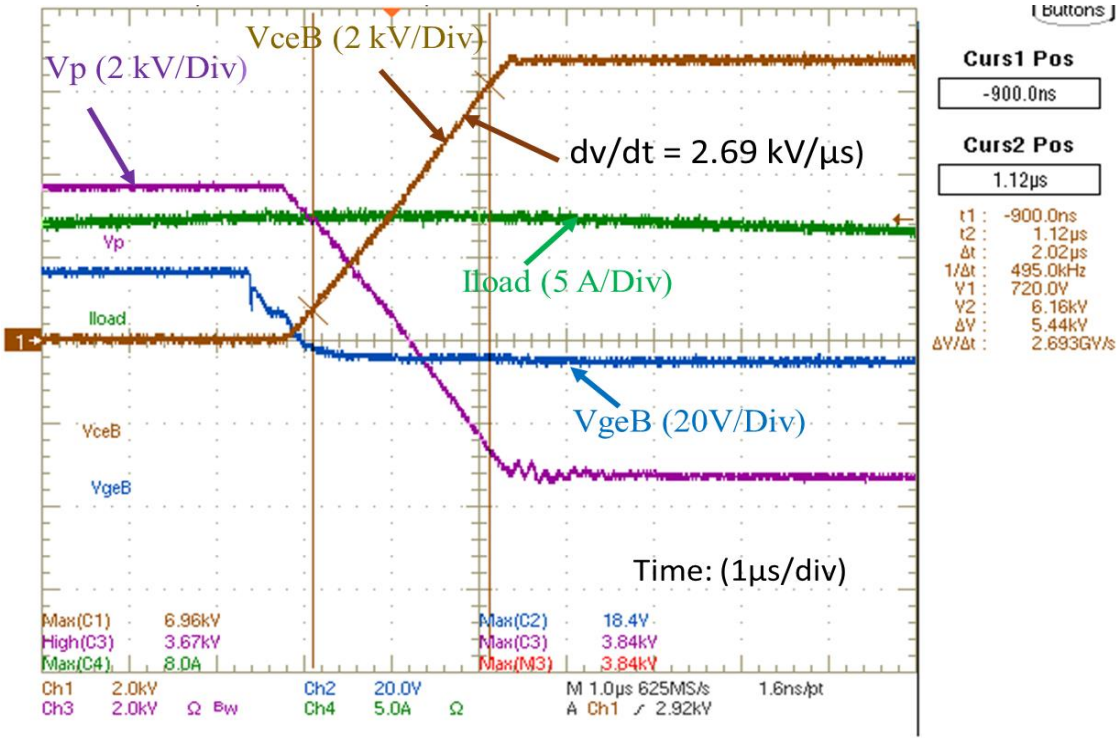


Fig. 5-20: With 1.1 nF snubber in ZVS half-bridge converter, *dv/dt* (2.69 kV/µs) across the bottom IGBT during turn-off

Fig. 5-19 and Fig. 5-20 show that both device voltage and the pole voltage do not have two slopes compared to the ZVS case without snubber and become single slope similar to majority carrier 10-15kV MOSFET switching voltage. The dv/dt across the IGBTs and also AC pole voltages are **reduced by nearly six times** as compared to ZVS case without snubber as mentioned section 5.3.1. The reduction in total power dissipation is 27.77% compared to the without a snubber.

5.3.3 Comparative evaluation of hard switching half-bridge DC-DC converter and soft switching DC-AC half-bridge using of 15 kV/40 A 5 µm filed stop buffer layer IGBT

In this section, the switching frequency of 5 µm 15 kV/40 A SiC IGBT module in hard switching DC-DC boost converter have been computed for the same switching voltage (at 7 kV), current (8.2 A) and also for same total losses of 68.89 W to 80 W (or junction temperature of 46.87^{o}C to 49.16 ^{o}C) as mentioned in section 5.3.2. The switching loss data for 15 kV/40 A SiC IGBT module at 7 kV DC bus for different current values and on state voltage drop for different current values have been characterized in Chapter 3, section 3.6 as shown in Fig. 3-48.

Using these loss data, the total losses (hard switching losses and conduction losses) in 15 kV/40 A module are calculated for a DC-DC boost bidirectional converter (i.e. half bridge pole leg) at a duty ratio of 0.75 using the PLECS simulation and analytical equation mentioned in [60]. The comparison of total losses with soft switching (ZVS) and hard switching is shown in Table 5-6 for the junction temperature (46.87^{o}C to 49.16 ^{o}C). For the same total power loss (68.89 W to 80 W) at 7 kV, 8.2 A, the estimated switching frequency of hard switching 15 kV/ 40 A module in DC-DC boost converter will be only 1.1 to 1.4 kHz.

Table 5-6: Comparison of switching frequency operation of 15 kV SiC IGBT with soft-switching and hard switching at 7 kV dc bus, 8 A switching current

	Total Power losses (Switching +Conduction losses)	**Switching Frequency**	**Junction temperature**
ZVS With external snubber (1.1 nF)	68.89 W to 80 W	5 kHz	46.87^{o}C to 49.16 ^{o}C
Hard switching	68.89 W to 80 W	1.1 kHz to 1.4 kHz	46.87^{o}C to 49.16 ^{o}C

The 35 kVA, 22 kV/800 V transformer parasitic currents are calculated using the characterized '*dv/dt*' with and without a snubber. Table 5-7 shows the comparison of parasitic capacitive currents drawn by a transformer with and without snubber in a DAB converter (shown in Fig. 5-1) using 5 µm 15 kV/40

A SiC IGBT. There is a significant reduction in parasitic transformer currents with snubber due to a reduction in AC pole voltage '*dv/dt*' as compared to the case without snubber case.

Table 5-7: Comparison of Transformer parasitic currents in DAB converter with and without snubber using 15 kV SiC IGBT (5 µm) at 9 kV dc bus, 5 A switching current

	AC pole *dv/dt*	**Transformer (35 kVA, 22 kV/800V) parasitic capacitance [63][64]**	**Parasitic capacitance current (C.*dv/dt*)**	**% of coupling current w.r.t rated current (5 A peak on HV side primary)**
DAB converter without external snubber	17.45kV/µs	Self-capacitance (C_p) 50 pF	0.87 A peak	17.5%
		Mutual-capacitance (C_{p1}) 300 pF	5.23 A peak	104%
DAB with external snubber (2.2 nF)	1.57 kV/µs	Self-capacitance (C_p) 50 pF	0.078 A peak	1.56%
		Mutual-capacitance (C_{p1}) 300 pF	0.47 A peak	9.4%

Therefore, it has been shown in from the sections 5.2-5.3 that a small external snubber capacitor across the 15 kV SiC IGBT will enable DC-DC soft switching converters like DAB with reduced total loss and high switching frequency with a significant reduction in '*dv/dt'*.

5.4 Series connection of HV SiC devices

The DC-DC soft switching converter (like DAB converter) if used in HVDC to MVDC applications, a series connection of devices may be required on HV side of DAB converter as shown in Fig. 5-21. Each switch on HV side of DAB converter could be either 10 kV -15 kV SiC MOSFET devices or 15 kV SiC IGBT. Similar to the series connection of LV SiC MOSFET devices (Chapter 2), the main challenges for series connection of HV SiC devices are: (1) unbalance in the static voltage balancing due to a mismatch in device leakage currents; (2) unbalance in the dynamic voltage balancing due to a mismatch in gate signal delays. With proper selection of external snubber capacitor (C_d) and resistor (R_s), the static and dynamic voltage imbalance between the devices can be reduced and hence matching of the devices can be avoided. The HV SiC IGBT or SiC MOSFET used on HV side of the DAB converter are connected with external snubber capacitor (C_d) and resistor (R_s) across each are shown in Fig. 5-21.

The sections 5.4.1 to 5.4.4 show the characterization of series connected HV SiC devices with different snubber values to enable DC-DC transformer-using series connected HV SiC devices per

arm, along with additional benefits such as zero voltage switching during turn-off to reduce switching losses and reduced '*dv/dt* '.

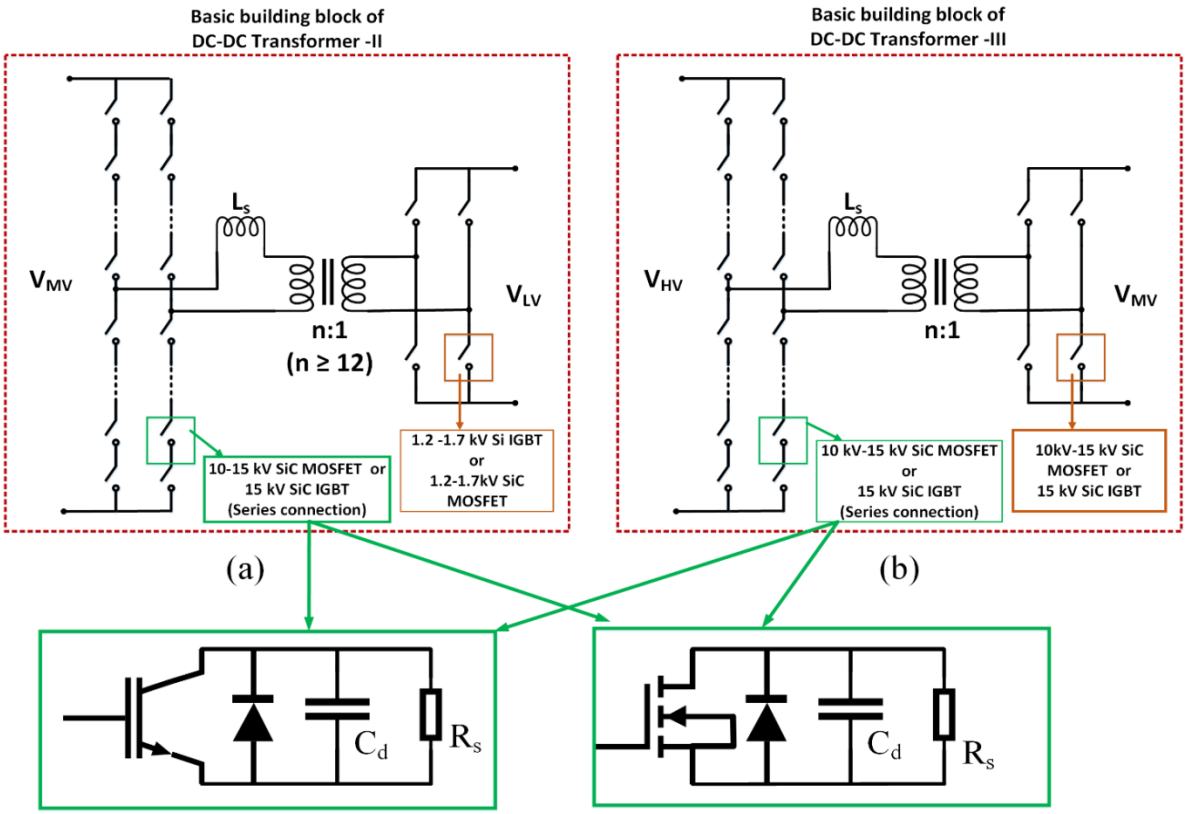


Fig. 5-21: Application of series connected HV SiC device on HV- side of DC-DC transformer building block for (a) MVDC to LVDC ; (b) HVDC to MVDC

5.4.1 Series connection of 15 kV/20 A SiC IGBT (2 µm field-stop buffer layer)

The 15 kV SiC IGBT (2 µm buffer layer) has been used for evaluation of series connection. The voltage blocking test on two 15 kV SiC IGBT devices is performed independently up to 10 kV voltage. Fig. 5-22 shows the plot of leakage current with device blocking voltage. It is observed that the two selected 15 kV SiC IGBTs have widespread leakage currents.

The static voltage-sharing test is performed without any compensation with two 15 kV SiC IGBT connected using the setup shown in Fig. 5-23 with gate to emitter voltage set at -5 V for both devices. The experimental setup with two series connected devices is shown in Fig. 5-24. From the experimental results, it is observed that there is a significant imbalance in static voltage (ΔV) sharing and only one device (V_{ce1}) blocking the total applied voltage as shown in Fig. 5-25. The imbalance in static voltage sharing is nearly 5 kV at a total voltage of 5.03 kV.

The voltage imbalance during dynamic mode is due to a mismatch in device parasitic capacitances, device turn-off delays (Δt_{doff}) and the difference in delay time between gate signals from external gate drivers. The dynamic voltage sharing test between two 15 kV SiC IGBT without any compensation method is performed. It is observed that the difference in dynamic voltage (ΔV_{max}) between the two 15 kV SiC IGBT devices during turn-off transition is around 1.3 kV, at a total voltage of 6 kV dc bus as shown in Fig. 5-26.

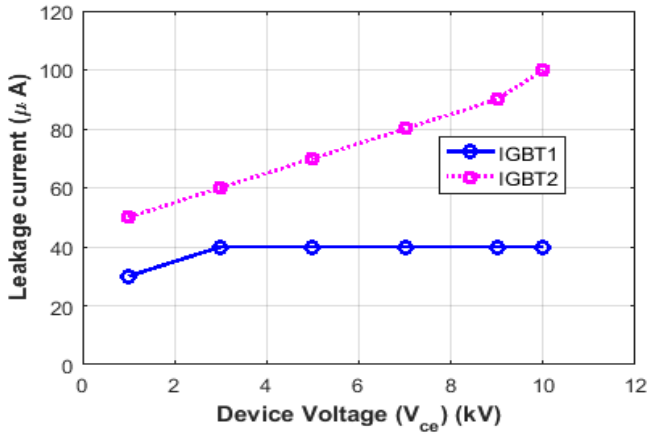


Fig. 5-22: Leakage current at different blocking voltages and T_j=25^{0}C

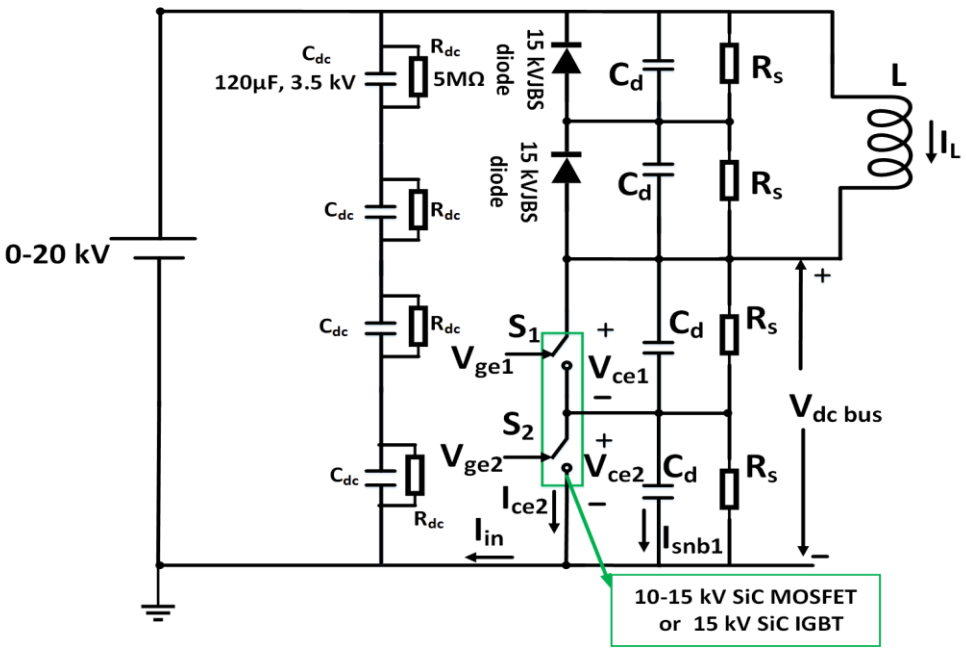


Fig. 5-23: Inductive clamped circuit of two series connected HV SiC devices

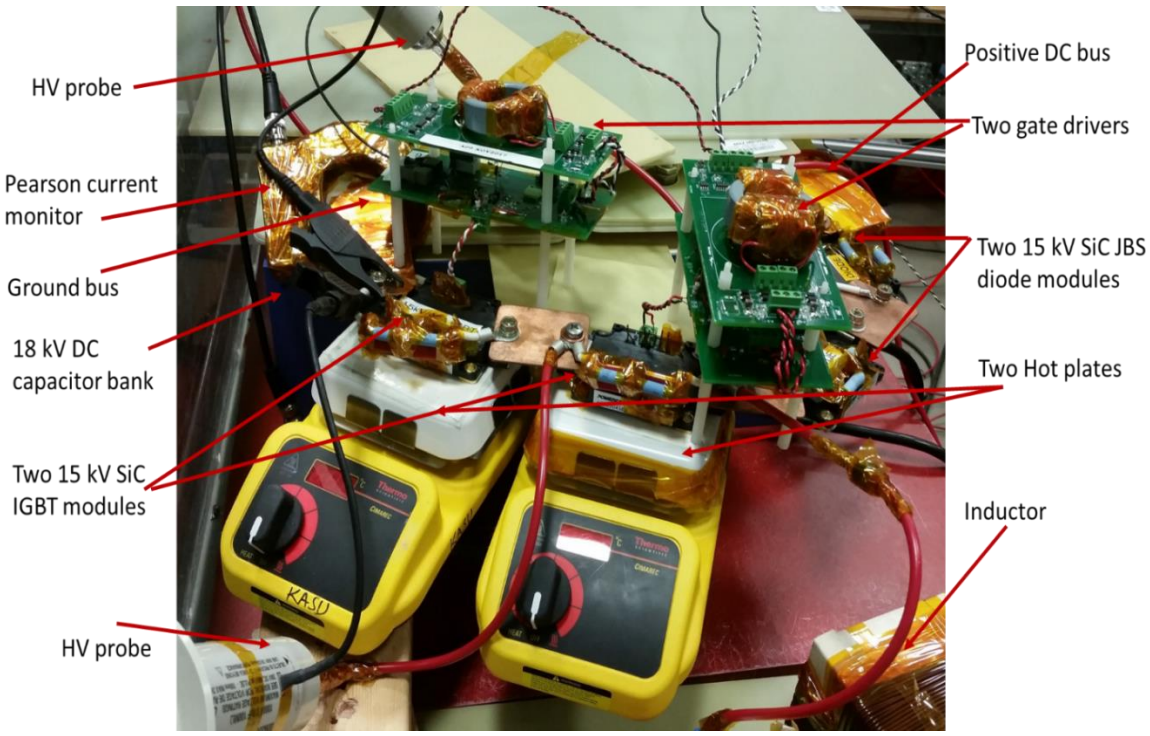


Fig. 5-24: Experimental setup of two series connected 15 kV SiC IGBT devices

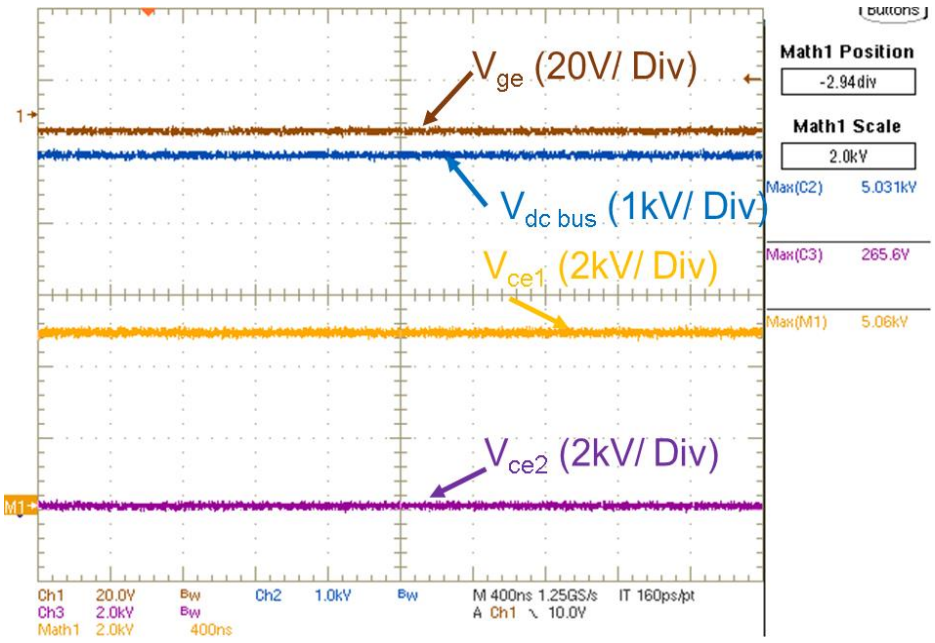


Fig. 5-25: Unbalanced static voltage sharing between two 15 kV SiC IGBT at 5 kV dc bus voltage and at T_j=25^{0}C; [Ch2 (Blue): Total dc bus voltage V_{dcbus}; Ch3 (Magenta): Bottom device V_{ce2} ; Math1(Yellow): Ch2-Ch3: Top device $V_{ce1;}$ Ch1(Brown): Bottom device gate voltage V_{ge}]

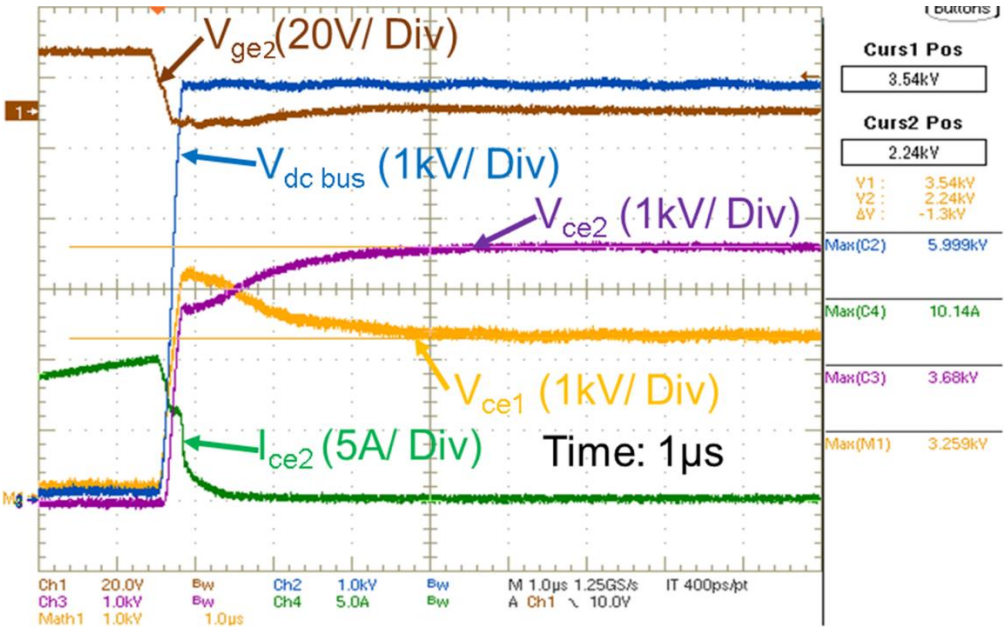


Fig. 5-26: Unbalanced dynamic voltage sharing between two 15 kV SiC IGBT at 6 kV dc bus voltage and at T_j=25^{0}C; [Ch1(Brown): Bottom device gate voltage V_{ge2}; Ch2 (Blue): Total dc bus voltage V_{dcbus}; Ch3 (Magenta): Bottom device V_{ce2}; Math1(Yellow): Ch2-Ch3: Top device V_{ce1} ; Ch4 (Green): Bottom device current: I_{ce2};]

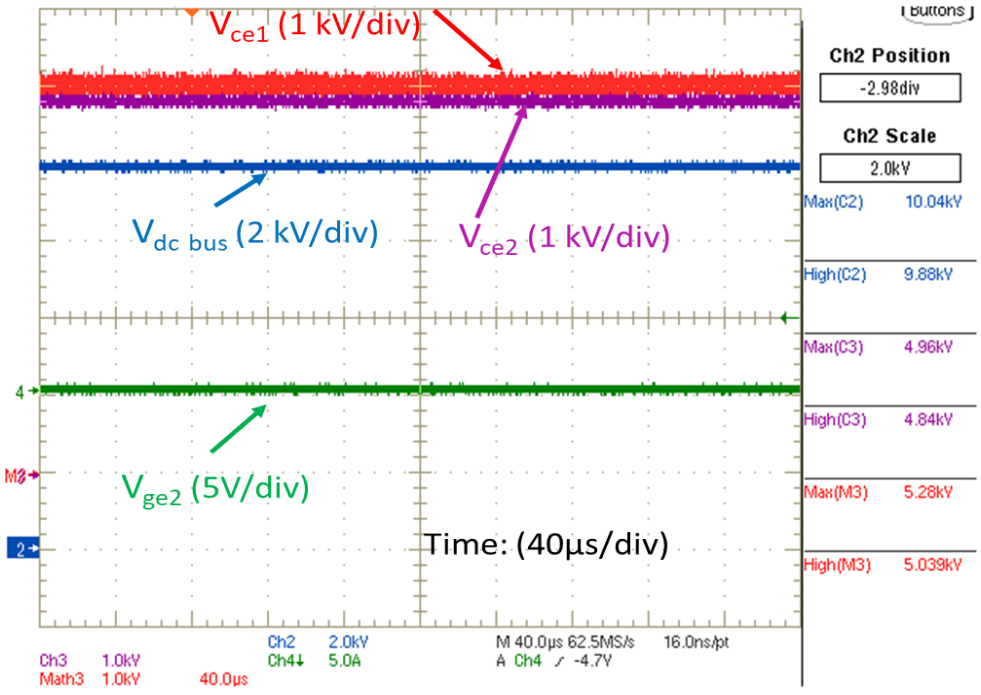


Fig. 5-27: Static voltage sharing between two 15 kV SiC IGBTs (2 µm) at 10 kV dc bus with external snubber resistor (R_s = 20 MΩ) and at T_j=25^{0}C

The experimental static and dynamic voltage test on two series connected 15 kV SiC IGBT (with an external snubber across each) are done using the inductive clamped setup shown in Fig. 5-23. The difference in static voltage (ΔV) imbalance is minimized with parallel balancing resistor R_s =20 MΩ connected across each device to offset the spread in leakage currents. Fig. 5-27 shows the static voltage sharing with external resistance (R_s). The voltage imbalance has been reduced significantly. The difference in static voltage imbalance at 10 kV total dc bus is nearly 200V and which is nearly 10% of the nominal base operating voltage of each device (V_{dcbus} /2=10 kV/2=5 kV).

The dynamic voltage balancing during turn-off is achieved with snubber capacitor (C_d) across each device. Fig. 5-28 shows the experimental results showing the dynamic voltage balancing between two series connected 15 kV, 20 A SiC IGBT devices with external snubber at 11 kV, 20 A. The difference in dynamic voltage between the two 15 kV SiC IGBT devices during turn-off transition is around 980V. Table 5-8 shows the difference in voltage imbalance between the two SiC IGBT device at different dc bus voltages and switching currents with snubber values of (C_dR_S): 2.2 nF, 20 MΩ and T_j=25^{0}C. The difference in voltage imbalance between the devices nearly constant for a given switching current and at different DC bus voltages. Therefore, it is expected that the voltage imbalance between two devices at 18 kV to 20 kV dc bus will also be nearly 1 kV for 20 A switching current. It is nearly 10-11% of the rated base operating voltage of each device ((V_{dcbus} /2 = 9 kV-10 kV). The 15 kV SiC IGBT device nominal operating voltage is 10 kV, therefore, the total dc bus voltage has to be 18 kV to 20 kV to make the voltage across the device nearly 9 kV to 10 kV.

Table 5-8: Summary of voltage imbalance between two SiC IGBT devices at different dc bus voltages and switching currents, with snubber value (C_dR_s): 2.2 nF, 20 MΩ, T_j=25^{0}C

DC bus voltage, switching current	Voltage imbalance between two SiC IGBT (2 µm)	DC bus voltage, switching current	Voltage imbalance between two SiC IGBT (2 µm)	DC bus voltage, switching current	Voltage imbalance between two SiC IGBT (2 µm)
9 kV, 10 A	600 V	9 kV, 15 A	800 V	9 kV, 20 A	1000 V
10 kV, 10 A	600 V	10 kV, 15 A	800 V	10 kV, 20 A	1000 V
11 kV, 10 A	600 V	11 kV, 15 A	800 V	11 kV, 20 A	1000 V

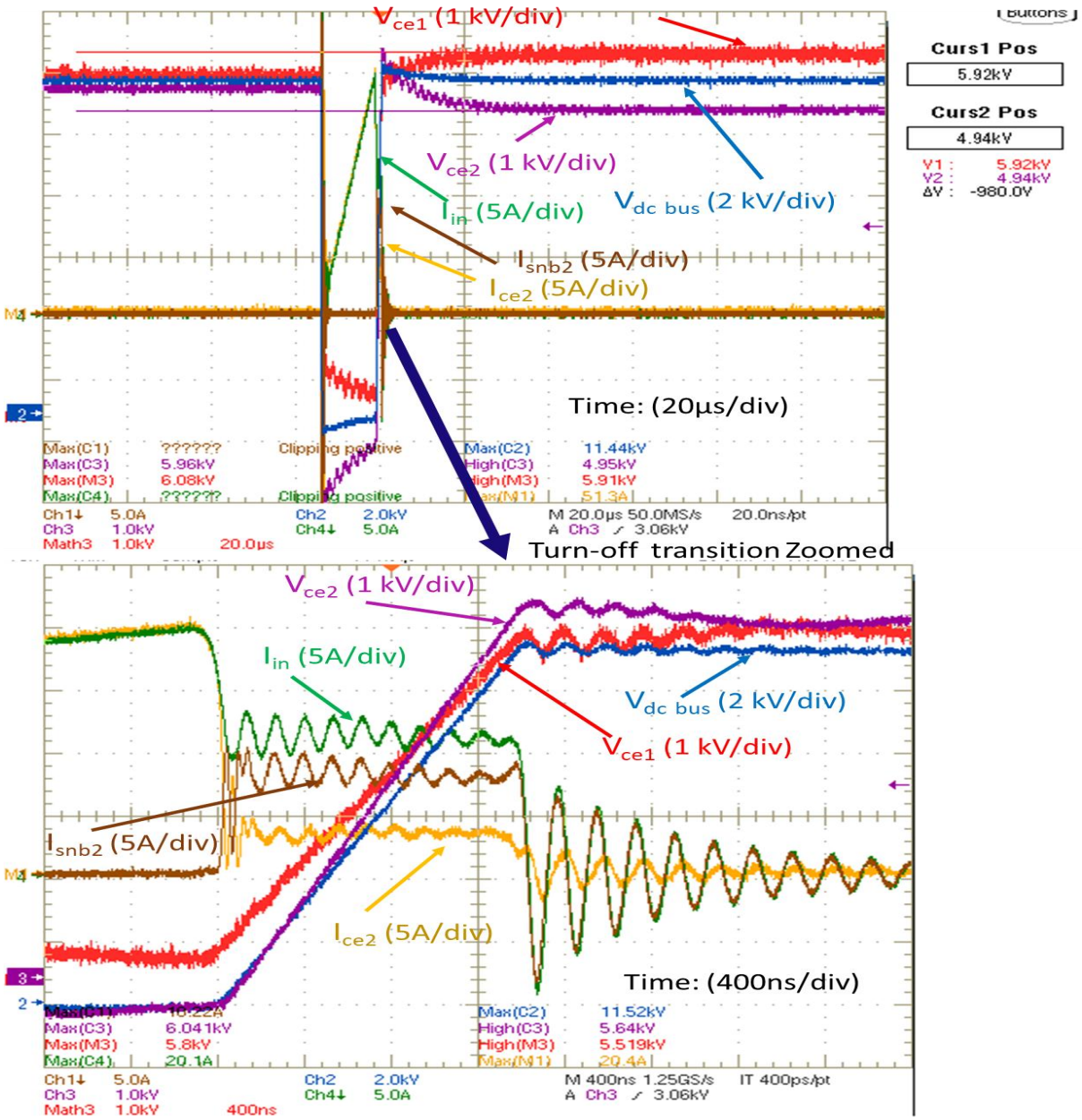


Fig. 5-28: Dynamic voltage sharing between two 15 kV SiC IGBT (2 µm buffer layer) devices at 11 kV dc bus voltage with external snubber (C_dR_s :2.2 nF, 20 MΩ), T_j=25^{0}C and *dv/dt* (4.2 kV/µs) of each device. [Ch1 (Brown): Bottom device snubber capacitor current I_{snb2}; Ch2 (Blue): Total dc bus voltage V_{dcbus}; Ch3 (Magenta): Bottom device V_{ce2}; Ch4 (Green): Input current from DC bus I_{in} ; Math3 (Red): Ch2-Ch3: Top device V_{ce1}; Math1 (Yellow): Bottom device current I_{ce2}]

Table 5-9: Summary of voltage imbalance between two 15 kV SiC IGBT devices (2 µm buffer layer) at different dc bus voltages and switching currents, with snubber value (C_dR_s):1.1 nF, 20 MΩ, T_j=25^{0}C

DC bus voltage, switching current	Voltage imbalance between two SiC IGBT (2 µm)	DC bus voltage, switching current	Voltage imbalance between two SiC IGBT (2 µm)	DC bus voltage, switching current	Voltage imbalance between two SiC IGBT (2 µm)
9 kV, 10 A	1.28 kV	9 kV, 15 A	1.62 kV	9 kV, 20 A	2 kV
10 kV, 10 A	1.28 kV	10 kV, 15 A	1.62 kV	10 kV, 20 A	2 kV
11 kV, 10 A	1.28 kV	11kV, 15 A	1.62 kV	11kV, 20 A	2 kV
12 kV 10 A	1.28 kV	12 kV, 15 A	1.62 kV	12 kV, 20 A	2 kV
13 kV 10 A	1.28 kV	13 kV, 15 A	1.62 kV	13 kV, 20 A	2 kV

Table 5-10: Summary of voltage imbalance between two 15 kV SiC IGBT devices (2 µm buffer layer) at different dc bus voltages and switching currents, with snubber value (C_dR_s): 2.2 nF, 20 MΩ, T_j=125^{0}C

DC bus voltage, switching current	Voltage imbalance between two SiC IGBT (2µm)	DC bus voltage, switching current	Voltage imbalance between two SiC IGBT (2µm)	DC bus voltage, switching current	Voltage imbalance between two SiC IGBT (2µm)
9 kV, 10 A	750 V	9 kV, 15 A	950 V	9 kV, 20 A	1200 V
10 kV, 10 A	750 V	10 kV, 15 A	950 V	10 kV, 20 A	1200 V
11 kV, 10 A	750 V	11kV, 15 A	950 V	11kV, 20 A	1200 V
12 kV, 10 A	750 V	12 kV, 15 A	950 V	12 kV 20 A	1200 V
13 kV, 10 A	750 V	13 kV, 15 A	950 V	13 kV 20 A	1200 V

The dynamic voltage test on two series connected SiC IGBT (2 µm buffer layer) devices has been conducted at different snubber values 1.1 nF, 20 MΩ. The summary of voltage imbalance between two devices at different DC bus voltages and switching currents is shown in Table 5-9. The voltage imbalance between two devices is increased nearly two times with 1.1 nF, 20 MΩ snubber values compared to 2.2 nF, 20 MΩ snubber values.

The dynamic voltage test on two series connected SiC IGBT device (2 µm layer) is also conducted with increased junction temperature. The two device base plates are heated using hotplate arrangement as shown in Fig. 5-24. Table 5-10 shows the summary of voltage imbalance between two devices at different DC bus voltages and switching currents with snubber values 2.2 nF, 20 MΩ and T_j=125^{0}C. Comparing Table 5-8 and Table 5-10, there is a slight increase in voltage imbalance between the two SiC IGBT devices at T_j= 25^{0}C to 125^{0}C, for a given switching current and at different dc bus voltages.

Therefore, a small external snubber capacitor and static balancing resistor across the 15 kV SiC IGBT (2 µm buffer layer) device will enable series connection with the voltage imbalance across the devices less than 10-12% of the rated nominal voltage of the device and also a significant reduction in *dv/dt*.

5.4.2 Series connection of 15 kV/40 A SiC IGBT (5 µm field-stop buffer layer)

This section presents the characterization of two series connected 15 kV/40 A SiC IGBT modules (5 µm buffer layer) (two parallel dies). The voltage-blocking test on two 15 kV/40 A SiC IGBT modules (5 µm buffer layer) devices is performed independently up to 10 kV voltage. Fig. 5-29 shows the plot of leakage current with device blocking voltage. Compared to 2 µm SiC IGBT devices, it is observed that the two-selected 5 µm 15 kV/40 A SiC IGBTs have much higher widespread in leakage currents.

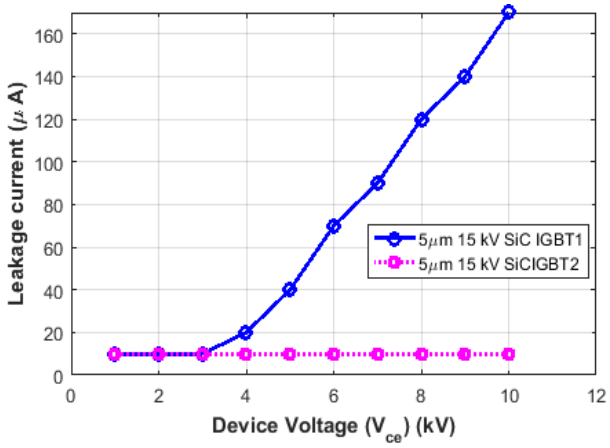


Fig. 5-29: Leakage currents of two 5 µm 15 kV SiC IGBT devices at different blocking voltages and T_j=25^{0}C

The static voltage-sharing test is performed with balancing resistor of 8 MΩ across each of the 15 kV SiC IGBT using the setup shown in Fig. 5-30 with gate to emitter voltage set at -5V for both the devices. The 2 µm 15 kV/40 A SiC IGBTs have been replaced with 5 µm SiC IGBT devices in the

experimental setup shown in Fig. 5-24. From the experimental results, it is observed that the imbalance in static voltage (ΔV) sharing is nearly 1.5 kV at a total dc bus voltage of 14 kV. Table 5-11 shows the percentage static voltage imbalance at different dc bus voltages and T_j=25^{0}C. The trend shows that the percentage of static voltage imbalance at higher dc bus (18 kV -20 kV dc bus) operation is nearly 20 % of the rated nominal operating voltage 15 kV SiC IGBT and the rated nominal operating voltage of 15 kV SiC IGBT is 10 kV. The static voltage balancing is also tested at T_j =125^{0}C. The percentage static voltage imbalance at 125^{0}C is nearly equal to 25^{0}C. Therefore, static balancing resistor (R_s) < 8 MΩ may need to be used to bring the static voltage imbalance to 10 to 15% of rated voltage or devices with marginal leakage current spread needs to be used for the series connection.

The leakage currents and their spread are much higher in 5 µm 15 kV SiC IGBT devices compared to 2 µm SiC IGBT devices. Therefore, the static voltage imbalance in the 5 µm SiC IGBT devices is higher than 2 µm SiC IGBT devices. In addition, the static voltage-balancing resistor is nearly two times lower than 2 µm SiC IGBT devices to offset high leakage current spread.

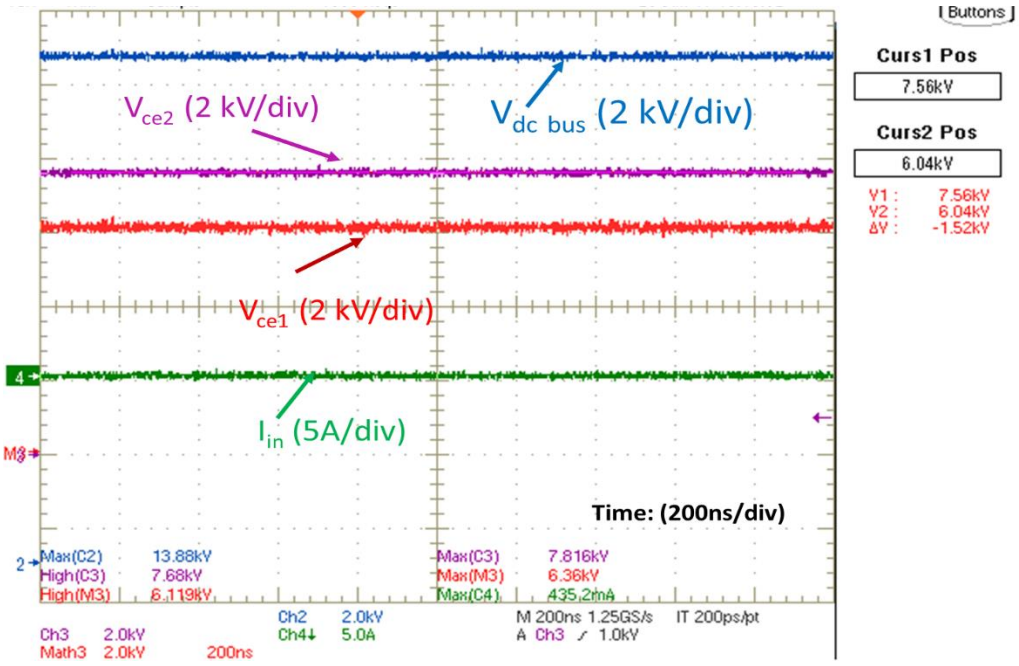


Fig. 5-30: Static voltage sharing between two 15 kV SiC IGBTs (5 µm) at 14 kV dc bus with external snubber resistor (R_s) and T_j = 25^{0}C

Table 5-11: Summary of static voltage imbalance between two 15 kV SiC IGBT devices (5 µm buffer layer) at different dc bus voltages with external snubber resistor (R_s): 8 MΩ, T_j=25^{0}C

DC bus voltage (V_{dcbus})	Difference in static voltage imbalance (ΔV_s)	% Difference in static voltage imbalance w.r.t rated base operating voltage (ΔV_s /V_{dcbus} /2) x100
6 kV	0.78 kV	26%
7 kV	0.94 kV	26.8%
9 kV	1.12 kV	24.9%
11 kV	1.2 kV	21.8%
13 kV	1.4 kV	21.5%
14 kV	1.5 kV	21.4%

The dynamic voltage balancing during turn-off is achieved with snubber capacitor (C_d) across each device. Fig. 5-31 shows the experimental results showing the dynamic voltage balancing between two series connected 15 kV, 40 A SiC IGBT devices with external snubber (1.1 nF, 8 MΩ) at 14 kV dc bus, 20 A switching current and T_j=125^{0}C. The difference in dynamic voltage between the two 15 kV SiC IGBT devices during turn-off transition is around 800 V. Table 5-12 shows the difference in voltage imbalance between the two SiC IGBT devices at different dc bus voltages and switching currents with snubber values of (C_dR_S): 1.1 nF, 8 MΩ and T_j=125^{0}C. The difference in voltage imbalance between the devices nearly constant for a given switching current and at different DC bus voltages. Therefore, it is expected that the voltage imbalance between two devices at 18 kV to 20 kV dc bus will also be nearly 900 V for 20 A switching current. It is nearly 10-11% of the rated base operating voltage of each device (V_{dcbus} /2 = 9 kV-10 kV) and the 15 kV SiC IGBT device nominal operating voltage is 10 kV. Therefore, the total dc bus voltage has to be 18 kV to 20 kV to make the voltage across the device nearly 9 kV to 10 kV.

Comparing Table 5-12 and Table 5-13, for the same value of snubber values, the dynamic voltage imbalance between the two 5 µm SiC IGBT devices is much less at 25^{0}C compared to 125^{0}C.

The dynamic voltage test on two series connected SiC IGBT devices has been conducted at different snubber values 0.5 nF, 8 MΩ and T_j=125^{0}C. The summary of voltage imbalance between the two devices at different DC bus voltages and switching currents is shown in Table 5-14. The voltage imbalance between two devices is increased nearly two times with 0.5 nF, 8 MΩ snubber values compared to 1.1 nF, 8 MΩ snubber values.

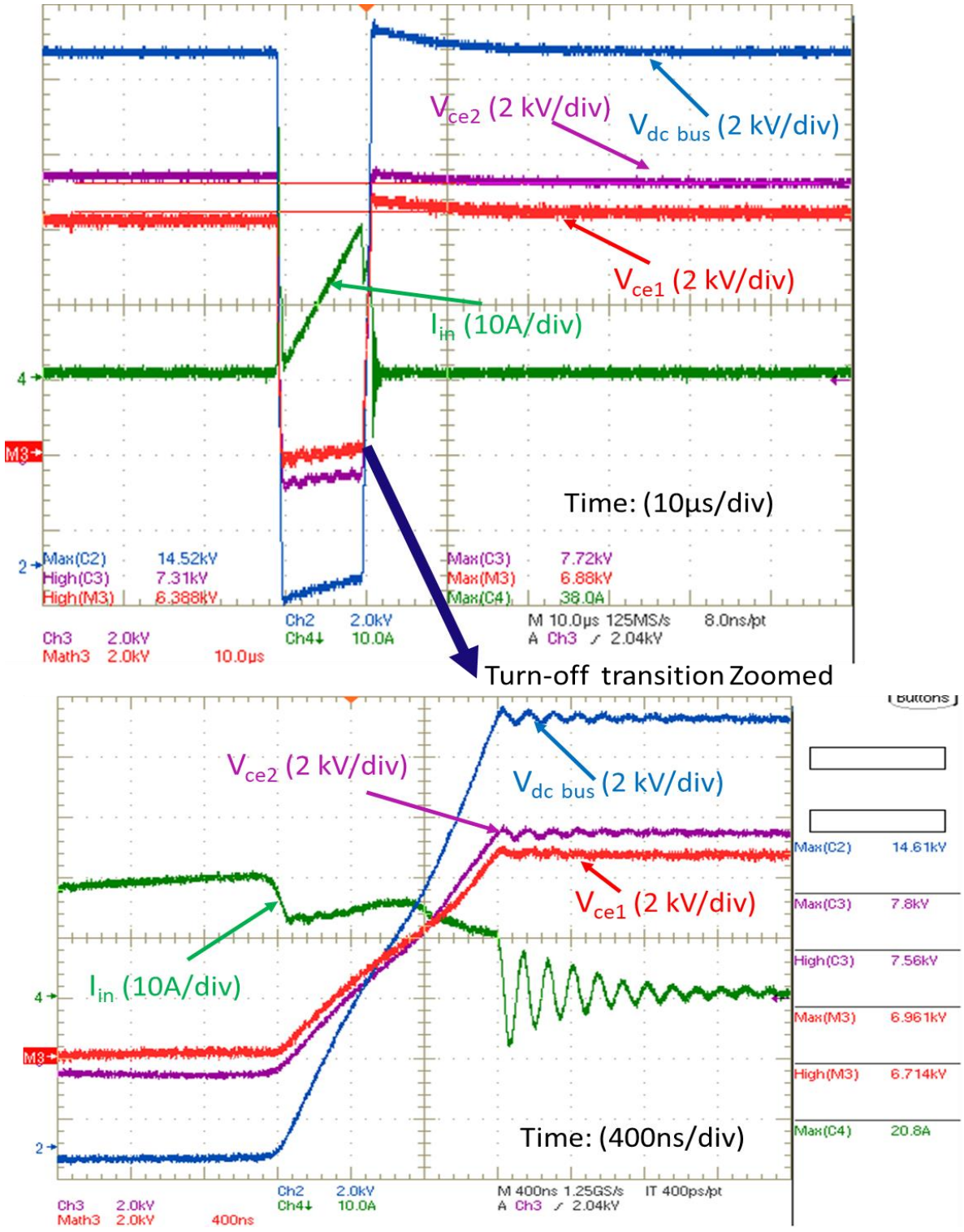


Fig. 5-31: Dynamic voltage sharing between two 15 kV SiC IGBT (5 µm buffer layer) devices at 14 kV dc bus voltage with external snubber (C_dR_s :1.1 nF, 8 MΩ), and dv/dt (5.8 kV/µs) of each device [Ch2 (Blue): Total dc bus voltage V_{dcbus}; Ch3 (Magenta): Bottom device V_{ce2}; Ch4 (Green): Input current from DC bus I_{in}; Math3 (Red): Ch2-Ch3: Top device V_{ce1}]

Table 5-12: Summary of dynamic voltage imbalance between two 15 kV SiC IGBT devices (5 µm buffer layer) at different dc bus voltages and switching currents, with snubber value (C_dR_s): 1.1 nF, 8 MΩ, $T_j=125^0C$

DC bus voltage, switching current	Voltage imbalance between two SiC IGBT (5µm)	DC bus voltage, switching current	Voltage imbalance between two SiC IGBT (5 µm)	DC bus voltage, switching current	Voltage imbalance between two SiC IGBT (5µm)
10 kV, 10 A	500 V	10 kV, 15 A	700 V	10 kV, 20 A	900 V
12kV, 10 A	500 V	12 kV, 15 A	700 V	12 kV, 20 A	900 V
13 kV, 10 A	500 V	13 kV, 15 A	700 V	13 kV, 20 A	900 V
14 kV, 10 A	500 V	14 kV, 15 A	700 V	14 kV, 20 A	900 V

Table 5-13: Summary of dynamic voltage imbalance between two 15 kV SiC IGBT devices (5 µm buffer layer)at different dc bus voltages and switching currents, with snubber value (C_dR_s): 1.1 nF, 8 MΩ, $T_j=25^0C$

DC bus voltage, switching current	Voltage imbalance between two SiC IGBT (5µm)	DC bus voltage, switching current	Voltage imbalance between two SiC IGBT (5µm)	DC bus voltage, switching current	Voltage imbalance between two SiC IGBT (5µm)
10 kV, 10 A	300 V	10 kV, 15A	200 V	10 kV, 20 A	< 100 V
12kV, 10 A	300 V	12kV, 15A	200 V	12 kV, 20 A	< 100 V
13 kV, 10 A	300 V	13 kV, 15A	200 V	13 kV 20 A	< 100 V
14 kV, 10 A	300 V	14kV, 15A	200 V	14 kV 20 A	< 100 V

Table 5-14: Summary of dynamic voltage imbalance between two 15 kV SiC IGBT devices (5 µm buffer layer) at different dc bus voltages and switching currents, with snubber value (C_dR_s): 0.5 nF, 8 MΩ, $T_j=125^0C$

DC bus voltage, switching current	Voltage imbalance between two SiC IGBT (5µm)	DC bus voltage, switching current	Voltage imbalance between two SiC IGBT (5µm)	DC bus voltage, switching current	Voltage imbalance between two SiC IGBT (5µm)
10 kV, 10 A	1.4 kV	10 kV, 15A	1.9 kV	10 kV, 20 A	2.1 kV
12 kV, 10 A	1.4 kV	12kV, 15A	1.9 kV	12 kV, 20 A	2.1 kV
13 kV, 10 A	1.4 kV	13 kV, 15 A	1.9 kV	13 kV, 20 A	2.1 kV
14kV, 10 A	1.4 kV	14 kV, 15 A	1.9 kV	14 kV, 20 A	2.1 kV

Comparing Table 5-10 and Table 5-12, the value of snubber capacitor required for 5 µm SiC IGBT devices is nearly 50% less compared to 2 µm SiC IGBT devices for the nearly same value of voltage imbalance between the devices.

Therefore, a small external snubber capacitor and static balancing resistor across the 15 kV SiC IGBT (5 µm buffer layer) device will enable series connection with the voltage imbalance across the devices less than 10-12% of the rated nominal voltage of the device and also a significant reduction in *dv/dt*.

5.4.3 Series connection of 15 kV SiC MOSFET devices

The static voltage-sharing test is performed with balancing resistor of 20 MΩ across each of the 15 kV SiC MOSFET using the setup shown in Fig. 5-30 with gate to source voltage set at -5 V for both the devices. The 15 kV SiC IGBTs have been replaced with 15 kV SiC MOSFET devices in the experimental setup shown in Fig. 5-24. From the experimental results, it is observed that the imbalance in static voltage (ΔV) sharing is nearly 1.5 kV at a total dc bus voltage of 14 kV. Table 5-15 shows the percentage static voltage imbalance at different dc bus voltages. The trend shows that the percentage of static voltage imbalance at higher dc bus (18 kV -20 kV dc bus) operation is nearly 20 % of the rated nominal operating voltage 15 kV SiC IGBT. The rated nominal operating voltage of 15 kV SiC MOSFET is 10 kV. Therefore, static balancing resistor (R_s) < 20 MΩ may need to be used to bring the static voltage imbalance to 10 to 15% of rated voltage.

Table 5-15: Summary of static voltage imbalance between two SiC IGBT devices at different dc bus voltages with (R_s): 20 MΩ, T_j=125^{0}C

DC bus voltage (V_{dcbus})	Difference in static voltage imbalance (ΔV_s)	% Difference in static voltage imbalance w.r.t rated base operating voltage (ΔV_s /V_{dcbus} /2) x100
5.8 kV	0.7 kV	23.8 %
6.8 kV	0.82 kV	23.4%
9 kV	1 kV	22.2%
10 kV	1.1 kV	22%
13 kV	1.2 kV	18.46%
13.8 kV	1.3 kV	18.7%

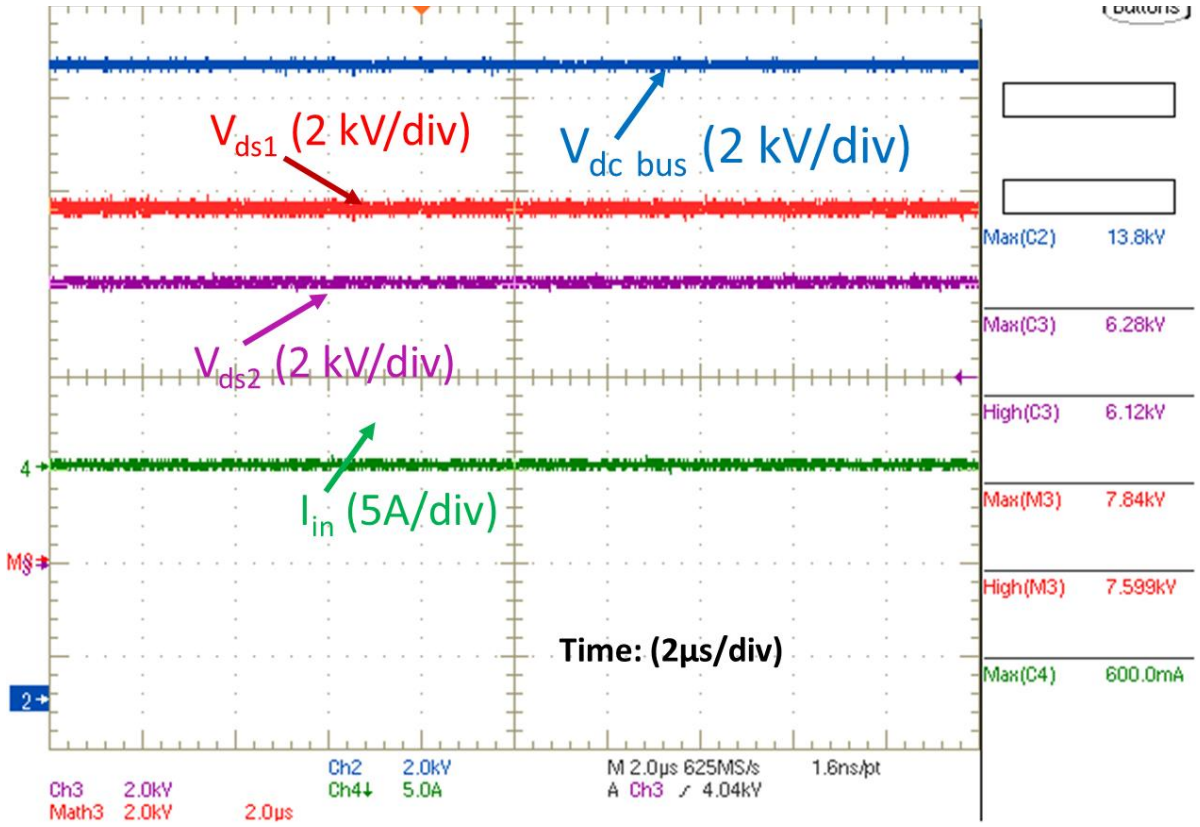


Fig. 5-32: Static voltage sharing between two 15 kV SiC MOSFET devices at 14 kV dc bus with external snubber resistor (R_s) and at T_j=125^{0}C

The dynamic voltage balancing during turn-off is achieved with snubber capacitor (C_d) across each device. Fig. 5-33 shows the experimental results showing the dynamic voltage balancing between two series connected 15 kV SiC MOSFET devices with external snubber (1.1 nF, 20 MΩ) at 14 kV dc bus, 20A switching current and T_j=125^{0}C. The difference in dynamic voltage between the two 15 kV SiC IGBT devices during turn-off transition is around 600 V. Table 5-16 shows the difference in dynamic voltage imbalance between the two SiC IGBT device at different dc bus voltages and switching currents with snubber values of (C_dR_S): 1.1 nF, 20 MΩ and T_j=125^{0}C. The difference in voltage imbalance between the devices nearly constant for a given switching current and at different DC bus voltages. Therefore, it is expected that the voltage imbalance between two devices at 18 kV to 20 kV dc bus will also be nearly 600 V for 20A switching current. The voltage imbalance is less than 10-11% of the rated base operating voltage of each device ((V_{dcbus} /2 = 9 kV-10 kV). The 15 kV SiC IGBT device nominal operating voltage is 10 kV, therefore, the total dc bus voltage has to be 18 kV to 20 kV to make the voltage across the device nearly 9 kV to 10 kV.

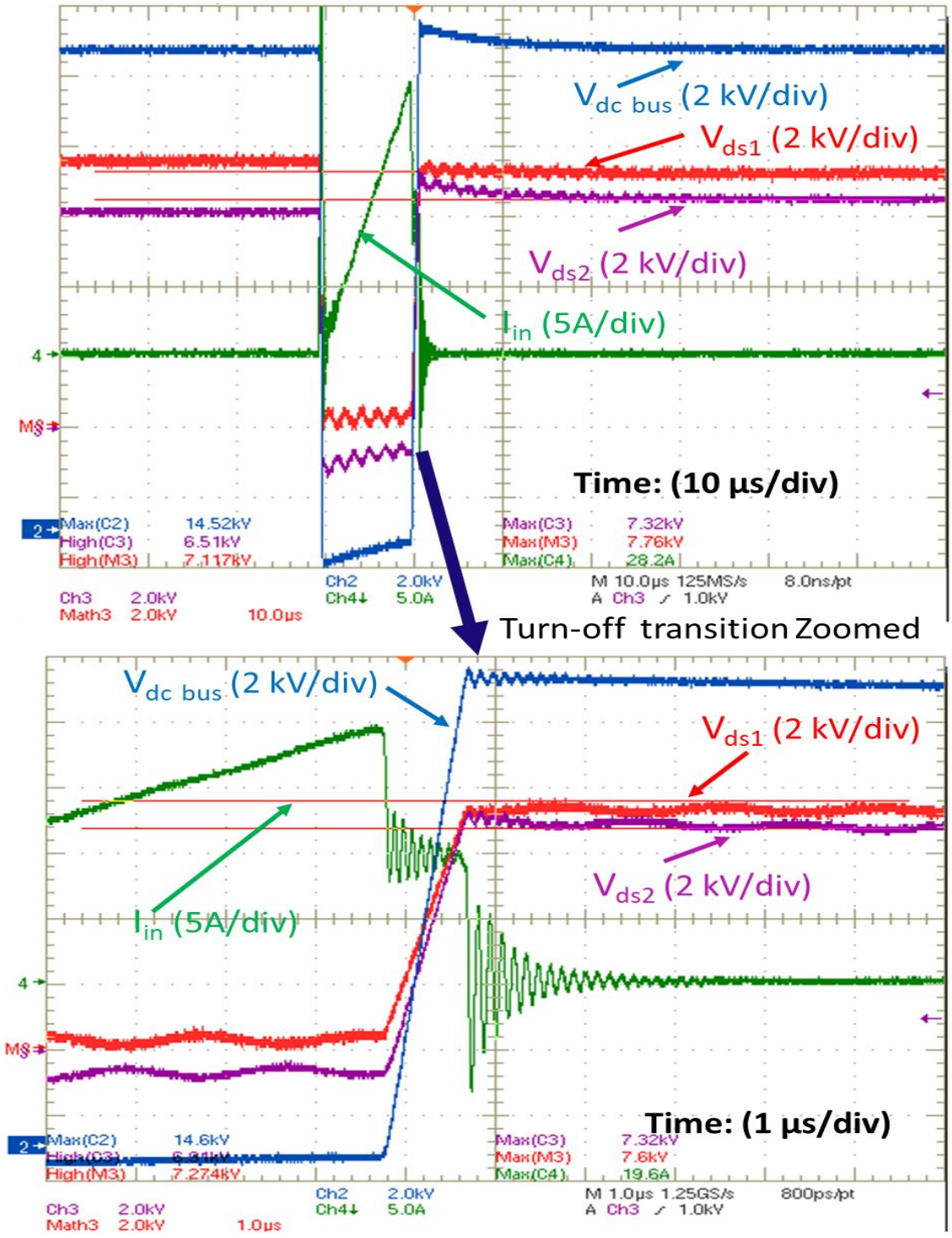


Fig. 5-33: Dynamic voltage sharing between two 15 kV SiC MOSFET devices at 14 kV dc bus voltage with external snubber (C_dR_s :1.1 nF, 20 MΩ), and dv/dt (8.5 kV/µs) of each device. [Ch2 (Blue): Total dc bus voltage V_{dcbus}; Ch3 (Magenta): Bottom device V_{ds2}; Ch4 (Green): Input current from DC bus I_{in}; Math3 (Red): Ch2-Ch3: Top device V_{ds1}]

Table 5-16: Summary of dynamic voltage imbalance between two 15 kV SiC MOSFET devices at different dc bus voltages and switching currents, with snubber value (C_dR_s): 1.1 nF, 20 MΩ, T_j=125^{0}C

DC bus voltage, switching current	Voltage imbalance between two SiC MOSFETs	DC bus voltage, switching current	Voltage imbalance between two SiC MOSFETs	DC bus voltage, switching current	Voltage imbalance between two SiC MOSFETs
12 kV, 10 A	525 V	12 kV, 15A	530 V	12 kV, 20 A	600 V
13 kV, 10 A	525 V	13 kV, 15 A	530 V	13 kV, 20 A	600 V
14 kV, 10 A	525 V	14 kV, 15 A	530 V	14 kV, 20 A	600 V

Table 5-17: Summary of dynamic voltage imbalance between two 15 kV SiC MOSFET devices at different dc bus voltages and switching currents, with snubber value (C_dR_s): 0.5 nF, 20 MΩ, T_j=25^{0}C

DC bus voltage, switching current	Voltage imbalance between two SiC MOSFETs	DC bus voltage, switching current	Voltage imbalance between two SiC MOSFETs	DC bus voltage, switching current	Voltage imbalance between two SiC MOSFETs
10 kV, 10 A	800 V	10 kV, 15 A	880 V	12 kV, 20 A	1000 V
12 kV, 10 A	800 V	12 kV, 15 A	880 V	13 kV, 20 A	1000 V
13 kV, 10 A	830 V	13 kV, 15 A	880 V	14 kV, 20 A	1000 V

The dynamic voltage balancing is also tested at T_j =25^{0}C with snubber value (C_dR_s): 1.1 nF, 20 MΩ, T_j=25^{0}C. The difference in the dynamic voltage imbalance voltage at 25^{0}C case is nearly equal to 125^{0}C case. Therefore, the increase in the voltage imbalance between the two 15 kV SiC MOSFET devices with an increase in temperature is negligible. This indicates that there is a strong matching between the two selected SiC MOSFET devices.

The dynamic voltage test on two series connected SiC MOSFET devices have been conducted at different snubber values 0.5 nF, 20 MΩ and T_j=25^{0}C. The summary of voltage imbalance between the two devices at different DC bus voltages and switching currents is shown in Table 5-17. The voltage imbalance between two devices is increased nearly **1.5 times** with 0.5 nF, 20 MΩ snubber values compared to 1.1 nF, 20 MΩ snubber values. However, the dynamic voltage imbalance between the two devices is still less than 10% of the rated device operating voltage. Table 5-18 shows the summary of snubber values (C_d, R_s) required for series connection 15 kV SiC devices.

Table 5-18: Summary of Snubber values required to enable series connection in HV SiC devices

Devices used for series connection	Snubber Capacitor (C_d)	Snubber Resistor (R_s)	% Static and dynamic voltage imbalance	Device Turn-off dv/dt at 7 kV across each and 20 A switching
15 kV SiC IGBT (2 µm buffer layer)	2.2 nF	10 -20 M Ω	10-12%	4.2 kV/µs
15 kV SiC IGBT (5 µm buffer layer)	1.1 nF	5 -10 M Ω	10-12%	6 kV/µs
15 kV SiC MOSFET	0.5 nF	20 M Ω	10-12%	16 kV/µs

5.4.4 Series connection of 10 kV SiC MOSFET devices

This section briefly presents series connection of 10 kV SiC MOSFET characterization. The experimental static and dynamic tests have been performed with two 10 kV SiC MOSFET devices in series, without external snubber (C_d R_s) across the device. The difference in static voltage sharing at 11 kV DC bus is 800 V as shown in Fig. 5-34 and the difference in dynamic voltage sharing is 800 V at 6 kV DC bus as shown in. It also shows that the overall *dv/dt* due to two 10 kV SiC MOSFETs is more than 50 kV/µs.

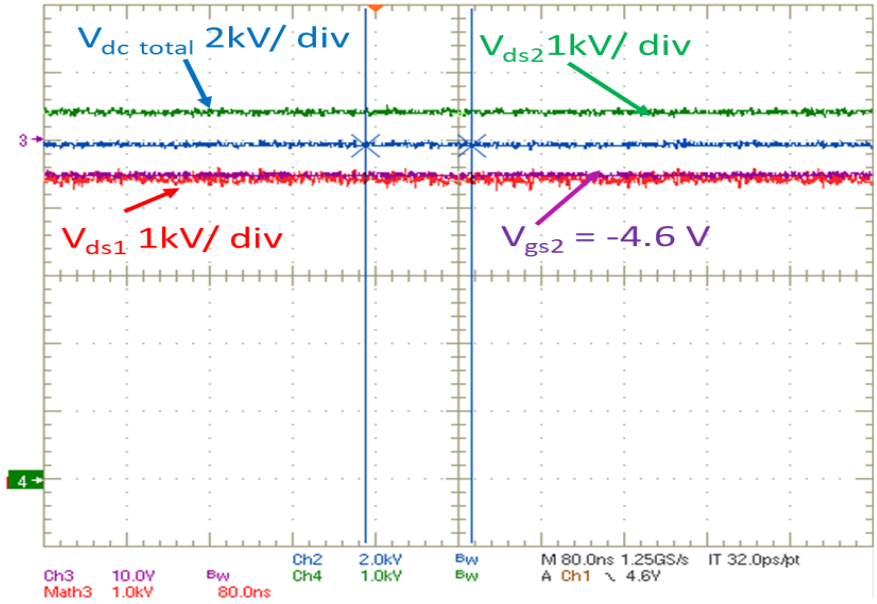


Fig. 5-34: Static voltage sharing between two 10 kV SiC MOSFETs during blocking mode at 10 kV DC bus voltage without external static balancing resistance (R_s) and at T_j=25^{0}C

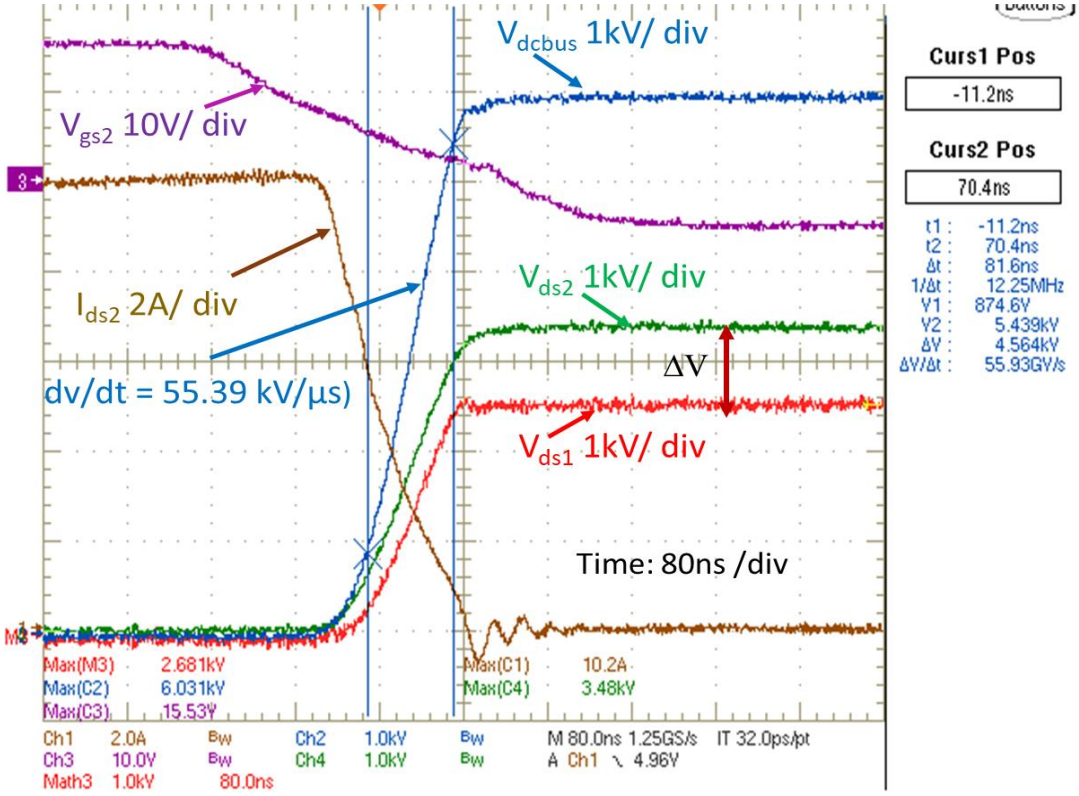


Fig. 5-35: Dynamic voltage sharing between two 10 kV SiC MOSFETs (a) at 6 kV dc bus voltage, T_j:25^{0}C [Magenta: Bottom device V_{gs2} (10 V/div); Blue: Total voltage (1 kV/div); Green: Bottom device V_{ds2} (1 kV/div); Red: Top device V_{ds1} (1 kV/div); Brown: Bottom device current: I_{ds2} (2 A/div)]

The difference in static voltage sharing is further minimized with paralleling resistor R_s =20 MΩ to 40 MΩ. The dynamic voltage balancing and 'dv/dt' during turn-off is achieved with snubber capacitor (C_d). The snubber (2.2 nF, 20 MΩ) limits device maximum $[dv/dt]_{max}$ to less than 5 kV/µs. The Fig. 5-36 shows the balanced dynamic voltage sharing between two series connected 10 kV SiC MOSFETs during turn-off transition with nearly zero voltage imbalance using snubber.

Therefore, similar to 15 kV SiC MOSFET series connection case, a small external snubber capacitor and static balancing resistor across the 10 kV SiC MOSFET will enable series connection with the voltage imbalance across the devices less than 10-12% of the rated nominal voltage of the device and also a significant reduction in *dv/dt*.

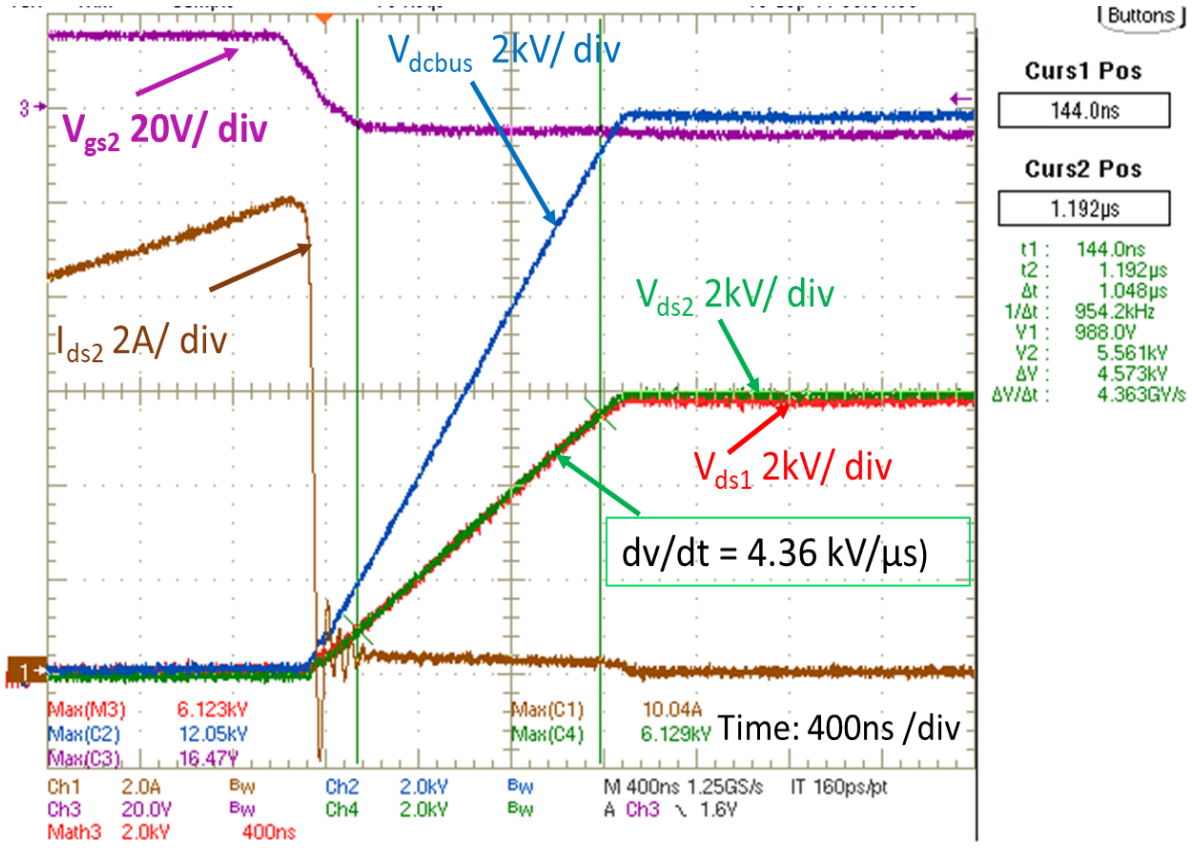


Fig. 5-36: Balanced dynamic voltage sharing between two 10 kV SiC MOSFETs (Gen-I) 12 kV DC bus voltage with snubber, T_j:25^{0}C [Magenta: Bottom device V_{gs2} (20 V/div); Blue: Total voltage (2 kV/div); Green: Bottom device V_{ds2} (2 kV/div); Red: Top device V_{ds1} (2 kV/div); Brown: Bottom device current: I_{ds2} (2 A/div)]

5.5 Power loss and efficiency evaluation of Dual active bridge (DAB) using SiC and Si devices for DC-DC Transformer application

This section presents the performance evaluation for two types of basic building block configurations of Dual active bridge (DAB) converter (as in Fig. 1-7 (a), Fig. 1-7-(c)). The DAB building blocks (type I & III) are shown again in Fig. 5-37 and Fig. 5-38 for easy reference. These building blocks transfer the power at high voltage step-up/down conversion ratios. The power loss and efficiency of these two types of DAB converters are evaluated using the loss data from previous sections in PLECS software. Table 5-19 and Table 5-20 show the device power losses of the DAB converter (on HV side and LV side of Type-I DAB) and converter efficiency for 100 kW input power, 5 kHz switching frequency, HV side Voltage (V_{HV}) =9 kV, LV side voltage (V_{LV}) =900 V. Table 5-19 and Table 5-20 also show the different combination of devices used in HV side and LV side of DAB (type-I)

converter. Comparing Table 5-19 to Table 5-20, the converter efficiency is more if 1.7 kV SiC MOSFETs are used on both sides (HV and LV side) of DAB converter compared to other cases.

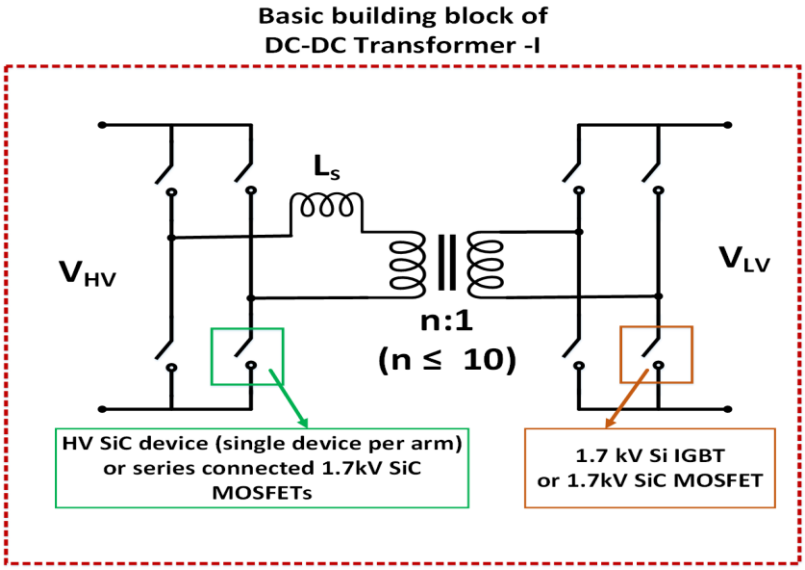


Fig. 5-37: Dual active bridge converter (Type-I)

Table 5-19: Power loss and efficiency comparison of DAB converter (Type-I) using SiC devices in HV side and Si IGBT devices on LV side for 100 kW, f_{sw}= 5 kHz, V_{HV} =9 kV, V_{LV}= 900 V

HV side device	LV side device	HV side (P_{sw}) per device	HV side (P_{cond}) per device	LV side (P_{sw}) per device	LV side (P_{cond}) per device	Converter Efficiency
15 kV SiC IGBT (2µm) single module per arm with snubber	1.7 kV Si IGBT single module per arm	237.43	50.57	257.67	121.8	97.3301
15 kV SiC IGBT (5µm) single module per arm with snubber	1.7 kV Si IGBT single module per arm	154.53	39.96	257.67	121.8	97.7042
15 kV SiC MOSFET single module per arm with snubber	1.7 kV Si IGBT single module per arm	0	156.969	257.67	121.8	97.8542
Nine series connected 1.7 kV SiC MOSFETs per arm with snubber	1.7 kV Si IGBT single module per arm	0.6977	1.3472	257.21	122.1	98.4337

Table 5-20: Power loss and efficiency comparison of DAB converter (Type-I) using SiC devices in HV side and 1.7 kV SiC MOSFET on LV side for 100 kW, f_{sw}= 5 kHz, V_{HV} =9 kV, V_{LV}= 900 V

HV side device	LV side device	HV side (P_{sw}) per device	HV side (P_{cond}) per device	LV side (P_{sw}) per device	LV side (P_{cond}) per device	Converter Efficiency
15 kV SiC IGBT (5um) single module per arm with snubber	1.7 kV SiC MOSFET single module per arm	154.53	39.96	28.6	69.97	98.8278
15 kV SiC MOSFET single module per arm with snubber	1.7 kV SiC MOSFET single module per arm	0	158.012	28.6	69.989	98.8304
Nine series connected 1.7 kV SiC MOSFETs per arm with snubber	1.7 kV SiC MOSFET single module per arm	0.6977	1.3472	28.55	72.187	99.5480

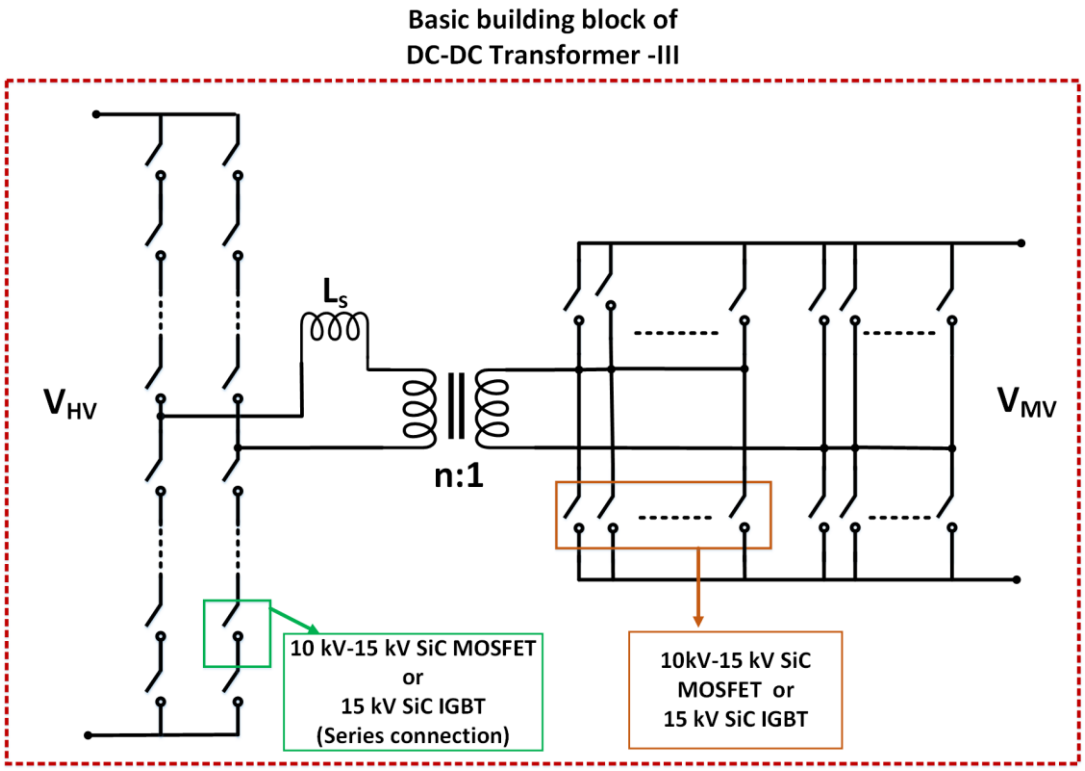


Fig. 5-38: Dual active bridge converter (Type-III)

To interconnect HVDC to MVDC, series connection on HV side can also be used as shown in Fig. 5-38. Table 5-21 shows the device power losses of the DAB converter (on HV side and LV side of Type-III DAB) and converter efficiency for 750 kW input power, 5 kHz switching frequency, HV side Voltage (V_{HV}) =60 kV, LV side voltage (V_{LV}) =10 kV. Comparing Table 5-19 to Table 5-21, the converter is efficiency is more if SiC devices are used on both sides (HV and LV side) of DAB

converter. Among the all SiC devices, SiC MOSFETs (10-15 kV SiC MOSFETs and series connected 1.7 kV SiC MOSFETs) give more efficiency compared to SiC IGBTs for soft switching converter like DAB.

Table 5-21: Power loss and efficiency comparison of DAB converter(Type-III) using HV SiC devices on both HV side and LV side for 750 kW, f_{sw}= 5 kHz, V_{HV} =60 kV, V_{LV}= 10 kV

HV side device	LV side device	HV side (P_{sw}) per device	HV side (P_{cond}) per device	LV side (P_{sw}) per device	LV side (P_{cond}) per device	Converter Efficiency
Six series connected 15 kV SiC IGBTs (5 µm buffer layer) per arm with snubber	Eight parallel 15 kV SiC IGBTs (5 µm buffer layer) per arm with snubber	200.893	48.9577	142.24	71.977	98.2865
Six series connected 15 kV SiC IGBTs (5 µm buffer layer) per arm with snubber	Eight parallel 15 kV SiC MOSFETs per arm with snubber	200.86	47.99	0	51.489	98.9840
Six series connected 15 kV SiC MOSFETs per arm with snubber	Eight parallel 15 kV SiC MOSFETs per arm with snubber	0	204.125	0	51.489	99.1271

5.6 Conclusions

- This chapter enables the operation of Punch through (PT) devices (15 kV SiC IGBTs) for high voltage and high power at extremely low *dv/dt* using small external snubber capacitor. It showed that a low-cost small snubber capacitor across the device makes Punch through (PT) devices behave like non punch-through (NPT) devices and it significantly reduces the *dv/dt* and also the turn-off losses without increasing the thickness of epitaxial drift layer of 15 kV SiC IGBT which leads to significant reduction in size and cost of the HV SiC IGBT device.
- The experimental ZVS characterization of 15 kV SiC IGBT for both 2µm and 5 µm buffer layer devices have been evaluated.
- The experimental demonstration of half-bridge ZVS converter with and without snubber using 15 kV/40 A modules at 7 kV DC bus, 8.2 A switching current and 5 kHz switching frequency has been reported. The **switching frequency** of 15 kV IGBT in ZVS based converter is **3-4 times higher** than in a hard switching converter for the same junction

temperature. Also, there is **nearly five times reduction** in transformer parasitic capacitive current in a DAB converter using 5 µm buffer layer SiC IGBT with snubber as compared to the case without a snubber.

- Series connection of HV SiC devices has been evaluated with external snubber for four separate independent cases: (i) series connection of two 15 kV SiC IGBTs (single die per module) (2 µm buffer layer) devices;

  (ii) the series connection of two 15 kV SiC IGBTs (two parallel dies per module) (5 µm buffer layer) devices;

  (iii) the series connection of two 15 kV SiC MOSFETs (two parallel dies per module);

  (iv) the series connection of two 10 kV SiC MOSFET (single die per module, Gen-I).
- The series connection of HV SiC devices will enable DC-DC soft switching converter such as DAB converter for HVDC to MVDC or MVDC to LVDC applications with **efficiency greater than 98%.**

Chapter 6 Conclusions

This dissertation focuses on the impact of series connected LV SiC MOSFET devices (such as 1.7 kV SiC MOSFET devices) and the recently developed HV SiC devices: 10 kV SiC MOSFET, 15 kV SiC IGBT, 15 kV SiC MOSFET on medium voltage (MV) converters to enable (i) MV high –speed motor drive applications; and (ii) HVDC-MVDC or MVDC-LVDC interconnection for DC grid applications. This section summarizes the main contributions of the thesis:

In Chapter 2, a series connection of low voltage SiC MOSFETs (1.7 kV SiC MOSFETs) with RC snubber investigated. Design criteria for selection of RC snubber for series connection is explained and a methodology to find optimal RC snubber for series connection using experimental characterization is presented. From the dynamic voltage characterization experiments it is found that lower limit of optimal snubber capacitor value is $C_d \geq 33$ nF. From the switching loss characterization, the upper limit for optimal resistor value $R_d \leq 4.7\ \Omega$. Measuring the switching loss per device in series connection of 'n' device with RC snubber is not feasible. Therefore, introduced a characterization circuit set-up to measure true switching losses per device and also its validation. Analytical expressions to determine the rating of snubber resistor and snubber resistor losses is presented. In addition, different configuration of converters (Full bridge, half-bridge, DC-DC phase-leg) have been demonstrated using series 1.7 kV SiC MOSFET devices in continuous switching mode at different operating conditions to showcase (i) the voltage imbalance is within the safe operating limit with increase in junction temperature, (ii) enabling MV/HV converter with switching frequencies up to 8 kHz for high-speed drives or grid-connected applications. It is shown that the series connection of 1.7 kV SiC MOSFETs will enable a simple two-level MV converter for high-speed MV motor drive applications with higher switching frequencies (up to 7.5 kHz), and fundamental frequencies (up to 500 Hz). Comparison of Si IGBT with series connected 1.7 kV SiC MOSFETs is presented. The series connection of four 1.7 kV SiC MOSFETs has significantly lower total loss compared to single 6.5 kV Si IGBT for the same current rating and for switching frequencies (f_{sw}) > 1 kHz. The estimated **powered density of** VSD section (both front-end and VSI) is **2.38 MW/m^3**, which is much higher than the "DOE" specifications of next generation high- speed drives **0.66 MW/m^3**.

In Chapter 3, detailed characterization of 15 kV SiC MOSFET is provided. Two different switching characterization circuits were considered and explained difference in switching loss data from these two setups. The importance of using correct switching characterization setup circuit is discussed to analyze the efficiencies of different hard switching converter topologies. Effect of crosstalk and

partial shoot through in a phase leg converter using in 15 kV SiC MOSFET is discussed and presented the selection of gate resistances to mitigate crosstalk. Demonstration of DC-DC boost converter using 15 kV SiC MOSFET at different operating conditions is presented. A method to compare HV SiC devices (15 kV SiC MOSFET and 15 kV SiC IGBT) is introduced and explained its importance from the point of power electronic converter design. Total loss of 15 kV SiC MOSFET module (two parallel dies per module) and 15 kV SiC IGBT module (single die and two parallel dies) is compared. This data will be useful for power converter designer to analyze the efficiency of different converter topologies. The switching frequency limits of 15 kV SiC MOSFET (two dies per modules), 15 kV SiC IGBT (single die per module) and 15 kV SiC IGBT (two dies per module) have been determined.

The experimental characterized data showed that for switching frequency < 4 kHz, the 15 kV SiC IGBT (single die per module) has a lower total loss compared to 15 kV SiC MOSFET(two dies per module) for the duty ratio of 0.5, at 10 kV dc bus and at same *dv/dt* values. Similarly, for switching frequency < 6.5 kHz, the 15 kV SiC IGBT(single die per module) has a lower total loss compared to 15 kV SiC MOSFET(two dies per module) for the duty ratio of 0.8, at 10 kV dc bus and at same *dv/dt* values.

For DC bus voltage of 8 kV, the 15 kV SiC MOSFET (two parallel dies per module) has a lower total loss and higher efficiency than the 15 kV SiC IGBT (two parallel dies per module) for any current, switching frequency and at same gate resistance values.

In Chapter 4, the HV SiC modules (10 kV SiC MOSFET, 15 kV SiC MOSFET, 15 kV SiC IGBT) with series connected 1.7 kV SiC MOSFETs are compared. This comparison is applicable for hard switching converter applications. It concludes that (i) the junction to case temperature rise is more in the equivalent 10-15 kV /150 A SiC modules for a given switching frequency compared to the series connection of 1.7 kV SiC MOSFET devices. The packaging thermal resistance is limiting the performance of HV SiC modules. Total losses of equivalent 10 kV/150 A SiC MOSFET modules (using either 1st or 3rd gen dies) are less compared to that of series connected 1.7 kV SiC MOSFET devices for 5.4 kV/150 A. For switching frequency less than 6.5 kHz and at duty ratio of 0.8, equivalent 15 kV/ 150 A SiC IGBT is more efficient compared to equivalent 15 kV/ 150 A SiC MOSFET modules and series connected 1.7 kV SiC MOSFETs. For switching frequency greater than 6.5 kHz, equivalent 15 kV/ 150 A SiC MOSFET modules are more efficient for 10 kV/150A operations compared to other two cases. However, the 10-15 kV SiC modules are not available commercially due to cost or other reasons at present. Therefore the series connection of LV SiC MOSFETs will provide an alternate method for enabling MV converter for high-speed drives or grid

connected converters applications. Also, the total loss of series connected 1.7 kV SiC MOSFET devices is 3 to 6 times lower compared to 3.3 kV Si-IGBT and 6.5 kV Si-IGBT for 5 kHz switching frequency.

Chapter 5 explained that design and operation of high voltage high power converters using HV SiC device is extremely difficult due to high *dv/dt*. This chapter investigated (i) the soft switching of HV SiC devices and (ii) series connection of HV SiC devices to enable the operation of these devices in DC-DC soft switching converters (such as DAB) for high voltage and high power application at extremely low *dv/dt* values using small external snubber capacitor. It showed that a low-cost small snubber capacitor across the device makes punch-through (PT) devices (15 kV SiC IGBT) behave like non-punch-through (NPT) devices and it significantly reduces the *dv/dt* and also the turn-off losses without increasing the thickness of epitaxial drift layer of 15 kV SiC IGBT which leads to significant reduction in size and cost of the HV SiC device. Experimental ZVS characterization of 15 kV SiC IGBT for both 2 μm and 5 μm buffer layer devices have been evaluated to show the reduction in *dv/dt* and switching losses. The experimental demonstration of DC-AC half-bridge ZVS converter with and without snubber using 15 kV/40 A modules at 7 kV DC bus, 8.2 A switching current and 5 kHz switching frequency is presented. The **switching frequency** of 15 kV/40 A SiC IGBT in ZVS based converter is **3-4 times higher** than in a hard switching converter for the same junction temperature. Also, there is a **nearly five times reduction** in transformer parasitic capacitive current in a DAB converter using 5 μm 15 kV/40 A SiC IGBT with snubber as compared to the case without snubber case.

Series connection of HV SiC devices has been evaluated with external snubber for four separate independent cases: (i) series connection of two 15 kV SiC IGBTs (single die per module) (2 μm buffer layer) devices; (ii) series connection of two 15 kV SiC IGBTs (two parallel dies per module) (5 μm buffer layer) devices; (iii) series connection of two 15 kV SiC MOSFETs (two parallel dies per module); (iv) series connection of two 10 kV SiC MOSFETs (single die per module, Gen-I) devices. Detailed experimental results are presented, to show the static and dynamic voltage sharing behavior of two series connected HV SiC devices with different snubber values and at different junction temperatures. The experimental characterization results show that a small external snubber capacitor and static balancing resistor across the HV SiC device will enable series connection with voltage imbalance across the devices less than 10-12% of the rated nominal operating voltage of the device. Also, the series connection with small snubber will give a significant reduction in '*dv/dt*' and turn-off losses to enable the design, operation of high power density MV DC-DC transformers or DC-DC soft switching converters. Power loss and efficiency of DC-DC soft switching converter (DAB) are

calculated using a different combination of SiC and Si devices. Among the all SiC devices, SiC MOSFETs (10-15 kV SiC MOSFETs and series connected 1.7 kV SiC MOSFETs) give more efficiency (> 99 %) compared to 15 kV SiC IGBTs for soft switching converter like DAB.

REFERENCES

[1] DE-FOA-0001208: Department of Energy (DOE) Office of Energy Efficiency and Renewable Energy (EERE)-Next Generation Electric Machines: Megawatt Class Motors, 2015, pp.1-88. Available at: ”https://energy.gov/eere/amo/next-generation-electric-machines.”

[2] R. Abebe, M. Di Nardo, D. Gerada, G. L. Calzo, L. Papini and C. Gerada, "High speed drives review: Machines, converters and applications," IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society, Florence, 2016, pp. 1675-1679.

[3] R. Teodorescu, F. Blaabjerg, J. K. Pedersen, E. Cengelci, and P. N. Enjeti,“Multilevel inverter by cascading industrial VSI,” IEEE Trans. Ind.Electron., Vol. 49, no. 4, pp. 832-838, Aug. 2002.

[4] D. Jiang, J. Xue, F. Wang and M. H. Kao, "High density Modular Multilevel Cascade Converter for medium-voltage motor drive," 2011 IEEE Electric Ship Technologies Symposium, Alexandria, VA, 2011, pp. 482-485.

[5] J.W.Palmour et al.,“Silicon Carbide Power MOSFETs breakthrough performance from 900 V up to 15 kV”, International Symposium onPower Semiconductor Devices & IC's (ISPD), 2014, pp.79-82.

[6] Vipindas Pala et al.,” 10 kV and 15 kV Silicon Carbide Power MOSFETs for Next -Generation Energy Conversion and Transmission Systems” Proc. IEEE ECCE, 2014, pp. 449-454.

[7] Kadavelugu, Arun; Bhattacharya, Subhashish; Ryu, Sei-Hyung; Van Brunt, Edward; Grider, David; Agarwal, Anant; Leslie, Scott; Characterization of 15 kV SiC n-IGBT and its application considerations for high power convertersEnergy Conversion Congress and Exposition (ECCE), 2013, pp. 2528-2535.

[8] Sachin Madhusoodhanan, et al.,"Medium Voltage (>= 2.3 kV) High Frequency Three-Phase Two-Level Converter Design and Demonstration Using 10 kV SiC MOSFETs for High Speed Motor Drive Applications", APEC, 2016 IEEE.

[9] B. Passmore et al., "The next generation of high voltage (10 kV) silicon carbide power modules," 2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Fayetteville, AR, 2016, pp.1-4.

[10] Vestas. V90-3.0 MW. Technical report, Vestas, 2009.

[11] AREVA Wind GmbH. M5000 wind turbine, 2012. Available online at http: //www.areva-wind.com.

[12] S. Lundberg. Wind Farm Configuration and Energy Efficiency Studies - Series DC versus AC Layouts. PhD thesis, Chalmers University of Technology, 2006.

[13] L. Max and S. Lundberg, "System efficiency of a DC/DC converter based wind turbine grid system," Nordic Wind Energy Conference, Espoo, Finland, 22-23 May, 2006.

[14] J. Robinson; D. Jovcic; G. Joos."Analysis and Design of an Offshore Wind Farm Using a MV DC Grid" IEEE Transactions on Power Delivery Year: 2010, Volume: 25, Issue: 4 Pages: 2164 – 2173.

[15] M. A. Bahmani, "Design and Optimization of hf transformers for high power dc-dc applications," Licentiate Thesis, Chalmers Univ. Technol., Gothenburg, Sweden, Apr. 2014.

[16] M. A. Bahmani, T. Thiringer, A. Rabiei and T. Abdulahovic, "Comparative Study of a Multi-MW High-Power Density DC Transformer With an Optimized High-Frequency Magnetics in All-DC Offshore Wind Farm," inIEEE Transactions on Power Delivery, vol. 31, no. 2, pp. 857-866, April 2016.

[17] Hualong Yu, Liqiang Yuan, Ting Lu, Zhengming Zhao and Shiqi Ji, "Structure design and analysis of high voltage IGBTs series connection experimental platform," Proceedings of The 7th International Power Electronics and Motion Control Conference, Harbin, China, 2012, pp. 1828-1832.

[18] Bolotnikov, A et al,"Overview of 1.2kV– 2kV SiC MOSFETs targeted for industrial power conversion applications" IEEE APEC, 2015, pp.2445-2452.

[19] Xinke Wu, et al ,"A 3600V/80 A Series–Parallel-Connected Silicon Carbide MOSFETs Module With a Single External Gate Driver" IEEE Transaction on Power Electronics, 2014, pp.2296-2306.

[20] Qiang Xiao, et al,"10kV/200A SiC MOSFET Module with Series-Parallel Hybrid Connection" ISPSD,2014,pp.349-352.

[21] J. Sigg, M. Bruckmann and P. Turkes, "The series connection of IGBTs investigated by experiments and simulation," PESC Record. 27th Annual IEEE Power Electronics Specialists Conference, Baveno, 1996, pp. 1760-1765 vol.2.

[22] Jiann-Fuh Chen, Jiunn-Nan Lin, Tsu-Hua Ai. "The Techniques of The Serial and Paralleled IGBTs". IECON IEEE 22nd International Conference, 1996, Vol.5~10, 999~1004.

[23] R. Withanage and N. Shammas, "Series Connection of Insulated Gate Bipolar Transistors (IGBTs)," in IEEE Transactions on Power Electronics, vol. 27, no. 4, pp. 2204-2212, April 2012.

[24] Kasunaidu Vechalapu, et al., "Performance evaluation of series connected 1700V SiC MOSFET devices", Wide Bandgap Power Devices and Applications (WiPDA), 2015 IEEE, pp. 184-194.

[25] Nagel, A.; Bernet, S. ; Bruckner, T. ; Steimer, P.K. ; Apeldoorn, O. "Characterization of

IGCTs for series connected operation", IEEE Industry Applications Conference, 2000, pp.1923-1929.

[26] Subhashish Bhattacharya, "Comparative evaluation of IGCT and GTO thyristor for series connection of high power voltage source inverter based FACTS applications", Power Electronics and Applications, 2007, pp.1-7.

[27] Consoli, A., Musumeci, S., Oriti, G., and Testa, A.: 'Active voltage balancement of series-connected IGBTs.' Conference Record of the Industry Applications Conf., 8–12 Oct 1995, Vol. 3, pp. 2752–2758.

[28] N. Y. A. Shammas, R. Withanage, and D. Chamud, "Review of series and parallel connection of IGBTs," IEEE Proc. Circuit, Devices Syst., vol. 153, no. 1, pp. 34–39, Feb. 2006.

[29] T. C. Lim, B. W. Williams, S. J. Finney and P. R. Palmer, "Series-Connected IGBTs Using Active Voltage Control Technique," in IEEE Transactions on Power Electronics, vol. 28, no. 8, pp. 4083-4103, Aug. 2013.

[30] B. J. Baliga, Power Semiconductor Devices. Boston, MA: PWS-Kent, 1996.

[31] Datasheet: CAS300M17BM2, available at " http://www.wolfspeed.com/cas300m17bm2".

[32] W. McMurray, "Selection of Snubbers and Clamps to Optimize the Design of Transistor Switching Converters," in IEEE Transactions on Industry Applications, vol. IA-16, no. 4, pp. 513-523, July 1980.

[33] W. McMurray, "Optimum Snubbers for Power Semiconductors," in IEEE Transactions on Industry Applications, vol. IA-8, no. 5, pp. 593-600, Sept. 1972.

[34] B. N. Torsæter, S. Tiwari, R. Lund and O. M. Midtgård, "Experimental evaluation of switching characteristics, switching losses and snubber design for a full SiC half-bridge power module," 2016 IEEE 7th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Vancouver, BC, 2016, pp. 1-8.

[35] Datasheet of ABB 6.5kV Si IGBT : 5SNA 0400J6501.

[36] Mrinal K. Das et al," 10 kV, 120 A SiC Half H-Bridge Power MOSFET Modules Suitable for High Frequency, Medium VoltageApplications" Energy Conversion Congress and Exposition (ECCE), 2011 IEEE.

[37] Kadavelugu, A. et al.,"Characterization of 15 kV SiC n-IGBT and its application considerations for high power converters" Energy Conversion Congress and Exposition (ECCE), 2013 IEEE,pp.2528-2535.

[38] Kadavelugu, A. et al.," Experimental switching frequency limits of 15 kV SiC N-IGBT module", Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE-ASIA), 2014, pp. 3726-3733.

[39] A. Kadavelugu *et al*., "Medium voltage power converter design and demonstration using 15 kV SiC N-IGBTs," 2015 IEEE Applied Power Electronics Conference and Exposition (APEC), Charlotte, NC, 2015, pp. 1396-1403

[40] Lixing Fu et al.,"The Development of A High-Voltage Power Device Evaluation Platform", Wide Bandgap Power Devices and Applications (WiPDA), 2014, pp.13-17.

[41] E. Van Brunt et al., "27 kV, 20 A 4H-SiC n -IGBTs" , 2014, ECSCRM, vol. 821, pp. 847-850.

[42] Mainali, K et al., " A Transformerless Intelligent Power Substation: A three -phase SST enabled by a 15-kV SiC IGBT" Power Electronics Magazine, IEEE, 2015, vol. 2, pp. 31-43.

[43] Mirzaee, H. et al.,"Design comparison of high power medium-voltage converters based on 6.5kV Si-IGBT/Si-PiN diode, 6.5kV Si-IGBT/SiC-JBS diode, and 10kV SiC MOSFET/SiC-JBS diode", Energy Conversion Congress and Exposition (ECCE), 2011 IEEE, pp. 2421 – 2428.

[44] Madhusoodhanan, S. et al., "Solid -State Transformer and MV Grid Tie Applications Enabled by 15 kV SiC IGBTs and 10 kV SiC MOSFETs Based Multilevel Converters" IEEE Trans. Ind. Appl.,2015, vol. 51, pp. 3343 – 3360.

[45] Vechalapu, K ; Kadavelugu, A.K.; Bhattacharya, S. "High voltage dual active bridge with series connected high voltage silicon carbide (SiC) devices" Energy Conversion Congress and Exposition (ECCE), 2014 IEEE, pp. 2057 – 2064.

[46] Woongje Sung; Jun Wang; Alex Q. Huang; B. Jayant Baliga , "Design and investigation of frequency capability of 15kV 4H-SiC IGBT," IEEE Int 'l Symposium on Power Semiconductor Devices and IC's (ISPSD), 2009, pp. 271-274.

[47] Z. Zhang; W. Zhang; F. Wang; L. M. Tolbert; B. J. Blalock, "Analysis of the switching speed limitation of wide band-gap devices in a phase-leg configuration," in Proc. IEEE Energy Conversion Congress and Exposition, Sept. 2012, pp. 3950-3955.

[48] Kadavelugu A;Bhattacharya, S "Design considerations and development of gate driver for 15 kV SiC IGBT" Applied Power Electronics Conference and Exposition (APEC), 2014, IEEE, pp. 1494 – 1501.

[49] Gangyao Wang; Alex Huang; Chushan Li, "ZVS range extension of 10A 15kV SiC MOSFET based 20kW Dual Active Half Bridge (DHB) DC-DC converter", Energy Conversion Congress and Exposition (ECCE), 2012 IEEE, pp. 1533 – 1539.

[50] S. Xu; W. Sun; D. Sun, "Analysis and design optimization of brushless DC motor's driving

circuit considering the Cdv/dt induced effect," in Proc. IEEE Energy Conversion Congress and Exposition 2010, 12-16 Sept. 2010, pp. 2091-2095.

[51] R. K. Burra; S.K. Mazumder; R. Huang, "DV/DT related spurious gate turn-on of bidirectional switches in a high-frequency cycloconverter," in IEEE Trans. Power Electronics, vol. 20, no. 6, Nov. 2005, pp. 1237-1243.

[52] T. Wu, "Cdv/dt induced turn-on in synchronous buck regulations," Tech. Rep., International Rectifier, 2007 [Online]. Available: http://www.irf.com/.

[53] A. Elbanhawy, "MOSFET susceptibility to cross conduction," in Proc. Power Electron. Technol., Apr. 2005, pp. 26-33.

[54] Fairchild Semiconductor AN-7019, "Limiting Cross-Conduction Current in Synchronous Buck Converter Designs," http://www.fairchildsemi.com/an/AN/AN-7019.pdf#page=1.

[55] Zheyu Zhang; Fred Wang; Leon M. Tolbert; Benjamin J. Blalock,"A novel gate assist circuit for cross talk mitigation of SiC power devices in a phase-leg configuration", Applied Power Electronics Conference and Exposition (APEC), 2013 IEEE, pp.1259 – 1265.

[56] Mrinal K. Das et al," 10 kV, 120 A SiC Half H-Bridge Power MOSFET Modules Suitable for High Frequency, Medium Voltage Applications" Energy Conversion Congress and Exposition (ECCE), 2011 IEEE, pp. 2689 – 2692

[57] Datasheet of Extruded Heat Sinks, Wakefield Engineering, part no.392-300AB.

[58] IGBT Power Losses Calculation Using the Data-Sheet ParametersApplication Note, V 1.1, January 2009

[59] S. Madhusoodhanan; K. Mainali; A. Tripathi; A. Kadavelugu; D. Patel; S. Bhattacharya, "Thermal design considerations for medium voltage power converters with 15 kV SiC IGBTs Power Electronics for Distributed Generation Systems (PEDG), 2015 IEEE,

pp.1-8.

[60] IGBT Power Losses Calculation Using the Data-Sheet ParametersApplication Note, V 1.1, January 2009.

[61] Arun Kadavelugu et al, “Zero Voltage Switching Characterization of 12 kV SiC” Power Semiconductor Devices & IC's (ISPSD), 2014 IEEE 26th International Symposium.

[62] Arun Kadavelugu et al, “Understanding dv/dt of 15 kV SiC N-IGBT and its control using active gate driver”, Energy Conversion Congress and Exposition (ECCE), 2014 IEEE.

[63] A. Tripathi *et al*., "Grid connected CM noise considerations of a three-phase multi-stage SST," *2015* 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia), Seoul, 2015, pp. 793-800.

[64] Krishna Mainali et al,” Design, Measurement and Equivalent Circuit Synthesis of High Power HF Transformer for Three-Phase Composite Dual Active BridgeTopology”, APEC, 2014, pp. 342-349.

[65] Datasheet of Extruded Heat Sinks, Wakefield Engineering, part no. 392-180AB.

APPENDIX

This chapter lists expressions of snubber current for different scenarios listed in chapter 2.6.1.

The solution for the snubber current '$i_{snb1}(s)$' given in (2-13) is given by (7-1) and (7-2) respectively.

$$
\begin{aligned}
i_{snb1}(t)=\Bigg\{ & \left(AG_1+\left(\frac{AG_3-AG_2a}{b}\right)e^{-at}\sin(bt)+AG_2e^{-at}\cos(bt)\right) \\
& +\left(\frac{(V_{dc}-L_sk)}{L_d}\right)e^{-a(t-T_r)}\sin(b(t-T_r))U_{T_r}(t) \\
& -\left(\begin{array}{l}\left(AG_1U_{T_r}(t)\right)+\left(\frac{AG_3-AG_2a}{b}\right)e^{-a(t-T_r)}\sin(b(t-T_r))U_{T_r}(t)+\\ AG_2e^{-a(t-T_r)}\cos(b(t-T_r))U_{T_r}(t)\end{array}\right) \\
& -\left(\begin{array}{l}\left(\frac{BG_1U_{T_f}(t)}{L_d}\right)+\left(\frac{BG_3-BG_2a}{bL_d}\right)e^{-a(t-T_f)}\sin(b(t-T_f))U_{T_f}(t)+\\ \left(\frac{BG_2}{L_d}e^{-a(t-T_f)}\cos(b(t-T_f))U_{T_f}(t)\right)\end{array}\right) \\
& +\left(\begin{array}{l}\frac{BG_1U_{T_r}(t)}{L_d}+\left(\frac{BG_3-BG_2a}{bL_d}\right)e^{-a(t-T_r)}\sin(b(t-T_r))U_{T_r}(t)+\\ \left(\frac{BG_2}{L_d}e^{-a(t-T_r)}\cos(b(t-T_r))U_{T_r}(t)\right)\end{array}\right) \\
& -\left(\frac{B(T_f-T_r)}{bL_d}e^{-a(t-T_r)}\sin(b(t-T_r))U_{T_r}(t)\right)\Bigg\}
\end{aligned}
$$

$$
A=\left(\frac{L_sk}{T_rL_d}\right);\ G_1=\frac{1}{\left(a^2+b^2\right)};\ G_1=-G_2;G_3=-2aG_1;\ a=\frac{R_d}{2L_d};\ \ b=\sqrt{\left(\frac{1}{L_dC_d}-\left(\frac{R_d}{2L_d}\right)^2\right)};\qquad (7\text{-}1)
$$

$$
\text{and } R_d<2\sqrt{\frac{L_d}{C_d}};
$$

$$
\begin{aligned}
i_{snb1}(t)=\Bigg\{ & \left(AG_1+\left(\frac{AG_3-AG_2a}{b}\right)e^{-at}\sinh(bt)+AG_2e^{-at}\cosh(bt)\right) \\
& +\left(\frac{\left(V_{dc}-L_sk\right)}{L_d}\right)e^{-a(t-T_r)}\sinh(b(t-T_r))U_{T_r}(t) \\
& -\left(\begin{array}{l}\left(AG_1U_{T_r}(t)\right)+\left(\frac{AG_3-AG_2a}{b}\right)e^{-a(t-T_r)}\sinh(b(t-T_r))U_{T_r}(t)+\\ AG_2e^{-a(t-T_r)}\cosh(b(t-T_r))U_{T_r}(t)\end{array}\right) \\
& -\left(\begin{array}{l}\left(\frac{BG_1U_{T_f}(t)}{L_d}\right)+\left(\frac{BG_3-BG_2a}{bL_d}\right)e^{-a(t-T_f)}\sinh(b(t-T_f))U_{T_f}(t)+\\ \left(\frac{BG_2}{L_d}e^{-a(t-T_f)}\cosh(b(t-T_f))U_{T_f}(t)\right)\end{array}\right) \\
& +\left(\begin{array}{l}\frac{BG_1U_{T_r}(t)}{L_d}+\left(\frac{BG_3-BG_2a}{bL_d}\right)e^{-a(t-T_r)}\sinh(b(t-T_r))U_{T_r}(t)+\\ \left(\frac{BG_2}{L_d}e^{-a(t-T_r)}\cosh(b(t-T_r))U_{T_r}(t)\right)\end{array}\right) \\
& -\left(\frac{B(T_f-T_r)}{bL_d}e^{-a(t-T_r)}\sinh(b(t-T_r))U_{T_r}(t)\right)\Bigg\}
\end{aligned}
$$

$$
A=\left(\frac{L_sk}{T_rL_d}\right);\ G_1=\frac{1}{\left(a^2-b^2\right)};\ G_1=-G_2;G_3=-2aG_1;\ a=\frac{R_d}{2L_d};\ b=\sqrt{\left(\left(\frac{R_d}{2L_d}\right)^2-\frac{1}{L_dC_d}\right)}; \qquad (7\text{-}2)
$$

$$
\text{and}\ \ R_d>2\sqrt{\frac{L_d}{C_d}}\ ;
$$

The solution for the snubber current '$i_{snb2}(s)$' given in (2-17) is given by (7-3).

for $R_d < 2\sqrt{\frac{L_{ds}}{C_d}}$,

$$i_{snb2}(t)=\left\{\begin{array}{l}\left(\frac{V_{dc}}{bL_{ds}}\right)e^{-at}\sin(bt)-\left(\begin{array}{l}\left(\frac{BG_1U_{T_f}(t)}{L_{ds}}\right)+\left(\frac{BG_3\text{-}BG_2a}{bL_{ds}}\right)e^{-a(t-T_f)}\sin(b(t-T_f))U_{T_f}(t)+\\ \left(\frac{BG_2}{L_{ds}}e^{-a(t-T_f)}\cos(b(t-T_f))U_{T_f}(t)\right)\end{array}\right)\\ +\left(\begin{array}{l}\frac{BG_1U_{T_r}(t)}{L_{ds}}+\left(\frac{BG_3\text{-}BG_2a}{bL_{ds}}\right)e^{-a(t-T_r)}\sin(b(t-T_r))U_{T_r}(t)+\\ \left(\frac{BG_2}{L_{ds}}e^{-a(t-T_r)}\cos(b(t-T_r))U_{T_r}(t)\right)-\left(\frac{B(T_f\text{-}T_r)}{bL_{ds}}e^{-a(t-T_r)}\sin(b(t-T_r))U_{T_r}(t)\right)\end{array}\right)\end{array}\right\}$$

$$G_1=\frac{1}{\left(a^2+b^2\right)};\ G_1=-G_2;G_3=-2aG_1;\ a=\frac{R_d}{2L_{ds}};\ \ b=\sqrt{\left(\frac{1}{L_{ds}C_d}-\left(\frac{R_d}{2L_{ds}}\right)^2\right)};$$

for $R_d > 2\sqrt{\frac{L_{ds}}{C_d}}$,

$$i_{snb2}(t)=\left\{\begin{array}{l}\left(\frac{V_{dc}}{bL_{ds}}\right)e^{-at}\sinh(bt)-\left(\begin{array}{l}\left(\frac{BG_1U_{T_f}(t)}{L_{ds}}\right)+\left(\frac{BG_3\text{-}BG_2a}{bL_{ds}}\right)e^{-a(t-T_f)}\sinh(b(t-T_f))U_{T_f}(t)+\\ \left(\frac{BG_2}{L_{ds}}e^{-a(t-T_f)}\cosh(b(t-T_f))U_{T_f}(t)\right)\end{array}\right)\\ +\left(\begin{array}{l}\frac{BG_1U_{T_r}(t)}{L_{ds}}+\left(\frac{BG_3\text{-}BG_2a}{bL_{ds}}\right)e^{-a(t-T_r)}\sinh(b(t-T_r))U_{T_r}(t)+\\ \left(\frac{BG_2}{L_{ds}}e^{-a(t-T_r)}\cosh(b(t-T_r))U_{T_r}(t)\right)-\left(\frac{B(T_f\text{-}T_r)}{bL_{ds}}e^{-a(t-T_r)}\sinh(b(t-T_r))U_{T_r}(t)\right)\end{array}\right)\end{array}\right\}$$

$$G_1=\frac{1}{\left(a^2-b^2\right)};\ G_1=-G_2;G_3=-2aG_1;\ a=\frac{R_d}{2L_{ds}};\ \ b=\sqrt{\left(\left(\frac{R_d}{2L_{ds}}\right)^2-\frac{1}{L_{ds}C_d}\right)};$$

(7-3)

The algebraic differential equations shown in (7-4) to (7-6) are corresponding to different sub-intervals of turn-off in a phase leg converter shown in Fig. 2-28. The '$i_{snb1}(s)$' for different subintervals are shown in (7-7) to (7-9). The solution for $i_{snb1}(s)$ different subintervals are shown in (7-10) to (7-12).

$$\begin{cases} \text{For } 0 \le t < T_f \text{ ,} \\ \begin{pmatrix} V_{dc} - L_s \dfrac{di_{Ls}(t)}{dt} + L_d \dfrac{di_{snb2}(t)}{dt} + R_d\ i_{snb2}(t) + V_{Cd2}(t) - L_d \dfrac{di_{snb1}(t)}{dt} \\ -R_d\ i_{snb1}(t) - V_{Cd1}(t) = 0 \end{pmatrix}; \\ V_{Cd1}(t) = \dfrac{1}{C_d}\int i_{snb1}(t)\,dt;\ \ V_{Cd2}(t) = \dfrac{1}{C_d}\int i_{snb2}(t)\,dt; \\ I = i_{snb1}(t) + i_{snb2}(t) + i_{ds1}(t);\ \ i_{ds1}(t) = I\left(1 - \dfrac{t}{T_f}\right);\ \ i_{Ls}(t) = i_{snb1}(t) + i_{ds1}(t); \\ i_{snb1}(0) = i_{snb2}(0) = 0;\ V_{Cd1}(0) = 0;\ \ V_{Cd2}(0) = -V_{dc}; \end{cases} \quad (7\text{-}4)$$

$$\begin{cases} \text{For } T_f \le t < T_c \text{ ,} \\ \begin{pmatrix} V_{dc} - L_s \dfrac{di_{Ls}(t)}{dt} + L_d \dfrac{di_{snb2}(t)}{dt} + R_d\ i_{snb2}(t) + V_{Cd2}(t) - L_d \dfrac{di_{snb1}(t)}{dt} \\ -R_d\ i_{snb1}(t) - V_{Cd1}(t) = 0 \end{pmatrix}; \\ V_{Cd1}(t) = \dfrac{1}{C_d}\int i_{snb1}(t)\,dt;\ \ V_{Cd2}(t) = \dfrac{1}{C_d}\int i_{snb2}(t)\,dt; \\ I = i_{snb1}(t) + i_{snb2}(t);\ \ i_{ds1}(t) = 0;\ \ i_{Ls}(t) = i_{snb1}(t) + i_{ds1}(t); \\ i_{snb1}(T_f) = i_{snb2}(T_f) = \dfrac{I}{2};\ V_{Cd2}(T_f) - V_{Cd1}(T_f) = \left(\dfrac{L_s I}{T_f}\right) - V_{dc}; \end{cases} \quad (7\text{-}5)$$

$$\begin{cases} \text{For } t \ge T_c \text{ ,} \\ V_{dc} - L_s \dfrac{di_{snb1}(t)}{dt} + V_{fwd} - L_d \dfrac{di_{snb1}(t)}{dt} - R_d\ i_{snb1}(t) - V_{Cd1}(t) = 0; \\ V_{Cd1}(t) = \dfrac{1}{C_d}\int i_{snb1}(t)\,dt; \\ I = i_{snb1}(t) + i_{snb2}(t);\ \ i_{snb1}(T_c) = i_{snb2}(T_c) \simeq \dfrac{I}{2};\ \ V_{Cd1}(T_c) = \left(V_{dc} + V_{fwd} - \dfrac{IR_d}{2}\right); \end{cases} \quad (7\text{-}6)$$

For $0 \le t < T_f$,

$$i_{snb1}(s)=\frac{\left(\frac{L_{ds}I}{T_f L_{dds}}\right)}{\left(s^2+\frac{2R_d}{L_{dds}}s+\frac{2}{L_{dds}C_d}\right)}+\frac{\left(\frac{R_d I}{T_f L_{dds}}\right)}{s\left(s^2+\frac{2R_d}{L_{dds}}s+\frac{2}{L_{d2s}C_d}\right)}+\frac{\left(\frac{I}{T_f L_{dds}C_d}\right)}{\left(s^2+\frac{2R_d}{L_{dds}}s+\frac{2}{L_{dds}C_d}\right)}; \quad (7\text{-}7)$$

For $T_f \le t < T_c$,

$$i_{snb1}(s)=\frac{\left(\frac{L_s I}{2L_{dds}}\right)s}{\left(s^2+\frac{2R_d}{L_{dds}}s+\frac{2}{L_{dds}C_d}\right)}+\frac{\left(\frac{R_d I}{L_{dds}}+\frac{L_s I}{L_{dds}T_f}\right)}{\left(s^2+\frac{2R_d}{L_{dds}}s+\frac{2}{L_{d2s}C_d}\right)}+\frac{\left(\frac{I}{L_{dds}C_d}\right)}{s\left(s^2+\frac{2R_d}{L_{dds}}s+\frac{2}{L_{dds}C_d}\right)}; \quad (7\text{-}8)$$

For $t \ge T_c$,

$$i_{snb1}(s)=\frac{\left(\frac{I}{2}\right)s}{\left(s^2+\frac{R_d}{L_{ds}}s+\frac{1}{L_{ds}C_d}\right)}+\frac{\left(\frac{R_d I}{2L_{ds}}\right)}{\left(s^2+\frac{R_d}{L_{ds}}s+\frac{1}{L_{ds}C_d}\right)}-\frac{\left(\frac{2V_{fwd}}{L_{ds}}\right)}{\left(s^2+\frac{R_d}{L_{ds}}s+\frac{1}{L_{ds}C_d}\right)}; \quad (7\text{-}9)$$

for $R_d < \sqrt{\frac{L_{dds}}{C_d}}$ and $0 \le t < T_f$,

$$i_{snb1}(t)=\left\{\begin{array}{l}\left(\frac{A}{b}\right)e^{-at}\sin(bt)+\left(\frac{R_d I}{T_f L_{dds}}\right)\left(G_1+\left(\frac{G_3-G_2 a}{b}\right)e^{-at}\sin(bt)+G_2 e^{-at}\cos(bt)\right) \\ +\left(\frac{I}{T_f L_{dds} C_d}\right)\left(G_1 t+\frac{G_2}{b}e^{-at}\sin(bt)+G_3\left(\begin{array}{l}G_1+\left(\frac{G_3-G_2 a}{b}\right)e^{-at}\sin(bt) \\ +G_2 e^{-at}\cos(bt)\end{array}\right)\right)\end{array}\right\}$$

$$A=\left(\frac{L_{ds} I}{T_f L_{dds}}\right);\ G_1=\frac{1}{\left(a^2+b^2\right)};\ G_1=-G_2;G_3=-2aG_1;\ a=\frac{R_d}{L_{dds}};\ \ b=\sqrt{\left(\frac{1}{L_{dds} C_d}-\left(\frac{R_d}{L_{dds}}\right)^2\right)};$$

For $R_d > \sqrt{\frac{L_{dds}}{C_d}}$ and $0 \le t < T_f$,

$$i_{snb1}(t)=\left\{\begin{array}{l}\left(\frac{A}{b}\right)e^{-at}\sinh(bt)+\left(\frac{R_d I}{T_f L_{dds}}\right)\left(G_1+\left(\frac{G_3-G_2 a}{b}\right)e^{-at}\sinh(bt)+G_2 e^{-at}\cosh(bt)\right) \\ +\left(\frac{I}{T_f L_{dds} C_d}\right)\left(G_1 t+\frac{G_2}{b}e^{-at}\sinh(bt)+G_3\left(\begin{array}{l}G_1+\left(\frac{G_3-G_2 a}{b}\right)e^{-at}\sinh(bt) \\ +G_2 e^{-at}\cosh(bt)\end{array}\right)\right)\end{array}\right\} \quad (7\text{-}10)$$

$$A=\left(\frac{L_{ds} I}{T_f L_{dds}}\right);\ G_1=\frac{1}{\left(a^2-b^2\right)};\ G_1=-G_2;G_3=-2aG_1;\ a=\frac{R_d}{L_{dds}};\ \ b=\sqrt{\left(\frac{-1}{L_{dds} C_d}+\left(\frac{R_d}{L_{dds}}\right)^2\right)};$$

for $R_d < \sqrt{\frac{L_{dds}}{C_d}}$ and $T_f \le t < T_c$,

$$i_{snb1}(t)=\left\{\begin{array}{l}\left(\frac{I}{2}\right)\left(e^{-a(t-T_f)}\cos(b(t-T_f))-\frac{a}{b}e^{-a(t-T_f)}\sin(b(t-T_f))\right)\\ +\left(\frac{R_d I}{bL_{dds}}+\frac{L_s I}{bL_{dds}T_f}\right)\left(e^{-a(t-T_f)}\sin(b(t-T_f))\right)\\ +\left(\frac{I}{L_{dds}C_d}\right)\left(\begin{array}{l}G_1+\left(\frac{G_3-G_2 a}{b}\right)e^{-a(t-T_f)}\sin(b(t-T_f))\\ +G_2 e^{-a(t-T_f)}\cos(b(t-T_f))\end{array}\right)\end{array}\right\}$$

$$G_1=\frac{1}{\left(a^2+b^2\right)};\ G_1=-G_2;G_3=-2aG_1;\ a=\frac{R_d}{L_{dds}};\ \ b=\sqrt{\left(\frac{1}{L_{dds}C_d}-\left(\frac{R_d}{L_{dds}}\right)^2\right)};$$

for $R_d > \sqrt{\frac{L_{dds}}{C_d}}$ and $T_f \le t < T_c$,

$$i_{snb1}(t)=\left\{\begin{array}{l}\left(\frac{I}{2}\right)\left(e^{-a(t-T_f)}\cosh(b(t-T_f))-\frac{a}{b}e^{-a(t-T_f)}\sinh(b(t-T_f))\right)\\ +\left(\frac{R_d I}{bL_{dds}}+\frac{L_s I}{bL_{dds}T_f}\right)\left(e^{-a(t-T_f)}\sinh(b(t-T_f))\right)\\ +\left(\frac{I}{L_{dds}C_d}\right)\left(\begin{array}{l}G_1+\left(\frac{G_3-G_2 a}{b}\right)e^{-a(t-T_f)}\sinh(b(t-T_f))\\ +G_2 e^{-a(t-T_f)}\cosh(b(t-T_f))\end{array}\right)\end{array}\right\}$$

$$G_1=\frac{1}{\left(a^2-b^2\right)};\ G_1=-G_2;G_3=-2aG_1;\ a=\frac{R_d}{L_{dds}};\ \ b=\sqrt{\left(\frac{-1}{L_{dds}C_d}+\left(\frac{R_d}{2L_{dds}}\right)^2\right)};\qquad (7\text{-}11)$$

for $R_d < 2\sqrt{\frac{L_{ds}}{C_d}}$ and $t > T_c$,

$$i_{snb1}(t)=\left\{\begin{array}{l}\left(\frac{I}{2}\right)\left(e^{-a(t-T_c)}\cos(b(t-T_c))-\frac{a}{b}e^{-a(t-T_c)}\sin(b(t-T_c))\right)\\ +\left(\frac{R_d I}{2bL_{ds}}\right)\left(e^{-a(t-T_c)}\sin(b(t-T_c))\right)\\ +\left(\frac{2V_{fwd}}{L_{ds}}\right)\left(e^{-a(t-T_c)}\sin(b(t-T_c))\right)\end{array}\right\}$$

for $R_d > 2\sqrt{\frac{L_{ds}}{C_d}}$ and $t > T_c$,

$$i_{snb1}(t)=\left\{\begin{array}{l}\left(\frac{I}{2}\right)\left(e^{-a(t-T_c)}\cosh(b(t-T_c))-\frac{a}{b}e^{-a(t-T_c)}\sinh(b(t-T_c))\right)\\ +\left(\frac{R_d I}{2bL_{ds}}\right)\left(e^{-a(t-T_c)}\sinh(b(t-T_c))\right)\\ +\left(\frac{2V_{fwd}}{L_{ds}}\right)\left(e^{-a(t-T_c)}\sinh(b(t-T_c))\right)\end{array}\right\} \quad (7\text{-}12)$$

$$a=\frac{R_d}{2L_{ds}};\quad b=\sqrt{\left(\frac{1}{L_{ds}C_d}-\left(\frac{R_d}{2L_{ds}}\right)^2\right)};$$