ABSTRACT

LI, JUN. Design, Control and Characteristics of Multilevel Active NPC Converters for High Power Applications. (Under the direction of Dr. Alex Q. Huang.)

Active neutral-point-clamped (ANPC) converter is a new family of multilevel technologies, which was originally proposed to solve the drawback of unbalanced power loss distribution among the devices in conventional neutral-point-clamped (NPC) converters. The purpose of this dissertation has been to further develop the design, topology, control and characteristics of ANPC converters for high power applications, such as large wind turbine systems and medium-voltage motor drive systems.

First, the concept of ETO Light NPC and ANPC Power Electronics Building Blocks (PEBB) is proposed. The electrical design and the component physical arrangement are discussed for the PEBBs. The methodologies for power loss calculation and thermal analysis of the PEBBs are presented with detailed analytical equation derivations. The system configurations with the proposed ETO Light PEBBs are identified for multi-MW wind turbine systems with AC and DC transmission, respectively. The thermal performance of the ETO Light NPC PEBB and ANPC PEBB is studied for the 5 MW and the 7 MW wind turbine cases, respectively.

Second, the fault tolerant capability of the 3L-ANPC converter is analyzed and the fault tolerant control strategies are proposed to enable the continuous operating of the converter under any single device open and short failure condition. The requirement on the fault detection time is also discussed. Moreover, the fault tolerant operation of the 3L-ANPC converter under multiple device failure conditions is studied. Simulation and experiment

results are provided for verification. Furthermore, the reliability comparison for 3L-NPC and 3L-ANPC converters is investigated. Finally, the control schemes are proposed for the 3L-ANPC converter when it is applied on the generator side of a direct-driven permanent magnet synchronous generator (PMSG) based large wind turbine system, which allows the wind turbine to remain in service and continue providing active power under device failure conditions. Simulation results verify the proposed methods.

Third, a new 9L-ANPC converter is proposed for the next generation PEBB technology for power quality improvement in high power applications. Its operating principles and control, as well as floating capacitor voltage balance schemes are presented in detail. Simulation and experiment results are provided for verification. The proposed 9L-ANPC topology is also compared with other conventional 9L converters and existing 9L-ANPC converters from several aspects. The results indicate that the new 9L-ANPC converter shows better overall performance. Finally, the proposed topology is applied on the grid side of a 6 MW wind turbine system to achieve a filterless grid connection. Simulation results prove that the harmonic limit of the utility standards can be satisfied even without using a grid passive filter, which implies that the cost, efficiency, power density and reliability of the system can be improved.

Last, a simplified space vector based current controller for any general N-level converter is proposed. In this method, the mapping technique between the subhexagon of the N-level converter and the hexagon of the two-level converter is used to identify the proper output voltage vector to suppress harmonic current content in steady state and obtain fast current

response in transient state. The proposed current controller does not require the calculation of the back EMF voltage of the load, and the controller complexity is greatly reduced due to the use of very simple lookup tables, thus it can easily be extended to any N-level converter. The proposed current controller is explained and verified by simulation on a five-level ANPC converter for motor drive applications.

Design, Control and Characteristics of Multilevel Active NPC Converters for High Power Applications

by
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DEDICATION

To my parents

Zongquan Li and **Wenhua Lin**

BIOGRAPHY

Jun Li was born in Shenyang, Liaoning province, China. He received his B.S. degree in Automation from Tianjin University, Tianjin, China and M.S. degree in Electrical Engineering from Zhejiang University, Hangzhou, China, in 2004 and 2006, respectively. He is currently pursuing his Ph.D. degree in North Carolina State University, Raleigh, NC, USA. Since 2006, he has been with the Semiconductor Power Electronics Center (SPEC) at North Carolina State University. Since 2008, he has been with the NSF Engineering Research Center for Future Renewable Electric Energy Delivery and Management (FREEDM) systems at North Carolina State University.

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Chapter 1 Introduction

1.1 Power Electronics for Wind Energy

Over the last several decades, the worldwide interest in renewable energy sources (wind, photovoltaic, geothermal and hydro) has risen drastically. A large number of power generation systems based on renewable energy sources are currently being developed and installed, and energy conversion efficiencies are being improved for the overall goal of CO_2 emission and our dependence on fossil fuels [1]. At present, wind power is one of the country's largest sources of new power generation compared to others penetrating the electric grid. In 2009, with over 10,000 megawatts (MW) installed, wind power accounted for 39% of all new generating capacity installed in U.S. [2]. The United States government has expectations of generating 20% of its electricity from wind power by 2030. This would require the U.S. wind power capacity to grow from 35 GW (as of 2009) to more than 300 GW in 2030. This is pictorially shown in Fig. 1.1 [3].

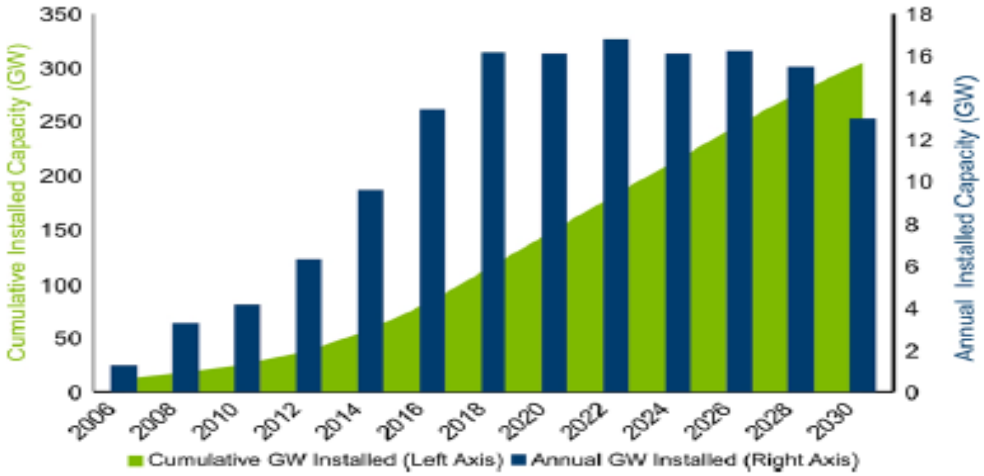


Fig. 1.1 Annual and cumulative wind installations by 2030 in U.S.

Throughout the past 20 years, along with the new wind turbine technologies being brought to the market every five years, the size of the wind turbines has grown linearly and has achieved reductions in life-cycle cost of energy (COE), as illustrated in Fig. 1.2 [3]. The motivation for developing larger turbines is to meet the desire of improving energy capture by extracting the stronger winds at higher elevations. However, there are some economic and logistical constraints to this trend of the continued growth in wind turbine size, such as transportation and physical installation.

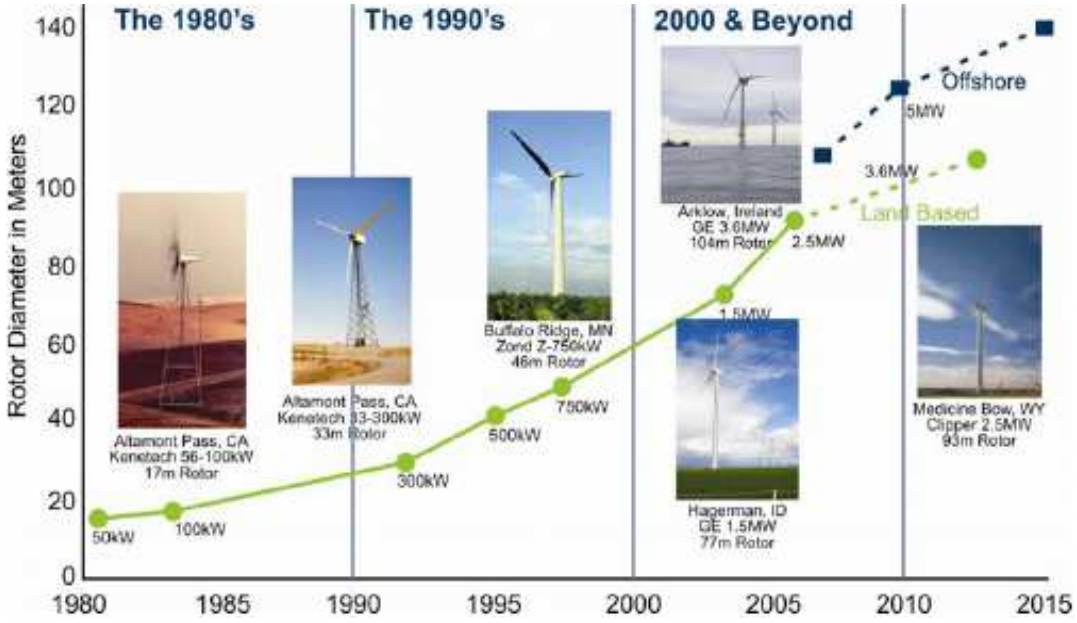


Fig. 1.2 The development of U.S. commercial wind turbines

The conventional fixed speed wind turbines were based on squirrel-cage induction generators which were directly connected to the grid. However, the controllability of the wind turbines becomes more and more important along with the increased power rating. In contrast to the traditional fixed speed wind turbines, the modern wind turbine technologies employ power electronics converters to realized variable speed turbine operation, which

brings many benefits including reduced mechanical stress on the mechanical components like the shaft and gearbox, increased power capture, and reduced acoustical noise. Power electronics converters play a very important role in integrating the wind power into power systems with high efficiency. Moreover, they are the key components for meeting the grid codes requirements, including the control of voltage, frequency, active and reactive power, fault ride-through capability, voltage and current harmonics, etc.

Fig. 1.3 shows the possible technical solutions and the technological roadmap for wind energy conversions, starting with wind power and converting the mechanical power into electrical power using different classes of generators and full-scale or partial-scale power electronics converters [4].

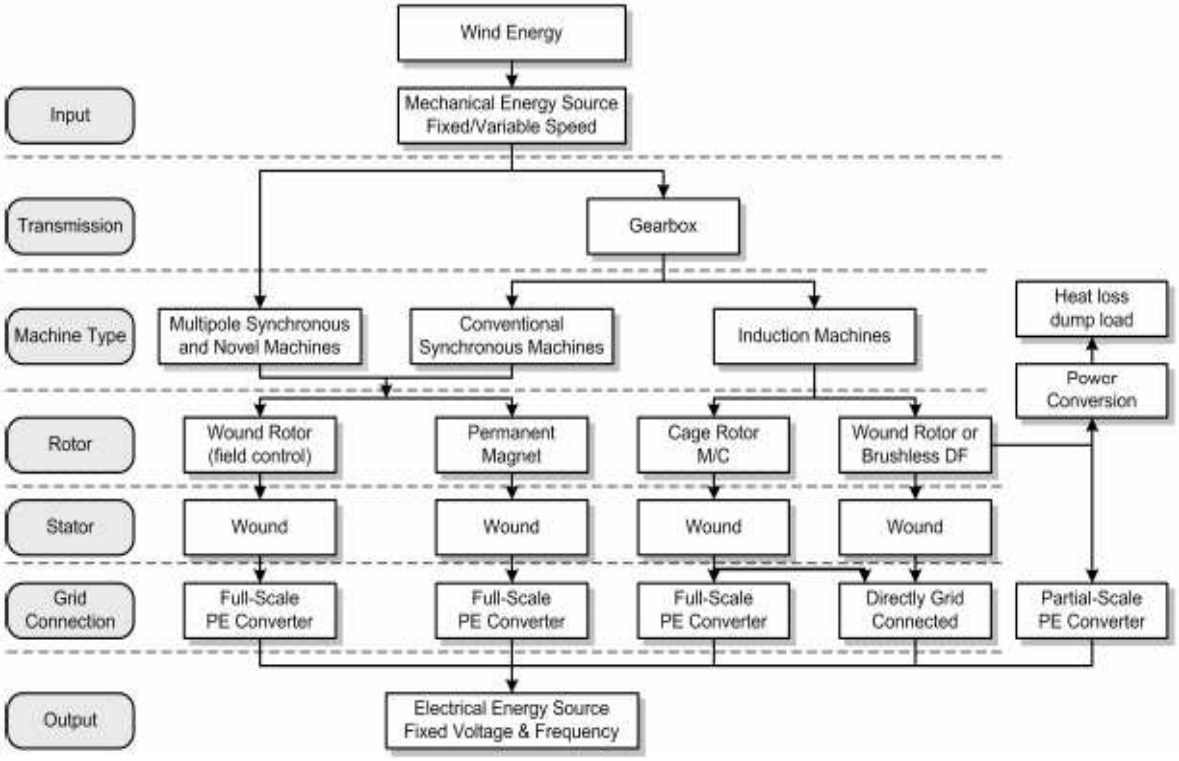


Fig. 1.3 Technical solutions and roadmap for wind turbine technologies

For multi-MW wind turbines, the rotational speed is typically 10-15 rpm. The most efficient way, regarding the weight of the system, for converting the low-speed, high-torque wind power to electrical power is to use a gearbox and a standard generator equipped with power converters. However, the gearbox can be eliminated by using a multi-pole generator, which is referred to as a direct-driven generator. Compared with a gearbox-coupled wind turbine generator, a direct-driven generator has reduced overall size, lower installation and maintenance cost, higher reliability, a flexible control method and quick response to wind fluctuations and load variation.

Currently, the most popular configurations of variable-speed wind turbine systems are the partial-scale power converter with doubly-fed induction generator (DFIG) in Fig. 1.4 (a), and the full-scale power converter with direct-driven permanent magnet synchronous generator (PMSG) in Fig. 1.4 (b). The main advantage of the DFIG configuration is the lower cost due to the use of a partial rating converter (around 30%). However, since the price of the semiconductor devices and power converters has been decreasing, the latter configuration is becoming more promising for multi-MW wind turbines, especially for offshore wind farms. Its main advantages include low maintenance requirement (no brushes and gearbox), protection against gearbox stress due to grid voltage variation and wind turbulence, better fault ride-through capability to meet grid codes, high efficiency and high power density due to the rare earth magnet and concentrated pole designs in PMSG, less moving parts, higher reliability and reduced overall size and weight due to gearless drive train.

The power ratings achieved by today's multi MW wind turbines are best handled at the medium-voltage level (3.3/4.16/6.9/13.8 kV) instead of the low-voltage level (690 V). At

higher voltage levels, the current levels are lower, hence, power losses in the generator, the converter and the cables in the system are minimized [5].

As one of the most important medium voltage converter technologies, multilevel converters have drawn increasing attention in the past decades, especially for the medium to high power, medium voltage applications, such as motor drives and wind turbine systems. Compared with traditional two-level converters, multilevel converters can effectively reduce the harmonic content in the input and output voltages as well as the EMI noise [6] [7]. These features have great benefits for the grid connection of the wind power generation.

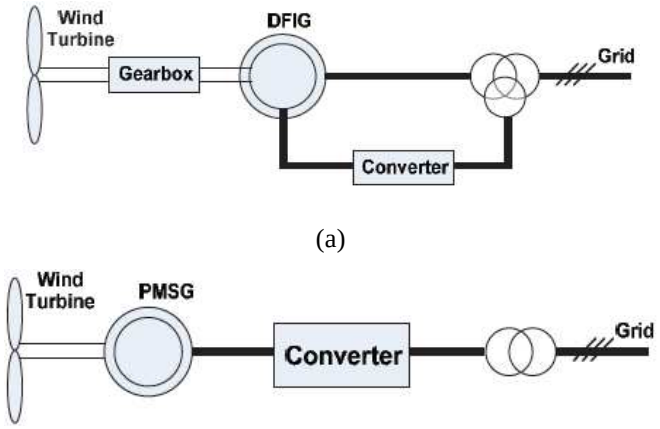


Fig. 1.4 Two typical configurations of variable-speed wind turbines (a) DFIG (b) direct-driven PMSG

1.2 Multilevel Converters

Multilevel converters are considered today as the state-of-the-art power conversion techniques for high power and power quality demanding applications. The main advantages of multilevel converters include higher voltage operating capability using lower voltage rating semiconductor devices, reduced dv/dt, lower common-mode voltages, reduced voltage and current harmonic content, higher efficiency, and potential fault-tolerant capability.

1.2.1 Concept of Multilevel Converters

Multilevel converters include an array of semiconductor devices and capacitive voltage sources. By proper connection and control, they can generate a multiple-step voltage waveform with variable and controllable frequency, phase and amplitude. The stepped waveform is synthesized by controlling the switch devices to connect the load to the different capacitive voltage sources. Fig. 1.5 shows one phase of the converters with two, three and nine level output waveform [8]. The action of the semiconductors devices is represented by an ideal switch with several positions. A two-level converter generates an output voltage with two values (levels) with respect to the negative terminal (N) of the capacitor, while the three-level converter generates three voltages, and so on. It is observed that two-level converters can generate a variable frequency and amplitude voltage waveform by adjusting a time average of the two voltage levels, which is usually performed with pulse-width modulation (PWM) techniques. Multilevel converters have the voltage level as another control degree of freedom to generate the output waveform to obtain improved output waveform quality.

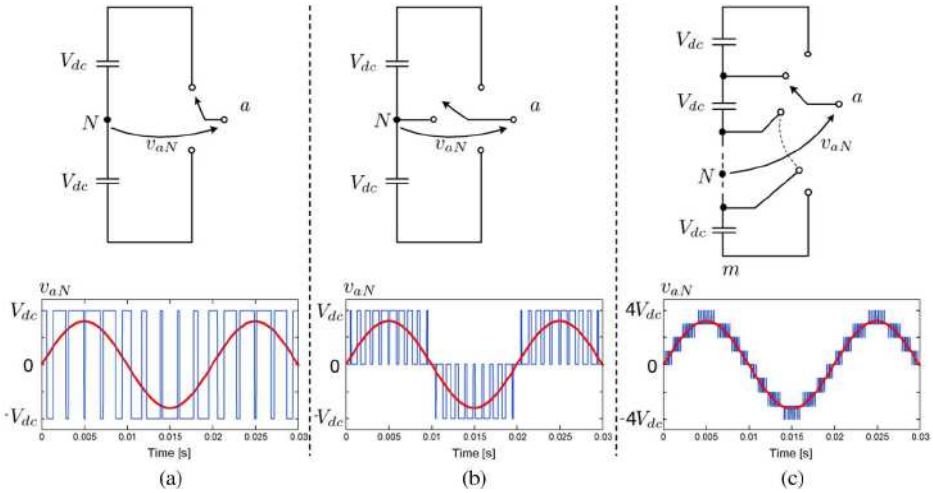


Fig. 1.5 One phase leg of a converter with (a) two levels (b) three levels and (c) nine levels

1.2.2 Topologies of Multilevel Converters

There are many ways to connect semiconductor devices and capacitive power sources to generate multilevel voltage waveforms. Over the years, several multilevel converter topologies have been introduced in the academic and industry settings [9] [10] [11]. Generally, these converters can be classified into two categories: multilevel converters with single DC source and multiple DC sources. Each category includes several different topologies, as shown in Fig. 1.6. The most widely known and used multilevel topologies are neutral-point-clamped (NPC) [12], flying capacitor (FC) [13] and cascaded H-bridge (CHB) [14]. The FC and CHB topologies are also known as multicell converters (MCs) due to their modular structure consisting of a number of smaller power cells.

More recently, some variations and combinations of these basic topologies have been proposed to improve the converter performance and satisfy the requirements for particular applications. Some examples include the following:

- The active NPC (ANPC) converter [15] produces a balanced power loss and junction temperature distribution among the semiconductor devices in the converter. Therefore, it enables a substantial increase in the maximum output power or switching frequency compared to the traditional NPC converter.
- The modular multilevel converter (MMC) [16] is composed of a cascaded connection of two-level flying-capacitor power cells (half-bridge cells). This topology allows the modular design concept, higher voltage operation, reduction in capacitor volume, and better output waveform quality.

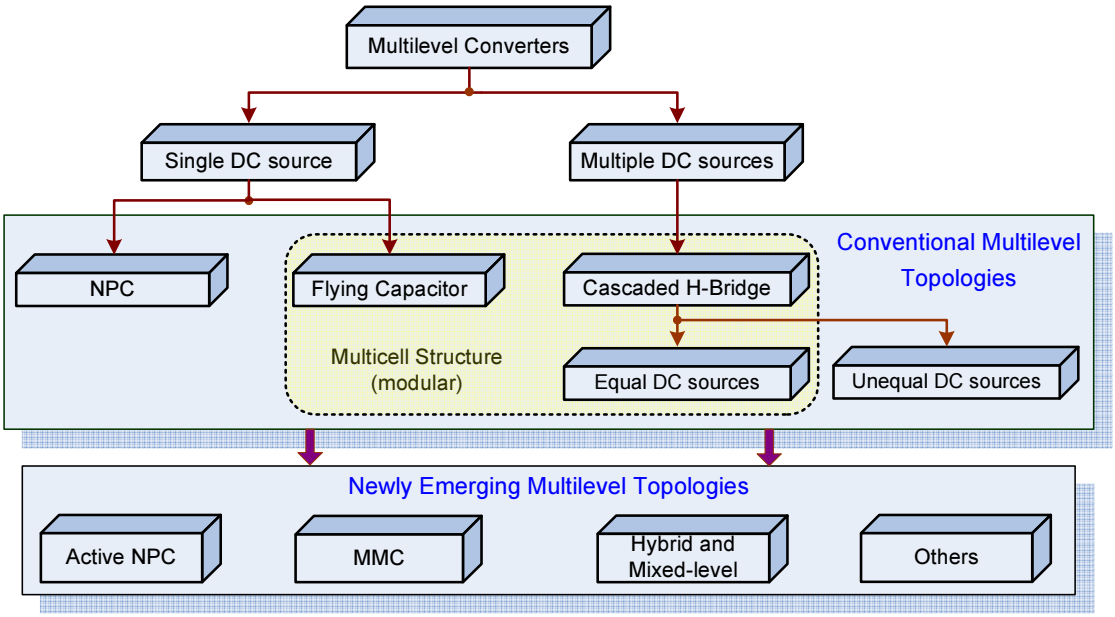


Fig. 1.6 Categories of multilevel converter topologies

- The hybrid and mixed-level cascaded converters [17] [18] [19] [20] [21] [22] are different compared to the traditional CHB converters fed by equal dc voltage sources. The hybrid converter, also called asymmetric converter, has an asymmetry in the dc voltage sources. It generates more output voltage levels compared to the CHB converter using less semiconductors devices and capacitors. Besides the H-bridge cell, other power cells like the NPC or FC cells, can also be used in the cascaded converter, thus various multilevel converters are derived, classified as mixed-level cascaded converters.

1.2.2.1 Neutral-point-clamped (NPC) converter

The NPC converter uses series-connected capacitors to divide the DC bus voltage into a set of voltage levels. To generate an *n*-level phase voltage, an NPC converter needs *n*-1 capacitors on the DC bus. Fig. 1.7 shows a five-level NPC converter. The DC bus consists of

four capacitors C_1, C_2, C_3, and C_4 with the voltage across each capacitor being $V_{dc}/4$. Each device voltage stress will be limited to $V_{dc}/4$ due to the presence of the clamping diodes.

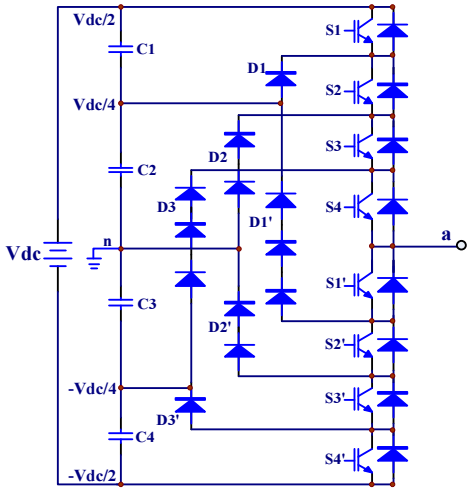


Fig. 1.7 Five-level neutral-point-clamped (NPC) converter

To explain how the staircase voltage is synthesized, the neutral point *n* is considered as the output phase voltage reference point. There are five switch combinations to synthesize five level voltages across *a* and *n*:

- For $V_{an} = V_{dc}/2$, turn on all upper switches S_1~S_4.
- For $V_{an} = V_{dc}/4$, turn on three upper switches S_2~S_4 and one lower switch S_1'.
- For $V_{an} = 0$, turn on two upper switches S_3 and S_4 and two lower switches S_1' and S_2'.
- For $V_{an} = -V_{dc}/4$, turn on one upper switches S_4 and three lower switch S_1'~S_3'.
- For $V_{an} = -V_{dc}/2$, turn on all lower switches S_1'~S_4'.

Four complementary switch pairs exist in each phase: (S_1, S_1'), (S_2, S_2'), (S_3, S_3'), and (S_4, S_4'). In a five-level NPC converter, although each device is only required to block a voltage level of $V_{dc}/4$, the clamping diodes must have different voltage ratings for reverse voltage blocking. For example, in Fig. 1.7, when lower devices S_2'-S_4' are turned on, D_1' needs to

block $3V_{dc}/4$. Similarly, D_2 and D_2' need to block $2V_{dc}/4$, and D_3 needs to block $3V_{dc}/4$. If each diode has the same voltage rating, then several diodes have to be placed in series. This large number of diodes causes a limitation in the number of levels of the converter. More than five levels might become impractical because of the diode reverse recovery. Also, the voltage unbalance in the dc-link capacitors may produce excessively large voltage on the devices and cause device failure. Therefore, a well performed control of the dc-link capacitor voltage balance is extremely important.

1.2.2.2 Flying capacitor (FC) converter

The FC converter uses a ladder structure of capacitors to clamp the device voltage to one capacitor voltage level. To generate an *n*-level phase voltage, *n*-1 capacitors are needed on the DC bus. Fig. 1.8 shows a five-level FC converter. Its voltage synthesis has more flexibility than a five-level NPC converter. The five-level voltages across *a* and *n* can be synthesized by the following switching combinations:

- For $V_{an} = V_{dc}/2$, turn on all upper switches S_1~S_4.
- For $V_{an} = V_{dc}/4$, there are three combinations. 1) S_1, S_2, S_3, S_1': $V_{an} = V_{dc}/2$ of upper C_4 – $V_{dc}/4$ of C_1; 2) S_2, S_3, S_4, S_4': $V_{an} = 3V_{dc}/4$ of C_3 – $V_{dc}/2$ of lower C_4; 3) S_1, S_3, S_4, S_3': $V_{an} = V_{dc}/2$ of upper C_4 – $3V_{dc}/4$ of C_3+ $2V_{dc}/4$ of C_2.
- For $V_{an} = 0$, there are six combinations. 1) S_1, S_2, S_1', S_2': $V_{an} = V_{dc}/2$ of upper C_4 – $2V_{dc}/4$ of C_2; 2) S_3, S_4, S_3', S_4': $V_{an} = 2V_{dc}/4$ of C_2 – $V_{dc}/2$ of lower C_4; 3) S_1, S_3, S_1', S_3': $V_{an} = V_{dc}/2$ of upper C_4 – $3V_{dc}/4$ of C_3 + $2V_{dc}/4$ of C_2 – $V_{dc}/4$ of C_1; 4) S_1, S_4, S_2', S_3': $V_{an} = V_{dc}/2$ of upper C_4 – $3V_{dc}/4$ of C_3 + $V_{dc}/4$ of C_1; 5) S_2, S_4, S_2', S_4': V_{an} =

$3V_{dc}/4$ of C_3 – $2V_{dc}/4$ of C_2 + $V_{dc}/4$ of C_1 – $V_{dc}/2$ of lower C_4; and 6) S_2, S_3, S_1', S_4': $V_{an} = 3V_{dc}/4$ of C_3 – $V_{dc}/4$ of C_1 – $V_{dc}/2$ of lower C_4.

- For voltage level $V_{an} = -V_{dc}/4$, there are three combinations. 1) S_1, S_1', S_2', S_3': V_{an} = $V_{dc}/2$ of upper C_4 – $3V_{dc}/4$ of C_3; 2) S_4, S_2', S_3', S_4': $V_{an} = V_{dc}/4$ of C_1 – $V_{dc}/2$ of lower C_4; 3) S_3, S_1', S_3', S_4': $V_{an} = 2V_{dc}/4$ of C_2 – $V_{dc}/4$ of C_1 – $V_{dc}/2$ of lower C_4.
- For voltage level $V_{an} = -V_{dc}/2$, turn on all lower switches, S_1'~S_4'.

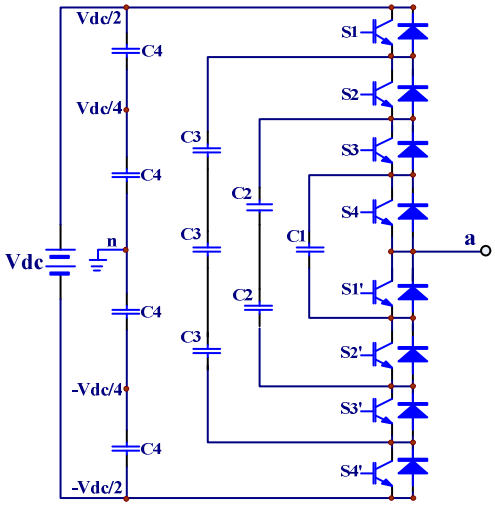


Fig. 1.8 Five-level flying capacitor (FC) converter

In the description above, the capacitors with positive signs are discharged, while those with negative signs are charged. By properly selecting the capacitor combinations, it is possible to balance the flying capacitor voltages.

Assuming the voltage rating of each capacitor is the same as the devices, an *m*-level converter requires a total of (*m*−1) (*m*−2) / 2 flying capacitors per phase, in addition to (*m*−1) capacitors on the dc-link. The implementation of the FC converters with higher number of levels is limited due to the large number of capacitors connected in series.

1.2.2.3 Cascaded H-Bridge (CHB) converter

The CHB converter is based on the series connection of a single-phase H-bridge converter with separate dc sources, which may be obtained from a battery, fuel cell, etc. Fig. 1.9 shows one phase leg of a five-level CHB converter with two cells in series. The phase voltage is synthesized by adding the voltages generated by each cell. Assuming the dc source voltages of the cells are the same and equals to V_{dc}, each H-bridge cell can generate three output voltage levels, which include $\pm V_{dc}$ and 0. This is achieved by connecting the capacitors sequentially to the AC side through different combinations of the four power switches. The output AC voltage of the converter varies from $-2V_{dc}$ to $+2V_{dc}$ with five levels.

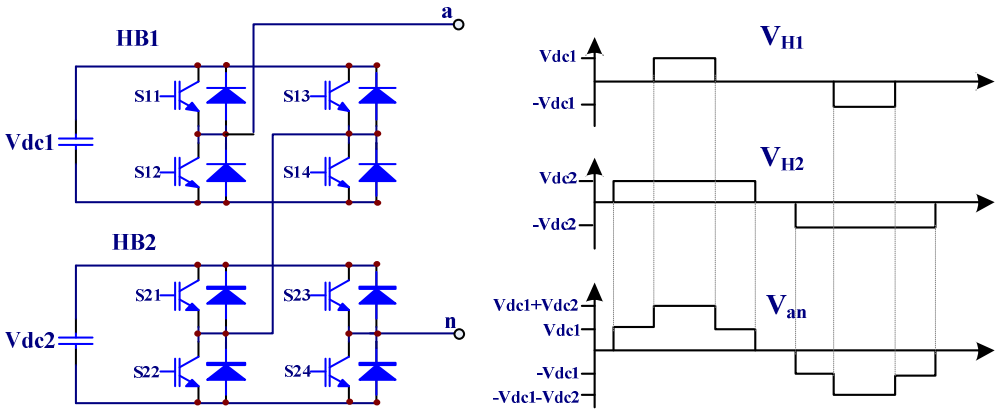


Fig. 1.9 Five-level cascaded H-bridge (CHB) converter

Compared with NPC and FC converters, the major advantage of the CHB topology is the reduced number of capacitors and diodes to achieve the same number of voltage levels. Moreover, the CHB topology provides the flexibility to increase the power rating and improve the waveform quality with increased options in obtainable voltage levels due to the modular structure. However, the necessity of multiple isolated dc sources is the main disadvantage.

Instead of using the same dc input voltages for each H-bridge cells, a proper selection of voltage asymmetry between the cells can produce different combinations of voltage levels and eliminate redundancies. This type of cascaded converter is named the asymmetric CHB converter [17]. As shown in Fig. 1.10, an asymmetry in the voltage ratio of 1:3 for a two-cell CHB converter leads to a nine-level waveform.

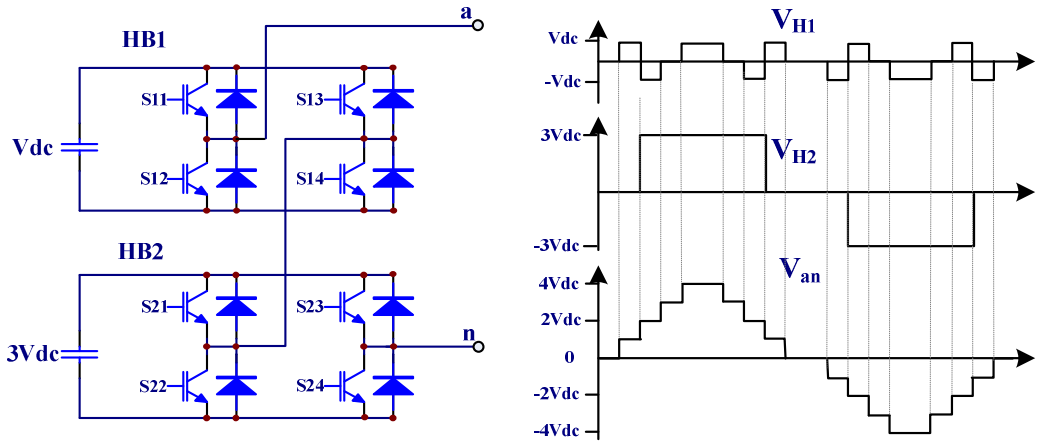


Fig. 1.10 Asymmetric cascaded converter with voltage ratio of 1:3 for the two H-bridge cells

The asymmetric CHB converter can achieve the same output voltage quality with less hardware. However, the maximum blocking voltage of the devices will limit the value of the permitted dc source. In this topology, it is also possible to use high-frequency PWM for one cell, while the other cell switches at a lower rate. For example, in Fig. 1.10, the bottom cell, with a higher dc input voltage, can use GTOs or IGCTs, and operate at its fundamental frequency. The top H-bridge cell, with a lower dc input voltage, can use IGBTs and switch at a PWM frequency to smooth the waveform [23].

Another alternative for reducing the number of isolated dc sources while generating the same number of voltage levels is to use a single power supply as the first dc voltage source,

and replace the remaining dc voltage sources with floating capacitors. The voltage balance of the floating capacitors can be achieved by using the redundant switching states of the converter [24].

1.2.2.4 Generalized multilevel converter

Fig. 1.11 shows a five-level generalized multilevel converter [25]. The existing multilevel converters, like the NPC and FC converters, can be derived from this topology. Since this converter is composed of a number of basic two-level cells, it is called the P2 multilevel converter. The voltage of each switching device, diode, and capacitor is $V_{dc}/4$. Using the same pyramid structure of the P2 converter, new topologies can be derived by replacing the two-level cells by three-level NPC or FC cells.

One feature of the generalized multilevel converter is the floating capacitor voltage self-balance capability regardless of load characteristics. However, compared with other multilevel converters, it requires more devices, diodes and capacitors, which limits its applications in practice.

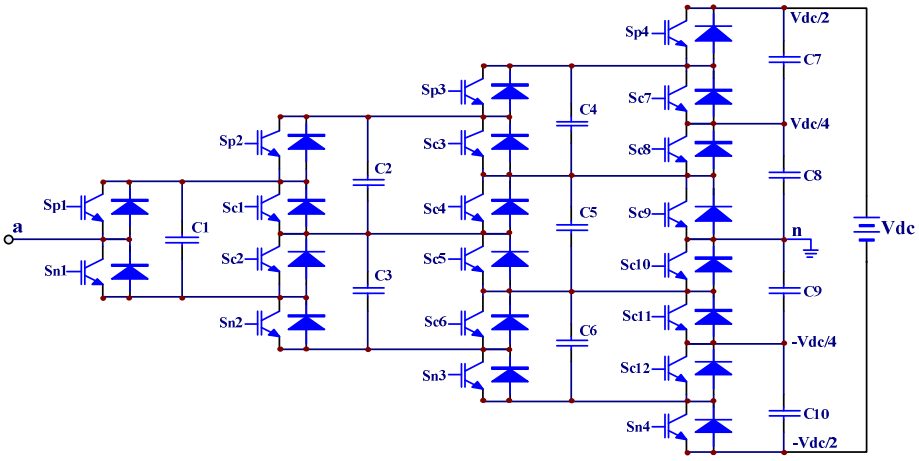


Fig. 1.11 Five-level generalized P2 multilevel converter

1.2.2.5 Mixed-level cascaded converter

For high voltage high power applications, it is possible to use NPC or FC converter cells to replace the H-bridge cells in a cascaded converter [26]. The main purpose is to reduce the number of isolated dc sources. This type of emerging multilevel topology is called the mixed-level cascaded converter. Fig. 1.12 shows a nine-level mixed-level cascaded converter incorporating the three-level FC converter as the basic cell. It is obvious that the NPC converter can also be used as the basic cell. Only two separate dc sources are needed for this converter. In contrast, for a nine-level CHB converter similar to Fig. 1.9, four separate dc sources are required.

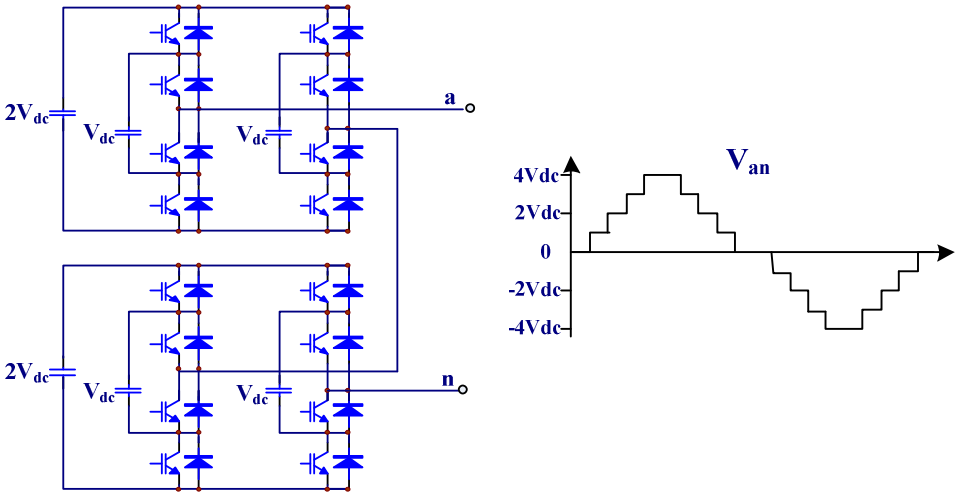


Fig. 1.12 Nine-level mixed-level cascaded converter using three-level FC cells

In [27], another mixed-level cascaded converter was proposed, which combines the three-level NPC converter and the single-phase H-bridge converter, as illustrated in Fig. 1.13. The NPC converter can generate the same number of output voltage levels as the single-phase H-bridge topology. However it only uses one common dc source for all three-phases, instead of separate sources for each H-bridge it replaces. The dc-link voltages of the converter are

configured in a 3:1 ratio (half of NPC dc-link voltage versus H-bridge dc-link voltage). This leads to a reduction of the required number of dc sources, from six to four, for a three-phase nine-level cascaded converter in Fig. 1.10.

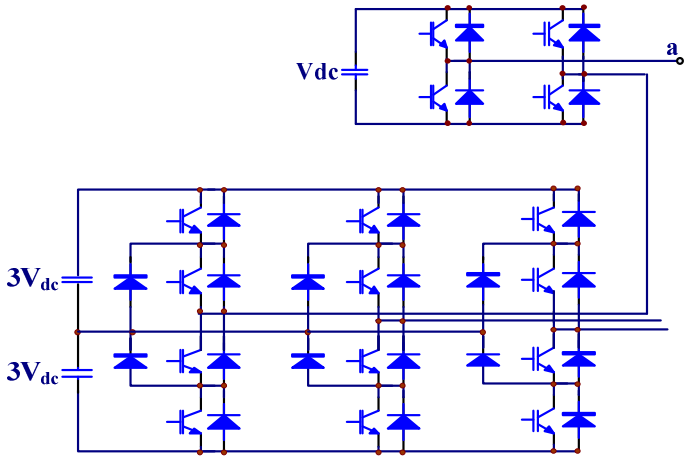


Fig. 1.13 Nine-level mixed-level cascaded converter with three-level NPC and H-bridge converters

1.2.2.6 Multi-pulse converter

This type of converter synthesizes the output voltage by connecting the output of a number of standard three-phase, two-level converters through transformers. A complicated transformer circuit is required to create the multilevel voltage waveform and increase the voltage and power rating. Fig. 1.14 shows an 18-pulse multilevel converter [28]. In order to add the converter output voltages together, the outputs of the three modules need to be synchronized with a separation of 120° between each phase. For example, obtaining a three-level voltage between outputs *a* and *b*, the voltage is synthesized by $V_{ab} = V_{a1\text{-}b1} + V_{b1\text{-}a2} + V_{a2\text{-}b2}$. The phase between b_1 and a_2 is provided by a_3 and b_3 through an isolated transformer. With three converters synchronized, the voltages $V_{a1\text{-}b1}$, $V_{b1\text{-}a2}$ and $V_{a2\text{-}b2}$ are all in phase. Thus, the output voltage level is simply tripled.

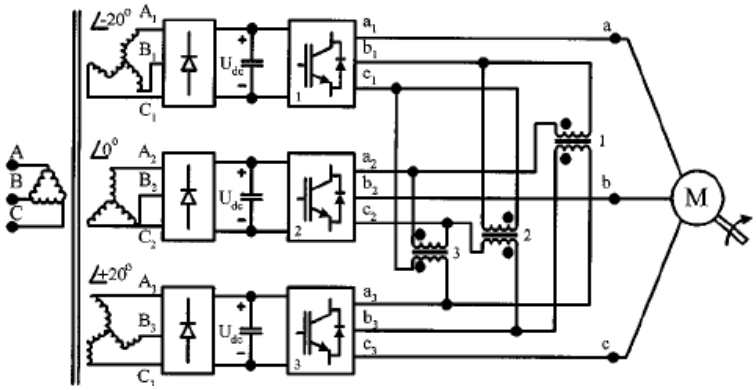


Fig. 1.14 An 18-pulse converter

1.2.2.7 Modular multilevel converter (MMC)

This converter, proposed in the early 2000s [16], has received more attention in recent years especially with HVDC applications [29] [30]. Basically, the MMC is composed of a number of single phase, two-level half-bridge converter cells by connecting them in series. Inductors are usually needed within each leg for protection during transitory short circuits.

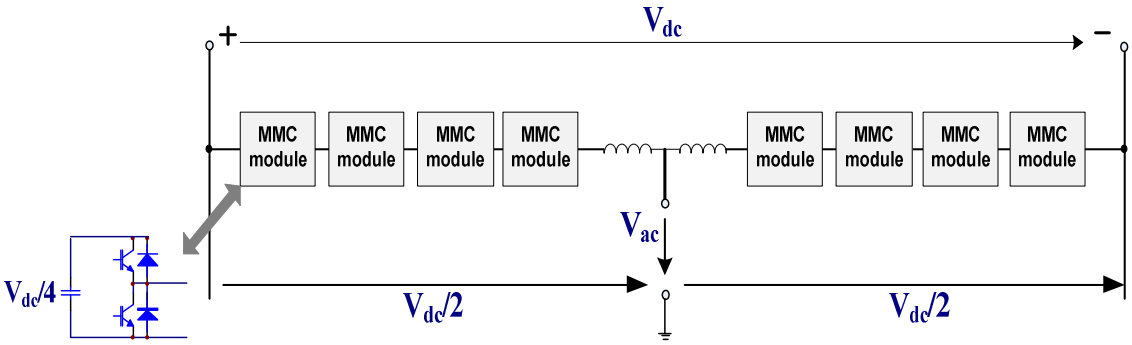


Fig. 1.15 Five-level modular multilevel converter

Fig. 1.15 shows a five-level MMC topology. The phase leg is divided into two equal arms, which can generate equal number of positive and negative levels at the AC output. In each MMC module, the two switches can connect or bypass its capacitor to the total capacitor array of the leg so as to generate a multilevel waveform. Since the capacitors in each module

are floating, the voltage balance control is required [31]. The advantages of the MMC are its modularity and scalability for the expansion to higher voltage and higher power and its unnecessity to use high voltage dc-link capacitors (or series-connected capacitors).

1.2.2.8 Active neutral-point-clamped (ANPC) converter

One major drawback of the 3L-NPC converter is the unequal power loss distribution among the semiconductor devices in the converter, which limits the maximum output power and switching frequency. In [15], it shows that the thermal design of a 3L-NPC converter is mainly determined by the four operating points given in Table 1-1. This issue can be solved by connecting an additional active switch in parallel to each NPC diode in the 3L-NPC converter, deriving the new three-level active NPC topology, as shown in Fig. 1.16.

Table 1-1 Operating points of a 3L-NPC converter with maximum unequal device power loss distribution

	Power factor	Modulation index	Most stressed semiconductor devices
Case 1	1 (inverter)	1.15	Outer switches
Case 2	1 (inverter)	0	NPC diodes
Case 3	-1 (rectifier)	1.15	Anti-parallel diodes of outer switches
Case 4	-1 (rectifier)	0	Inner switches

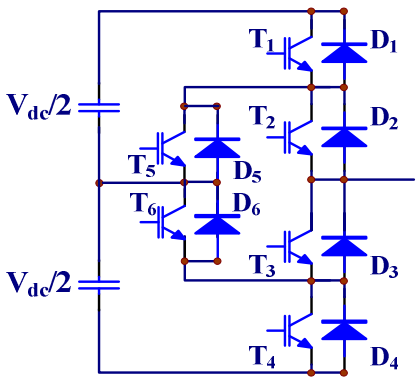


Fig. 1.16 Three-level active neutral-point-clamped (ANPC) converter

The output voltage levels and the switching states of a three-level ANPC converter are given in Table 1-2.

Table 1-2 Three-level ANPC converter output voltage levels and switching states

Output level	Switching Sequence					
	T1	T2	T3	T4	T5	T6
+ (V_{dc}/2)	1	1	0	0	0	1
0 (0U2)	0	1	0	0	1	0
0 (0U1)	0	1	0	1	1	0
0 (0L1)	1	0	1	0	0	1
0 (0L2)	0	0	1	0	0	1
– (-V_{dc}/2)	0	0	1	1	1	0

With the clamping switches, extra switching states are created to generate the “0” output level allowing the output current to go through the upper or lower clamping path. This allows for an improved distribution of the device conduction losses. Moreover, the communications to or from the new states “0U2”, “0U1” “0L2” and “0L1” determine the distribution of the device switching losses. For example, during the commutation from “+” to “0U2”, the phase current commutates to the upper path of the neutral tap. First, T_6 is turned off, then T_1 is turned off and finally T_5 is turned on after a dead time. During the commutation, T_1 experiences switching losses. During the commutation from “+” to “0L1”, the phase current commutates to the lower path of the neutral tap. During this commutation, T_1 remains in the on-state. T_2 is turned off and T_3 is turned on after a dead time, and T_2 experiences switching losses. Table 1-3 shows the distribution of the device switching losses for all commutations [15]. With the additional active NPC switches, the conduction losses and switching losses of the semiconductors devices can be adjusted by choosing a proper zero switching state. Therefore, a substantial increase in the maximum output power and switching frequency can be achieved.

Table 1-3 Device switching losses in the three-level active NPC converter

	T_1	D_1	T_2	D_2	T_3	D_3	T_4	D_4	T_5	D_5	T_6	D_6
Positive phase current												
+ ↔0U2	√									√		
+ ↔0U1	√									√		
+ ↔0L1			√			√						
+ ↔0L2	√					√						
0U2↔-			√					√				
0U1↔-			√			√						
0L1↔-								√			√	
0L2↔-								√			√	
Negative phase current												
+ ↔0U2		√							√			
+ ↔0U1		√							√			
+ ↔0L1				√	√							
+ ↔0L2		√			√							
0U2↔-				√			√					
0U1↔-				√	√							
0L1↔-							√					√
0L2↔-							√					√

Recently, a five-level ANPC converter has been introduced in [32], which combines a three-level ANPC leg with a three-level FC cell connected between the internal ANPC switching devices, as shown in Fig. 1.17. The floating capacitor voltage is controlled to $V_{dc}/4$ using redundant switching states. Adding more FC cells to the five-level ANPC converter enables the converter to reach a higher number of levels easily. Moreover, since the DC link is a 3L-NPC structure, the voltage balancing issue of the dc-link capacitors for an NPC converter with higher number of levels can be avoided.

Three-level and five-level ANPC converters have been successfully introduced to industry in the last five years. PCS8000, a three-level ANPC converter with back-to-back configuration, is applied to the AC excitation system for pump storage plants, covering a power range from 20 to 200 MVA [33] [34]. The ACS2000, a five-level ANPC converter

product introduced by ABB recently [35], is based on HV-IGBT technology. It aims at lower power MV drives, and is available from 0.4 to 1 MVA, rated at 6 to 6.9 kV in a back-to-back configuration.

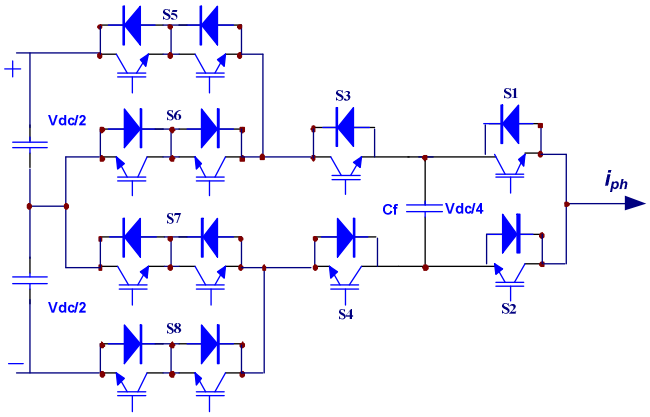


Fig. 1.17 Five-level active NPC converter

1.2.3 Applications of Multilevel Converters

Multilevel converters are considered as the state-of-the-art solution for medium voltage, high power applications today. Several major manufacturers have commercialized NPC, FC and CHB converters with different control methods for various applications. Particularly, the NPC topology has been widely used in the high-power AC drives like pumps, fans, mills, and so on [36] [37]. The back-to-back configuration of the NPC topology is used in regenerative conveyors for the mining industry [38] and grid interfaces for renewable energy sources like wind power [39] [40]. On the other hand, FC converters have found their place in the market for high bandwidth, high switching frequency applications, such as medium-voltage traction drives [41]. CHB converters have been successfully commercialized for very high power and power quality demanding applications up to a range of 31 MVA due to the series expansion capability. This topology has also been reported for active filter and reactive power

compensation applications [42], electric and hybrid vehicles [43] [44], photovoltaic power conversion [45] and uninterruptible power supplies [46]. A summary of multilevel converter-driven applications is illustrated in Fig. 1.18 [11].

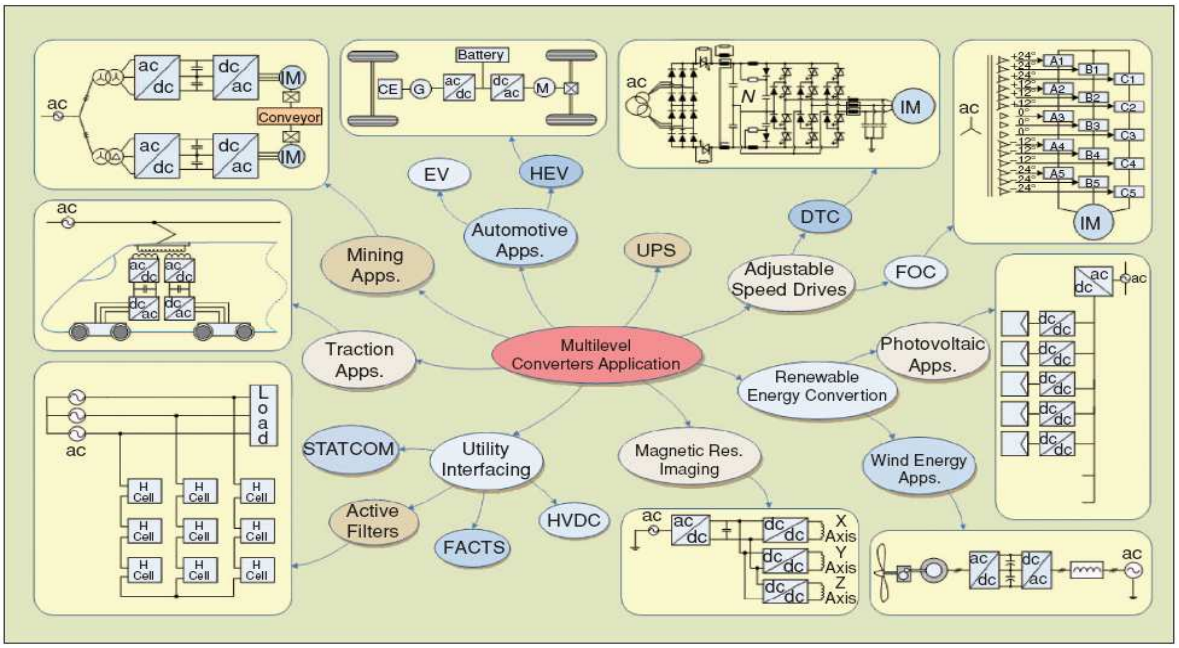


Fig. 1.18 Applications of multilevel converters

1.3 Motivation and the Dissertation Outline

Among various multilevel converters, active neutral-point-clamped (ANPC) converter is one of the most emerging multilevel technologies. Currently, the main research topics on ANPC converters include loss balancing algorithms, new converter topologies and control schemes. Some research and work on ANPC converters have been reported. However, further explorations are still needed on the new topology, control, features of ANPC converters as well as the promising applications in industry areas. The purpose of this dissertation is to further develop the design, topology, control and characteristics of

multilevel ANPC converters in high power applications, such as large wind turbine systems and high power motor drive systems.

Based on the flow of the contributions, this dissertation is divided into six chapters:

In Chapter 2, the concept of ETO Light NPC and ANPC Power Electronics Building Blocks (PEBB) is proposed. The electrical design and thermal analysis of the PEBBs are presented with detailed analytical equation derivations. The component physical arrangement of the ETO Light stack is also discussed to achieve the optimal stray inductance. The system configurations with the proposed ETO Light PEBBs are identified for the MW-level wind turbine systems. The thermal performance of the ETO Light NPC and ANPC PEBBs is studied for the 5 MW and 7 MW wind turbine systems, respectively.

In Chapter 3, the fault tolerant capability of the 3L-ANPC converter is analyzed for the single device open and short failure conditions first. The control strategies are proposed to enable the continuous operating of the 3L-ANPC converter under any single device failure condition. The requirement of the fault detection time is also discussed. Furthermore, the fault tolerant operation of the 3L-ANPC converter under multiple device open and short failure conditions is studied. Both simulation and experiment results prove the fault tolerant ability of the 3L-ANPC converter. A comprehensive reliability comparison for the 3L-NPC and 3L-ANPC converters is investigated. The results show that the 3L-ANPC converter has higher reliability than the 3L-NPC converter for motor drive applications. For grid-connected applications, the reliability of the 3L-NPC and 3L-ANPC converters is almost the same for single and multiple device open failure conditions. However, for single and multiple device short failure, the 3L-NPC converter has higher reliability than the 3L-ANPC converter.

Finally, the control schemes are proposed for the 3L-ANPC converter when it is applied on the generator side of a direct-driven PMSG based large wind turbine system. Besides the better loss balancing in devices, the fault tolerant ability of the 3L-ANPC converter also allows the wind turbine to remain in service and continue providing real power under device failure conditions. The simulation results are provided to verify the proposed control schemes for a 5MW wind turbine system.

In Chapter 4, a new 9-level ANPC converter is proposed for the next generation PEBB technology for power quality improvement in high power applications. The new 9-level ANPC converter combines the 5L-ANPC PEBB and HBBB together to generate a 9-level waveform. The converter operating principles and control, as well as the floating capacitor voltage balance scheme are presented in detail. The hybrid converter concept, which employs different types of power devices, is discussed for the new 9-level converter. Simulation and experiment results validate the proposed converter concept. The new 9-level ANPC topology is also compared with other conventional 9-level converters and existing 9-level ANPC converters from several aspects. The results show that the new ANPC converter shows better overall performance. Finally, the proposed 9-level converter is applied on the grid side of a 6 MW wind turbine system to achieve a filterless grid connection. The simulation results prove that the harmonic limit of the utility standards can be satisfied even without using a grid passive filter, which implies that the cost, efficiency, power density and reliability of the wind turbine system can be improved.

In Chapter 5, a simplified space vector-based current controller for any general N-level converters is proposed. In this current controller, the mapping techniques between the

subhexagon of the N-level converter and the hexagon of the two-level converter is used to identify the proper output voltage vector to suppress harmonic current content in steady state and obtain fast current response in transient state. Moreover, due to the existence of the redundant switching states in the N-level converter, the optimum switching state and switching sequence can be selected to meet the specific control requirements, such as the floating capacitor voltage control, power losses balance in the devices, and so on. The proposed current controller does not require the calculation of the back EMF voltage of the load, and the controller implementation is greatly simplified due to the use of very simple lookup tables, therefore it can be easily extended to any general N-level converter. The generalized procedures of the proposed current controller for any N-level converter are summarized. The current controller is explained and simulated on a five-level ANPC converter in a motor drive system, and the simulation results prove its correctness.

In Chapter 6, the conclusions for this dissertation are drawn and the future work is proposed.

Chapter 2 Electrical Design and Thermal Analysis of ETO Light Power Electronics Building Blocks (PEBB)

2.1 Electrical Design of ETO Light PEBBs

2.1.1 Emitter Turn-off (ETO) Thyristor

The emitter turn-off (ETO) thyristor is one of the state-of-the-art high power semiconductor devices, which are suitable for high power and high frequency applications. By optimally integrating the commercial GTO thyristor, power MOSFET and a specially designed control circuit, the ETO thyristor has the advantages of fast switching speed, low on-state voltage drop, and high current turn-off capability. The latest version of the ETO thyristor (Gen-4 ETO) is much more reliable and intelligent. It has some unique features including its built-in voltage, current and temperature sensors, control power self-generation capability, and true optical controlled turn-on and turn-off [47]. Fig. 2.1 shows the simplified equivalent circuit and a photo of a 4500V/4000A Gen-4 ETO thyristor.

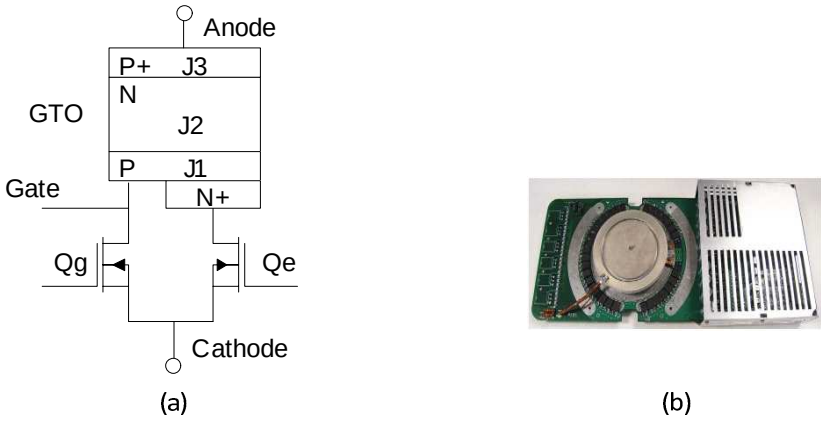


Fig. 2.1 Gen-4 ETO thyristor at 4.5kV/4kA (a) simplified equivalent circuit (b) photo

2.1.2 ETO Light PEBBs

2.1.2.1 Configuration of the ETO Light PEEBs

The circuit diagrams of the proposed ETO Light NPC PEBB and ANPC PEBB are shown in Fig. 2.2 and Fig. 2.3, respectively. These PEBBs can be used in various frequency converters like STATCOMs, MV drives and wind power converters.

In the proposed PEBBs, the switching devices are Gen-4 ETOs. The anti-parallel diodes, the NPC diodes and the clamp circuit diodes are ABB fast recovery diode 5SDF 10H4502. The snubber inductor L is used to limit the di/dt at turn-on of the ETOs, and the RCD clamp circuit is used to limit the overvoltage at turn-off of the ETOs. The snubber and clamp circuit are placed at both the positive and negative DC bus of the ETO Light PEBBs.

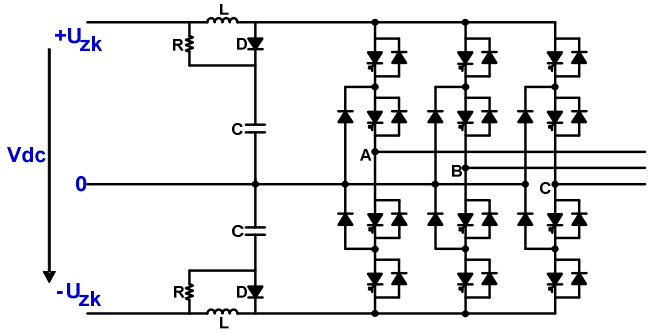


Fig. 2.2 Circuit diagram of ETO Light NPC PEBB

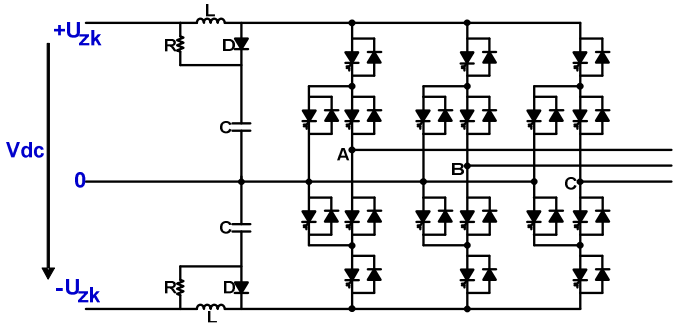


Fig. 2.3 Circuit diagram of ETO Light ANPC PEBB

2.1.2.2 Electrical parameters of the ETO Light PEBBs' components

Based on the voltage rating of the ETOs and diodes, the proposed ETO Light PEBBs are designed for a nominal line-to-line output RMS voltage of 3.3 kV.

The relationship between the DC bus voltage V_{dc} and the line-to-line output RMS voltage $V_{l\text{-}l,\,rms}$ is given by:

$$V_{l-l,\,rms} = 0.612 \cdot m \cdot V_{dc} \tag{2-1}$$

Here, "*m*" is modulation index ranging from 0 ~ 1.15.

According to (2-1), the required minimum DC bus voltage is:

$$V_{dc,\,\min} = 3.3kV / (1.15 \times 0.612) = 4685\,V \tag{2-2}$$

Finally, V_{dc} is selected to be 5 kV, which allows a 6% DC bus voltage margin for better dynamic characteristics.

To determine the parameters of *L*, *R* and *C* for the snubber and clamp circuit, the design rules are given below [48]:

$$L = (V_{dc} / 2) / (di / dt) \tag{2-3}$$

$$C = (1.1 \sim 1.3)L \tag{2-4}$$

$$R = (0.6 \sim 1.1)\sqrt{L / C} \tag{2-5}$$

Here, *di/dt* is the anti-parallel diode decay rate of the on-state current, and according to the datasheet [49], the maximum *di/dt* of the diode 5SDF 10H4502 is 650 A/μs.

Finally, the parameters are determined to be L=4 μH, C=5.2 μF and R=0.65 Ω. The simulation waveforms of the clamp capacitor voltage and the clamp circuit reset time at 2 kA peak current test condition are shown in Fig. 2.4. As seen, the peak clamp capacitor voltage is around 3.34 kV and the clamp circuit reset time is around 14 μs.

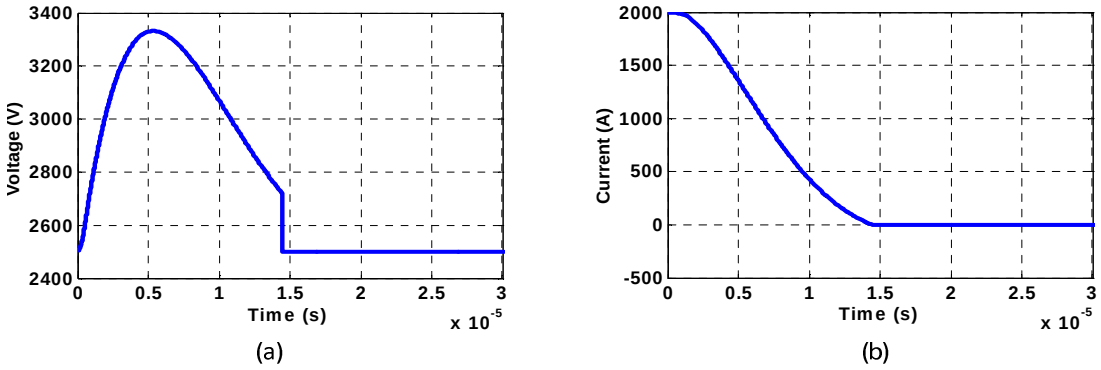


Fig. 2.4 Simulation waveform of the snubber and clamp circuit of ETO Light PEBBs at I_{peak}=2 kA (a) clamp capacitor voltage (b) clamp circuit reset time

2.1.2.3 Design of ETO Light stack

Each of the proposed ETO Light PEBBs is composed of three stacks. The electrical circuit diagram and component physical arrangement of the ETO Light NPC stack and ETO Light ANPC stack are shown in Fig. 2.5 and Fig. 2.6, respectively.

Considering the cost, reliability and compact structure, a heat pipe based air cooling system is used to remove the heat from the proposed ETO Light stack. The use of heat pipes allows us to avoid the drawbacks of conventional water cooling system, such as the need of good electrical isolation, elaborate pipes and heat exchangers maintenance. The power density and reliability of the ETO Light PEBBs are also improved by using less pipes and components. A customized heat pipe with 2.2 kW heat removal capability is used for ETO Light PEBBs. Fig. 2.7 shows a photo of the ETO thyristor with double-side heat pipe cooling.

The main components of the ETO Light NPC stacks and ANPC stacks are summarized in Table 2-1.

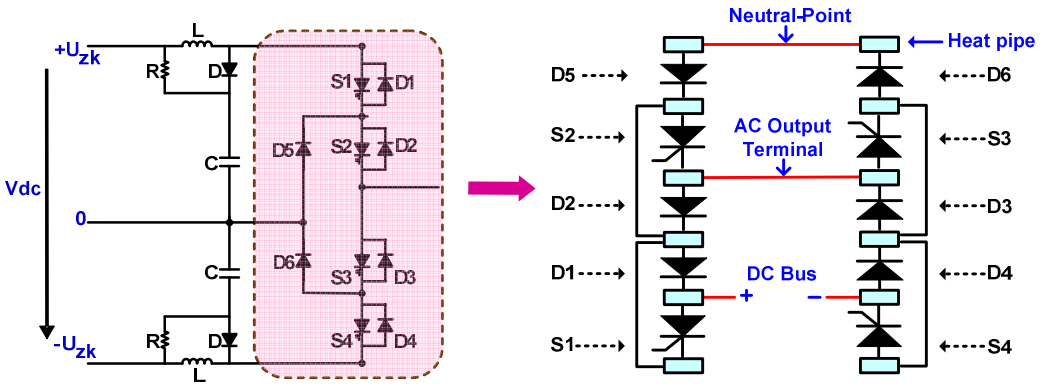


Fig. 2.5 Circuit diagram and component physical arrangement of ETO Light NPC stack

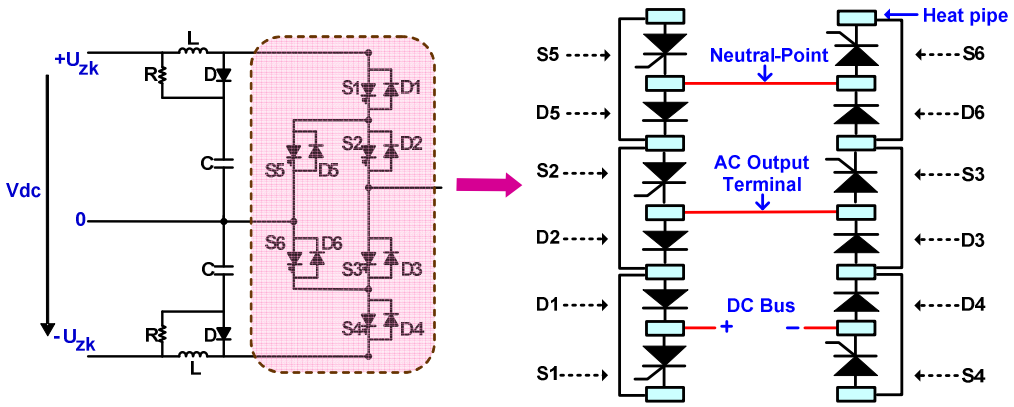


Fig. 2.6 Circuit diagram and component physical arrangement of ETO Light ANPC stack

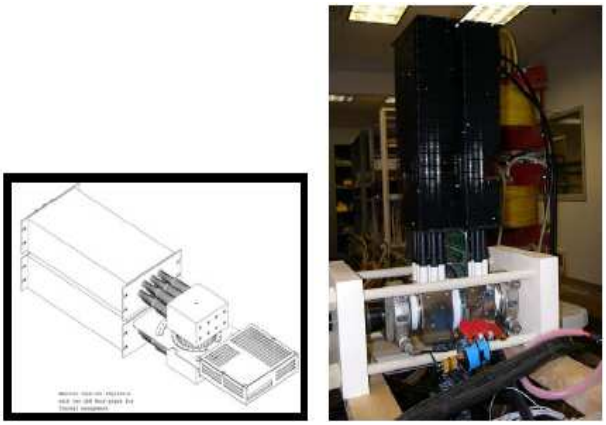
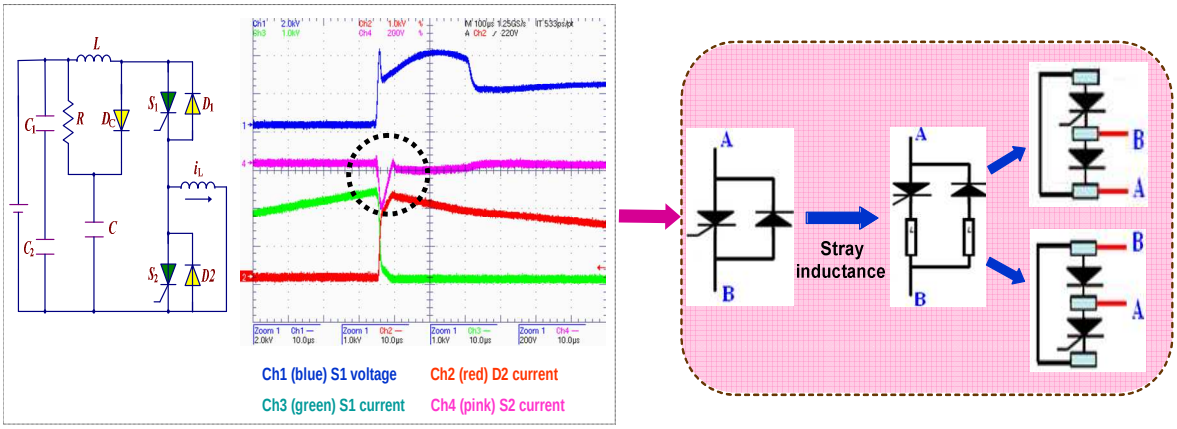


Fig. 2.7 Photo of ETO device with double-side heat pipe cooling

Table 2-1 Main components of the ETO Light Stacks

ETO Light stack	Number of components		
	Gen-4 ETO	Diode 5SDF 10H4502	Heat pipe
NPC stack	4	6	12
ANPC stack	6	6	14

For the component arrangement of the ETO Light stack, one basic principle is to obtain optimal and useful stray inductance. The experiment test results of the ETO-based half-bridge are shown in Fig. 2.8 (a).



(a) (b)

Fig. 2.8 Component physical arrangement for optimal and useful stray inductance (a) experiment test results of ETO-based half-bridge (b) two solutions for the component arrangement of ETO Light stack

When the load current commutates from the ETO to diode, the induced voltage on the loop inductance in series with the diode will be applied to the ETO together with the diode forward recovery voltage. This voltage can cause a certain amount of negative current to flow through the ETO. If any attempt is made to turn on the ETO during that period, the ETO may fail due to the junction breakdown. The reverse current through the ETO is not completely avoidable, however its amplitude and tail can be reduced by proper component

arrangement to increase the loop inductance in series with the ETO and decrease the loop inductance in series with the anti-parallel diode.

By studying all the possible component arrangement methods, two solutions for the ETOs and their anti-parallel diode arrangement are shown in Fig. 2.8 (b), and are finally used in the proposed ETO Light NPC and ANPC stacks.

2.2 Power Loss and Thermal Analysis of ETO Light PEBBs

In this section, the methodologies for power loss and thermal analysis of ETO Light NPC and ANPC PEBBs are presented. The detailed analytical equations are derived.

2.2.1 Methodology for Power Loss Calculation of ETO Light PEBBs

2.2.1.1 Power loss characteristics of the devices

The device power losses consist of switching loss and conduction loss. Switching loss includes turn-on loss and turn-off loss. Due to the use of the di/dt inductor, ETO turn-on loss is small and can be neglected.

Under junction temperature of 125°C, the turn-off energy per pulse at 2.5kV DC bus voltage and the on-state voltage of Gen-4 ETO, as shown in Fig. 2.9, are expressed by:

$$E_{off}(I) = a \times I + b = 0.0041 \times I + 0.21 \quad \textbf{(2-6)}$$

$$V_{on}(I) = c \times I + d = 0.0014 \times I + 1.1 \quad \textbf{(2-7)}$$

Here, E_{off} *(I)* is the ETO turn-off energy in Joule, V_{on} *(I)* is the ETO on-state voltage in Volts, and I is the current in Ampere.

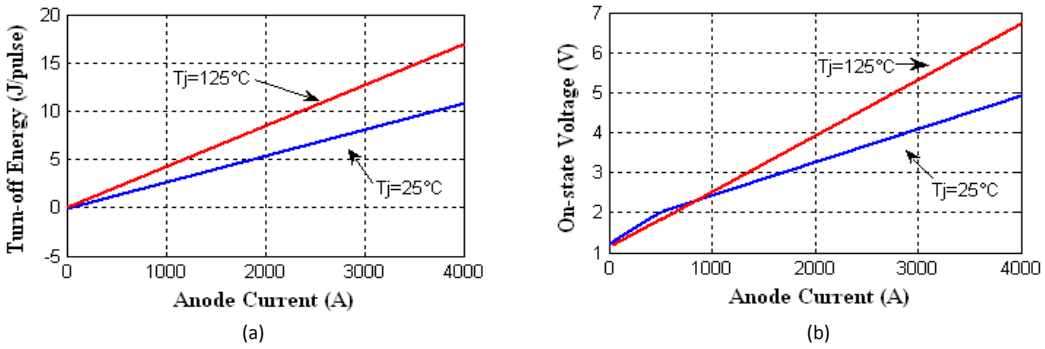


Fig. 2.9 Experiment test curve of Gen-4 ETO power loss characteristics at junction temperature of 125°C (a) turn-off energy per pulse at 2.5kV DC bus voltage (b) on-state voltage

Similarly, under junction temperature of 125°C, the power loss characteristics of the diode 5SDF 10H4502 are expressed by [50]:

$$E_{switching}(I) = e \times I + f = 0.00018 \times I + 0.8 \quad \textbf{(2-8)}$$

$$V_{on}(I) = g \times I + h = 5.674 \cdot 10^{-4} \times I + 2.307 \quad \textbf{(2-9)}$$

Here, $E_{switching}\ (I)$ is the diode turn-off energy in Joule including the diode's turn-off energy and reverse recovery energy. $V_{on}\ (I)$ is the diode on-state voltage in Volts.

2.2.1.2 Analytical power loss equations of ETO Light PEBBs

First, the assumptions for the power loss calculation of ETO Light PEBBs are that 1) the sine-triangle PWM is used; 2) 3rd harmonic voltage is injected; 3) switching frequency is 10 times larger than fundamental frequency.

The reference voltage and load current are expressed by:

$$V_{ref} = m \cdot \cos(wt) - \frac{1}{6} m \cdot \cos(3wt) \quad \textbf{(2-10)}$$

$$I = I_{amp} \cdot \cos(\alpha) = I_{amp} \cdot \cos(wt - \varphi) \quad \textbf{(2-11)}$$

Here, m is modulation index, I_{amp} is the load current amplitude, w is the fundamental angular frequency, α is the load current phase angle and φ is the load impedance angle.

The switching loss P_{sw} and conduction loss P_{cond} of ETO thyristor are expressed by:

$$P_{sw} = f_{sw} \cdot \frac{1}{2\pi} \cdot \int_0^{2\pi} E_{off}(I) \cdot d\alpha \tag{2-12}$$

$$P_{cond} = \frac{1}{2\pi} \cdot \int_0^{2\pi} I \cdot V_{on}(I) \cdot D(\alpha) \cdot d\alpha \tag{2-13}$$

The total power loss P_{loss} of ETO thyristor is:

$$P_{loss} = P_{sw} + P_{cond} \tag{2-14}$$

Here, f_{sw} is the device switching frequency, α is the load current phase angle, ranging from 0 ~ 2π, and $D(\alpha)$ is the device switching duty cycle. Similarly, the diode power losses can be calculated by the same method.

1. Analytical power loss equations for ETO Light NPC PEBB

The modulation signals, output phase and line-to-line voltages are shown in Fig. 2.10.

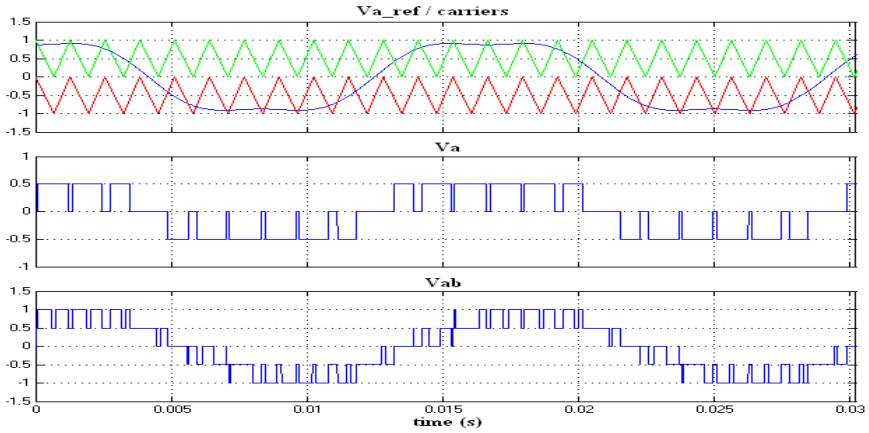


Fig. 2.10 Modulation and voltage waveforms of ETO Light NPC PEBB

Due to the symmetric structure of NPC topology, the switching loss, duty cycle and conduction loss of S_1 and S_4 are the same. The conclusion is also true for other pairs of devices (S_2 & S_3, D_1 &D_4, D_2 &D_3, D_5 & D_6).

According to (2-12) ~ (2-14), the switching losses of S_1, S_2, D_1, D_2 and D_5 are given by:

$$P_{sw\_S1} = f_{sw} \cdot \frac{1}{2\pi}\left[a \cdot I_{\text{amp}} \cdot (1+\cos\varphi) + b \cdot (\pi - |\varphi|) \right] \tag{2-15}$$

$$P_{sw\_S2} = f_{sw} \cdot \frac{1}{2\pi}\left[a \cdot I_{\text{amp}} \cdot (1-\cos\varphi) + b \cdot |\varphi| \right] \tag{2-16}$$

$$P_{sw\_D1} = f_{sw} \cdot \frac{1}{2\pi}\left[e \cdot I_{\text{amp}} \cdot (1-\cos\varphi) + f \cdot |\varphi| \right] \tag{2-17}$$

$$P_{sw\_D2} = 0 \tag{2-18}$$

$$P_{sw\_D5} = f_{sw} \cdot \frac{1}{2\pi}\left[e \cdot I_{\text{amp}} \cdot (1+\cos\varphi) + f \cdot (\pi - |\varphi|) \right] \tag{2-19}$$

The duty cycles of S_1, S_2, D_1 (D_2) and D_5 are expressed by:

$$d_{S1} = \begin{cases} m \cdot \cos(wt) - \frac{1}{6} m \cdot \cos(3wt), & wt \in \left[0, \frac{\pi}{2}\right] and \left[\frac{3\pi}{2}, 2\pi\right] \\ 0, & wt \in \left[\frac{\pi}{2}, \frac{3\pi}{2}\right] \end{cases} \tag{2-20}$$

$$d_{S2} = \begin{cases} 1 + m \cdot \cos(wt) - \frac{1}{6} m \cdot \cos(3wt), & wt \in \left[\frac{\pi}{2}, \frac{3\pi}{2}\right] \\ 1, & wt \in \left[0, \frac{\pi}{2}\right] and \left[\frac{3\pi}{2}, 2\pi\right] \end{cases} \tag{2-21}$$

$$d_{D1,\,D2} = \begin{cases} m \cdot \cos(wt) - \frac{1}{6} m \cdot \cos(3wt), & wt \in \left[\frac{3\pi}{2}, \frac{3\pi}{2} + \phi\right] \\ 0, & wt \in \left[0, \frac{3\pi}{2}\right] and \left[\frac{3\pi}{2} + \phi, 2\pi\right] \end{cases} \tag{2-22}$$

$$d_{D5} = \begin{cases} 1 - m \cdot \cos(wt) + \frac{1}{6} m \cdot \cos(3wt), & wt \in \left[0, \frac{\pi}{2}\right] and \left[\frac{3\pi}{2} + \phi, 2\pi\right] \\ 1 + m \cdot \cos(wt) - \frac{1}{6} m \cdot \cos(3wt), & wt \in \left[\frac{\pi}{2}, \frac{\pi}{2} + \phi\right] \\ 0, & wt \in \left[\frac{\pi}{2} + \phi, \frac{3\pi}{2} + \phi\right] \end{cases} \tag{2-23}$$

The conduction losses of S_1, S_2, D_1 (D_2) and D_5 are:

$$P_{cond\_S1}=\frac{1}{2\pi}\left[\begin{array}{l}\frac{c\cdot I_{amp}{}^2\cdot m}{2}\cdot\left(\frac{7}{30}\cdot\cos(2\varphi)+\frac{19}{18}+\frac{4}{3}\cdot\cos(\varphi)-\frac{4}{90}\cdot\cos(3\varphi)\right)\\+d\cdot I_{amp}\cdot m\cdot\left(\frac{9}{16}\cdot\sin|\varphi|+\frac{\pi-|\varphi|}{2}\cdot\cos(\varphi)-\frac{1}{48}\cdot\sin(3|\varphi|)\right)\end{array}\right] \quad \textbf{(2-24)}$$

$$P_{cond\_S2}=\frac{1}{2\pi}\left[\begin{array}{l}\frac{c\cdot I_{amp}{}^2}{2}\cdot\pi+2\cdot d\cdot I_{amp}\\+\frac{c\cdot I_{amp}{}^2\cdot m}{2}\cdot\left(-\frac{7}{30}\cdot\cos(2\varphi)-\frac{19}{18}+\frac{4}{3}\cdot\cos(\varphi)-\frac{4}{90}\cdot\cos(3\varphi)\right)\\+d\cdot I_{amp}\cdot m\cdot\left(-\frac{9}{16}\cdot\sin|\varphi|+\frac{|\varphi|}{2}\cdot\cos(\varphi)+\frac{1}{48}\cdot\sin(3|\varphi|)\right)\end{array}\right] \quad \textbf{(2-25)}$$

$$P_{cond\_D1}=\frac{1}{2\pi}\left[\begin{array}{l}\frac{g\cdot I_{amp}{}^2\cdot m}{2}\cdot\left(\frac{7}{30}\cdot\cos(2\varphi)+\frac{19}{18}-\frac{4}{3}\cdot\cos(\varphi)+\frac{4}{90}\cdot\cos(3\varphi)\right)\\+h\cdot I_{amp}\cdot m\cdot\left(\frac{9}{16}\cdot\sin|\varphi|-\frac{|\varphi|}{2}\cdot\cos(\varphi)-\frac{1}{48}\cdot\sin(3|\varphi|)\right)\end{array}\right] \quad \textbf{(2-26)}$$

$$P_{cond\_D5}=\frac{1}{2\pi}\left[\begin{array}{l}\frac{g\cdot I_{amp}{}^2}{2}\cdot\pi+2\cdot h\cdot I_{amp}+\frac{g\cdot I_{amp}{}^2\cdot m}{2}\cdot\left(-\frac{7}{15}\cdot\cos(2\varphi)-\frac{19}{9}\right)\\+h\cdot I_{amp}\cdot m\cdot\left(-\frac{9}{8}\cdot\sin|\varphi|+\left(|\varphi|-\frac{\pi}{2}\right)\cdot\cos(\varphi)+\frac{1}{24}\cdot\sin(3|\varphi|)\right)\end{array}\right] \quad \textbf{(2-27)}$$

2. Analytical power loss equations of ETO Light ANPC PEBB

The PWM strategy and loss balancing method have a great impact on the loss distribution of semiconductor devices and thus affect the thermal performance of the ANPC converter. The main loss balancing schemes are summarized below.

- Feedback-controlled loss balancing scheme [51]

This scheme uses the same reference voltages and carrier signals as those of the conventional three-level NPC converter for the PWM modulation. However, it sends the

feedback signals of the load current, dc-link voltage and cooling water temperature to the built-in loss and thermal model. Based on this information, the losses and junction temperatures of the devices are calculated on-line, which is then used to select the proper commutations to keep the hottest devices as cool as possible, as shown in Fig. 2.11 (a). However, the real-time junction temperature calculation needs a fast digital controller such as a FPGA, and it also increases the control complexity.

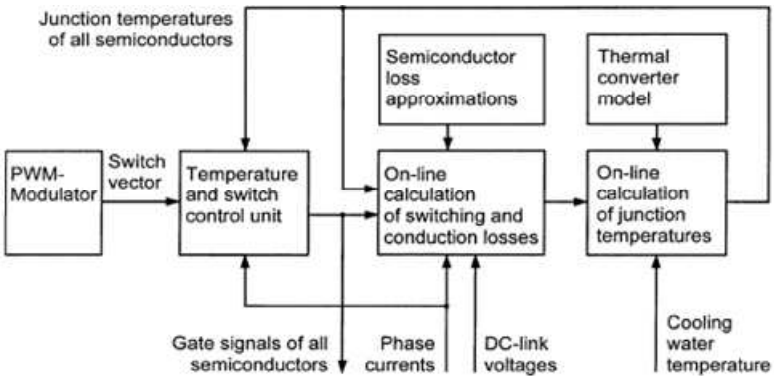
- Feedforward loss balancing scheme [52]

Different from the previous feedback-controlled scheme, feedforward loss balancing control calculates the device loss and junction temperature for all relevant operating points off-line by computer simulation instead of real-time calculation. The optimal ratios between different types of commutations, which are functions of modulation index and power factor, are stored in a lookup table. Finally the predefined ratio or sequence of commutations is implemented by a controller, as shown in Fig. 2.11 (b). This method is simpler, but the loss-balancing effect is not good for fast transient and abnormal load conditions. Moreover, it also requires the behavior of the modulation methods at all operating points to be predictable.

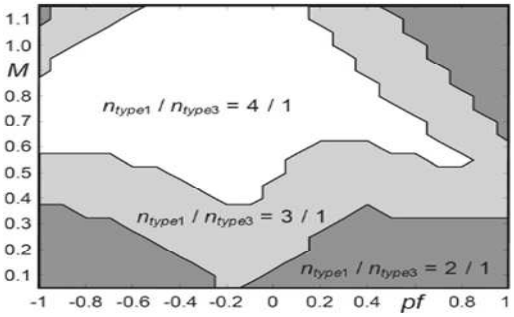
- Natural doubling-frequency loss balancing scheme [53]

In this scheme, the reference voltage S_r is compared with two carrier signals with 180° phase shift on the horizontal axis. Fig. 2.11 (c) shows the switching states and output voltage for the positive and negative half cycle of the reference voltage, respectively. These commutation sequences lead to a natural doubling of the apparent switching frequency. Each switch commutes at the switching frequency f_s and the output voltage has an apparent switching frequency equal to 2 f_s. The loss balancing effect of this method may not be as

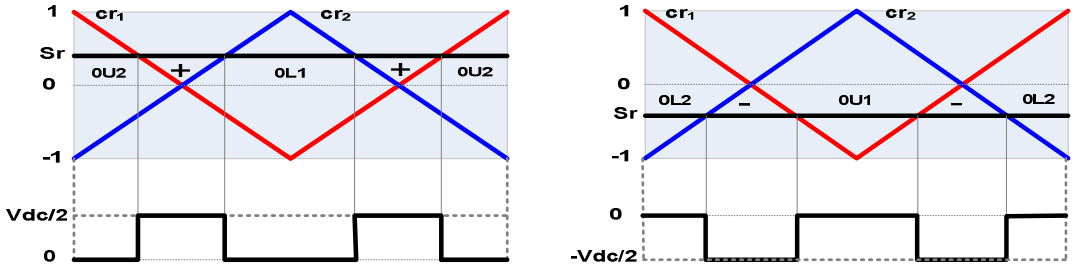
good as the other two schemes, since it uses completely natural commutations rather than those based on the converter operating points and feedback signals. However, it is easy to implement, and more convenient to derive the analytical equations for converter power loss calculation. So, we choose this method for the thermal analysis of ETO Light PEBB.



(a)



(b)



(i) Sr>0 (ii) Sr<0

(c)

Fig. 2.11 Loss balancing schemes of 3-level ANPC converter (a) feedback-controlled loss balancing scheme (b) feedforward loss balancing scheme (c) natural doubling-frequency loss balancing scheme

Due to the symmetric structure of the ANPC topology, the switching loss, duty cycle and conduction loss of S_1 and S_4 are the same. The conclusion is also true for other pairs of devices (S_2 & S_3, S_5 & S_6, D_1 &D_4, D_2 &D_3 and D_5 & D_6).

According to (2-12) ~ (2-14), the switching losses of S_1, S_2, S_6, D_1, D_2 and D_5 are:

$$P_{sw\_S1} = f_{sw} \cdot \frac{1}{2\pi}\left[a \cdot I_{\text{amp}} \cdot \left(1+\cos\varphi\right) + b \cdot \left(\pi - |\varphi|\right)\right] \quad \textbf{(2-28)}$$

$$P_{sw\_S2} = f_{sw} \cdot \frac{1}{2\pi}\left[a \cdot I_{\text{amp}} \cdot 2 + b \cdot \pi\right] \quad \textbf{(2-29)}$$

$$P_{sw\_S6} = f_{sw} \cdot \frac{1}{2\pi}\left[a \cdot I_{\text{amp}} \cdot \left(1-\cos\varphi\right) + b \cdot |\varphi|\right] \quad \textbf{(2-30)}$$

$$P_{sw\_D1} = f_{sw} \cdot \frac{1}{2\pi}\left[e \cdot I_{\text{amp}} \cdot \left(1-\cos\varphi\right) + f \cdot |\varphi|\right] \quad \textbf{(2-31)}$$

$$P_{sw\_D2} = f_{sw} \cdot \frac{1}{2\pi}\left[e \cdot I_{\text{amp}} \cdot 2 + f \cdot \pi\right] \quad \textbf{(2-32)}$$

$$P_{sw\_D5} = f_{sw} \cdot \frac{1}{2\pi}\left[e \cdot I_{\text{amp}} \cdot \left(1+\cos\varphi\right) + f \cdot \left(\pi - |\varphi|\right)\right] \quad \textbf{(2-33)}$$

The duty cycles of S_1, S_2, S_6, D_1, D_2 and D_5 are:

$$d_{S1} = \begin{cases} m \cdot \cos(wt) - \frac{1}{6} m \cdot \cos(3wt), & wt \in \left[0, \frac{\pi}{2}\right] and \left[\frac{3\pi}{2} + \phi, 2\pi\right] \\ 0, & wt \in \left[\frac{\pi}{2}, \frac{3\pi}{2} + \phi\right] \end{cases} \quad \textbf{(2-34)}$$

$$d_{S2} = \begin{cases} \frac{1}{2}\left[1 + m \cdot \cos(wt) - \frac{1}{6} m \cdot \cos(3wt)\right], & wt \in \left[0, \frac{\pi}{2} + \phi\right] and \left[\frac{3\pi}{2} + \phi, 2\pi\right] \\ 0, & wt \in \left[\frac{\pi}{2} + \phi, \frac{3\pi}{2} + \phi\right] \end{cases} \quad \textbf{(2-35)}$$

$$d_{S6}=\begin{cases}\frac{1}{2}\left[1-m\cdot\cos(wt)+\frac{1}{6}m\cdot\cos(3wt)\right], & wt\in\left[0,\frac{\pi}{2}\right]and\left[\frac{3\pi}{2}+\phi,2\pi\right]\\ \frac{1}{2}\left[1+m\cdot\cos(wt)-\frac{1}{6}m\cdot\cos(3wt)\right], & wt\in\left[\frac{\pi}{2},\frac{\pi}{2}+\phi\right]\\ 0, & wt\in\left[\frac{\pi}{2}+\phi,\frac{3\pi}{2}+\phi\right]\end{cases} \quad \textbf{(2-36)}$$

$$d_{D1}=\begin{cases}m\cdot\cos(wt)-\frac{1}{6}m\cdot\cos(3wt), & wt\in\left[\frac{3\pi}{2},\frac{3\pi}{2}+\phi\right]\\ 0, & wt\in\left[0,\frac{3\pi}{2}\right]and\left[\frac{3\pi}{2}+\phi,2\pi\right]\end{cases} \quad \textbf{(2-37)}$$

$$d_{D2}=\begin{cases}\frac{1}{2}\left[1+m\cdot\cos(wt)-\frac{1}{6}m\cdot\cos(3wt)\right], & wt\in\left[\frac{\pi}{2}+\phi,\frac{3\pi}{2}+\phi\right]\\ 0, & wt\in\left[0,\frac{\pi}{2}+\phi\right]and\left[\frac{3\pi}{2}+\phi,2\pi\right]\end{cases} \quad \textbf{(2-38)}$$

$$d_{D5}=\begin{cases}\frac{1}{2}\left[1-m\cdot\cos(wt)+\frac{1}{6}m\cdot\cos(3wt)\right], & wt\in\left[0,\frac{\pi}{2}\right]and\left[\frac{3\pi}{2}+\phi,2\pi\right]\\ \frac{1}{2}\left[1+m\cdot\cos(wt)-\frac{1}{6}m\cdot\cos(3wt)\right], & wt\in\left[\frac{\pi}{2},\frac{\pi}{2}+\phi\right]\\ 0, & wt\in\left[\frac{\pi}{2}+\phi,\frac{3\pi}{2}+\phi\right]\end{cases} \quad \textbf{(2-39)}$$

The conduction losses of S_1, S_2, S_6, D_1, D_2 and D_5 are:

$$P_{cond\_S1}=\frac{1}{2\pi}\left[\begin{array}{l}\frac{c\cdot {I_{amp}}^2\cdot m}{2}\cdot\left(\frac{7}{30}\cdot\cos(2\varphi)+\frac{19}{18}+\frac{4}{3}\cdot\cos(\varphi)-\frac{4}{90}\cdot\cos(3\varphi)\right)\\ +d\cdot I_{amp}\cdot m\cdot\left(\frac{9}{16}\cdot\sin|\varphi|+\frac{\pi-|\varphi|}{2}\cdot\cos(\varphi)-\frac{1}{48}\cdot\sin(3|\varphi|)\right)\end{array}\right] \quad \textbf{(2-40)}$$

$$P_{cond\_S2}=\frac{1}{2}\cdot\frac{1}{2\pi}\left[\begin{array}{l}\frac{c\cdot {I_{amp}}^2}{2}\cdot\pi+2\cdot d\cdot I_{amp}+d\cdot I_{amp}\cdot m\cdot\frac{\pi}{2}\cdot\cos(\varphi)\\ +\frac{c\cdot {I_{amp}}^2\cdot m}{2}\cdot\left(\frac{8}{3}\cdot\cos(\varphi)-\frac{4}{45}\cdot\cos(3\varphi)\right)\end{array}\right] \quad \textbf{(2-41)}$$

$$P_{cond\_S6}=\frac{1}{2}\cdot\frac{1}{2\pi}\left[\begin{array}{l}\frac{c\cdot I_{\max}{}^2}{2}\cdot\pi+2\cdot d\cdot I_{\max}+\frac{c\cdot I_{\max}{}^2\cdot m}{2}\cdot\left(-\frac{7}{15}\cdot\cos(2\varphi)-\frac{19}{9}\right)\\ +d\cdot I_{\max}\cdot m\cdot\left(-\frac{9}{8}\cdot\sin|\varphi|+\left(|\varphi|-\frac{\pi}{2}\right)\cdot\cos(\varphi)+\frac{1}{24}\cdot\sin(3|\varphi|)\right)\end{array}\right] \quad \textbf{(2-42)}$$

$$P_{cond\_D1}=\frac{1}{2\pi}\left[\begin{array}{l}\frac{g\cdot I_{amp}{}^2\cdot m}{2}\cdot\left(\frac{7}{30}\cdot\cos(2\varphi)+\frac{19}{18}-\frac{4}{3}\cdot\cos(\varphi)+\frac{4}{90}\cdot\cos(3\varphi)\right)\\ +h\cdot I_{amp}\cdot m\cdot\left(\frac{9}{16}\cdot\sin|\varphi|-\frac{|\varphi|}{2}\cdot\cos(\varphi)-\frac{1}{48}\cdot\sin(3|\varphi|)\right)\end{array}\right] \quad \textbf{(2-43)}$$

$$P_{cond\_D2}=\frac{1}{2}\cdot\frac{1}{2\pi}\left[\begin{array}{l}\frac{g\cdot I_{\max}{}^2}{2}\cdot\pi+2\cdot h\cdot I_{\max}+h\cdot I_{\max}\cdot m\cdot\left(-\frac{\pi}{2}\right)\cdot\cos(\varphi)\\ +\frac{g\cdot I_{\max}{}^2\cdot m}{2}\cdot\left(-\frac{8}{3}\cdot\cos(\varphi)+\frac{4}{45}\cdot\cos(3\varphi)\right)\end{array}\right] \quad \textbf{(2-44)}$$

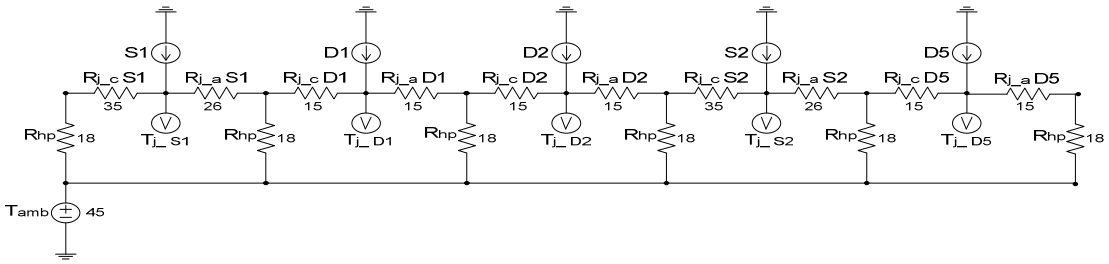
$$P_{cond\_D5}=\frac{1}{2}\cdot\frac{1}{2\pi}\left[\begin{array}{l}\frac{g\cdot I_{\max}{}^2}{2}\cdot\pi+2\cdot h\cdot I_{\max}+\frac{g\cdot I_{\max}{}^2\cdot m}{2}\cdot\left(-\frac{7}{15}\cdot\cos(2\varphi)-\frac{19}{9}\right)\\ +h\cdot I_{\max}\cdot m\cdot\left(-\frac{9}{8}\cdot\sin|\varphi|+\left(|\varphi|-\frac{\pi}{2}\right)\cdot\cos(\varphi)+\frac{1}{24}\cdot\sin(3|\varphi|)\right)\end{array}\right] \quad \textbf{(2-45)}$$

2.2.2 Methodology for Thermal Analysis of ETO Light PEBBs

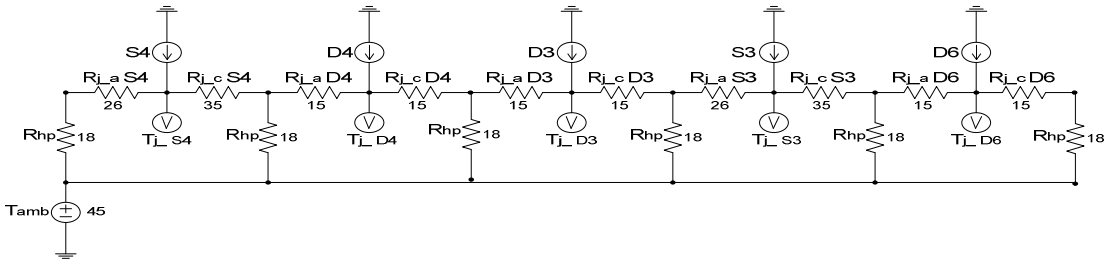
The output current and output power capability of the ETO Light PEBBs can be calculated based on the devices power losses and thermal impedance. In this study, a loop calculation is implemented to find the reasonable peak current at the peak output power point of the PEBBs. The procedure is described as follows. First, an initial current value is used to compute the thermal loss. Then, if the thermal loss is higher than the thermal limitation, the current will be decreased; otherwise, the current will be increased. Finally, a reasonable current will be found. The thermal limitation includes two aspects. First, the steady-state

junction temperatures of all the ETOs and diodes are below 125 °C. Second, the maximum power dissipation on the individual heat pipe must be lower than 2.2 kW.

To estimate the steady-state junction temperature of the devices of ETO Light PEBBs, the electrical-equivalent thermal network model needs to be constructed based on the physical arrangement of ETO Light stack. According to Fig. 2.5 and Fig. 2.6, the thermal network models of the ETO Light NPC and ANPC stacks are derived and shown in Fig. 2.12 and Fig. 2.13, respectively.



(a)

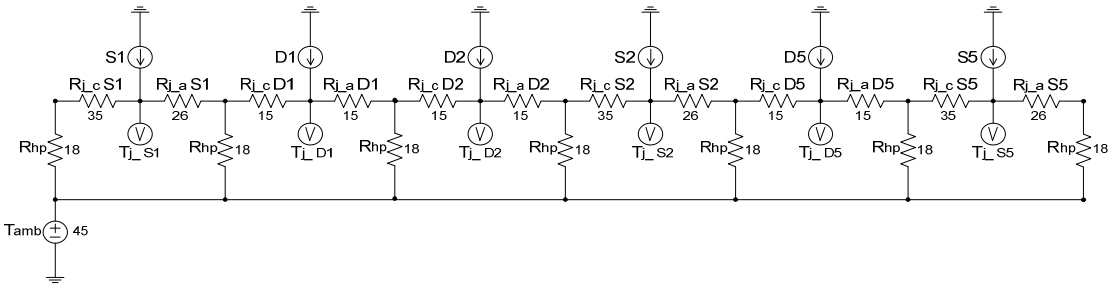


(b)

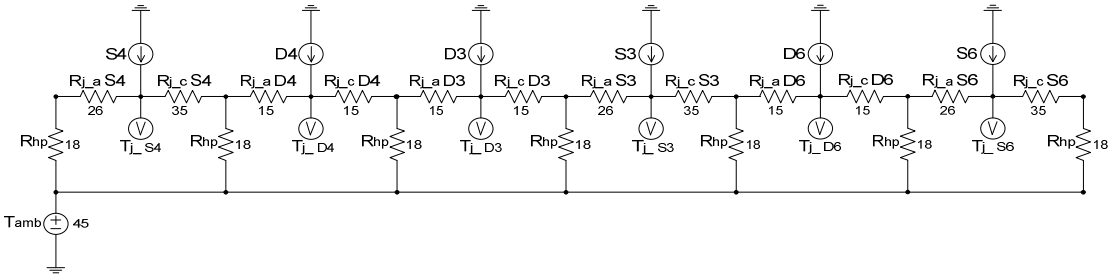
Fig. 2.12 Thermal network model of ETO Light NPC stack (a) left side of the single-pole stack (S_1, S_2, D_1, D_2, D_5) (b) right side of the single-pole stack (S_3, S_4, D_3, D_4, D_6)

The resistors represent the thermal resistances of the devices and heat pipes, the voltage source represents the ambient temperature, and the current sources represent the power losses on each device. The sum of the thermal resistances from junction to Anode and that from case to heatsink is donated as $R_{j\text{-}a}$. The sum of the thermal resistances from junction to

Cathode and that from case to heatsink is donated as $R_{j\text{-}c}$. R_{hp} represents the thermal resistance of the heat pipe from the contact point to the air, and it equals to 18 K/kW at 5 m/s flow rate of cooling air. The ambient temperature is 45 °C.



(a)



(b)

Fig. 2.13 Thermal network model of ETO Light ANPC stack (a) left side of the single-pole stack (S_1, S_2, S_5, D_1, D_2, D_5) (b) right side of the single-pole stack (S_3, S_4, S_6, D_3, D_4, D_6)

By simulating the above circuits using the simulation software like MATLAB, or solving the constructed equations based on the thermal network models, steady-state junction temperatures of the devices in ETO Light PEBBs can be obtained [54] [55].

2.2.3 Analysis Results and Comparison of ETO Light PEBBs

According to the methodologies for power loss calculation and thermal analysis discussed above, the ETO Light NPC and ANPC PEBBs are analyzed for generator operation (e.g. generator side converter operation in wind turbine system) and motor operation (e.g.

grid side converter operation in wind turbine system), respectively. The main calculation and simulation results and the comparison of ETO Light NPC and ANPC PEBBs are discussed below.

2.2.3.1 Analytical results of ETO Light PEBBs under generator mode

First, the ETO Light PEBBs are analyzed for working under generator mode. In this mode, the PEBBs will receive real power from power sources, such as generators. The main parameters and thermal performance results are shown in Table 2-2. The apparent switching frequency is selected to be 1 kHz, which is a proper choice for high power applications. Due to the natural doubling-frequency PWM strategy, the actual device switching frequency for ANPC PEBB is 500 Hz, which is half of the device switching frequency in NPC PEBB.

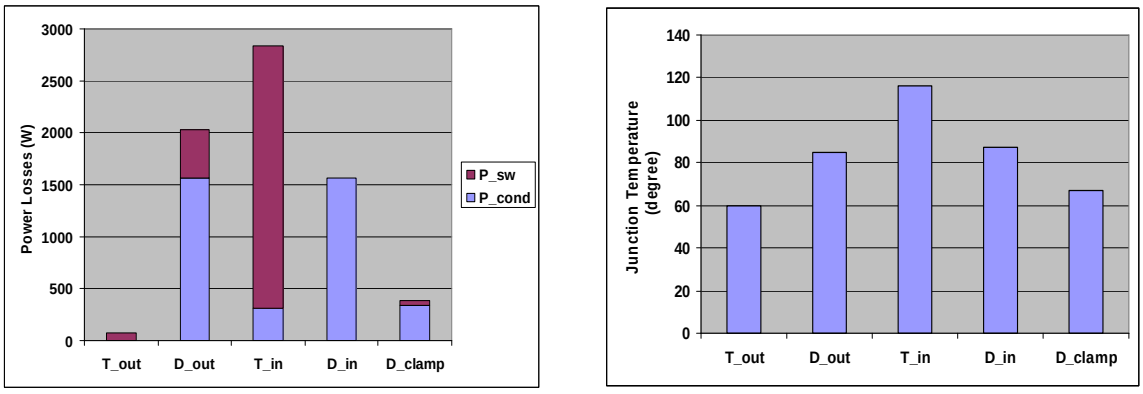
Table 2-2 Main parameters and thermal performance of ETO Light PEBBs under generator mode

DC voltage	5 kVDC	
Switching frequency	1 kHz (apparent f_{sw})	
Line-line RMS voltage	3.3 kVAC	
Power factor	cos (Φ)= -0.95	
Ambient temperature	45 °C	
	NPC PEBB	Active NPC PEBB
PWM modulation	SPWM with 3rd harmonic injection	Doubling-frequency PWM with 3rd harmonic injection
Modulation index	1.078	1.078
Peak RMS current	1.346 kA	1.539 kA
Peak output power	7.69 MVA	8.74 MVA
Total device losses	41.34 kW	47.61 kW
Maximum power loss on individual heat pipe	2.2 kW	2.2 kW

According to the results, it is observed that the maximum output power of ETO Light NPC and ANPC PEBBs is 7.69 MVA and 8.74 MVA respectively in generator mode. The ANPC PEBB produces 14% higher output power compared to the NPC PEBB, which is

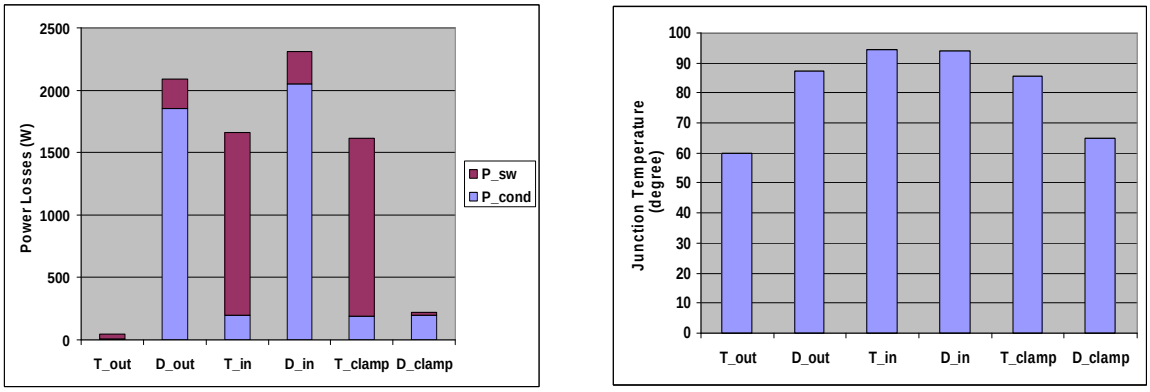
realized by managing the power losses among the devices to achieve a balanced distribution. Also, the maximum heat removal capability of the heat pipe is the thermal limitation in this mode. The maximum power loss on an individual heat pipe reaches the 2.2 kW limit before the steady-state junction temperature of the hottest device reaches 125 °C.

The device power losses and junction temperature of ETO Light NPC and ANPC PEBBs under generator mode at peak output power are show in Fig. 2.14 and Fig. 2.15, respectively.



(a) (b)

Fig. 2.14 Devices power loss and junction temperature distribution of ETO Light NPC PEBB under generator mode at peak output power (a) power loss distribution (b) junction temperature distribution



(a) (b)

Fig. 2.15 Devices power loss and junction temperature distribution of ETO Light ANPC PEBB under generator mode at peak output power (a) power loss distribution (b) junction temperature distribution

It can be found that hottest device junction temperature in an ANPC PEBB is much lower than that in an NPC PEBB. This implies that by using the heat pipes with more sufficient cooling capability or by using better loss balancing schemes, the peak output power rating of the ETO Light ANPC PEBB can be even higher.

2.2.3.2 Analytical results of ETO Light PEBBs under motor mode

Now, the ETO Light PEBBs are analyzed for working under motor mode. In this mode, the PEBBs will provide real power to loads, such as motor drives or utility grid. The main parameters and thermal performance results are shown in Table 2-3. Different from generator mode, the power factor is positive in this case.

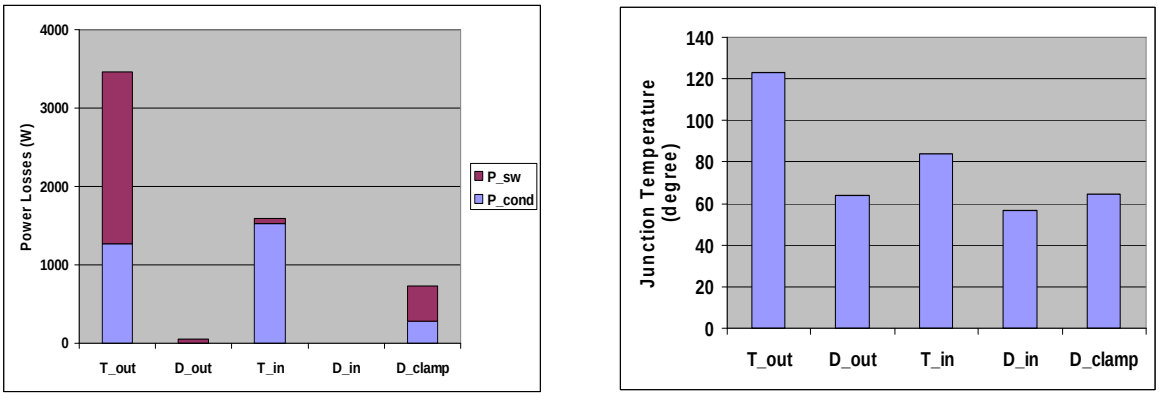
Table 2-3 Main parameters and thermal performance of ETO Light PEBBs under motor mode

DC voltage	5 kVDC	
Switching frequency	1 kHz (apparent f_{SW})	
Line-line RMS voltage	3.3 kVAC	
Power factor	cos (Φ)= 0.95	
Ambient temperature	45 °C	
	NPC PEBB	Active NPC PEBB
PWM modulation	SPWM with 3rd harmonic injection	Doubling-frequency PWM With 3rd harmonic injection
Modulation index	1.078	1.078
Peak RMS current	1.163 kA	1.478 kA
Peak output power	6.65 MVA	8.45 MVA
Total device losses	34.99 kW	47.38 kW
Maximum power loss on individual heat pipe	1.754 kW	1.974 kW

The calculation results show that the maximum output power of ETO Light NPC and ANPC PEBBs is 6.65 MVA and 8.45 MVA respectively in motor mode. Compared with NPC PEBB, an increased power of 27% is obtained with ANPC topology. The device power

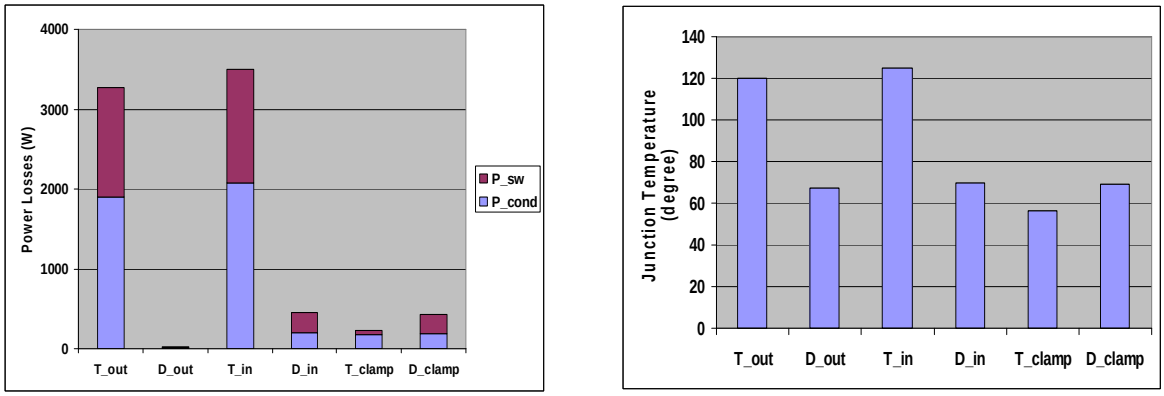
losses and junction temperature of ETO Light NPC and ANPC PEBBs under motor mode at peak output power are show in Fig. 2.16 and Fig. 2.17, respectively.

It is observed that the steady-state junction temperature of the ETO limits the PEBB thermal capability in this case. Moreover, with an improved loss balancing solution, the maximum output power of the ETO Light ANPC PEBB is able to increase further.



(a) (b)

Fig. 2.16 Devices power loss and junction temperature distribution of ETO Light NPC PEBB under motor mode at peak output power (a) power loss distribution (b) junction temperature distribution

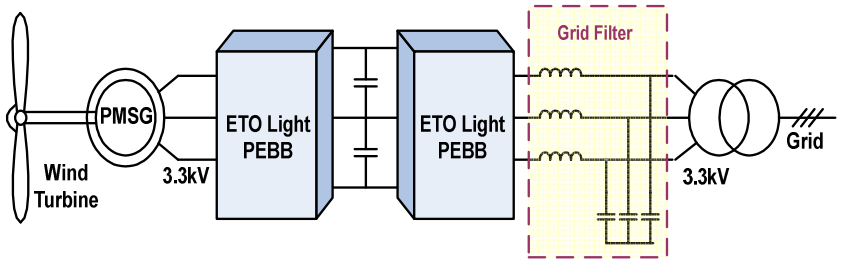


(a) (b)

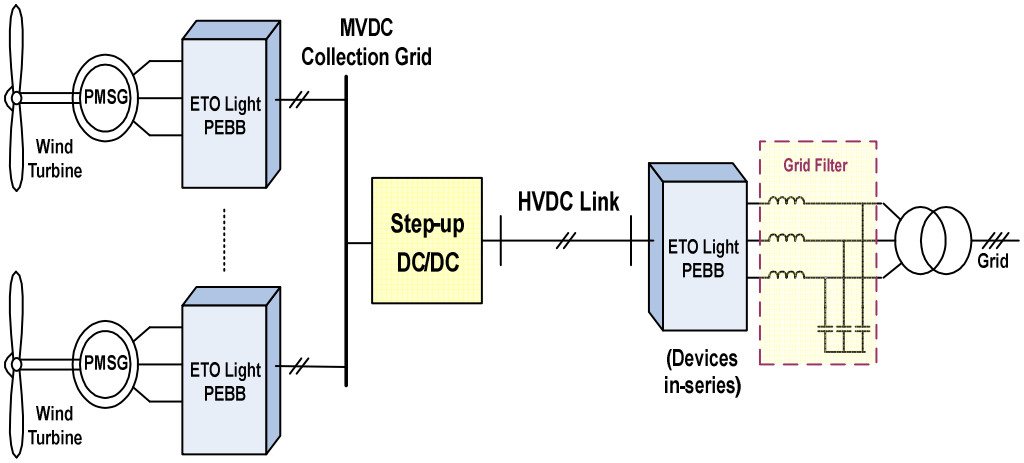
Fig. 2.17 Devices power loss and junction temperature distribution of ETO Light ANPC PEBB under motor mode at peak output power (a) power loss distribution (b) junction temperature distribution

2.2.4 ETO Light PEBBs for Large Wind Turbine Applications

The proposed ETO Light PEBBs can be used as the electrical interface, and applied in multi-MW wind turbine systems. Fig. 2.18 shows the typical system configurations for the large wind turbines with AC and DC transmission, respectively.



(a)



(b)

Fig. 2.18 Application of ETO Light PEBBs in direct-driven PMSG based wind turbine systems (a) configuration with AC transmission (b) configuration with DC transmission

Based on the calculated maximum output power rating of the ETO Light PEBBs, the NPC PEBB can support up to a 5 MW wind turbine, while the ANPC PEBB can be applied for a wind turbine rated for 7 MW. Fig. 2.19 and Fig. 2.20 show the detailed device power loss and junction temperature of the ETO Light NPC and ANPC PEBBs at 5 MW and 7 MW

operating point, respectively. The other parameters (DC bus voltage, modulation index, apparent switching frequency, power factor and ambient temperature) are the same as those in Table 2-2 and Table 2-3.

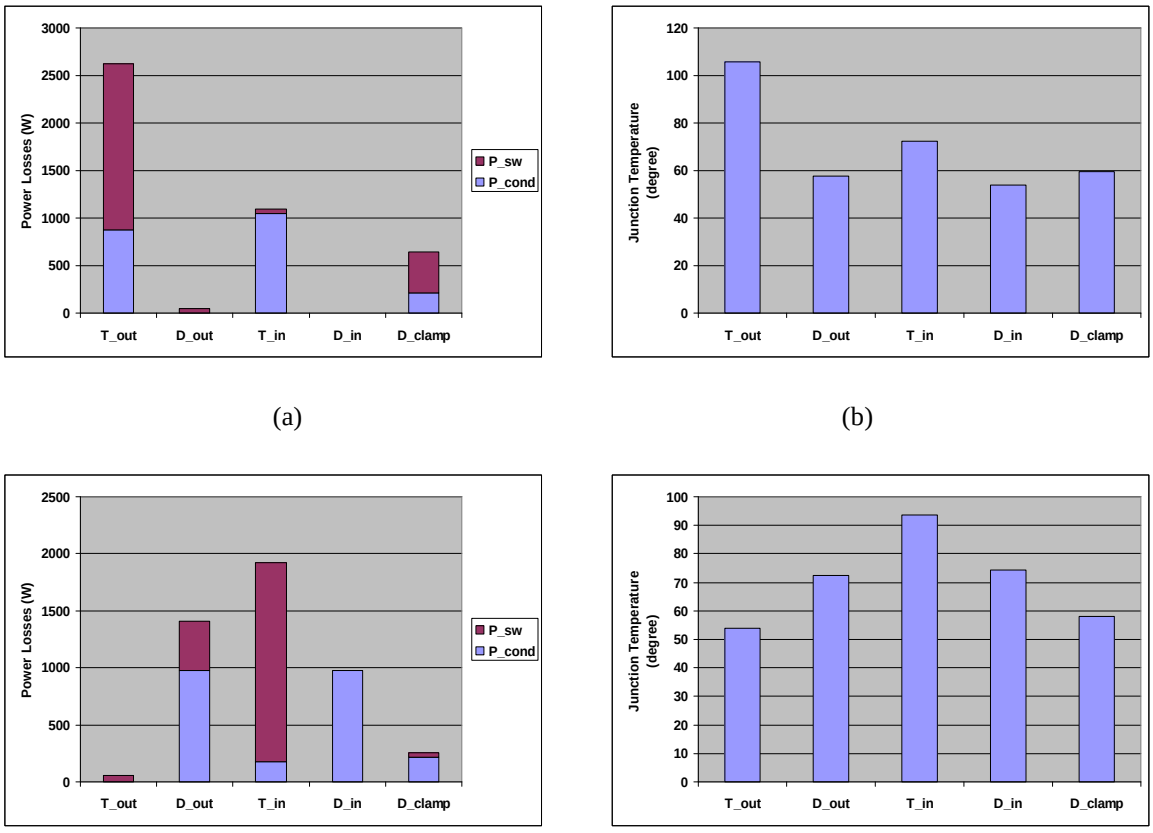
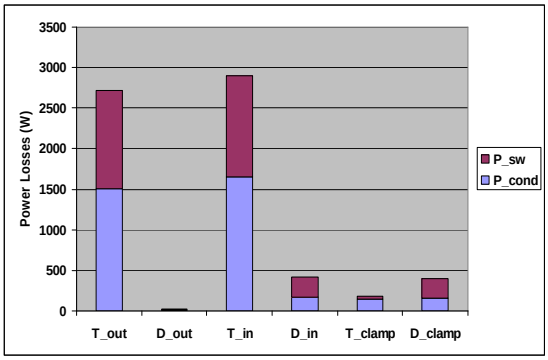
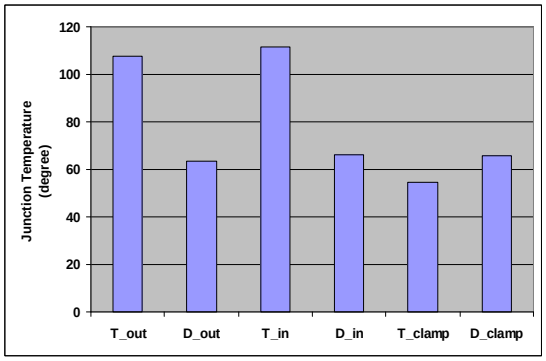


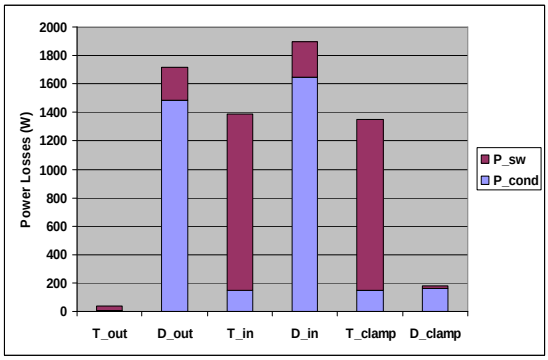
Fig. 2.19 Analysis results of ETO Light NPC PEBB at 5 MW operating point (a) device power loss of grid converter (b) device junction temperature of grid converter (c) device power loss of generator converter (d) device junction temperature of generator converter



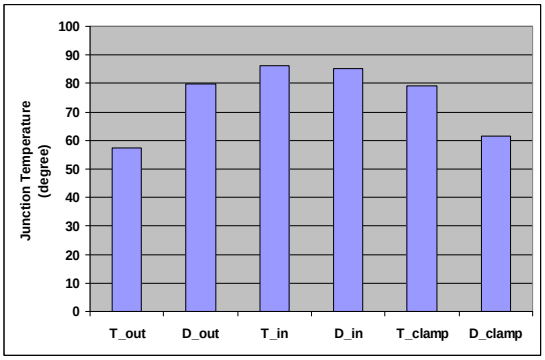
(a)



(b)



(c)



(d)

Fig. 2.20 Analysis results of ETO Light ANPC PEBB at 7 MW operating point (a) device power loss of grid converter (b) device junction temperature of grid converter (c) device power loss of generator converter (d) device junction temperature of generator converter

2.3 Summary

In this chapter, the concept of the ETO Light power electronics building blocks (PEBB) is presented. The electrical design of ETO Light NPC PEBB and ANPC PEBB is presented. The selection criteria of the DC bus voltage, snubber and clamp circuit components, and heat pipe based air cooling system is discussed. The component physical arrangement of ETO Light stacks is designed to achieve the optimal and useful stray inductance. Due to the unique features of the Gen-4 ETO and the heat pipe based air cooling solution, the ETO Light PEBB is optically controlled, and allows no external power supply to provide control power of the

converter. Moreover, the ETO Light PEBB is a stand-alone unit which can easily be applied in many different converter designs and its modularity also allows converting it easily into different topologies.

The methodologies for power loss and thermal analysis of ETO Light PEBBs are introduced. The detailed analytical equations of the device power losses are derived for both ETO Light NPC PEBB and ANPC PEBB. The electrical-equivalent thermal network models of ETO Light PEBBs are constructed. Thermal analysis is implemented for NPC and ANPC PEBBs. The results show that, the maximum output power of ETO Light NPC and ANPC PEBBs is 7.69 MVA and 8.74 MVA respectively under generator mode, and the ANPC PEBB produces 14% higher output power compared to the NPC PEBB. In this condition, the maximum heat removal capability of the heat pipe is the thermal limitation. The results also show that the maximum output power of ETO Light NPC and ANPC PEBBs is 6.65 MVA and 8.45 MVA respectively under motor mode, and the ANPC PEBB produces 27% higher output power compared to the NPC PEBB. The steady-state junction temperature of the ETO limits the PEBB thermal capability in this case.

Finally, the proposed ETO Light PEBBs are applied in large wind turbine systems, and the system configurations are identified. ETO Light NPC PEBB and ANPC PEBB can support up to 5 MW and 7 MW wind turbines respectively, and the thermal performance of the PEBBs is studied for both cases.

Chapter 3 Fault Tolerant Design of ANPC Converters

3.1 Fault Tolerant Issues of Power Electronics Converters

3.1.1 Fault Tolerant Requirements

In an electrical system equipped with voltage source converters, the main possible failure causes include: (1) AC line fault (line to ground and line to line short); (2) DC bus fault (dc-link capacitor failure and DC bus to ground short); (3) device failure (open and short circuit failure of the switches and diodes); (4) controller fault (loss of gate drive signals). In this work, we mainly focus on the fault resulting from the device failure.

When a device failure occurs in the converter, it usually requires tripping the converter and then isolating it from the system to avoid further serious damage. However, in the critical industrial processes with high standstill cost and in the safety-critical applications, such as aerospace, military, mining and transmission system, the requirement of a high reliability and survivability of the system is usually very important. Therefore, the motivation toward the improvement of the system reliability has drawn lots of interest in the research including fault diagnosis and fault tolerant operation for power electronics converters. This study is especially relevant for multilevel converters, because they have very complex topologies and a large number of power devices, which usually imply an increased failure probability.

3.1.2 Review of Fault Tolerant Techniques of Multilevel Converters

For two-level converters, the basic solution is to incorporate a duplex converter redundancy, so that the backup converter can replace the failed main converter after the fault [56] [57]. Another economic solution is to add an additional phase-leg instead of a complete

converter [58]. These two solutions allow consistent output power rating and power quality compared to normal operation, thus they are considered to be effective fault tolerant solutions for two-level converters. However, they may not be practical for multilevel converters. Since multilevel converters consist of a large number of power devices and components, the cost of the additional converter or phase-leg redundancy becomes too high. Some researchers have addressed the fault tolerant issues for several popular multilevel converters including NPC, FC and CHB topologies [59]. In this section, the main techniques for the fault diagnosis and fault tolerant strategies of multilevel converters are summarized.

3.1.2.1 Fault diagnosis

The main fault diagnosis techniques for multilevel converters are summarized below.

- Switch measurement: this method needs to monitor the voltage and/or current of each device, which can be done by the commercial device gate drivers without adding additional hardware [60]. Both device open failure and short failure can be identified by this solution. For example, if the voltage across the device is always zero regardless of the gate signal, then the device fails in short.
- Output voltage/current waveform analysis: this method is based on the measured output phase voltage or current waveform and has been used to detect the fault in NPC and CHB converters [61] [62] [63] [64] [65]. After the fault occurs, the measured phase voltage or current is different from that in normal operation, which results in an error signal. This error signal can be processed and tabulated to detect the device failure information. This fault diagnosis method usually requires the time of at least 1/8 ~ 1 fundamental period between the fault occurrence and the fault

detection. However, in [64], the author proposed a novel method allowing the fastest detection time for device open failure in NPC converters to be within a maximum of two sampling times (several hundred μs).

- Others methods: The spectral analysis based detection is presented for the fault diagnosis of FC and CHB converters [66]. The principle is that for an interleaved converter, the fault will result in high amplitude content at the cell switching frequency at the output voltage harmonic. Therefore by analyzing the spectrum of the output voltage, a fault can be detected. Another method uses the artificial intelligence (AI) algorithm for CHB converters [67]. It measures the output phase voltage and applies a series of mathematical algorithms (like the FFT) and correlations to the measured data. Then, the neural network (NN) analyzes the data to detect the fault.

3.1.2.2 Fault tolerant strategies

Some fault tolerant strategies for different multilevel converter topologies have been reported by researchers, and are summarized below.

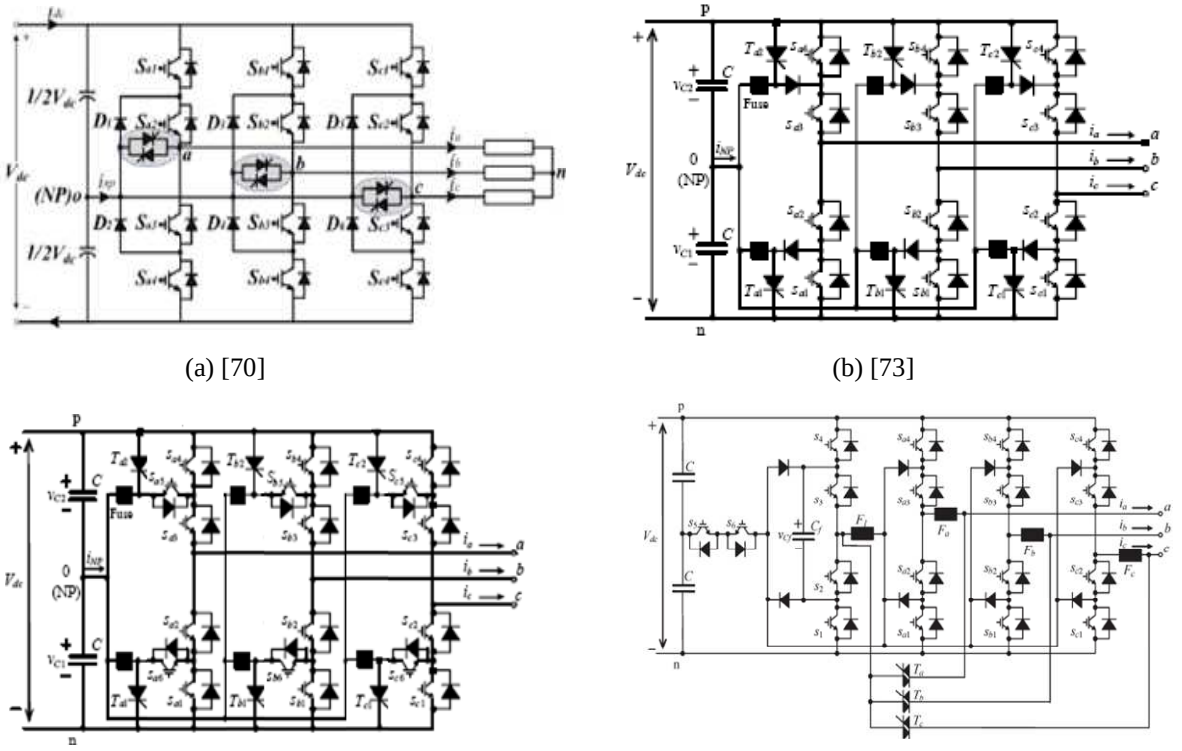
- NPC converters

In [60] [68], using the redundant switching states, sliding-mode control is applied for the fault tolerant operation of 3L-NPC converters without adding additional hardware. It is only effective for device short failure. Moreover, when the outer devices fail in short, the inner devices have to withstand the full dc-link voltage during the fault tolerant operation, and this fact should be taken into consideration for the converter design. For inner device short failure, the maximum modulation index will be reduced to about one half. In [69], a five-level NPC converter with the similar fault tolerant strategy is discussed.

In [70] [71], an additional pair of thyristors is added between the neutral point (NP) of the dc-link and each phase output of the NPC converter to handle device open failure, as shown in Fig. 3.1 (a). Using these thyristors, the faulty phase can be connected to the NP of the dc-link when any single device fails in open. With the modified PWM modulation, the fault tolerant operation can be achieved, and no device withstands the full dc-link voltage. However, the maximum modulation index and thus the maximum output voltage are reduced. Moreover, this method does not consider device short failure.

In [72] [73], another two fault tolerant solutions are introduced for NPC converters by adding several additional fuses, thyristors and power devices to each phase, as shown in Fig. 3.1 (b)~(c). During the fault operation, the faulty phase can switch between the upper and lower dc-link, therefore, the maximum modulation index is the same as normal operation. They also allow multiple device failures in one phase or even two or three phases simultaneously. However, only short circuit failure is considered in these two methods, and some devices have to withstand the full dc-link voltage during the fault tolerant operation.

In [74], a fourth-leg and additional fuses, thyristors and power devices are added to NPC converters, as shown in Fig. 3.1 (d). In normal operation, the fourth-leg can provide a stiff NP voltage. In fault tolerant operation, this leg substitutes the faulty phase, therefore the normal behavior of the NPC converters can be guaranteed and the power devices do not withstand overvoltage. This method is effective for both open and short circuit failure. However, this solution makes the converter topology too complicated and too costly.



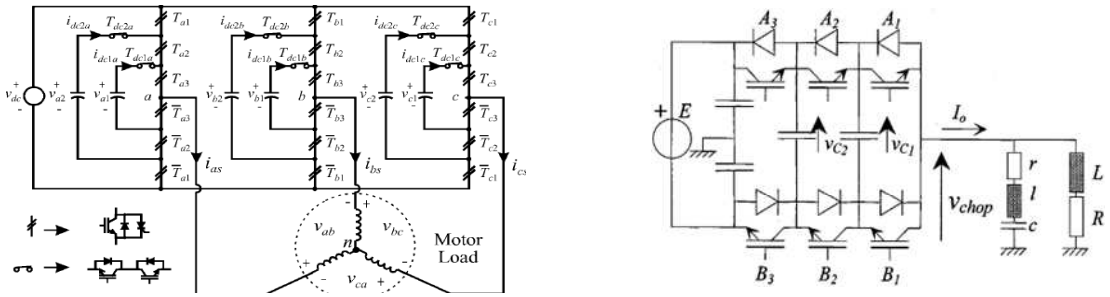
(a) [70] (b) [73]

(c) [73] (d) [74]

Fig. 3.1 Fault tolerant strategies for NPC converters

- FC converters

In [75], a thyristor is added in parallel to each device in a four-level FC converter so that the failed device can be bypassed. In addition, two more switches are needed to connect in series with the dc branches of each phase, as shown in Fig. 3.2 (a). This solution is valid for both single device open and short failure, and the maximum output voltage and its waveform quality are the same as normal operation. In [76], no additional components are added to the FC converter, as shown in Fig. 3.2 (b). After the fault, the reconfiguration of the converter modulator can be made to achieve fault tolerant operation. This solution only works for device short circuit failure and the number of output voltage levels is reduced. In both methods, some devices need to be oversized to withstand the overvoltage across them.



(a) [75] (b) [76]

Fig. 3.2 Fault tolerant strategies for FC converters

- CHB converters

In [77], an additional redundant H-bridge cell is added to each leg of the CHB converters for fault tolerant operation. When one H-bridge cell in the leg fails, it is isolated from the leg by using a bypass switch. After that, the redundant cell becomes operative, and the converter operation goes back to the normal status. However, when no back-up H-bridge cell is available, as shown in Fig. 3.3, the control and modulation can be reconfigured to sustain the operation [78] [79]. One way is to bypass as many cells as possible in the three phases, so that the number of the operative cells in each phase is the same, then the converter can still generate balanced line-to-line voltage. Another method is to bypass the faulty cell, and use the phase shift between the voltage references for all the other operative cells in the three phases. For both methods, the available maximum output voltage is reduced.

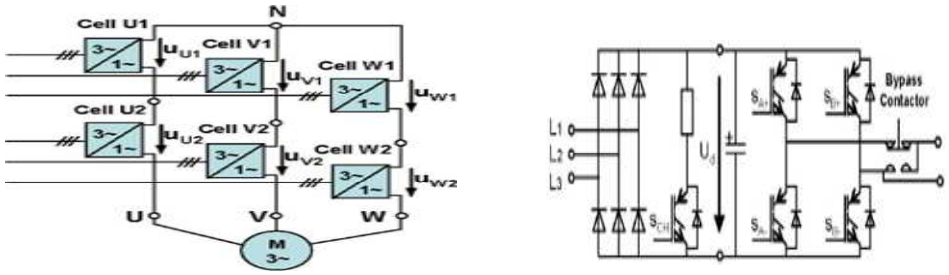


Fig. 3.3 Fault tolerant strategies for CHB converters

According to the discussions above, it can be found that in most fault tolerant solutions, additional components (such as power devices, fuses, or even a phase-leg) are required to be added to the standard multilevel converter topologies for the fault tolerant operation. This will increase the system cost and may even reduce the converter reliability due to the use of more components. Moreover, both device open and short circuit failure may occur in the converters depending on the characteristics and failure mechanism of the power devices, thus, a comprehensive fault tolerant scheme should consider both failure types.

3.2 Fault Tolerant Design of ANPC Converters

The main motivation of this work is to achieve fault tolerant operation for 3L-ANPC converters under both device open and short circuit failure by adding less or even no additional components to the standard 3L-ANPC topology.

3.2.1 Analysis of 3L-ANPC Converters under Device Failure Conditions

Fig. 3.4 shows the circuit of a three-level ANPC converter. The relation of switching states, switching sequence and output voltage of phase A in the converter is given in Table 3-1. In normal operation (no device failure occurs), one of the four zero switching states (0U1, 0U2, 0L1 and 0L2) is selected to balance the power loss distribution among the devices in the converter based on the loss balancing schemes [51] [52] [53].

Under device failure condition, due to the symmetrical structure of 3L-ANPC topology, the failure of S_{a1}/D_{a1} and S_{a4}/D_{a4} has similar effects on the converter. The conclusion is the same for the other pairs of S_{a2}/D_{a2} & S_{a3}/D_{a3}, S_{a5}/D_{a5} & S_{a6}/D_{a6}. Therefore only one from each pair will be analyzed in the following fault analysis.

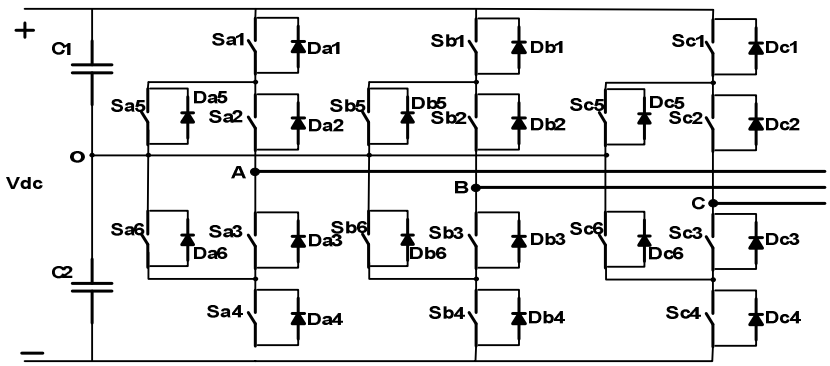


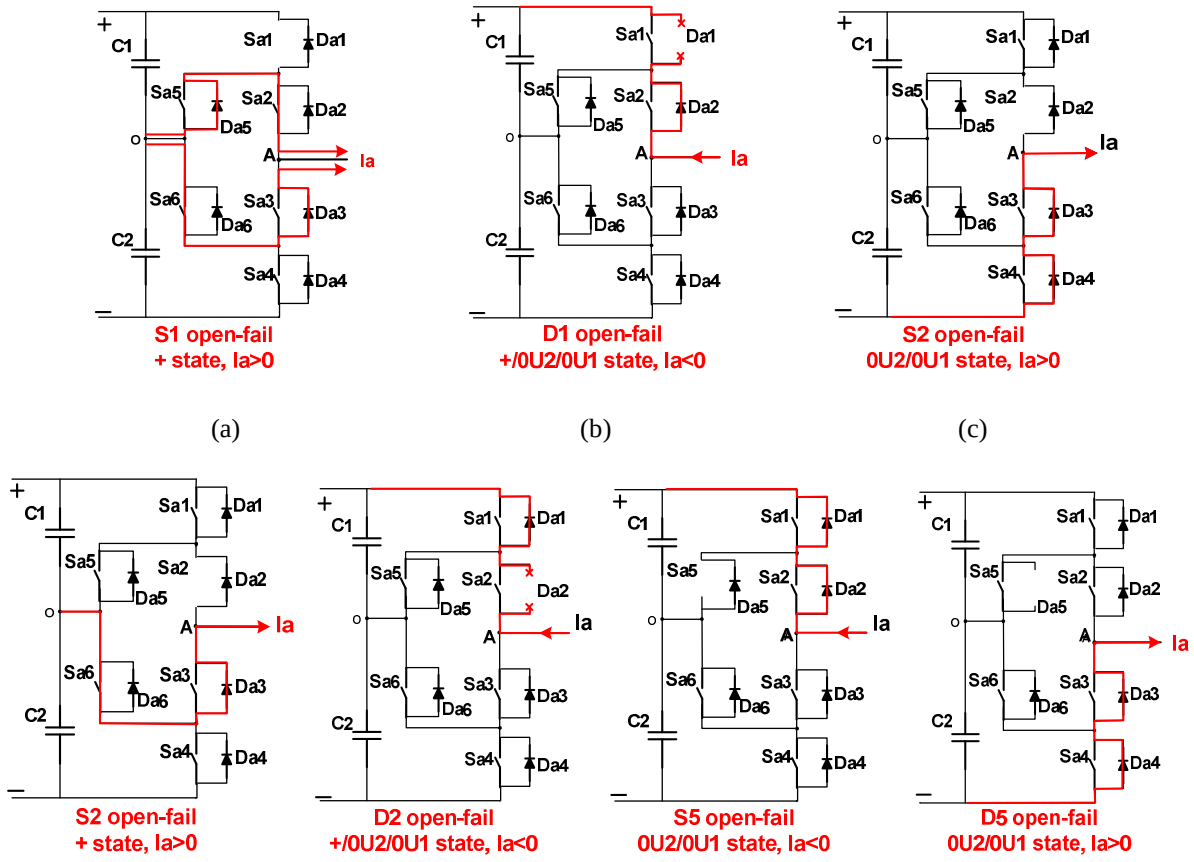
Fig. 3.4 Circuit of three-level ANPC converter

Table 3-1 Switching states, switching sequence and output voltage of a three-level ANPC converter

Switching states	Switching sequence						Output voltage
	Sa1	Sa2	Sa3	Sa4	Sa5	Sa6	
+	1	1	0	0	0	1	+Vdc/2
0U2	0	1	0	0	1	0	0
0U1	0	1	0	1	1	0	0
0L1	1	0	1	0	0	1	0
0L2	0	0	1	0	0	1	0
-	0	0	1	1	1	0	-Vdc/2

Fig. 3.5 shows the current flow path at different output voltage levels under the open circuit failure of S_{a1}/D_{a1}, S_{a2}/D_{a2} and S_{a5}/D_{a5} respectively. The positive direction of the current is defined as flowing out of the phase AC terminal. As seen, when S_{a1} open failure occurs at "+" state, if $I_a>0$, as shown in Fig. 3.5 (a), then the phase output is connected to the NP of the dc-link instead of the positive DC bus. Fig. 3.5 (c) shows S_{a2} open failure occurs at "0U2/0U1" state when $I_a>0$, then the phase output is connected to the negative DC bus rather than the NP of the dc-link. Fig. 3.5 (f) shows S_{a5} open failure occurs at "0U2/0U1" state when $I_a<0$, then the phase output is connected to the positive DC bus instead of the NP of the dc-link. Due to the incorrect output voltage, the output current will become unsymmetrical and the NP of the dc-link will be unbalanced. When D_{a1} open fault occurs at "+/0U2/0U1"

state and I_a<0, as shown in Fig. 3.5 (b), the condition is even worse since the phase current I_a becomes discontinuous due to the cut-off of the conduction path, and the induced voltage on the load inductor and loop inductor may cause overvoltage on the converter and cause damage. For other device failure cases, the analysis can be studied in the similar way.



(a) (b) (c)

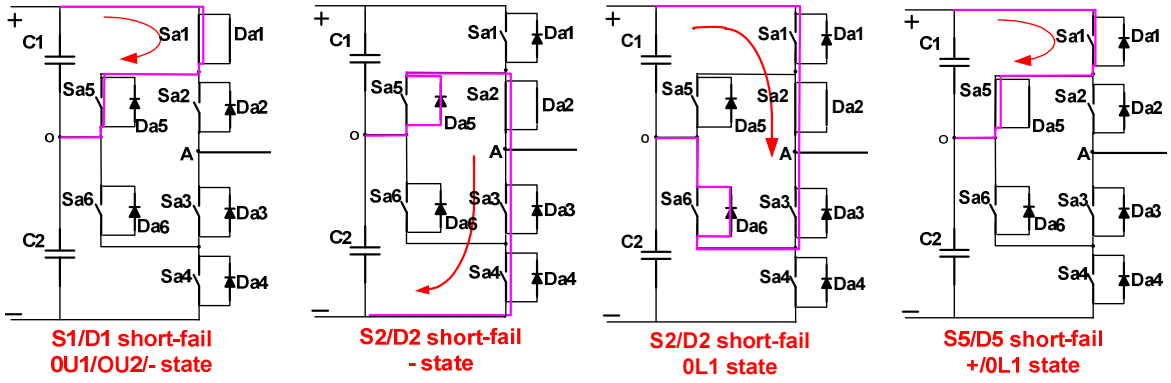
(d) (e) (f) (g)

Fig. 3.5 Examples of current flow path under single device open failure in 3L-ANPC converters

Device short circuit failure can cause even more serious problems compared to open circuit failure. The reason is that under short-circuit failure, the dc-link capacitors may be discharged through a short-current conduction path directly, and thus some devices may break down due to over-currents. Because the voltage of one dc-link capacitor will drop to

zero quickly, some devices may have to withstand the full DC bus voltage and become damaged due to the experienced overvoltage. If we assume the capacitors and devices can survive in this condition, the output current will not be a balanced sinusoidal waveform anymore, which is similar to the open circuit failure cases.

Fig. 3.6 shows the current flow path under short circuit failure of S_{a1}/D_{a1}, S_{a2}/D_{a2} and S_{a5}/D_{a5} respectively. When S_{a1}/D_{a1} short failure occurs, if the switching state commutates to "0U1/0U2/-", as shown in Fig. 3.6 (a), the upper capacitor C_1 will be shorted by S_{a1}/D_{a1} and S_{a5}. Fig. 3.6 (b) and (c) show that if S_{a2}/D_{a2} short failure occurs, "-" state forms a short current path for lower capacitor C_2, while "0L1" state provides a short current path for upper capacitor C_1. If S_{a5}/D_{a5} short circuit failure occurs at "+/0L1" state, as shown in Fig. 3.6 (d), the condition is the same as Fig. 3.6 (a). Similarly the short current path of the dc-link capacitors can be found for the other device short failure conditions.



(a) (b) (c) (d)

Fig. 3.6 Examples of current flow path under single device short failure in 3L-ANPC converters

3.2.2 Proposed Fault Tolerant Strategy of 3L-ANPC Converters

In this section, the fault tolerant strategy for both single device open and short circuit failure in a three-level ANPC converter is proposed [80].

3.2.2.1 Strategy for device open circuit failure

From the analysis above, it shows that the device open failure may impact the proper operation of the 3L-ANPC converter and cause the neutral-point voltage unbalance and the unsymmetrical or discontinuous output currents. However, with a proper control strategy, the active NPC switches S_{a5} and S_{a6} can provide a fault tolerant ability for the converter under device open failure condition. The principles of the fault tolerant control strategy under single device open failure are given below.

- If S_{a5}/D_{a5} or S_{a6}/D_{a6} open failure occurs, the active NPC converter topology is derived into a similar configuration as the conventional NPC converter topology.
- If any single device open failure occurs among S_{a1}/D_{a1} through S_{a4}/D_{a4}, the output AC terminal of the faulty phase (the phase with the failed device) needs to be connected to the neutral-point of the dc-link. The modulation signals also need to be modified in order to maintain the balanced three-phase line-to-line voltages.

According to the principles above, the modified switching states and switching sequences for the fault tolerant operation under single device open failure are given in Table 3-2. After the device open circuit failure is detected, the 3L-ANPC converter transits immediately from normal operation into fault tolerant operation. Knowing the position of the failed device, a new switching sequence is used to generate the certain switching state according to Table 3-2.

With the proposed control strategy, under S_{a5}/D_{a5} or S_{a6}/D_{a6} open circuit failure, the faulty phase is still able to output three voltage levels “+”, “0” and “-”, which is similar to the conventional NPC converters. Therefore, the reference voltage signals need not change, and the maximum modulation index and the output voltage waveform quality are not reduced.

Moreover, to further look into this failure condition, if only S_{a5} fails, while D_{a5} is healthy, then besides the "0L1" and "0L2" switching states, the faulty phase can still generate "0U1" and "0U2" switching states when the phase current direction is positive. This means the device power loss balancing function can still be implemented to some extent even during the fault tolerant operation, and this feature is different from the 3L-NPC converters.

Table 3-2 Solution for single device open failure of a 3L-ANPC converter

Fault device	Switching states	Switching sequence						Output voltage
		Sa1	Sa2	Sa3	Sa4	Sa5	Sa6	
Sa5/Da5	+	1	1	0	0	0	1	+Vdc/2
	0L1	1	0	1	0	0	1	0
	0L2	0	0	1	0	0	1	
	-	0	0	1	1	0	0	-Vdc/2
Sa6/Da6	+	1	1	0	0	0	0	+Vdc/2
	0U2	0	1	0	0	1	0	0
	0U1	0	1	0	1	1	0	
	-	0	0	1	1	1	0	-Vdc/2
Sa1/Da1	0U2	0	1	0	0	1	0	0
	0L2	0	0	1	0	0	1	
Sa2/Da2	0L2	0	0	1	0	0	1	0
Sa3/Da3	0U2	0	1	0	0	1	0	0
Sa4/Da4	0U2	0	1	0	0	1	0	0
	0L2	0	0	1	0	0	1	

Under other device open failure conditions, the faulty phase can only generate "0" switching state because it is always connected to the neutral-point of the dc-link. This means the reference voltage signals have to be modified in order to generate the balanced line-to-line voltages and the sinusoidal output currents. In the carrier-based PWM modulation of the 3L-ANPC converter, the references of the phase voltages and line-to-line voltages in normal operation are expressed by (3-1) and (3-2), respectively.

$$\begin{cases} Va = m \cdot \sin(wt) \\ Vb = m \cdot \sin(wt - \frac{2\pi}{3}) \\ Vc = m \cdot \sin(wt + \frac{2\pi}{3}) \end{cases} \quad \textbf{(3-1)}$$

$$\begin{cases} Vab = \sqrt{3} \cdot m \cdot \sin(wt + \frac{\pi}{6}) \\ Vbc = \sqrt{3} \cdot m \cdot \sin(wt - \frac{2\pi}{3} + \frac{\pi}{6}) \\ Vca = \sqrt{3} \cdot m \cdot \sin(wt + \frac{2\pi}{3} + \frac{\pi}{6}) \end{cases} \quad \textbf{(3-2)}$$

Here, m is the modulation index. V_a, V_b and V_c are the phase voltage references. V_{ab}, V_{bc} and V_{ca} are the line-to-line voltage references. ω is the fundamental angular frequency.

When the faulty phase (e.g. Phase-A) can only output "0" voltage level, instead of using the balanced phase voltages as the reference signals, we must modify the reference signals to make sure the line-to-line voltages are balanced in the 3L-ANPC converter. As long as the line-to-line voltages are symmetrical and sinusoidal, the three-phase output currents will be balanced and sinusoidal. In order to keep the line-to-line voltages similar to (3-2), a new set of phase voltage references is provided in (3-3).

$$\begin{cases} Va = 0 \\ Vb = -\sqrt{3} \cdot m \cdot \sin(wt + \frac{\pi}{6}) \\ Vc = \sqrt{3} \cdot m \cdot \sin(wt + \frac{2\pi}{3} + \frac{\pi}{6}) \end{cases} \quad \textbf{(3-3)}$$

If we assume the device open failure is detected at 0.05s, then the waveform of the new phase voltage reference signals of the 3L-ANPC converter is shown in Fig. 3.7.

It can be observed that, to avoid over modulation, the maximum modulation index derived from (3-3) is limited to 0.577, and it is $1/\sqrt{3}$ of the maximum modulation index in

normal operation. This means the output voltage and the output power of the converter have to be reduced. Moreover, for the open failure of S_{a1}/D_{a1} and S_{a4}/D_{a4}, the redundant switching states still exist for "0" output voltage level, thus they can be used to balance the device power losses.

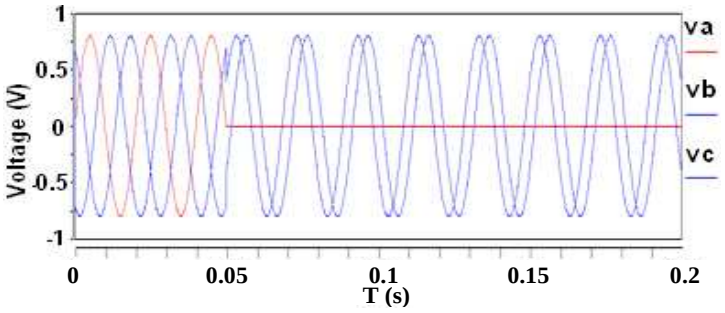


Fig. 3.7 Modified modulation signals for fault tolerant operation of 3L-ANPC converters

3.2.2.2 Strategy for device short circuit failure

According to the previous discussion on the current flow path under device short failure conditions, we need to avoid the appearance of the switching states and switching sequences that can construct the short current path for the dc-link capacitors. In order to do this, two solutions are proposed here.

In Solution-I, the modified switching states and switching sequences are given in Table 3-3. In this scheme, when S_{a1}/D_{a1} or S_{a4}/D_{a4} has a short circuit failure, the faulty phase can still output three voltage levels "+", "0" and "-" by choosing the appropriate modified switching sequence. Therefore the output voltage and current of the converter are almost the same as those in normal operation. For the other device short failure cases, we can use the similar method as that for device open failure conditions to connect the faulty phase to the neutral-point of the dc-link, and modify the reference signals as (3-3). Accordingly, the

maximum modulation index will be reduced to 0.577. However, the drawback of Solution-I is that a certain device will have to withstand the full DC bus voltage under S_{a1}/D_{a1} or S_{a4}/D_{a4} short failure condition. For example, according to Table 3-3, when S_{a1}/D_{a1} fails short, the overvoltage will occur on S_{a2}/D_{a2} at "-" state. Similarly, when S_{a4}/D_{a4} fails short, the voltage across S_{a3}/D_{a3} will be full DC bus voltage at "+" state. For a standard ANPC converter, the voltage rating of the selected power devices is lower than the DC bus voltage (theoretically, equal to half of the DC bus voltage). For example, a 3L-ANPC converter with 5kV DC bus voltage usually employs the 4.5 kV power devices. Therefore, some devices may take the risk to break down due to overvoltage during fault tolerant operation with Solution-I.

Table 3-3 Solution-I for single device short failure of a 3L-ANPC converter

Fault device	Switching states	Switching sequence						Output voltage
		Sa1	Sa2	Sa3	Sa4	Sa5	Sa6	
Sa1/Da1	+	0	1	0	0	0	1	+Vdc/2
	0	0	0	1	0	0	1	0
	-	0	0	1	1	0	0	-Vdc/2
Sa2/Da2	0	0	0	0	0	1	0	0
Sa3/Da3	0	0	0	0	0	0	1	0
Sa4/Da4	+	1	1	0	0	0	0	+Vdc/2
	0	0	1	0	0	1	0	0
	-	0	0	1	0	1	0	-Vdc/2
Sa5/Da5	0	0	1	0	0	0	0	0
Sa6/Da6	0	0	0	1	0	0	0	0

To overcome the drawback of the previous solution, Solution-II is proposed, as shown in Table 3-4. In this solution, no matter which device fails in short, the faulty phase is always connected to the neutral-point of the dc-link, and the reference signals are modified according to (3-3). By doing so, overvoltage will not appear on any device, but the maximum

modulation index will be reduced to 0.577 and the maximum output power of the converter will be reduced. The advantage of Solution-II is that it can be applied for any standard 3L-ANPC converter without any special requirement on the voltage rating of inner devices.

In this work, we mainly focus on Solution-II for fault tolerant operation under device short failure in the 3L-ANPC converter.

Table 3-4 Solution-II for single device short failure of a 3L-ANPC converter

Fault device	Switching states	Switching sequence						Output voltage
		Sa1	Sa2	Sa3	Sa4	Sa5	Sa6	
Sa1/Da1	0	0	0	1	0	0	1	0
Sa2/Da2	0	0	0	0	0	1	0	0
Sa3/Da3	0	0	0	0	0	0	1	0
Sa4/Da4	0	0	1	0	0	1	0	0
Sa5/Da5	0	0	1	0	0	0	0	0
Sa6/Da6	0	0	0	1	0	0	0	0

3.2.2.3 Summary of fault tolerant operation under single device failure in 3L-ANPC converters

With the proposed fault tolerant control strategy, Table 3-5 summarizes the status of the devices and their impact on the status of the faulty phase and the maximum modulation index of the 3L-ANPC converter under single device open failure conditions. For the device status, “ok” means both devices in the pair (like S_{a1} and D_{a1}) are healthy. “fail” means either one or both devices fail. To describe the faulty phase status, “healthy” means no device fails in the phase. “no reduction fault” means the faulty phase can still generate “+”, “0” and “-” levels; “reduction fault” means the faulty phase can only output “0” level. The maximum modulation index indicates the available output voltage level, and thus the power rating

under fault tolerant operation. If the maximum modulation index is limited to 0.577, the converter has to be derated.

Table 3-5 Summary of fault tolerant operation under single device open failure in a 3L-ANPC converter

Sa1/Da1	Sa2/Da2	Sa3/Da3	Sa4/Da4	Sa5/Da5	Sa6/Da6	Phase status	Maximum modulation index
ok	ok	ok	ok	ok	ok	healthy	1.15
fail	ok	ok	ok	ok	ok	reduction fault	0.577
ok	fail	ok	ok	ok	ok	reduction fault	0.577
ok	ok	fail	ok	ok	ok	reduction fault	0.577
ok	ok	ok	fail	ok	ok	reduction fault	0.577
ok	ok	ok	ok	fail	ok	no reduction fault	1.15
ok	ok	ok	ok	ok	fail	no reduction fault	1.15

Table 3-6 summarizes the status of the devices and their impact on the status of the faulty phase and the maximum modulation index of the 3L-ANPC converter under single device short failure conditions by using “Solution-II”. It can be found that any device short failure will result in the reduction of the maximum modulation index, which means the converter has to be derated.

Table 3-6 Summary of fault tolerant operation under single device short failure in a 3L-ANPC converter with Solution-II

Sa1/Da1	Sa2/Da2	Sa3/Da3	Sa4/Da4	Sa5/Da5	Sa6/Da6	Phase status	Maximum modulation index
ok	ok	ok	ok	ok	ok	healthy	1.15
fail	ok	ok	ok	ok	ok	reduction fault	0.577
ok	fail	ok	ok	ok	ok	reduction fault	0.577
ok	ok	fail	ok	ok	ok	reduction fault	0.577
ok	ok	ok	fail	ok	ok	reduction fault	0.577
ok	ok	ok	ok	fail	ok	reduction fault	0.577
ok	ok	ok	ok	ok	fail	reduction fault	0.577

From the summary above, it shows that the proposed strategies enable the 3L-ANPC converter to continue operating under any single device open and short failure conditions. For S_{a5}/D_{a5} or S_{a6}/D_{a6} open failure, the faulty phase can still generate three output voltage levels and the maximum modulation index is not reduced. Under other device failure conditions, the faulty phase can only generate "0" output voltage level, and the maximum modulation index is reduced to 0.577.

3.2.2.4 Requirement of fault detection time

For device short failure, the fault detection time is very critical to protect the other healthy devices from further damage caused by overcurrent or overvoltage. In [81], the short failure protection with fuses is discussed for a 3L-NPC converter. We use the similar method to analyze the device short failure and fault detection time in the ETO Light 3L-ANPC PEBBs. Assume the "DC shoot through" fault is caused by the undesired conduction of two ETOs, as shown in Fig. 3.6 (a), and then the simplified circuit is shown in Fig. 3.8.

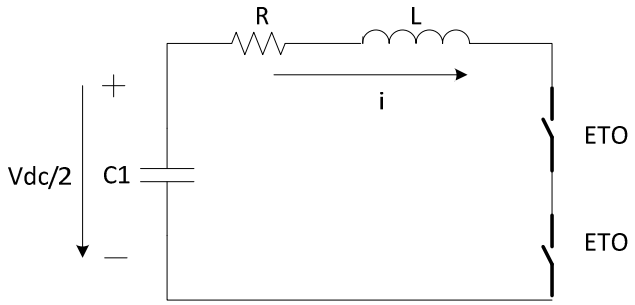


Fig. 3.8 Simplified circuit of "DC shoot through" failure in ETO Light 3L-ANPC PEBB

In the circuit, the capacitor C_1 is the upper dc-link capacitor. The resistor R includes the resistance of the capacitor C_1 and two ETOs. The inductor L is the snubber inductor. The circuit parameters are V_{dc}=5000V, L=4μH, C_1=1.05mF (the voltage ripple across the dc-link

capacitor is within 10%), R=2.5mΩ (resistance of the capacitor C_1) +2×1.4 mΩ (resistance of the ETO). The circuit is simulated in MATLAB. The initial inductor current is 1237A (the worst case), which is the peak phase current under the nominal operating point with a 5 MW output power. The initial capacitor voltage is 2500V. The waveforms of the capacitor voltage and inductor current during the "DC shoot through" are shown in Fig. 3.9.

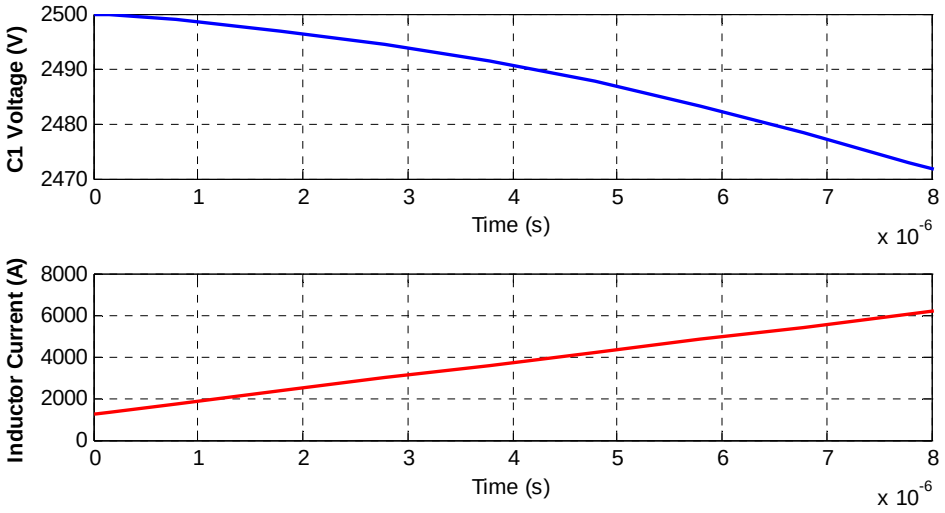


Fig. 3.9 Capacitor voltage (top) and inductor current (bottom) during the discharge of C_1

As seen, in the worst case, the inductor current reaches the ETO's maximum controllable turn-off current level 4000A at around 4.5μs. The change in the capacitor voltage is much slower, and the voltage is around 2488V at 4.5μs. This implies that when a device short failure occurs, in order to ensure the proper turn-off of the healthy ETOs and continue the fault tolerant operation, the detection time needs to be very short (less than 4.5μs), which is a challenge for the fault detection techniques. We also notice that if the inductor initial current is lower, or the snubber inductor is larger, then the allowable detection time can be longer. Simulation results show that if the initial inductor current is 0A, with a 4μH snubber inductor,

the detection time limit can be increased to 6.4μs. When the snubber inductor value is increased to 10μH, then even if the initial inductor current is 1237A as the worst case, the allowable detection time can be extended to 11.2μs.

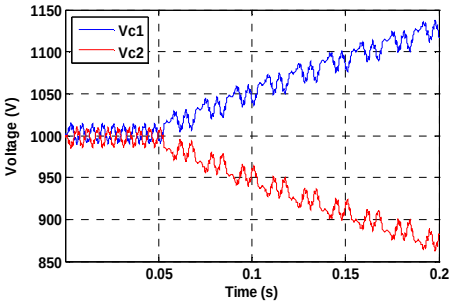
Regarding the fault detection time for device open failure, it is not as critical as that for device short failure. In [64], the author claimed that, using the voltage waveform analysis method, the detection time can be realized within a maximum of two sampling times, typically several hundred μs for a 3L-NPC converter. This time scale is usually fast enough to deal with the device open failure in a 3L-ANPC converter.

3.2.3 Simulation and Experiment Verification

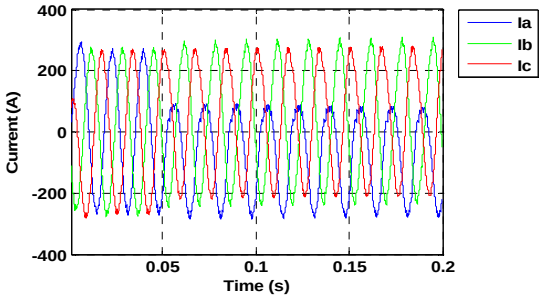
3.2.3.1 Simulation verification

To verify the proposed fault tolerant strategies, simulation is implemented in MATLAB/Simulink. The simulation parameters are DC bus voltage V_{dc}=2kV, dc-link capacitors C_1=C_2=6.6mF, carrier-based SPWM modulation, switching frequency f_{sw}=780Hz, modulation index mi=0.8, fundamental frequency f=60Hz, and inductive load (R=2Ω, L=6mH). In the simulation, we assume that the fault occurs and is detected at 0.05s.

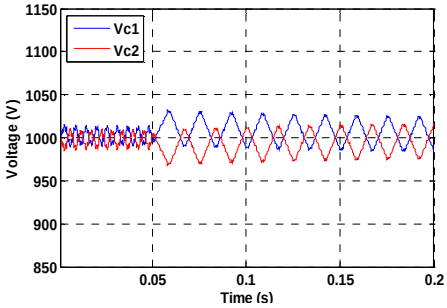
Fig. 3.10, Fig. 3.11 and Fig. 3.12 show the neutral-point voltage of the dc-link and the load current waveforms without and with the proposed control for single device open failure on S_{a1}/D_{a1}, S_{a2}/D_{a2} and S_{a5}/D_{a5}, respectively. Fig. 3.13 and Fig. 3.14 show the neutral-point voltage of the dc-link and load current waveforms without and with the proposed control for single device short failure on S_{a1}/D_{a1} and S_{a5}/D_{a5}, respectively.



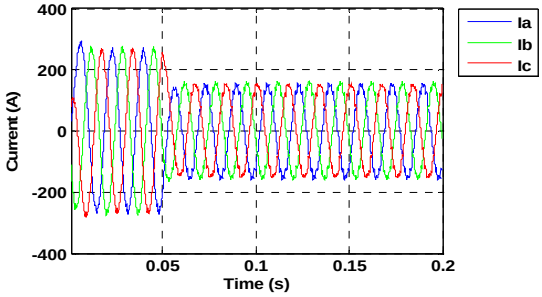
(a) NP voltage without the proposed control



(b) Load current without the proposed control

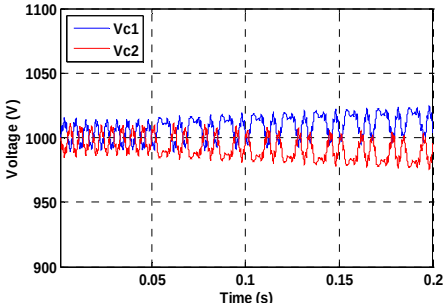


(c) NP voltage with the proposed control

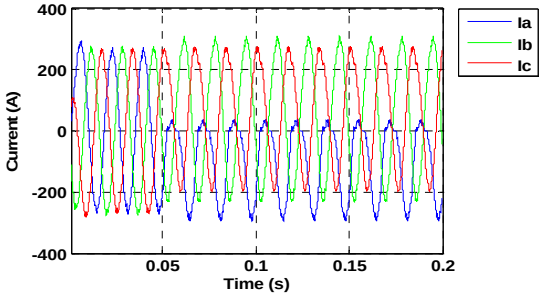


(d) Load current with the proposed control

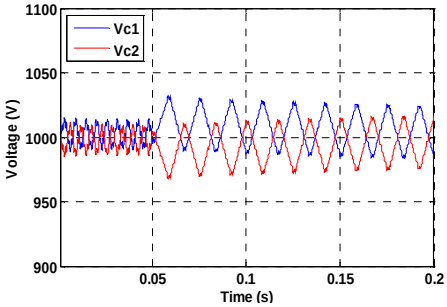
Fig. 3.10 Neutral-point voltage and load current waveforms under S_{a1}/D_{a1} open circuit failure



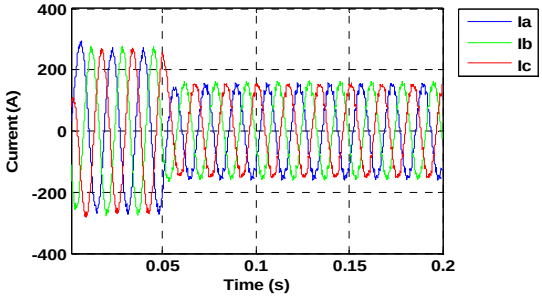
(a) NP voltage without the proposed control



(b) Load current without the proposed control

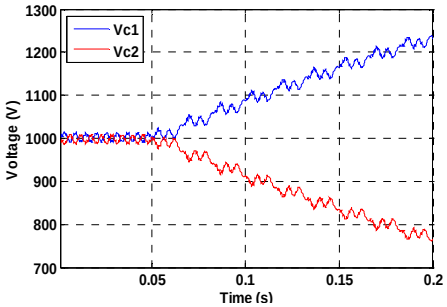


(c) NP voltage with proposed the control

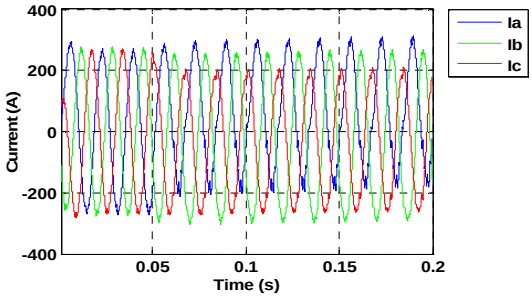


(d) Load current with the proposed control

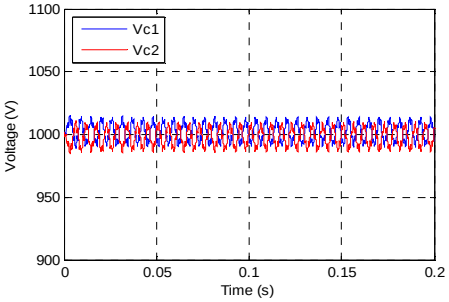
Fig. 3.11 Neutral-point voltage and load current waveforms under S_{a2}/D_{a2} open circuit failure



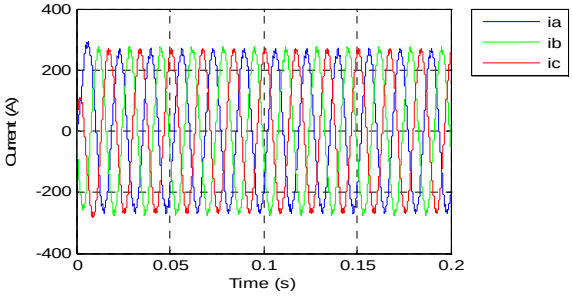
(a) NP voltage without the proposed control



(b) Load current without the proposed control

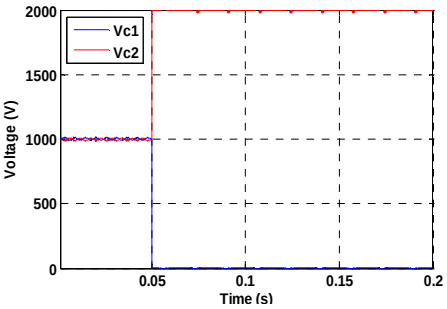


(c) NP voltage with the proposed control

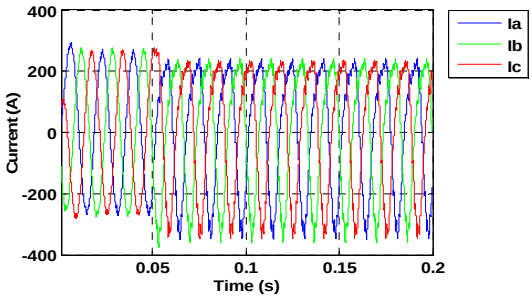


(d) Load current with the proposed control

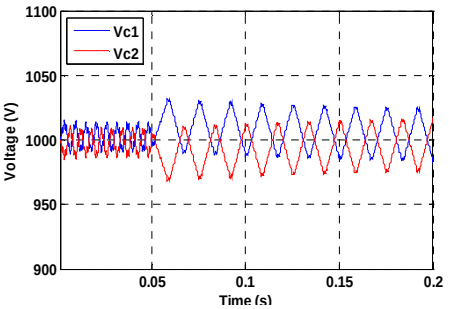
Fig. 3.12 Neutral-point voltage and load current waveforms under S_{a5}/D_{a5} open circuit failure



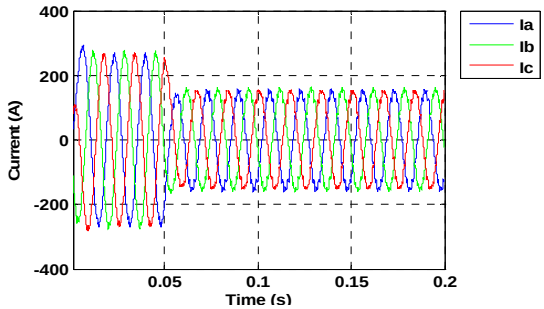
(a) NP voltage without the proposed control



(b) Load current without the proposed control

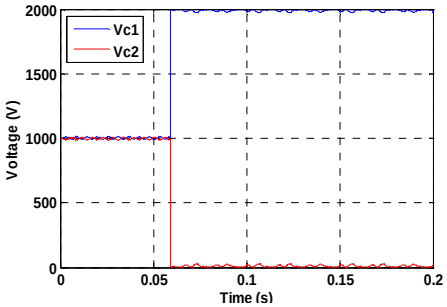


(c) NP voltage with the proposed control

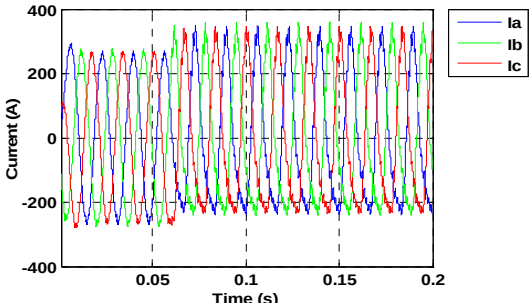


(d) Load current with the proposed control

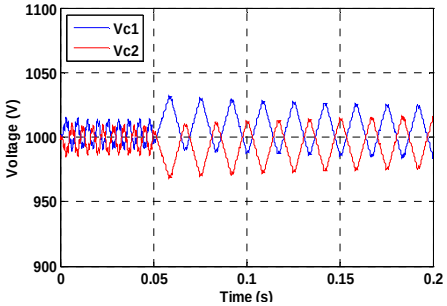
Fig. 3.13 Neutral-point voltage and load current waveforms under S_{a1}/D_{a1} short circuit failure



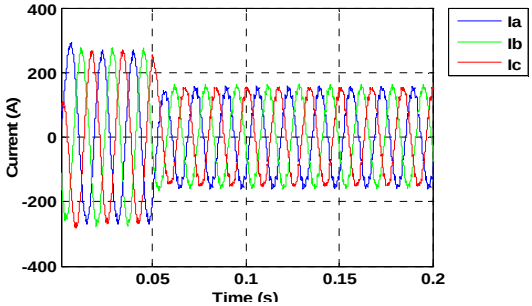
(a) NP voltage without the proposed control



(b) Load current without the proposed control



(c) NP voltage with the proposed control



(d) Load current with the proposed control

Fig. 3.14 Neutral-point voltage and load current waveforms under S_{a5}/D_{a5} short circuit failure

The simulation results show that with the proposed control strategies, the 3L-ANPC converter has the fault tolerant ability under both device open and short failure conditions. Without the proposed control, the converter is not able to work properly after the device failure occurs, including the unbalance of the neutral-point voltage of the dc-link and unsymmetrical output currents of the converter. By modifying the switching sequence for a certain switching state and setting the new voltage reference signals, the neutral-point balance can be achieved, and the stable and continuous output currents are also available. If the faulty phase can still output three voltage levels “+”, “0” and “-”, the converter output voltage is not reduced. Otherwise, when the faulty phase has to be connected to the neutral-point of the dc-link, only “0” output voltage level is available, and consequently the output voltage is reduced and the output power is derated in the 3L-ANPC converter.

3.2.3.2 Experiment verification

The proposed fault tolerant control strategies are verified on a 10kW three-level ANPC converter prototype, as shown in Fig. 3.15. The power devices are Powerex CM75DY-24H IGBT modules. The controllers are TI TMS320F2812 DSP and Altera FLEX10KA FPGA. The main experiment parameters are given in Table 3-7.

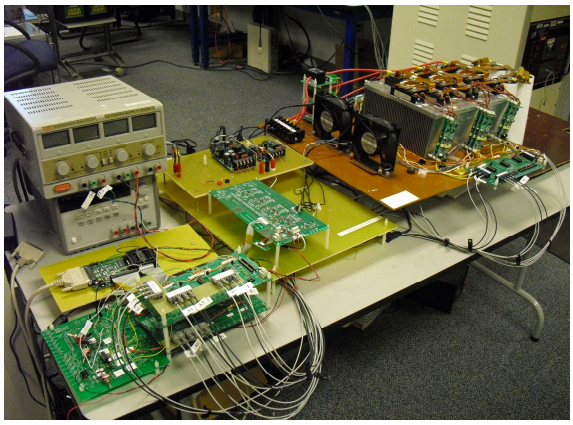
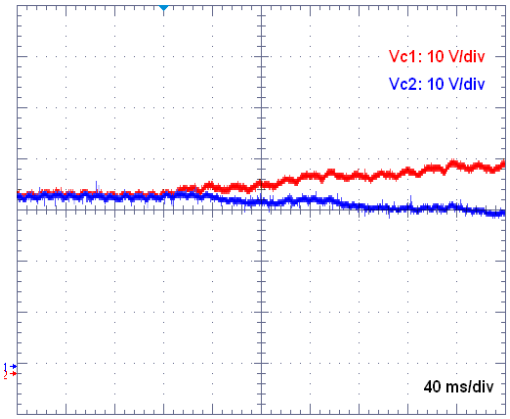


Fig. 3.15 Prototype of a 10kW 3L-ANPC converter

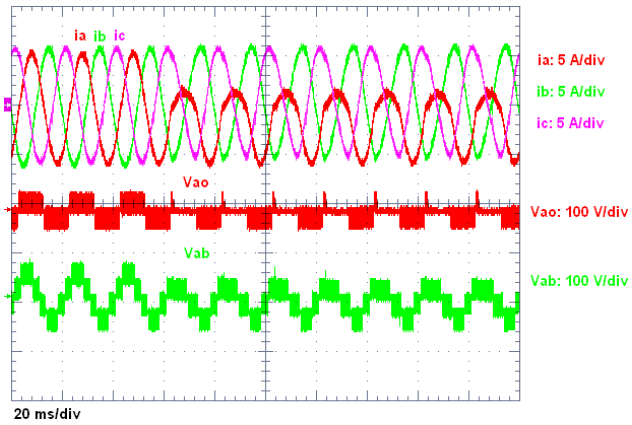
Table 3-7 Experiment parameters

Dc bus voltage	Vdc=70V
DC-link capacitors	C_1=C_2=12 mF
Load	Inductive load (4 ohm+2.5 mH)
Modulation	Carrier-based PWM
Modulation index	mi=0.8
Fundamental frequency	50 Hz
Carrier frequency	2 kHz

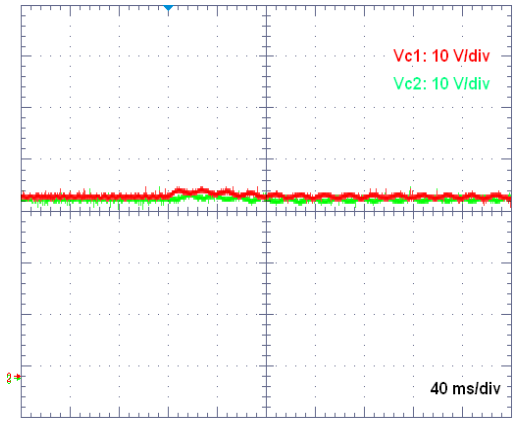
Fig. 3.16, Fig. 3.17 and Fig. 3.18 show the neutral-point voltage, the output currents, the faulty phase voltage and the line-to-line voltage waveforms without and with the proposed control for single device open failure on S_{a1}/D_{a1}, S_{a2}/D_{a2} and S_{a5}/D_{a5}, respectively.



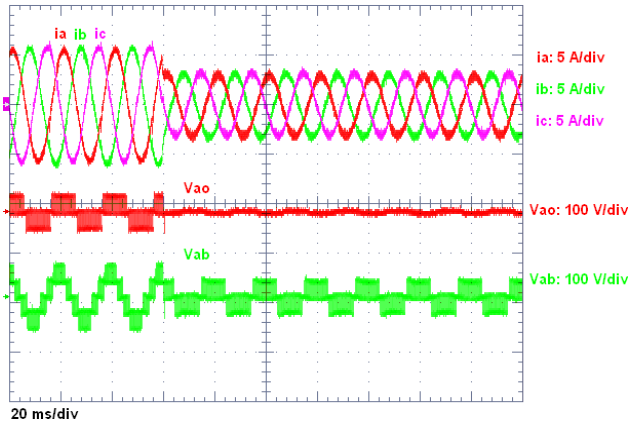
(a) NP voltage without the proposed control



(b) output current and voltage without the proposed control

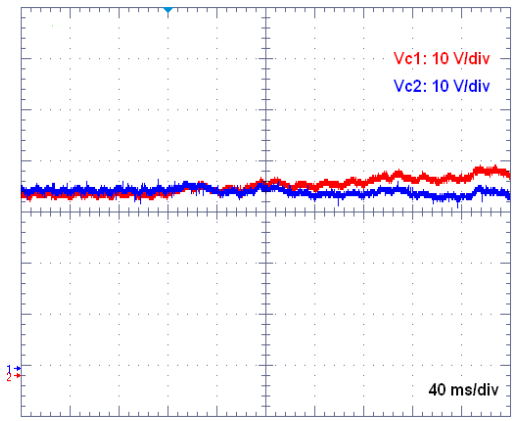


(c) NP voltage with the proposed control

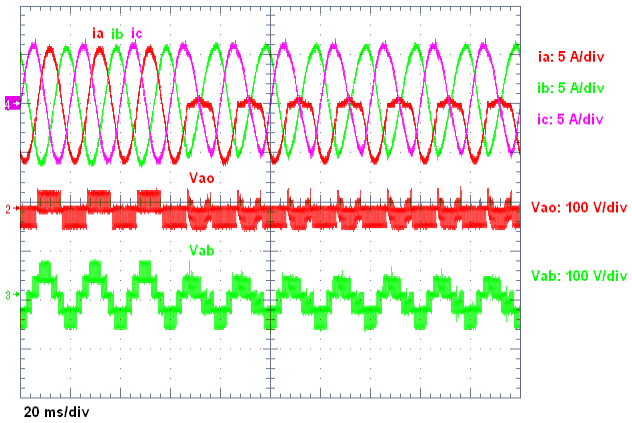


(d) output current and voltage with the proposed control

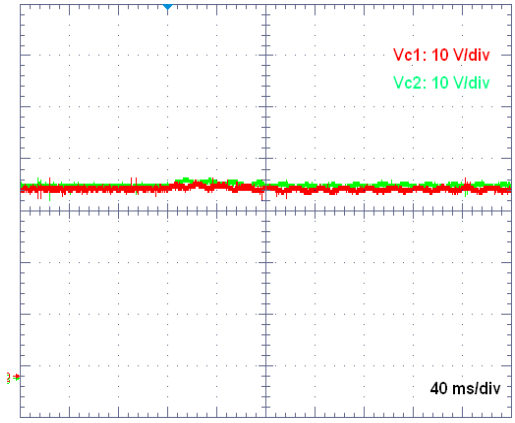
Fig. 3.16 Neutral-point voltage, output currents, faulty phase voltage and line-to-line voltage waveforms under S_{a1}/D_{a1} open circuit failure in a 3L-ANPC converter



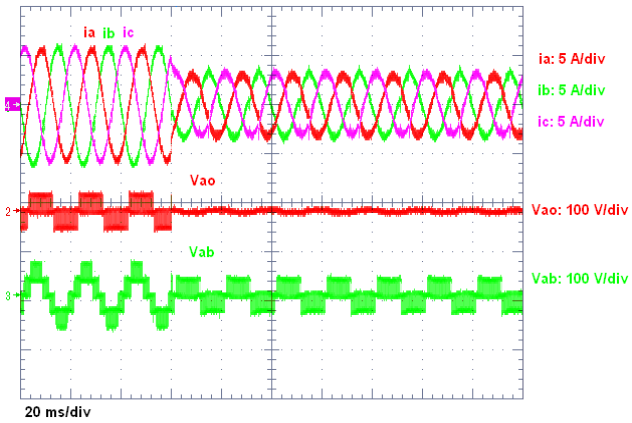
(a) NP voltage without the proposed control



(b) output current and voltage without the proposed control

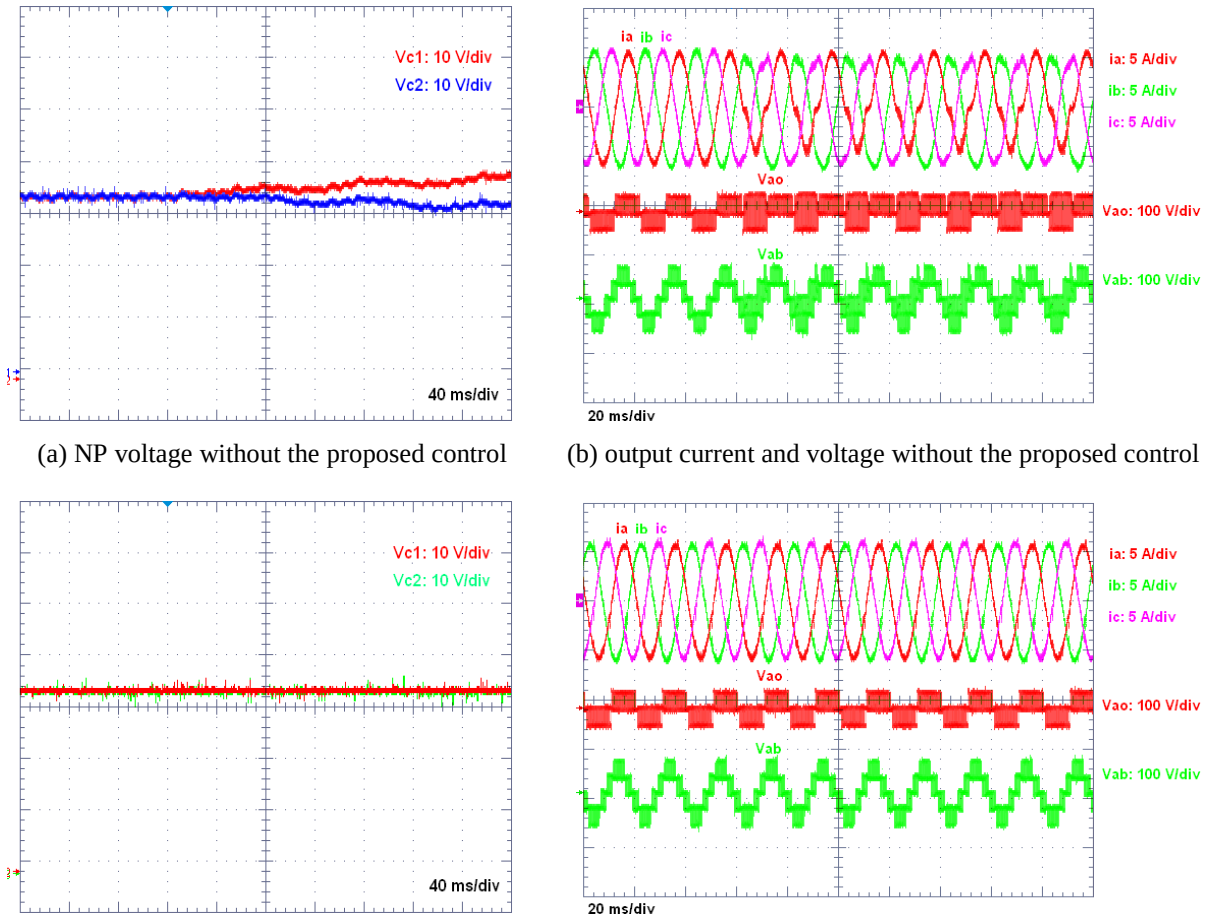


(c) NP voltage with the proposed control



(d) output current and voltage with the proposed control

Fig. 3.17 Neutral-point voltage, output currents, faulty phase voltage and line-to-line voltage waveforms under S_{a2}/D_{a2} open circuit failure in a 3L-ANPC converter



(a) NP voltage without the proposed control

(b) output current and voltage without the proposed control

(c) NP voltage with the proposed control

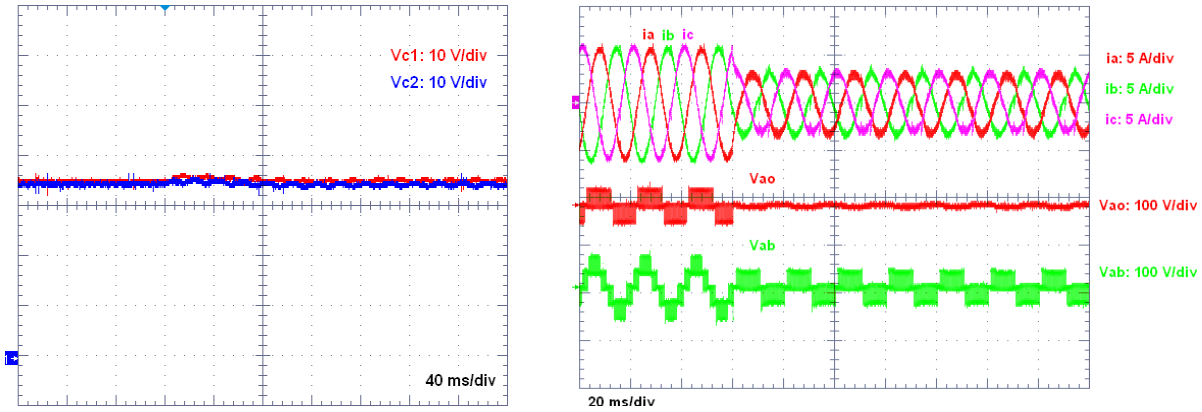
(d) output current and voltage with the proposed control

Fig. 3.18 Neutral-point voltage, output currents, faulty phase voltage and line-to-line voltage waveforms under S_{a5}/D_{a5} open circuit failure in a 3L-ANPC converter

Fig. 3.19 and Fig. 3.20 show the neutral-point voltage, the output current, the faulty phase voltage and the line-to-line voltage waveforms with the proposed control for single device short failure on S_{a1}/D_{a1} and S_{a5}/D_{a5}, respectively.

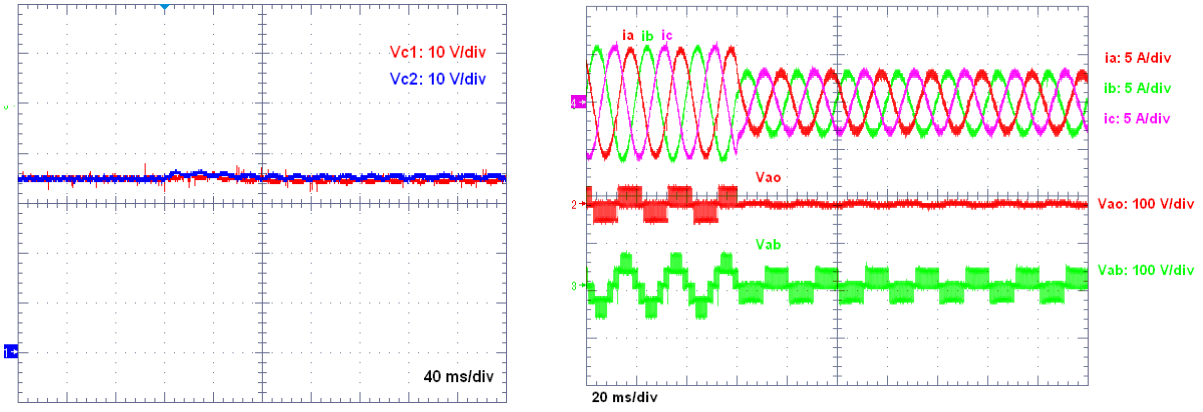
The experiment results reflect the simulation results. With the proposed fault tolerant strategies, under S_{a5}/D_{a5} open circuit failure condition, the 3L-ANPC converter can still output three voltage levels, therefore, the faulty phase voltage, the line-to-line voltage, and the output currents are almost the same as those in normal operation. The neutral-point

voltage of the dc-link is still balanced. When the device failure occurs in S_{a1}/D_{a1} or S_{a2}/D_{a2} regardless of open or short failure, the output currents are still stable and continuous by using the proposed control. However, the current amplitude is reduced, which is limited by the maximum modulation index. The neutral-point voltage ripple becomes slightly larger compared to normal operation because the current of the faulty phase is always connected to the neutral-point, but the voltage and current waveforms show that this NP voltage ripple will not impact the proper operation of the 3L-ANPC converter.



(a) NP voltage with the proposed control (b) output current and voltage with the proposed control

Fig. 3.19 Neutral-point voltage, output currents, faulty phase voltage and line-to-line voltage waveforms under S_{a1}/D_{a1} short circuit failure in a 3L-ANPC converter



(a) NP voltage with the proposed control (b) output current and voltage with the proposed control

Fig. 3.20 Neutral-point voltage, output currents, faulty phase voltage and line-to-line voltage waveforms under S_{a5}/D_{a5} short circuit failure in a 3L-ANPC converter

3.2.4 Analysis for Multiple Device Failure of 3L-ANPC Converters

In this section, we analyze the fault tolerant ability of the 3L-ANPC converter under multiple device open and short failure. The multiple device failure can occur in one phase or even in two or three phases simultaneously.

3.2.4.1 Multiple device open failure

Table 3-8 summarizes the status of the devices and their impact on the status of the faulty phase of the 3L-ANPC converter under multiple device open failure conditions. For example, if S_{a1}/D_{a1} through S_{a4}/D_{a4} are all healthy, then even if S_{a5} and S_{a6} fail simultaneously, the faulty phase still receives the "no reduction fault" status. In another example, if S_{a2}/D_{a2} and S_{a5}/D_{a5} are healthy, the faulty phase still has the "reduction fault" status even if all the other devices in the phase fail together. Compared to Table 3-5, the phase status has a new option, referred to as "no reduction fault (2-level)" when S_{a5}/D_{a5} and S_{a6}/D_{a6} fail open. In this status, the faulty phase can only output "+" and"-" output voltage levels as a two-level converter.

Table 3-8 Fault operation under multiple device open failure (in one phase) in a 3L-ANPC converter

Sa1/Da1 Sa4/Da4	Sa2	Da2	Sa3	Da3	Sa5	Da5	Sa6	Da6	Phase status
ok	ok	ok	ok	ok	fail	ok	fail	ok	no reduction fault
ok	ok	ok	ok	ok	ok	fail	ok	fail	no reduction fault
ok	ok	ok	ok	ok	ok	ok	fail	fail	no reduction fault
ok	ok	ok	ok	ok	fail	fail	ok	ok	no reduction fault
ok	ok	ok	ok	ok	fail	fail	fail	fail	no reduction fault (2-level)
fail	ok	fail	ok	fail	fail	ok	fail	ok	reduction fault
fail	fail	ok	fail	ok	ok	fail	ok	fail	reduction fault
fail	ok	ok	fail	fail	ok	ok	fail	fail	reduction fault
fail	fail	fail	ok	ok	fail	fail	ok	ok	reduction fault

According to the phase status shown in Table 3-8, we can summarize the possible fault tolerant operations for a three-phase 3L-ANPC converter under multiple device open failure conditions. To understand these operations, the analysis based on the voltage vector diagram of a 3L-ANPC converter is used for the explanation and illustration.

- If the status of all three phases are either “healthy” or “no reduction fault”, then each phase still generates three output voltage levels “+”, “0” and “-”. Therefore the converter can operate like normal operation. In the voltage vector diagram shown in Fig. 3.21 (a), all the vectors are still available. If the “no reduction fault (2-level)” exists in the phase status, then considering the worst case in which the status of all the three phases are “no reduction fault (2-level)”, there are still six critical voltage vectors available on the external limit of the vector diagram, as shown in Fig. 3.21 (b), therefore the converter can operate like a two-level converter, while the waveform quality is reduced but the maximum modulation index is still 1.15.
- When the status of one phase (e.g. Phase-A) is “reduction fault”, then if the status of the other two phases are “healthy” or “no reduction fault”, the available voltage vectors are shown in Fig. 3.21 (c). As seen, the six critical voltage vectors on the perimeter of the inner hexagon are still available, which indicates that the line-to-line voltages of the converter are similar to a two-level converter. Therefore the fault tolerant operation can be obtained, while the maximum modulation index is limited to 0.577. Now we consider an even worse case compared to the previously mentioned cases. If the status of the other two phases is “no reduction fault (2-level)”, then Fig. 3.21 (d) shows the available four voltage vectors under this condition. In fact, the

equivalent circuit of the 3L-ANPC converter under this operation mode is topologically identical to the four-switch three-phase converter, which has been presented to achieve the fault tolerant operation of a two-level converter in [57]. Therefore, the 3L-ANPC converter is able to operate under this condition, and the maximum modulation index is reduced to 0.577.

- If the status of the two phases (e.g. phase A and B) are “reduction fault”, then, even if the third phase is “healthy”, only three voltage vectors are available, which are (0 0 -), (0 0 0) and (0 0 +). In this case, the 3L-ANPC converter can not continue operating.

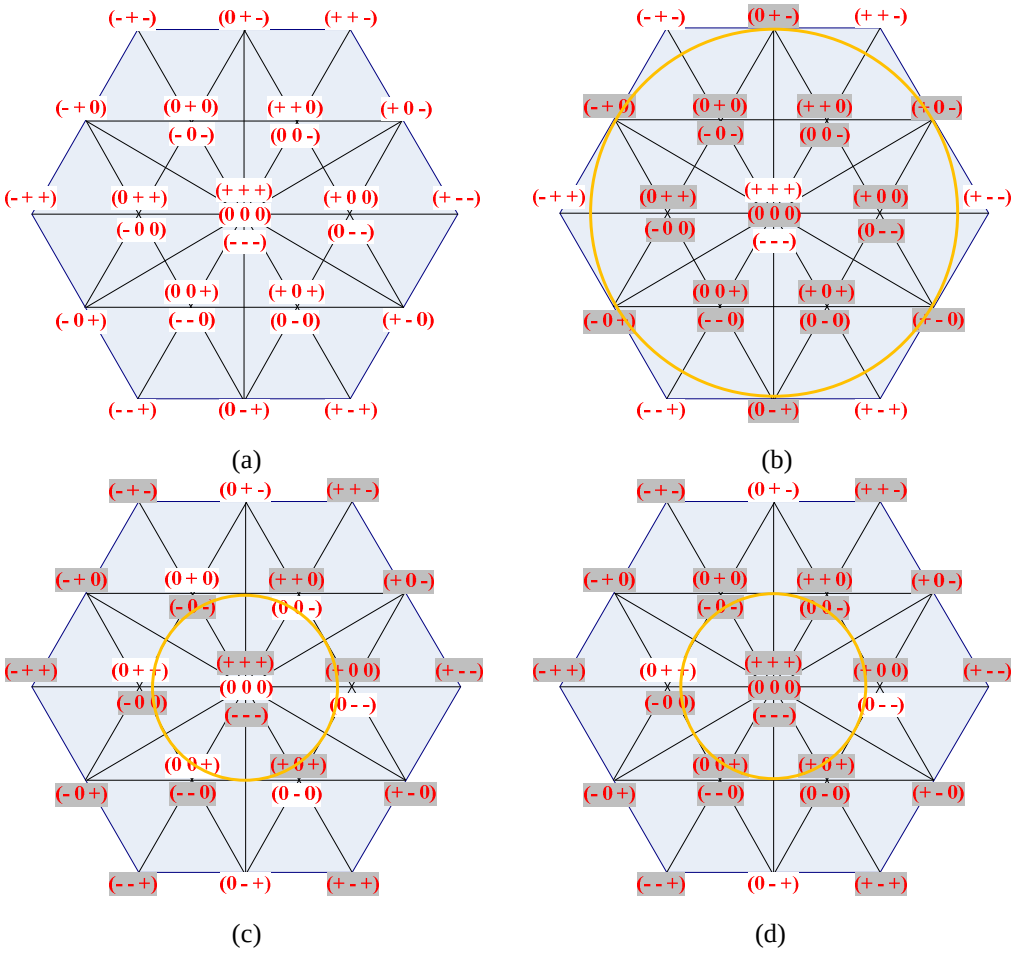


Fig. 3.21 Vector diagram of a 3L-ANPC converter under multiple device open failure conditions

According to the discussion above, Table 3-9 summarizes the fault tolerant capability of a 3L-ANPC converter under multiple device open failure conditions. Depending on the phase status of the converter, the fault tolerant operation can be classified into three modes. For mode-1 and mode-2, the maximum modulation index is 1.15. For mode-3, the maximum modulation index is 0.577. Moreover, only mode-1 allows the same waveform quality as normal operation.

Table 3-9 Fault tolerant capability of a 3L-ANPC converter under multiple device open failure conditions

	Phase A status	Phase B status	Phase C status
Mode-1	healthy / no reduction fault	healthy / no reduction fault	healthy / no reduction fault
Mode-2	no reduction fault (2-level)	healthy/ no reduction fault/ no reduction fault (2-level)	healthy/ no reduction fault/ no reduction fault (2-level)
Mode-3	reduction fault	healthy/ no reduction fault/ no reduction fault (2-level)	healthy/ no reduction fault/ no reduction fault (2-level)

We notice that, in [62], another possible fault tolerant operation was proposed for a 3L-NPC converter, which also applies for a 3L-ANPC converter. This solution uses only one dc-link capacitor to generate a two-level voltage waveform. For example, if S_{a1}/D_{a1}, S_{b1}/D_{b1} and S_{c1}/D_{c1} fail together, then the faulty phases can only generate "0" and "-" output voltage levels using the bottom dc-link capacitor. Fig. 3.22 shows the available voltage vectors. In this condition, the 3L-ANPC converter can operate like a two-level converter, and the maximum modulation index is reduced to 0.577. Similarly, instead of using the bottom dc-link capacitor, we can also use the upper dc-link capacitor to achieve fault tolerant operation of the 3L-ANPC converter when S_{a4}/D_{a4}, S_{b4}/D_{b4} and S_{c4}/D_{c4} fail together.

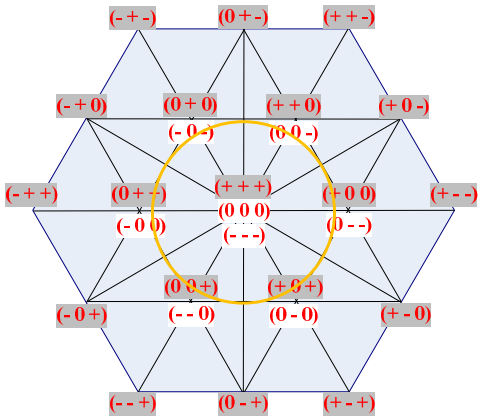


Fig. 3.22 Vector diagram of a 3L-ANPC converter using one dc-link capacitor for fault tolerant operation

3.2.4.2 Multiple device short failure

Table 3-10 summarizes the status of the devices and their impact on the status of the faulty phase of the 3L-ANPC converter under multiple device short failure conditions. As seen, the faulty phase can only generate "0" output voltage level under any device short failure condition, classifying the phase status to be "reduction fault". For example, if S_{a1}/D_{a1} and S_{a4}/D_{a4} are healthy, then even if all the other devices in the phase fail simultaneously, the faulty phase still has the "reduction fault" status. In another example, as long as S_{a2}/D_{a2}, S_{a4}/D_{a4} and S_{a5}/D_{a5} are all healthy, the faulty phase still has the "reduction fault" status even though all the other devices in the phase fail together.

Table 3-10 Fault operation under multiple device short failure (in one phase) in a 3L-ANPC converter

Sa1/Da1	Sa2/Da2	Sa3/Da3	Sa4/Da4	Sa5/Da5	Sa6/Da6	Phase status
ok	fail	fail	ok	fail	fail	reduction fault
fail	ok	fail	ok	ok	fail	reduction fault
ok	fail	ok	fail	fail	ok	reduction fault

According to the proposed control strategies, Table 3-11 summarizes the fault tolerant capability of a 3L-ANPC converter under multiple device short failure conditions. It shows

that there is only one mode for the fault tolerant operation under multiple device short failure condition, in which only one phase status can be “reduction fault” while the status of the other two phases must be “healthy”. The maximum modulation index is reduced to 0.577 during the fault tolerant operation.

Table 3-11 Fault tolerant capability of a 3L-ANPC converter under multiple device short failure conditions

	Phase A status	Phase B status	Phase C status
Mode-1	reduction fault	healthy	healthy

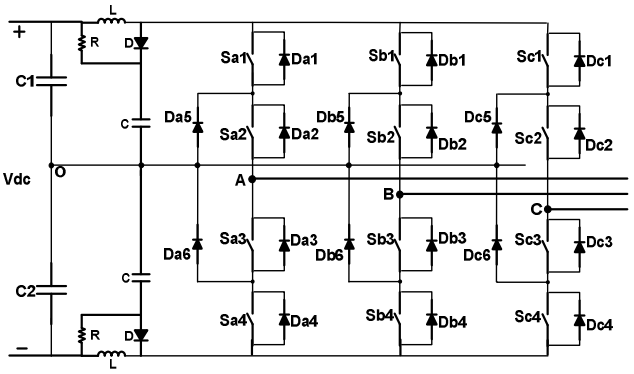
3.3 Reliability Comparison for 3L-NPC and 3L-ANPC Converters

In the published work, the comparison between 3L-NPC converters and 3L-ANPC converters mainly focused on the converter power rating, efficiency and cost [82] [83]. Since a 3L-ANPC converter has more devices than a 3L-NPC converter, the reliability comparison is also worth investigation. However, no work has been reported on this topic yet.

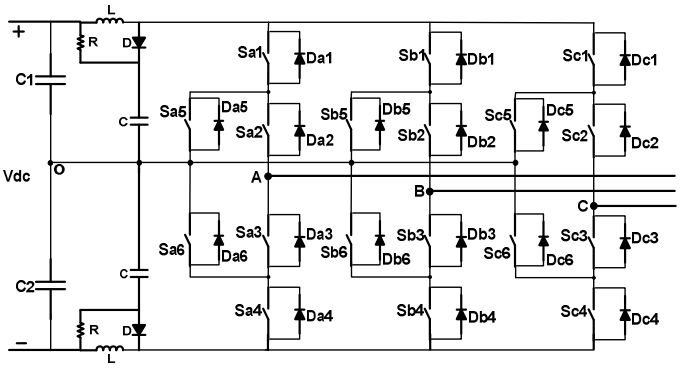
The circuits of a 3L-NPC and a 3L-ANPC converter with snubber and clamp circuit are shown in Fig. 3.23. The main components and their count for reliability calculation are listed in Table 3-12. As seen, the only difference between the two converters is that the 3L-ANPC converter has 6 additional switches (with gate drivers) compared to the 3L-NPC converter. It is usually considered that adding more devices will reduce the reliability of a converter. In this section, we will provide a comprehensive reliability comparison for these two converters.

Table 3-12 Main components and count of 3L-NPC and 3L-ANPC converters for reliability calculation

Topology	Switch	Anti-parallel diode	NPC diode	DC-link capacitor	Snubber and clamp circuit
3L-NPC	12	12	6	2	2
3L-ANPC	18	12	6	2	2



(a) 3L-NPC converter



(b) 3L-ANPC converter

Fig. 3.23 Circuit diagram of 3L-NPC and 3L-ANPC converters with snubber and clamp circuit

3.3.1 Fault Tolerant Operation of 3L-NPC Converters

Before starting the comparison, we need to analyze the fault tolerant operation of a 3L-NPC converter. Some researchers have reported the fault tolerant ability of the 3L-NPC converters, which has been discussed at the beginning of this chapter. We summarize the fault tolerant operation of the 3L-NPC converter under single and multiple device open and short failure condition as follows.

3.3.1.1 Single and multiple device open failure

Table 3-13 summarizes the status of the devices and their impact on the status of the faulty phase in the 3L-NPC converter under single device open failure conditions. As seen, if

S_{a2} or S_{a3} fails in open, the converter can not operate anymore. For any other single device open failure, the fault tolerant operation is available. For example, if S_{a1}/D_{a1} fails, the faulty phase still has the status of "reduction fault". If D_{a5} fails, the faulty phase has the status of "no reduction fault (2-level)".

Table 3-13 Summary of fault tolerant operation under single device open failure in a 3L-NPC converter

Sa1/Da1	Sa2	Da2	Sa3	Da3	Sa4/Da4	Da5	Da6	Phase status
ok	ok	ok	ok	ok	ok	ok	ok	healthy
fail	ok	ok	ok	ok	ok	ok	ok	reduction fault
ok	ok	fail	ok	ok	ok	ok	ok	reduction fault
ok	fail	ok	ok	ok	ok	ok	ok	fail
ok	ok	ok	ok	fail	ok	ok	ok	reduction fault
ok	ok	ok	fail	ok	ok	ok	ok	fail
ok	ok	ok	ok	ok	fail	ok	ok	reduction fault
ok	ok	ok	ok	ok	ok	fail	ok	no reduction fault (2-level)
ok	ok	ok	ok	ok	ok	ok	fail	no reduction fault (2-level)

Table 3-14 shows the status of the devices and their impact on the status of the faulty phase in the 3L-NPC converter under multiple device open failure conditions. For example, if S_{a1}/D_{a1} through S_{a4}/D_{a4} are healthy, then even if D_{a5} and D_{a6} fail simultaneously, the faulty phase still has the "no reduction fault (2-level)" status. In another example, as long as S_{a2}, S_{a3}, D_{a5} and D_{a6} are healthy, the phase still has the "reduction fault" status even if all the other devices in the phase fail together.

Table 3-14 Operation under multiple device open failure (in one phase) in a 3L-NPC converter

Sa1/Da1	Sa2	Da2	Sa3	Da3	Sa4/Da4	Da5	Da6	Phase status
ok	ok	ok	ok	ok	ok	fail	fail	no reduction fault (2-level)
fail	ok	fail	ok	fail	fail	ok	ok	reduction fault

For the fault tolerant capability of the 3L-NPC converter under multiple device open failure conditions, Table 3-9 is still valid while the “no reduction fault” status does not exist. In mode-1 and mode-2, the maximum modulation index is 1.15. In mode-3, the maximum modulation index is 0.577. Moreover, only mode-1 allows the same waveform quality as normal operation. In [62], the author proposed the solution to use only one dc-link capacitor to generate a two-level voltage waveform for the fault tolerant operation. We have discussed the operating principles of this solution for multiple device open failure analysis of the 3L-ANPC converter in detail, and the analysis is almost the same for the 3L-NPC converter. Therefore, we will not repeat the description here.

3.3.1.2 Single and multiple device short failure

Using the same analysis for the 3L-ANPC converter, Table 3-15 summarizes the status of the devices and their impacts on the status of the faulty phase and the voltage across the devices in the 3L-NPC converter under single device short failure conditions. When S_{a1}/D_{a1} or S_{a4}/D_{a4} fails, overvoltage will occur across S_{a2} and S_{a3}, respectively, which may cause damage to the device. So the fault tolerant operation is not available for a 3L-NPC converter when S_{a1}/D_{a1} or S_{a4}/D_{a4} fails in short. For any other single device short failure, the converter can operate like a two-level converter with the maximum modulation index reduced to 0.577.

Table 3-16 shows the status of the devices and their impact on the status of the faulty phase in the 3L-NPC converter under multiple device short failure conditions. As seen, the faulty phase can only generate “0” output voltage level and its status is “reduction fault”. For example, if S_{a1}/D_{a1} and S_{a4}/D_{a4} are healthy, then the faulty phase is classified with the “reduction fault” status even if all the other devices in the phase fail simultaneously. In

another example, if S_{a1}/D_{a1} fails in short, then S_{a2}/D_{a2}, S_{a4}/D_{a4} and D_{a5} must be healthy and D_{a6} must fail in short in order to achieve fault tolerant operation, and this operation is different from the 3L-ANPC converter, in which S_{a6}/D_{a6} can be either healthy or failed.

Table 3-15 Summary of fault tolerant operation under single device short failure in a 3L-NPC converter

Sa1/Da1	Sa2/Da2	Sa3/Da3	Sa4/Da4	Da5	Da6	Phase status	Device overvoltage
ok	ok	ok	ok	ok	ok	healthy	no
fail	ok	ok	ok	ok	ok	no reduction fault (2-level)	Sa2
ok	fail	ok	ok	ok	ok	reduction fault	no
ok	ok	fail	ok	ok	ok	reduction fault	no
ok	ok	ok	fail	ok	ok	no reduction fault (2-level)	Sa3
ok	ok	ok	ok	fail	ok	reduction fault	no
ok	ok	ok	ok	ok	fail	reduction fault	no

Table 3-16 Operation under multiple device short failure (in one phase) in a 3L-NPC converter

Sa1/Da1	Sa2/Da2	Sa3/Da3	Sa4/Da4	Da5	Da6	Phase status
ok	fail	fail	ok	fail	fail	reduction fault
fail	ok	fail	ok	ok	fail (must)	reduction fault
ok	fail	ok	fail	fail (must)	ok	reduction fault

For multiple device short failure conditions of the 3L-NPC converter, Table 3-11 is still valid. Only one phase status can be “reduction fault” while the other two phases must be healthy. The maximum modulation index is reduced to 0.577.

3.3.2 Reliability Analysis Techniques

To assess the converter reliability, some definitions are recalled first as below [84]:

1) Reliability is the characteristics of a system or component expressed by the probability that it will perform a required function under stated conditions for a stated period of time.

2) Failure rate λ is the frequency at which a system or component fails. It is usually given in Failure in Time (FIT), where 1 FIT is equal to one failure within 10^9 operation hours.

According to the MIL-HDBK-217F military standard [85], the failure density function of electronic devices is expressed by:

$$f(t) = \lambda e^{-\lambda \cdot t} \quad (t > 0) \tag{3-4}$$

The reliability function of a component gives the probability of survival until time t:

$$R(t) = 1 - \int_0^t f(t)dt = 1 - (1 - e^{-\lambda \cdot t}) = e^{-\lambda \cdot t} \tag{3-5}$$

To evaluate the reliability of a converter consisting of a number of components, depending on the complexity and redundancy characteristics of the converter, different computation methods can be used [86] [87] [88].

For a simple power electronics converter without redundancy or fault tolerant ability, any failure in one of the components in the converter will cause the entire converter to fail. Therefore, the components can be viewed as a series connected system. The reliability function of the converter can be expressed by:

$$R(t) = \prod_{i=1}^{n} R^i(t) = e^{-\lambda^1 \cdot t} e^{-\lambda^2 \cdot t} \ldots e^{-\lambda^n \cdot t} \tag{3-6}$$

Where, $R^i(t)$ is the reliability of component *i*. λ^1, $\lambda^2 \ldots \lambda^n$ are the failure rates of component 1, 2 …n, respectively.

For a converter with fault tolerant ability, if it consists of n components and requires that at least k components are healthy so that the converter can continue operating, then it is called the k-out-of-n: G system. The reliability function of the converter is expressed by (3-7).

$$R(t) = \sum_{i=k}^{n} (-1)^{i-k} \binom{i-1}{k-1} \sum_{s1<s2<...<si} \prod_{l=1}^{i} R^{s_l}(t) \quad \textbf{(3-7)}$$

Where, $R^{s_l}(t)$ is the reliability function of the component represented by S_l.

However, according to the analysis for the fault tolerant operation of the 3L-NPC and 3L-ANPC converters, it can be found the these two converters are even more complicated than the k-out-of-n: G system. In order to assess their reliability functions, our proposed method is that the component and device failure rates are aggregated to evaluate the converter overall reliability function. This means the converter reliability function should be derived from the sum of all the possible fault tolerant operations.

3.3.3 Reliability Function of 3L-NPC and 3L-ANPC Converters

In this work, the reliability of the 3L-NPC and 3L-ANPC converters is analyzed and compared for a general purpose rather than an accurate reliability engineering calculation. Therefore, some factors, such as quality factors, stress factor and temperature factor, are not considered. The components included for the reliability analysis are switches and their gate drivers, anti-parallel diodes, NPC diodes, snubber/clamp circuit and dc-link capacitors. The failure rates of these components are listed in Table 3-17 [89] [90]. Since for any fault tolerant operation, the dc-link capacitors and the snubber and clamp circuits must be healthy, they can be viewed as a whole part, and its reliability function is given by:

$$Q = (e^{-\lambda_4 t})^2 \cdot (e^{-\lambda_5 t})^2 \quad \textbf{(3-8)}$$

Table 3-17 Component failure rates for reliability analysis and comparison

Component	Failure rate λ of the component	
	FIT (10^{-9} occ./h)	occ./yr.
IGCT+Gate driver	λ_1=50+200=250	0.0022
Anti-parallel diode	λ_2=20	0.0001752
NPC diode	λ_3=20	0.0001752
Snubber/Clamp circuit	λ_4=300	0.0026
DC-link capacitor	λ_5=120	0.0010521

The reliability function for 3L-ANPC and 3L-ANPC converters are derived in the following sections for single and multiple device open and short failure conditions.

3.3.3.1 3L-NPC converters

First, we define that $T_{x|x=a,b,c}$ is the probability that all the devices in phase *x* are healthy, as given by:

$$T_a = T_b = T_c = (e^{-\lambda_1 t})^4 \cdot (e^{-\lambda_2 t})^2 (e^{-\lambda_3 t})^2 \quad \textbf{(3-9)}$$

1) Reliability function under single device short failure condition

According to Table 3-15, in a 3L-NPC converter, S_{x1}/D_{x1} and S_{x4}/D_{x4} in all three phases must be healthy to ensure the continuous operating of the converter. If any other device fails in short, the converter can still operate with a reduced maximum modulation index equal to 0.577.

We define $X_{x|x=a,b,c}$ as the probability that only one device from S_{x2}, D_{x2}, S_{x3}, D_{x3}, D_{x5} and D_{x6} in phase *x* fails, as given by:

$$\begin{aligned} X_a = X_b = X_c = {} & 2 \cdot (1 - e^{-\lambda_1 t})(e^{-\lambda_1 t})^2 \cdot (e^{-\lambda_2 t})^4 (e^{-\lambda_3 t})^2 \\ & + 2 \cdot (1 - e^{-\lambda_2 t})(e^{-\lambda_1 t})^4 \cdot (e^{-\lambda_2 t})^3 \cdot (e^{-\lambda_3 t})^2 \\ & + 2 \cdot (1 - e^{-\lambda_3 t})(e^{-\lambda_1 t})^4 \cdot (e^{-\lambda_2 t})^4 \cdot (e^{-\lambda_3 t}) \end{aligned} \quad \textbf{(3-10)}$$

Then the converter reliability function is derived by:

$$R_{NPC\_single\_short} = (T_a \cdot T_b \cdot X_c + T_b \cdot T_c \cdot X_a + T_a \cdot T_c \cdot X_b + T_a \cdot T_b \cdot T_c) \cdot Q \quad \textbf{(3-11)}$$

In some applications, if they require that the maximum modulation index still needs to be 1.15 during the fault tolerant operation, then all the devices in the converter must be healthy, and thus the reliability function of the converter is:

$$R_{NPC\_single\_short} = T_a \cdot T_b \cdot T_c \cdot Q \quad \textbf{(3-12)}$$

2) Reliability function under multiple device short failure conditions

According to Table 3-11 and Table 3-16, for multiple device short failure conditions, the failure can only occur in one phase, while the other two phases must be healthy. We define $X_{x|x=a,b,c}$ as the probability that the status of phase x is "reduction fault" under multiple device short failure, as given by:

$$X = \overline{T}_1 \cdot T_2 \cdot T_4 \cdot D_5 \cdot \overline{D}_6 + T_1 \cdot \left(\overline{T}_4 \cdot T_3 \cdot D_6 \cdot \overline{D}_5 + T_4 \cdot \left(1 - T_2 \cdot T_3 \cdot D_5 \cdot D_6\right)\right) \quad \textbf{(3-13)}$$

Here, $T_{m|m=1\sim4}$ is the probability that both devices in the pair are healthy. For example, for the pair of S_{x1}/D_{x1}, T_1 represents the probability that both S_{x1} and D_{x1} are healthy. $\overline{T}_m = 1 - T_m$ represents the probability that at lease one device in the pair fails. So we have:

$$\begin{aligned} X_a = X_b = X_c = &\left(1 - (e^{-\lambda_1 t}) \cdot (e^{-\lambda_2 t})\right) \cdot (e^{-\lambda_1 t})^2 \cdot (e^{-\lambda_2 t})^2 \cdot (e^{-\lambda_3 t}) \cdot (1 - e^{-\lambda_3 t}) \\ &+ \left(1 - (e^{-\lambda_1 t}) \cdot (e^{-\lambda_2 t})\right) \cdot (e^{-\lambda_1 t})^2 \cdot (e^{-\lambda_2 t})^2 \cdot (e^{-\lambda_3 t}) \cdot (1 - e^{-\lambda_3 t}) \\ &+ (e^{-\lambda_1 t})^2 \cdot (e^{-\lambda_2 t})^2 \cdot \left(1 - (e^{-\lambda_1 t})^2 \cdot (e^{-\lambda_2 t})^2 \cdot (e^{-\lambda_3 t})^2\right) \end{aligned} \quad \textbf{(3-14)}$$

Then the converter reliability function is expressed by:

$$R_{NPC\_multiple\_short} = (T_a \cdot T_b \cdot X_c + T_b \cdot T_c \cdot X_a + T_a \cdot T_c \cdot X_b + T_a \cdot T_b \cdot T_c) \cdot Q \quad \textbf{(3-15)}$$

If certain applications require that the maximum modulation index still needs to be 1.15 during the fault tolerant operation, then all the devices in the converter must be healthy. In this case, the reliability function of the converter is given by:

$$R_{NPC\_multiple\_short} = T_a \cdot T_b \cdot T_c \cdot Q \tag{3-16}$$

3) Reliability function under single device open failure condition

According to Table 3-13, in a 3L-NPC converter, S_{x2} and S_{x3} in all three phases must be healthy for the successful operation of the converter. We define $X_{x|x=a,b,c}$ as the probability that one device from S_{x1}, S_{x4} and D_{x1} through D_{x6} in phase *x* fails, as given by:

$$\begin{aligned} X_a = X_b = X_c = {} & 2 \cdot (1-e^{-\lambda_1 t})(e^{-\lambda_1 t})^3 \cdot (e^{-\lambda_2 t})^4 (e^{-\lambda_3 t})^2 \\ & + 4 \cdot (1-e^{-\lambda_2 t})(e^{-\lambda_1 t})^4 \cdot (e^{-\lambda_2 t})^3 \cdot (e^{-\lambda_3 t})^2 \\ & + 2 \cdot (1-e^{-\lambda_3 t})(e^{-\lambda_1 t})^4 \cdot (e^{-\lambda_2 t})^4 \cdot (e^{-\lambda_3 t}) \end{aligned} \tag{3-17}$$

Then the reliability function of the converter is:

$$R_{NPC\_single\_open} = (T_a \cdot T_b \cdot X_c + T_b \cdot T_c \cdot X_a + T_a \cdot T_c \cdot X_b + T_a \cdot T_b \cdot T_c) \cdot Q \tag{3-18}$$

If the applications only require that the maximum modulation index needs to be 1.15 during the fault tolerant operation, then as shown in Table 3-13, D_{x5} or D_{x6} in phase *x* is also allowed to fail, while S_{x1}, S_{x4}, D_{x1} through D_{x4} in phase *x* must be healthy. In this case, the faulty phase can only generate a two-level waveform. We need to modify (3-17) into (3-19).

$$X_a = X_b = X_c = 2 \cdot (1-e^{-\lambda_3 t})(e^{-\lambda_1 t})^4 \cdot (e^{-\lambda_2 t})^4 \cdot (e^{-\lambda_3 t}) \tag{3-19}$$

If we only consider the fault tolerant operation in which both the maximum modulation index and the waveform quality are the same as normal operation, then all the devices must be healthy, and the reliability function can be expressed by:

$$R_{NPC\_single\_open} = T_a \cdot T_b \cdot T_c \cdot Q \tag{3-20}$$

Then the reliability function of the converter has the same expression as (3-18).

4) Reliability function under multiple device open failure conditions

According to Table 3-9 and Table 3-14, for the fault tolerant operation under multiple device open failure conditions, it allows at most one faulty phase with "reduction fault" status, while the status of the other two phases can be "healthy" or "no reduction fault (2-level)".

We define $X_{1|x=a,b,c}$ as the probability that all of S_{x1}, S_{x4}, D_{x1} and D_{x4} in phase *x* are healthy, $X_{2|x=a,b,c}$ as the probability that all of S_{x2}, S_{x3}, D_{x5} and D_{x6} in phase *x* are healthy, and $X_{3|x=a,b,c}$ as the probability that both D_{x2} and D_{x3} in phase *x* are healthy. $T_{x|x=a,b,c}$ is defined as the probability that all of the devices S_{x1}/D_{x1} through S_{x4}/D_{x4} in phase *x* are healthy. So we have:

$$A_1 = B_1 = C_1 = (e^{-\lambda_1 t})^2 \cdot (e^{-\lambda_2 t})^2 \quad \textbf{(3-21)}$$

$$A_2 = B_2 = C_2 = (e^{-\lambda_1 t})^2 (e^{-\lambda_3 t})^2 \quad \textbf{(3-22)}$$

$$A_3 = B_3 = C_3 = (e^{-\lambda_2 t})^2 \quad \textbf{(3-23)}$$

$$T_a = T_b = T_c = (e^{-\lambda_1 t})^4 \cdot (e^{-\lambda_2 t})^4 \quad \textbf{(3-24)}$$

The converter reliability function is then express by:

$$R_{NPC\_mutiple\_open} = \left((1 - A_1 \cdot A_3) \cdot A_2 \cdot T_b \cdot T_c + (1 - B_1 \cdot B_3) \cdot B_2 \cdot T_a \cdot T_c + (1 - C_1 \cdot C_3) \cdot C_2 \cdot T_a \cdot T_b + T_a \cdot T_b \cdot T_c\right) \cdot Q \quad \textbf{(3-25)}$$

However, in (3-25), it does not consider the fault tolerant operation solution, in which only the upper or lower dc-link capacitor is used to generate a two-level waveform, as shown in Fig. 3.22. Therefore, we also need to calculate the reliability function under this operating condition, and exclude the common part from the reliability function in (3-25) in order to avoid the double counting. We define *T* as the probability that all the S_{x4}, D_{x4} and D_{x3} in the

three phases are healthy. $P_{x|x=a,b,c}$ is the probability that all the devices S_{x1}, D_{x1} and D_{x2} in phase *x* are healthy. $\bar{P}_{x|x=a,b,c}$ is the probability that one or more failure occur in S_{x1}, D_{x1} and D_{x2} in phase *x*. Therefore, we have:

$$T = (e^{-\lambda_1 t})^3 \cdot (e^{-\lambda_2 t})^6 \quad \textbf{(3-26)}$$

$$P_a = P_b = P_c = (e^{-\lambda_1 t}) \cdot (e^{-\lambda_2 t})^2 \quad \textbf{(3-27)}$$

$$\bar{P}_a = \bar{P}_b = \bar{P}_c = 1 - (e^{-\lambda_1 t}) \cdot (e^{-\lambda_2 t})^2 \quad \textbf{(3-28)}$$

The converter reliability function can be express by:

$$R_{NPC\_mutiple\_open} = 2 \cdot A_2 \cdot B_2 \cdot C_2 \cdot T \cdot \left(\bar{P}_a \cdot \bar{P}_b \cdot P_c + \bar{P}_b \cdot \bar{P}_c \cdot P_a + \bar{P}_a \cdot \bar{P}_c \cdot P_b + \bar{P}_a \cdot \bar{P}_b \cdot \bar{P}_c \right) Q \quad \textbf{(3-29)}$$

Therefore, the final reliability function of the 3L-NPC converter under multiple device open failure conditions should be the sum of the results in (3-25) and (3-29).

In some applications, if it requires that the maximum modulation index is 1.15 during fault tolerant operation, then the status of faulty phases can not be “reduction fault”. This means all the devices S_{x1}/D_{x1} through S_{x4}/D_{x4} in phase *x* must be healthy. Therefore the reliability function of the converter under this operating condition is given by:

$$R_{NPC\_mutiple\_open} = T_a \cdot T_b \cdot T_c \cdot Q \quad \textbf{(3-30)}$$

In some applications with more stringent requirements, both the maximum modulation index and the output voltage and current waveform quality are required to be the same as normal operation. In this case, all the devices in the converter must be healthy. Therefore, the reliability function is expressed by:

$$R_{NPC\_mutiple\_open} = \left(A_1 \cdot A_2 \cdot A_3 \cdot B_1 \cdot B_2 \cdot B_3 \cdot C_1 \cdot C_2 \cdot C_3 \right) \cdot Q \quad \textbf{(3-31)}$$

3.3.3.2 3L-ANPC converters

We define $T_{x|x=a,b,c}$ as the probability that all the devices in phase x are healthy, given by:

$$T_a = T_b = T_c = (e^{-\lambda_1 t})^6 \cdot (e^{-\lambda_2 t})^4 (e^{-\lambda_3 t})^2 \quad \textbf{(3-32)}$$

1) Reliability function under single device short failure condition

According to Table 3-6, a 3L-ANPC converter can continue operating under any single device short failure condition with a reduced maximum modulation index equal to 0.577.

We define $X_{x|x=a,b,c}$ as the probability that one device fails in phase x, as given by:

$$\begin{aligned} X_a = X_b = X_c = {} & 6 \cdot (1-e^{-\lambda_1 t})(e^{-\lambda_1 t})^5 \cdot (e^{-\lambda_2 t})^4 \cdot (e^{-\lambda_3 t})^2 \\ & + 4 \cdot (1-e^{-\lambda_2 t})(e^{-\lambda_1 t})^6 \cdot (e^{-\lambda_2 t})^3 \cdot (e^{-\lambda_3 t})^2 \\ & + 2 \cdot (1-e^{-\lambda_3 t})(e^{-\lambda_1 t})^6 \cdot (e^{-\lambda_2 t})^4 \cdot (e^{-\lambda_3 t}) \end{aligned} \quad \textbf{(3-33)}$$

Then the converter reliability function is derived by:

$$R_{ANPC\_single\_short} = \left(T_a \cdot T_b \cdot X_c + T_b \cdot T_c \cdot X_a + T_a \cdot T_c \cdot X_b + T_a \cdot T_b \cdot T_c\right) \cdot Q \quad \textbf{(3-34)}$$

If we only consider the fault tolerant operations in which the maximum modulation index is still 1.15, then all the devices in the converter must be healthy. Thus the reliability function of the converter is given by:

$$R_{ANPC\_single\_short} = T_a \cdot T_b \cdot T_c \cdot Q \quad \textbf{(3-35)}$$

2) Reliability function under multiple device short failure conditions

According to Table 3-10 and Table 3-11, for multiple device short failure, at least two phases must have the "healthy" status, while the status of the other phase can be "reduction fault". We define $X_{x|x=a,b,c}$ as the probability that the status of phase x is "reduction fault" under multiple device short failure conditions, as given by:

$$X = \overline{T}_1 \cdot T_2 \cdot T_4 \cdot T_5 + T_1 \cdot \left(\overline{T}_4 \cdot T_3 \cdot T_6 + T_4 \cdot \left(1 - T_2 \cdot T_3 \cdot T_5 \cdot T_6\right)\right) \quad \textbf{(3-36)}$$

$$X_a = X_b = X_c = \left(1-(e^{-\lambda_1 t})\cdot(e^{-\lambda_2 t})\right)\cdot(e^{-\lambda_1 t})^3\cdot(e^{-\lambda_2 t})^2\cdot(e^{-\lambda_3 t}) + \left(1-(e^{-\lambda_1 t})\cdot(e^{-\lambda_2 t})\right)(e^{-\lambda_1 t})^3\cdot(e^{-\lambda_2 t})^2\cdot(e^{-\lambda_3 t}) + (e^{-\lambda_1 t})^2\cdot(e^{-\lambda_2 t})^2\cdot\left(1-(e^{-\lambda_1 t})^4\cdot(e^{-\lambda_2 t})^2\cdot(e^{-\lambda_3 t})^2\right) \quad \textbf{(3-37)}$$

Then, the converter reliability function is expressed by:

$$R_{ANPC\_multiple\_short} = (T_a\cdot T_b\cdot X_c + T_b\cdot T_c\cdot X_a + T_a\cdot T_c\cdot X_b + T_a\cdot T_b\cdot T_c)\cdot Q \quad \textbf{(3-38)}$$

If we only consider the fault tolerant operations in which the maximum modulation index is still 1.15, then all the devices in the converter must be healthy. In this case, the reliability function of the converter is given by:

$$R_{ANPC\_multiple\_short} = T_a\cdot T_b\cdot T_c\cdot Q \quad \textbf{(3-39)}$$

3) Reliability function under single device open failure condition

According to Table 3-5, the 3L-ANPC converter can continue operating under any single device open failure condition. Therefore, the reliability function is the same as (3-34).

If we only consider the fault tolerant operation in which both the maximum modulation index and the waveform quality are the same as normal operation, then the status of the faulty phase must be “no reduction fault”. Therefore we need to modify (3-33) into:

$$X_a = X_b = X_c = 2\cdot(1-e^{-\lambda_1 t})(e^{-\lambda_1 t})^5\cdot(e^{-\lambda_2 t})^4\cdot(e^{-\lambda_3 t})^2 + 2\cdot(1-e^{-\lambda_3 t})(e^{-\lambda_1 t})^6\cdot(e^{-\lambda_2 t})^4\cdot(e^{-\lambda_3 t}) \quad \textbf{(3-40)}$$

Then, the reliability function has the same expression as (3-34).

4) Reliability function under multiple device open failure conditions

According to Table 3-8 and Table 3-9, for multiple device open failure in the 3L-ANPC converter, Table 3-18 shows the possible combinations of the three phase status for the successful operation of the converter. In the table, the phase status “3L output” means the

phase can generate all three voltage levels. “2L output” means the phase can only generate $\pm V_{dc}/2$. “0” means the phase can generate zero level, but not all three voltage levels.

The probability that one phase has the status of “0” is given by:

$$\begin{aligned} P_0 = {} & S_2 \cdot D_5 \cdot \left[D_2 \cdot S_5 \cdot \left(1 - S_1 \cdot S_3 \cdot S_4 \cdot D_1 \cdot D_3 \cdot D_4\right) + \bar{D}_2 \cdot S_3 \cdot D_6 + D_2 \cdot \bar{S}_5 \cdot S_3 \cdot D_6 \cdot \left(1 - S_1 \cdot S_4 \cdot D_1 \cdot D_3 \cdot D_4\right) \right] \\ & + \bar{S}_2 \cdot S_6 \cdot D_3 \left[1 - \left(1 - D_2 \cdot S_5\right) \cdot \left(1 - S_3 \cdot D_6\right) \right] \\ & + S_2 \cdot \bar{D}_5 \cdot S_6 \cdot D_3 \left(\bar{S}_3 \cdot S_5 \cdot D_2 + S_3 \cdot \left[\bar{D}_2 \cdot D_6 + D_2 \cdot \left(1 - \bar{D}_6 \cdot \bar{S}_5\right) \cdot \left(1 - S_1 \cdot S_4 \cdot D_1 \cdot D_4\right) \right] \right) \end{aligned} \quad \textbf{(3-41)}$$

Here, $S_{m|m=1\sim6}$ and $D_{m|m=1\sim6}$ are the probability that the device S_m and D_m are healthy, respectively. $\bar{S}_m = 1 - S_m$ and $\bar{D}_m = 1 - D_m$ represents the probability that the device S_m and D_m fail, respectively. So we have:

$$\begin{aligned} P_0 = {} & (e^{-\lambda_1 t})^2 \cdot (e^{-\lambda_2 t}) \cdot (e^{-\lambda_3 t}) - (e^{-\lambda_1 t})^5 \cdot (e^{-\lambda_2 t})^4 \cdot (e^{-\lambda_3 t}) + (e^{-\lambda_1 t})^2 \cdot (1 - e^{-\lambda_2 t}) \cdot (e^{-\lambda_3 t})^2 \\ & + (1 - e^{-\lambda_1 t}) \cdot (e^{-\lambda_1 t})^2 \cdot (e^{-\lambda_2 t}) \cdot (e^{-\lambda_3 t})^2 - (1 - e^{-\lambda_1 t}) \cdot (e^{-\lambda_1 t})^4 \cdot (e^{-\lambda_2 t})^4 \cdot (e^{-\lambda_3 t})^2 \\ & + (1 - e^{-\lambda_1 t}) \cdot (e^{-\lambda_1 t})^2 \cdot (e^{-\lambda_2 t}) \cdot (e^{-\lambda_3 t}) + (1 - e^{-\lambda_1 t}) \cdot (e^{-\lambda_1 t})^2 \cdot (e^{-\lambda_2 t})^2 \\ & - (1 - e^{-\lambda_1 t}) \cdot (e^{-\lambda_1 t})^3 \cdot (e^{-\lambda_2 t})^2 \cdot (e^{-\lambda_3 t}) + (1 - e^{-\lambda_1 t}) \cdot (e^{-\lambda_1 t})^3 \cdot (e^{-\lambda_2 t})^2 \cdot (1 - e^{-\lambda_3 t}) \\ & + (e^{-\lambda_1 t})^3 \cdot (1 - e^{-\lambda_2 t}) \cdot (e^{-\lambda_2 t}) \cdot (1 - e^{-\lambda_3 t}) \cdot (e^{-\lambda_3 t}) + (e^{-\lambda_1 t})^3 \cdot (e^{-\lambda_2 t})^2 \cdot (1 - e^{-\lambda_3 t}) \\ & - (e^{-\lambda_1 t})^5 \cdot (e^{-\lambda_2 t})^4 \cdot (1 - e^{-\lambda_3 t}) - (1 - e^{-\lambda_1 t}) \cdot (e^{-\lambda_1 t})^3 \cdot (e^{-\lambda_2 t})^2 \cdot (1 - e^{-\lambda_3 t})^2 \\ & + (1 - e^{-\lambda_1 t}) \cdot (e^{-\lambda_1 t})^5 \cdot (e^{-\lambda_2 t})^4 \cdot (1 - e^{-\lambda_3 t})^2 \end{aligned} \quad \textbf{(3-42)}$$

Table 3-18 Possible operating conditions of a 3L-ANPC converter for multiple device open failure

Phase A status	Phase B status	Phase C status
0	2L output /3L output	2L output /3L output
2L output /3L output	0	2L output /3L output
2L output /3L output	2L output /3L output	0
2L output /3L output	2L output /3L output	2L output /3L output

We define T as the probability that S_{x1}/D_{x1} through S_{x4}/D_{x4} are all healthy in phase x, as given by:

$$T = S_1 \cdot S_2 \cdot S_3 \cdot S_4 \cdot D_1 \cdot D_2 \cdot D_3 \cdot D_4 = (e^{-\lambda_1 t})^4 \cdot (e^{-\lambda_2 t})^4 \quad \textbf{(3-43)}$$

The probability that one phase has the status of "3L output" is given by:

$$P_{3L} = (\bar{D}_5 \cdot S_6 \cdot \bar{S}_5 \cdot D_6 + \bar{D}_5 \cdot S_6 \cdot S_5 + D_5 \cdot \bar{S}_5 \cdot D_6 + D_5 \cdot S_5) \cdot T \quad \textbf{(3-44)}$$

$$\begin{aligned} P_{3L} = {} & [(1-e^{-\lambda_1 t}) \cdot (1-e^{-\lambda_3 t}) \cdot (e^{-\lambda_1 t}) \cdot (e^{-\lambda_3 t}) + (1-e^{-\lambda_3 t}) \cdot (e^{-\lambda_1 t})^2 + (1-e^{-\lambda_1 t}) \cdot (e^{-\lambda_3 t})^2 \\ & + (e^{-\lambda_1 t}) \cdot (e^{-\lambda_3 t})] \cdot (e^{-\lambda_1 t})^4 \cdot (e^{-\lambda_2 t})^4 \end{aligned} \quad \textbf{(3-45)}$$

The probability that one phase has the status of "2L output" is given by:

$$P_{2L} = (\bar{D}_5 \cdot \bar{S}_6 + \bar{D}_5 \cdot S_6 \cdot \bar{D}_6 \cdot \bar{S}_5 + D_5 \cdot \bar{D}_6 \cdot \bar{S}_5) \cdot T \quad \textbf{(3-46)}$$

$$\begin{aligned} P_{2L} = {} & \left[(1-e^{-\lambda_1 t}) \cdot (1-e^{-\lambda_3 t}) + (1-e^{-\lambda_1 t}) \cdot (1-e^{-\lambda_3 t})^2 \cdot (e^{-\lambda_1 t}) + (1-e^{-\lambda_1 t}) \cdot (1-e^{-\lambda_3 t}) \cdot (e^{-\lambda_3 t}) \right] \\ & \cdot (e^{-\lambda_1 t})^4 \cdot (e^{-\lambda_2 t})^4 \end{aligned} \quad \textbf{(3-47)}$$

Then, the converter reliability function is expressed by:

$$R_{ANPC\_mutiple\_open} = \left(3 \cdot P_0 \cdot (P_{2L} + P_{3L})^2 + \left(P_{2L} + P_{3L} \right)^3 \right) \cdot Q \quad \textbf{(3-48)}$$

However, in (3-48), it does not consider the fault tolerant operation solution, in which only the upper or lower dc-link capacitor is used to generate a two-level waveform, as shown in Fig. 3.22. Therefore, we also need to calculate the reliability function under this operating condition, and exclude the common part from the reliability function in (3-48) in order to avoid the double counting. We define P_{0-} as the probability that the faulty phase can only generate 0 and $-V_{dc}/2$ output voltage levels (and the phase status is "P_{0-}"), as given by:

$$\begin{aligned} P_{0-} = {} & S_3 \cdot S_4 \cdot D_3 \cdot D_4 \cdot \left\{ S_2 \cdot D_5 \cdot \left[D_2 \cdot S_5 \cdot (1 - S_1 \cdot D_1) + \bar{D}_2 \cdot D_6 + D_2 \cdot \bar{S}_5 \cdot D_6 \cdot (1 - S_1 \cdot D_1) \right] \right. \\ & \left. + \bar{S}_2 \cdot S_6 \cdot \left[1 - \bar{D}_6 (1 - D_2 \cdot S_5) \right] + S_2 \cdot \bar{D}_5 \cdot S_6 \cdot \left[\bar{D}_2 \cdot D_6 + D_2 \cdot \left(1 - \bar{D}_6 \cdot \bar{S}_5 \right) \cdot (1 - S_1 \cdot D_1) \right] \right\} \end{aligned} \quad \textbf{(3-49)}$$

$$
\begin{aligned}
P_{0-} = {} & (e^{-\lambda_1 t})^4 \cdot (e^{-\lambda_2 t})^3 \cdot (e^{-\lambda_3 t}) - (e^{-\lambda_1 t})^5 \cdot (e^{-\lambda_2 t})^4 \cdot (e^{-\lambda_3 t}) + (e^{-\lambda_1 t})^3 \cdot (1-e^{-\lambda_2 t}) \cdot (e^{-\lambda_2 t})^2 \cdot (e^{-\lambda_3 t})^2 \\
& + (1-e^{-\lambda_1 t}) \cdot (e^{-\lambda_1 t})^3 \cdot (e^{-\lambda_2 t})^3 \cdot (e^{-\lambda_3 t})^2 - (1-e^{-\lambda_1 t}) \cdot (e^{-\lambda_1 t})^4 \cdot (e^{-\lambda_2 t})^4 \cdot (e^{-\lambda_3 t})^2 \\
& + (1-e^{-\lambda_1 t}) \cdot (e^{-\lambda_1 t})^3 \cdot (e^{-\lambda_2 t})^2 - (1-e^{-\lambda_1 t}) \cdot (e^{-\lambda_1 t})^3 \cdot (e^{-\lambda_2 t})^2 \cdot (1-e^{-\lambda_3 t}) \\
& + (1-e^{-\lambda_1 t}) \cdot (e^{-\lambda_1 t})^4 \cdot (e^{-\lambda_2 t})^3 \cdot (1-e^{-\lambda_3 t}) + (e^{-\lambda_1 t})^4 \cdot (1-e^{-\lambda_2 t}) \cdot (e^{-\lambda_2 t})^2 \cdot (1-e^{-\lambda_3 t}) \cdot \left(e^{-\lambda_3 t}\right) \\
& + (e^{-\lambda_1 t})^4 \cdot (e^{-\lambda_2 t})^3 \cdot (1-e^{-\lambda_3 t}) - (e^{-\lambda_1 t})^5 \cdot (e^{-\lambda_2 t})^4 \cdot (1-e^{-\lambda_3 t}) \\
& - (1-e^{-\lambda_1 t}) \cdot (e^{-\lambda_1 t})^4 \cdot (e^{-\lambda_2 t})^3 \cdot (1-e^{-\lambda_3 t})^2 + (1-e^{-\lambda_1 t}) \cdot (e^{-\lambda_1 t})^5 \cdot (e^{-\lambda_2 t})^4 \cdot (1-e^{-\lambda_3 t})^2
\end{aligned}
\tag{3-50}
$$

For the fault tolerant operation, two phases can have the "P_{0-}" status and the remaining phase has "3L output" status. Or, the status of all three phases is "P_{0-}". The converter reliability function for this type of operation is:

$$
R_{NPC\_mutiple\_open} = 2 \times \left(3 \times {P_{0-}}^2 \cdot P_{3L} + {P_{0-}}^3\right) \cdot Q \tag{3-51}
$$

Therefore, the final reliability function of the 3L-ANPC converter under multiple device open failure conditions should be the sum of the results in (3-48) and (3-51).

If we only consider the fault tolerant operation in which the maximum modulation index is still 1.15 during the fault tolerant operation, then the all the three phases can have the status of either "2L output" or "3L output". Therefore the reliability function is expressed by:

$$
R_{ANPC\_mutiple\_open} = \left(P_{2L} + P_{3L}\right)^3 \cdot Q \tag{3-52}
$$

If we only consider the fault tolerant operation in which the maximum modulation index and waveform quality are the same as normal operation, then all the three phases must have the "3L output" status. Therefore the reliability is expressed by:

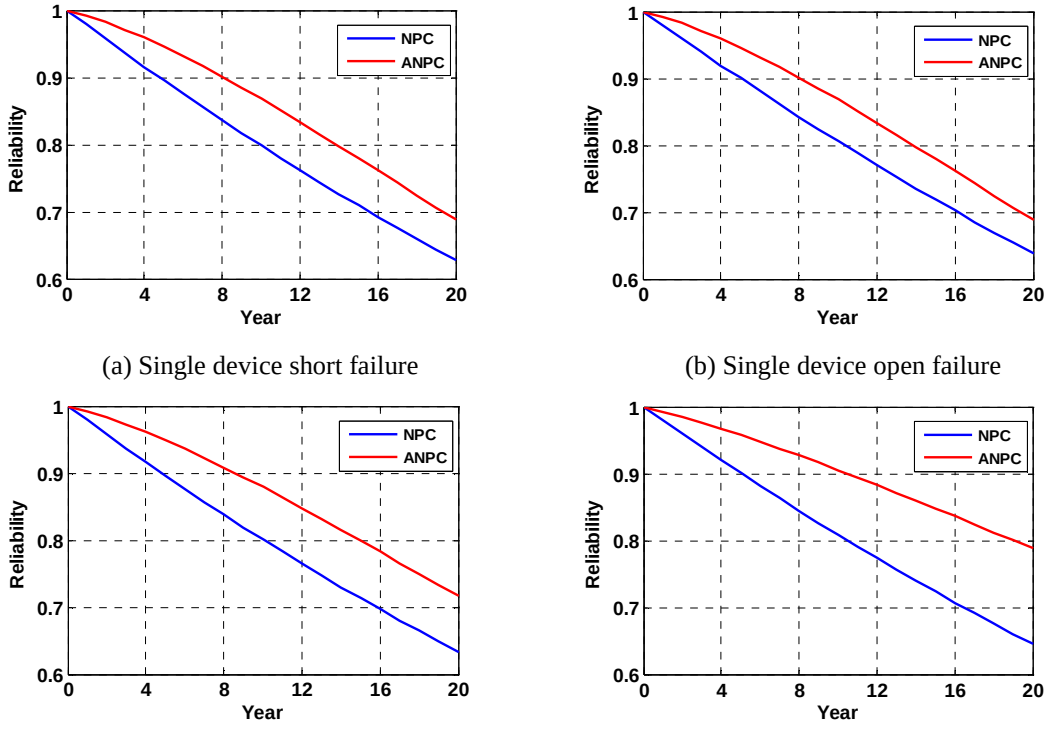
$$
R_{ANPC\_mutiple\_open} = {P_{3L}}^3 \cdot Q \tag{3-53}
$$

3.3.4 Reliability Comparison of 3L-NPC and 3L-ANPC Converters

Based on the above results of the reliability function of the 3L-NPC and 3L-ANPC converters, we plot and compare their reliability functions calculated over a span of 20 years

for single and multiple device open and short failure conditions. Considering the requirements of different applications, the comparison is studied for three cases as follows.

- Case 1: the reliability function includes all the possible fault tolerant operating conditions for the 3L-NPC and the 3L-ANPC converters. In this case, the maximum modulation index and the output voltage and current waveform quality can be the same or lower compared to those in normal operation. The comparison for the reliability of the two converters are plotted for single device short failure (ssf), single device open failure (sof), multiple device short failure (msf) and multiple device open failure (mof) in Fig. 3.24 (a) through (d), respectively.



(a) Single device short failure

(b) Single device open failure

(c) Multiple device short failure

(d) Multiple device open failure

Fig. 3.24 Reliability function comparison for the 3L-NPC and 3L-ANPC converters (Case 1)

In order to look into the reliability variation ΔR for the two converters, we define:

$$\Delta R = \left(R_{ANPC} - R_{NPC} \right) / R_{NPC} \tag{3-54}$$

Here, R_{ANPC} and R_{NPC} are the reliability of the 3L-ANPC and 3L-NPC converters, respectively.

The reliability variation ΔR for Case 1 is plotted in Fig. 3.25.

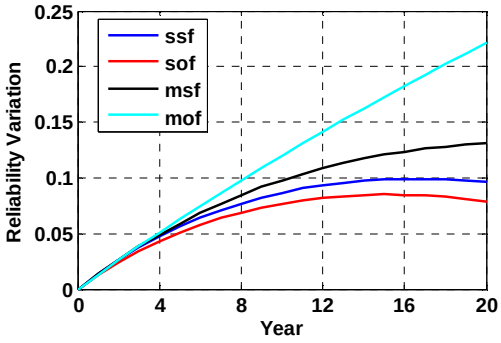
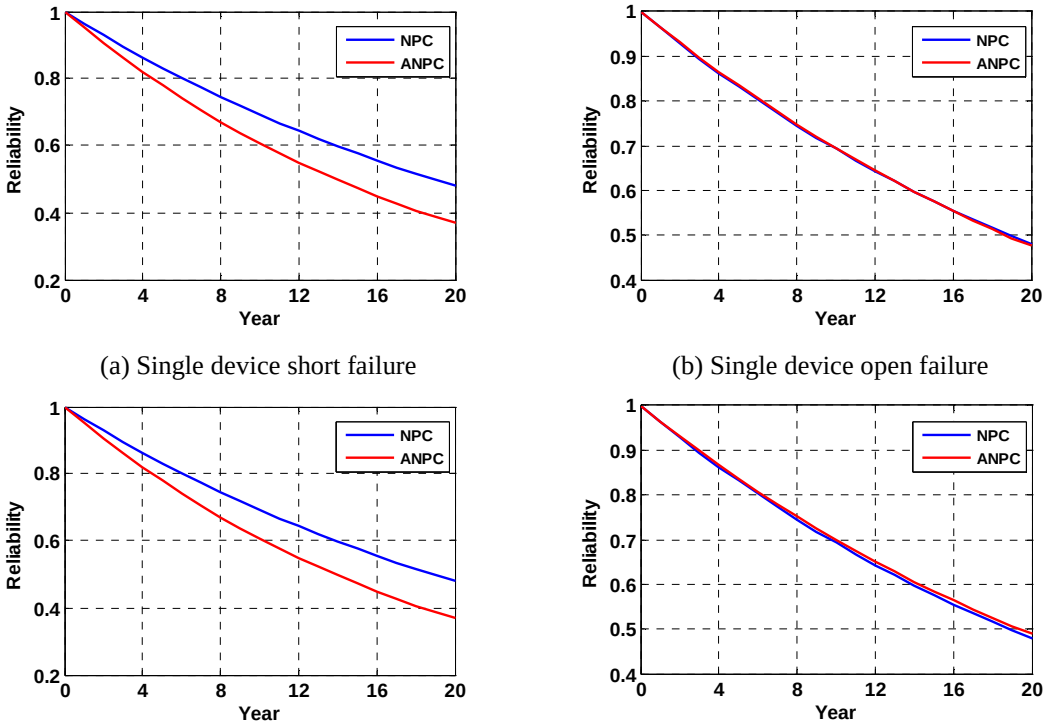


Fig. 3.25 Reliability variations for the 3L-NPC and 3L-ANPC converters (Case 1)

- Case 2: the reliability function only includes the fault tolerant operating conditions in which both the maximum modulation index and the output voltage and current waveform quality are the same as those in normal operation. The comparison for the reliability of the two converters are plotted for single device short failure, single device open failure, multiple device short failure and multiple device open failure in Fig. 3.26 (a) through (d), respectively.



(a) Single device short failure

(b) Single device open failure

(c) Multiple device short failure

(d) Multiple device open failure

Fig. 3.26 Reliability function comparison for the 3L-NPC and 3L-ANPC converters (Case 2)

The reliability variation ΔR for Case 2 is plotted in Fig. 3.27

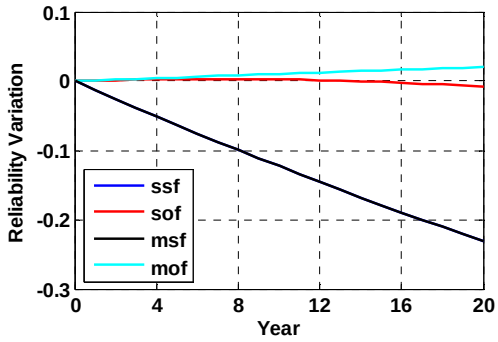
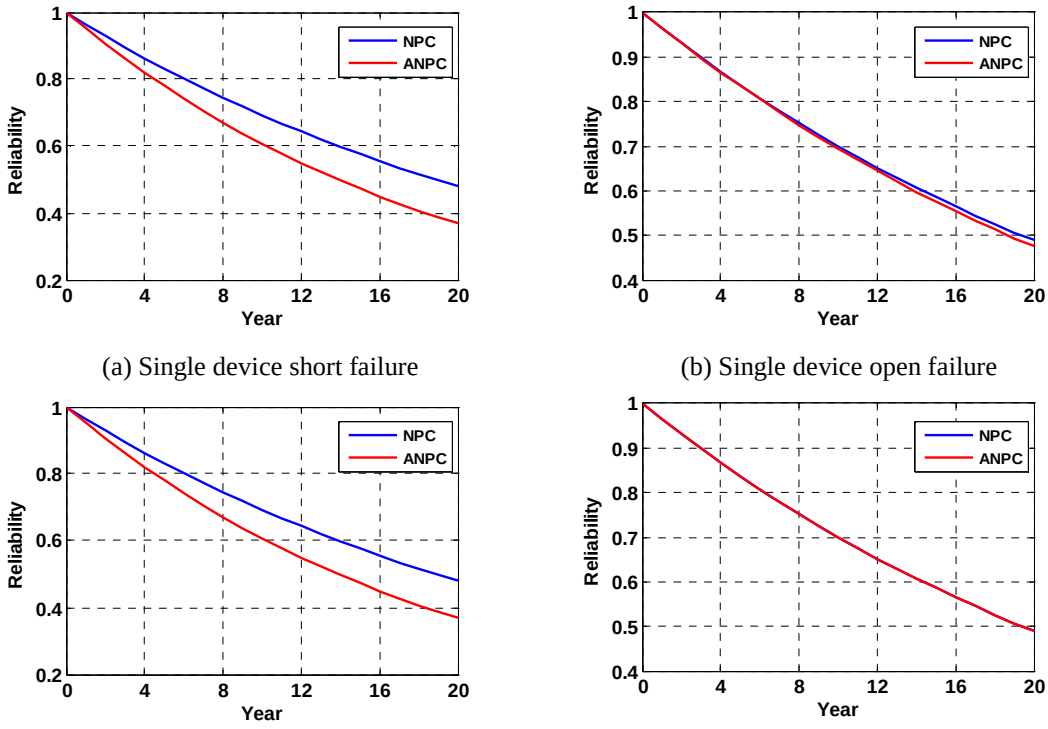


Fig. 3.27 Reliability variations for the 3L-NPC and 3L-ANPC converters (Case 2)

- Case 3: the reliability function only includes the fault tolerant operating conditions in which the maximum modulation index is the same as that in normal operation. Compared to Case 2, the waveform quality is not considered in this case. The

comparison for the reliability of the two converters are plotted for single device short failure, single device open failure, multiple device short failure and multiple device open failure in Fig. 3.28 (a) through (d), respectively.



(a) Single device short failure

(b) Single device open failure

(c) Multiple device short failure

(d) Multiple device open failure

Fig. 3.28 Reliability function comparison for the 3L-NPC and 3L-ANPC converters (Case 3)

The reliability variation ΔR for Case 3 is plotted in Fig. 3.29.

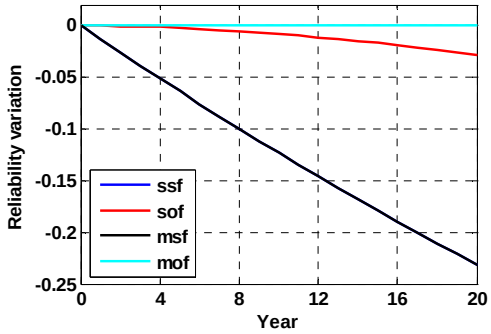


Fig. 3.29 Reliability variations for the 3L-NPC and 3L-ANPC converters (Case 3)

For Case 1, the reliability analysis and comparison for the 3L-NPC and 3L-ANPC converters can be used for motor drive applications, in which a reduced maximum modulation index is usually allowed during the fault tolerant operation, and the motor drive system can continue working, but at a lower speed or lower output power. From Fig. 3.24 and Fig. 3.25, it is observed that the 3L-ANPC converters have higher reliability compared to the 3L-NPC converters for the applications belonging to Case 1. For example, considering over a span of 16 years, the 3L-ANPC converters have an increased reliability around 18%, 12.5%, 10% and 8.5% compared to the 3L-NPC converters for multiple device open failure, multiple device short failure, single device short failure and single device open failure, respectively. For Case 2 and Case 3, the results reflect the converter reliability analysis and comparison for the grid-connected applications, in which the reduced maximum modulation index is not allowed since the converter output is connected to the grid with a fixed voltage. Moreover, Case 2 also accounts for the applications with more stringent harmonic requirements. In such applications, even during fault tolerant operation, the converters are still required to generate the same waveform quality as normal operation. From Fig. 3.26 through Fig. 3.29, it shows that, in the applications belonging to Case 2 and Case 3, the reliability of the 3L-ANPC converter is similar to that of the 3L-NPC converter for single and multiple device open failure. However, for single and multiple device short failure, the NPC converters have a much higher reliability than the 3L-ANPC converters.

Therefore, from the reliability aspect, the 3L-ANPC converter is better than the 3L-NPC converter for motor drive applications. However, for grid-connected applications, the 3L-NPC converter shows overall better reliability.

3.4 Control of ANPC Generator Converter for Large Wind Turbine

3.4.1 Application of ANPC Generator Converter for Large Wind Turbine

The MW wind turbine system with a direct-driven PMSG and a full-scale converter is becoming more attractive for offshore wind power generation. The main advantages of this configuration include low mechanical maintenance requirement, robust gearless construction, high efficiency of PM machine and better grid-code fulfillment. In this configuration, a back-to-back 3L-NPC converter is usually used. The circuit diagram of a 4-quadrant 3L-NPC wind power converter is shown in Fig. 3.30.

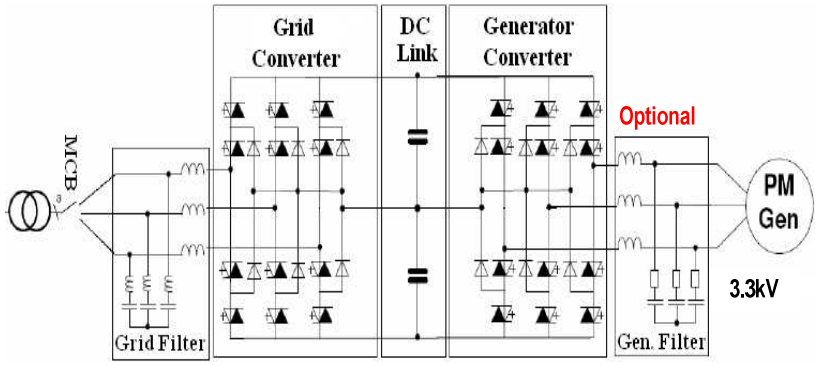


Fig. 3.30. Circuit diagram of 4-quadrant B2B 3L-NPC wind power converter

However, due to the drawback of the unequal loss distribution among the power devices in the 3L-NPC topology, the maximum output power of the converter is limited. Since the trend of the wind turbines is moving toward higher unit capacity, it is more practical to increase the converter power rating by optimizing the device utilization, so as to match the large wind turbine capacity. Moreover, when open and short circuit failure occurs on the power devices in the generator converter, the converter is usually required to be shut down to protect the wind turbine system. This will reduce the system availability and reliability, and

cause economic loss. Since today's wind turbine rating has reached multi-MW level, it is beneficial to maintain the wind turbine in service and continue supporting the real power under certain device failure conditions. This is also meaningful for the operation stability of the power system with a high percentage of wind power penetration.

In this work, we propose to apply a 3L-ANPC converter on the generator side of a MW direct-driven wind turbine system. The better thermal performance of the ANPC converter enables to support the wind turbine at higher power level. Moreover, the fault tolerant capability of the 3L-ANPC converter enables the wind turbine to remain in service and continue providing real power under device failure conditions. This unique feature is very meaningful, especially for offshore wind farm. Since the period between two service visits is long for offshore wind sites, the disconnection of the wind turbine caused by the power device failure is very costly. Therefore, the proposed solution enables to bring benefits in terms of reliability and economic saving. Fig. 3.31 shows the configuration of a direct-driven PMSG based large wind turbine system with a 3L-ANPC generator converter. On grid side, the converter can be either a 3L-NPC converter or a 3L-ANPC converter.

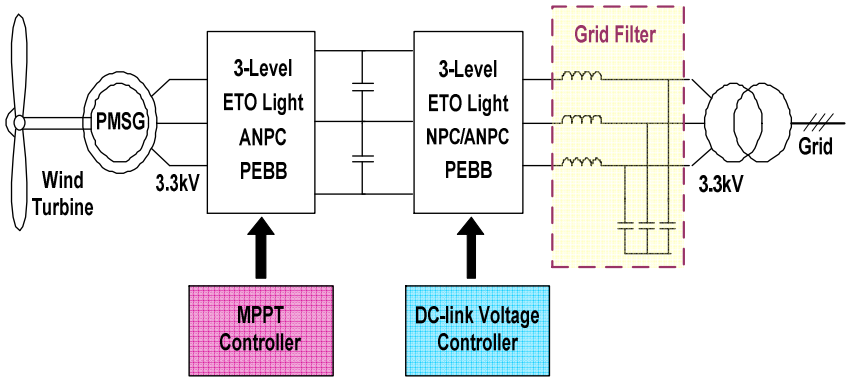


Fig. 3.31 Configuration of a large wind turbine system employing a 3L-ANPC generator converter

3.4.2 Control of ANPC Generator Converter

In this section, the control schemes of the 3L-ANPC generator converter for both normal operation (fault-free mode) and fault operation (device failure mode) are presented as follows.

3.4.2.1 Control scheme of ANPC generator converter under normal operation

The rotor aerodynamics of the wind turbine is expressed by [91]:

$$P_T = \frac{1}{2}\rho A_r C_p(\beta,\lambda) V_w{}^3 \tag{3-55}$$

Where P_T is the extracted power from the wind (W), ρ is the air density (kg/m^3), A_r is the area swept by the rotor (m^2), C_p is the power coefficient, λ is the tip speed ratio, V_w is the wind speed (m/s), β is the pitch angle of the rotor blades (degree).

The power coefficient C_p is expressed by:

$$C_p(\beta,\lambda) = C_1 \cdot (C_2 \cdot \frac{1}{\Lambda} - C_3 \cdot \beta - C_4 \cdot \beta^x - C_5) \cdot e^{-C_6 \cdot \frac{1}{\Lambda}} + C_7 \cdot \lambda \tag{3-56}$$

Here, C_1=0.5176, C_2=116, C_3=0.4, C_4=0, C_5=5, C_6=21, C_7=0.0068, and $\frac{1}{\Lambda}$ is defined as:

$$\frac{1}{\Lambda} = \frac{1}{\lambda + 0.08\beta} - \frac{0.035}{1+\beta^3} \tag{3-57}$$

The typical wind power curve is shown in Fig. 3.32.

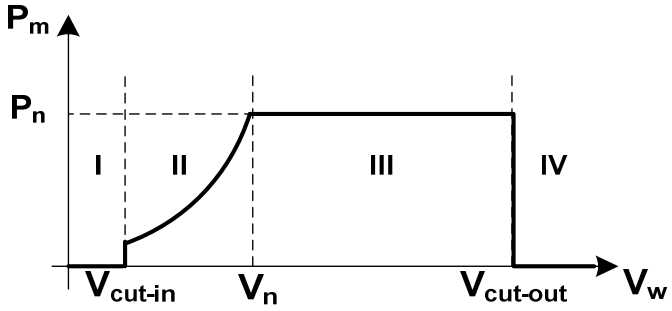


Fig. 3.32 Typical wind power curve

In normal operation, depending on the region that the wind speed belongs to, as shown in Fig. 3.32, different control schemes are used for the 3L-ANPC generator converter [92]:

- When the wind speed is below the cut-in speed V_{cut_in} (region I) or beyond the cut_out speed V_{cut_out} (region IV), the generator converter and the wind turbine are shut down, thus no real power is transferred to the grid.
- When the wind speed is between the cut-in speed V_{cut_in} and the rated speed V_n (region II), the controller of the generator converter implements the Maximum Power Point Tracking (MPPT) algorithm to extract the maximum power from wind by adjusting the generator speed to keep the optimal tip speed ratio λ_{opt}. In this control mode, the pitch angle is usually fixed to zero. In this work, we mainly focus on the control scheme of the 3L-ANPC generator converter for the wind speed in region II.
- When the wind speed is between the rated speed V_n and the cut-out speed V_{cut_out} (region III), the controller of generator converter needs to limit the extracted power at the rated level. This is done by maintaining the generator speed constant and adjusting the pitch angle.

For the grid side 3L-NPC or 3L-ANPC converter, the control scheme is to regulate the DC bus voltage, the dc-link neutral-point balance and the grid-side power factor. Fig. 3.33 shows the controller diagram for the grid converter. It is a synchronous voltage oriented control (VOC) with PI controllers, and has been widely used for grid-connected applications [93]. This control strategy is based on the coordinate transformation between the stationary *abc* and the synchronous *dq* reference frames. The inner current loops assure fast transient response and high static performance. The decomposition of the AC current in *dq* axes

provides the decoupled control for the active power (or DC bus voltage) and reactive power (or AC voltage). In this work, the control scheme comprises the DC voltage controller and the active component of the current in the *d*-axis, while the reactive power and the reactive component of the current are controlled in the *q*-axis. The dc-link neutral-point balance control is implemented in the PWM modulator by using the redundant switching states of the 3L-NPC or 3L-ANPC converter.

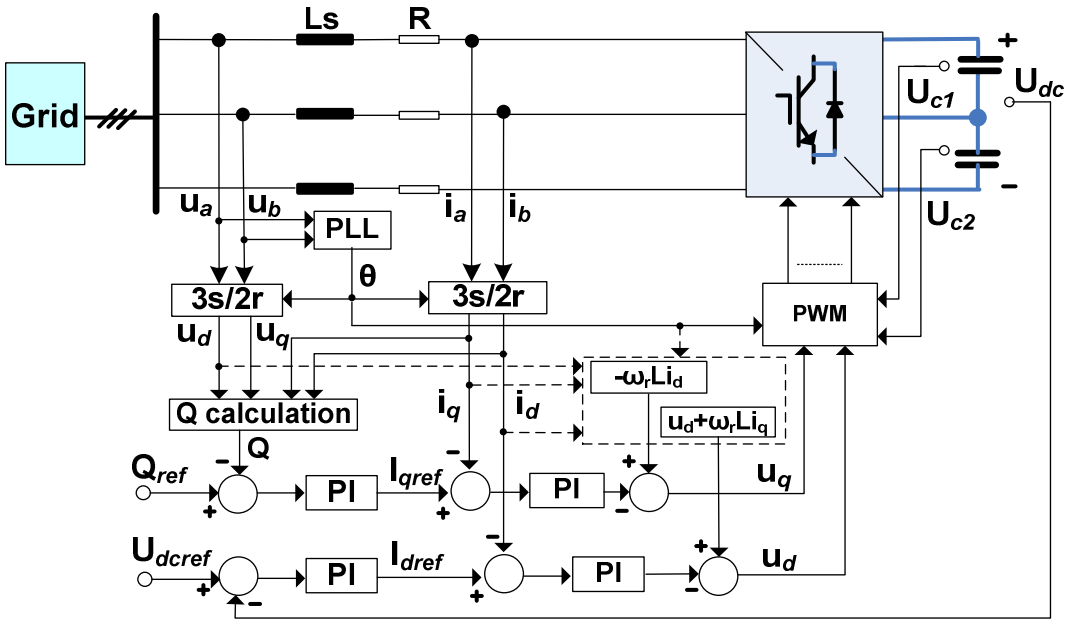


Fig. 3.33 Controller diagram of the grid side converter

The 3L-ANPC generator converter implements the MPPT control. The controller diagram is shown in Fig. 3.34. The Field Oriented Control (FOC) is used to perform the speed control of the PMSG by decoupling the flux linkage and torque control [94]. The *d*-axis is rotating along the magnetic field direction. The reference of the *d*-axis current is set to be zero, so that a simple torque control can be achieved only by controlling the *q*-axis current. The outer loop calculates the torque reference T_{em_ref} based on the MPPT algorithm [95]. The

reference of the *q*-axis current is proportional to the torque reference. The MPPT algorithm keeps the power efficient C_p at its maximum value C_{pmax}. The optimal torque reference T_{em_ref} is given by the equations below.

$$T_{em\_ref} = K \cdot \omega_r^{\,2} \tag{3-58}$$

$$K = \frac{1}{2}\rho \cdot A_r \cdot R^3 \frac{C_{p\max}}{\lambda_{opt}^{\,3}} \tag{3-59}$$

$$C_{p\max} = C_p\left(\beta\big|_{\beta=0}, \lambda_{opt}\right) \tag{3-60}$$

Here, λ_{opt} is the optimal tip speed ratio, C_{pmax} is the maximum power coefficient, ω_r is rotor speed, and R is blade radius.

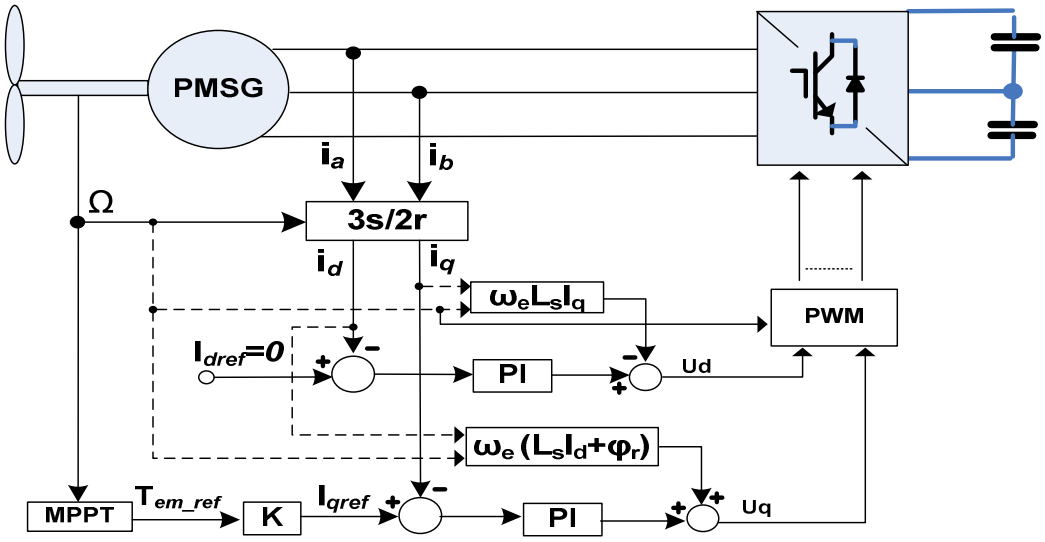


Fig. 3.34 Controller diagram of the generator side converter under normal operation

3.4.2.2 Control scheme of ANPC generator converter under fault operation

According to the previous analysis for the fault tolerant ability of the 3L-ANPC converter, through the switching states and switching sequences reconfiguration and modulation signals modification, the 3L-ANPC converter is still able to operate under single device open and

short failure condition. The principles of the fault tolerant operation and control strategies are recalled and summarized as below.

- If S_5/D_5 or S_6/D_6 has open failure, referred to as *type (a)* failure, then by choosing the proper switching state and switching sequence, the 3L-ANPC converter can be derived into a configuration which is similar to the 3L-NPC converter. During the fault tolerant operation, the maximum modulation index is still 1.15, and the voltage and current waveform quality are not impacted.
- For other device failure conditions, referred to as *type (b)* failure, the faulty phase is connected to the neutral-point of the dc-link through a proper "zero" switching state. Meanwhile, the reference voltage signals are modified to maintain the balanced line-to-line voltage of the converter. During the fault tolerant operation, the maximum modulation index is reduced to 0.577.

For *type (a)* device failure, since the maximum modulation index and output voltage are not reduced by using the fault tolerant control, the controller of the generator converter can still implement MPPT algorithm and extract the maximum power for the whole wind speed range in region II shown in Fig. 3.32. The wind turbine operation is almost the same as normal operation.

However, for *type (b)* device failure, since the maximum modulation index is reduced to 0.577, the available maximum output voltage of the generator converter is limited, resulting in a limited adjustable speed range of the PMSG. This means that when the wind speed exceeds a certain limit, the MPPT algorithm will not be available anymore.

Table 3-19 shows the main parameters of the 5 MW wind turbine and PMSG [96] [97].

Table 3-19 Main parameters of the 5 MW wind turbine and PMSG

Wind Turbine Parameters		PMSG parameters	
Rate power P_n	5 MW	Rate power P_n	5 MW
Rated rotor speed n_r	14.8 rpm	Rated voltage (L-L RMS)	3.3 kV
Rotor diameter D	116 m	Rated current (RMS)	0.92 kA
Hub height	138 m	Power factor	0.95
Hub height mean speed	11.8 m/s	Phase resistor R_s	50 mΩ
Cut in wind speed	2.5 m/s	d-aix inductance $L_{md}+L_\sigma$	3.5218 mH
Cut out wind speed	25 m/s	q-aix inductance $L_{mq}+L_\sigma$	3.5218 mH
Rated wind speed	11.8 m/s	PM flux	14.3522Wb
Optimum tip speed ratio γ	7.6179	Number of pole pairs	118
Maximum power coefficient C_p	0.4746	Inertia factor	2.5e5 $kg.m^2$
Air density	1.225 kg/m^3	Friction factor	2.26e4 N.m.s

Since the stator resistance and inductance of the generator are very small, we first make an approximate assumption that the stator back-EMF voltage is the same as the stator voltage. Therefore the ratio between the rotor speed and the modulation index is almost constant. Using the fault tolerant control scheme for *type (b)* device failure, the maximum adjustable rotor speed, which corresponds to the maximum modulation index 0.577, is calculated by:

$$\omega_r = \frac{0.577}{1.078} \times 14.8\, rpm = 7.93\, rpm \tag{3-61}$$

Here, 1.078 is the modulation index at the rated operating point with 3.3 kV output line-to-line RMS voltage of the converter.

If the optimum tip speed ratio λ_{opt} is kept constant, then the maximum wind speed, at which the MPPT algorithm is still available, is given by:

$$V_w = \frac{0.577}{1.078} \times 11.8 m/s = 6.32\ m/s \tag{3-62}$$

So, in region II, when the wind speed is below 6.32 m/s, the MPPT algorithm can still be obtained by adjusting the rotor speed. However, when the wind speed is above 6.32 m/s, the

MPPT algorithm can not be achieved anymore because the required modulation index exceeds the available maximum limitation 0.577. Under this condition, we can transit the controller of the generator converter from the MPPT mode to the constant speed mode, in which the rotor speed is controlled to be constant at the maximum limit 7.93 rpm (about 0.83 rad/s). Fig. 3.35 shows the extracted wind power curve under the constant rotor speed mode. In this control mode, the pitch angle is still fixed to zero.

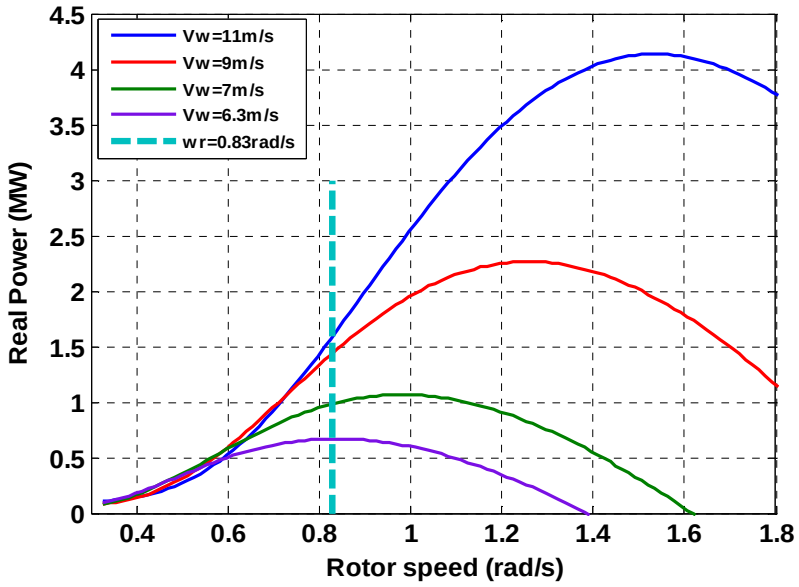


Fig. 3.35 Extracted wind power curve with the constant speed control for wind speed in region II

From Fig. 3.35, it is observed that, when the wind speed is higher than 6.32 m/s, although the wind turbine can not extract the same maximum power as that in normal operation, however when the generator operates at the constant rotor speed ω_r=7.93 rpm (0.83 rad/s), the wind turbine can still generates the amount of output power which is the allowable maximum value under *type (b)* device failure condition. If the rotor speed is lower than 0.83 rad/s, the generated power will also become smaller.

Here, we notice that another possible solution to further increase the extracted power under the *type (b)* fault tolerant operation is to increase the DC bus voltage of the converter, which can be controlled by the grid-side converter. Under *type (b)* failure, if the DC bus voltage is increased by ΔV, and then the available maximum rotor speed is derived by:

$$\omega_r = (1+\frac{\Delta V}{5000})\times 7.93\ rpm \quad \textbf{(3-63)}$$

Due to the linear relation between the rotor speed ω_r and the wind speed V_w under MPPT control mode, the maximum wind speed, at which the MPPT algorithm is still available with the increased DC bus voltage, is given by:

$$V_w = (1+\frac{\Delta V}{5000})\times 6.32\ m/s \quad \textbf{(3-64)}$$

Now we take the ETO Light ANPC PEBB as an example. The maximum long term DC voltage for the ETOs and 5SDF 10H4502 diodes is 2800V. The nominal DC bus voltage of the PEBB is 5000V. In Fig. 3.36, we plot the extracted power at different wind speed under different DC bus voltages ranging from 5000V to 5600V during the *type (b)* fault tolerant operation.

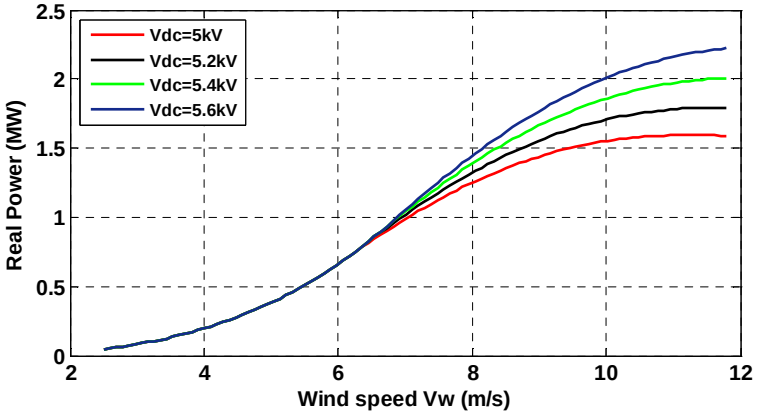


Fig. 3.36 Extracted power at different DC bus voltages under *type (b)* device failure

From Fig. 3.36, it can be found that by increasing the DC bus voltage, more power at higher wind speed can be extracted for *type (b)* failure. For example, at V_{dc}=5 kV, the extracted power at V_w=11.8m/s is 1.589 MW. At V_{dc}=5.6 kV, the extracted power at V_w=11.8m/s is 2.223 MW. It implies that almost 40% higher power can be extracted by increasing the DC bus voltage from 5 kV to 5.6 kV. However, in the following discussion and simulation study, we still keep the DC bus voltage at 5 kV to simplify the analysis.

Based on the analysis for the operation of the wind turbine and generator converter under *type (a)* and *type (b)* device failure conditions, Fig. 3.37 shows the control diagram of the 3L-ANPC generator converter during the fault tolerant operation. Knowing the wind speed, the position and failure type of the failed device, one control mode will be selected from the MPPT control and the constant rotor speed control to generate the reference value I_{q_ref} for the *q*-axis current, which is then sent to the inner current loop of the generator converter controller shown in Fig. 3.34.

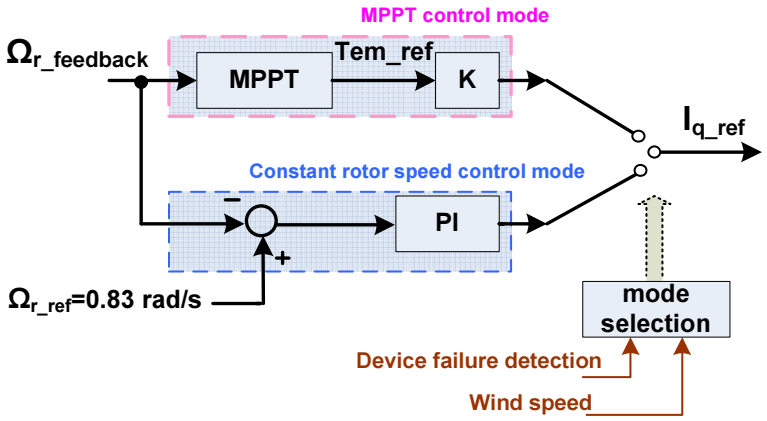


Fig. 3.37 Control diagram of the 3L-ANPC generator converter under fault tolerant operation

The assumption for the previous analysis is that the ratio between the modulation index and the rotor speed is almost constant since the generator stator resistance and inductance are

very small. However, the stator back-EMF voltage is not strictly equal to the stator voltage if the stator resistance and inductance can not be neglected, especially when the extracted wind power is large at high wind speed. Therefore, the previous assumption is not absolutely accurate. For this issue, several cases are studied and simulated in MATLAB to further look into the exact relation of the wind speed, the rotor speed and the modulation index under the MPPT control mode and the constant rotor speed control mode, respectively.

Under the MPPT control mode in normal operation, the relation between the wind speed and the rotor speed is given in (3-65). The data of the wind speed and the corresponding rotor speed, which is acquired from the simulation test, is plotted in Fig. 4.26. It shows that the simulation results match the analytical equation in (3-65), and prove that the ratio between the rotor speed and the wind speed is almost constant in normal operation under MPPT control mode for the wind speed in region II.

$$\omega_r = \frac{V_w \times \lambda_{opt}}{R} = \frac{V_w \times 7.6179 \times 30}{58 \times \pi} = 1.2542 \times V_w \qquad \textbf{(3-65)}$$

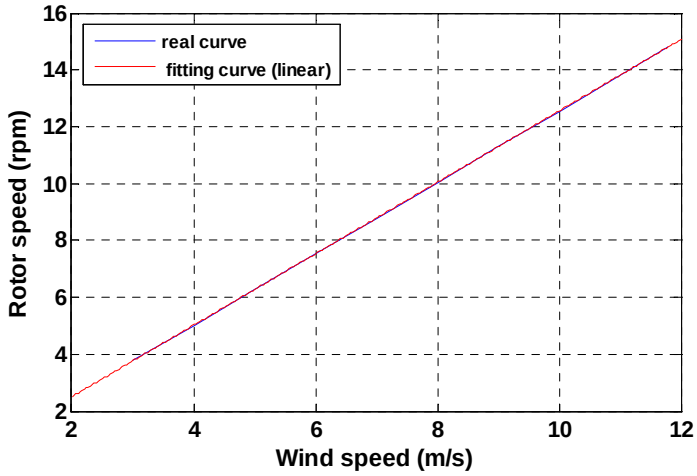


Fig. 3.38 Relation between the rotor speed and the wind speed in normal operation under MPPT control

Under the MPPT control mode in normal operation, the data of the rotor speed and the corresponding modulation index, which is acquired from the simulation test, is plotted in Fig. 3.39.

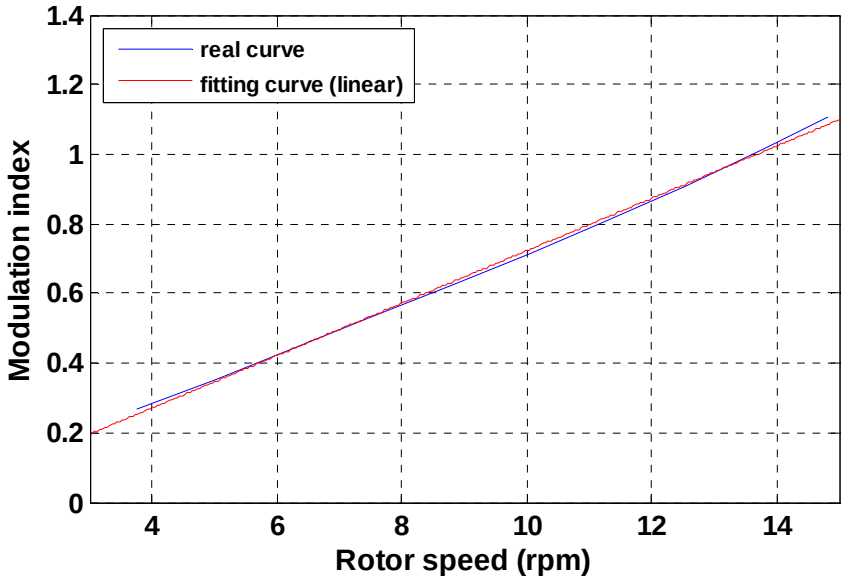


Fig. 3.39 Relation between rotor speed and modulation index in normal operation under MPPT control

From Fig. 3.39, it can be observed that the ratio between the rotor speed and the corresponding modulation index is not exactly constant. Detailed simulation shows that with the MPPT control, when the wind speed V_w equals to 6.32 m/s, the rotor speed is 7.93 rpm, and the modulation index is 0.5597. When the wind speed V_w equals to 6.51 m/s, the rotor speed is 8.17 rpm and the modulation index reaches 0.577, which is the maximum modulation index under *type (b)* fault tolerant control.

In normal operation, if we use the constant speed control instead of the MPPT control in the simulation study, then when the rotor speed is 7.93 rpm, the relation between the wind speed and the modulation index is shown in Table 3-20. Similarly, in another simulation

study, when the rotor speed is controlled at 8.17 rpm, the relation between the wind speed and the modulation index is shown in Table 3-21.

Table 3-20 Wind speed and modulation index at ω_r=7.93 rpm under normal operation

Wind speed (m/s)	6.32	8	9	10	11.8
Modulation index	0.5597	0.5604	0.5611	0.5617	0.5619

Table 3-21 Wind speed and modulation index at ω_r=8.17 rpm under normal operation

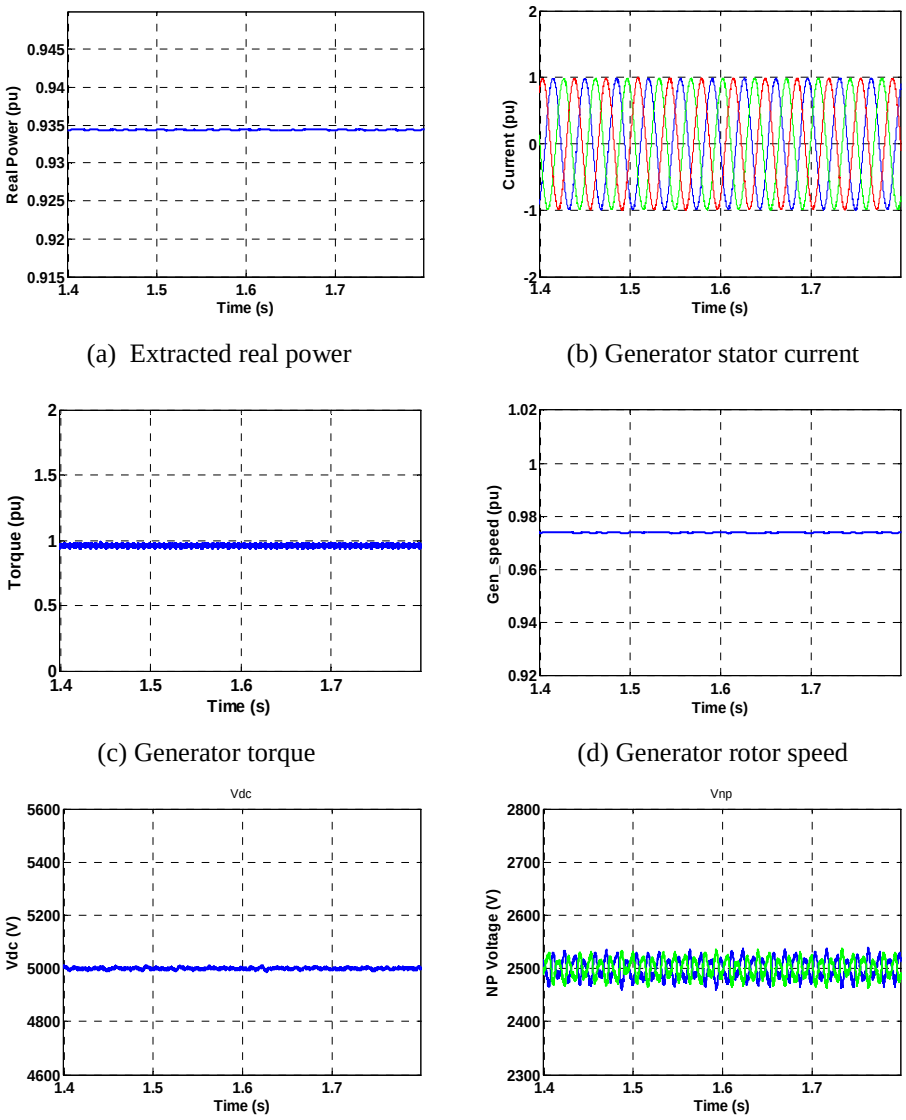
Wind speed (m/s)	6.51	8	9	10	11.8
Modulation index	0.5769	0.5777	0.5787	0.5796	0.5801

From Table 3-20 and Table 3-21, it is observed that under the constant speed control mode, when the wind speed is higher, the modulation index will also increase. The reason is that the torque increases for the higher extracted power. Therefore, if we control the rotor speed at 8.17 rpm under *type (b)* fault tolerant operation, the wind turbine system may be unstable at high wind speed. For example, when the wind speed V_w=11.8 m/s, the required modulation index is 0.5801, which exceeds the maximum modulation index limit 0.577 during the fault operation, thus the controller may oscillate and result in instability. However, if we control the rotor speed at 7.93 rpm as we did in the previous analysis and discussion, then even at the wind speed V_w=11.8 m/s, the required modulation index 0.5619 is still lower than the maximum modulation index limit 0.577, and the generator can operate in a stable mode. Another advantage is that due to the margin of the modulation index (around 3%), it also brings benefits in terms of system dynamic performance. Therefore, finally we choose to control the rotor speed at 7.93 rpm under *type (b)* fault tolerant operation.

3.4.3 Simulation Verification

To verify the proposed control schemes for the 3L-ANPC generator converter under fault tolerant operation, the simulation study of a 5 MW direct-driven PMSG based wind turbine system is implemented in MATLAB. The main parameters of wind turbine system are given in Table 3-19. In the simulation, we assume that the device failure occurs at 1.5s in phase A of the 3L-ANPC generator converter. The waveforms of the extracted real power, the generator stator current, the generator torque, the rotor speed, the dc-link voltage and the neutral-point voltage are plotted for each test case.

Fig. 3.40 shows the generator side waveforms at the wind speed V_w=11.5m/s with D_5 open circuit failure at 1.5s. This device failure belongs to *type (a)* failure, so the fault tolerant control strategy will derive the 3L-ANPC converter into a configuration similar to the 3L-NPC converter. Hence, the maximum modulation index is not reduced. From the waveforms, it can be observed that the operation of the wind turbine and the generator almost has no change after D_5 fails. The MPPT algorithm is still effective.



(a) Extracted real power (b) Generator stator current

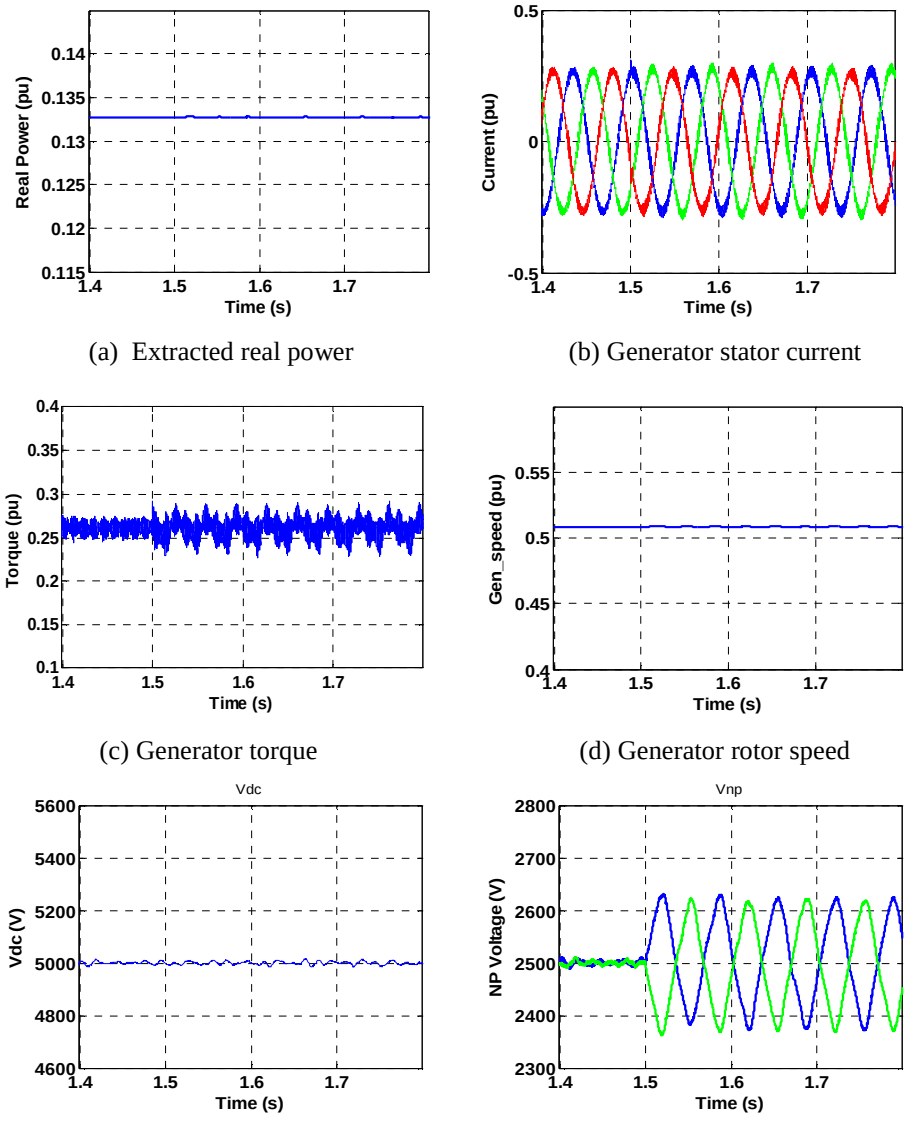
(c) Generator torque (d) Generator rotor speed

(e) DC-link voltage (f) Neutral-point voltage

Fig. 3.40 Generator side waveforms under D_5 open failure at V_w=11.5m/s with fault tolerant control

Fig. 3.41 shows the generator side waveforms at the wind speed V_w=6m/s with D_2 short circuit failure at 1.5s. This failure belongs to *type (b)* failure, so the maximum modulation index is limited to 0.577 under fault tolerant control. However, since the wind speed V_w is below 6.32m/s, the MPPT algorithm can still be achieved. The post-fault waveforms are

almost the same as those in normal operation. Because the fault tolerant control always connects the faulty phase of the 3L-ANPC generator converter to the neutral-point of the dc-link after D_2 fails, the ripple of the neutral-point voltage becomes slightly larger, which will consequently increase the torque ripple slightly. However, the waveforms show this small ripple increase has little impact for the proper operation of the converter and the wind turbine.



(a) Extracted real power

(b) Generator stator current

(c) Generator torque

(d) Generator rotor speed

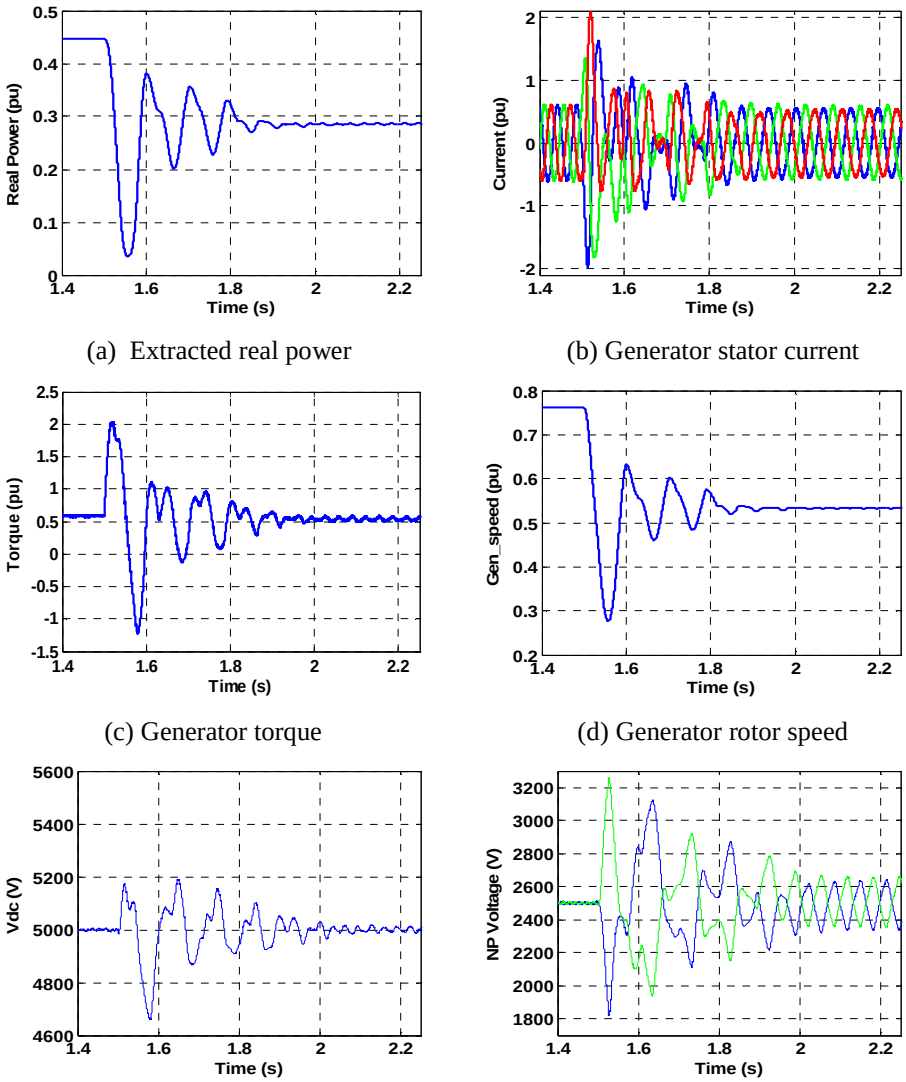
(e) DC-link voltage

(f) Neutral-point voltage

Fig. 3.41 Generator side waveforms under D_2 short failure at V_w=6 m/s with fault tolerant control

Fig. 3.42 shows the generator side waveforms at the wind speed V_w=9m/s with D_2 open circuit failure at 1.5s. This failure belongs to *type (b)* failure, so the maximum modulation index is limited to 0.577 with fault tolerant control. Since the wind speed V_w is above 6.32m/s, and then based on the control diagram in Fig. 3.37, the generator controller will transit from the MPPT mode to the constant rotor speed mode after the device failure. The rotor speed is controlled to be 7.93rpm. The decrease of the extracted real power and the rotor speed can be observed in the waveforms. The transient period takes about 0.4s for the wind turbine and the generator to reach the new steady-state operating point after D_2 failure. The performance of this dynamic transition can be further improved by choosing the appropriate PI parameters for the speed controller and current controller.

The simulation results prove that by using the proposed control schemes, the 3L-ANPC generator converter allows the wind turbine to continue operating and provide real power to the grid under device failure conditions.



(a) Extracted real power (b) Generator stator current

(c) Generator torque (d) Generator rotor speed

(e) DC-link voltage (f) Neutral-point voltage

Fig. 3.42 Generator side waveforms under D_2 open circuit failure at V_w=9 m/s with fault tolerant control

3.5 Summary

Fault tolerant operation of power electronics converters is very important for the critical industrial processes with high associated standstill cost and safety-critical applications. In this chapter, the study focuses on the fault cased by the power device open and short circuit failure.

First, the existing fault diagnosis techniques and fault tolerant strategies of the conventional multilevel converters are reviewed and summarized. Then the fault tolerant ability of the 3L-ANPC converter is analyzed for both device open and short failure conditions. The analysis shows that when device open failure occurs in the 3L-ANPC converter, the output currents become unsymmetrical and the neutral-point voltage of the dc-link becomes unbalanced. Regarding the device short failure, the dc-link capacitor may be discharged through the "DC shoot through" path formed by the failed device, which may cause overcurrent or overvoltage on the other healthy devices and cause damage. The fault tolerant control strategies of the 3L-ANPC converter are proposed to enable the continuous operating of the converter under any single device open and short failure condition. Under S_5/D_5 or S_6/D_6 open failure condition, by choosing the proper switching state and switching sequence, the 3L-ANPC converter can be derived into a configuration which is similar to the 3L-NPC converter. During the fault tolerant operation, the maximum modulation index is still 1.15, and the voltage and current waveform quality is not impacted. If the failure occurs on any other device in the converter, the faulty phase is connected to the neutral-point of the dc-link through a proper "zero" switching state. Meanwhile, the reference voltage signals are modified to maintain the balance of the line-to-line voltages of the converter. During the fault tolerant operation, the maximum modulation index is reduced to 0.577. Moreover, the requirement of the fault detection time is also discussed to ensure the proper fault tolerant operation.

Furthermore, the fault tolerant operation of the 3L-ANPC converter under multiple device open and short failure conditions is studied. It shows that the proposed fault tolerant

control schemes enable the 3L-ANPC converter to operate properly even if multiple devices fail simultaneously. Therefore, the reliability and survival capability of the 3L-ANPC converter are greatly improved. Simulation and experiment results validate the proposed methods.

Compared to the 3L-NPC converter, the 3L-ANPC converter employs 6 additional devices, and this may imply lower converter reliability. However, the comprehensive reliability analysis and comparison for the two converters show that the 3L-ANPC converter has higher reliability than the 3L-NPC converter for motor drive applications, in which the reduction of the maximum modulation index is usually allowed during fault operation, and the motor drive system can continue working, but at a lower speed or lower output power. For grid-connected applications, in which the reduction of the maximum modulation index is not allowed since the converter output is connected to the grid with a fixed voltage, the reliability of the 3L-ANPC converter is similar to that of the 3L-NPC converter for single and multiple device open failure. But for single and multiple device short failure, the 3L-NPC converter has higher reliability than the 3L-ANPC converter.

Finally, the control schemes are proposed for the 3L-ANPC converter for both normal operation and fault operation when it is applied on the generator side of a direct-driven PMSG based large wind turbine system. When the device fails in the generator converter, based on the information of the wind speed, the position and failure type of the failed device, one control mode can be selected from the MPPT control and the constant rotor speed control, so that the wind turbine system can continue operating. If the maximum modulation index is limited to 0.577 during the fault operation, in order to extract more power from wind, it

shows that one option is to increase the DC bus voltage of the converter to a proper level, which can be implemented by the grid-side converter. Therefore, besides the feature of the balanced loss distribution among the devices, the fault tolerant ability of the 3L-ANPC converter also allows the wind turbine to remain in service and continue providing real power to the grid under device failure conditions, which can bring benefits in terms of reliability and economic saving. The simulation results verify the proposed methods and the proper operation of a 5MW wind turbine system.

Chapter 4 Topology, Control and Application of a New Nine-Level ANPC Converter

In this chapter, a new 9-level ANPC converter is proposed for the next generation of high power PEBB technologies to help improve power quality and remove the passive filters in order to reduce the size and weight of the high power converter systems, such as the grid-connection of multi-MW large wind turbine systems.

4.1 Next Generation High Power Medium Voltage PEBBs

Multilevel converters are widely used in high power, medium voltage applications such as adjustable speed drives and the recently emerging electrical interface for grid connection of renewable energy sources. An overview of the available industrial medium voltage converters on the market is depicted in Table 4-1.

Table 4-1 An overview of the industrial medium voltage converters on the market

Manufacture	Product	Voltage (kV)	Power (MVA)	Technology	Semiconductor
ABB	ACS1000	2.3; 3.3; 4.0; 4.16	0.315~5	3L-NPC-VSC	IGCT
	ACS 6000	3; 3.3	3~27	3L-NPC-VSC	IGCT
	ACS 5000	(4.16); 6.0; 6.6; 6.9	2~24	5L-NPC-HB-VSC	IGCT
	ACS 2000	6; 6.6; 6.9	0.4~1	5L-ANPC-VSC	MV IGBT
	PCS 8000	3.3	16	3L-ANPC-VSC	IGCT
Allen Bradley	PowerFlex 7000	2.4; 3.3; 4.16; 6.6	0.15~6.7	PWM-CSI	SGCT
Siemens	Sinamics GM150	2.3; 3.3; 4.16; 6.6	0.8~10	3L-NPC-VSC	MV IGBT
	Sinamics SM150	3.3	5~28	3L-NPC-VSC	IGCT
	Perfect Harmony	2.3~13.8	0.3~30	ML-SCHB-VSC	LV/MV IGBT
Converteam	MV 5000	2.3;3.3;4.2	1.4~7.2	2L-VSC	MV IGBT
	MV 6000	2.3;3.3;4.2	0.3~8	4L-FLC-VSC	MV IGBT
	MV 7000	3.3	7~9.5 / 6~8	3L-NPC-VSC	GTO / MV IGBT

It can be found that the NPC voltage source converter is the most popular topology in medium voltage applications. The number of levels for most multilevel converter products is below five-level, while three-level converters have more penetration in the market [98] [99].

For the next generation of multilevel PEBB technologies in high power applications, the converters with higher number of levels (5-level, 9-level) are needed [100] [101]. One of the main motivations is to improve the power quality and thus reduce the size and weight of the high power converter system by removing the bulky passive filters. Two examples are given as below.

First, in the next generation transformerless Integrated Power System (IPS) for all-electric ships, as shown in Fig. 4.1, the gearless auxiliary power generator concept needs a filterless, multilevel converter solution for the power conversion units to further reduce the weight and size of the auxiliary power generator system. For the power conversion from a high speed PM generator to the auxiliary DC link, a multilevel converter (5-level, 9-level) is needed to limit the total harmonic current distortion below 5% on the generator side without using the bulky passive filters. On the other hand, for the power conversion from the auxiliary DC link to supply the 60 Hz AC shipboard, a multilevel converter (5-level, 9-level) is also needed to limit the total harmonic current distortion on the grid side without using passive filters. The total harmonic distortion of the grid voltage feeding a purely resistive load needs to be below 5%. By avoiding passive filters with heavy chokes, the power density of the shipboard AC power conversion can be increased.

Second, in MW-level wind energy conversion systems, the grid filters are usually appropriately selected to smooth the output voltage and current waveforms of the grid side

converter to remain in compliance with the harmonic limit standards set by the utilities. In recent years, the power capacity of wind turbines has been increasing continuously. Currently, the Repower 5 MW wind turbines and the Enercon E-126 6 MW wind turbines have been installed in Germany. The even higher power level units (10 MW and 12 MW) are either under development or at the prototype stage [102]. At these power ratings, the passive filters are massive and may have potential resonant risk. Therefore, the filterless grid connection concept, which is realized by employing power converters with higher number of levels, is proposed to omit the passive grid filter for the benefits in terms of reduced cost, size and weight, increased power density and higher reliability.

In this work, we focus on the multilevel converter applications in wind power systems.

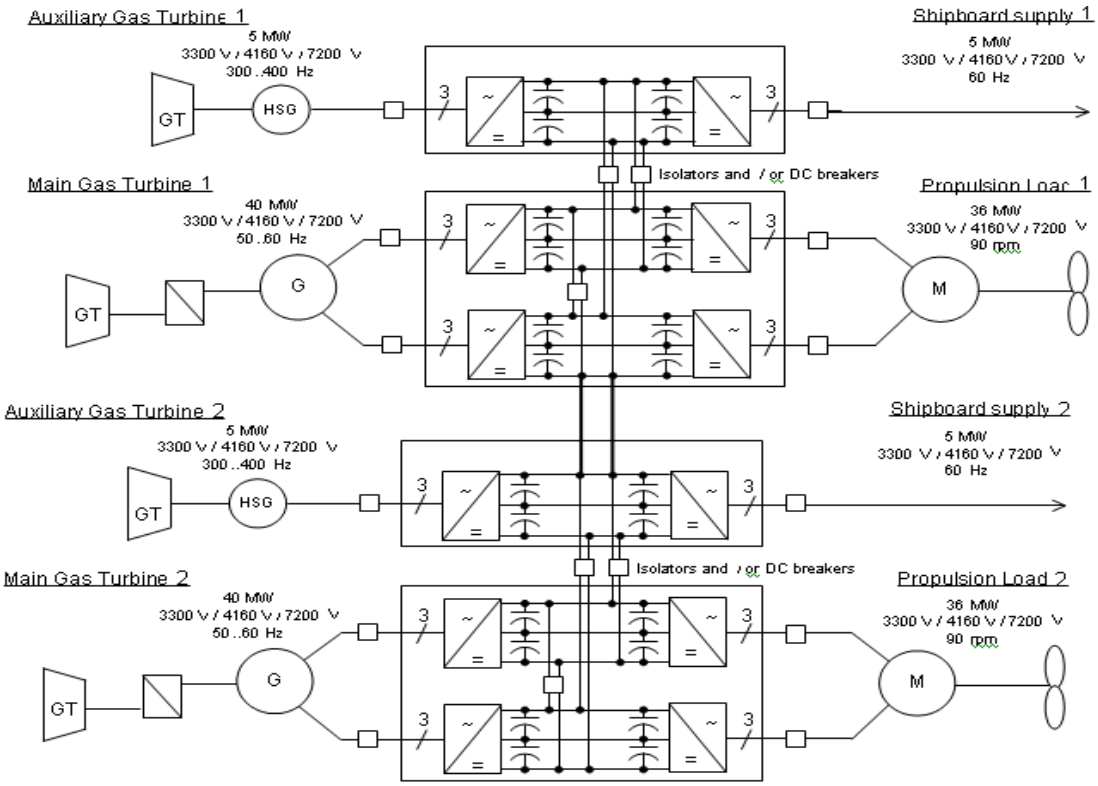


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Fig. 4.1 Next generation transformerless Integrated Power System (IPS) for all-electric ships

4.2 Filterless Grid Connection for Large Wind Turbine Systems

4.2.1 Concept of Filterless Grid Connection

The configuration of a conventional wind turbine system with full-scale converter and direct-driven PM synchronous generator is shown in Fig. 4.2. As seen, a three-level back-to-back NPC converter is usually used in the system and the output of the converter is connected through a grid passive filter to a feeder transformer, which adjusts to higher utility voltages by employing a proper turns-ratio. The grid filter is usually an LC filter in combination with a special damping circuit. The tuned passive filter allows the system operation to meet the harmonic limit required by the IEEE 519 standard [103].

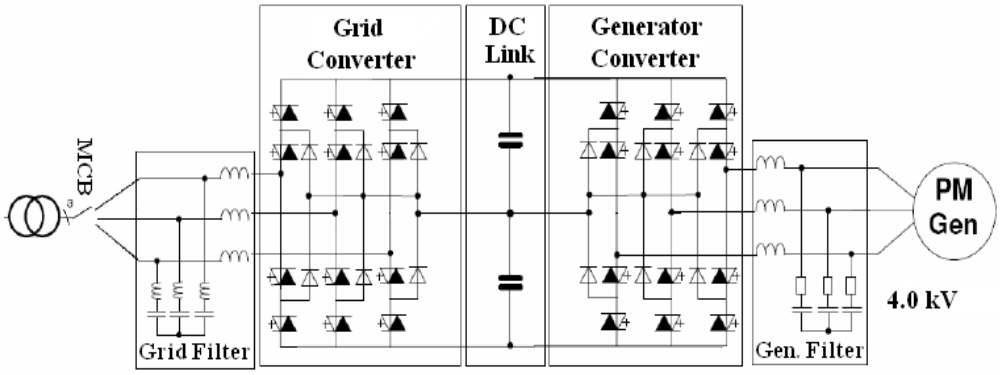


Fig. 4.2 Conventional wind turbine system with full-scale converter and direct-driven PMSG

A five-level active NPC converter has been proposed on the grid side to remove the massive grid filter [104]. The circuit of a 5L-ANPC converter has been shown in Fig. 1.17. It enables the wind turbine system to meet the harmonic limits of IEEE 519 standard without using passive filters. However, in order to fulfill the requirements of the more stringent VDEW standard, an LC grid filter is still needed. The diagram of this wind turbine system is shown in Fig. 4.3.

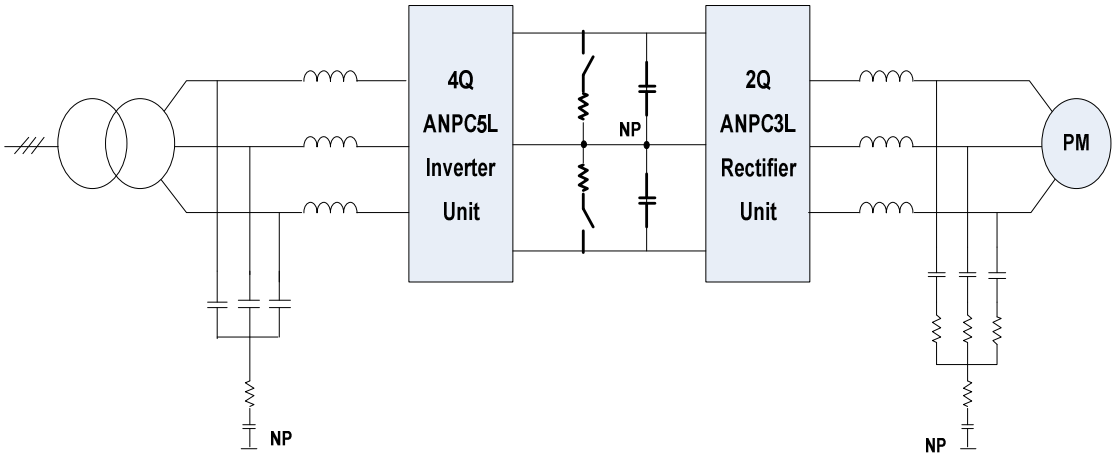


Fig. 4.3 Diagram of the wind turbine system with a 5L-ANPC converter on the grid side

To completely remove the grid filter, further efforts are needed to upgrade the five-level ANPC converter to a topology with a higher number of levels so as to generate sufficient output waveform quality to comply with VDEW standard. It has been proven that the use of a 9-level converter on the grid side shows a global compliancy on almost the whole harmonic range with VDEW standard [105]. It is obvious that, along with a higher number of voltage levels, the multilevel converters can generate better output waveform quality. However, this upgrade requires additional components, such as semiconductor devices and capacitors, which increase the complexity, cost and reliability of the converter and the system. Therefore, in this work, we mainly focus on the 9-level converter topologies.

4.2.2 Review of the 9-Level ANPC Converters

In this section, the existing 9-level ANPC converters are summarized. The characteristics of the different topologies are discussed.

4.2.2.1 9-level ANPC standard converter

Fig. 4.4 shows the circuit of a 9-level ANPC standard converter. It is derived from the generalized ANPC topology and is able to generate a 9-level output voltage waveform by cascading two additional stages of a two-level converter cell (half-bridge topology) to each phase of a similar standard 5L-ANPC converter [32]. In each phase of the converter, there exists three floating capacitors, and the relation of their voltages and half dc-link voltage is 1:2:3:4. A special control scheme is required to keep the voltage balance of the floating capacitors. The blocking voltages of the power device in the converter are: V_{dc} for S_9-S_{12} and $V_{dc}/4$ for S_1-S_8.

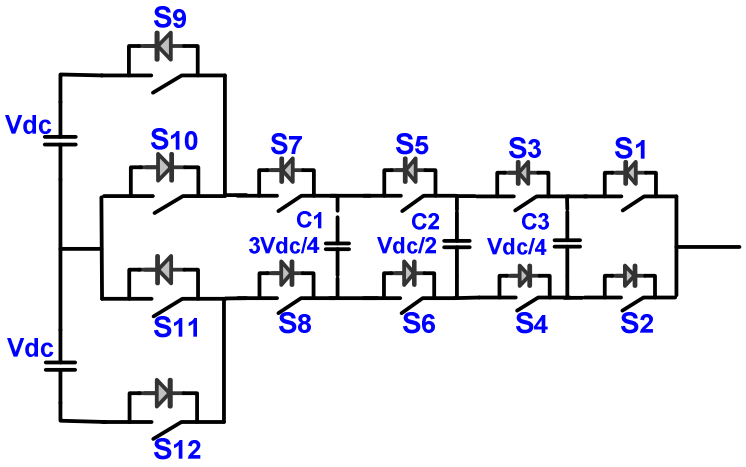


Fig. 4.4 Circuit of the 9-level ANPC standard converter

4.2.2.2 9-level Common Cross Connected Stage (C^3S) converter

Fig. 4.5 shows the circuit of the 9-level C^3S converter [106]. It connects a C^3S PEBB to a similar standard 5L-ANPC converter for a 9-level output voltage waveform. The C^3S PEBB consists of six power devices and one floating capacitor, and it is shared by all three phases. Besides the capacitor in the PEBB, each phase of the converter has only one floating

capacitor. The voltages of C_1 and C_2 are ½ and ¼ of half dc-link voltage, respectively. Since the C^3S PEBB is influenced by all three phases simultaneously, the device blocking voltages are complicated and are follows: $5V_{dc}/4$ for S_5-S_8, $3V_{dc}/4$ for S_3-S_4, $V_{dc}/2$ for S_1-S_2 and $V_{dc}/4$ for S_9-S_{14}. To stabilize the floating capacitor voltages, the maximum modulation index is limited to 0.925 at full active power, which means the dc-link voltage is not fully utilized. The complete three-phase converter diagram is shown in Fig. 4.6 [105].

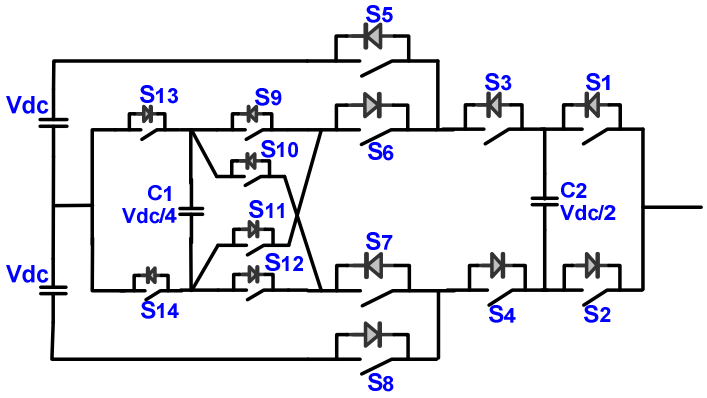


Fig. 4.5 Circuit of the Common Cross Connected Stage (C^3S) converter

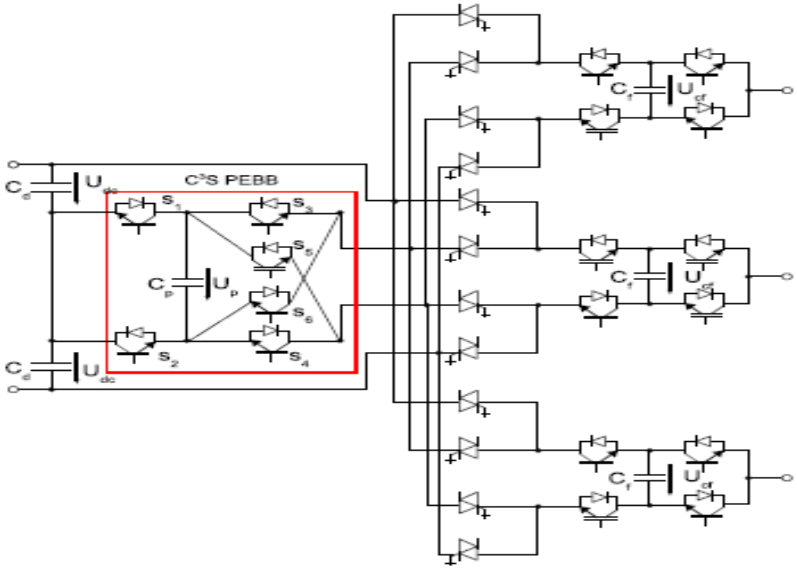


Fig. 4.6 Circuit diagram of the three-phase 9-level C^3S converter

4.2.2.3 9-level Cross Connected Intermediate Level (CCIL) converter

Fig. 4.7 shows the 9-level CCIL converter circuit [107]. Different from the previous 9-level C^3S converter, this topology can be viewed as inserting a CCIL PEBB into each phase of a similar standard 5L-ANPC converter. The CCIL PEBB consists of 6 power devices and one floating capacitor. There are 2 floating capacitors in each phase of the converter, and their voltages are ½ and ¼ of half dc-link voltage, respectively. The device blocking voltages are V_{dc} for S_{11}-S_{14}, $V_{dc}/2$ for S_7-S_{10} and $V_{dc}/4$ for S_1-S_6.

This topology is a double capacitors 9-level redundant non-boosting structure. In [107], another topology, referred to as "single capacitor 9L non-redundant boosting converter", which can save two power devices and one capacitor for each phase, is also introduced, as shown in Fig. 4.8. However, in order to balance its floating capacitor voltage, the control scheme is very complicated (using fuzzy logic control), and the maximum modulation index is limited to 0.91 under full active power. Therefore, in this work, we only focus on the first topology (double capacitor redundant non-boosting CCIL converter).

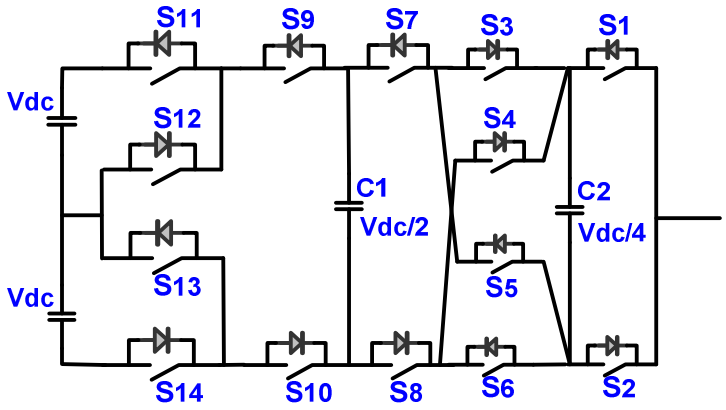


Fig. 4.7 Circuit of the 9-level Cross Connected Intermediate Level (CCIL) converter

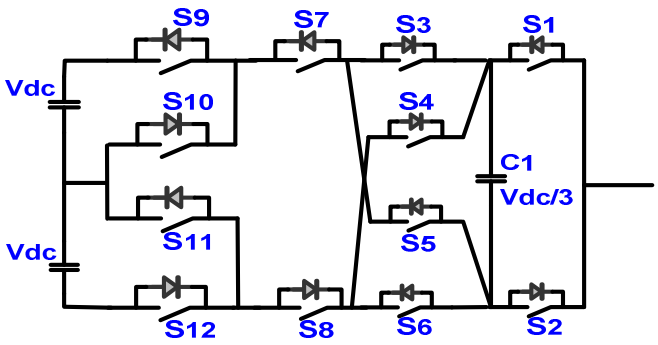


Fig. 4.8 Circuit of single capacitor 9-level Cross Connected Intermediate Level (CCIL) converter

4.2.2.4 9-level 3L-ANPC plus HBBBs converter

The circuit of the 9L 3L-ANPC plus HBBBs (H-bridge building blocks) converter is shown Fig. 4.9. It generates a 9-level output voltage waveform by cascading two HBBBs to each phase of a standard 3L-ANPC converter. Each phase has two floating capacitors and their voltages are ½ and ¼ of half dc-link voltage, respectively. The device blocking voltages are V_{dc} for S_9-S_{14}, $V_{dc}/2$ for S_5-S_8 and $V_{dc}/4$ for S_1-S_4.

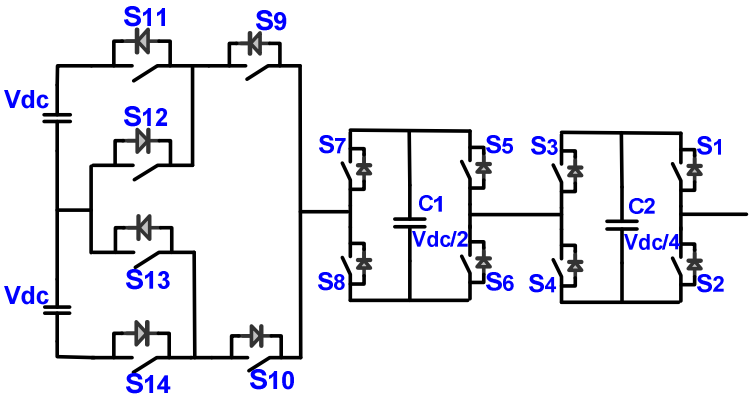


Fig. 4.9 Circuit of 9-level 3L-ANPC plus HBBBs converter

In [27], a similar topology is studied for medium voltage motor drive applications, which connects only one HBBB to each phase of a conventional three-level NPC converter to achieve 9-level output. The circuit of a 9-level 3L-ANPC plus single HBBB converter is

shown in Fig. 4.10. Model-predictive control (MPC) is used to stabilize the floating capacitor voltages because there are no redundant switching states in the converter, therefore the controller design is very complicated compared to those using redundant switching states. Another drawback of the converter is that the maximum modulation index is limited to 0.95 under full active power. Therefore, in this work, we mainly focus on the 3L-ANPC plus two HBBBs converter.

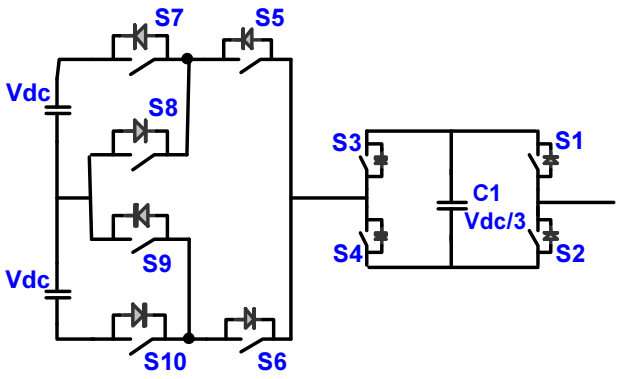


Fig. 4.10 Circuit of 9-level 3L-ANPC plus single HBBB converter

4.3 A New 9-Level ANPC Converter

This work aims to upgrade a 5L-ANPC converter to a 9-level converter and achieve a filterless grid connection for large wind turbine systems. A new topology, named 5L-ANPC plus HBBB converter, is proposed and discussed in detail in the following sections.

4.3.1 Topology of the New 9-Level ANPC Converter

The circuit diagram of the proposed new 9-level ANPC converter is shown in Fig. 4.11. Different from the other 9-level ANPC converters above, in the proposed topology, one HBBB is directly connected to each phase of a standard 5L-ANPC converter. Therefore, this topology is named 5L-ANPC plus HBBB converter. Each phase has two floating capacitors,

and their voltages are ½ and ¼ of half dc-link voltage, respectively. The device blocking voltages are V_{dc} for S_5-S_8, $V_{dc}/2$ for S_1-S_4 and $V_{dc}/4$ for S_{11}-S_{22}.

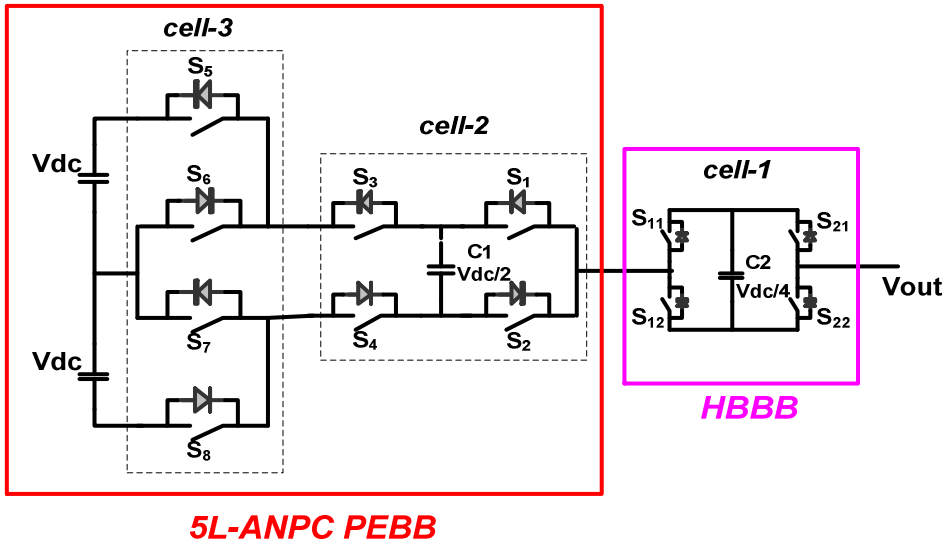


Fig. 4.11 The proposed 9-level topology—5L-ANPC plus HBBB converter

Regarding the floating capacitors, their capacitance needs to limit the voltage ripple seen by the capacitors for a given switching frequency, which can be calculated by (4-1).

$$C = \frac{I_{pk}}{\Delta V_C}\frac{1}{f_c} \tag{4-1}$$

Where I_{pk} is the peak phase current, ΔV_C is the peak-to-peak voltage ripple across the floating capacitors, and f_c is the switching frequency.

If we assume the two floating capacitors in each phase have the same peak-to-peak per unit voltage ripple based on their rated voltage, and the phase peak current and the equivalent switching frequency are the same for the two capacitors, then we have a relation for the capacitance of the two capacitors shown as (4-2).

$$C_2 = 2 \cdot C_1 \tag{4-2}$$

For one phase-leg of the new 9-level ANPC converter, the energy stored in the floating capacitor C_1 and C_2 is expressed by (4-3) and (4-4), respectively.

$$E_{C1} = \frac{1}{2} \cdot C_1 \cdot \left(\frac{V_{dc}}{2} \right)^2 = \frac{1}{8} \cdot C_1 \cdot {V_{dc}}^2 \quad \textbf{(4-3)}$$

$$E_{C2} = \frac{1}{2} \cdot C_2 \cdot \left(\frac{V_{dc}}{4} \right)^2 = \frac{1}{32} \cdot C_2 \cdot {V_{dc}}^2 \quad \textbf{(4-4)}$$

Therefore, the total stored energy in each phase of the converter is given by (4-5).

$$E_{total} = E_{C1} + E_{C2} = \frac{1}{32} \left(4 \cdot C_1 + C_2 \right) \cdot {V_{dc}}^2 \quad \textbf{(4-5)}$$

The proposed topology is considered to be an effective and practical solution to expand an existing 5L-ANPC converter in the wind turbine system to a 9-level converter because it has the following features.

- Both 5L-ANPC and HBBB are standard power electronics building blocks (PEBBs), so the potential technical risk associated with the converter innovations is reduced.
- Few mechanical structure modifications are needed for upgrading the 5L-ANPC converter to the new 9-level ANPC converter, since it only requires connecting the AC output terminals of the two PEBBs together with cables. Because these terminals are usually reserved on the PEBB products, the converter system installation is more straightforward and the implementation is much easier.
- It is easy to maintain the voltage balance of the floating capacitors by using redundant switching states. Such methods allow the voltage balance control in one phase totally independent from the other two phases. Moreover, the maximum modulation index is not impacted, and can reach up to 1.15 under full active power transfer.

- The dc-link structure of the new 9-level converter is the same as that in the 3L-NPC and 3L-ANPC converters. This is beneficial for a direct-drive PMSG based large wind turbine system with a full-scale converter, because the generator converter is usually a 3L-NPC or 3L-ANPC converter and it needs minor modification when the grid converter is upgraded from a 5L-ANPC converter to the new 9-level converter.
- The dc-link voltage and neutral-point balance can be regulated by the generator side converter. So the control of the proposed 9-level grid side converter can be simplified.

4.3.2 Operation and Control of the New 9-Level ANPC Converter

In the proposed topology, the 5L-ANPC PEBB and HBBB can generate 5-level and 3-level output voltage waveforms, respectively. Through the proper switching state combinations of the two building blocks, a 9-level output voltage waveform is obtainable.

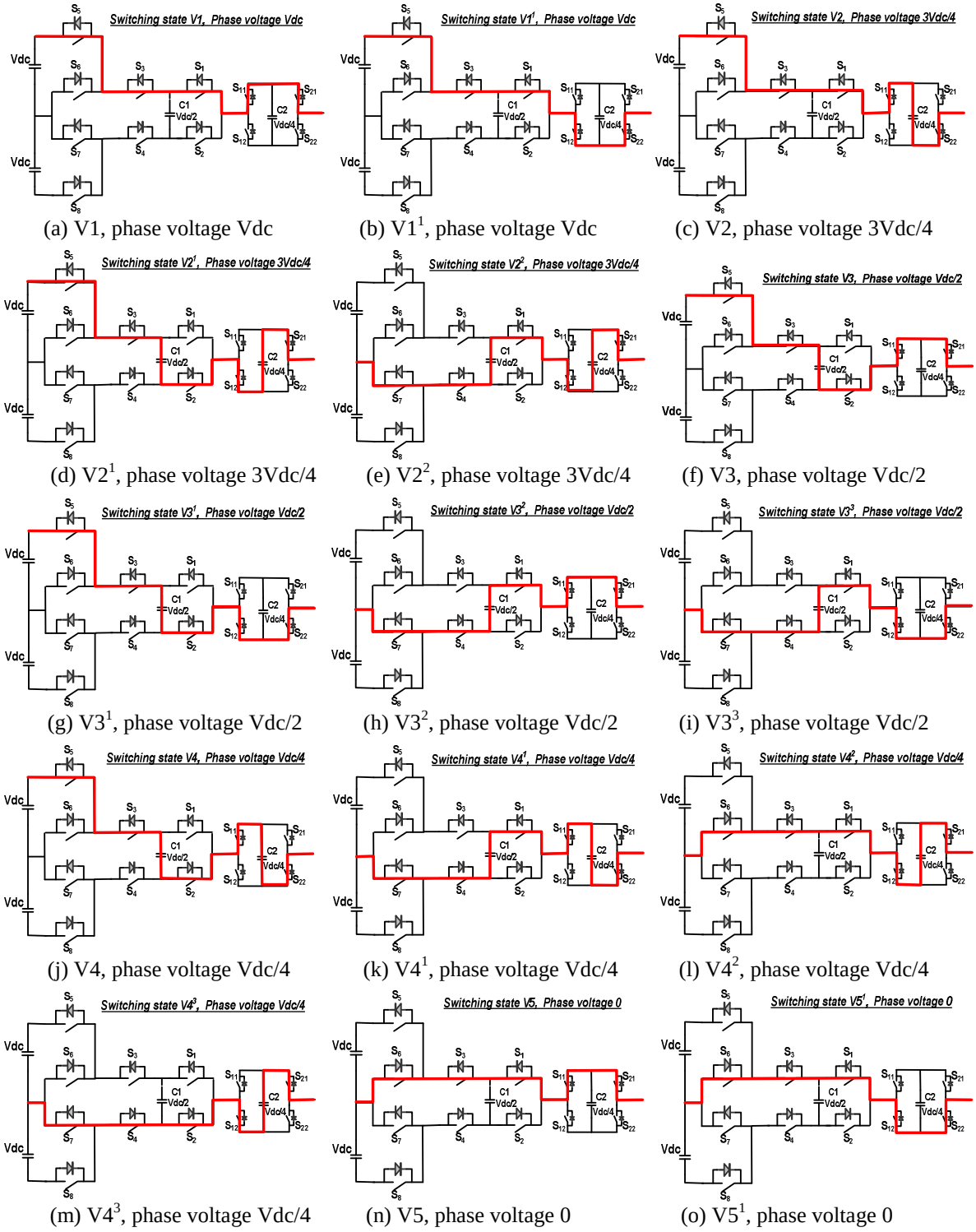
Fig. 4.12 shows the possible switching states, and the associated output voltage and current flow path of the proposed 9-level ANPC converter when the output phase voltage is positive. This occurs during the positive half cycle of the fundamental period. Due to the symmetrical structure of the converter, the operation during the other half cycle of the fundamental period when the output phase voltage is negative, can be analyzed and derived in a similar way. The complete switching states, switching sequence, and the effect on the floating capacitor voltages of the new 9-level ANPC converter are summarized in Table 4-2. In the table, “1” and “0” represent the on-state and off-state for the device, respectively. For each switching state, the impact on the floating capacitor voltage may be different. “+”, “-” and “o” represent charging, discharging and no effect on the floating capacitor, respectively.

The positive direction of the phase current is defined as flowing out of the AC terminal. It can be found that the output voltage is synthesized by adding or subtracting the dc-link capacitor voltages and the floating capacitor voltages, while several switching states are available to generate the same output phase voltage. For example, there are three options to generate the output voltage $3V_{dc}/4$, as shown in Fig. 4.12 (c) (d) and (e). The expressions for the output voltage synthesization are provided in (4-6), (4-7) and (4-8). These redundant switching states can be used to balance the floating capacitor voltage, which is explained later.

$$V_{out} = V_{dc} - V_{C2} = V_{dc} - V_{dc} / 4 = 3V_{dc} / 4 \quad \textbf{(4-6)}$$

$$V_{out} = V_{dc} - V_{C1} + V_{C2} = V_{dc} - V_{dc} / 2 + V_{dc} / 4 = 3V_{dc} / 4 \quad \textbf{(4-7)}$$

$$V_{out} = 0 + V_{C1} + V_{C2} = V_{dc} / 2 + V_{dc} / 4 = 3V_{dc} / 4 \quad \textbf{(4-8)}$$



(a) V1, phase voltage Vdc (b) V1[1], phase voltage Vdc (c) V2, phase voltage 3Vdc/4

(d) V2[1], phase voltage 3Vdc/4 (e) V2[2], phase voltage 3Vdc/4 (f) V3, phase voltage Vdc/2

(g) V3[1], phase voltage Vdc/2 (h) V3[2], phase voltage Vdc/2 (i) V3[3], phase voltage Vdc/2

(j) V4, phase voltage Vdc/4 (k) V4[1], phase voltage Vdc/4 (l) V4[2], phase voltage Vdc/4

(m) V4[3], phase voltage Vdc/4 (n) V5, phase voltage 0 (o) V5[1], phase voltage 0

Fig. 4.12 Switching states, output voltage, and current conduction path of the new 9-level ANPC converter during half of the fundamental period in which the output phase voltage is positive

Table 4-2 Switching states and their impact on floating capacitor voltage in the new 9L ANPC converter

Cell-3				*Cell-2*				*Cell-1*				Phase voltage	Effect on C_1		Effect on C_2		Switching state
S_8	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_{11}	S_{12}	S_{21}	S_{22}		I>0	I<0	I>0	I<0	
0	1	0	1	0	1	0	1	1	0	1	0	Vdc	o	o	o	o	V1
0	1	0	1	0	1	0	1	0	1	0	1	Vdc	o	o	o	o	$V1^1$
0	1	0	1	0	1	0	1	1	0	0	1	3Vdc/4	o	o	+	-	V2
0	1	0	1	0	1	1	0	0	1	1	0	3Vdc/4	+	-	-	+	$V2^1$
0	1	0	1	1	0	0	1	0	1	1	0	3Vdc/4	-	+	-	+	$V2^2$
0	1	0	1	0	1	1	0	1	0	1	0	Vdc/2	+	-	o	o	V3
0	1	0	1	0	1	1	0	0	1	0	1	Vdc/2	+	-	o	o	$V3^1$
0	1	0	1	1	0	0	1	1	0	1	0	Vdc/2	-	+	o	o	$V3^2$
0	1	0	1	1	0	0	1	0	1	0	1	Vdc/2	-	+	o	o	$V3^3$
0	1	0	1	0	1	1	0	1	0	0	1	Vdc/4	+	-	+	-	V4
0	1	0	1	1	0	0	1	1	0	0	1	Vdc/4	-	+	+	-	$V4^1$
1	0	1	0	0	1	0	1	0	1	1	0	Vdc/4	o	o	-	+	$V4^2$
0	1	0	1	1	0	1	0	0	1	1	0	Vdc/4	o	o	-	+	$V4^3$
0	1	0	1	1	0	1	0	1	0	1	0	0	o	o	o	o	V5
0	1	0	1	1	0	1	0	0	1	0	1	0	o	o	o	o	$V5^1$
1	0	1	0	0	1	0	1	1	0	1	0	0	o	o	o	o	$V5^2$
1	0	1	0	0	1	0	1	0	1	0	1	0	o	o	o	o	$V5^3$
0	1	0	1	1	0	1	0	1	0	0	1	-Vdc/4	o	o	+	-	V6
1	0	1	0	0	1	0	1	1	0	0	1	-Vdc/4	o	o	+	-	$V6^1$
1	0	1	0	0	1	1	0	0	1	1	0	-Vdc/4	+	-	-	+	$V6^2$
1	0	1	0	1	0	0	1	0	1	1	0	-Vdc/4	-	+	-	+	$V6^3$
1	0	1	0	0	1	1	0	1	0	1	0	-Vdc/2	+	-	o	o	V7
1	0	1	0	0	1	1	0	0	1	0	1	-Vdc/2	+	-	o	o	$V7^1$
1	0	1	0	1	0	0	1	1	0	1	0	-Vdc/2	-	+	o	o	$V7^2$
1	0	1	0	1	0	0	1	0	1	0	1	-Vdc/2	-	+	o	o	$V7^3$
1	0	1	0	1	0	1	0	0	1	1	0	-3Vdc/4	o	o	-	+	V8
1	0	1	0	0	1	1	0	1	0	0	1	-3Vdc/4	+	-	+	-	$V8^1$
1	0	1	0	1	0	0	1	1	0	0	1	-3Vdc/4	-	+	+	-	$V8^2$
1	0	1	0	1	0	1	0	1	0	1	0	-Vdc	o	o	o	o	V9
1	0	1	0	1	0	1	0	0	1	0	1	-Vdc	o	o	o	o	$V9^1$

The pulse-width modulation (PWM) for the new 9-level ANPC converter is shown in Fig. 4.13. Carrier-based PWM with 3rd harmonic injection is used in this PWM method to extend the maximum modulation index to 1.15 under linear modulation. As seen, the eight triangular carriers have the same frequency and amplitude, and their occupied voltage bands are continuous. By comparing the reference signal with each of the triangular carriers, the corresponding devices are switched to generate the 9-level voltage waveform in each phase.

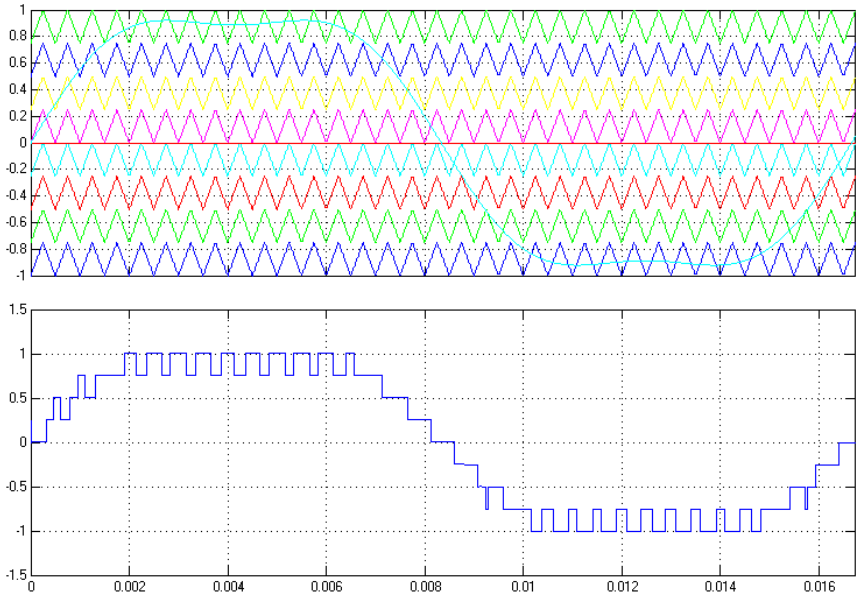


Fig. 4.13 PWM signals and the output voltage of the proposed 9-level ANPC converter

To ensure the proper operation of the proposed converter, the voltage of the two floating capacitors in each phase must be kept balanced around their reference voltage level. Typically, there are two types of solutions for the floating capacitor voltage control in multilevel converters. One method is based on the common mode voltage control. This solution does not need the redundant switching states to balance the capacitor voltage, therefore the converter requires less power devices and capacitors to generate the same

number of voltage levels. However, the implementation of this method is very complicated since advanced control algorithms are needed, such as model predictive control and fuzzy logic control. Another drawback is the limitation of the maximum modulation index under full active power transfer operation of the converter. The other solution, which is widely used in industrial applications, is to use redundant switching states to balance the floating capacitor voltage. This method is easy to implement in the controller and has little impact on the limitation of the maximum modulation index under full active power transfer. In this work, the latter solution, which is based on redundant switching states, is adopted for the proposed 9-level ANPC converter.

From Table 4-2 and Fig. 4.13, it is observed that the two floating capacitors in each phase will be charged or discharged at certain output voltage levels depending on the selected switching state and the direction of the output phase current. Moreover, when a switching state is selected to balance the floating capacitor voltage in one phase, it may only impact one of two capacitor voltages (e.g. V2), or may impact both of them (e.g. $V2^1$ and $V2^2$). For the latter case, the controller needs to prioritize the capacitors first in order to choose the proper switching state. The capacitor with a more deviated voltage should be given a higher priority, so that even though the selected switching state for the current switching cycle is not optimal for the voltage balance of the inferior capacitor, the overall corrective action is still applied to the converter to assure its proper operation.

For example, when the output phase voltage is $3V_{dc}/4$, the control scheme to balance the floating capacitor voltage is explained below.

- If the voltage deviation of C_1 is larger than C_2, then C_1 has higher priority:
    - When C_1 needs charged and if I>0, then $V2^1$ is selected. Otherwise, if I<0, then $V2^2$ should be selected.
    - When C_1 needs discharged and if I>0, then $V2^2$ is selected. Otherwise, if I<0, $V2^1$ should be selected.

For both cases, while the selected switching state is working on balancing the voltage of C_1, the correct voltage balance action may not occur on the capacitor C_2, because the impact on C_2 is to discharge when I>0 and charge when I<0 without considering the actual voltage state of C_2. The voltage deviation on C_2 may become larger in the current switching cycle, but it will obtain the higher priority in the next switching cycle if its voltage deviation exceeds that of C_1, then the proper control for capacitor C_2 will be chosen.

- If the voltage deviation of C_2 is larger than C_1, then C_2 has higher priority:
    - When C_2 needs charged, then V2 is selected in the case when I>0. The voltage status of C_1 will not be affected during this period.
    - When C_2 needs charged and I<0, if C_1 needs charged, then $V2^2$ is selected; or if C_1 needs discharged, $V2^1$ will be used. In this case, the voltages of C_1 and C_2 will be regulated simultaneously.
    - When C_2 needs discharged, then V2 is selected in the case when I<0. The voltage status of C_1 will not be affected during this period.
    - When C_2 needs discharged and I>0, if C_1 needs charged, then $V2^1$ is selected; or if C_1 needs discharged, $V2^2$ is chosen. In this case, the voltages of C_1 and C_2 can be regulated simultaneously.

Similarly, the switching state selection for the other output phase voltages can be derived.

Some switching states generate the same voltage level, and have the same impact on the floating capacitor voltage (e.g. V5 and $V5^3$). Then these switching states can be optimally selected to balance the device power losses in the converter.

4.3.3 Semiconductor Device Selection

The trade-offs of selecting semiconductor devices for specific applications are within the device switching frequency and voltage rating. Equipped with different power devices, the converter is able to exploit their individual advantages [23]. The proposed 9-level ANPC converter is targeted for a 5~6 MW wind turbine system. The dc-link voltage is 6.4 kVdc. The fundamental frequency of the reference signal is 60 Hz and the PWM carrier frequency is 2 kHz. ETO thyristors [108] and IGBTs are used in this converter. 5.5kV/6.5kV ETO thyristors are used for S_5~S_8, 3.3kV IGBTs for S_1~S_4, and 1.7kV IGBTs for S_{11}~S_{22}. To utilize the ETOs' strength of the high voltage and current rating and low conduction loss, *Cell-3* (S_5~S_8) is switched at the fundamental frequency. The IGBTs (*Cell-1, 2*) are switched at (or slightly below) the carrier frequency. In order to achieve this, minor modifications are made in Table 4-2. First, the switching states $V4^2$ and V6 will not be used. Second, to generate "0" output phase voltage, the switching states V5 and $V5^1$ are used when the voltage reference is positive, while $V5^2$ and $V5^3$ are selected when the voltage reference is negative.

4.3.4 Simulation and Experiment Verification

To verify the proposed 9-level ANPC converter topology and control scheme, simulation and experiment are employed. The test circuit diagram of the new 9-level ANPC PEBB is

shown in Fig. 4.14. Since we use the redundant switching states to control the floating capacitor voltage, the voltage balance control in each phase is independent from the other two phases of the converter. Therefore one phase of the new 9-level ANPC PEBB is sufficient to prove the correctness of the proposed topology, control and the floating capacitor voltage balance scheme. In this work, the neutral-point balance issue of the dc-link is not addressed in the controller design because it can be controlled more easily by the front-end converter in the back-to-back converter configuration. Therefore, two constant DC voltage sources are connected to the dc-link of the 9-level ANPC converter.

For both simulation and experiment, the main parameters are: half DC bus voltage V_{dc}=60 V, fundamental frequency f=60 Hz, carrier frequency f_c=2 kHz, floating capacitors C_1=2.7 mF, C_2=5.4 mF. The load is a 12 Ω resistor in series with a 2.5 mH inductor.

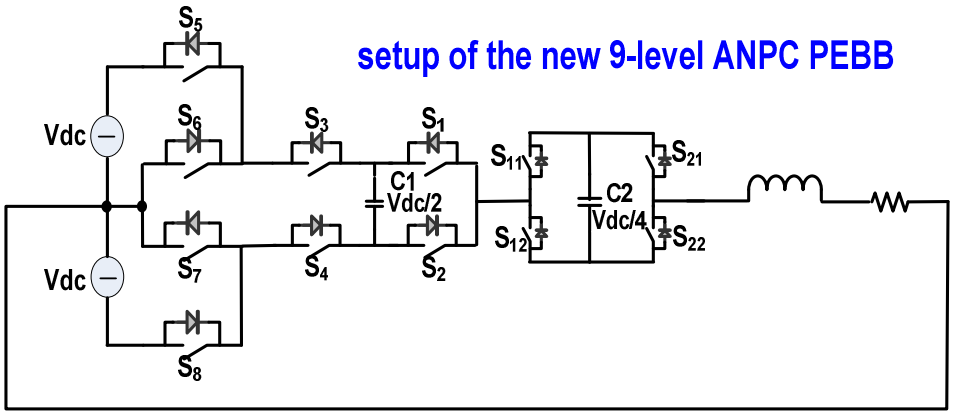


Fig. 4.14 Circuit diagram of the new 9-level ANPC PEBB for simulation and experiment study

4.3.4.1 Simulation results

In the simulation, the modulation index is set to be 0.96. Fig. 4.15 shows the phase voltage, the gate drive signals for *Cells 1~3* (S_5, S_1 and S_{21}) and the floating capacitor voltages, from top to bottom.

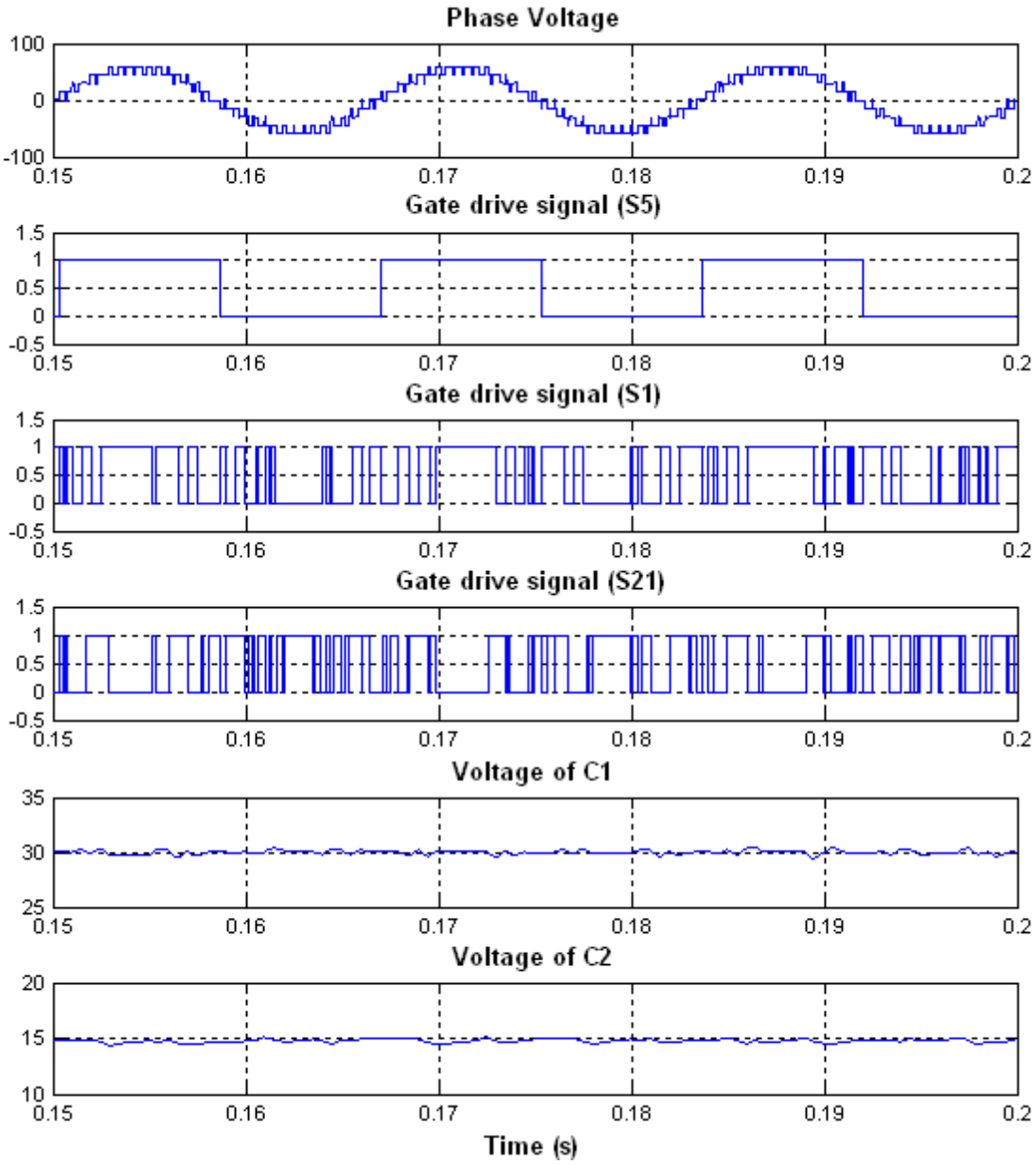


Fig. 4.15 Simulation waveform of the new 9-level ANPC PEBB

The simulation results show that with the proposed control scheme, the new 9-level ANPC converter can generate a 9L voltage waveform, and the two floating capacitor voltages can be controlled around their reference value. The gate drive signals imply that the devices in *Cell-3* switch at fundamental frequency, and the devices in *Cell-2* switch at the

frequency which is slightly lower than the carrier frequency. The devices in *Cell-1* switch at the carrier frequency. This indicates the possibility to use a hybrid converter concept by employing different types of power devices.

4.3.4.2 Experiment results

The laboratory prototype of the new 9-level ANPC PEBB is shown in Fig. 4.16. For the power stage, the discrete IGBT modules (Powerex CM75DY-24H) are used for the 5L-ANPC PEBB and the IPM (Mitsubishi PM50RSA120) is used for the HBBB. The controller is TI TMS320F2812 DSP. The power stage and the digital controller platform are connected through optical fibers.

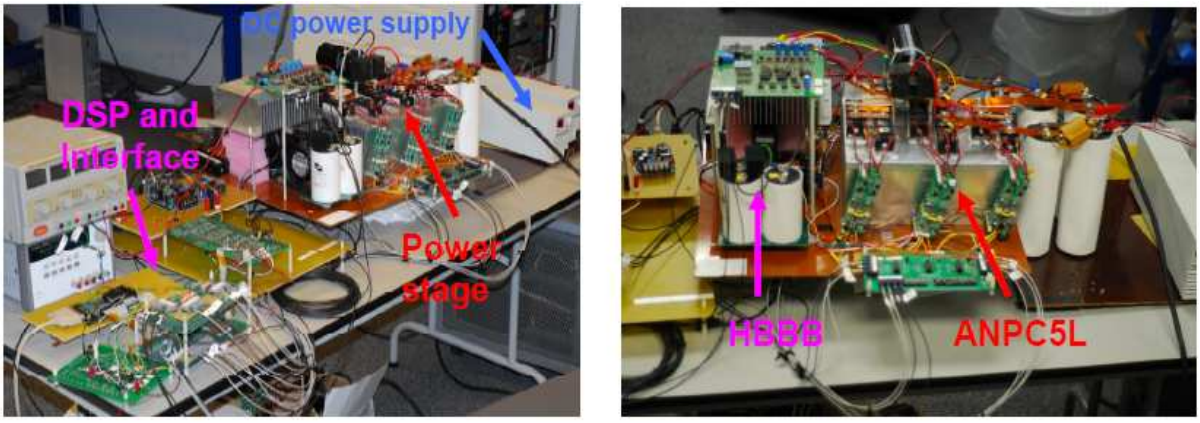
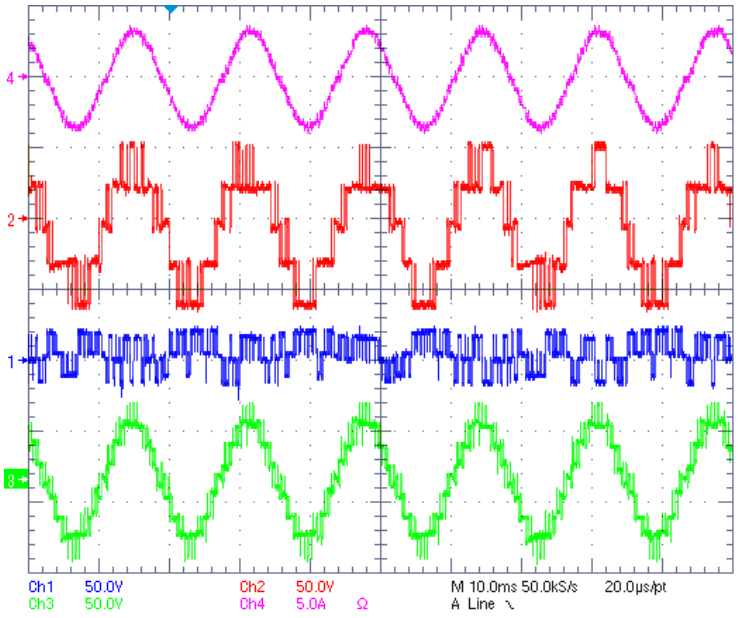


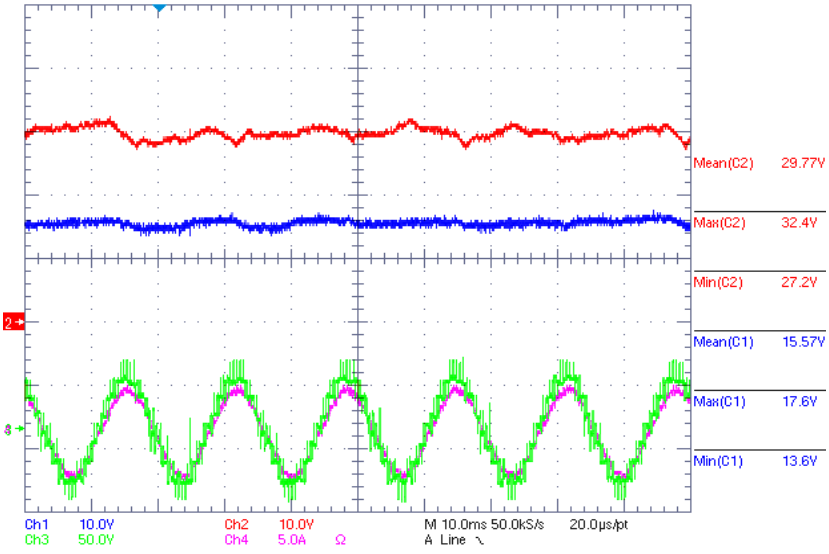
Fig. 4.16 Experiment prototype of the new 9-level ANPC PEBB

Fig. 4.17 and Fig. 4.18 show the steady-state waveforms using a modulation index of 0.8 and 0.96, respectively. The load current, the phase voltage of 5L-ANPC PEBB, the phase voltage of HBBB and the phase voltage of the new 9-level ANPC converter are shown from top to bottom in Fig. 4.17 (a) and Fig. 4.18 (a) for the two modulation index cases, respectively. Fig. 4.17 (b) and Fig. 4.18 (b) show the floating capacitor voltages, the load

current and the phase voltage of the 9-level ANPC converter for the two modulation index cases, respectively.

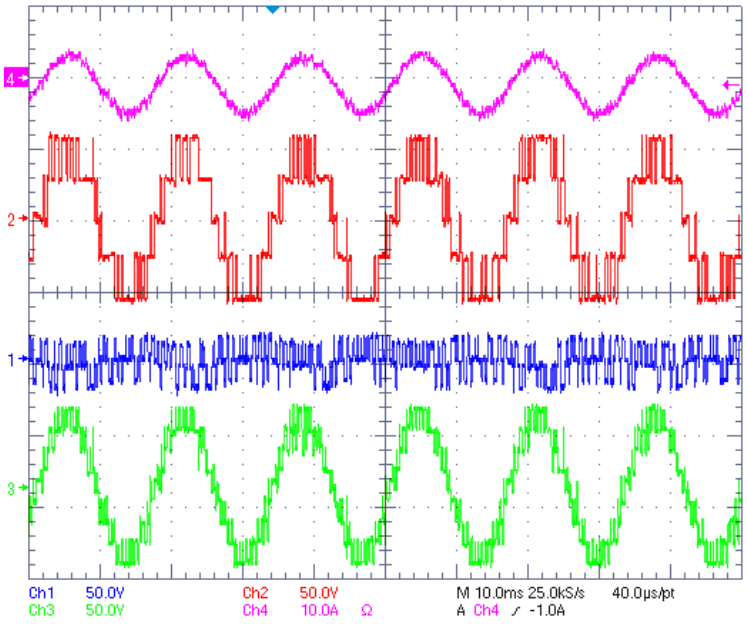


(a) Load current (pink), 5L-ANPC phase voltage (red), HBBB phase voltage (blue) and 9L ANPC converter phase voltage (green) from top to bottom

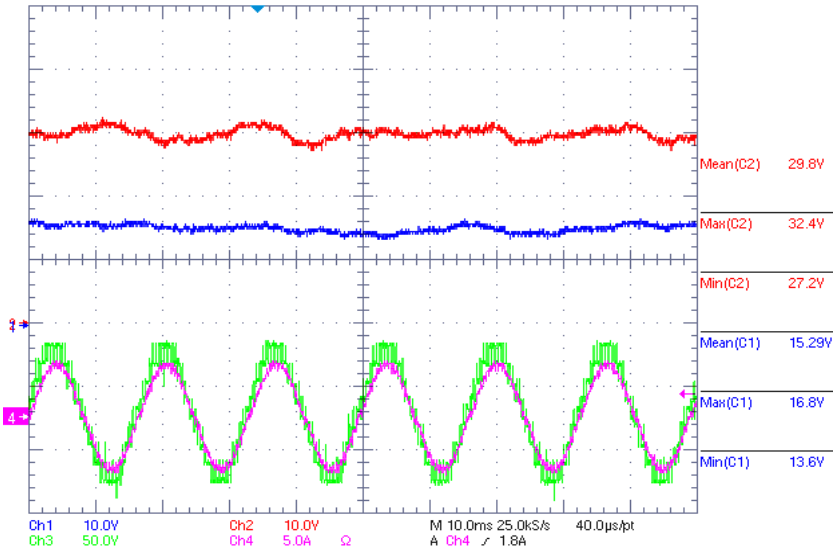


(b) C_1 voltage (red), C_2 voltage (blue), load current (pink) and phase voltage (green) of the new 9-level ANPC converter from top to bottom

Fig. 4.17 Waveforms of the new 9-level ANPC converter using a modulation index=0.8



(a) Load current (pink), 5L-ANPC phase voltage (red), HBBB phase voltage (blue) and 9L ANPC converter phase voltage (green) from top to bottom



(b) C_1 voltage (red), C_2 voltage (blue), load current (pink) and phase voltage (green) of the new 9-level ANPC converter from top to bottom

Fig. 4.18 Waveforms of the new 9-level ANPC converter using a modulation index=0.96

Fig. 4.19 and Fig. 4.20 show the dynamic-state waveforms with the change of the modulation index within a certain time. In Fig. 4.19, the modulation index increases from 0.8 to 0.96 within 160ms. During this period, the output phase voltage of the 9-level ANPC converter is always a 9-level waveform. In Fig. 4.20, the modulation index increases from 0.7 to 0.84 within 100ms. During this period, the output phase voltage of the 9-level ANPC converter moves from a 7-level waveform to a 9-level waveform. In both figures, the floating capacitor C_1 voltage, the floating capacitor C_2 voltage and the output phase voltage of the 9-level ANPC converter are shown from top to bottom.

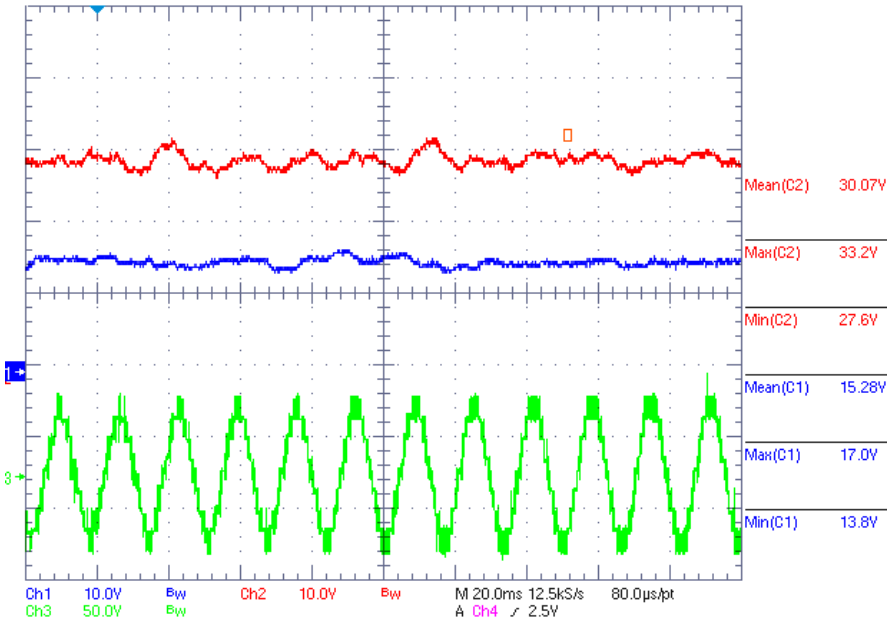


Fig. 4.19 Waveforms of the new 9L ANPC converter when modulation index changes from 0.8 to 0.96 with 160ms: C_1 voltage (red), C_2 voltage (blue) and output phase voltage (green) from top to bottom

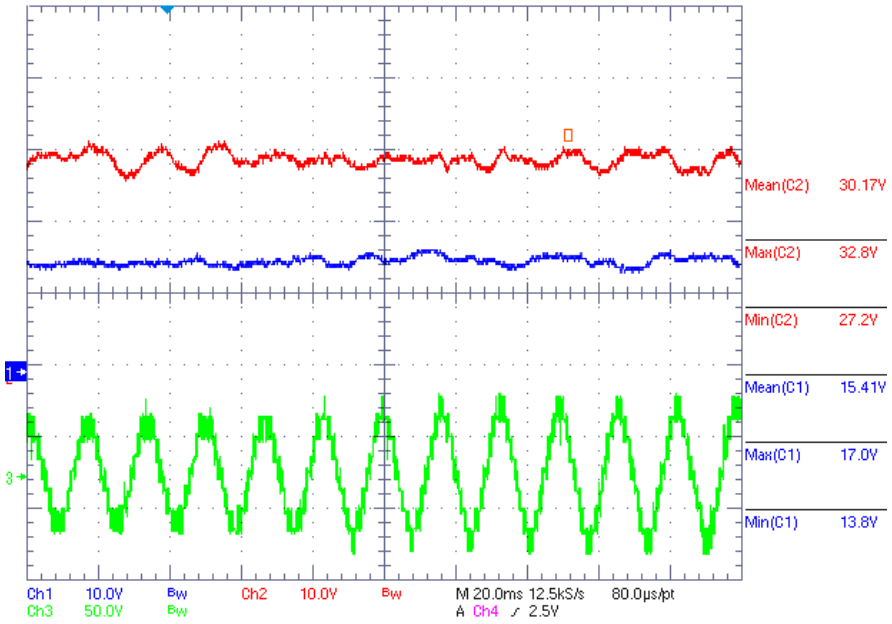


Fig. 4.20 Waveforms of the new 9L ANPC converter when modulation index changes from 0.7 to 0.84 with 100ms: C_1 voltage (red), C_2 voltage (blue) and output phase voltage (green) from top to bottom

The experiment results show that the proposed 9-level ANPC converter is able to generate 9 voltage levels by combining the output phase voltages of the 5L-ANPC PEBB and HBBB. The proposed control scheme is able to balance the floating capacitor voltage for both steady-state and dynamic operations.

4.4 Comparison of Different 9-Level Converter Topologies

In this section, the proposed new 9-level ANPC converter is compared with other conventional 9-level converters and 9-level ANPC converters.

4.4.1 Conventional 9-Level Converter Topologies

The most popular conventional multilevel converters are neutral-point-clamped (NPC) topology, flying capacitor (FC) topology and cascaded H-bridge (CHB) topology. They are mostly used in commercial products as 3-level, 4-level and 5-level converters. However, they

have some limitations when the number of the output voltage levels becomes higher, such as the 9-level topologies in this study for the filterless grid connection of large wind turbine systems:

- For the NPC topology, the large number of clamping diodes and the voltage balance of the dc-link capacitors are big issues for the NPC converter with higher number of voltage levels. The unbalanced loss distribution among the devices in the NPC converter is another drawback.
- For the FC topology, the number of floating capacitors, and therefore the total stored energy is large for a 9-level converter. Moreover, for high power wind power generation, considering the switching loss of power devices, the converter switching frequency can not be high, thus the size and cost of the floating capacitors are the main disadvantage.
- For the CHB topology, it requires a large number of isolated dc voltage sources. In MV drive applications, these dc sources are usually provided from the bulky multi-winding transformers and rectifiers, which is not practical for wind power converters. Another solution is to feed the dc-link of each H-bridge with a special-designed medium/high frequency transformer connected to a front-end rectifier. However, it will greatly increase the complexity and the cost of the converter and the system, thus making it inappropriate for wind turbine systems.

4.4.2 The 9-Level ANPC Converter Topologies

Compared with the conventional multilevel converter topologies, the characteristics of the ANPC converters, such as the improved thermal management of the power devices, higher output power rating and switching frequency, and easier expansion for higher number of voltage levels, make them attractive as the power electronics interface for a filterless grid connection in large wind turbine systems.

The proposed new 9-level ANPC converter is compared with other existing 9-level ANPC topologies from several aspects, including the number of individual power devices, the total switch blocking voltage, the selection of the commercial power device products, the floating capacitor number, the voltage rating and the total stored energy, and the limitation of the maximum modulation index at full active power delivery. The number of semiconductor devices and their blocking voltage ratings give an idea about the cost, reliability and the losses of the converter. The total device blocking voltage indicates the total amount of silicon installed, which is linked with the cost of the converter. The total number of capacitors and their voltage ratings define the total stored energy, thus representing the bulk and reliability of the converter, and the impact on the cost and power density of the system. The maximum modulation index reflects the utilization of the dc-link voltage and the output power rating of the converter.

In [105], the stored energy in the floating capacitor of the converter was found to have a linear relation with the capacitor voltage, as explained below.

First, we assume that all of the compared 9L converter topologies are switched with the same carrier frequency at the same nominal operating point. The energy in the capacitor is:

$$E_C = \frac{1}{2} \cdot C \cdot V_C{}^2 \tag{4-9}$$

According to (4-1), (4-9) can be re-written as (4-10).

$$E_C = \frac{1}{2} \cdot \frac{I_{pk}}{\Delta V_C} \frac{1}{f_c} \cdot V_C{}^2 \tag{4-10}$$

Since we have:

$$\Delta V_C = \eta \cdot V_C \tag{4-11}$$

Here, η is the voltage ripple across the floating capacitor, given in per unit based on the capacitor rated voltage. For example, a 15% voltage ripple on the capacitor means η equals to 0.15. Substituting (4-11) into (4-10), we obtain (4-12).

$$E_C = \frac{1}{2} \cdot \frac{I_{pk}}{\eta} \frac{1}{f_c} \cdot V_C \tag{4-12}$$

Since all the converters are assumed to work at the same nominal operating point and switching frequency, the values of I_{pk}, η and f_c in (4-12) are identical for all the capacitors in different 9-level ANPC converters. This indicates that the stored energy in the capacitor has a linear relation with the capacitor voltage. Therefore, to compare the stored energy in all the floating capacitors in different 9L converters, only the number and voltage of the floating capacitors are needed, which is expressed by (4-13).

$$E_{total} = k \cdot \sum_{i=1}^{\#\,of\ caps} V_{C(i)} \tag{4-13}$$

Here, k is a constant factor.

A comparison of the results is given in Table 4-3. In the table, "V_{dc}" is half of the DC bus voltage. Since the dc-link voltage of the proposed 9L converter is selected to be 6.4 kV, V_{dc} equals 3.2 kV.

Table 4-3 Comparison of different 9-level ANPC converters (three-phase configuration)

	5L-ANPC plus HBBB converter	ANPC standard converter	CCCS converter	CCIL converter	3L-ANPC plus HBBBs converter
Individual switch number	36	36	30	42	42
Total switch blocking voltage	$21V_{dc}$	$18\ V_{dc}$	$24\ V_{dc}$	$22.5\ V_{dc}$	$27\ V_{dc}$
Selected commercial device rating	12 * 6.5kV +12 * 3.3kV +12 * 1.7kV	12 * 6.5kV +24 * 1.7kV	24 * 4.5kV +18* 3.3kV +6 * 1.7kV	12 * 6.5kV +12 * 3.3kV +18 * 1.7kV	18 * 6.5kV +12 * 3.3kV +12 * 1.7 kV
Floating capacitor number	6	9	4	6	6
Capacitor sustained voltage	$3 * V_{dc}/2$ $+3 * V_{dc}/4$	$3 * 3\ V_{dc}/4$ $+3 * V_{dc}/2$ $+3 * V_{dc}/4$	$3 * V_{dc}/2$ $+1 * V_{dc}/4$	$3 * V_{dc}/2$ $+3 * V_{dc}/4$	$3 * V_{dc}/2$ $+3 * V_{dc}/4$
Total stored energy (p.u.)	1	2	0.78	1	1
Modulation index limit at full active power delivery	1.15	1.15	0.925	1.15	1.15

According to the results in Table 4-3, the CCCS converter has the smallest individual switch number and floating capacitor number. This is because the CCCS PEBB is common to all three phases of the converter. However, its total switch blocking voltage is larger. In fact, considering the selection from the commercial power device products, its switch number is the highest among all the compared topologies. Another issue is that its maximum modulation index is only 0.925 at full active power, which limits its applications.

The ANPC standard converter has a smaller total switch blocking voltage. However, it needs 3 additional capacitors which need to withstand the voltage level at $3V_{dc}/4$. Due to the switching frequency limitation in high power applications, such capacitors are bulky and expensive, and account for a fraction of converter failure. Their higher stored energy is also a drawback in terms of system reliability.

Another option, not shown in Table 4-3, is the 3L-NPC plus HBBBs converter. Compared with the 3L-ANPC plus HBBBs topology, the only difference is that it uses 3L-NPC PEBB instead of 3L-ANPC PEBB. The drawback of this topology is apparent compared with the proposed ANPC topology. First, it needs 6 additional clamping diodes rated at 6.5kV voltage rating. Moreover, since it can not balance the device losses, larger devices have to be used (e.g. 91mm instead of 68mm ETO thyristors).

The proposed 9-level ANPC converter shows better overall features compared to other conventional 9-level converters and 9-level ANPC converters. Furthermore, both the 5L-ANPC and HBBB are standard building blocks in the market, so the technical risk is low, and the mechanical installation is much easier and more practical compared with other solutions, especially in the case of upgrading an existing 5L-ANPC converter to 9L topology in the wind turbine system. Therefore it provides an effective and practical solution for the filterless grid connection of MW wind turbine systems.

4.5 Application of the New 9-Level ANPC Converter

4.5.1 Description of the Filterless Wind Turbine System

In this work, the proposed 9-level ANPC converter is applied on the grid side of a large wind turbine system without passive grid filters. The system configuration is shown in Fig. 4.21. As seen, the grid filter is removed, and the 9-level ANPC converter is directly connected to the point of common coupling (PCC) through a feeder transformer which adjusts to higher utility voltages by using a proper turns-ratio.

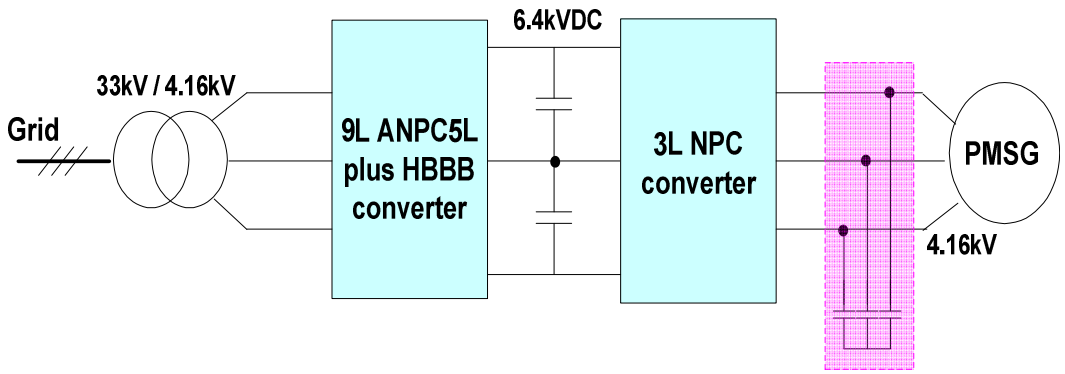


Fig. 4.21 Filterless grid connection of the large wind turbine system with the new 9-level ANPC converter

The proposed 9-level ANPC converter is targeted at a 5~6 MW wind turbine. The dc-link voltage is 6.4 kVDC. The rated converter output line-to-line voltage and the transformer secondary side rated line-to-line voltage is 4.16 kVAC at 60 Hz. The modulation index at the nominal operating point is 1.062. The PWM carrier frequency of the 9-level ANPC converter is 2 kHz, which is appropriately selected for the high power level and meeting the harmonic limits of the utility standards. The impedance of the transformer is 12% of the base impedance, and this is reasonable considering the secondary fault current for a 5~6 MW power converter. The most stringent requirement of IEEE519 for meeting harmonic limit is at low short circuit ratios (SCR) equal to 20. The simulation model for the grid side is shown in Fig. 4.22, which is represented by a series connection of inductance, resistance and equivalent voltage source. The inductance is calculated as 12% of the base impedance for the feeder transformer, plus a grid SCR of 20. The resistance is calculated as 2% of the base impedance. The RMS voltage of the AC voltage source is 4.16 kVAC (line-to-line) at 60 Hz. The floating capacitors of the 9-level ANPC converter are C_1=2 mF and C_2=4 mF.

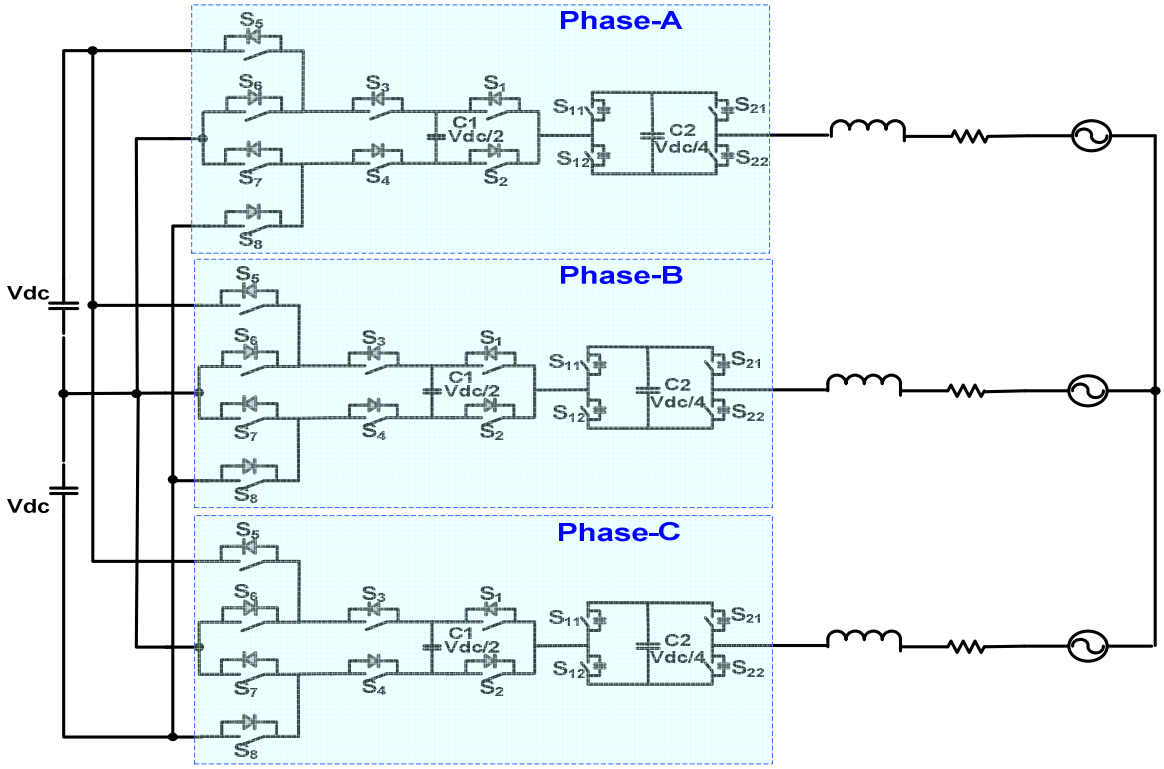


Fig. 4.22 Filterless grid side configuration of the large wind turbine system in the simulation model

The proposed 9-level ANPC grid converter controls the active power production of the wind turbine and the grid side power factor. A standard d-q decoupled vector control is used for the system. In Fig. 4.23, the reactive power reference, Q_{ref}, is set to be 0 for unity power factor. The active power reference P_{ref} is calculated from the MPPT algorithm. In this simulation, P_{ref} is set at 1 p.u. as full active power transfer. The dc-link is modeled by two constant dc voltage sources assuming that the generator converter keeps the dc-link voltage constant and the neutral-point voltage balanced. The floating capacitor voltages, the direction of the output currents and the reference voltage signals are used in the SPWM modulator for the voltage control of the floating capacitors.

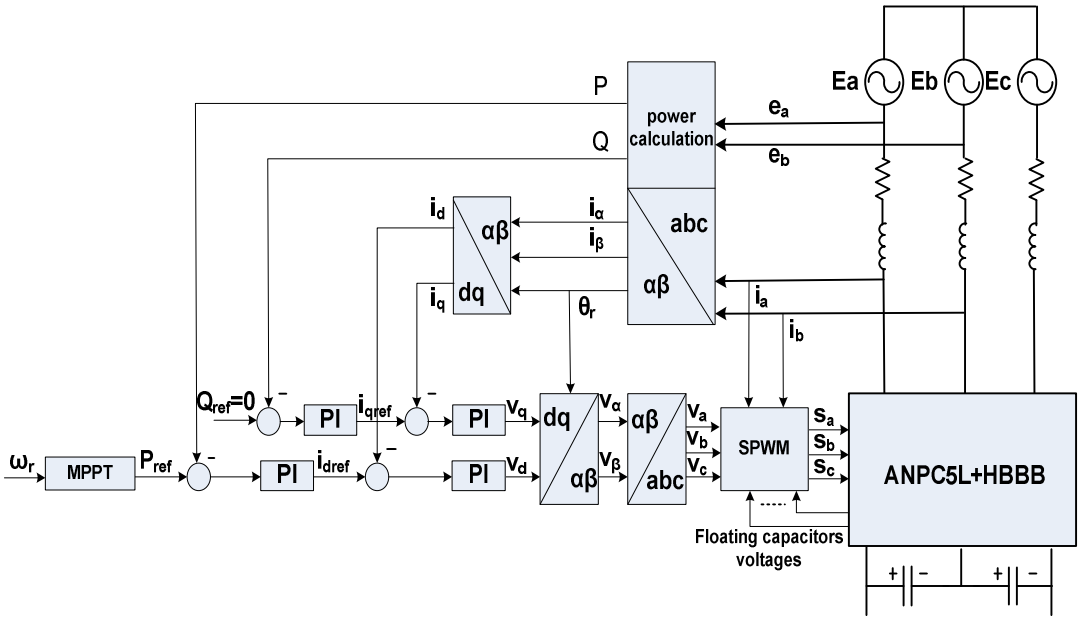
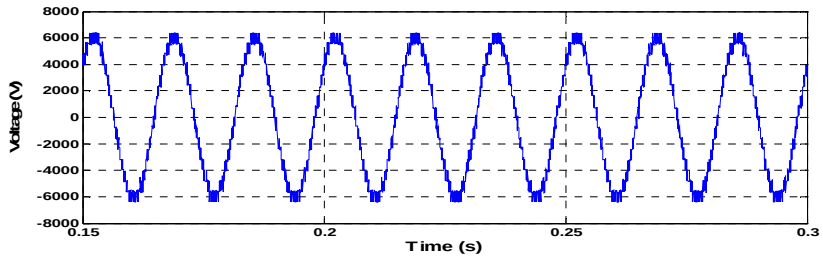


Fig. 4.23 The controller diagram of the grid converter

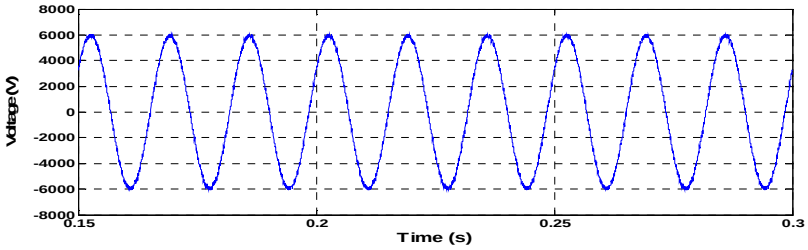
4.5.2 Simulation Verification

To verify the operation of the proposed 9-level ANPC converter in the large wind turbine system and the fulfillment of the harmonic limit requirement of utility standards without using a grid passive filter, the model, shown in Fig. 4.22, is simulated in MATLAB/Simulink.

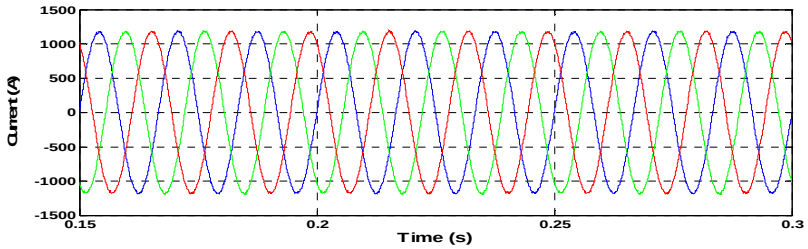
Fig. 4.24 shows the output line-to-line voltage of the converter, the line-to-line voltage and the line current at the PCC of the grid, the floating capacitor voltages of the converter from top to bottom. The results show that the proposed 9-level ANPC converter can generate a 17-level line-to-line voltage waveform using the presented control method. The six floating capacitor voltages in all three phases can be balanced around the reference values (1.6 kVDC for C_1, and 800Vdc for C_2) at full active power delivery. The average voltage ripples for C_1 and C_2 are 6.25% and 13.75%, respectively. The voltage ripple can be reduced if larger capacitance values are chosen.



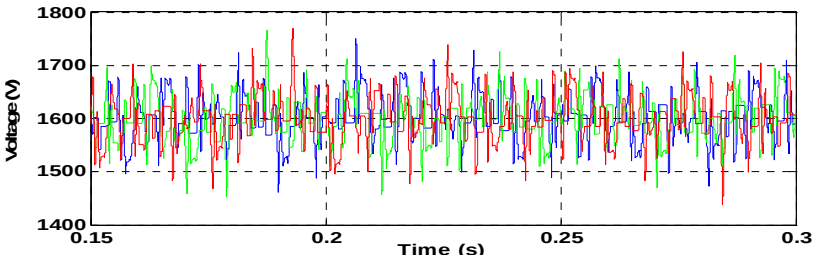
(a) Output line-to-line voltage of the converter



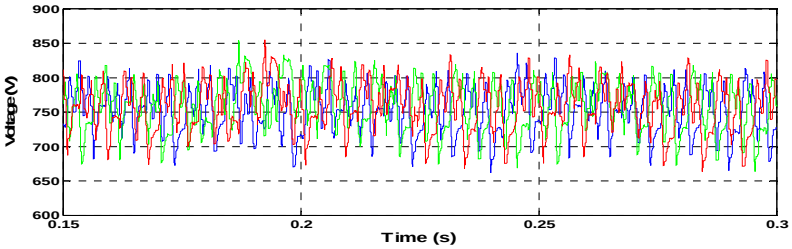
(b) Line-to-line voltage at PCC of the grid



(c) Line currents at PCC of the grid



(d) C_1 voltage in three phases



(e) C_2 voltage in three phases

Fig. 4.24 Waveforms of the proposed converter for filterless grid connection of large wind turbine system

To verify the grid connection compliance to the harmonic limits of the utility standards, Fig. 4.25 illustrates the converter compliance with IEC 61000-2-12 voltage harmonic limits at the PCC [109]. Fig. 4.26 illustrates the converter compliance with IEEE519 and VDEW current harmonic limits at the PCC [110] [111].

The PCC line-to-line voltage THD up to the 50th order harmonic is 1.02%, which is less than IEC61000-2-12 standard of 8%. The line current THD up to 100th order harmonic is 0.59% and it is less than IEEE519 standard of 5%. Moreover, Fig. 4.25 and Fig. 4.26 show that, with the proposed 9-level ANPC converter topology and control scheme, the distribution of the harmonics across the frequency spectrum also meets the standard requirements.

The results prove that the new 9-level ANPC converter enables the filterless grid connection for large wind turbine systems.

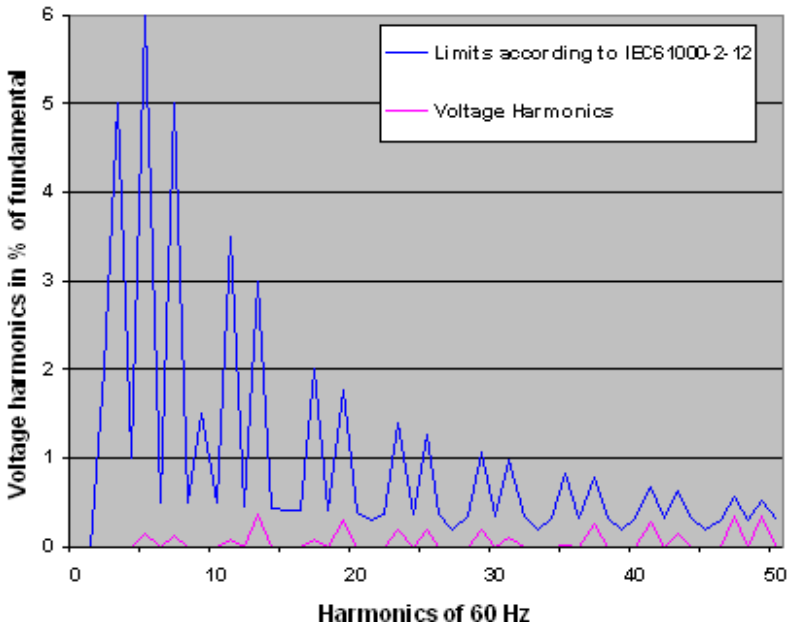


Fig. 4.25 Voltage harmonics at the PCC and applicable limits

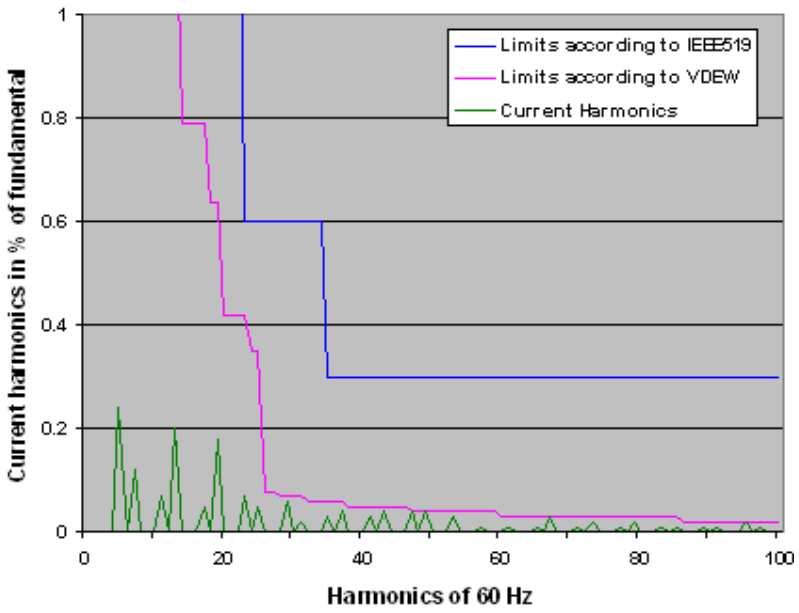


Fig. 4.26 Current harmonics at the PCC and applicable limits

4.6 Summary

The next generation high power PEBB technology requires the multilevel converters with a higher number of voltage levels (5-level, 9-level) to reduce or even remove the bulky passive filter, thus reduce the size and weight of the converter and the overall system.

This work proposes a new 9-level ANPC converter topology for high power medium voltage applications. The new converter combines the 5L-ANPC PEBB and HBBB together to generate a 9-level voltage waveform, and its operating principles and control are presented. To balance the floating capacitor voltages, the strategy for the redundant switching state selection based on the priority information of the floating capacitors is presented in detail. The hybrid converter concept is discussed for the proposed topology, in which different types of power devices are employed to explore their individual advantages. The main advantages of the new 9-level ANPC converter include less potential technical risk associated with the

converter topology innovations, few mechanical structure modifications and easy installation if upgrading from 5L-ANPC to 9L converter, independent per-phase control and easier controller design for floating capacitor voltage balance, no maximum modulation index limit at full active power delivery, the 3L-NPC and 3L-ANPC dc-link infrastructure remain if a direct connection to a 3L-NPC or 3L-ANPC generator side converter in a back-to-back converter configuration is desired. Simulation and experiment results validate the proposed concept.

To illustrate the benefits of the new topology, it is compared with other conventional 9-level converters and existing 9-level ANPC converters from several aspects including the number of individual power devices, the total switch blocking voltage, the selection from commercial power device products, the floating capacitors number, voltage rating and the total stored energy, and the limitation of maximum modulation index at full active power transfer. The results show that new ANPC converter shows better overall performance among all the 9-level converters.

Finally, the proposed topology is applied on the grid side of a MW wind turbine system to achieve a filterless grid connection. The system configuration and control scheme are discussed. The simulation results prove that the proposed system configuration fulfills the harmonic limit requirement of the utility standards even without using the grid passive filter. This feature implies that the cost, efficiency, power density and reliability of the large wind turbine system can be improved.

Chapter 5 A Simplified Space Vector Based Current Controller for Any General N-Level Converter

In this chapter, using mapping techniques, a simplified current controller for any general N-level converter based on space vector theory is proposed to suppress harmonic current content during steady state operation and obtain fast current response during transient operation. Such current controller performance is very important for high power motor drive systems, in which the reference motor speed input can be either constant or a fast ramp depending on the required motor operating condition. In wind turbine systems, depending on the wind condition, either stable or turbulent wind speed can be foreseen. In both applications, the design of the current controller needs to consider the requirement of low harmonic current content in steady state and fast current response in transient state.

5.1 Current Controller of Multilevel Converters

The performance of the multilevel converters in industrial applications largely depends on the quality of the applied current controller. The basic requirements of a current controller include a low current harmonic content in steady state and a quick current response in transient state [112] [113] [114].

In [115], a PWM current controller for two-level converters based on space vector (SV) theory was introduced to satisfy the controller requirements above. Different from the predictive current controller, this control technique uses feedback control and requires less complicated calculations. The SV-based current controller was further extended and applied for a three-level NPC converter in a vector-controlled motor drive system in [116]. However,

the information about the load parameters is required for the calculation of the back EMF voltage of the motor. To overcome this drawback, an improved method based on lookup tables was introduced in [117], which avoided calculating the back EMF voltage. This feature is very useful when the back EMF voltage is difficult to calculate accurately (e.g. load parameters are unknown, or motor operates at low speed) or when it is already given (e.g. PCC voltage in grid connection system). However, this improved current controller needs large and complicated lookup tables, which prohibits its application in multilevel converters with higher number of levels.

5.2 Principle of the SV-based Current Controller for Two-level Converters

Fig. 5.1 shows the equivalent circuit of a two-level voltage source converter. The relation between the voltage and the current vectors are expressed as follows:

$$\boldsymbol{v}_k = L \cdot \frac{d\boldsymbol{i}}{dt} + R \cdot \boldsymbol{i} + \boldsymbol{e}_n \qquad \textbf{(5-1)}$$

Here $\boldsymbol{v}_k$ is the converter output voltage vector and $\boldsymbol{i}$ is the load current vector. $\boldsymbol{e}_n$ is the back EMF voltage vector, which represents the inner reduced voltage vector for a motor drive system, or the PCC voltage vector for a grid connected system.

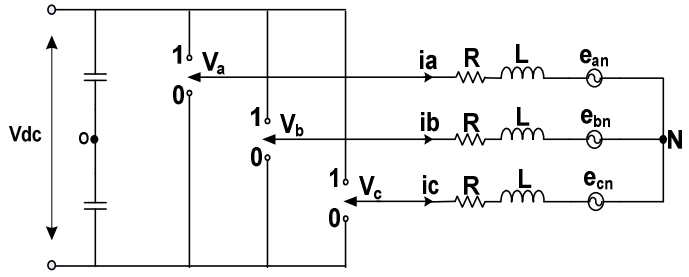


Fig. 5.1 Equivalent two-level converter circuit

The voltage vector diagram of the two-level converter is shown in Fig. 5.2. As seen, corresponding to the on and off state of the switching devices, there are totally 7 independent output voltage vectors $\boldsymbol{v}_0 \sim \boldsymbol{v}_6$, while $\boldsymbol{v}_0$ has two redundant switching states (0 0 0) and (1 1 1). Here, "1" represents the phase output is connected to the positive DC bus by turning-on the upper switch, while "0" represents the phase output is connected to the negative DC bus by turning-on the lower switch.

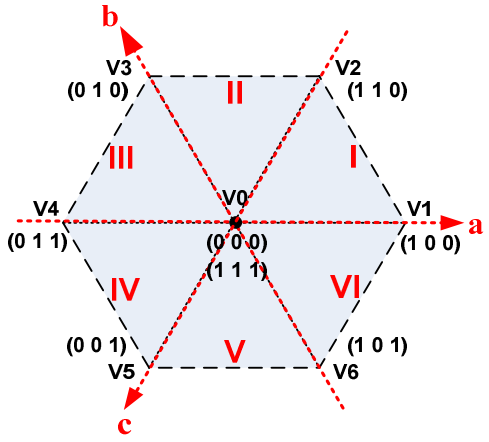


Fig. 5.2 Voltage vector diagram of the two-level converter

The current deviation vector is defined as (5-2):

$$\boldsymbol{\Delta i} = \boldsymbol{i}^* - \boldsymbol{i} \tag{5-2}$$

Where $\boldsymbol{i}^*$ is the reference current vector.

Substituting (5-2) into (5-1) and manipulating, we obtain (5-3):

$$L \cdot \frac{d\Delta \boldsymbol{i}}{dt} + R \cdot \Delta \boldsymbol{i} = \left(L \cdot \frac{d\boldsymbol{i}^*}{dt} + R \cdot \boldsymbol{i}^* + \boldsymbol{e}_n \right) - \boldsymbol{v}_k \tag{5-3}$$

Generally, $R \cdot \Delta \boldsymbol{i}$ is small and can be neglected, so the following equations are obtained:

$$L \cdot \frac{d\Delta \boldsymbol{i}}{dt} \approx \boldsymbol{e} - \boldsymbol{v}_k \tag{5-4}$$

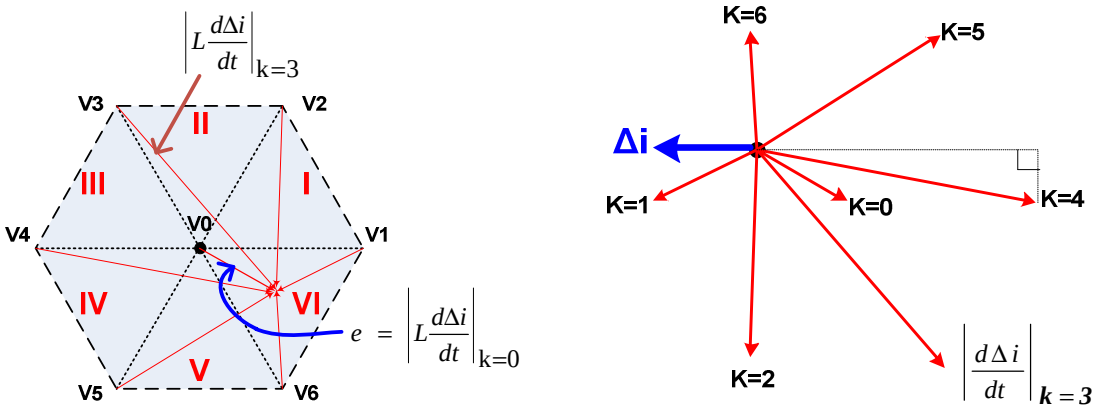
$$\boldsymbol{e} = L \cdot \frac{d\boldsymbol{i}^*}{dt} + R \cdot \boldsymbol{i}^* + \boldsymbol{e}_n \qquad \textbf{(5-5)}$$

Where $\boldsymbol{e}$ represents the voltage vector at the load side.

The value of $d\Delta\boldsymbol{i}/dt$ depends on the selected $\boldsymbol{v}_k$, and it determines the performance of the current controller.

In [115], the author proposed that to reduce the harmonic current content in steady state, the output voltage vector, which is located on the vertexes of the small triangle region that $\boldsymbol{e}$ belongs to, and the corresponding $d\Delta\boldsymbol{i}/dt$ has the smallest opposite direction component to $\Delta\boldsymbol{i}$ should be selected. To obtain a fast current response in transient state, the output voltage vector, whose corresponding $d\Delta\boldsymbol{i}/dt$ has the largest opposite direction component to $\Delta\boldsymbol{i}$, should be chosen. One example is given below for explanation.

First we assume $\boldsymbol{e}$ belongs to the triangle VI, which is surrounded by $\boldsymbol{v}_0$, $\boldsymbol{v}_1$ and $\boldsymbol{v}_6$. $L \cdot d\Delta\boldsymbol{i}/dt$ can be obtained depending on the selected $\boldsymbol{v}_k$, as shown in Fig. 5.3 (a). We assume $\Delta\boldsymbol{i}$ is detected in the position as given in Fig. 5.3 (b). For the voltage vector $v_{k|k=4}$, its corresponding $d\Delta\boldsymbol{i}/dt$ has the largest opposite direction component to $\Delta\boldsymbol{i}$, therefore, it is selected for fast current response in transient state. Among all the three voltage vectors on the vertexes of the triangle VI, the voltage vector $v_{k|k=0}$, whose corresponding $d\Delta\boldsymbol{i}/dt$ has the smallest opposite direction component to $\Delta\boldsymbol{i}$, should be selected for low harmonic current content in steady state.



(a) (b)

Fig. 5.3 Example of the SV-based current controller for two-level converters (a) output voltage vector v_k and the corresponding $|L \cdot d\Delta i / dt|_k$ (b) current deviation vector Δi and its derivatives $|d\Delta i / dt|_k$

5.3 The Proposed Simplified SV-based Current Controller

In this section, the simplified SV-based current controller for multilevel converters with a higher number of levels is proposed. As a case study, a five-level active NPC converter is used to explain and demonstrate the proposed current controller.

5.3.1 Five-level Active NPC Converters

The phase-leg circuit of a five-level active NPC converter is re-drawn in Fig. 5.4 below. It is actually a hybrid multilevel converter topology, which combines the 3L-ANPC leg with a 3L-FC cell connected between the internal ANPC switches. The voltage of the intermediate floating capacitor is 1/4 of the total dc-link voltage, and its voltage must be kept balanced to assure the proper operation of the converter.

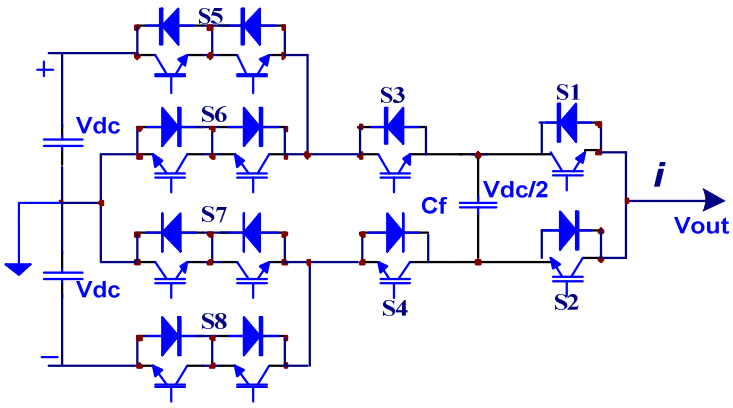


Fig. 5.4 Five-level active NPC converter

In a five-level ANPC converter, each phase is able to generate five output voltage levels from eight different switching combinations as listed in Table 5-1. In the table, "n/a", "+" and "-" represent no impact, charge and discharge for the floating capacitor, respectively. The redundant switching states, which can generate the same output voltage level, are observed. For example, the voltage $V_{dc}/2$ can be obtained by the switching state V2 or V3. Nevertheless, they have opposite impacts on the floating capacitor voltage. For positive output current (flowing out of the phase AC terminal), V2 charges the floating capacitor while V3 discharges it. Therefore, they can be used to control the floating capacitor voltage.

The voltage vector diagram of a three-phase 5L-ANPC converter is shown in Fig. 5.5. The converter has 61 independent output voltage vectors, and some of them have redundant switching states. For example, for the voltage vector $\boldsymbol{v}_0$, it has five redundant switching states (0 0 0), (1 1 1), (2 2 2), (3 3 3) and (4 4 4). For the voltage vector $\boldsymbol{v}_1$, it has four redundant switching states (1 0 0), (2 1 1), (3 2 2), and (4 3 3). Here, the three-phase switching state (*a b c*) is labeled according to the output voltage and the switching state in each phase leg of the 5L-ANPC converter, as given in Table 5-1.

Table 5-1 Output voltage and switching states of a five-level active NPC converter

S8	S7	S6	S5	S4	S3	S2	S1	Output voltage	Effect on Cf		Switching state
									I>0	I<0	
0	1	0	1	0	1	0	1	V_{dc}	n/a	n/a	4 (V1)
0	1	0	1	0	1	1	0	V_{dc} /2	+	-	3 (V2)
0	1	0	1	1	0	0	1	V_{dc} /2	-	+	3 (V3)
0	1	0	1	1	0	1	0	0	n/a	n/a	2 (V4)
1	0	1	0	0	1	0	1	0	n/a	n/a	2 (V5)
1	0	1	0	0	1	1	0	- V_{dc} /2	+	-	1 (V6)
1	0	1	0	1	0	0	1	- V_{dc} /2	-	+	1 (V7)
1	0	1	0	1	0	1	0	-V_{dc}	n/a	n/a	0 (V8)

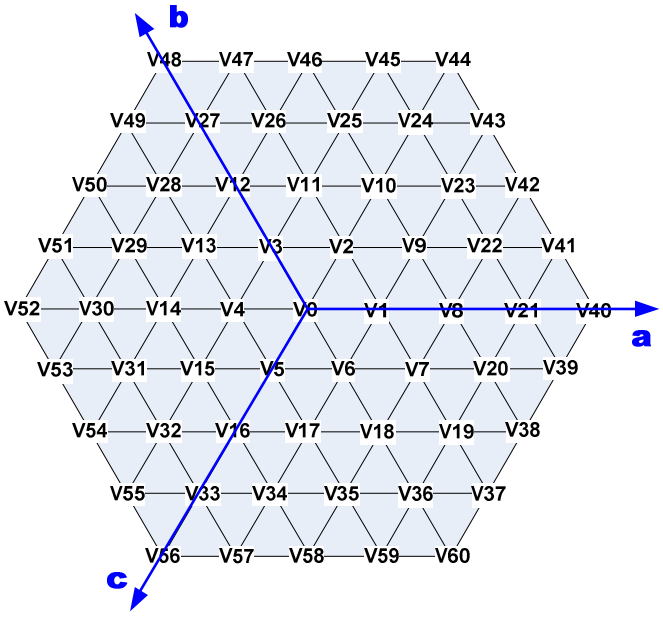


Fig. 5.5 Space vector diagram of a three-phase five-level ANPC converter

In this work, the small triangle formed by the adjacent three output voltage vectors is defined as a sector. Six adjacent sectors surrounding a center voltage vector form a hexagon, named subhexagon. For example, in Fig. 5.5, one sector is formed by the 3 adjacent voltage vectors $\boldsymbol{v}_0 \sim \boldsymbol{v}_2$, and one subhexagon is formed by $\boldsymbol{v}_0 \sim \boldsymbol{v}_6$, while $\boldsymbol{v}_0$ is located at the center.

In the following sections, the proposed current controller is explained in detail showing how to choose the proper output voltage vector, the optimum switching state and switching sequence for the steady state and the transient state, respectively.

5.3.2 Voltage Vector Selection to Suppress Harmonic Current Content in Steady State

As discussed previously in the example of the two-level converter in Fig. 5.3, in order to find the proper voltage vector to suppress the current harmonic content in steady state, we need to know the region of $\boldsymbol{e}$ and $\boldsymbol{\Delta i}$ [115] [117]. To do this, besides the "*a*-*b*-*c*" coordinate system shown in Fig. 5.2 and Fig. 5.5, another "*x*-*y*-*z*" coordinate system, in which the new *x*-*y*-*z* axes rotate counterclockwise 30° from the *a*-*b*-*c* axes, as shown in Fig. 5.6, is needed for defining the region of $\boldsymbol{\Delta i}$ and detecting the region of $\boldsymbol{e}$. The following relation exists between the "*a*-*b*-*c*" coordinates and the "*x*-*y*-*z*" coordinates:

$$\begin{bmatrix} x \\ y \\ z \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} 1 & 0 & -1 \\ -1 & 1 & 0 \\ 0 & -1 & 1 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad \textbf{(5-6)}$$

Fig. 5.6 shows that the regions of the current vectors are separated by the "*x*-*y*-*z*" axes and divided into the regions labeled 1 to 6. Moreover, the mapping relation of the current vector regions between the 5L-ANPC converter and the two-level converter is also illustrated in Fig. 5.6. As seen, since the positions of the *x*-*y*-*z* axes and the current vector regions are not changed between the two converters, it indicates that the same method for the two-level converter can be used to determine the region of $\boldsymbol{\Delta i}$ for the 5L-ANPC converter. The lookup table for the region detection of $\boldsymbol{\Delta i}$ is summarized in Table 5-2. In the table, "1" indicates a

plus sign and "0" indicates a minus sign. It can be observed that only the polarity of the each phase current deviation Δi_a, Δi_b and Δi_c is needed, which is easy to calculate. For instance, if Δi_b and Δi_c are positive, then Δi is in region 4, regardless of the polarity of Δi_a.

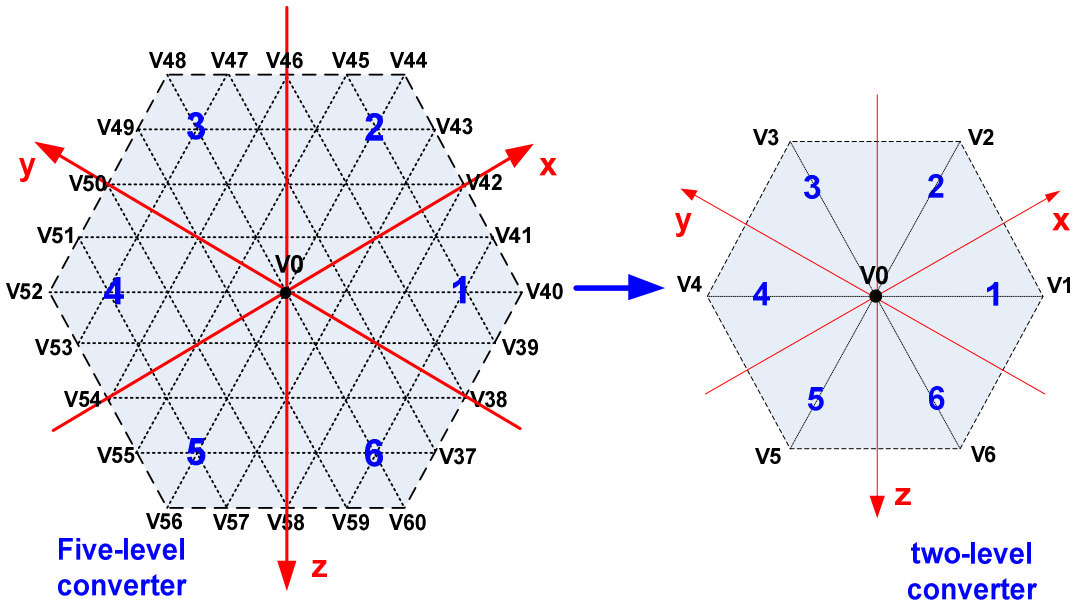


Fig. 5.6 Mapping of the current vector regions between five-level and two-level converters

Table 5-2 Region detection of Δi

Δi_a	Δi_b	Δi_c	Region of Δi
-	0	0	1
1	1	-	2
0	-	0	3
-	1	1	4
0	0	-	5
1	-	1	6

For a two-level converter, the region of e, shown in Fig. 5.2, is divided into region I to region VI. It has been found that when the region of e and Δi are known, then based on the principle of the SV-based current controller, the proper output voltage vector can be

determined to suppress harmonic current content in steady state according to Table 5-3 [115]. For example, if $\boldsymbol{e}$ is in region V, and $\Delta\boldsymbol{i}$ is in region 4, then $\boldsymbol{v}_5$ should be selected.

Table 5-3 Region of $\Delta\boldsymbol{i}$, $\boldsymbol{e}$ and the selected $\boldsymbol{v}_k$ for the two-level converter in steady state

Region of $\boldsymbol{e}$	Region of $\Delta\boldsymbol{i}$					
	1	2	3	4	5	6
I	V_1	V_2	V_2	V_0	V_0	V_1
II	V_2	V_2	V_3	V_3	V_0	V_0
III	V_0	V_3	V_3	V_4	V_4	V_0
IV	V_0	V_0	V_4	V_4	V_5	V_5
V	V_6	V_0	V_0	V_5	V_5	V_6
VI	V_1	V_1	V_0	V_0	V_6	V_6

As analyzed above, to find the proper output voltage vector, the region of $\boldsymbol{e}$ must be detected first. For the case of a 5-level ANPC converter, this means that the sector in which $\boldsymbol{e}$ belongs to, needs to be identified first.

In [115], it proposed to use the information of the present $\boldsymbol{v}_k$ and the signs of the current deviation vector derivatives to judge the region of $\boldsymbol{e}$ in the two-level converter. This method is shortly explained here. According to the principle of the SV-based current controller, the proper voltage vector is always chosen out of the three vectors located on the vertexes of the small triangle that $\boldsymbol{e}$ belongs to. Therefore, if the present output voltage vector is $\boldsymbol{v}_1$, shown in Fig. 5.2, it can be regarded that $\boldsymbol{e}$ belongs to the region I or VI. From (5-4) and Fig. 5.6, the plus and minus sign of the current deviation derivative on z-axis $\Delta\boldsymbol{i}_z'$ correspond to the region VI and I, respectively.

One unique feature of the proposed current controller is the simple solution to detect the region of $\boldsymbol{e}$. By using the mapping technique, no accurate calculation for the amplitude and

position of $\boldsymbol{e}$ is needed for the 5L-ANPC converter. Fig. 5.7 shows the mapping method for the voltage vectors and the region of $\boldsymbol{e}$ between the subhexagon of the five-level converter and the hexagon of the two-level converter. The present output voltage vector $\boldsymbol{v}_k$ of the 5L-ANPC converter is mapped to $\boldsymbol{v}_0$ of the two-level converter and the subhexagon which is centered at $\boldsymbol{v}_k$ in the 5-level converter is mapped to the hexagon of the two-level converter.

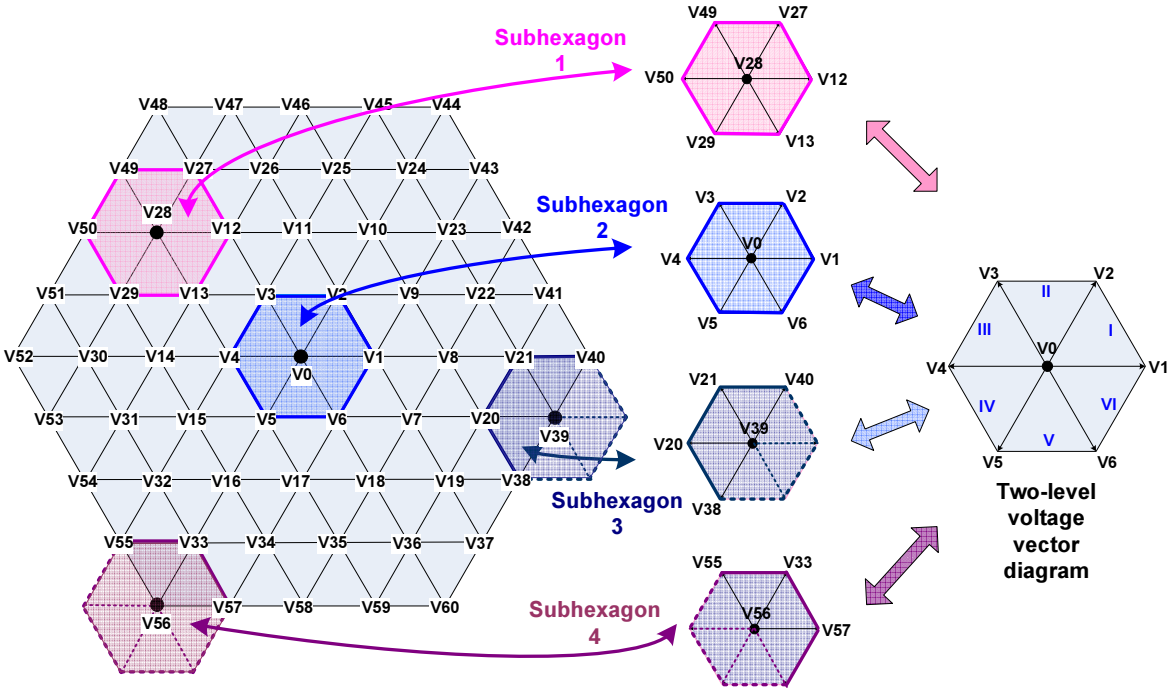


Fig. 5.7 Mapping of the voltage vectors and region of $\boldsymbol{e}$ between five-level and two-level converters

For example, in the 5L-ANPC converter, if the present output voltage vector is $\boldsymbol{v}_{28}$, as shown in Fig. 5.7, then "Subhexagon-1" will be mapped to the hexagon of the two-level converter, where the voltage vectors $\boldsymbol{v}_{28}$, $\boldsymbol{v}_{12}$, $\boldsymbol{v}_{27}$, $\boldsymbol{v}_{49}$, $\boldsymbol{v}_{50}$, $\boldsymbol{v}_{29}$ and $\boldsymbol{v}_{13}$ in the 5L-ANPC converter are mapped to $\boldsymbol{v}_0, \boldsymbol{v}_1, \boldsymbol{v}_2, \boldsymbol{v}_3, \boldsymbol{v}_4, \boldsymbol{v}_5$ and $\boldsymbol{v}_6$ in the two-level converter, respectively. We also notice that when the present voltage vector $\boldsymbol{v}_k$ is on the perimeter of the voltage

vector diagram, which means $\boldsymbol{v}_k$ belongs to $\boldsymbol{v}_{37} \sim \boldsymbol{v}_{60}$, then in order to use the mapping method above, we need to assume a virtual subhexagon, where only 4 or 5 voltage vectors in the virtual subhexagon really exist in the 5L-ANPC converter. For instance, when the present voltage vector is $\boldsymbol{v}_{56}$, "Subhexagon-4" will be selected and mapped to the two-level converter hexagon, where $\boldsymbol{v}_{56}$, $\boldsymbol{v}_{57}$, $\boldsymbol{v}_{33}$ and $\boldsymbol{v}_{55}$ in the 5L-ANPC converter are mapped to $\boldsymbol{v}_0$, $\boldsymbol{v}_1$, $\boldsymbol{v}_2$ and $\boldsymbol{v}_3$ in the two-level converter, respectively. The proposed mapping relation is standard and easy to be derived offline and stored in a lookup table.

Using the mapping technique, a simplified method, as shown in Table 5-4, can be used to detect the region of $\boldsymbol{e}$ for the 5L-ANPC converter. As seen, only the signs of the current deviation derivatives $\Delta \boldsymbol{i}_x'$, $\Delta \boldsymbol{i}_y'$ and $\Delta \boldsymbol{i}_z'$ are needed. Since the present output voltage vector $\boldsymbol{v}_k$ in the 5L-ANPC converter is always mapped to $\boldsymbol{v}_0$ in the two-level converter, in the lookup table for the region detection of $\boldsymbol{e}$ of the two-level converter in [115], we only need to consider the case $\boldsymbol{v}_k = \boldsymbol{v}_0$.

Table 5-4 Region detection of $\boldsymbol{e}$ for the 5L-ANPC converter

$\Delta \boldsymbol{i}_x'$	$\Delta \boldsymbol{i}_y'$	$\Delta \boldsymbol{i}_z'$	Region of $\boldsymbol{e}$
1	0	0	I
1	1	0	II
0	1	0	III
0	1	1	IV
0	0	1	V
1	0	1	VI

An example is illustrated here. If the present output voltage vector of the 5-level ANPC converter is $\boldsymbol{v}_{28}$, since the selected voltage vector is always from the three vectors located on the vertexes of the sector including $\boldsymbol{e}$, it can be regarded that $\boldsymbol{e}$ belongs to one of the 6

triangles in the “Subhexagon-1”. After mapping “Subhexagon-1” to the two-level converter hexagon, “+”, “+” and “-“ signs of the current deviation derivatives on the *x*-*y*-z axes respectively will detect that $\boldsymbol{e}$ is in region II, which corresponds to the sector formed by $\boldsymbol{v}_{28}, \boldsymbol{v}_{27}$ and $\boldsymbol{v}_{49}$ in the 5L-ANPC converter, as shown in Fig. 5.7.

After knowing the region of $\boldsymbol{e}$, we can find the proper voltage vector to suppress harmonic current content in steady state for the converter by using Table 5-3, which is the same as the table for the two-level converter. However, the selected voltage vector from Table 5-3 belongs to $\boldsymbol{v}_0 \sim \boldsymbol{v}_6$ in the two-level converter, so it needs to be reversely mapped to the 5L-ANPC converter to get the corresponding output voltage vector. The reverse mapping is similar to the mapping process, and it is easy to be implemented according to Fig. 5.7.

Following the previous example, since $\boldsymbol{e}$ is in region II after mapped to the two-level converter, then according to Table 5-3, if $\boldsymbol{\Delta i}$ is detected in region 3, then $\boldsymbol{v}_3$ is selected in the two-level converter. Using the reverse mapping, as shown in Fig. 5.7, the real output voltage vector is $\boldsymbol{v}_{49}$ in “Subhexagon-1” of the 5L-ANPC converter. Finally $\boldsymbol{v}_{49}$ will be selected to suppress harmonic current content in steady state.

We also notice that when the present voltage vector $\boldsymbol{v}_k$ belongs to $\boldsymbol{v}_{37} \sim \boldsymbol{v}_{60}$, the number of the possible region of $\boldsymbol{e}$ is limited. For example, if $\boldsymbol{v}_k = \boldsymbol{v}_{39}$, then $\boldsymbol{e}$ is only possible to exist in the region II, III or IV after mapped to the two-level converter. Therefore, in this case, only part of Table 5-3 and Table 5-4 will be used to select the output voltage vector, and the virtual voltage vectors will not be chosen. This indicates that the hypothetical virtual subhexagon will not affect the correctness of the proposed current controller.

5.3.3 Voltage Vector Selection to Obtain Fast Current Response in Transient State

To obtain fast current response in transient state, the voltage vector, whose corresponding $d\Delta \boldsymbol{i}/dt$ has the largest opposite direction component to $\Delta \boldsymbol{i}$, should be selected. For example, in a 5L-ANPC converter, if $\Delta \boldsymbol{i}$ is in region 1, then $\boldsymbol{v}_{40}$ is chosen, as shown in Fig. 5.6.

Table 5-5 shows the method to select the output voltage vector of the 5L-ANPC converter in transient state. As seen, the only needed information is the region of $\Delta \boldsymbol{i}$, while the mapping technique is not required in this mode. The region of $\Delta \boldsymbol{i}$ can be detected according to Table 5-2.

Table 5-5 Region of $\Delta \boldsymbol{i}$ and the selected $\boldsymbol{v}_k$ in transient state

Region of $\Delta \boldsymbol{i}$	$\boldsymbol{v}_k$
1	V_{40}
2	V_{44}
3	V_{48}
4	V_{52}
5	V_{56}
6	V_{60}

5.3.4 Operation Mode Selection of the Current Controller

The operation mode of the proposed current controller is determined based on two hexagons “m” and “h” with a presetting window size, as shown in Fig. 5.8. When $\Delta \boldsymbol{i}$ is out of the hexagon of “h”, the transient state mode will be selected. If $\Delta \boldsymbol{i}$ is within the hexagon of “m”, the present voltage vector $\boldsymbol{v}_k$ is kept and no switching actions occur. Otherwise, the steady state mode is selected. The window size of the hexagon “m” can be set as a constant

value, or be adaptively controlled to achieve constant average switching frequency [115]. In this work, we set the window size as a constant for simplicity.

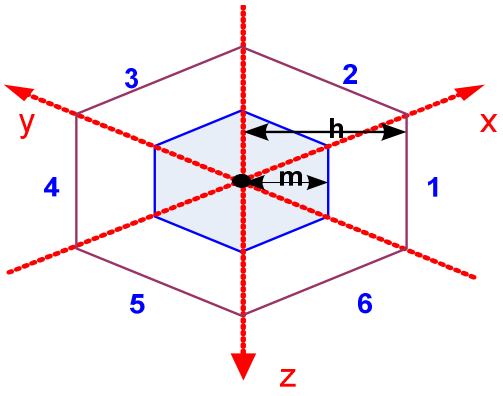


Fig. 5.8 Operation mode selection for the current controller

5.3.5 Floating Capacitor Voltage Balance

For a three-phase five-level ANPC converter, there are 61 voltage vectors, and some of them have redundant switching states. The complete voltage vector diagram with all the redundant switching states is drawn in Fig. 5.9. Moreover, there are also additional redundant switching states for the output voltage in each phase of the converter. As shown in Table 5-1, two redundant switching states exist for each of the output phase voltage $\pm V_{dc}/2$ and 0. All these redundant switching states greatly increase the control flexibility of the five-level ANPC converter, such as the control of the neutral-point voltage of the dc-link and the floating capacitor voltage.

In [118], the method for selecting the redundant switching states of a five-level converter has been proposed to regulate the neutral-point voltage of the dc-link and the floating capacitor voltage. This method requires considerable effort and extensive memory space to store the large amount of data and lookup tables. However, in this work, we only focus on the

floating capacitor voltage control, since we assume the front-end active rectifier, such as the three-level NPC rectifier, can implement the dc-link neutral-point voltage balance control, which allows a great simplification for the control of the 5L-ANPC converter. Moreover, the redundant switching states can also contribute to the device power losses balance.

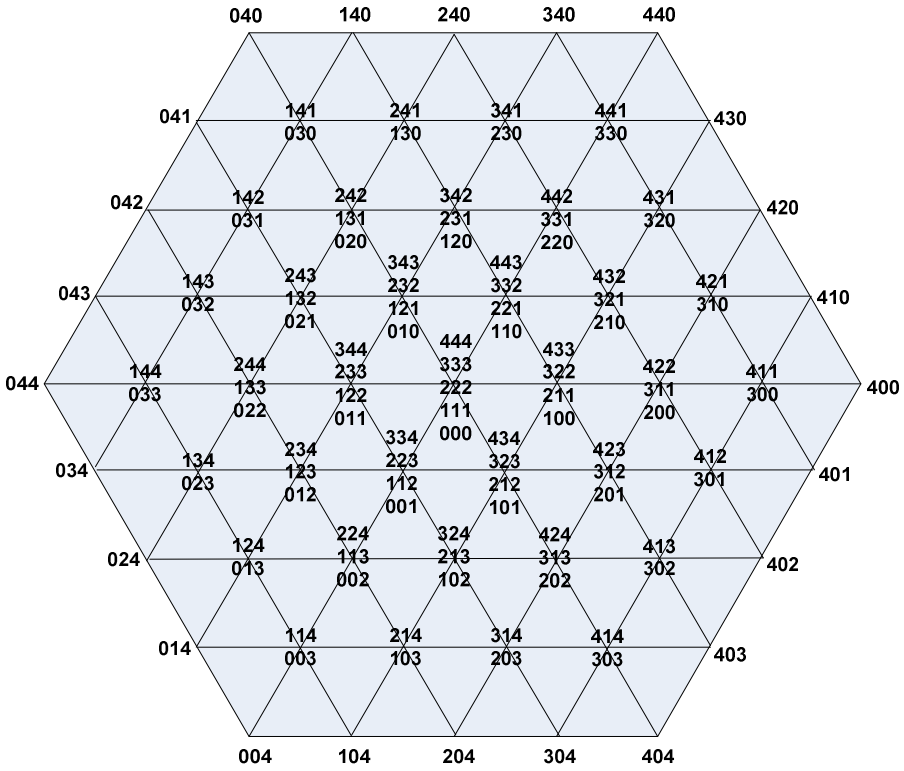


Fig. 5.9 Complete redundant switching states of a three-phase 5L-ANPC converter

For example, when $\boldsymbol{v}_{21}$ is finally selected in the 5L-ANPC converter after the reverse mapping, the impact of its redundant switching states on the floating capacitor voltage in each phase is listed in Table 5-6. In the table, “n/a”, “+” and “-” represent no impact, charge and discharge for the floating capacitor voltage, respectively.

Table 5-6 Impact of the redundant switching states (RSS) of $\boldsymbol{v}_{21}$ for the floating capacitor voltage

	RSS	3-phase state	Phase state			Vcf_a		Vcf_b		Vcf_c	
			a	b	c	Ia>0	Ia<0	Ib>0	Ib<0	Ic>0	Ic<0
$\boldsymbol{v}_{21}$	1	(4 1 1)	V1	V6	V6	n/a	n/a	+	-	+	-
	2		V1	V6	V7	n/a	n/a	+	-	-	+
	3		V1	V7	V6	n/a	n/a	-	+	+	-
	4		V1	V7	V7	n/a	n/a	-	+	-	+
	5	(3 0 0)	V2	V8	V8	+	-	n/a	n/a	n/a	n/a
	6		V3	V8	V8	-	+	n/a	n/a	n/a	n/a

Table 5-6 shows that, to generate $\boldsymbol{v}_{21}$, there are totally 6 choices by considering both the three-phase switching state redundancy and the switching state redundancy in each phase of the converter. These redundancies may impact the voltage of the three floating capacitors in different ways, and can be used to control their voltage balance. In case all the three floating capacitor voltages can not be regulated simultaneously by the same switching state, the capacitor prioritization scheme, which is similar as that in Chapter 4, can be used so that the selected switching state is able to control the more deviated (higher priority) capacitor first to assure the proper operation of the converter [119]. One example is explained below.

- If the voltage deviation of the floating capacitor in phase A (C_{f_a}) is larger than the other two floating capacitors in phase B and phase C (C_{f_b} C_{f_c}), then C_{f_a} has higher priority. Therefore only the three-phase switching state (3 0 0) will be used. One of the two redundant switching states for (3 0 0) can be selected as follows.
    - When C_{f_a} needs charged, if I_a>0 (output current flows out of the AC terminal of phase A), then the RSS "5" is selected. On the contrary, if I_a<0, then RSS "6" should be selected.

- When C_{f_a} needs discharged, if $I_a>0$, then the RSS "6" is selected. On the contrary, if $I_a<0$, then RSS "5" should be selected.

- If the largest voltage deviation of the floating capacitors occurs in phase B or phase C, then C_{f_b} or C_{f_c} has higher priority. Thus only the three-phase switching state (4 1 1) will be used. One of the four redundant switching states for (4 1 1) can be selected according to Table 5-7. In the table, for the status of the floating capacitors, "+" and "-" mean the capacitor needs charged and discharged, respectively. For the current direction, "+" and "-" represent the current flows out of and into the phase AC terminal, respectively.

Table 5-7 Switching state selection for three-phase state (4 1 1) when C_{f_b} or C_{f_c} has higher priority

3-phase state	Status of C_{f_b}		+	+	-	-
	Status of C_{f_c}		+	-	+	-
(4 1 1)	Direction of I_b	Direction of I_c	RSS			
	+	+	1	2	3	4
	+	-	2	1	4	3
	-	+	3	4	1	2
	-	-	4	3	2	1

Besides the floating capacitor voltage control, the redundant switching states can help to balance the device power losses. For example, in Table 5-1, V4 and V5 can generate the same output phase voltage 0, and they have no impact on floating capacitor voltage. However, they allow the current to flow through different conduction paths, which means we can actively control the current path so as to balance the device power losses. Taking one phase with positive current as an example, V4 allows the current flowing through and correspondingly causing conduction loss on S_6, S_3 and S_1, as shown in Fig. 5.10 (a).

Otherwise, V5 conducts the current through S_7, S_4 and S_2, and cause conduction losses within them, as shown in Fig. 5.10 (b). This means when the output phase voltage is required to be 0, we can choose either V4 or V5 to actively balance the device power losses.

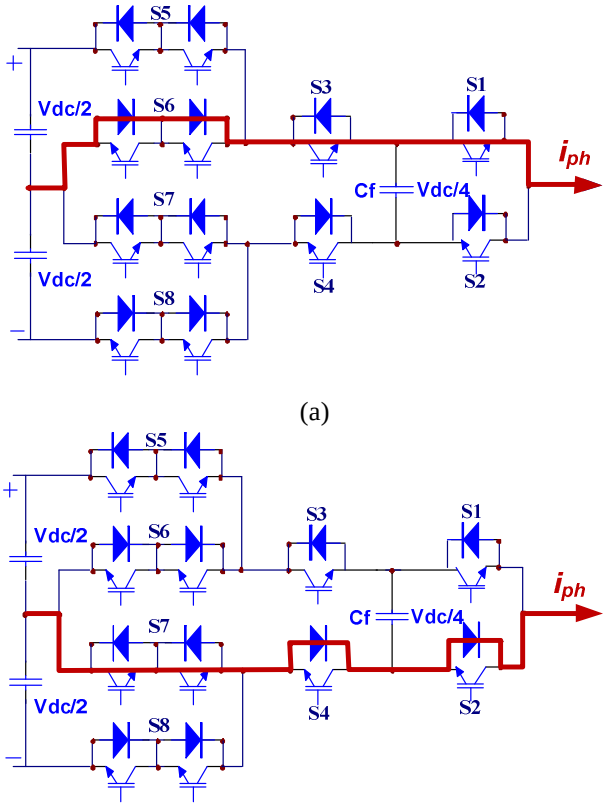


Fig. 5.10 The conduction path for the positive current when the output phase voltage is 0 (a) V4 is selected (b) V5 is selected

5.3.6 Procedures of the Proposed Current Controller for Any General N-Level Converter

As discussed above, the proposed current controller does not require the calculation of the back EMF voltage, and the controller complexity is greatly simplify due to the used of the very simple lookup tables, thus it can be easily applied for any general N-level converter. The generalized procedures of the proposed current controller are summarized below.

1. Measure and sample the instantaneous three phase currents and calculate the current deviation in the "*a*-*b*-*c*" coordinates $\Delta \boldsymbol{i}_a$, $\Delta \boldsymbol{i}_b$ and $\Delta \boldsymbol{i}_c$;
2. Use the mapping technique to detect the region of the current deviation vector $\Delta \boldsymbol{i}$ according to Table 5-2;
3. Compare the current deviation vector $\Delta \boldsymbol{i}$ with the window size of the two hexagons "m" and "h" to determine the current controller operation mode, and then:
   a) If $|\Delta \boldsymbol{i}| < m$, keep the present output voltage vector $\boldsymbol{v}_k$.
   b) If $|\Delta \boldsymbol{i}| > h$, choose the voltage vector according to Table 5-5 to obtain fast current response in transient state.
   c) Or else, choose the voltage vector to suppress harmonic current content in steady state by following the steps below.
      1) Calculate the current deviation derivatives in the "*x*-*y*-z" coordinates $\Delta \boldsymbol{i}_x'$, $\Delta \boldsymbol{i}_y'$ and $\Delta \boldsymbol{i}_z'$, and determine the region of $\boldsymbol{e}$ according to Table 5-4.
      2) Using the mapping and reverse mapping techniques, together with the pre-stored lookup tables which include the corresponding relation between the subhexagon of the N-level converter (with the present $\boldsymbol{v}_k$ at the center) and the hexagon of the two-level converter, select the proper voltage vector according to Table 5-3.
      3) If the selected voltage vector in the N-level converter has redundant switching states, choose the proper one according to the specific control requirements,

such as floating capacitor voltage control and device power losses balance according to the similar method shown in Table 5-7 and Fig. 5.10.

The procedures flow chart diagram of the proposed current controller for any general N-level converter is given below:

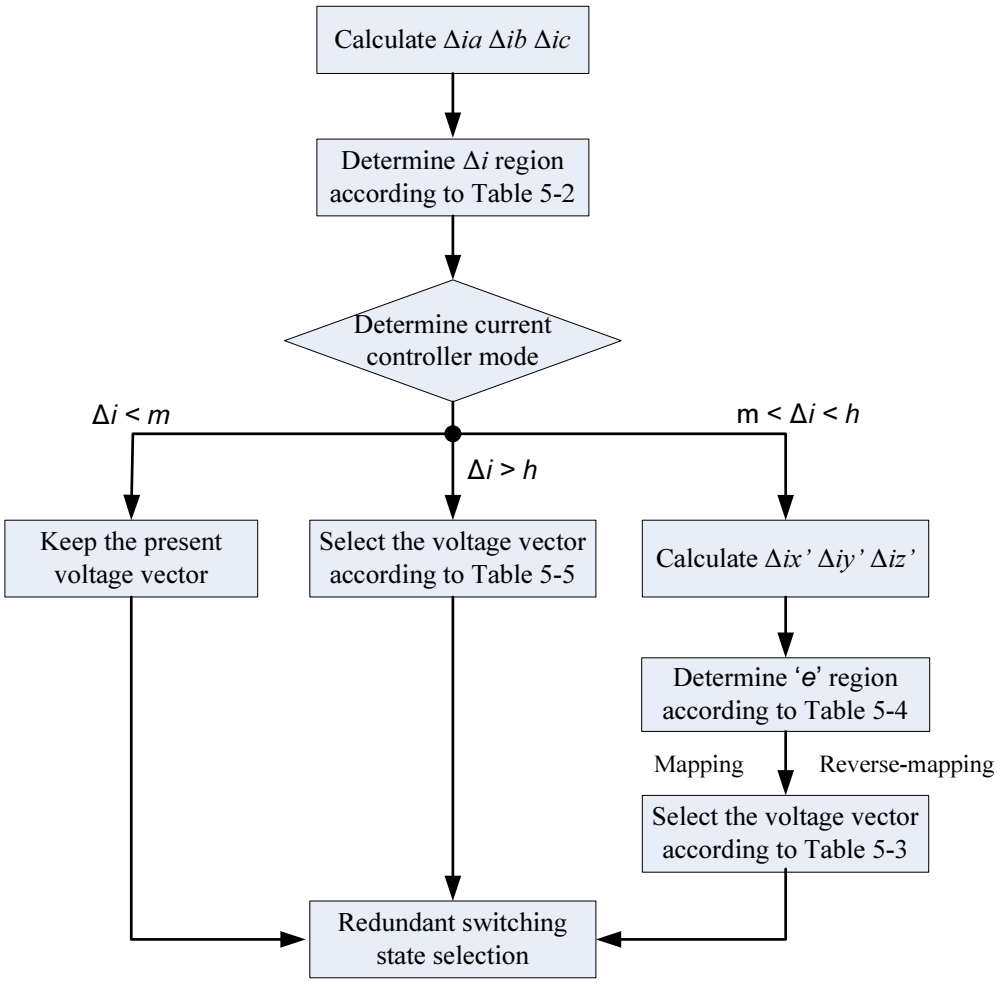


Fig. 5.11 Procedure flow chart of the proposed current controller for any general N-level converter

5.4 Simulation Verification

The proposed current controller is implemented in a 5L-ANPC converter based vector-controlled motor drive system in MATLAB/Simulink for verification. Fig. 5.12 shows the

system configuration. The main system parameters are listed in Table 5-8. The dc-link is modeled by two constant 350 VDC voltage sources since we assume that the dc-link voltage and neutral-point voltage balance are controlled by the frond-end active rectifier unit.

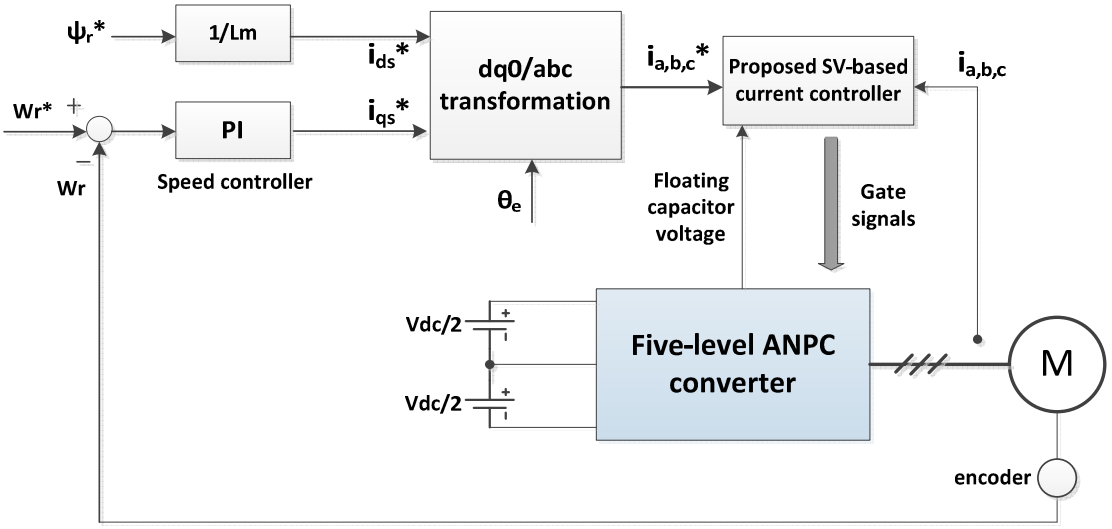


Fig. 5.12 Configuration of the simulation system

Table 5-8 Main system parameters

Total DC bus voltage V_{dc}		700V
Floating capacitor C_f		1mF
Induction motor data	Nominal power, voltage and frequency	50HP, 460V, 60Hz
	Stator resistance and inductance	0.087 Ω, 0.8mH
	rotor resistance and inductance	0.228 Ω, 0.8mH
	Mutual induction (Lm)	34.7mH
	Inertia, friction factor and pole pairs	1.662 (kg.m^2), 0.1 (N.m.s), 2

5.4.1 Steady State Operation Mode Validation

In the simulation for steady state operation mode, the motor speed reference is 160 rad/s, and the load torque is 180 N.m. In this simulation, the window size of the hexagon “m” is set to be 3A. Fig. 5.13 shows the reference phase current, the actual phase current, the output

line-to-line voltage, and the floating capacitor voltages of the converter from top to bottom. Fig. 5.14 shows the RMS current error calculated by:

$$i_{\_error} = \sqrt{\left(i_a^* - i_a\right)^2 + \left(i_b^* - i_b\right)^2 + \left(i_c^* - i_c\right)^2} \quad \textbf{(5-7)}$$

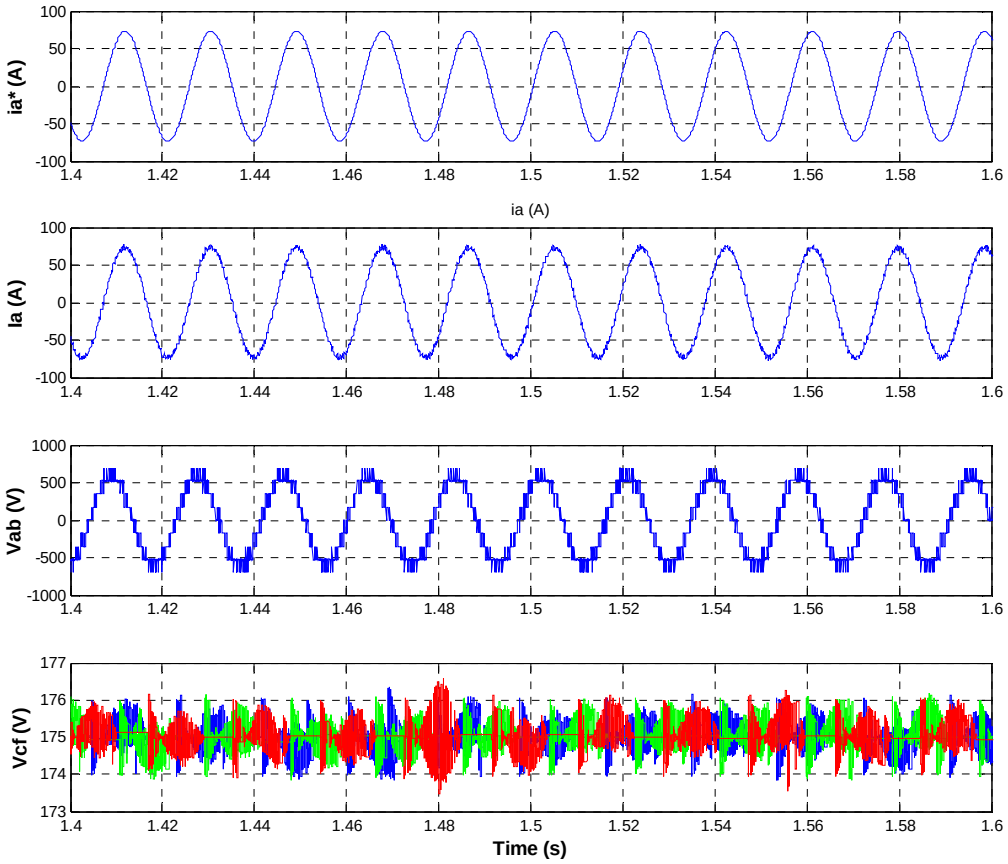


Fig. 5.13 Waveforms in steady state, from top to bottom: stator reference current, stator actual current, line-to-line voltage, and three-phase floating capacitor voltages

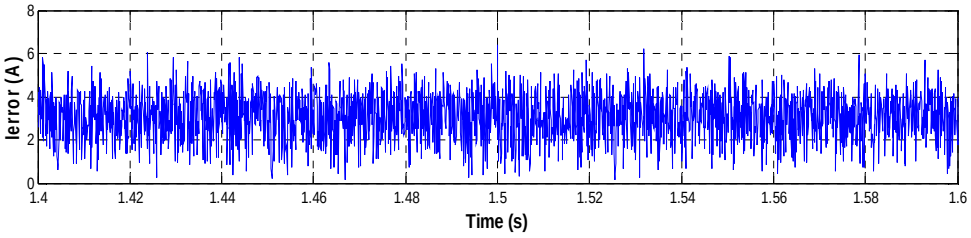


Fig. 5.14 RMS current error in steady state

5.4.2 Transient State Operation Mode Validation

In the simulation for transient state operation mode, the load torque is 0. The motor speed reference has a step change from 80 rad/s to 160 rad/s at 1.5s, and then back to 80 rad/s at 1.9s. In this simulation, the window size of the hexagon "h" is set to be 9A. Fig. 5.15 shows the reference and actual motor speed, the reference phase current, the actual phase current, the output line-to-line voltage, and the floating capacitor voltages of the converter from top to bottom. Fig. 5.16 shows the RMS current error.

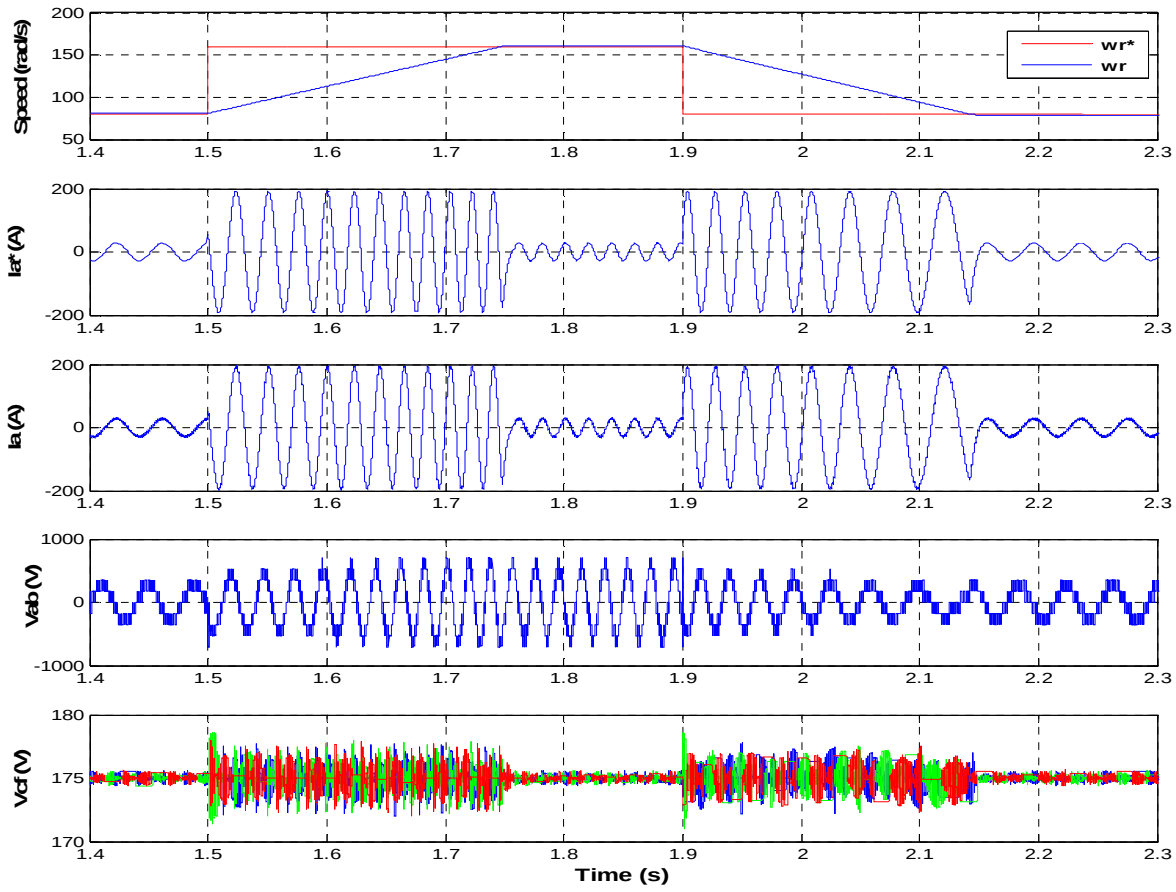


Fig. 5.15 Waveforms in transient state, from top to bottom: reference and actual motor speed, stator reference current, stator actual current, line-to-line voltage, and three-phase floating capacitor voltages

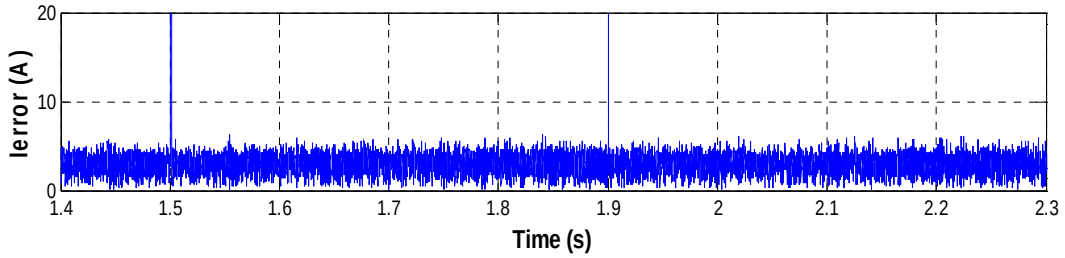


Fig. 5.16 RMS current error in transient state

From the simulation results above, we can see that the proposed current controller can achieve good current tracking performance in steady state, and RMS current error is small. The results also show fast current response for transient state when there is sudden reference current change. Moreover, the floating capacitor voltages are well-controlled by using the redundant switching states.

5.5 Summary

In this paper, a simplified space vector based current controller for any general N-level converter is proposed to suppress current harmonic content in steady state and achieve fast current response in transient state. Using the presented mapping technique, the subhexagon of the N-level converter can be mapped to the hexagon of the two-level converter. Thus, according to the principles of the SV-based current controller for the two-level converter, the proper output voltage vector of the N-level converter can be identified after the reverse mapping. Moreover, due to the existence of the redundant switching states in the N-level converter, the optimum switching state and switching sequence can be selected to meet the specific control requirements, such as balancing the device power loss distribution, regulating the floating capacitor voltage and so on.

Compared with the previous works on the SV-based current controller for multilevel converters, the proposed current controller does not require the calculation of the back EMF voltage of the load, and the controller implementation is greatly simplified due to the use of very simple lookup tables, therefore it can be easily extended to any general N-level converter. The generalized procedures of the current controller for any N-level converter are summarized. The proposed current controller is explained and simulated in a five-level ANPC converter for the motor drive system. The simulation results prove the correctness of the proposed current controller.

Chapter 6 Conclusions and Future Work

6.1 Conclusions

In this research work, major contributions have been made in investigating the design, topology, control and characteristics of multilevel active NPC converters for high power applications, like large wind turbine systems and motor drive systems. The contributions and achievements of this dissertation are summarized as follows.

1. The concept of the ETO Light NPC and ANPC PEBBs is proposed, which are stand-alone units and can easily be converted into different converter topologies and applied for different applications. The electrical design, the component physical arrangement, and the methodologies for the power loss and thermal analysis of the ETO Light PEBBs are developed. The detailed power loss analytical equations are derived, and the electrical-equivalent thermal network models are constructed for both the ETO Light NPC and ANPC PEBBs. The thermal performance of the proposed two ETO Light PEBBs is studied and compared for generator operation mode and motor operation mode, respectively.
2. The application of the ETO Light PEBBs in large wind turbine systems is proposed. The configurations of the ETO Light wind power converters are identified for the wind turbine systems with AC and DC transmission, respectively. The thermal performance of the ETO Light NPC and ANPC PEBB is studied for a 5 MW and a 7 MW wind turbine system, respectively.

3. The operation of the 3L-ANPC converter is analyzed for single device open and short failure conditions, respectively. To enable the continuous operating under device failure condition, the fault tolerant ability and the fault tolerant control strategies of the 3L-ANPC converter are proposed. The requirement of the fault detection time is discussed. By using the proposed control schemes, the 3L-ANPC converter can still generate three-phase symmetrical and stable output currents and keep the neutral-point voltage of the dc-link balanced. However, the maximum modulation index of the converter has to be reduced for some device failure conditions. Furthermore, the operation of the 3L-ANPC converter under multiple device failure conditions is investigated. The results show that the proposed fault tolerant control allows the continuous operating of the converter even if multiple devices fail simultaneously. Therefore, the reliability and survivability of the 3L-ANPC converter are greatly improved. Simulation and experiment results validate the proposed methods.
4. In order to compare the reliability of the 3L-NPC converter and the 3L-ANPC converter, the fault tolerant operation of the 3L-NPC converter is analyzed and summarized. The method for assessing the converter reliability is discussed. A comprehensive reliability comparison is investigated for the 3L-NPC converter and the 3L-ANPC converter. The results show that the 3L-ANPC converter has higher reliability than the 3L-NPC converter for motor drive applications, in which the reduction of the maximum modulation index is usually allowed during fault operation, and the motor drive system can continue working, but at a lower speed or lower output power. For grid-connected applications, in which the reduction of the

maximum modulation index is not allowed since the converter output is connected to the grid with a fixed voltage, the reliability of the 3L-ANPC converter is almost the same as that of the 3L-NPC converter for single and multiple device open failure. However, for single and multiple device short failure, the 3L-NPC converter has higher reliability than the 3L-ANPC converter.

5. The 3L-ANPC converter is proposed to be applied on the generator side of a direct-driven PMSG based large wind turbine system. Besides the feature of the balanced loss distribution among the devices, the fault tolerant capability of the 3L-ANPC converter also allows the wind turbine to remain in service and continue providing real power under device failure conditions. The control schemes are proposed for the 3L-ANPC generator converter under normal operation and device failure operation. Under fault operation, depending on the position and failure type of the failed device and the wind speed, the wind turbine will work at either MPPT control mode or constant rotor speed control mode. The purpose of the proposed control schemes is to extract the maximum power from wind under the current system operating condition. Moreover, the option to increase the DC bus voltage of the converter is also discussed to extract more power at higher wind speed under device failure conditions. The simulation results verify the proposed control strategies and the proper operation of a 5 MW wind turbine system.
6. A new 9-level ANPC converter, referred to as the 5L-ANPC plus HBBB converter, is proposed for the next generation PEBB technology for high power applications. The topology, operating principle and control, as well as the floating capacitor voltage

balance scheme, are presented in detail. The main features of the proposed 9-level ANPC converter are identified. The hybrid converter concept, in which different types of power devices are employed, is discussed for the proposed topology.

7. To illustrate the benefits of the new 9-level ANPC topology, it is compared with other conventional 9-level converters and existing 9-level ANPC converters from several aspects, including the number of individual semiconductor devices, the total switch blocking voltage, the selection from commercial power device products, the floating capacitors number, voltage rating and the total stored energy, and the limitation of the maximum modulation index at full active power transfer. The results show that proposed converter shows better overall performance among all the 9-level converters.
8. The proposed 9-level ANPC converter is applied on the grid side of a 6 MW wind turbine system to achieve a filterless grid connection. The system configuration and control scheme are presented. The simulation results prove that the proposed system configuration fulfills the harmonic limit requirement of the utility standards even without using the grid passive filter.
9. A simplified space vector based current controller for any general N-level converter is proposed. Using the presented mapping technique, the subhexagon of the N-level converter can be mapped to the hexagon of the conventional two-level converter, and an appropriate voltage vector can be selected to suppress current harmonic content in steady state and achieve fast current response in transient state. Moreover, due to the existence of the redundant switching states in the N-level converter, the optimum switching state and switching sequence can be selected to meet the specific control

requirements, such as balancing the device power loss distribution and regulating the floating capacitor voltage. The proposed SV-based current controller does not require the calculation of the back EMF voltage of load, and the controller complexity is greatly simplified due to the use of very simple lookup tables, thus it can be easily extended to any general N-level converter. The generalized procedures of the current controller for any N-level converter are summarized. The proposed current controller is explained and verified by simulation on a five-level ANPC converter in the motor drive system.

6.2 Future Work

To make this research more comprehensive, the following work can be continued in the future.

1. The long term thermal testing of the ETO Light Stacks and the ETO Light PEBBs at the nominal operating point can be implemented. Then, based on the actual experiment measurement data, the electrical design and the component physical arrangement can be further evaluated. The thermal performance of the ETO Light PEBBs can be further analyzed and investigated, and the accuracy of the thermal model in Chapter 2 can be improved.
2. The analysis of the large-signal and the small-signal modeling of the 3L-ANPC converter should be studied in the future. The modeling of the 3L-ANPC converter under normal operating condition is almost the same as that of the 3L-NPC converter, which has already been reported by researchers. However, the modeling of the 3L-

ANPC converter under fault tolerant operation has not bee studied yet, and it is very important for the controller design of the 3L-ANPC converter. The optimal control parameters, like the PI parameters, should be designed for the normal operation and the fault tolerant operation separately, so as to achieve better converter and system performance. Moreover, the fault tolerant ability and the control strategies of the 3L-ANPC converter can be further investigated for the motor drive systems and various load conditions, such as unbalance load and non-linear load.

3. For the simplified space vector based current controller, the constant average switching frequency control for the multilevel converters with a higher number of voltage levels can be further studied.

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