ABSTRACT

XI, ZHENGPING. Control Strategies of STATCOM during System Faults. (Under the direction of Dr. Subhashish Bhattacharya.)

The possibility of generating or absorbing controllable reactive power with various power electronic switching converters has long been recognized. Alternating Current Transmission Systems (FACTS) controller is the key element for flexible, controllable, and secure transforming transmission and distribution (T&D) system. Advances in power electronics technologies, such as the gate-turn-off thyristors (GTOs), modular voltage source converter (VSC) technology and digital control technology, promote the implementation of these new electronic concepts in transmission systems.

This dissertation is dedicated to a comprehensive study of multilevel voltage source converter based STATCOM and its application, especially its operation during system fault. To solve STATCOM operation problem during system faults, “Emergency PWM” is proposed. When a system fault is detected, “Emergency PWM” (EPWM) is implemented with angle control until the fault is removed. By this way, the switches are working in the 60Hz during normal time; there is no extra system loss. EPWM can prevent over-current and trips in the VSC during and after system fault, and ensures that the STATCOM supplies required reactive power.

Based on normal three-phase PLL, “Instantaneous PLL” (IPLL) is proposed. By using the voltage vector angle as the output of PLL, IPLL considers not only positive sequence, but also negative sequence, which is generated by system faults. System with IPLL has the same performance as system with normal PLL, and the system performance is

improved by IPLL during system faults. It means a system can implement normal PLL for normal operation, and switch to IPLL at the fault.

Ice accumulated on power transmission lines in winter can cause severe damage to power system. VSC based STATCOM provides good asset utilization during the majority of the time when ice-melting is not required. By changing *Iq* reference under *Iq* regulation, fiving fixed angle for angle control to keep charging DC capacitors and changing DC voltage according the demanded DC current through transmission conductors, the STATCOM can perform the ice melting function when it is needed. The incremental cost for ice-melting capability is relatively small. The changeover procedure is simple and can be accomplished by remote control.

The integration and control of energy storage systems (ESSs), such as Supercapacitor (Ultracapacitor - UCAP) into a D-STATCOM (Distribution system STATCOM) is developed to enhance power quality and improve distribution system reliability. This dissertation develops the control concepts to charge/discharge the UCAP by the D-STATCOM, and validate the performance of an integrated D-STATCOM/UCAP system for improving distribution system performance under all types of system related disturbances.

Control Strategies of STATCOM during System Faults

by
Zhengping Xi

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APPROVED BY:

Dr. Subhashish Bhattacharya Chair of Advisory Committee	Dr. Alex Q. Huang
Dr. Mesut E. Baran	Dr. Arkady Kheyfets

DEDICATION

To my parents

Shaohuang Xi & Zhaozheng Chen

BIOGRAPHY

The author, Zhengping Xi, was born in Beijing, China. She received her Bachelor degree in Automation from Tshinghua University, Beijing, China, in 2000 and Master degree in Electrical Engineering from Chinese Academy of China, in 2003. She was doing research in Sliding Mode control in Nottingham University, UK, from 2003 to 2005.

In 2006, she joined the Semiconductor Power Electronics Center (SPEC) and the National Science Foundation's Engineering Research Center Future Renewable Electric Energy Delivery and Management (FREEDM) system in the Department of Electrical and Computer Engineering at North Carolina State University (NCSU) as a graduate research assistant to pursue her PhD degree.

Her research interests are power electronic converters modeling and control, power electronics applications in power systems, energy storage system, and power system simulation.

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CHAPTER 1 INTRODUCTION

1.1 Overview

The possibility of generating or absorbing controllable reactive power with various power electronic switching converters has long been recognized [1]-[8]. However the practical implementation of these concepts for transmission line applications was not possible without suitable high-power electronic switches, having the inherent capability to turn off in response to a gating command. Flexible Alternating Current Transmission Systems (FACTS) controller, an AC transmission system incorporating power electronic-based or other static controllers which provide better power flow control and enhanced dynamic stability by control of one or more AC transmission system parameters (voltage, phase angle and impedance), is the key element for flexible, controllable, and secure transforming transmission and distribution (T&D) system.

Advances in power electronics technologies, such as the gate-turn-off thyristors (GTOs), modular voltage source converter (VSC) technology and digital control technology, promote the implementation of these new electronic concepts in transmission systems. The development of such an advanced power electronics-based transmission controller to solve typical and challenging system issues, such as ice-melt problem, would improve the implement of this controller [11].

1.2 Shunt-connected Controllers and STATCOM

In general, FACTS controllers can be divided into three categories [2]

- In series with the power system (series compensation),
- In shunt with the power system (shunt compensation),
- Both in series and in shunt with the power system.

Among FACTS controllers, the shunt-connected controllers have shown feasibility in term of cost effectiveness in a wide range of problem-solving from transmission to distribution levels. Moreover, the shunt controller can improve transient stability and can damp power oscillation during a post-fault event. Using a high-speed power converter, the shunt controller can further alleviate or even cancel the flicker problem [10].

In principle, all shunt controllers inject current into the system at the point of connection. A variable shunt impedance connected to the line voltage causes a variable current flow and hence represents injection of current into the line. As long as the injected current is in phase quadrature with the line voltage, the shunt controller only supplies or consumes variable reactive power [2].

The shunt controller basically consists of three groups:

- Static var compensator (SVC)
- Static synchronous compensator (STATCOM)
- Static synchronous generator (SSG) or STATCOM with energy-storage system (ESS)

Switching power converters have been able to operate at high switching frequencies and to provide a faster response by employing turn-off-capability semiconductor devices. This makes the voltage source converter (VSC) an important part in the FACTS controller [3].

STATCOM is the first power-converter-based shunt-connected controller, which has broad applications in electric utility industry. The STATCOM is the solid-state-based power converter version of the Static Var Compensator (SVC). The concept of the STATCOM was proposed by Gyugyi in 1976 [2]. STATCOM has played an important role in power industry since 1980 [12]. Operating as a shunt-connected SVC, the real and reactive power exchange between the STATCOM and the transmission network line is produced by a controllable AC voltage source generated by a voltage source converter. The first high-power STATCOM in the United State was installed at the Tennessee Valley Authority (TVA) Sullivan Substation in 1995. The ±100MVA STATCOM is used to regulate the 161kV bus voltage during the daily load buildup, with a 48-pulse power converter consists of eight two-level VSCs, controlled in a 60Hz staircase [13]-[14].

Compared with conventional FACTS, SVC, STATCOM has many advantages with its natures [2][15][16]:

- V-I and V-Q characteristics: STATCOM can be operated over its full output current range even at very low system voltage levels. In other words, the maximum capacitive or inductive output current of the STATCOM can be maintained independently of the AC system voltage, and the maximum Var generation or absorption changes linearly with the AC system voltage. Reversely, the maximum attainable compensating current of SVC decreases linearly with ac system voltage, and the maximum var output decreases with the square of this voltage. The STATCOM is superior to the SVC in providing voltage support under large system disturbances during which the voltage excursions would be

well outside of the linear operating range of the compensator. The capability of providing maximum compensating current at reduced system voltage enables the STATCOM to perform in a variety of applications the same dynamic compensation as an SVC of considerably higher rating.

- Transient stability: The ability of the STATCOM to maintain full capacitive output current at low system voltage makes it more effective than the SVC in improving the transient stability. The transmittable power can be increased if the shunt compensation is provided by a STATCOM rather than by an SVC.

- Response time: SVC includes TCR (thyristor controlled reactor), which per-phase can be controlled per half cycle through changing the firing angle, and TSC (thyristor switched capacitor), which needs a full cycle to upgrade for a transient-free switching. With the semiconductor device having turn-off capability and VSC technology, STATCOM can update its control at least within half-cycle with line switching frequency.

- Capability to exchange real power: STATCOM, in contrast to SVC, has the unique capability to interface with an energy storage system, exchange real power with the power network in bi-directions, and independently control both reactive power and real power.

- Harmonics: With the innovation of VSC topologies and fast switching semiconductor devices and modulation methods, the harmonics emission of STATCOM is very low and a filter is not required.

- Loss vs. Var output characteristic: Both STATCOM and SVC have relatively low loss nearby zero Var output. The loss contribution of power semiconductors and related components to the total compensator losses are higher for the STATCOM than for the SVC. However, the rapid semiconductor developments will reduce the device losses, and the technological advances probably will have help to reduce the overall losses of the STATCOM more than those of the SVC.

- Physical size and installation: With high power density of semiconductor devices and VSC capability to circulate reactive power, STATCOM does not need large capacitor and reactor banks, which are used in conventional SVCs. Thus, overall size is significantly reduced (about 30～40%) for STATCOM.

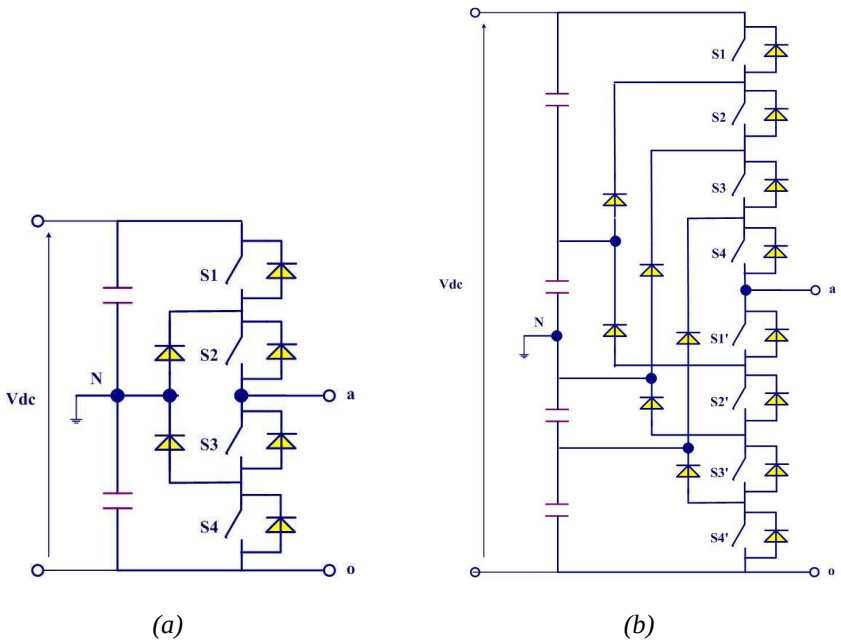
- Lifetime: Compared to a typical life of thousands operation times for mechanical breakers or switches, a semiconductor device has almost infinite switching cycles. With less passive components, STATCOM has an even longer lifetime than SVC. With fast development and improvement of semiconductor devices, the lifetime of STATCOM is expected to be improved further.

1.3 Multilevel Converter Topology

Due to MVA level of STATCOM implement, high power voltage source converter is needed in most cases where conventional two-level converters without device series connection cannot handle. Multilevel converters are currently considered as one of the industrial solution for high dynamic performance and power-quality demanding applications. The multilevel

converters typically synthesize the staircase voltage wave from several levels of dc capacitor voltages, covering a power range from 1 to 30MW [17].

Over the years, many different multilevel converter topologies have been reported. The most known and established topologies are the diode clamped (neutral point clamped) multilevel converter; the capacitor clamped (flying capacitor) multilevel converter, and the cascaded H-bridge multilevel converter.



(a) *(b)*

Figure 1-1 Diode clamped multilevel converter topologies (a) Three-level (b) Five-level

The phase A of a three-level diode clamped converter is shown in Figure 1-1 (a) in which the dc bus consists of two capacitors. The negative bar of the upper converter and the positive bar of the lower one are joined together to form the new phase output, while the original phase outputs are connected via two clamping diodes to form the neutral point *N*, dividing the DC-link voltage in two. Each device voltage stress will be limited to one

capacitor voltage level through clamping diodes. In addition, the neutral point enables the generation of a zero voltage level, obtaining a total of three different voltage levels.

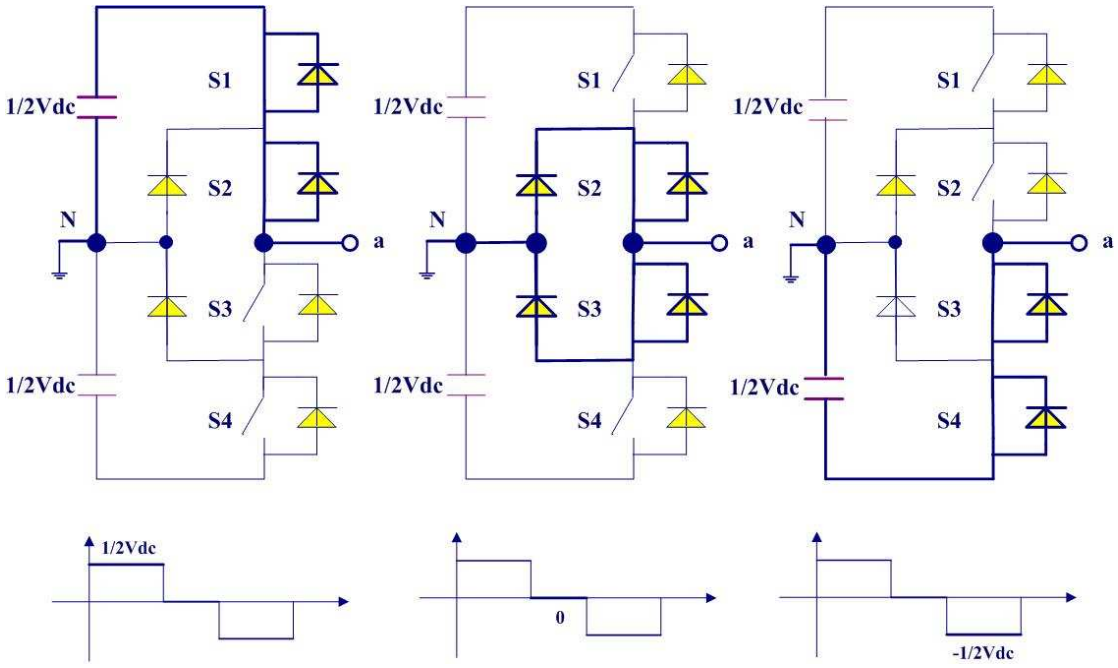


Figure 1-2 Three-level diode clamped converter switching states and corresponding output voltage level

The switching state of a converter is a set of signals used to control each switching device of power circuit. They can modify its conduction state and the way the load is connected to the different nodes of the DC side circuit. Hence a particular switching state generates a corresponding output voltage level. Figure 1-2 shows the three different switching states for the phase A of a three-level diode clamped converter and their corresponding output voltage levels. For voltage level *½* V_{dc}, turn on S_1, S_2; for voltage level *0* V_{dc}, turn on S_2, S_3; for voltage level *-½* V_{dc}, turn on S_3, S_4. The obtained equivalent circuit is highlighted to show

how the output node A is linked to the positive, neutral, and negative nodes of the DC side circuit. The same switching states can be applied for phases B and C.

The diode clamped converter topology can be extended to higher power rates and more output voltage levels by adding additional power switches and clamping diodes to be able to block higher voltages. Figure 1-1 (b) shows phase A of a five-level diode clamped converter. The number of clamping diodes needed to share the voltage increases dramatically. This fact, together with the increasing difficulty to control the DC-link capacitor unbalance, has kept the industrial acceptance of the diode clamped converter topology up to three levels only.

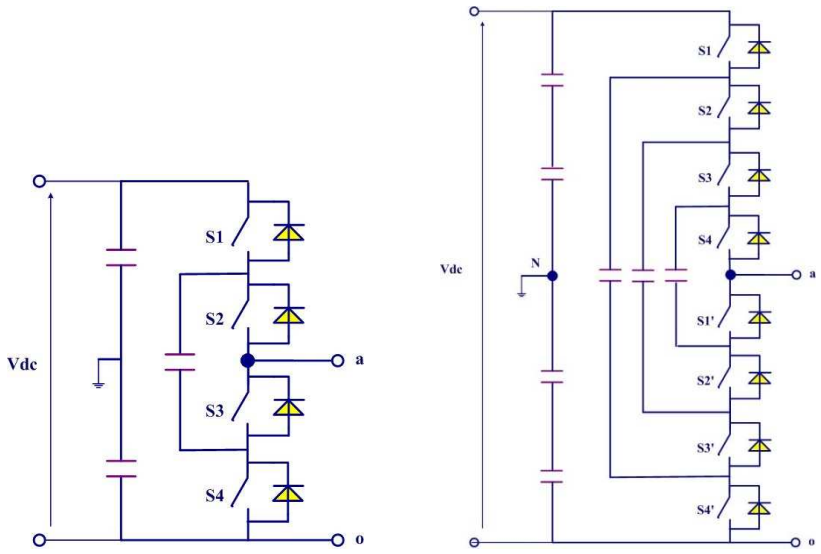
The advantages and disadvantages of a diode clamped converter are [18]:

Advantages:

- When the number of levels is high enough, harmonic content will be low enough to avoid the need for filters.
- Efficiency is high because all devices are switched at the fundamental frequency.
- Reactive power flow can be controlled.

Disadvantages:

- Excessive clamping diodes are required when the number of levels is high.
- It is difficult to do real power flow control for the individual converter.



(a) *(b)*

Figure 1-3 Capacitor clamped multilevel converter topologies (a) Three-level (b) Five-level

The phase A of a three-level capacitor clamped converter is shown in Figure 1-3 (a). The voltage level defined in the capacitor clamped converter is similar to that of the diode clamp type converter. The zero level is obtained by connecting the load to the positive or negative bar through the flying capacitor with opposite polarity respect the DC-link. For voltage level *½ V_{dc}*, turn on *S_1, S_2*; for voltage level *0 V_{dc}*, turn on *S_1, S_3*; for voltage level *-½ V_{dc}*, turn on *S_3, S_4.* Figure 1-4 shows the switching states and their equivalent power circuits with corresponding output voltage levels.

The capacitor clamped converter topology can be extended to higher power rates and more output voltage levels by adding additional power switches and clamping diodes to be able to block higher voltages. Figure 1-3 (b) shows the phase A of a five-level capacitor clamped converter.

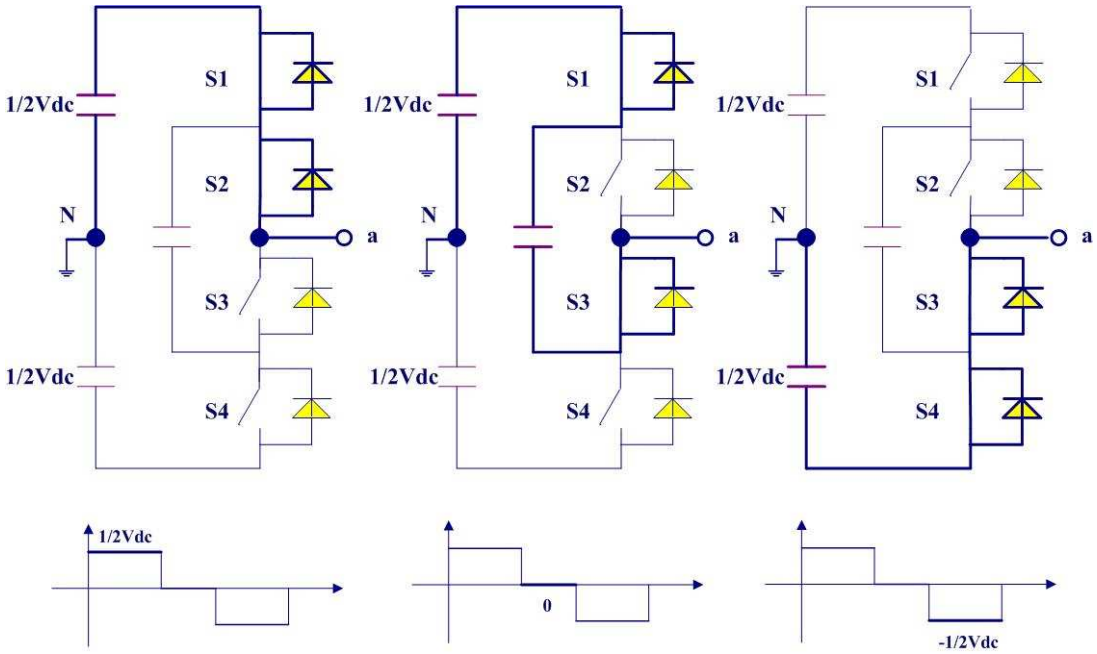


Figure 1-4 Three-level capacitor clamped converter switching states and corresponding output voltage level

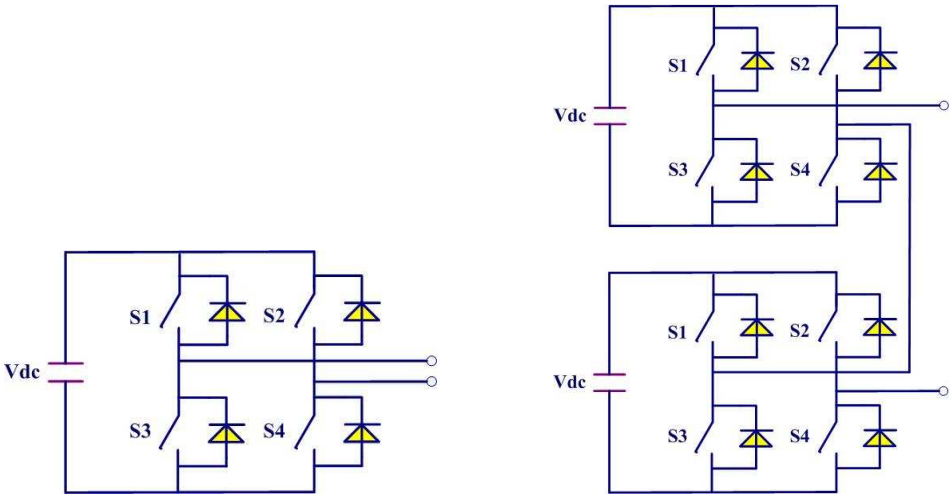
The advantages and disadvantages of a flying capacitor converter are [18]:

Advantages:

- Large amount of storage capacitors provides extra ride through capabilities during power outage.
- Provides switch combination redundancy for balancing different voltage levels.
- When the number of levels is high enough, harmonic content will be low enough to avoid the need for filters.
- Both real and reactive power flow can be controlled, making a possible voltage source converter candidate for high voltage DC transmission.

Disadvantages:

- An excessive number of storage capacitors is required when the number of converter levels is high. High-level systems are more difficult to package and more expensive with the required bulky capacitors.
- The inverter control will be very complicated, and the switching frequency and switching losses will be high for real power transmission.



(a) *(b)*

Figure 1-5 Cascaded H-bridge multilevel converter topologies (a) Three-level (b) Five-level

The Figure 1-5 (a) shows the phase A of a three-level cascaded H-bridge converter. Cascaded multilevel converter is formed by the series connection of two or more H-bridge converters. Each H-bridge corresponds to two voltage source phase legs, where the line-line voltage is the converter output.

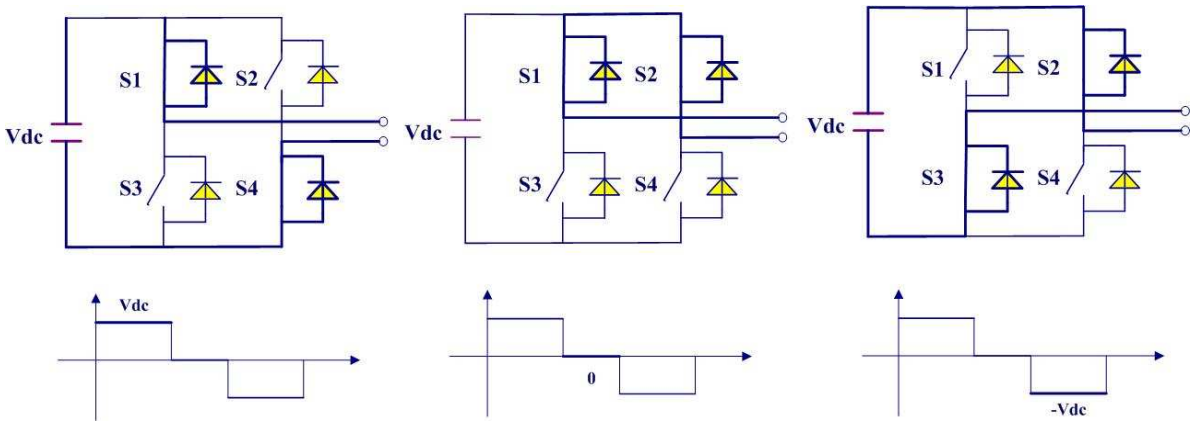


Figure 1-6 Three-level cascaded H-bridge converter switching states and corresponding output voltage level

Figure 1-6 shows the three different output voltage levels and their corresponding equivalent circuits. For voltage level V_{dc}, turn on S_1, S_4; for voltage level *0* V_{dc}, turn on S_1, S_2; for voltage level -V_{dc}, turn on S_2, S_3. Figure 1-5 (b) shows phase A of a five-level cascaded H-bridge converter.

The advantages and disadvantages of a cascaded multilevel converter are [18]:

Advantages:

- Requires the least number of components among all multilevel converters to achieve the same number of voltage levels.
- Modularized circuit layout and packaging is possible because each level has the same structure, and there are no extra clamping diodes or voltage balancing capacitors.
- Soft-switching can be used in this structure to avoid bulky and lossy resistor-capacitor-diode snubbers.

Disadvantages:

- Needs separate DC sources for real power conversions, and thus its applications are somewhat limited.

Without semiconductor devices connected in series, the multilevel converters show feasible capability of clamping the voltage across individual devices below their limitations. This allows the recent semiconductor devices to be utilized in higher-voltage applications without incurring voltage sharing problems. Another significant advantage of the multilevel configuration is the harmonic reduction in the output waveform with low switching frequency. The quality of the output voltage is improved as the number of voltage levels increases, so the quantity of output filters can be decreased. The transformers can be eliminated due to the reduced voltage that the switch sustains.

1.4 Control Technology

The main function of the STATCOM control is to operate the converter power switches so as to produce a synchronous output voltage waveform that forces the reactive power exchange required for compensation by generating a set of coordinated timing waveforms, which determines the on and off periods of each switch in the converter corresponding to the wanted output voltage. These timing waveforms have a defined phase relationship between them, determined by the converter pulse number, the method used for constructing the output voltage waveform, and the required angular phase relationship between the three outputs.

The magnitude and angle of the output voltage determine the reactive current the converter draws from, and thereby the reactive power it exchanges with the AC system. There are two typical STATCOM control schemes: 1) Direct control method is to keep the DC voltage

constant and control the reactive output current directly by controlling the converter output voltage through voltage control mechanism; 2) Indirect control method derives the necessary magnitude and angle for the converter output voltage to establish the required DC voltage on the DC capacitor since the magnitude of the AC output voltage is directly proportional to the DC capacitor voltage. Because of this proportionality, the reactive output current can be controlled indirectly via controlling the DC capacitor voltage, which is controlled by the angle of the output voltage.

Space vector control is widely implemented in motor drives and Uninterruptible Power Supply (UPS) control. In those applications, due to the real power input to the system, DC bus voltage and current need to be regulated by controlling real power. With space vector control methodology, real current I_d and reactive current I_q are controlled separately. A 1^{st} order transfer function including decoupling control items and neglecting the DC-side dynamics is proposed by Dr. F. Z. Peng and utilized for the STATCOM internal current control design [18]. A generalized 2_{nd} order transfer function of a CMC-based STATCOM including the cross-coupling effects but neglecting DC-side dynamics is derived for the internal current loop control design by Dr. Siriroj Sirisukprasert [19][20].

In STATCOM application, the bus voltage is regulated by exchanging reactive power between STATCOM and power system. In another word, there is no real power exchange during the voltage regulation procedure. As a result, I_d is equal to 0. In [21], angle control method is proposed. Compared with space vector control, which controls I_d and I_q by regulating the magnitude and phase of inverter output voltage, angle control methodology

keeps the bus voltage and inverter output voltage in the same phase in steady state and controls I_q by regulating magnitude of inverter output voltage, which is determined by DC bus voltage.

For STATCOM with space vector control, different magnitudes of converter output voltages are controlled by adding notches to the converter output, which can be achieved by changing modulation index of Pulse-Width Modulation (PWM). The PWM application has a negative impact on the multi-pulse waveform quality, resulting in high THD. For STATCOM with angle control, the control angle has some value to achieve I_q change and keeps as *0* in the steady state. Comparing these two control methodologies, the angel control is presently considered practical for transmission line applications.

1.5 STATCOM Operation Problems

Of all the possible contingencies that the converter has to be protected against, four events have been identified [22]:

- Device failure
- Inrush current and startup stresses
- Disturbance in AC system
- Severe DC bus unbalance

In case of device failure, the primary system protection has to be built into the in converter design. The author of [22] gives detailed protection for device short circuit event and open circuit event. There are many discussions on STATCOM operation with unbalance DC bus

voltage. In this dissertation, the primary protection on disturbance in AC system case through a suitable control scheme will be introduced.

1.6 Phase-Locked Loop

The control systems of modern FACTS are becoming sophisticated and the good performance of the utility connected systems depends on the quality and precision in which the utility voltage information is obtained. The role of Phase-locked loop (PLL) structure/dynamics in meeting these requirements is becoming an important research topic [23]. A reference phase signal synchronized with the AC system is provided by PLL. This reference signal is used as a basic carrier wave for deriving valve-firing pulses in control circuits. The actual valve-firing instants are calculated using the PLL output as the base signal and adding the desired valve firings. Typically, the desired firings are calculated in the main control circuit achieving regulation of some output system variables. The dynamically changing reference from a PLL therefore influences actual firings and it plays an important role in the system dynamic performance.

Under distorted utility conditions, the PLL structure should not interfere on the AC power conversion systems performance and must be able to maintain the phase lock. Besides, the PLL system should be able to lock-in as fast as possible and to provide the reference signals without distortions [24].

When faults occur in power system, grid voltage is unbalance. The negative sequence component will make double grid frequency fluctuation in synchronous reference frame, which will badly deteriorate the PLL function. The zero crossing detection method is

presented in [25]. It tracks the grid phase angle by detecting the zero crossing points of the line voltage instantly, but it is sensitive to the distortion the singles and the variation of each phase is not considered in angle detection process. The most commonly used PLL technology is the so-called synchronous reference frame strategy (SRF) to detect the phase angle in the d-q axes [26]-[29]. The traditional SRF-PLL system is composed of phase detector part and the loop filter part. The phase detection is obtained by the transformation from the natural reference frame to the synchronous reference frame. The loop filter determines the dynamics of the PLL system. The performance of conventional SRF-PLL is not good when the utility voltage presents voltage unbalances and/or voltage harmonic components. In [30], a double decoupled SRFPLL (DDSRF-PLL) is reported. The main part of the DDSRF-PLL is its positive and negative sequence decoupling computational unit which is used for solve the unbalanced problem. The DDSRF-PLL includes two decoupling computational units and other four low pass filter for filtering the harmonic distortion. In [32], a sinusoidal signal integrator (SSI) based PLL used for real power filter application was reported. The SSI-PLL combines a harmonics filtering and positive sequence extraction in the stationary rotational reference frame condition. The dynamic response and filtering performance is a trade-off for this method. In [33], an enhanced PLL (EPLL) is given. The EPLL structure is not simple enough, since it composed of four EPLL components and a positive sequence extraction unit for the whole PLL system. Its dynamic response is lower because of the low pass filters applications for a higher filtering performance. In [34], a multi-block adaptive notch filter (ANF) integrated into a conventional three-phase synchronous reference frame phase-locked

loop (SRFPLL). To remove frequency ripple cased by input signal unbalance and remove harmonic errors.

1.7 Ice-melter Technology

The transmission system within the temperate and northern climes must contend with the vagaries of ice storms. Ice accumulated on the transmission line can cause extensive damage to the power system, causing towers to collapse [25] - [39]. There have been some viable methods to solve this problem. The Electro-Impulse De-Icing (EIDI) mentioned in [25], involves discharge of a capacitor through an electric coil. This coil, when energized produces a strong magnetic field to produce a large amplitude impulsive force to De-ice an operating power line. The use of specially strengthened lines may require rebuilding the line, which could be uneconomic. The application of high-frequency current to melting ice on power transmission lines in [36]-[37] is also not a good solution because a large amount of reactive support would be required. The voltage to generate the necessary current through the line would be too large and the current cannot be controlled easily. Ice on power transmission lines can be melted effectively by passing DC currents through the transmission conductors. The use of short circuit AC current, in [38], may not supply enough current to melt ice buildup. Large line-commutated thyristor converters can be built to provide a controlled source of DC power for these applications. This costly equipment would not be useable for any other purpose and would only provide value on the very rare occasions when ice buildup occurs. The STATCOM can provide a novel, cost-effective solution, by connecting via its DC terminals to a source and used as an interface to the AC power system [39].

In a conventional application, STATCOM can be used to provide fast reactive power for voltage support and power oscillation damping. The same equipment, with a simple control reconfiguration, can perform ice melting function when it is needed.

1.8 Motivation and Dissertation Outline

The goal of this report is to achieve high-performance and reliable controller for the STATCOM. Major contributions are addressed as follows:

- Emergency PWM
- Instantaneous Phase-locked Loop
- STATCOM de-icer implementation
- Supercapacitor as energy storage for distribution system

Based on the sequence of the contributions above, this dissertation is divided into seven chapters.

Chapter 1 introduces the motivation and background of this dissertation. High power converter topologies and applications are briefly described. STATCOM control topologies and operation problem are presented.

Chapter 2 presents the principals of STATCOM operation and control. Vector control and angle control methods are derived from the equivalent circuit. The STATCOM operation problem is explained by a real system example.

Chapter 3 begins with discussion of system performance with STATCOM. Vector control and angle control are compared to define the problem.

Chapter 4 proposes “Emergency PWM” and “Instantaneous Phase-locked Loop” as practical operation strategies for STATCOM under faults in the power system.

Chapter 5 presents the modeling and control design of STATCOM for De-Icer application. Three control reconfiguration are introduced.

Chapter 6 presents the design and control of integrated STATCOM and Supercapacitor for distribution system performance improvement. The system performance under faults is discussed through current spectra analysis.

Chapter 7 draws conclusion for this report and proposes the future work. The possible future work, such as control and model of STATCOM combined with non-linear transformer, saturable transformer flux control, control of integrated STATCOM and Supercapacitor, etc, could be further studied.

CHAPTER 2 STATCOM SYSTEM OPERATION AND CONTROL

2.1 STATCOM

Basically, the STATCOM system is comprised of three main parts: a Voltage Source Converter (VSC), a set of coupling reactors or a step-up transformer, and a controller. The STATCOM is connected to the power networks at a Point of Common Coupling (PCC), where the voltage-quality problem is a concern. The Figure 2-1 shows the schematic configuration of STATCOM. The charged capacitor C_{dc}, provides a DC voltage to the converter, which produces a set of controllable three-phase output voltages. The exchange of real power and reactive power between the STATCOM and the power system can be controlled by adjusting the amplitude and phase of the converter output voltage V_o through the turn-on/turn-off of VSC switches, so that the VSC output current $I_{q,}$ which is equal to the sum of the VSC output voltage V_o minus the voltage at PCC V_{pcc} divided by the impedance of coupling reactor X, can be controlled.

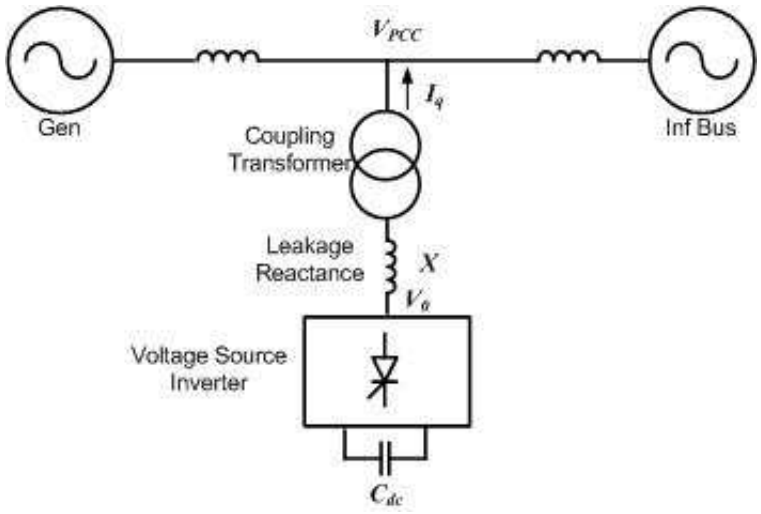


Figure 2-1 Schematic configuration of STATCOM

In the case of an ideal lossless power converter, *Vo* is controlled to be in phase with V_{pcc}. In this case, there is no real power circulated in the STATCOM; therefore, a real power source is not needed. When STATCOM operates in standby mode, V_o and V_{pcc} have the same magnitude and phase. There is no reactive power between STATCOM and system, as shown in Figure 2-2 (a). When V_o is greater than V_{pcc}, leading reactive current is drawn from the line and the STATCOM operates in capacitive mode, as shown in the Figure 2-2 (b). When V_o is smaller than V_{pcc}, lagging reactive current is drawn and the STATCOM operates in inductive mode, as shown in the Figure 2-2 (c). In practice a small amount of real power is also drawn from the line to supply the losses of the converter.

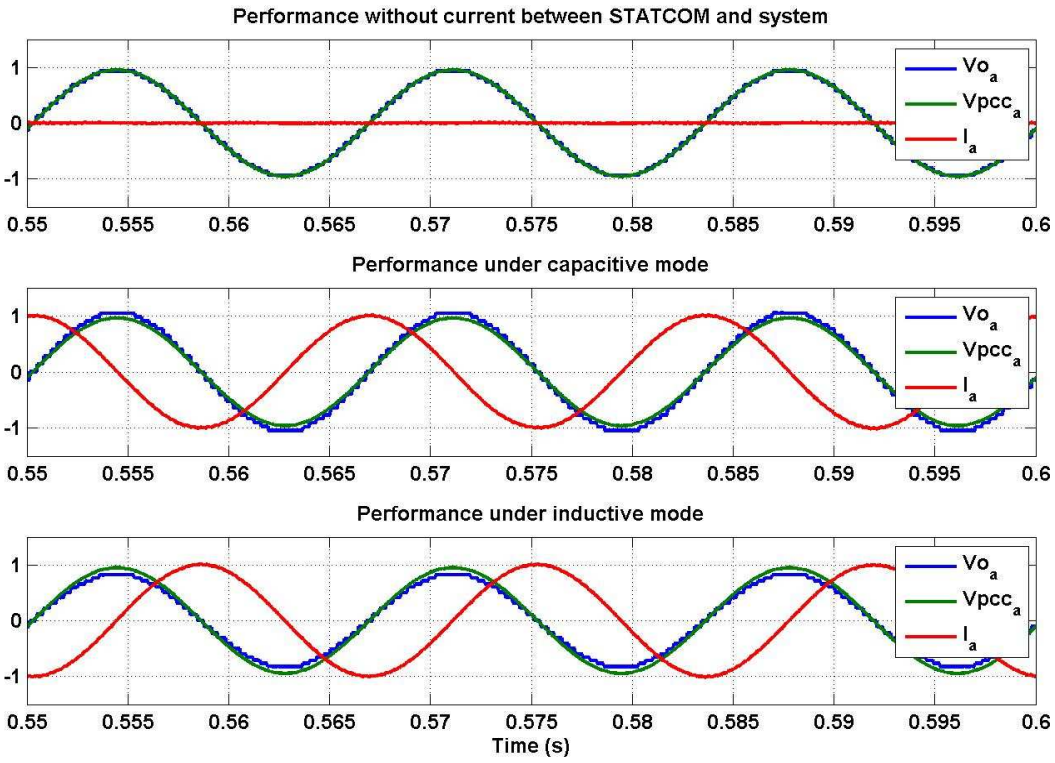


Figure 2-2 Inverter output voltage (Voa), Bus voltage (Vpcca) and Inverter current (Ia) when STATCOM operates in (a) no reactive power between STATCOM and system (b) capacitive mode, (c) inductive mode

2.2 48-pulse Voltage Source Converter

Figure 2-3 (a) and (b) show the output line-to-line waveforms of a two-level VSC and a three-level voltage source converter, respectively. Both converters operate at the same line-to-line voltage of 500 V, operated with PWM. The frequency spectra of Figure 2-3 (a) and (b) are shown in Figure 2-3 (c) and (d), respectively. The results show that the total harmonic distortion (THD) of the three-level converter output voltage is 23.69%, whereas it is 38.68% for that of the two-level VSC. As a result, the three-level converter can operate at a lower

switching frequency to achieve the same THD. Meanwhile, at the same THD, the output filter circuit for the three-level converter can be much smaller.

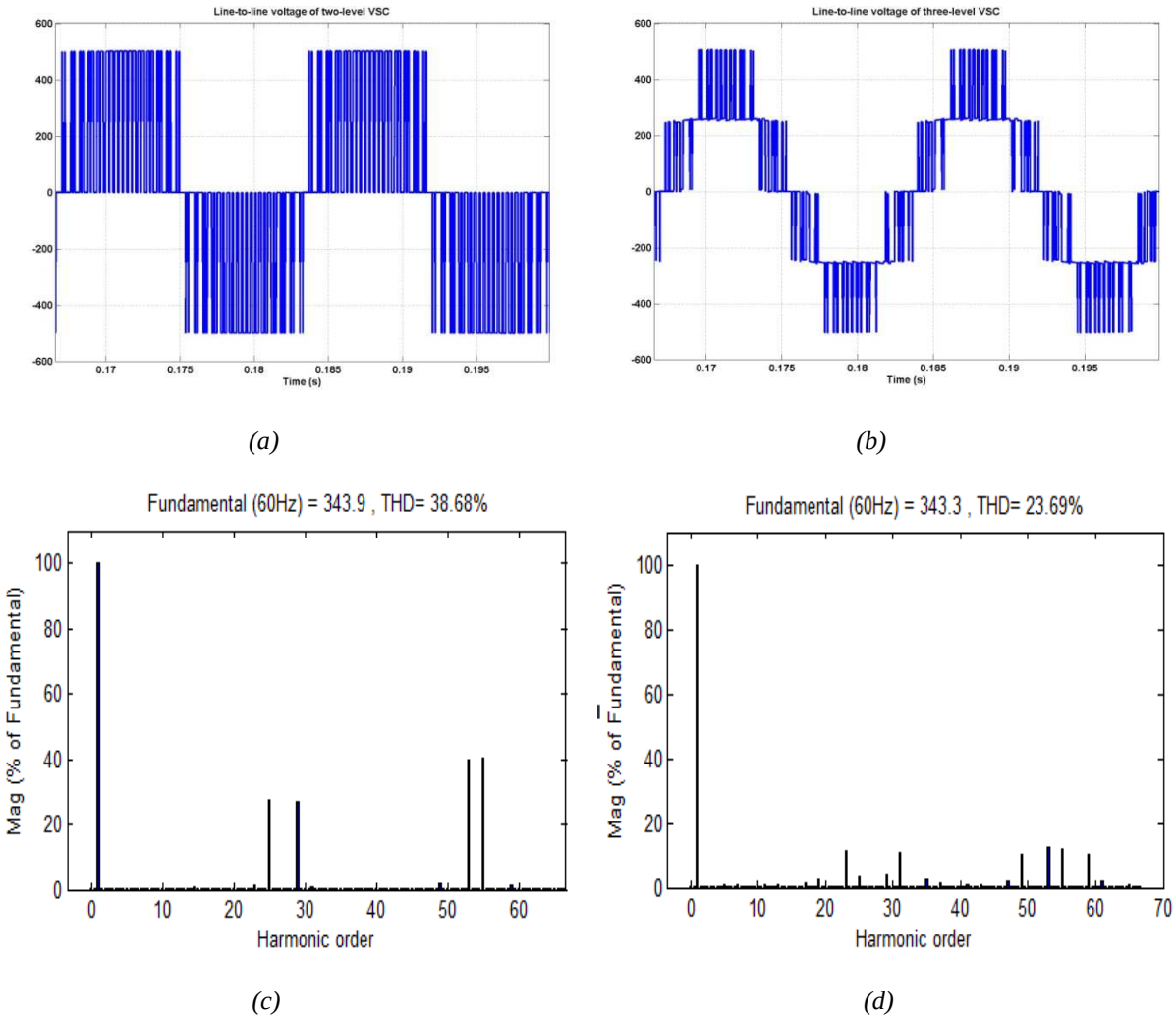


Figure 2-3 Simulation results for (a) the two-level VSC line-to-line voltage, (b) the three-level VSC line-to-line voltage, (c) the frequency spectrum of (a), (d) the frequency spectrum of (b)

To avoid additional filter circuit, a greater number of voltage pulses are required. The THD of the multilevel converter voltages is relatively low. Figure 2-4 shows the phase voltage of a

3-level VSC. The phase voltage V_{aN} with respect to the hypothetical midpoint N of the DC voltage is given by

$$V_{aN} = \frac{2V_d}{\pi}\sum_{k=1}^{\infty}\frac{(-1)^{k-1}}{2k-1}sin\frac{(2k-1)\sigma}{2}\sin(2k-1)\,\omega t,\ \ k = 1,2,3\ldots$$

Equation 2-1

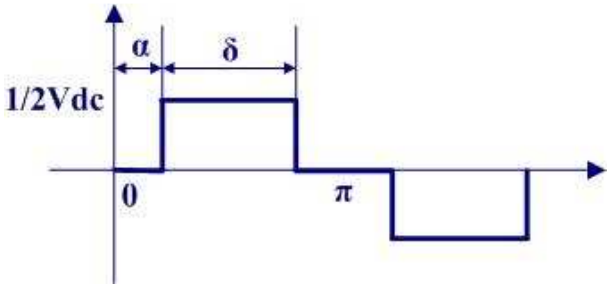


Figure 2-4 The phase voltage of 3-level VSC

The phase-to-phase voltage V_{ab} is given by

$$V_{ab} = \frac{4V_{dc}}{\pi}\sum_{k=1}^{\infty}\frac{1}{2k-1}sin\frac{(2k-1)\pi}{3}sin\frac{(2k-1)\sigma}{2}sin(2k-1)\,(\omega t+\frac{\pi}{6}),\ \ k = 1,2,3\ldots$$

Equation 2-2

The phase-to-neutral voltage V_{an} with respect to the AC neutral point n is given by

$$V_{an} = \frac{8V_{dc}}{3\pi}\sum_{k=1}^{\infty}\frac{(-1)^{k-1}}{2k-1}\sin^2\frac{(2k-1)\pi}{3}sin\frac{(2k-1)\sigma}{2}\sin(2k-1)\,\omega t,\ \ k = 1,2,3\ldots$$

Equation 2-3

Figure 2-5 shows the configuration of three-level 24 pulse VSC. The phase-to-phase voltage V_{ab} of one converter is connected to a delta-connected secondary of a transformer, with $\sqrt{3}$

times the turns compared to the wye-connected secondary, which is connected to phase-to-natural voltage V_{an} of the other converter, and the pulse train of the other converter is shifted by 30º. These two output voltages are then added to give

$$\frac{4V_{dc}}{\pi}\left[sin\frac{\delta}{2}sin\omega t - \frac{1}{11}sin\frac{11\delta}{2}sin11\omega t + \frac{1}{13}sin\frac{13\delta}{2}sin13\omega t - \frac{1}{23}sin\frac{23\delta}{2}sin23\omega t + \frac{1}{25}sin\frac{25\delta}{2}sin25\omega t + \cdots\right]$$

Equation 2-4

δ is set to 7.5º to eliminate the 11th and 13th harmonics, then Equation 2-4 is

$$V_{24} = \frac{4V_{dc}}{\pi}\left[sin\frac{\delta}{2}sin\omega t - \frac{1}{23}sin\frac{23\delta}{2}sin23\omega t + \frac{1}{25}sin\frac{25\delta}{2}sin25\omega t + \cdots\right]$$

Equation 2-5

The output voltage has normal harmonics $n = 24r \pm 1$, where *r = 0, 1, 2…i.e; 23th, 25th, 47th, 49th*… with typical magnitudes (1/23, 1/25, 1/47, 1/49…), respectively, with respect to the fundamental.

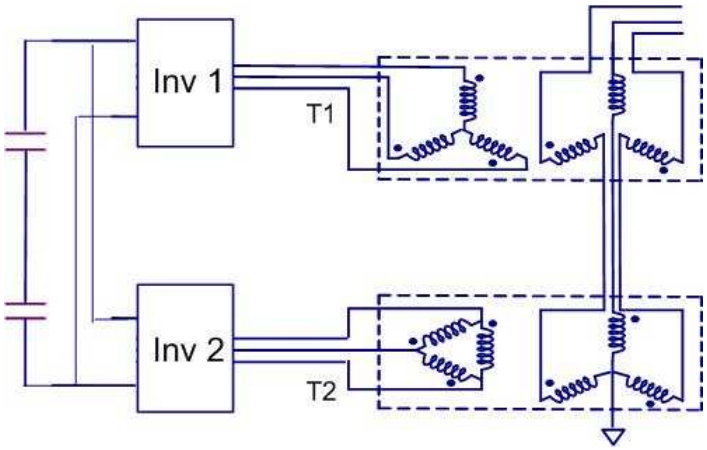


Figure 2-5 The 24-pulse voltage source converter circuit

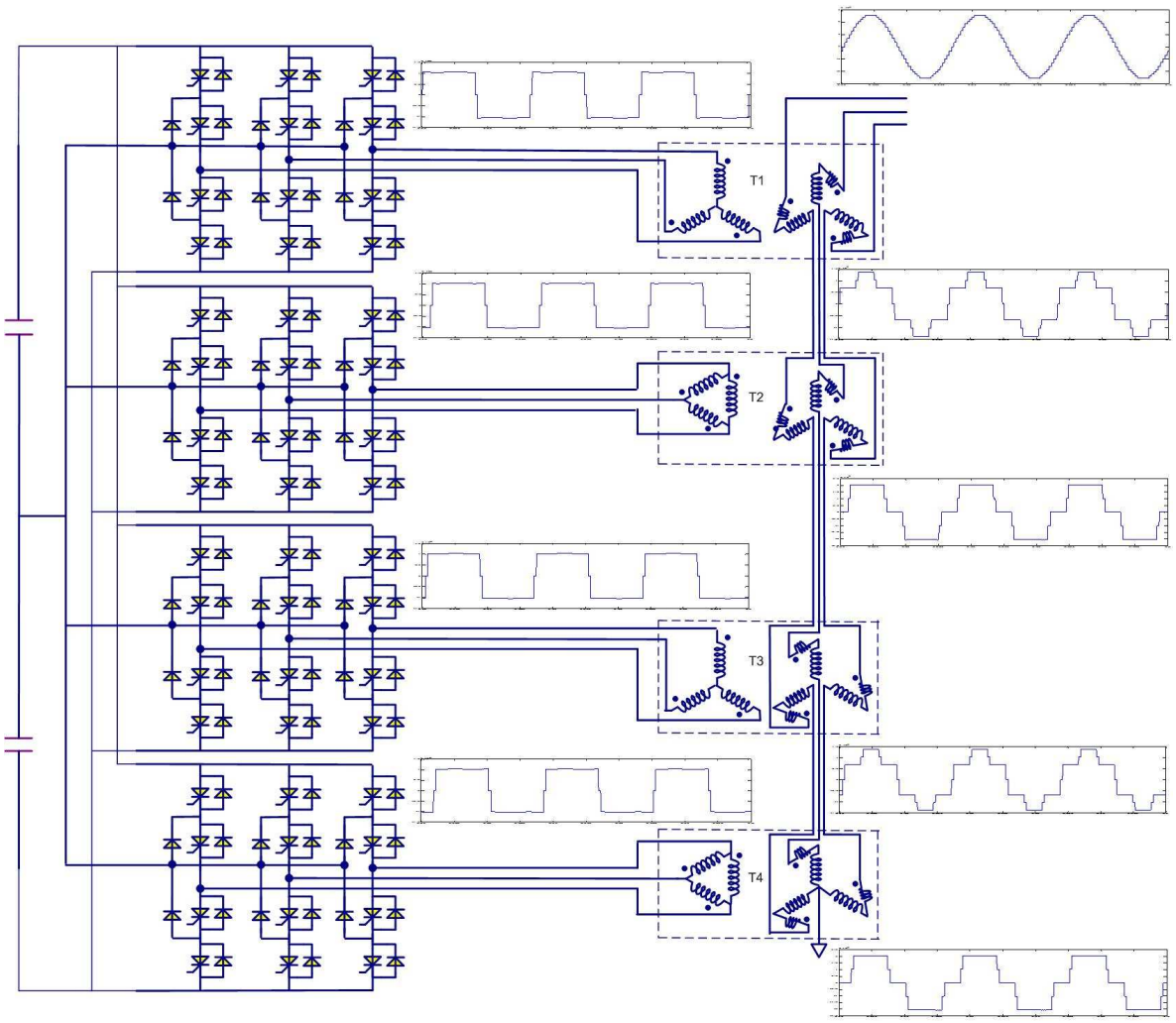


Figure 2-6 The 48-pulse voltage source converter circuit and waveform construction for STATCOM application

Figure 2-6 shows the 3-level 48 pulse VSC topology and the output voltage waveform construction for STATCOM application. The VSC consists of four (Inv 1 – Inv4) 3-level Neutral Point Clamped (NPC) converters which are connected in series by four (T1-T4) transformer coupling. The primary side of the transformer is connected in series. Due to the strict loss penalty for STATCOM application, each VSC is operated at fundamental frequency switching or in square-wave mode. The voltage waveform for each VSC output

and the waveform construction (summation) on the transformer primary side is shown in Figure 2-6.

Two 24-pulse VSCs, phase-shifted by 7.5º from each other, can provide the full 48-pulse converter operation. Using a symmetrical shift criterion, the 7.5º are proved in the following way: phase-shift winding with -3.75º on the two coupling transformers of on 24-pulse converter and +3.75º on the other two transformers of the second 24-pulse converter. The firing pulses need a phase shift of +3.75º. The output voltage has normal harmonics $n = 48r \pm 1$, where $r = 0, 1, 2…$*i.e;* 47^{th}, 49^{th}, 95^{th}, 98^{th}… with typical magnitudes (1/47, 1/49, 1/95, 1/97…), respectively, with respect to the fundamental. With a sufficiently high number of voltage levels, the 48-pulse converter can cancel harmonics synthesize clean sinusoidal output voltage using a relatively small filter circuit. Figure 2-7 shows the frequency spectrum of 48 pulse VSC, the THD is reduced to 0.86%.

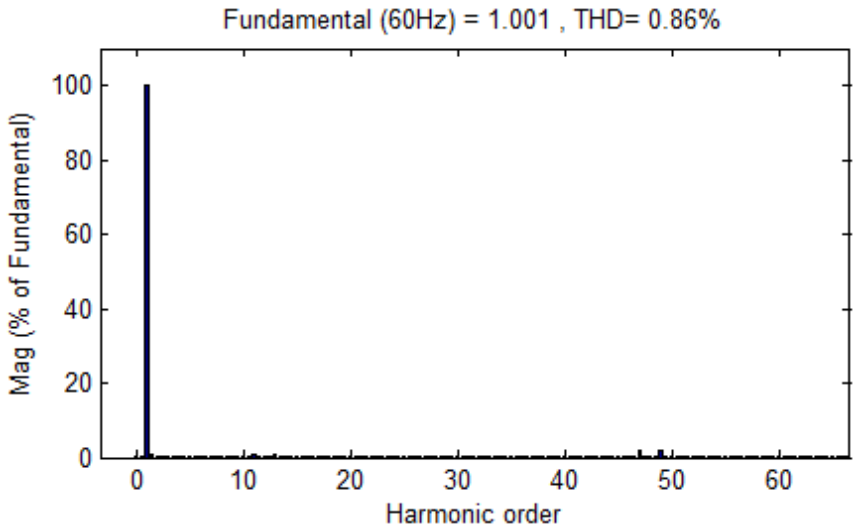


Figure 2-7 The frequency spectrum of 48 pulse VSC

2.3 STATCOM Control Methods

2.3.1 Equivalent circuit and equations [21]

Figure 2-8 shows the STATCOM equivalent circuit, including a DC-side capacitor, an converter and series inductance in the three lines connecting to the transmission line, where L_s accounts for the leakage of the actual power transformers, R_p, in shunt with the capacitor, represents the switching losses in the inverter, R_s, in series with the AC line, represents the inverter and transformer conduction losses.

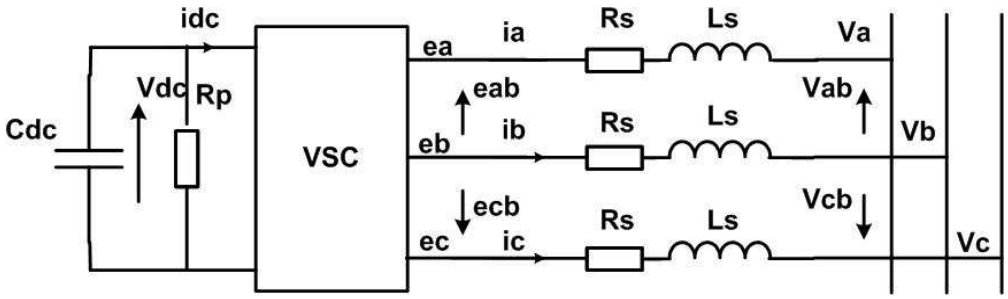


Figure 2-8 Equivalent circuit of VSC with harmonic bus voltages

The ac-side circuit a phase has the following equation:

$$R_s i_a + L_s p i_a = e_a - v_a$$

Equation 2-6

Where $p = d / dt$.

The AC-side circuit three phase equations in matrix can be written as:

$$p\begin{bmatrix} i_a' \\ i_b' \\ i_c' \end{bmatrix} = \begin{bmatrix} -\frac{R_s'\omega_b}{L'} & 0 & 0 \\ 0 & -\frac{R_s'\omega_b}{L'} & 0 \\ 0 & 0 & -\frac{R_s'\omega_b}{L'} \end{bmatrix} \begin{bmatrix} i_a' \\ i_b' \\ i_c' \end{bmatrix} + \frac{\omega_b}{L'} \begin{bmatrix} e_a' - v_a' \\ e_b' - v_b' \\ e_c' - v_c' \end{bmatrix}$$

Equation 2-7

Where a per-unit system has been adopted according to the following definitions:

$$L' = \frac{\omega_b L_s}{z_{base}},\ C' = \frac{1}{\omega_b C z_{base}},\ R_s' = \frac{R_s}{z_{base}},\ R_p' = \frac{R_p}{z_{base}}$$

$$i_x' = \frac{i_x}{i_{base}},\ v_x' = \frac{v_x}{v_{base}},\ e_x' = \frac{e_x}{v_{base}},\ z_{base} = \frac{v_{base}}{i_{base}}$$

Equation 2-8

With applying Park's transformation matrix shown in Equation 2-9,

$$T = \frac{2}{3}\begin{bmatrix} \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ -\sin(\theta) & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}$$

Equation 2-9

Equation 2-7 can be transformed to the synchronously rotating reference frame as Equation 2-10, where $\omega = d\theta / dt$:

$$p\begin{bmatrix} i_d' \\ i_q' \end{bmatrix} = \begin{bmatrix} -\frac{R_s'\omega_b}{L'} & \omega \\ -\omega & -\frac{R_s'\omega_b}{L'} \end{bmatrix} \begin{bmatrix} i_d' \\ i_q' \end{bmatrix} + \frac{\omega_b}{L'} \begin{bmatrix} e_d' - |v'| \\ e_q' \end{bmatrix}$$

Equation 2-10

Neglecting the voltage harmonics produced by the inverter, we can write a pair of equations for e_d' and e_q' as:

$$e_d' = kv_{dc}'\cos(\alpha)$$
$$e_q' = kv_{dc}'\sin(\alpha)$$

Equation 2-11

Where *k* is a factor for the inverter which relates the DC side voltage to the amplitude of the phase-to-neutral voltage at the inverter AC side terminals, and α is the angle by which the inverter voltage vector leads the line voltage vector.

2.3.2 Vector control

To obtain a decoupled control of i_d' and i_q', Equation 2-11 can be rewritten as:

$$e_d' = \frac{L'}{\omega_b}\left(x_1 - \omega i_q'\right) + |v'|$$
$$e_q' = \frac{L'}{\omega_b}\left(x_2 + \omega i_d'\right)$$

Equation 2-12

Substituting of Equation 2-12 into Equation 2-10, we can get

$$p\begin{bmatrix} i_d' \\ i_q' \end{bmatrix} = \begin{bmatrix} -\frac{R_s'\omega_b}{L'} & 0 \\ 0 & -\frac{R_s'\omega_b}{L'} \end{bmatrix} \begin{bmatrix} i_d' \\ i_q' \end{bmatrix} + \frac{\omega_b}{L'} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix}$$

Equation 2-13

Through a simple first-order transfer function, we can get the feedback loops and proportional-plus-integral (PI) compensation as:

$$x_1 = \left(i_d^* - i_d'\right) + \frac{R_s'\omega_b}{L'}\left(\frac{i_d^* - i_d'}{p}\right) = \left(k_a + \frac{k_b}{p}\right)\left(i_d^* - i_d'\right)$$
$$x_2 = \left(i_q^* - i_q'\right) + \frac{R_s'\omega_b}{L'}\left(\frac{i_q^* - i_q'}{p}\right) = \left(k_a + \frac{k_b}{p}\right)\left(i_q^* - i_q'\right)$$

Equation 2-14

Where k_a and k_b are parameters of PI controller.

Space vector control is shown in the Figure 2-9. The converter output current I_{inv} is decomposed into reactive current I_q and real current I_d components. E_q* is obtained by comparing I_q and the external reactive current reference I_q*, determined from the STATCOM outer-loop voltage control system. E_d* is obtained by comparing I_d and the internal real current reference I_d*, derived from the DC voltage regulation loop. E_q* and E_d* are converted into the magnitude and angle of the wanted converter output voltage, from which the appropriate gate drive signals, in proper relationship with the phase-locked loop provided phase reference, are derived.

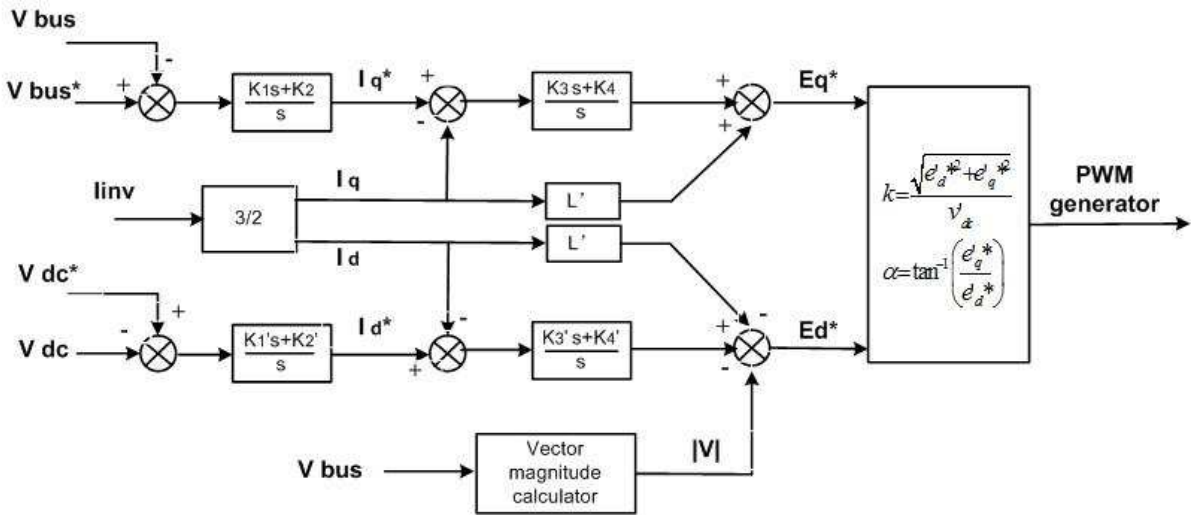
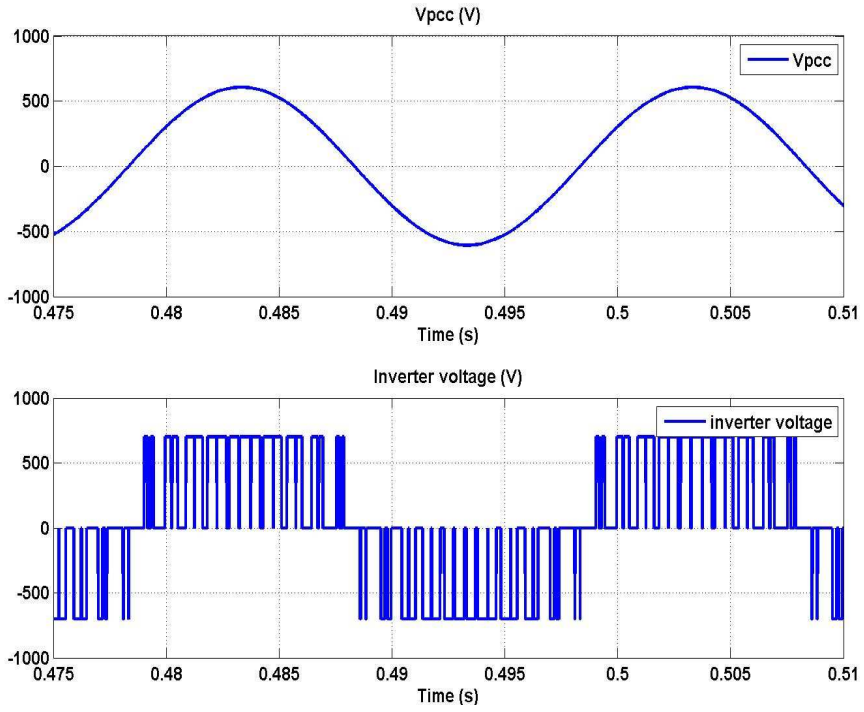
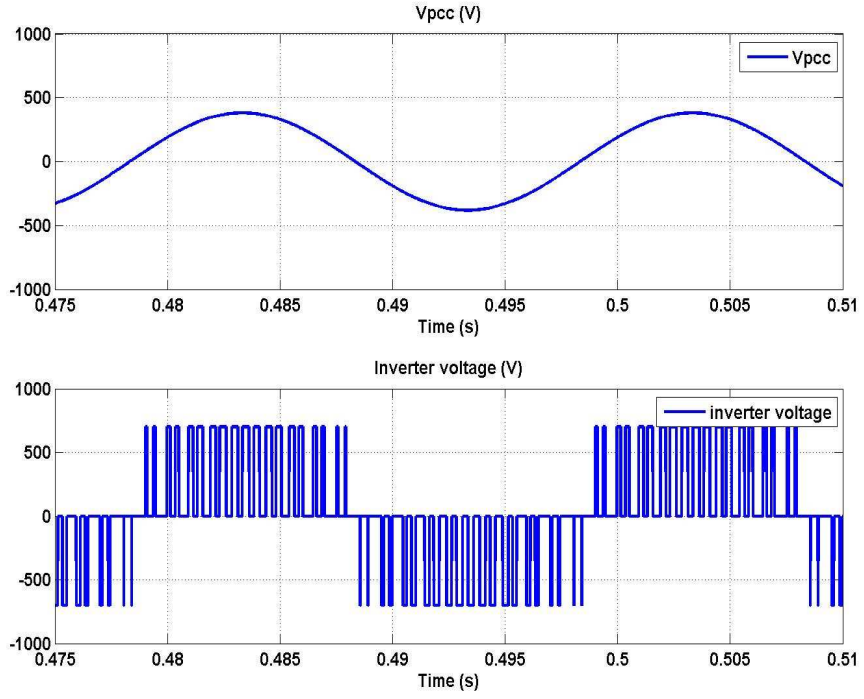


Figure 2-9 Block diagram of space vector control

Observe that in the space vector, the DC bus voltage is regulated to be constant. In order to control I_q, the converter output voltage is controlled to be in the same phase with AC bus voltage by adding notches, i.e. implementing the modulation index of PWM, as this has a direct effect on the VSC voltage magnitude, whereas the phase angle, which basically determines the real power P flowing into the controller and hence the charging and discharging on the capacitor, is used to directly control the DC voltage magnitude. The Figure 2-10 shows a 2-level VSC output voltage in two cases with different AC bus voltage. In both cases, the DC bus voltage is regulated to be 700V. The carrier frequency is 1200Hz. The AC bus voltage magnitude is 606V and 381V in case 1 and 2, separately. Compared with case 1 with higher AC bus voltage, to get the same I_q, there are more and wider notches in inverter output voltage in case 2 with lower AC bus voltage. The modular index of case 1 is equal to 0.89. The modular index of case 2 is equal to 0.58.



Case 1, Vpcc = 606V, Vdc = 700V, m = 0.89



Case 2, Vpcc = 381V, Vdc = 700V, m =0.58

Figure 2-10 Control AC bus voltage magnitude through modulation index of PWM

2.3.3 Angle Control

In Figure 2-8, the instantaneous powers at the AC and DC side of the inverter are equal, giving the following power balance equation:

$$v'_{dc}\, i'_{dc} = \tfrac{3}{2}\left(e'_d\, i'_d + e'_q\, i'_q\right)$$

Equation 2-15

And the DC side circuit equation is

$$pv'_{dc} = -\omega_b C'\left(i'_{dc} + \frac{v'_{dc}}{R'_p}\right)$$

Equation 2-16

Combining Equation 2-10, Equation 2-11 and Equation 2-16, the following state equations can be obtained:

$$p\begin{bmatrix} i_d' \\ i_q' \\ v_{dc}' \end{bmatrix} = \begin{bmatrix} -\frac{R_s'\omega_b}{L'} & \omega & \frac{k\omega_b}{L'}\cos(\alpha) \\ -\omega & -\frac{R_s'\omega_b}{L'} & \frac{k\omega_b}{L'}\sin(\alpha) \\ \frac{-3}{2}kC'\omega_b\cos(\alpha) & \frac{-3}{2}kC'\omega_b\sin(\alpha) & -\frac{\omega_b C'}{R_p'} \end{bmatrix}\begin{bmatrix} i_d' \\ i_q' \\ v_{dc}' \end{bmatrix} - \frac{\omega_b}{L'}\begin{bmatrix} |v'| \\ 0 \\ 0 \end{bmatrix}$$

Equation 2-17

To show the features of α, i_d and i_q, a 2-bus 500kV power system with a 48-pulse VSC based ± 100MVAR STATCOM is shown in Figure 2-11 as the evaluation system.

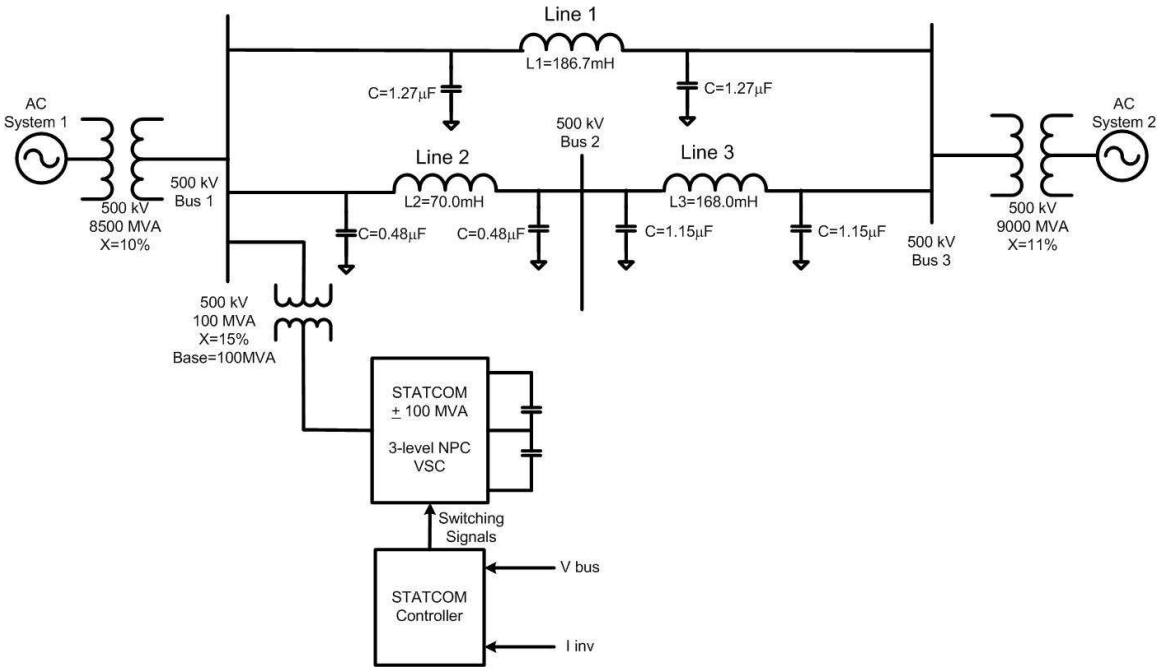


Figure 2-11 System simulation with a 48-pulse VSC based ± 100 MVAR STATCOM in Matlab/Simulink in a 2-bus power system

The steady-state solution of STATCOM circuit using typical system parameters is plotted in Figure 2-12 as a function of α_0 with parameters in the evaluation system list in Table 2-1, the "0" notations correspond to steady state values.

Table 2-1 Parameters of evaluation system

Power rating	100 MVA
Line-line voltage / inverter	15kV
Phase current	1.67kA
Transmission line voltage	500kV
Each Transformer	125kV/15kV
DC capacitor voltage	18.7kV
DC capacitor	3mF
Interface inductor	1.19mH, 15mΩ

According to Equation 2-8, $L' = 0.05$, $C' = 0.049$, $k = 0.46$, $R_s' = 0.0017$, $R_p' = \infty$, $v_0' = 1.0$, $\omega_0 = \omega_b = 377$ in the system.

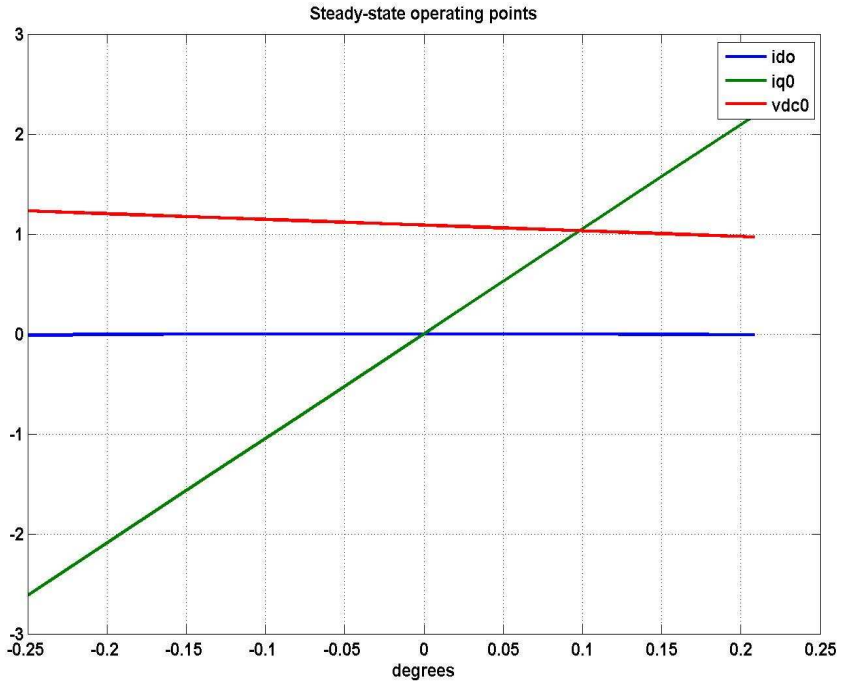


Figure 2-12 Steady State Characteristics of evaluation STATCOM system, where $L'=0.05$, $C'=0.049$, $k=0.46$, $R_s'=0.0017$, $R_p'=\infty$, $v_0'=1.0$, $\omega_0=\omega_b=377$

The figure has the following features:

- i_{d0} is very small compared with i_{q0}, which means there is almost no real power exchange between STATCOM and the power system, when there is +1p.u. reactive power exchange between them.
- The range of α_0 for one per-unit swing in i_{q0} is very small, which means i_{q0} control has small effect on DC bus voltage.

- i_{q0} varies almost linearly with respect to α_0 in the range shown in the figure. A positive α_0 means that STATCOM supplies reactive power to the system while a negative value implies absorbing reactive power from the system.

Equation 2-17 is nonlinear if α is regards as an input variable. The linearization process yields the following equation:

$$p\begin{bmatrix}\Delta i_d' \\ \Delta i_q' \\ \Delta v_{dc}'\end{bmatrix} = [A_\Delta]\begin{bmatrix}\Delta i_d' \\ \Delta i_q' \\ \Delta v_{dc}'\end{bmatrix} + [B_\Delta]\begin{bmatrix}\Delta v' \\ \Delta\alpha\end{bmatrix}$$

Equation 2-18

Where,

$$[A_\Delta] = \begin{bmatrix} -\frac{R_s'\omega_b}{L'} & \omega_b & \frac{k\omega_b}{L'}\cos(\alpha_0) \\ -\omega_b & -\frac{R_s'\omega_b}{L'} & \frac{k\omega_b}{L'}\sin(\alpha_0) \\ \frac{-3}{2}kC'\omega_b\cos(\alpha_0) & \frac{-3}{2}kC'\omega_b\sin(\alpha_0) & -\frac{\omega_b C'}{R_p'} \end{bmatrix},$$

$$[B_\Delta] = \begin{bmatrix} -\frac{\omega_b}{L'} & -\frac{k\omega_b v_{dc0}'}{L'}\sin(\alpha_0) \\ 0 & \frac{k\omega_b v_{dc0}'}{L'}\cos(\alpha_0) \\ 0 & \frac{3}{2}kC'\omega_b\left(i_{d0}'\sin(\alpha_0) - i_{q0}'\cos(\alpha_0)\right) \end{bmatrix}$$

In STATCOM application, the bus voltage is regulated by exchanging reactive power between STATCOM and power system. In another word, there is no real power exchange during the voltage regulation procedure. As a result, i_d is equal to 0. Compared with space

vector control, which controls i_d and i_q by regulating the magnitude and phase of inverter output voltage, in angle control methodology, changes in the magnitude of the converter output voltage are brought about indirectly by causing the DC bus capacitor to charge or discharge to a different voltage level. The converter output voltage is kept substantially in phase with the AC bus voltage. Raising or lowering the magnitude of the converter voltage causes the reactive current delivered to the AC bus to rise or fall, respectively. Small positive or negative deviations in the phase of the inverter voltage cause an increase or decrease of the dc bus voltage.

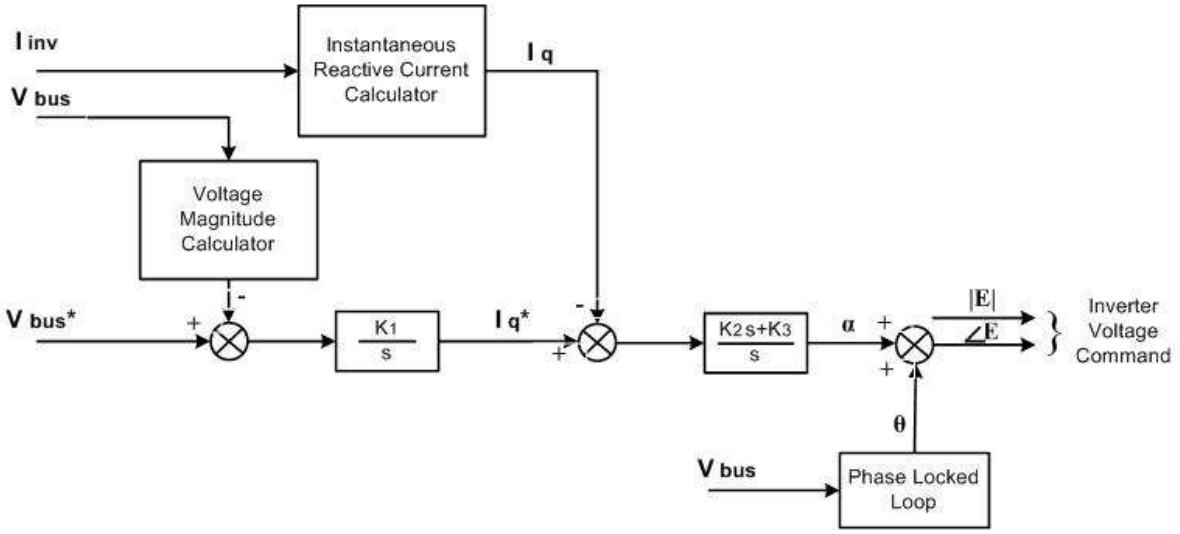


Figure 2-13 STATCOM angle controller block diagram

Figure 2-13 shows the implemented STATCOM angle controller. Refer to Figure 2-12, to control bus voltage V_{bus} by adjusting reactive current i_q, i.e. reactive power exchanging between the power system and STATCOM, the inputs to the outer loop controller are V_{bus} and reference value V_{bus}*, the deference between which generates reactive current reference

i_q* responsible for the system voltage control. An inner feedback loop is used to regulate the STATCOM instantaneous reactive current. The magnitude of i_q is compared to i_q*. The error thus obtained provides angle α, which defines the necessary phase shift between the output voltage of the converter and the AC system voltage needed for charging (or discharging) the storage capacitor to the DC voltage level required. AC system voltage operates a phase-locked loop that provides the basic synchronizing signal, angle θ. Angle $\theta+\alpha$ operates the gate pattern logic that provides the individual gate drive logic signals to operate the converter power switches.

2.3.4 Angle Control vs. Vector Control

In practice, for transmission line applications, a multi-pulse sinusoidal voltage is required to achieve adequate waveform quality. To compare the angle control and vector control, a 24-pulse STATCOM consists of two 3-level VSCs and two phase-shifting transformers as shown in Figure 2-5 Figure 2-5 is considered. The Figure 2-14 (a) and (b) show the STATCOM output voltage with angle control and vector control, separately. In Figure 2-14 (a), a clear 24-pulse voltage waveform with a phase displacement of 15° is obtained after adding electromagnetically the output voltages of two converters. In Figure 2-14(b), DC voltage reference is set refer to one operating point, for other operating points, vector control is realized by changing modulation index of PWM, i.e. high-frequency switching. As a result, adding the output voltages of two converters degrades the number of voltage pulse. The voltage quality will deteriorate because of reduced voltage levels and THD will increase substantially. Comparing these two control methodologies, angle control is more difficult to

be implemented, but STATCOM with angle control can generate higher-number-pulse sinusoidal voltage. Consequently, the angel control is presently considered practical for transmission line applications. And also, since switches are operated in fundamental frequency, angle control results in lower losses of the system.

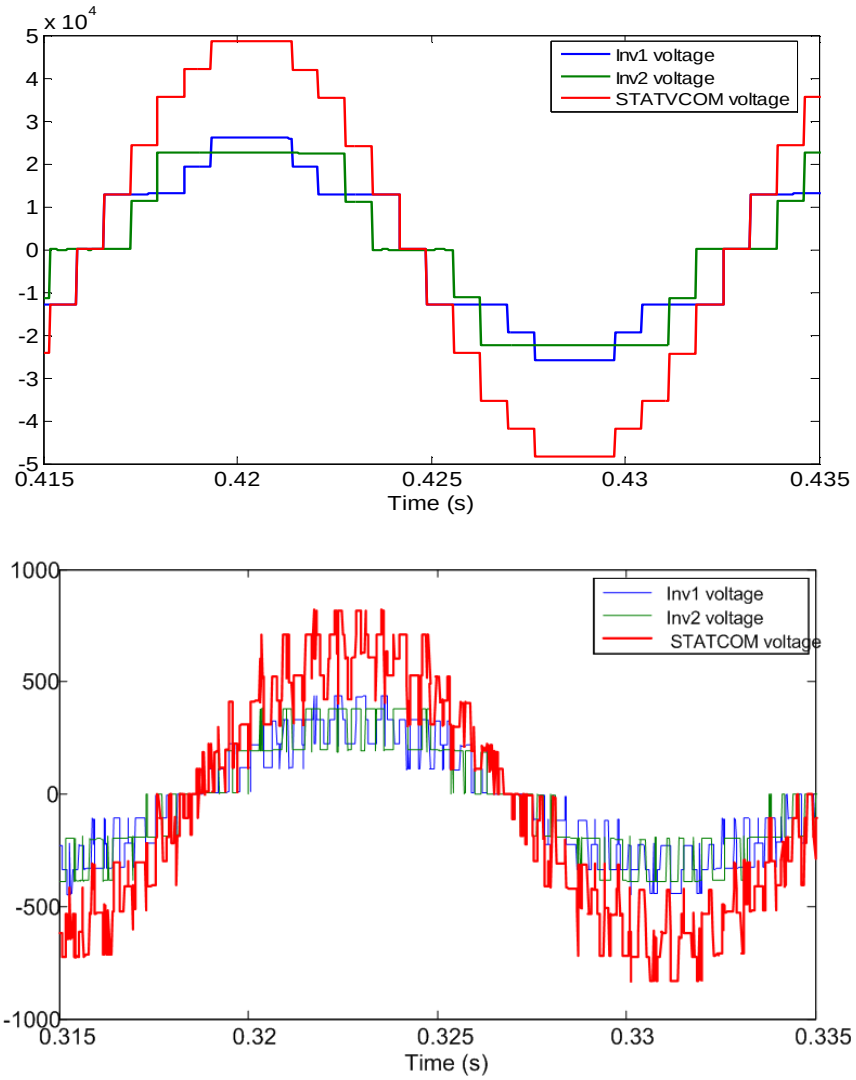


Figure 2-14 STATCOM output voltages with (a) angle control, (b) vector control.

2.4 STATCOM Operation Problems

Figure 2-15 shows the performance of VSC circuit which has been commercially used at two installations in the US, each for a 150MVAR STATCOM connected to a 138kV bus. The STATCOM performance is very good for voltage regulation. However, the performance of the STATCOM under system faults (such as single line-ground faults) results in converter over-currents and STATCOM trips. Figure 2-15 shows the Phase B bus voltage dips for 4 cycles due to a single-line to ground fault in 138kV system. It is seen that the primary STATCOM currents are large and the STATCOM trips. Examining further, it is seen that the VSCs "stop-gating" during the fault due to over-current strategy and enable the STATCOM to remain online, but cannot prevent the STATCOM trip recovering from the fault. It is realized that the VAR support functionality of the STATCOM is required the most during and after a system fault.

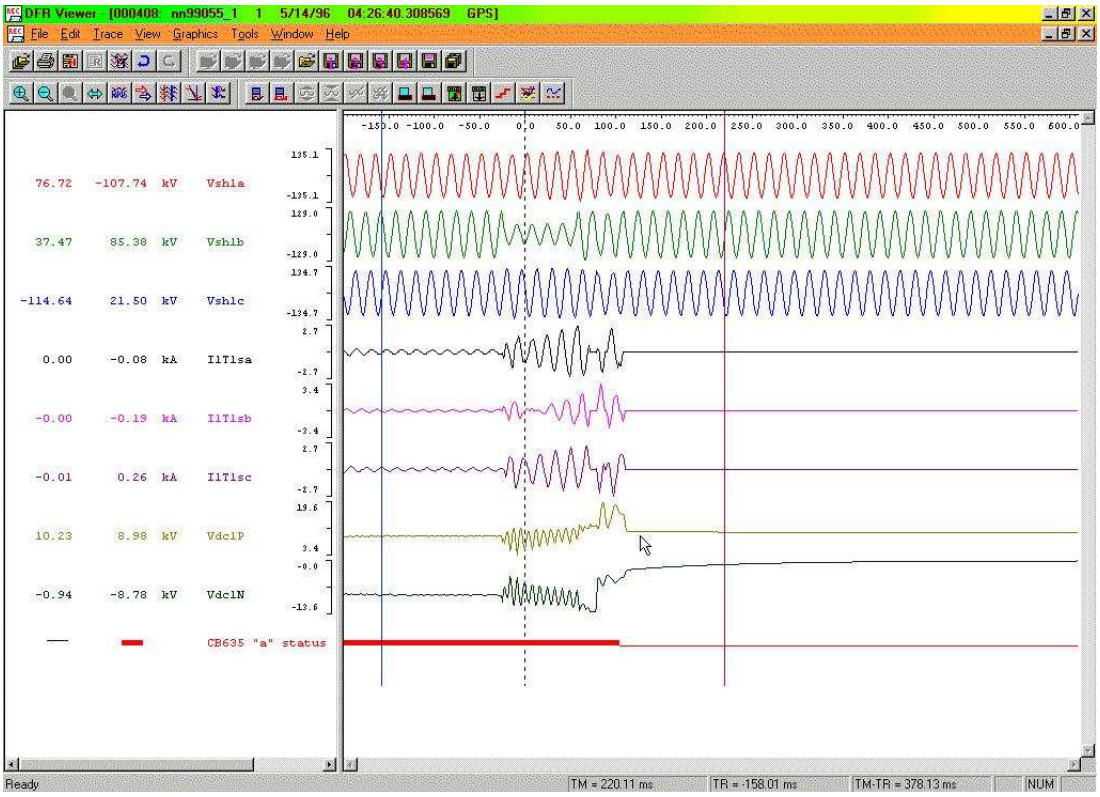


Figure 2-15 SATTCOM performance under remote single-line to ground fault resulting in Phase B bus voltage sag

CHAPTER 3 STATCOM OPERATION UNDER SYSTEM FAULTS - MOTIVATION AND PROBLEM STATEMENT

3.1 STATCOM Operation

3.1.1 STATCOM Operation under Normal Condition

Figure 3-1 and Figure 3-2 show the power system with STATCOM operation (shown in Figure 2-11) in Var regulation mode, with i_q reference is equal to 1, under normal system conditions. The STATCOM 48-pulse voltage waveform is verified in Figure 3-1. The VSC phase currents in Figure 3-2 are within 1550A (1 pu.) without any system disturbances.

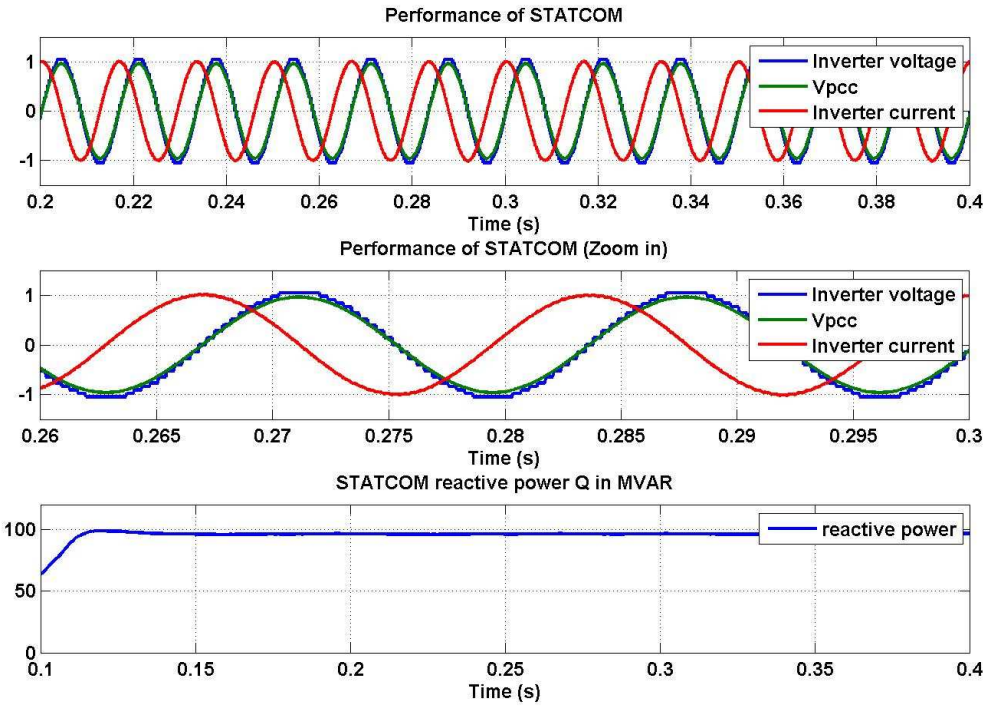


Figure 3-1 STATCOM operation in Var regulation mode under normal system condition (a) Bus voltage, STATCOM primary 48-pulse voltage, STATCOM primary injected current, (b) STATCOM reactive power Q in MVAR

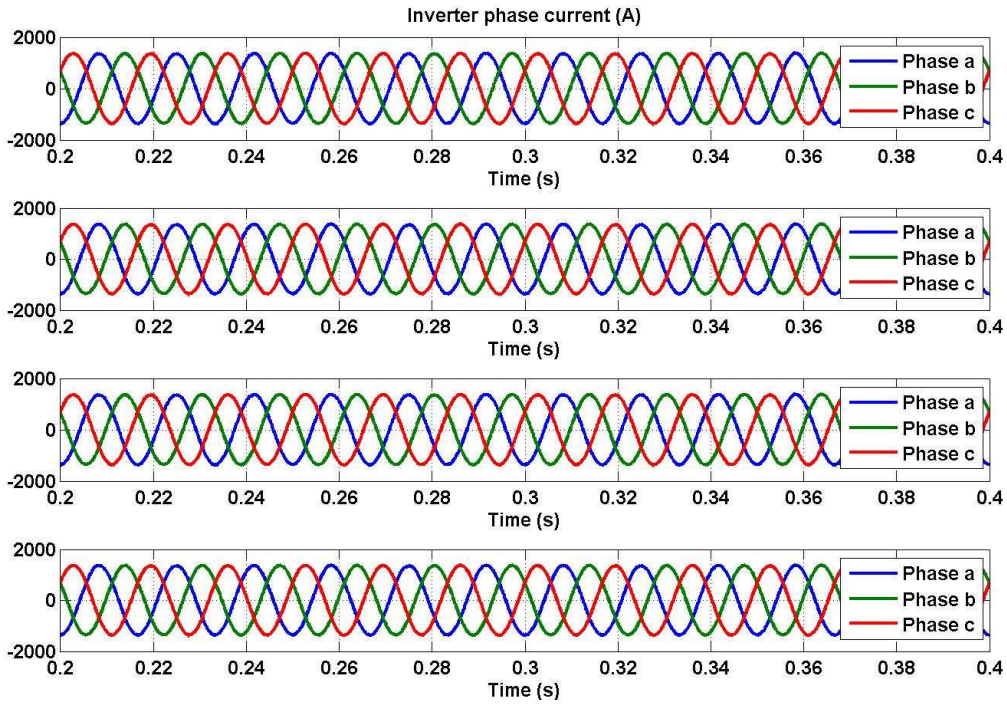


Figure 3-2 Four VSC phase currents under normal system operations

3.1.2 STATCOM Operation under Single-line to Ground Fault

Figure 3-3 and Figure 3-4 show the STATCOM operation in Var regulation mode under 6-cycle single-line to ground fault at bus 2. There is sag on AC bus voltage and accordingly, at the output voltage of converter due to the fault. Figure 3-4 shows that the VSC currents exceed 3000A (twice that of nominal 1550A peak in Figure 3-2), and will result in over-current and trip to protect the VSC devices in a practical system.

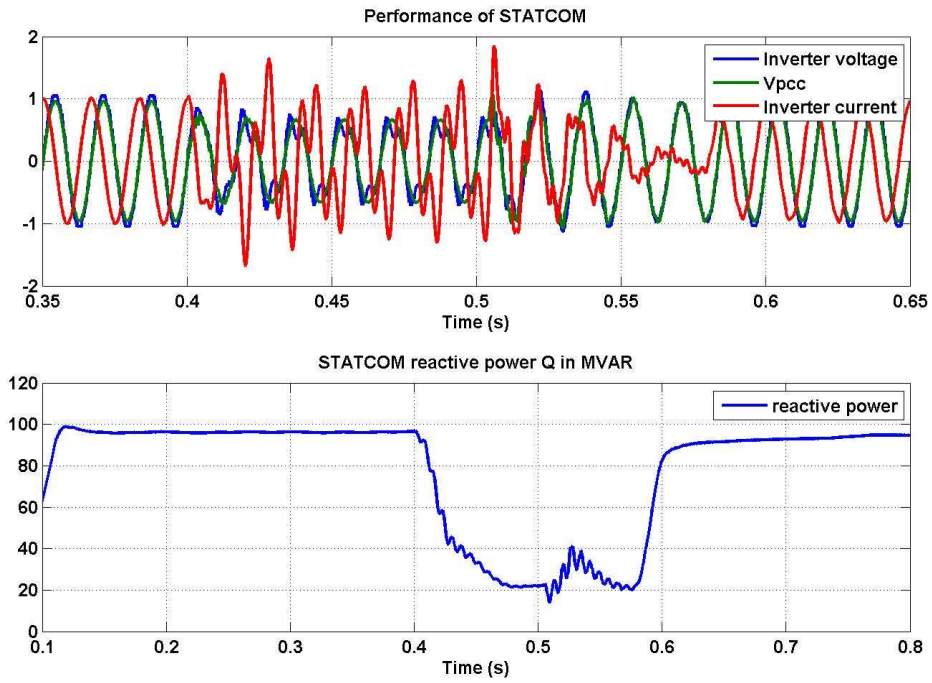


Figure 3-3 STATCOM operation in Var regulation mode under single-line to ground fault condition (a) Bus voltage, STATCOM primary 48-pulse voltage, STATCOM primary injected current, (b) STATCOM reactive power Q in MVAR

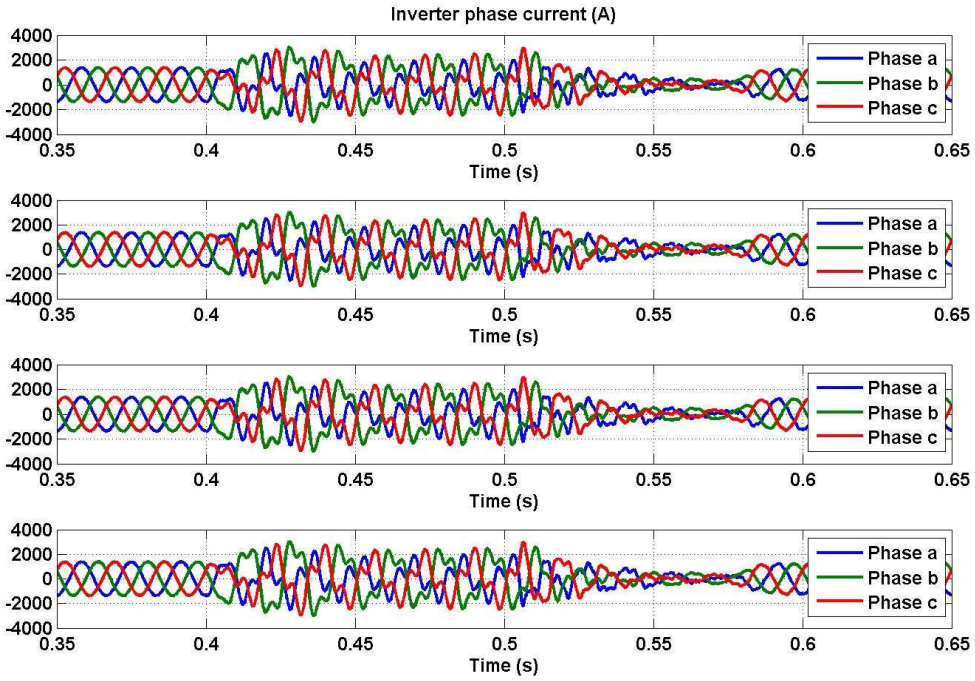


Figure 3-4 Four VSC phase currents under single-line to ground fault condition

3.1.3 STATCOM Operation under line-line fault

Figure 3-5 and Figure 3-6 show the ATATCOM operation in Var regulation mode under 6-cycle line-line fault at bus 2. Figure 3-6 shows that the VSC current, the peak value of which is 4 pu., is much higher than that under normal condition.

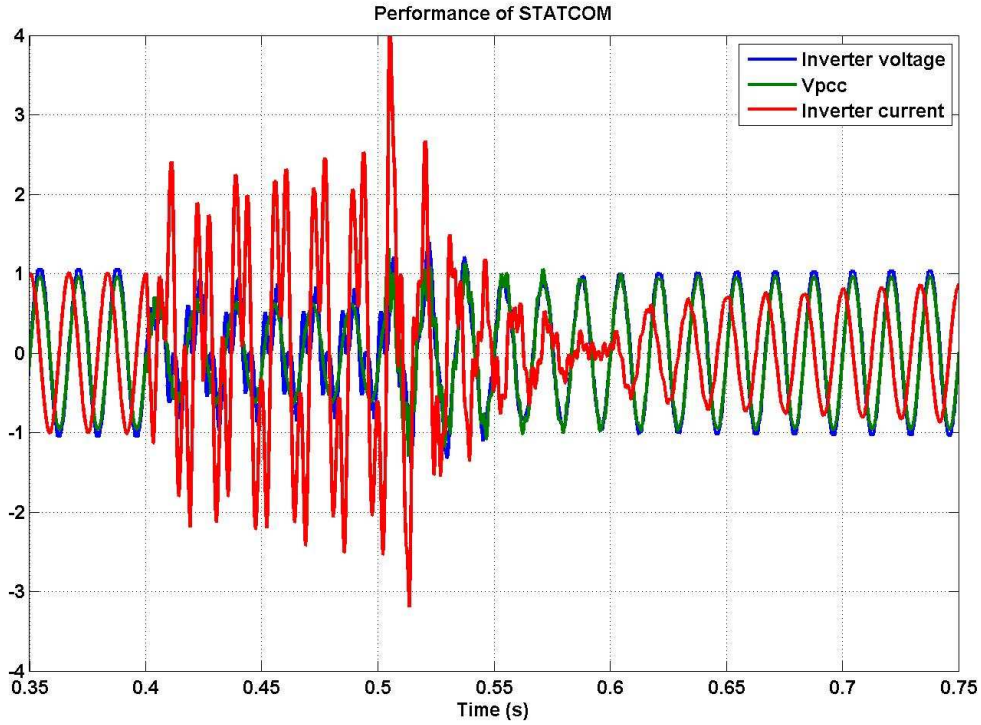


Figure 3-5 STATCOM operation in Var regulation mode under line-line fault: Bus voltage, STATCOM primary 48-pulse voltage, STATCOM primary injected current

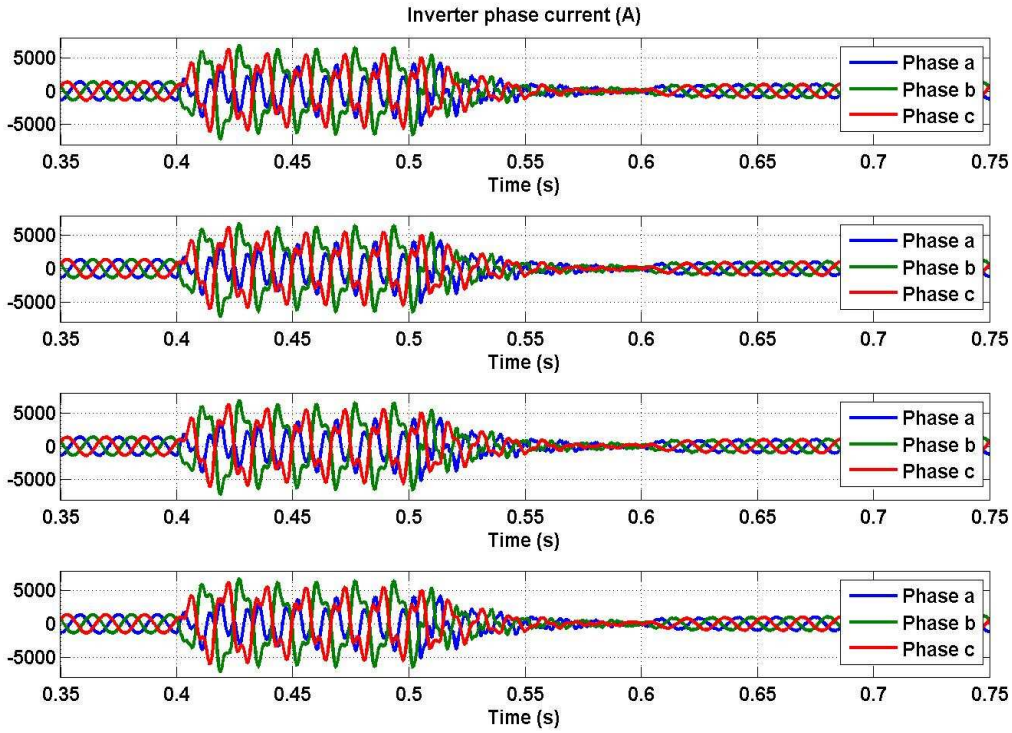


Figure 3-6 Four VSC phase currents under line-line fault

3.2 DC Capacity Design

3.2.1 DC Capacity Design

Neglecting losses (i.e. $R_s = 0$, $R_p = \infty$) and assume the steady-state condition, $\alpha = 0$, the state equation for the VSC in per-unit as:

$$p\begin{bmatrix} i_d' \\ i_q' \\ v_{dc}' \end{bmatrix} = \begin{bmatrix} 0 & \omega_b & \frac{k\omega_b}{L'} \\ -\omega_b & 0 & 0 \\ \frac{-3}{2}kC'\omega_b & 0 & 0 \end{bmatrix} \begin{bmatrix} i_d' \\ i_q' \\ v_{dc}' \end{bmatrix} - \frac{\omega_b}{L'} \begin{bmatrix} |v'| + v_{hd}' \\ v_{hq}' \\ 0 \end{bmatrix}$$

Equation 3-1

where $p = d/dt$, k is a factor between DC voltage and the amplitude (peak) of the phase-to-neutral voltage at the inverter AC-side, and α is the angle by which the inverter voltage (V_{inv}) vector leads the line/bus voltage (V_{bus}) vector.

The magnitude of negative-sequence current i_{-1}' can be calculated from Equation 3-1:

$$\left|i_{-1}'\right| = \frac{v_h'\left[1 - \frac{k^2 C'}{8L'}\right]}{L'\left[1 - \frac{k^2 C'}{2L'}\right]}$$

Equation 3-2

The simulation result of the power system with STATCOM shown in Figure 2-11 shows the impact of negative sequence and harmonic currents as under single-line to fault (SLG). In this simulation, the system is under i_q (Var or current) regulation in fully capacitive mode ($i_q^* = 1.0$ *pu*). There is 6-cycle SLG fault on bus 2. Figure 3-7 shows the RMS values of negative-sequence and 3rd, 5th, and 7th harmonics of the inverter (Inv1) phase current during the SLG fault period, corresponding to different DC capacitor C_{dc} (*pu*) design values. This result is same for Inv2, Inv3, Inv4 and STATCOM primary current, except for different scaling. Notice that from Equation 3-2, for $C' = 2L'/k^2$, i_{-1}' becomes infinite, and for $C' = 8L'/k^2$, i_{-1}' is zero – i.e. the VSC draws no negative-sequence current from the line, even under negative sequence bus voltage disturbance. The lossless assumptions used to derive Equation 3-1 are not valid for real STATCOM – thus the currents are not exactly zero. In this simulation, with $C_{dc} = 925\mu F$ *(0.78 pu)* at point A, negative-sequence current is minimum (*36.3 A rms*). Note that *1.0 pu* positive sequence rms current is *1026.5 A* and the nominal DC bus voltage is *20.6*

kV. This C_{dc} design method can be used to eliminate negative sequence and/or harmonic currents drawn from the bus under different bus voltage disturbances. Figure 3-8 shows the DC voltage spectrum of the system with $C_{dc} = 925\mu F$ under SLG fault. We can see that the negative sequence current caused by SLG is cancelled by the 2nd harmonics on DC bus voltage. As a result, the control is based on positive sequence voltage. The results with only negative sequence bus voltages are similar as given in Figure 3-7.

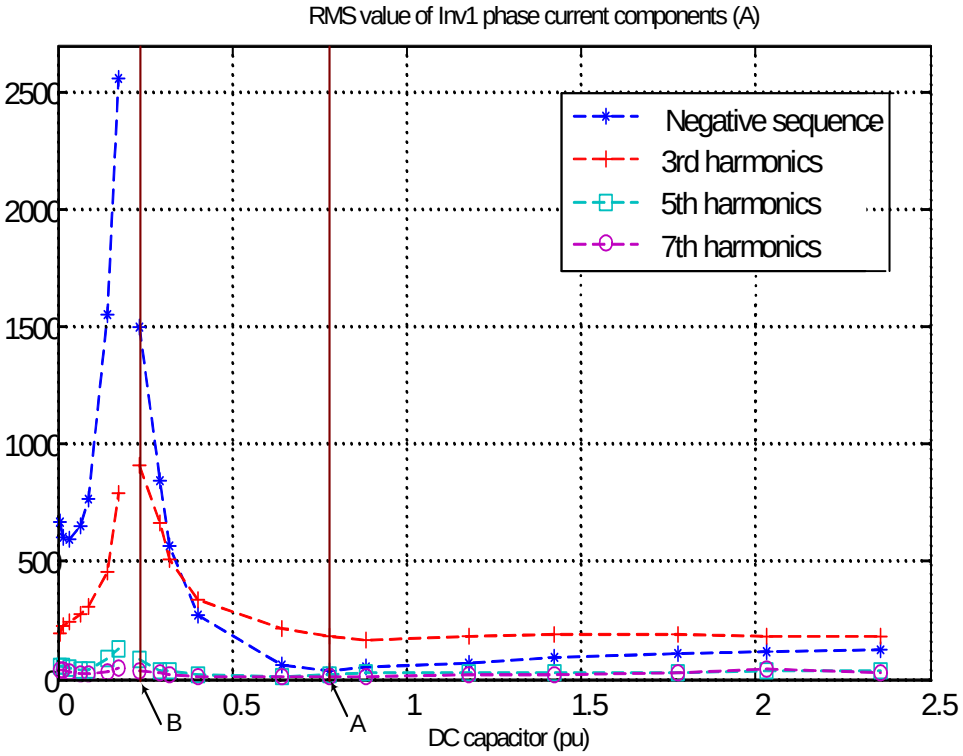


Figure 3-7 VSC phase current vs DC capacitor under SLG fault in the system

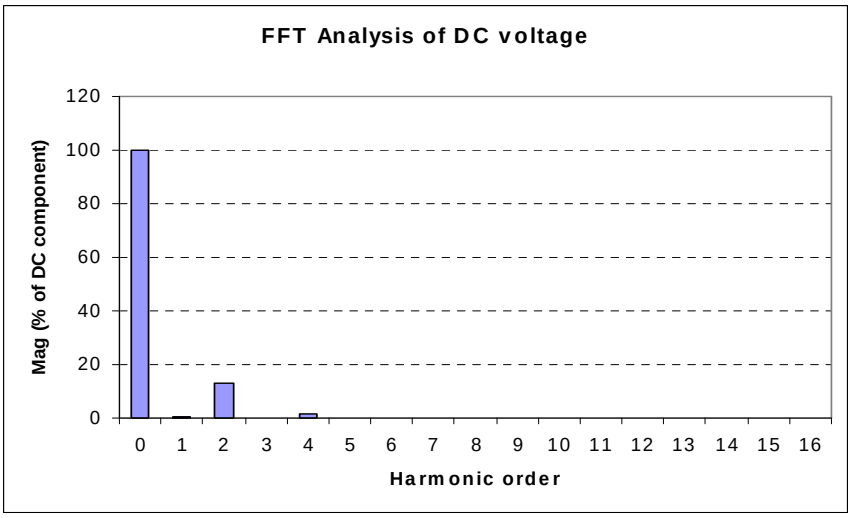


Figure 3-8 V_{dc} spectrum of the system with C_{dc} = 925μF under SLG fault

The UCC (Unit Capacitance Constant) as defined for the two STATCOM designs - point A and point B are given below. This is similar to the "inertia constant" H of the synchronous generator.

$$H(925\mu F) = \frac{\frac{1}{2}CV^2}{MVA} = 0.0009s = 0.1\text{ms}$$

$$H(3000\mu F) = \frac{\frac{1}{2}CV^2}{MVA} = 0.0031s = 3.1\text{ms}$$

The design method is based on per unit and is scalable - e.g. for a 25MVA STATCOM connected to 69kV, the optimum value of C_{dc} = *12mF* (*0.78 pu*) minimizes negative sequence current under negative sequence bus voltage distortion.

3.2.2 STATCOM Operation with Different C_{dc}

The Figure 3-9 shows the i_q reference for Var (i_q or current) regulation. At $t = 0.2s$, the i_q command step changes from fully capacitive mode ($i_q^* = 1$) to fully inductive mode ($i_q^* = -1$), and at $t = 0.4s$, it steps back to fully capacitive mode.

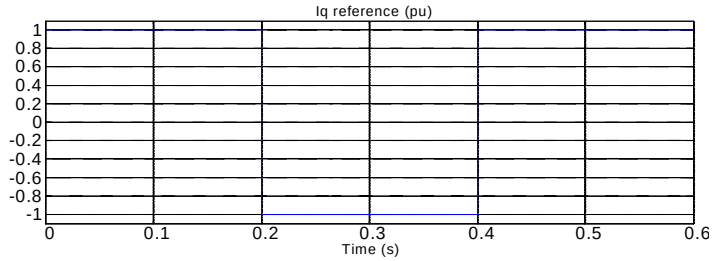


Figure 3-9 i_q *reference command to the "angle controller"*

The Figure 3-10 shows simulation results of the system with $C_{dc} = 925\mu F$ (*0.78 p.u.*) as shown by point A in Figure 3-7 under normal system condition. Note that the designed point A (in Figure 3-7) with $C_{dc} = 925\mu F$ (*0.78 p.u.*) is optimum for this STATCOM. The Figure 3-10 (a) shows good dynamic response of i_q current regulator to be within ¼ cycle by the STATCOM. The Figure 3-10 (b) shows the control angle (α) generated by the "angle controller". Note that under normal steady state conditions the control angle is very small and the control angle changes during transient conditions – such as step changes in i_q reference as shown in Figure 3-10 (a). In steady state, the three phase inverter currents are balanced and changes phase when the i_q reference changes from capacitive to inductive as shown in Figure 3-10 (c). Note that the inverter currents are within the VSC over-current limits during the i_q reference step changes. The other inverter (Inv2-Inv4) currents are similar.

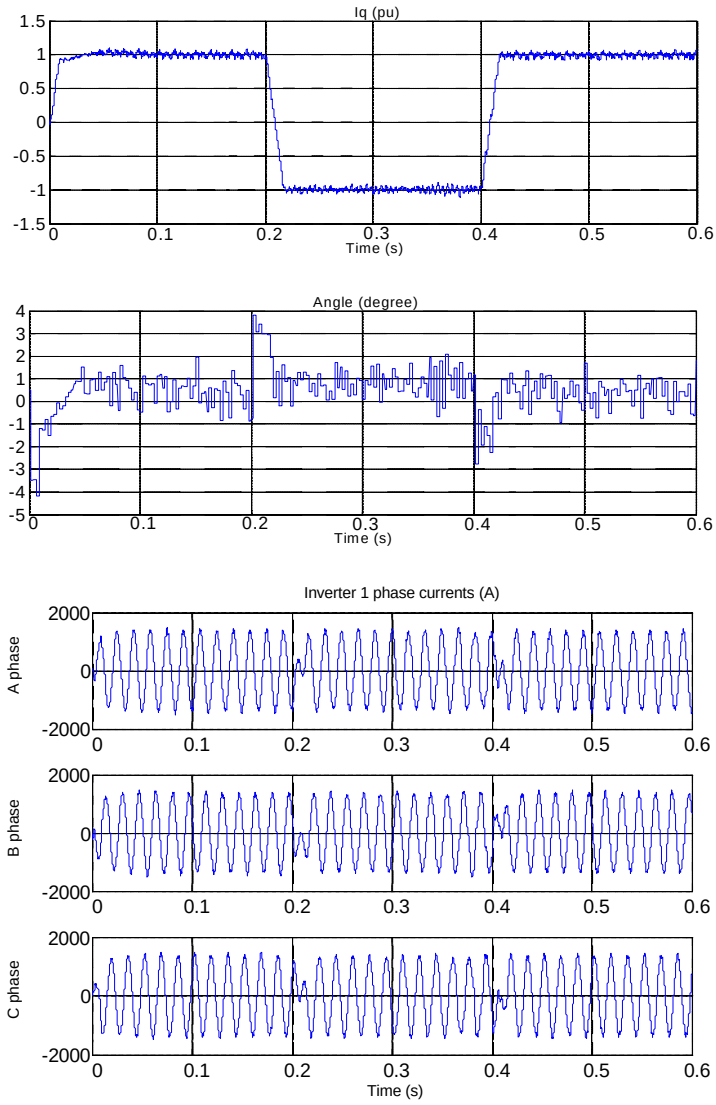


Figure 3-10 Simulation results C_{dc} = 925μF (0.78 p.u.), (a) i_q reactive current of the STATCOM (b) Control angle α from "angle controller" (c) inverter 1 phase current

System simulation was repeated with a non-optimum designed point B (in Figure 3-7) with C_{dc} = *3000μF* (*0.24 p.u.*) for the STATCOM under normal system conditions. This is mainly to compare the impact of the C_{dc} design on the inverter currents and STATCOM reactive current i_q response.

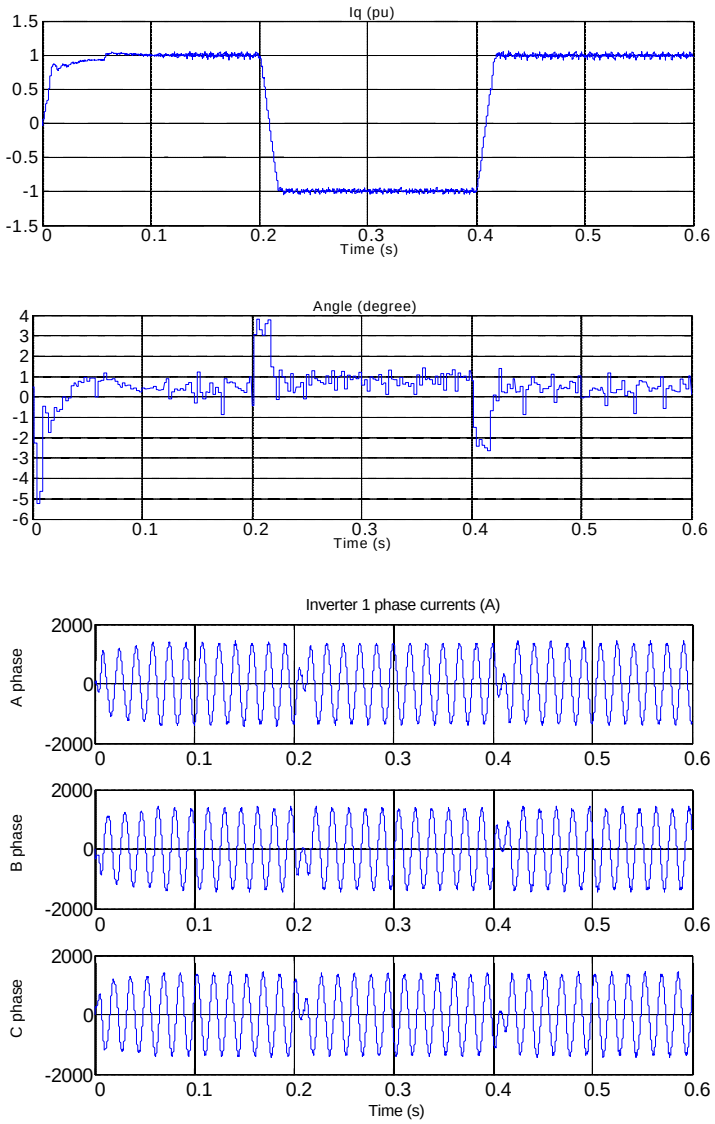


Figure 3-11 Simulation results Cdc = 3000μF (0.24 p.u.), (a) iq reactive current of the STATCOM (b) Control angle α from "angle controller" (c) inverter 1 phase current

The Figure 3-11 (a) shows good dynamic response of i_q current regulator to be within ¼ cycle by the STATCOM. The i_q step change response is almost same as in Figure 3-10 (a) with optimum value of $C_{dc} = 925\mu F$ (*0.78 p.u.*). This result shows importantly that C_{dc} does not affect the current response of the STATCOM under normal condition. The Figure 3-11 (b)

shows the control angle (α) generated by the "angle controller". The perturbations in the control angle (α) are similar to that in Figure 3-10 (b), and are also independent of the C_{dc} design point A or point B. In steady state, the three phase inverter currents are balanced and changes phase when the i_q reference changes from capacitive to inductive as shown in Figure 3-11 (c). Note that the inverter currents are also within the VSC over-current limits during the i_q reference step changes, as in Figure 3-10 (c) with $C_{dc} = 925\mu F$ (*0.78 pu*). The other inverter (Inv2-Inv4) currents are similar. The results in Figure 3-10 (c) and Figure 3-11 (c) show that the inverter currents are independent of C_{dc} under normal system conditions – i.e. When there is only positive sequence bus voltage.

The Figure 3-12 and Figure 3-13 show the STATCOM with different C_{dc} response to the same 6-cycle SLG at bus 2. The Figure 3-12 shows the system bus voltage, i_q and Inv1 phase currents of the STATCOM with $C_{dc} = 925\mu F$ (*0.78 p.u.*) as shown by point A in Figure 3-7. The Figure 3-13 shows the system bus voltage, i_q and Inv1 phase currents of the STATCOM with $C_{dc} = 3000\mu F$ (*0.24 p.u.*) as shown by point B in Figure 3-7. The SLG fault is on phase A, so as shown in Figure 3-12(a) and Figure 3-13 (a), the bus voltage V_a sags, but V_b and V_c are not affected. Comparing Figure 3-12(c) and Figure 3-13 (c), the Inv1 peak current with $C_{dc} = 3000\mu F$ during SLG fault is almost twice that of the VSC operation under normal system conditions (i.e. without fault or with only positive sequence bus voltage). This will result in over-current in the VSC and trip of the STATCOM to protect the semiconductor devices. However, the peak current of the VSC with $C_{dc} = 925\mu F$ does not increase that much (as shown in Figure 3-12). This simulation result verifies the VSC current component analysis shown in Figure 3-7.

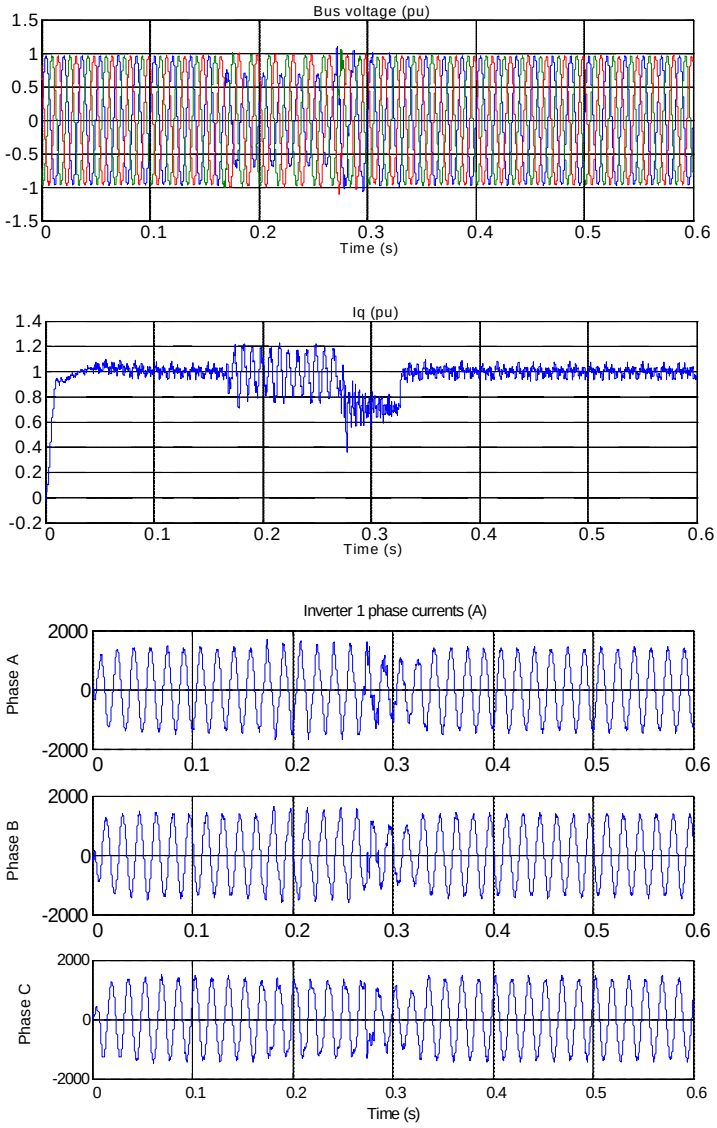


Figure 3-12 Simulation results C_{dc} = 925μF under SLG on phase A, (a) Bus voltage (b) reactive current i_q (c) inverter 1 phase current

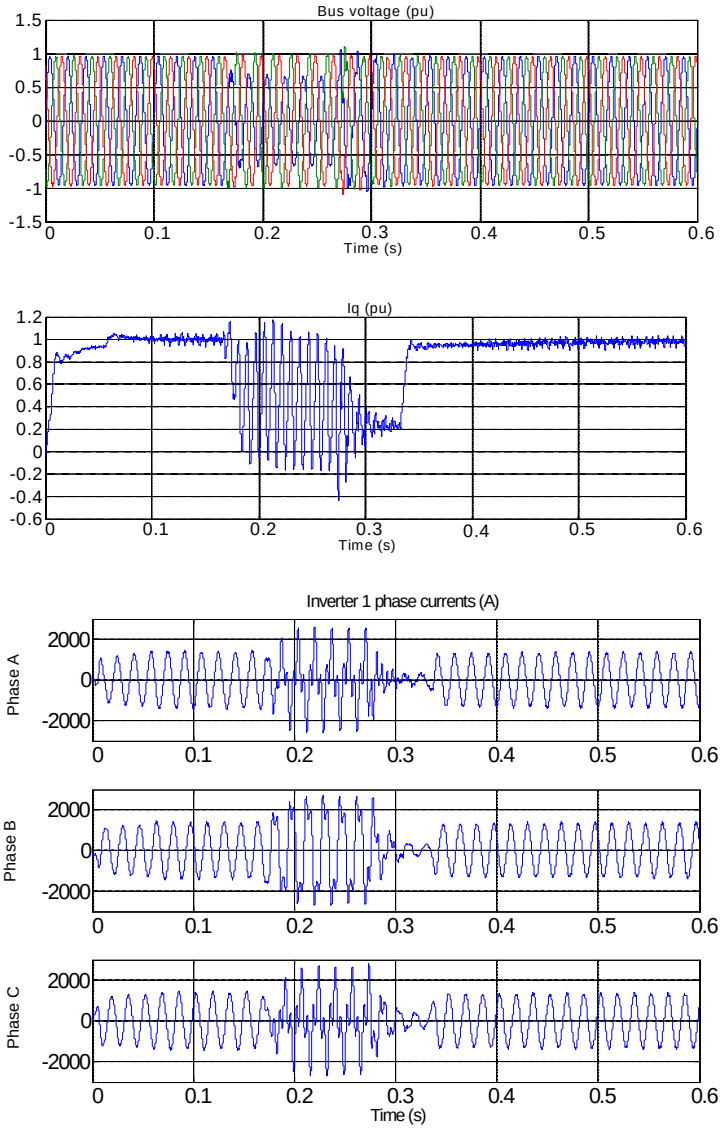


Figure 3-13 Simulation results C_{dc}=3000μF under SLG on phase A, (a) Bus voltage (b) reactive current i_q (c) Inv1 phase current

CHAPTER 4 STATCOM OPERATION UNDER SYSTEM FAULTS – PROPOSED SOLUTIONS

The C_{dc} design method poses another problem. The Figure 4-1 show the RMS values of Inv1 phase current in system with three-phase fault and line-line fault on bus 2. The STATCOM is operating under i_q (Var) regulation in fully capacitive mode ($i_q^* = 1$). In Figure 3-7 with $C_{dc} = 925\mu F$ ($0.78\ pu$) –at point A, the negative-sequence current has the minimum value, equal to *36.3A*. However, as shown in Figure 4-1, with the same value of C_{dc}, the negative-sequence currents are *314.2A* and *202.7A* respectively, under three-phase fault and line-line fault. Comparing Figure 3-7 and Figure 4-1, it is seen that the designed C_{dc} value to eliminate the negative-sequence current in system with SLG is not the optimum C_{dc} value for minimum negative sequence (and other harmonic currents) in system with other types of fault, and vice versa. In other words, the optimum design of C_{dc} depends on the type of bus voltage distortion. The VSC current control strategy developed in the next section can reduce the harmonic currents practically with any value of C_{dc} design, under all types of bus voltage distortions.

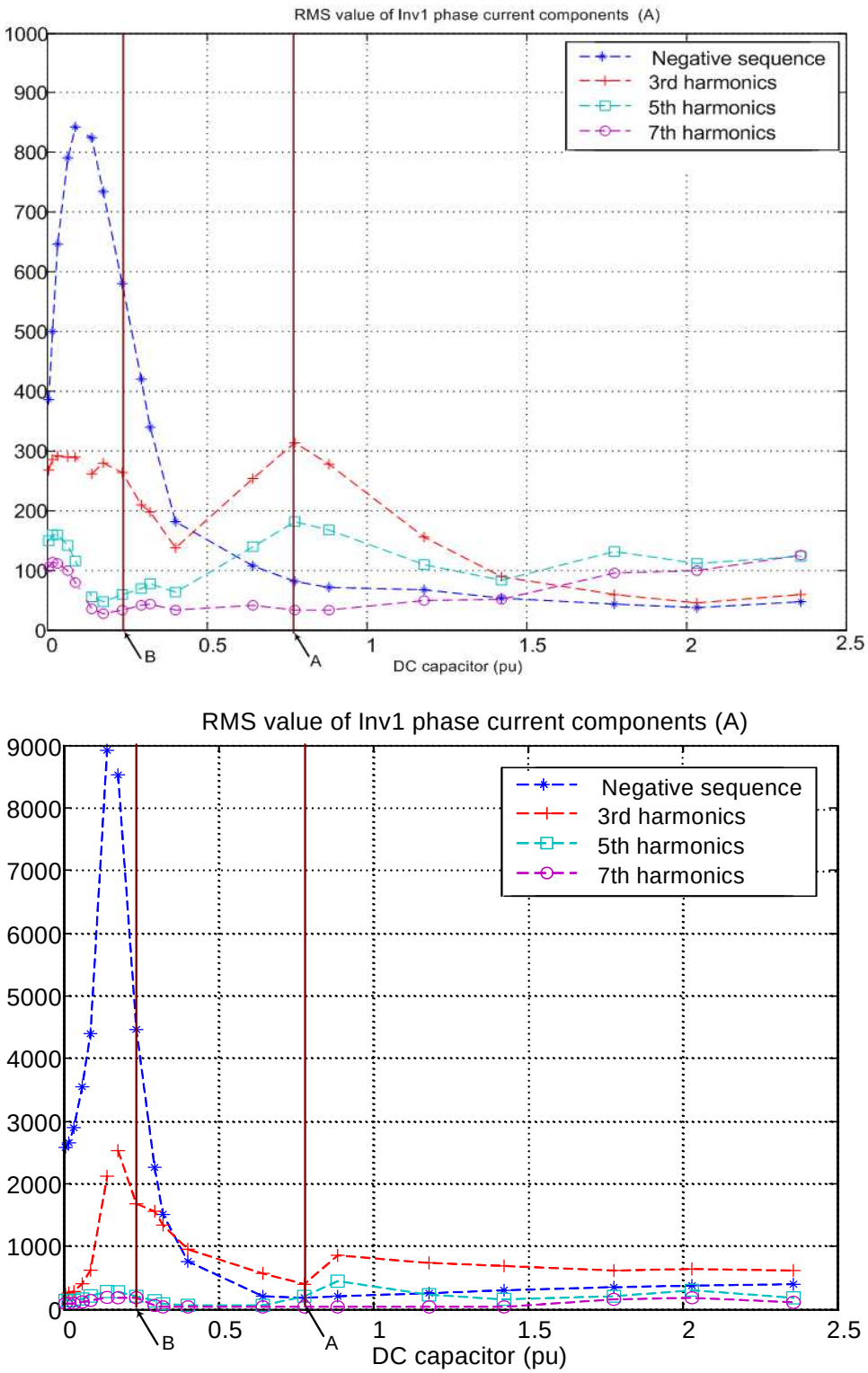


Figure 4-1 VSC Inv1 phase current vs dc capacitor under (a) three phase fault (b) line-line fault

4.1 Current Control ("Emergency PWM")

In the current control, the VSCs individually detect and self-implement PWM switching to control their phase (VSC pole and device) currents within predetermined limits, as illustrated in the Figure 4-2. Each VSC will ensure that its over-current limit is not reached during and after the system fault, and under any bus voltage condition (including negative sequence and harmonics). This control strategy enables the STATCOM to remain online during and recovering from a system fault, when its VAR support is required the most. Further, this control strategy is independent of the value of C_{dc} design for the VSC. The C_{dc} can be designed to minimize impact of negative sequence bus voltage, whereas current control can be used to minimize negative sequence and harmonic currents under all other types of bus disturbances (such as harmonic bus voltages).

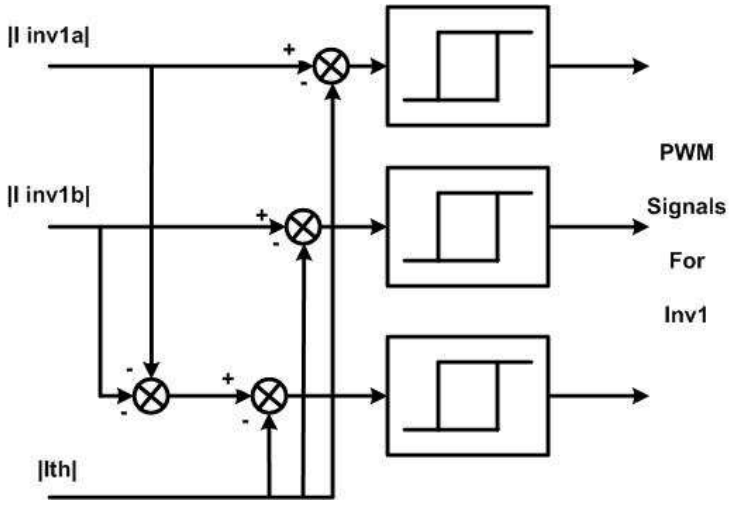


Figure 4-2 Controller to generate PWM trigger signal for Inv1

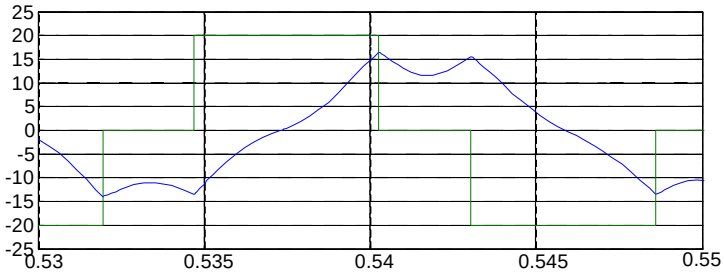


Figure 4-3 VSC phase voltage and current without current control during fault

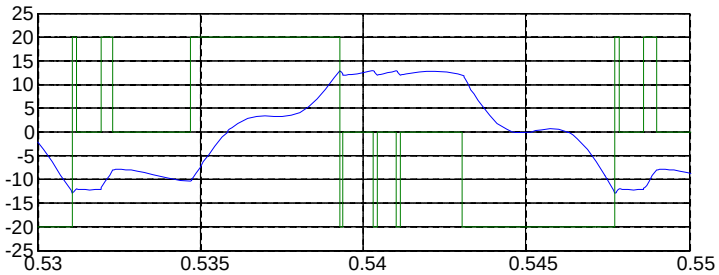


Figure 4-4 VSC phase voltage and current with current control during fault

The introduction of the proposed method to suppress the currents up to the converter limits is investigated in the following. The Figure 4-3 shows the VSC phase output voltage and current without current control implementation during a system fault. As the switching frequency is fixed to the line frequency the controller is unable to respond satisfactory and reject this perturbation. The phase (GTO device) current rapidly increases at the onset of the fault and over-current of the VSC devices happens. The current control concept is illustrated in the Figure 4-4. By introducing the emergency PWM, we allow the converter to switch faster within the fault to suppress the current rise and keep the converter alive with in safe operating area. It is seen that the VSC phase current is controlled such that the STATCOM still delivers required reactive power (or current) during the fault. The extra switching in the

VSC will result in higher losses during this period. However, the priority is to keep the STATCOM online to support bus voltage during and recovering from a system fault.

The Figure 4-5, Figure 4-6 and Figure 4-7 show the system under different faults and with the proposed current control, the STATCOM controller generates both positive (V_{inv_pos}) and negative sequence voltage (V_{inv_neg}) in response to dynamically changing system voltage, to control negative sequence bus current (I_{inv_neg}) and I_{inv}.

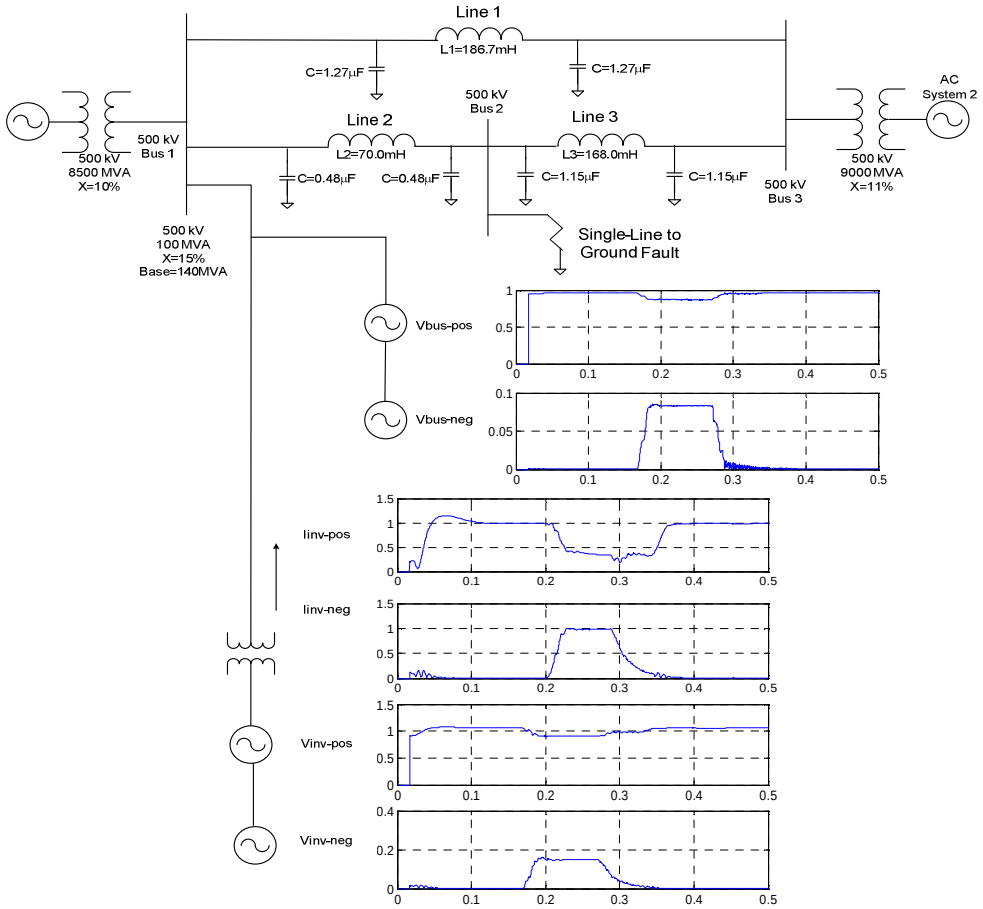


Figure 4-5 System under SLG fault and with proposed current control

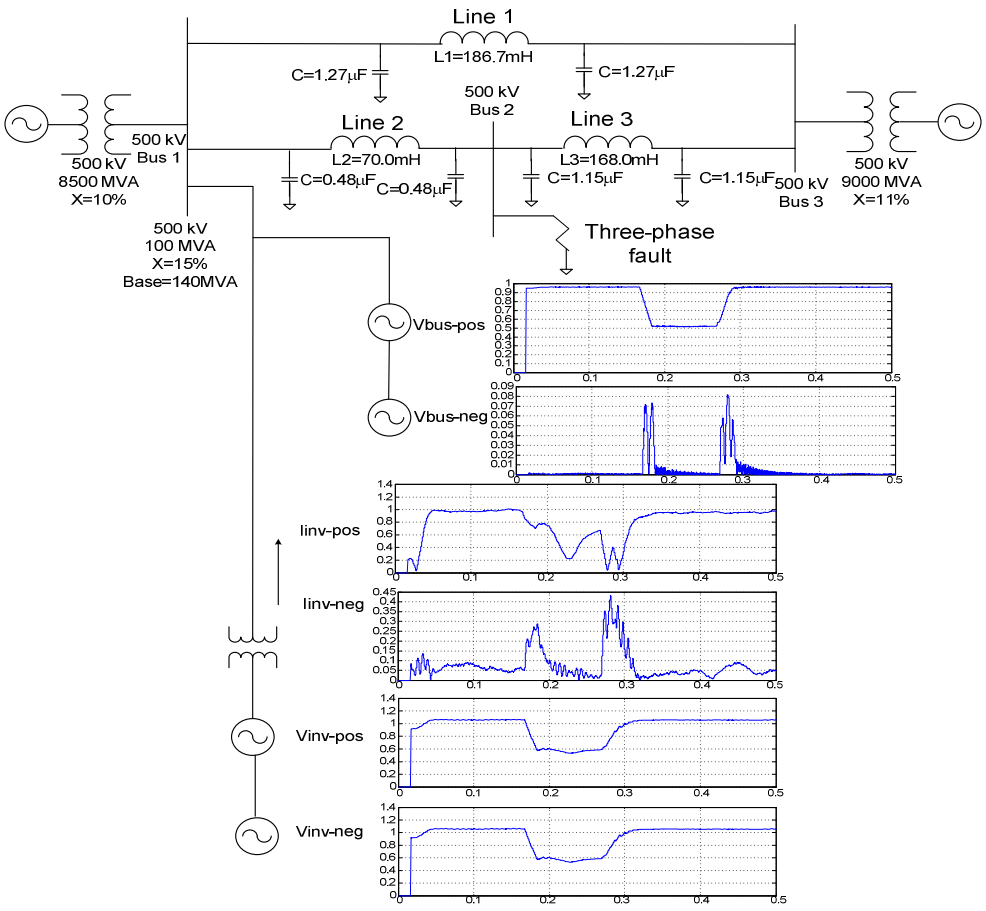


Figure 4-6 System under three phase fault and with proposed current control

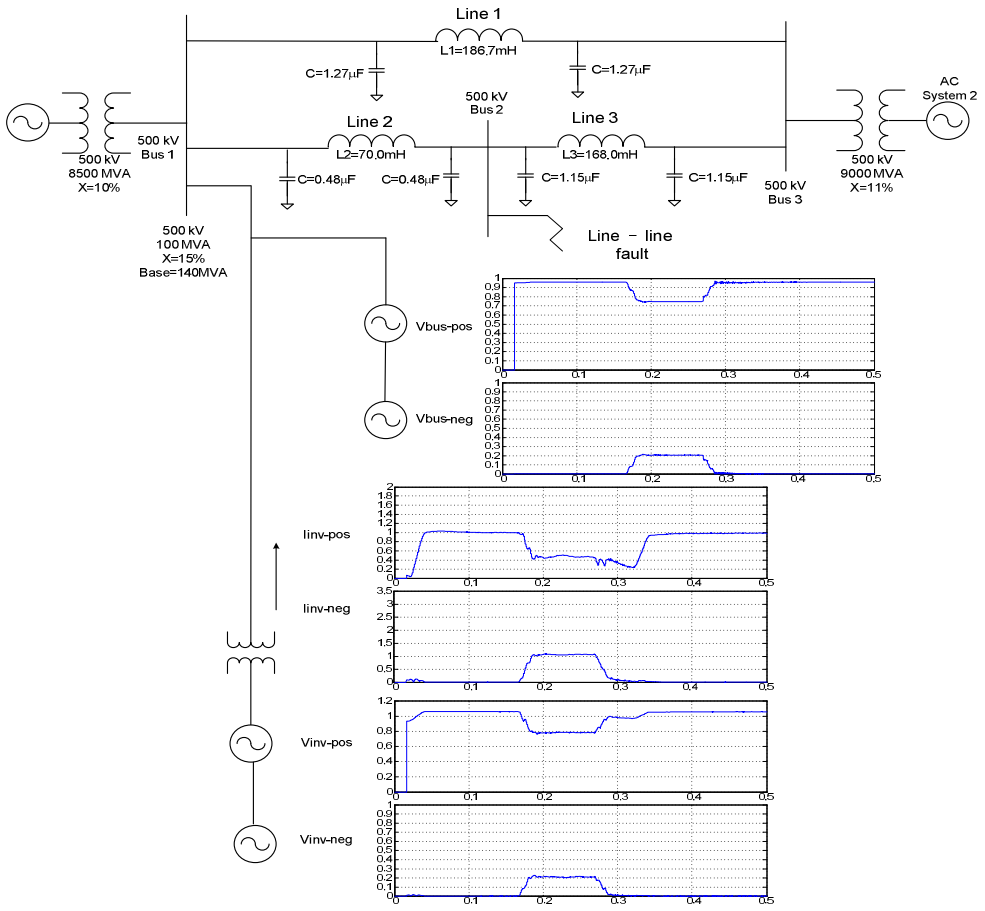


Figure 4-7 System under line-line fault and with proposed current control

The Figure 4-8, Figure 4-9 and Figure 4-10 show the VSC Inv1 phase current negative-sequence component of the system under SLG fault, three-phase fault and line-line fault with and without the current control strategy. In each figure, the "*" represents the RMS value of Inv1 current without current control, and the "+" represents RMS value of Inv1 current with the current control strategy. In all three cases, corresponding to most C_{dc}, the current controller reduces the negative sequence current amplitude.

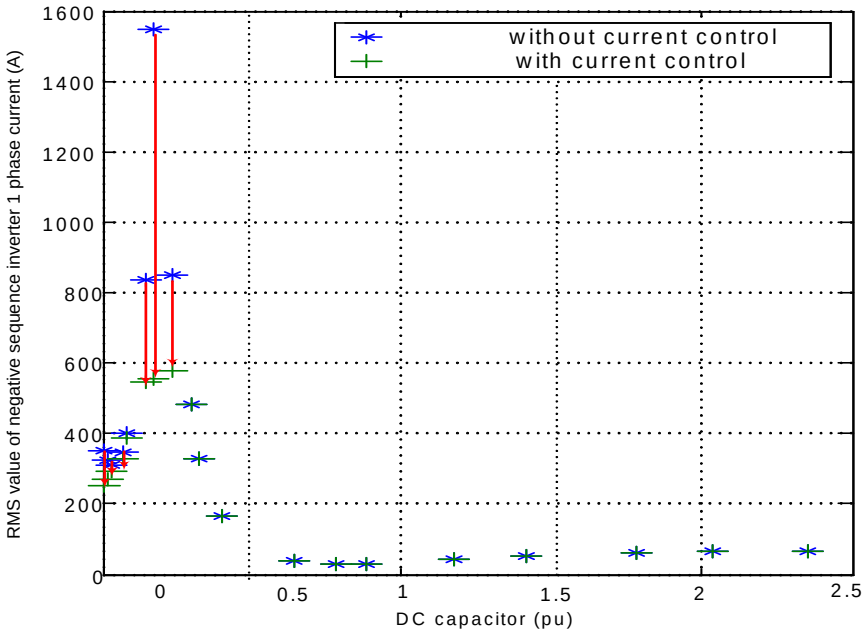


Figure 4-8 VSC Inv1 phase current negative-sequence component vs DC capacitor with and without current control strategy under SLG fault

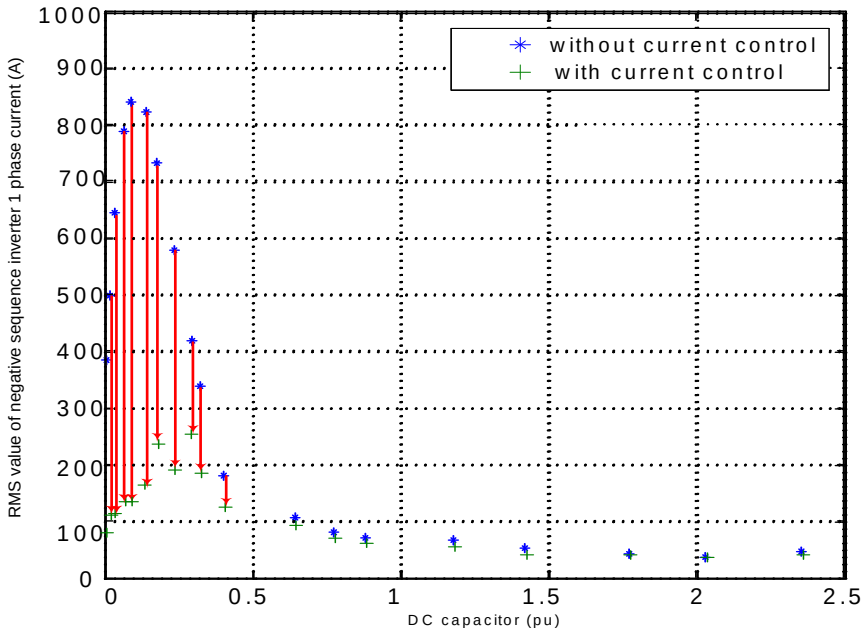


Figure 4-9 VSC Inv1 phase current negative-sequence component vs DC capacitor with and without current control strategy under three-phase fault

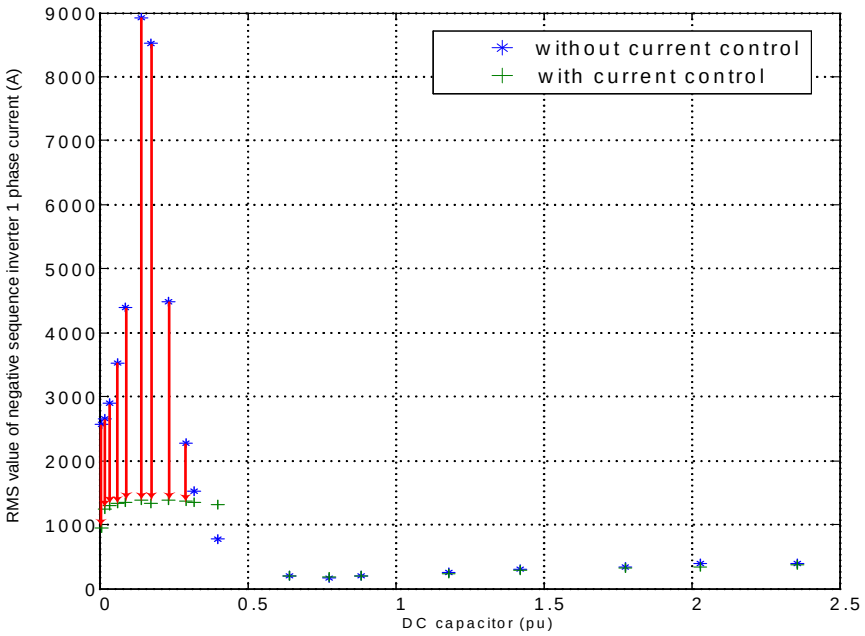


Figure 4-10 VSC Inv1 phase current negative-sequence component vs DC capacitor with and without current control strategy under line-line fault

In this current control strategy, since the total VSC phase current is kept within a predetermined limit, therefore individually the negative sequence current and harmonic currents are not totally eliminated. For certain DC capacitor values, the VSC over-currents generated by the system are lower than the predetermined limit, and hence the current controller does not trigger the PWM signals.

4.2 Instantaneous PLL [43]

The basic configuration of the PLL system is shown in Figure 4-11. The phase voltages V_a, V_b, V_c, are obtained from sampled line to line voltages. As shown in Figure 4-12, these stationary reference frame voltages are transformed to voltages V_α, V_β by Clark

transformation (Equation 4-1) and then voltages V_d, V_q (a frame of reference synchronized to the utility frequency) by Park transformation (Equation 4-2).

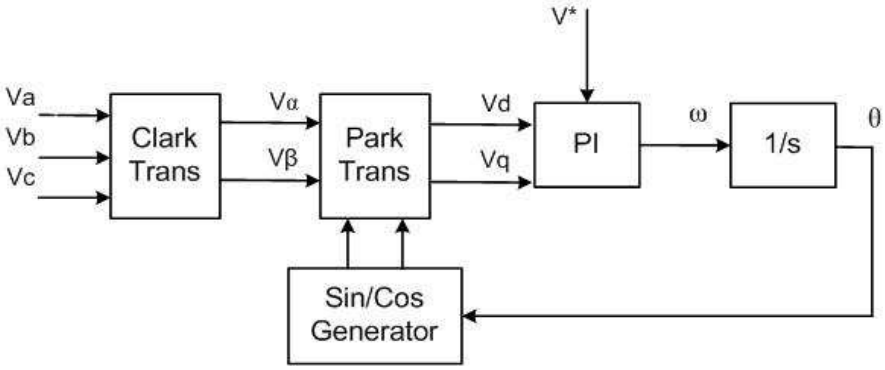


Figure 4-11 The basic three-phase PLL structure

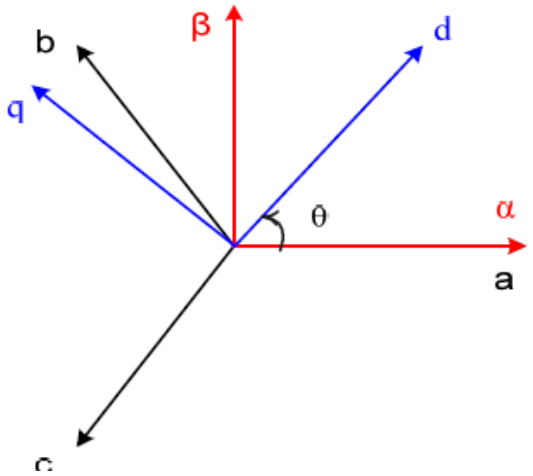


Figure 4-12 Transformation from three-phase two-phase

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}$$

Equation 4-1

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix}$$

Equation 4-2

The angle θ used in these transformations is obtained by integrating a frequency command ω, in other words, by synchronizing the PLL rotating reference frame and the utility voltage vector. If the frequency command ω is identical to the utility frequency, the voltages V_d, and V_q appear as DC values depending on the angle θ.

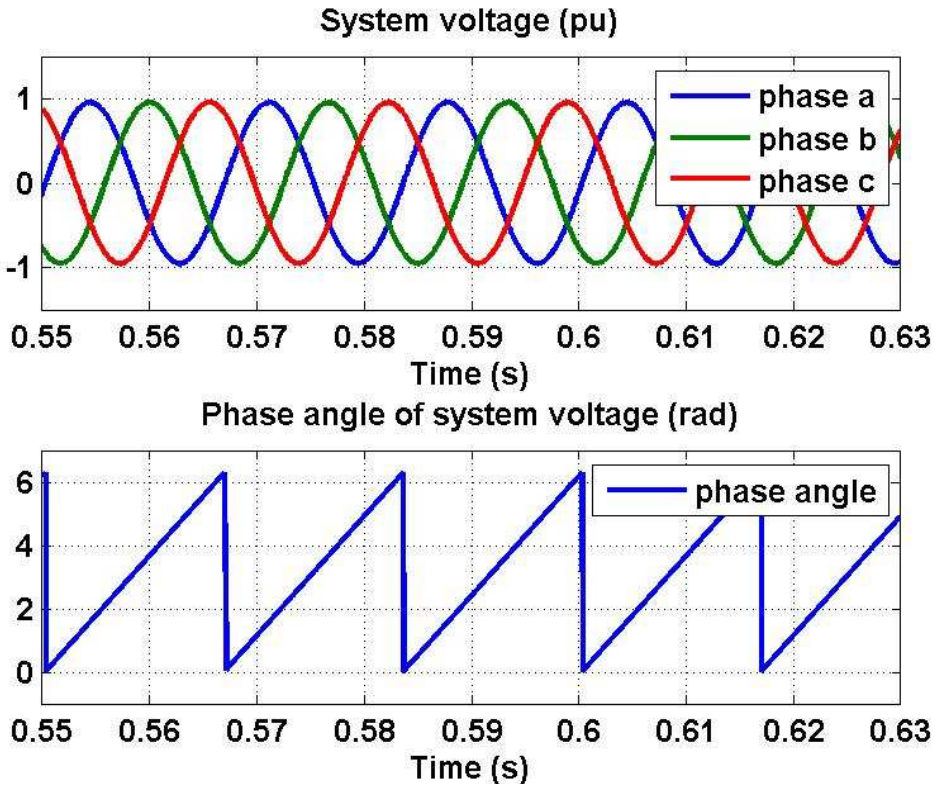


Figure 4-13 Phase angle of the system voltage from PLL

In the given method, a PI regulator is used to obtain the value of θ (or ω) which drives the feedback voltage V_d to a commanded value V_d*. In other words, the regulator results in a

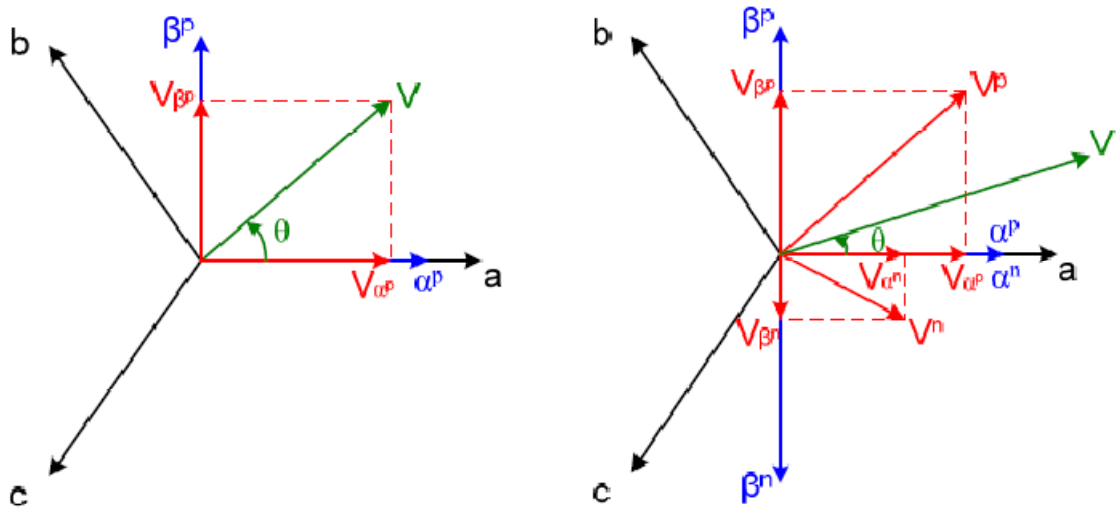
rotating frame of reference with respect to which the transformed voltage V_d, has the desired DC value V_d*. The frequency of rotation of this reference frame is identical to the frequency of the utility voltage. Figure 4-13 shows the three-phase system voltage and the phase angle of system voltage from PLL.

4.2.1 Instantaneous PLL

In Figure 4-14, the effect of negative sequence on voltage phase is investigated. V_α and V_β are in phase with and orthogonal to V_a. Under normal condition, the voltage only involves positive sequence. The voltage and phase (θ) are shown in Figure 4-14 (a). V_α and V_β can be presented as follows:

$$v_\alpha = v^p cos\theta^p$$
$$v_\beta = v^p sin\theta^p$$

Equation 4-3



(a) *(b)*

Figure 4-14 Voltage and phase under (a) normal condition, (b) system fault

When there is system fault or voltage disturbance, the phase is determined by positive sequence and negative sequence voltages, as shown is Figure 4-14 (b). V_α and V_β can be presented as follows:

$$v_\alpha = v^p cos\theta^p + v^n cos\theta^n$$
$$v_\beta = v^p sin\theta^p - v^n sin\theta^n$$

Equation 4-4

In the second step of normal PLL, the transformation matrix is decided by three-phase phase order. As a result, the PLL, based on the positive-sequence bus voltage, cannot response to dynamical changing in negative-sequence bus voltage due to system faults.

The "Instantaneous PLL" is shown in Figure 4-15. Three-phase bus voltage (V_a, V_b, V_c), including positive-sequence and negative-sequence voltage, is transformed to two-phase voltage (V_α, V_β) in $\alpha\beta$ stationary coordinate (as Equation 4-1). The phase angle (θ') is obtained from inverse tangent of V_β / V_α. The angel θ from the low pass filter, which is the angle of voltage vector in $\alpha\beta$ coordinate, is regard as phase angle of the system. The "Instantaneous PLL" does not depend on three-phase phase order, so negative-sequence voltage is considered in this method. Over-current due to negative sequence generated during system faults can be prevented.

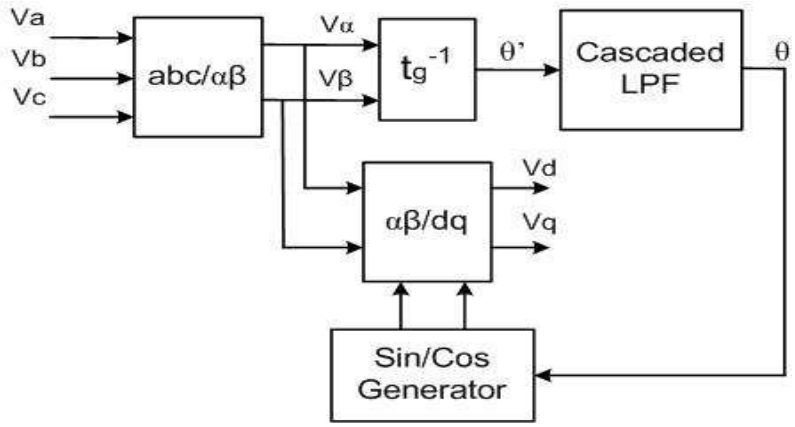


Figure 4-15 Instantaneous PLL structure

4.2.2 Simulation results

Figure 4-17 and Figure 4-18 show the STATCOM operation in voltage regulation mode with the voltage reference shown in Figure 4-16. The system in Figure 4-17 implements normal PLL and the system in Figure 4-18 implements "Instantaneous PLL". The STATCOM 48-pulse voltage waveforms of both systems are same as shown in Figure 4-17 (a) and Figure 4-18 (a).

Table 4-1 RMS values of bus voltage of system with PLL

Period	Normal PLL (p.u)	Instantaneous PLL (p.u)
0.2-0.25 second	0.7835	0.7861
0.3-0.35 second	0.7747	0.7766
0.4-0.45 second	0.7659	0.7707
0.5-0.55 second	0.6001	0.6008
0.6-0.65 second	0.7645	0.7644

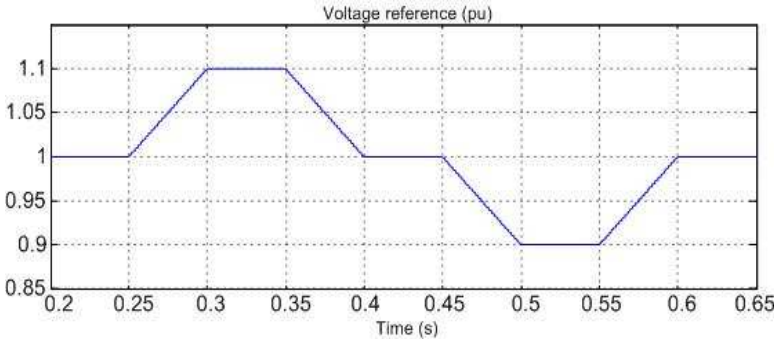


Figure 4-16 The bus voltage regulation reference signal for voltage regulation mode

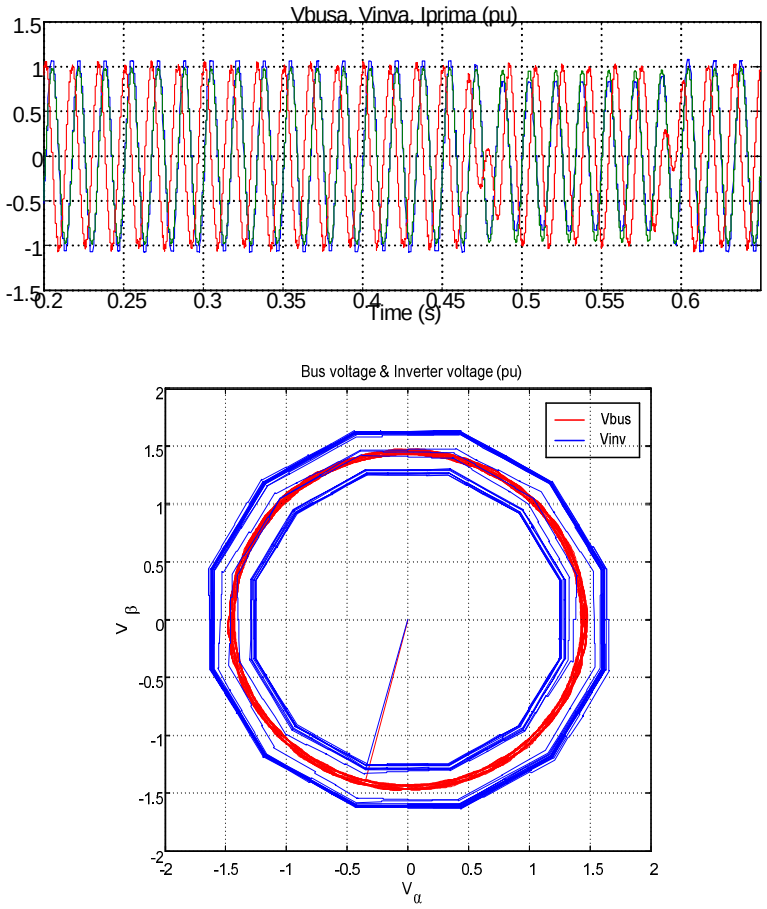


Figure 4-17 System with normal PLL, operating in voltage regulation. Phase A bus voltage, STATCOM primary 48-pulse voltage in (a) time domain, (b) αβ stationary coordinate

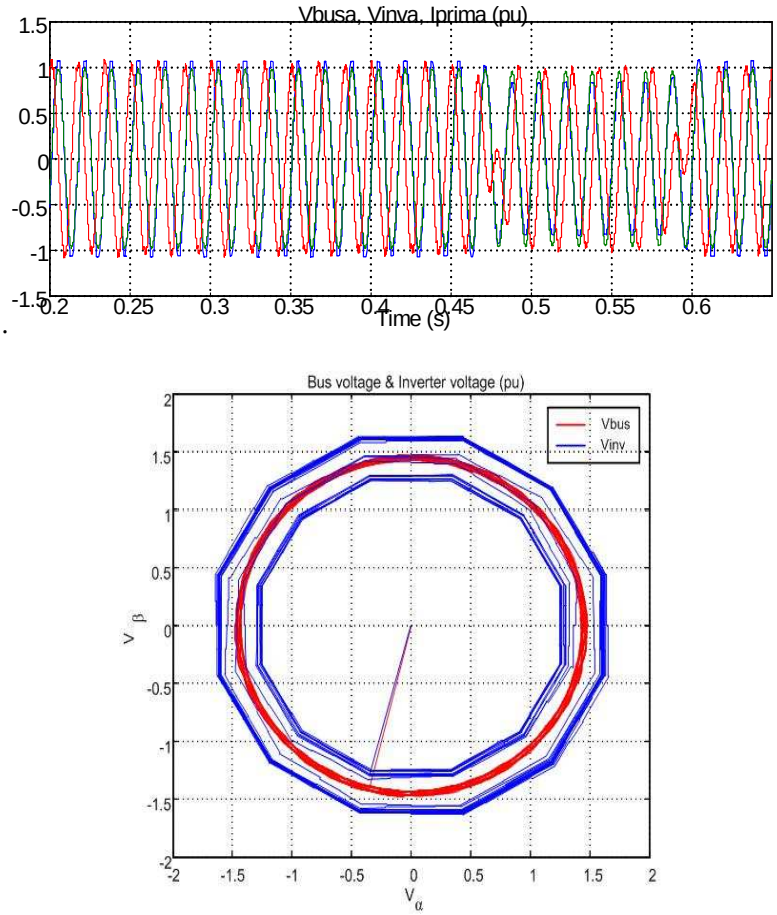


Figure 4-18 System with Instantaneous PLL, operating in voltage regulation. Phase A bus voltage, STATCOM primary 48-pulse voltage in (a) time domain, (b) αβ stationary coordinate

In Figure 4-17 (b) and Figure 4-18 (b), in *αβ* stationary coordinate, inverter voltages in both systems follow voltage reference to regulate bus voltage. Table 4-1 lists the RMS values of bus voltage of both systems. The performance of both PLL in normal operation of the power system can be hardly distinguished.

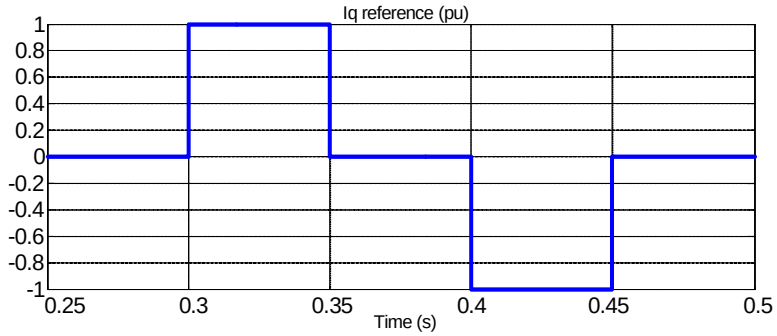


Figure 4-19 The reference signal for the i_q or VAR regulation mode

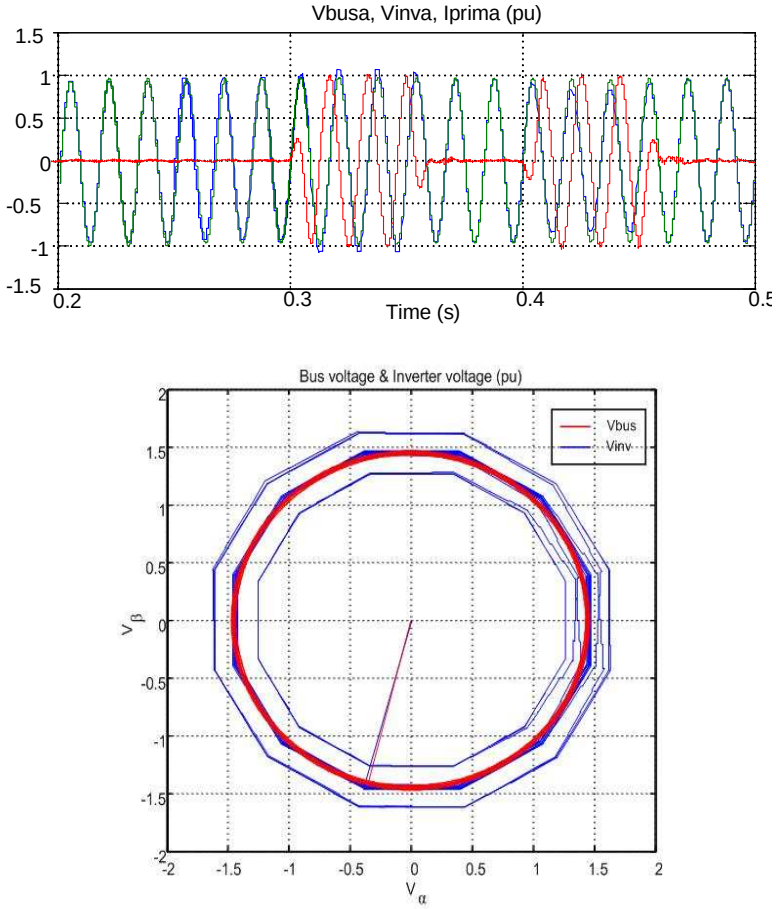


Figure 4-20 System with normal PLL, operating i_q regulation. Phase A bus voltage, STATCOM primary 48-pulse voltage (pu) in (a) time domain (b) αβ stationary coordinate

Figure 4-20 and Figure 4-21 show the STATCOM operation in i_q regulation mode with the i_q reference shown in Figure 4-19. The system in Figure 4-20 implements normal PLL and the system in Figure 4-21 implements "Instantaneous PLL". In Figure 4-20 (a) and Figure 4-21 (a), during $T = 0.3s$ to $0.35s$, the STATCOM operates in fully capacitive mode, and the inverter current is leading the bus voltage. During $T = 0.4s$ to $0.45s$, the STATCOM operates in fully inductive mode, the inverter current is lagging the bus voltage. The bus voltages of both systems are same. In Figure 4-20 (b) and Figure 4-21 (b), in $\alpha\beta$ stationary coordinate, inverter voltages in both systems follow iq reference to regulate bus voltage.

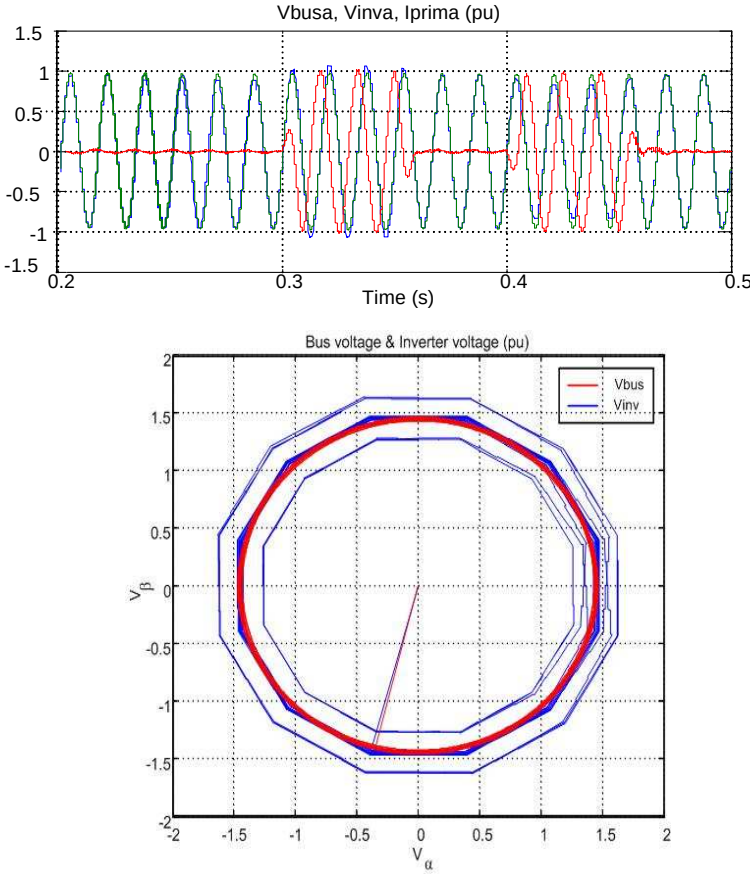


Figure 4-21 System with Instantaneous PLL, operating i_q regulation. Phase A bus voltage, STATCOM primary 48-pulse voltage (pu) in (a) time domain (b) αβ stationary coordinate

By comparing the simulation of the system implementing normal PLL and "Instantaneous PLL" with voltage regulation mode (Figure 4-17 and Figure 4-18) and i_q regulation mode (Figure 4-20 and Figure 4-21) under normal condition, we can see that, "Instantaneous PLL" does not change the system performance under normal condition, which means normal PLL and "Instantaneous PLL" can switch to each other for a stable system under normal condition.

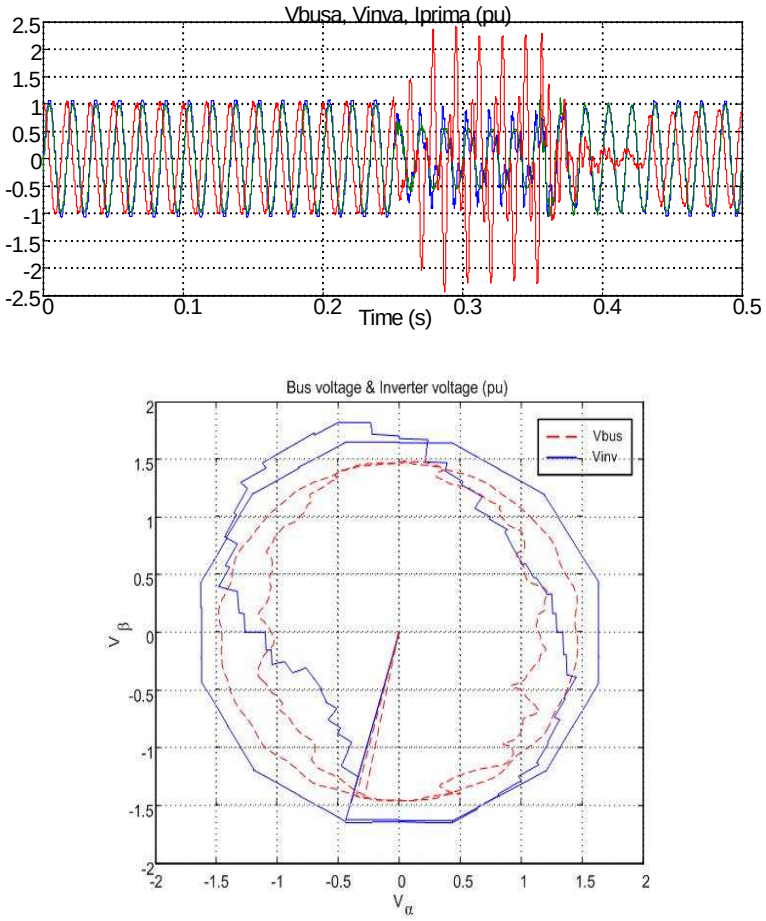


Figure 4-22 System with normal PLL, under SLG fault. Phase A bus voltage and STATCOM primary 48-pulse voltage in (a) time domain, (b) αβ stationary coordinate

Figure 4-22 and Figure 4-23 show the STATCOM operation in i_q regulation mode with

normal PLL and IPLL under 6-cycle SLG fault at bus 2.

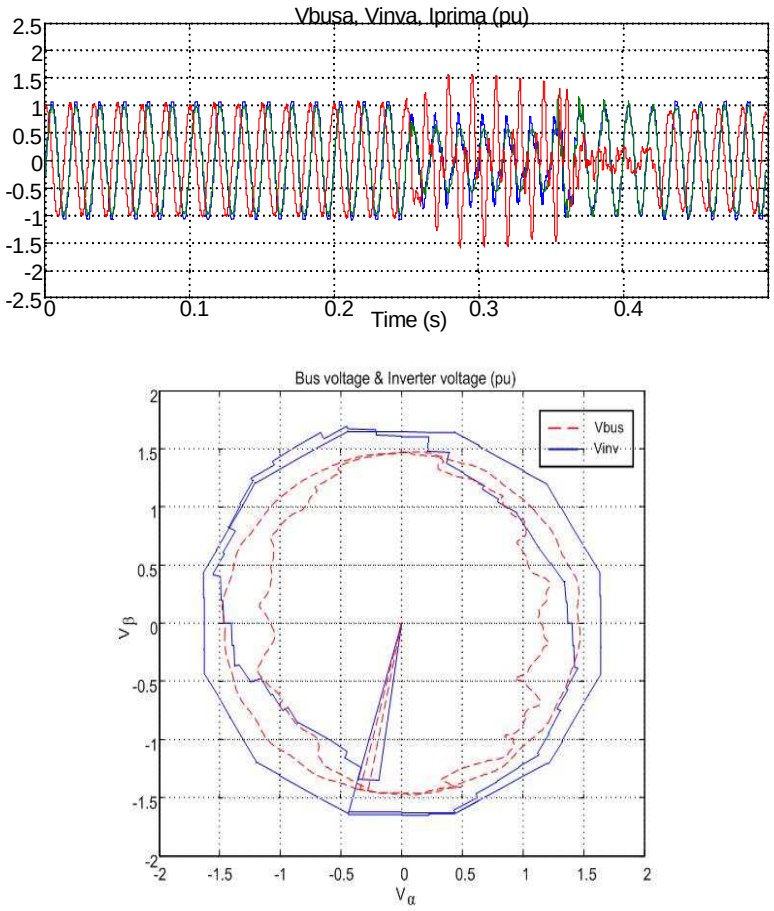


Figure 4-23 System with Instantaneous PLL, under SLG faul. Phase A bus voltage and STATCOM primary 48-pulse voltage in (a) time domain, (b) αβ stationary coordinate

Figure 4-22 (a) shows that the VSC currents exceed 2 p.u., which is higher than that of system with nominal PLL in Figure 4-21 (a), and will result in over-current and trip to protect the VSC devices in a practical system. Bus voltage and inverter voltage during the period from one cycle before the SLG fault happens to one cycle after the SLG fault happens in *αβ* stationary coordinate is destroyed because of the fault. Figure 4-23 (a) shows that the VSC current is limited within *1.5 p.u.* and will allow the STATCOM to be online during and

recovering from SLG fault. Compared with Figure 4-21(b), the voltage in αβ stationary coordinate is not distorted that much because of the IPLL implementation. In Figure 4-24, the voltage phases of system with normal PLL and IPLL are shown. During SLG, we can see IPLL tracks the real phase correctly and the oscillation on the phase signal is the signal that the controller needs to regulate the system voltage.

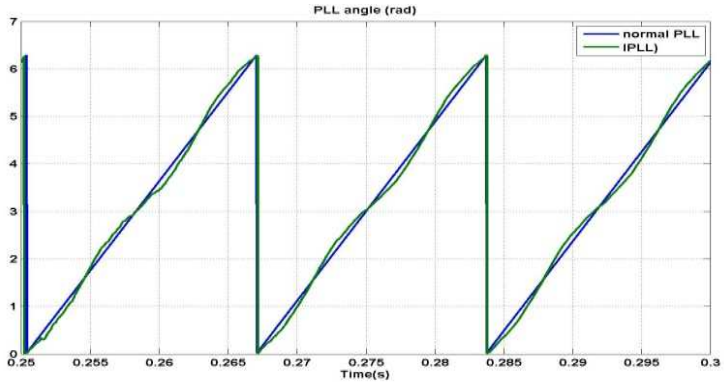


Figure 4-24 Voltage phase of system with (a) normal PLL, (b) IPLL, under SLG fault

4.3 Verification on Real Time Digital Simulator (RTDS)

RTDS (Real Time Digital Simulator) provides power systems simulation technology for fast, reliable, accurate and cost-effective study of power systems with complex High Voltage Alternating Current (HVAC) and High Voltage Direct Current (HVDC) networks. RTDS is a fully digital electromagnetic transient power system simulation platform for precise modeling and analysis of transient phenomena, utilizing simulation time close to the time frame of actual events. The power system algorithms are calculated quickly enough to continuously produce output conditions that realistically represent conditions in a real network. Additionally, RTDS can be connected directly to power system control and protection

equipment. It is a safe way to test designed controller on RTDS before implementation in the real system.

To verify the proposed methods, RTDS platform is used with sampling time of 50 µsec. Figure 4-25 to Figure 4-28 present the operation performance of the angle-controlled STATCOM under normal condition.

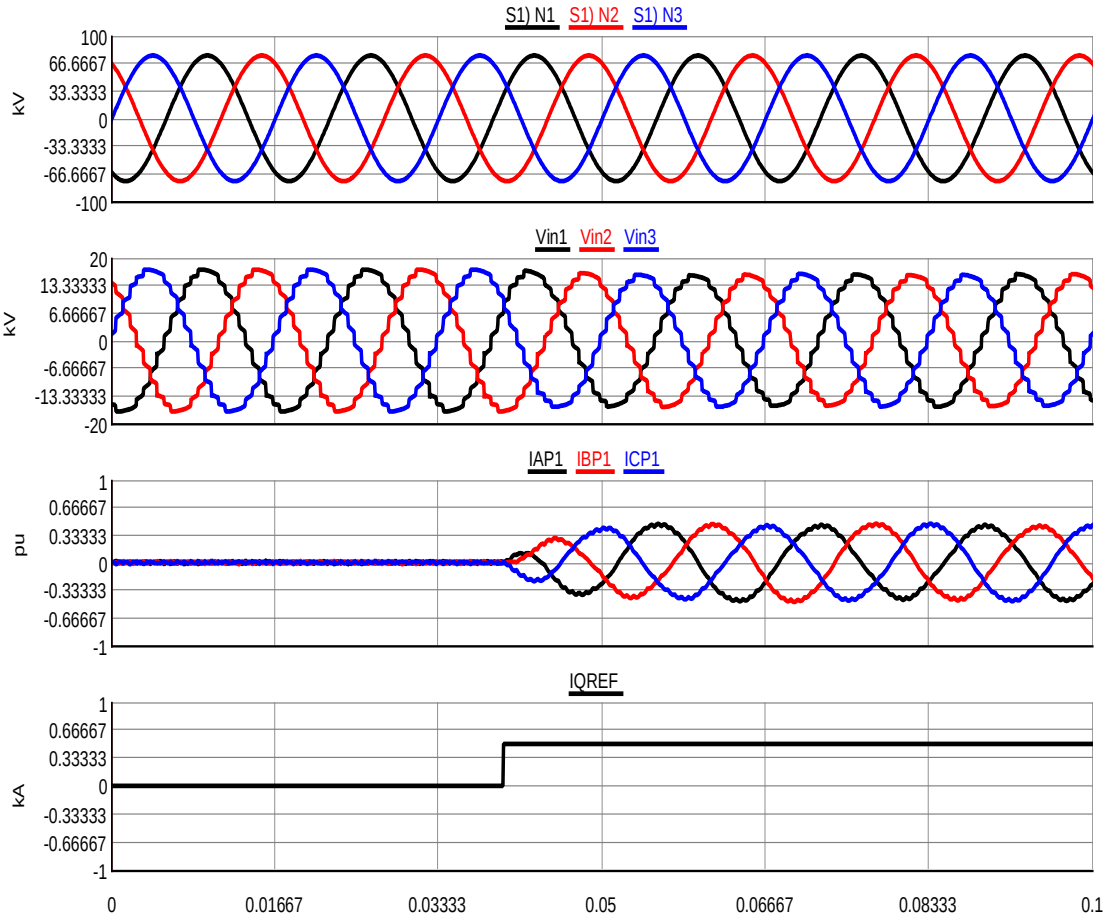


Figure 4-25 Angle-controlled STATCOM start-up dynamics to supply 0.5pu capacitive power- i_q = 0.5pu

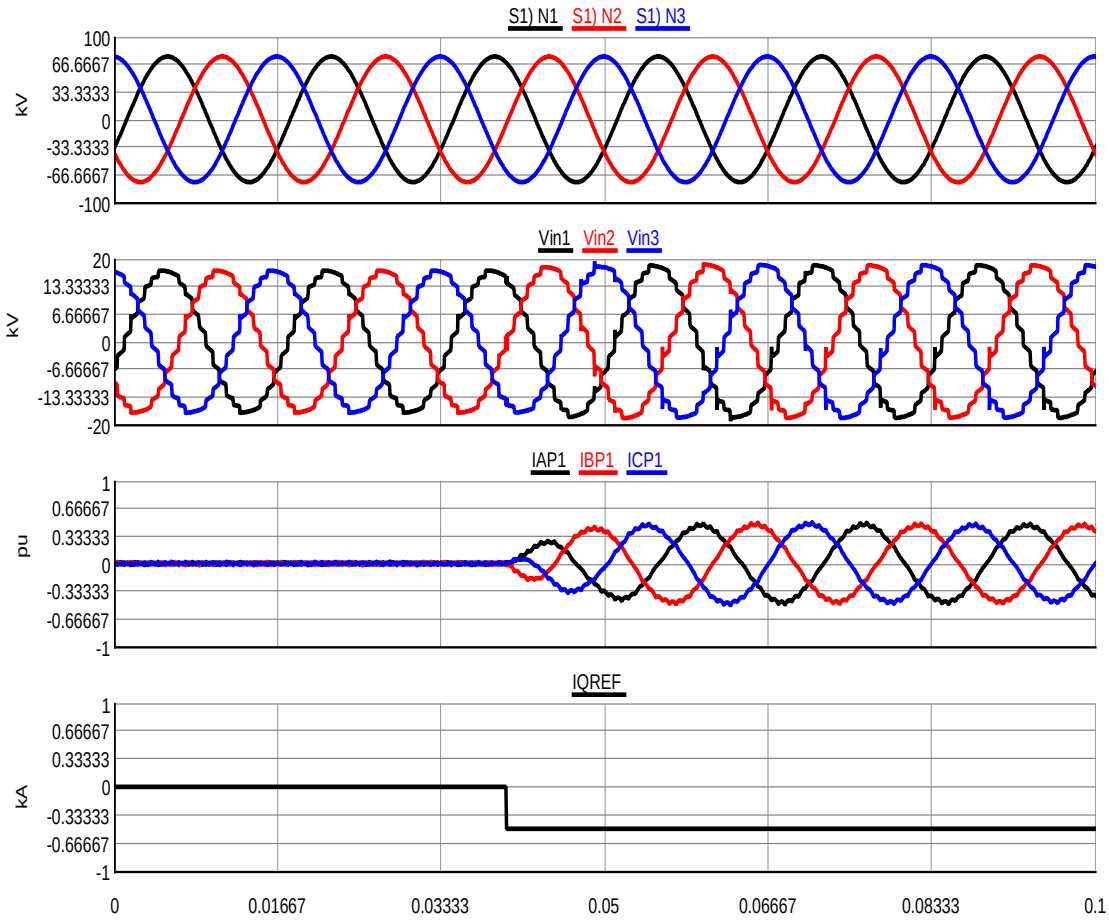


Figure 4-26 Angle-controlled STATCOM start-up dynamics to supply 0.5pu inductive power- i_q = -0.5pu

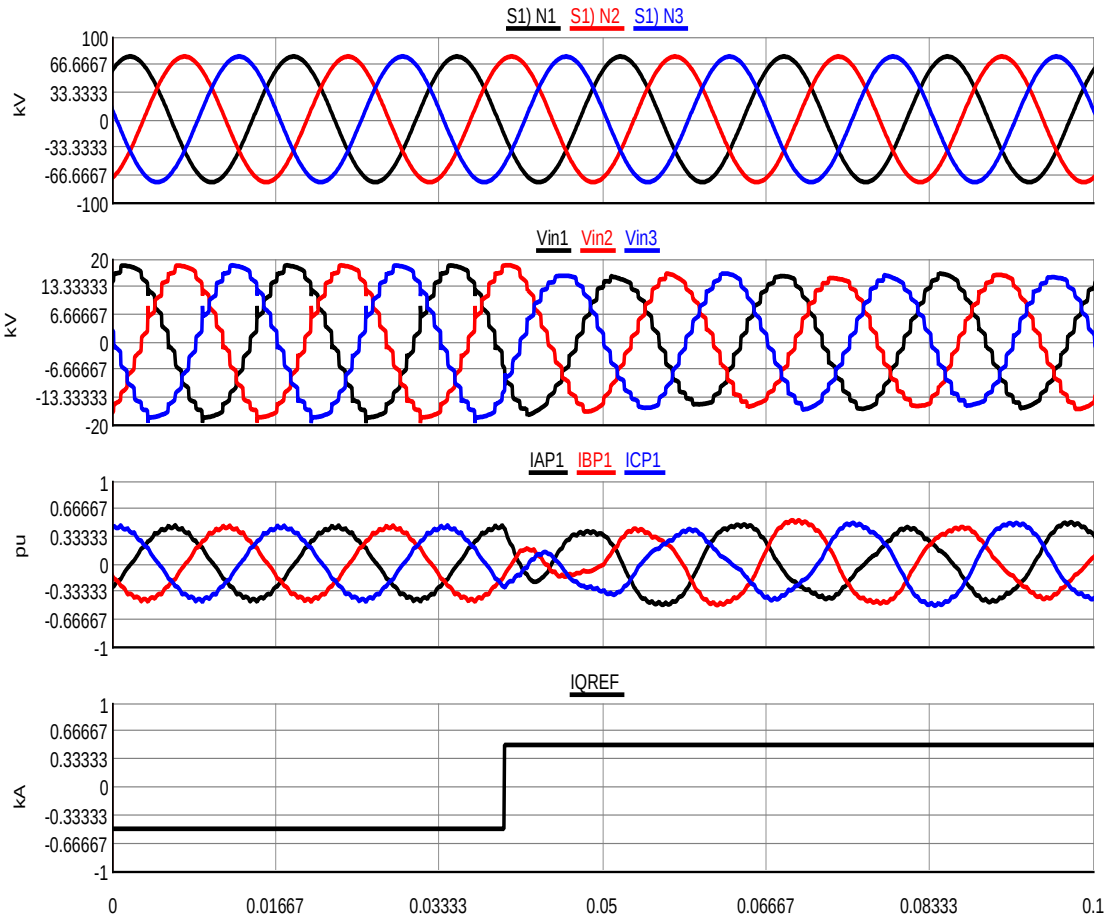


Figure 4-27 Angle-controlled STATCOM transition dynamics from 0.5pu inductive to 0.5pu capacitive-i_q= -0.5 to 0.5

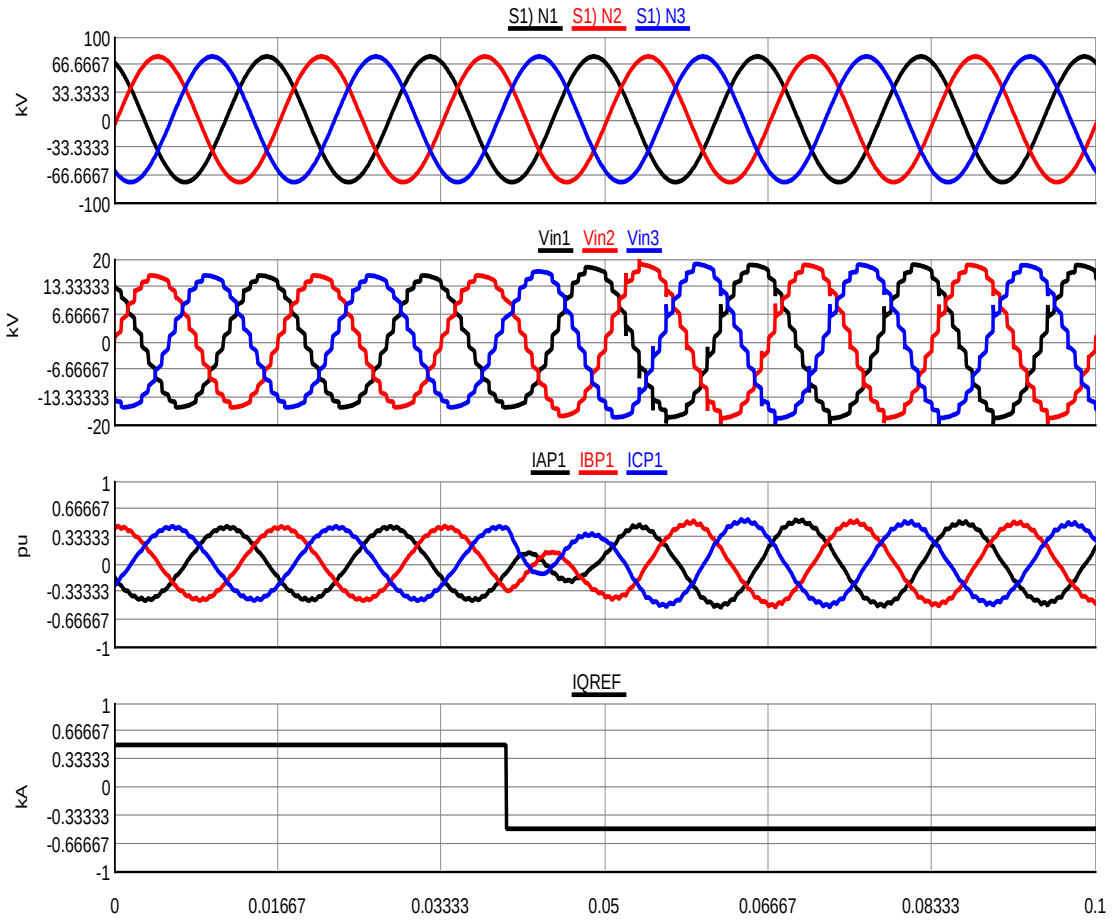


Figure 4-28 Angle-controlled STATCOM transition dynamics from 0.5pu capacitive to 0.5pu inductive-iq= 0.5 to -0.5

Figure 4-29 and Figure 4-30 show the STATCOM operation in *Iq* regulation mode with normal PLL and IPLL under 6-cycle single-line to ground (SLG) fault near STATCOM. As it can be seen, IPLL functions similar to normal PLL under normal conditions. Due to this severe fault, the PCC voltage drops to around 20% of the nominal voltage. The presented voltages are at secondary of the STATCOM (converter side). Figure 4-29 shows that the VSC currents exceed 2 pu under this nearby fault. This amount of current will result in overcurrent and trip to protect the VSC devices in a practical system. On the other hand, with

IPLL as presented in Figure 4-30, VSC currents do not increase significantly which allow the STATCOM to be online during and after SLG fault. The PLL signals with these two methods have been also presented in Figure 4-31. In fact, this result suggests the required synchronizing signal which is needed for the controller reference frame.

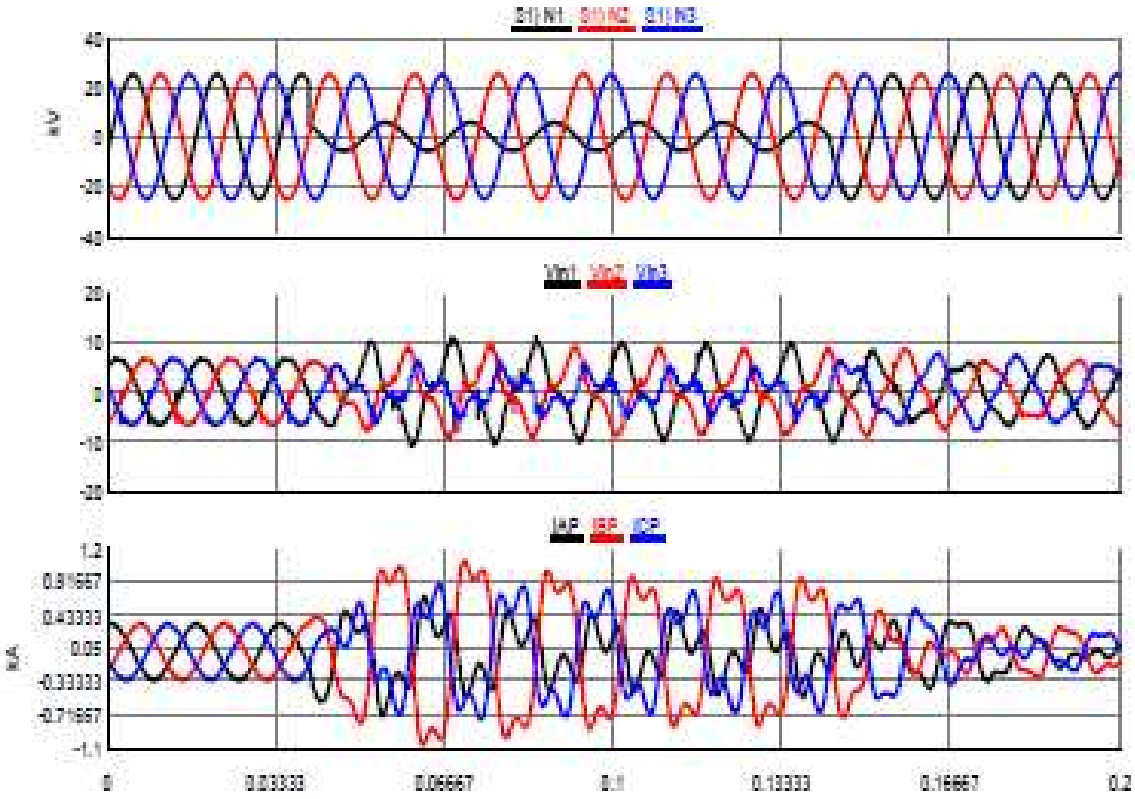


Figure 4-29 System with normal PLL under 6-cycle single-line to ground (SLG) fault near STATCOM

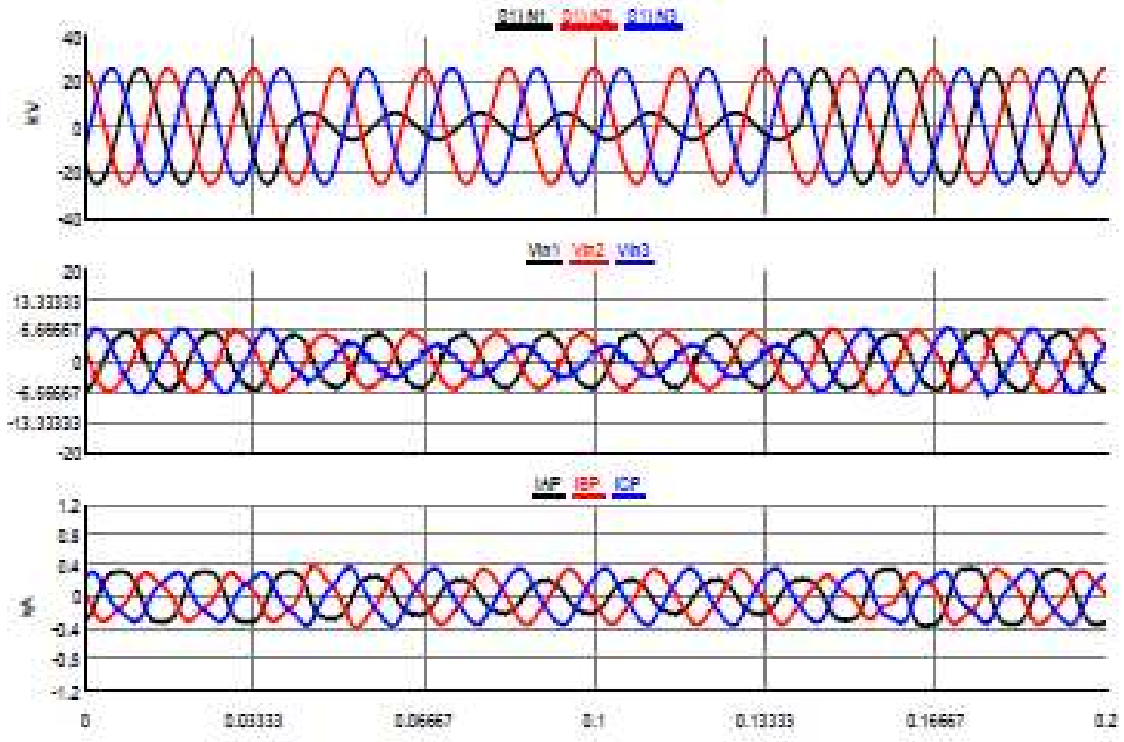


Figure 4-30 System with IPLL under 6-cycle single-line to ground (SLG) fault near STATCOM

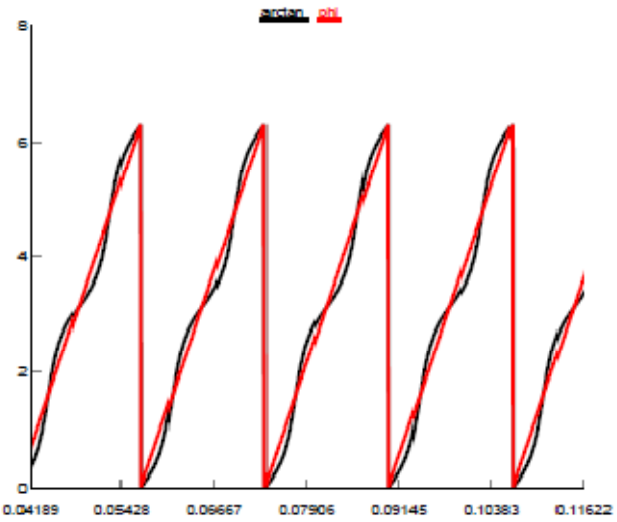


Figure 4-31 Synchronous reference frame signal with normal and PLL under single-line to ground fault

CHAPTER 5 STATCOM FOR DE-ICER APPLICATION [44]

The transmission line de-icer is required to provide large DC current (typically in the range of 5kA to 10kA) into a shorted transmission line to rapidly melt ice accumulation on the line. Due to the seldom nature of the de-icing requirement, it is imperative that the de-icer operate regularly as some other useful device in the transmission system.

The STATCOM is considered a suitable solution for ice-melt issue, which is one of the most common power system issue irritating customers. In a conventional application, STATCOM can be used to provide fast reactive power for voltage support and power oscillation damping. The same equipment, with a simple control reconfiguration, can perform ice melting function when it is needed. However, how to realize the application is not concluded yet.

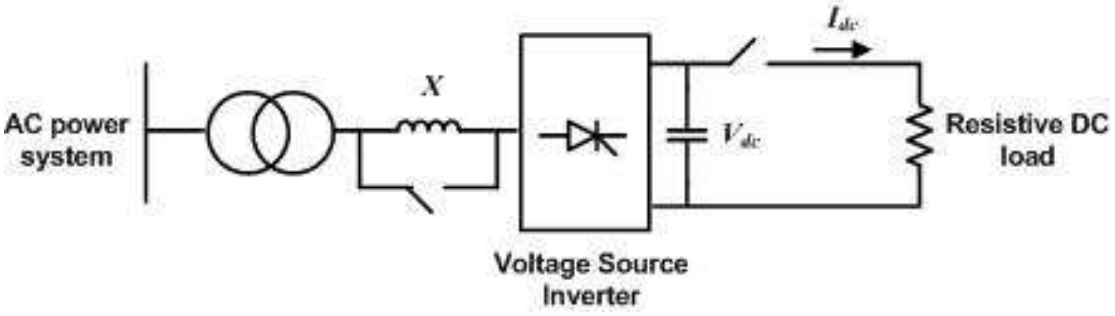


Figure 5-1 Illustration of STATCOM for ice melting application

Figure 5-1 shows the STATCOM for ice melting application. A large (approximately 1 p.u.) three phase as reactor, X, is connected in series with the output of the STATCOM on the secondary side of the coupling transformer to keep the DC bus voltage during de-icing implementation. A bypass switch is provided to short-circuit the reactor. On the DC side,

switches are provided so that the (iced) transmission lines can be connected to the DC terminals of the inverter. For normal STATCOM duty, the reactor is bypassed and the DC-side switches are open. For ice-melting, the reactor bypass is opened and the DC-side switches are closed.

In a conventional STATCOM application, the inverter AC terminal voltage changes very little over the range of reactive operation. In general, the inverter DC terminal voltage always has a minimum value determined by the sine-wave peak of the existing inverter AC terminal voltage. The DC voltage may be higher than this minimum value but can never be lower. If a resistive load is connected to the DC terminals, it would not generally be possible to regulate the DC voltage down to zero for the ice melting application, however, a regulated DC voltage must be provided from zero to the maximum specified value. This is done by means of a simple reconfiguration of the STATCOM power circuit when it is needed for ice melting. In this chapter, three different circuit topologies of single and dual STATCOM and the control reconfigurations required for de-icer mode, by changing reactive current I_q reference under I_q regulation; fixed angle reference for angle control to control DC capacitor voltage; and by changing DC voltage according to a reference DC current through transmission conductors, are described. Simulation results are presented for a 48-pulse VSC based +150 MVA STATCOM connected to a 2-bus power system. By changing the control configuration, STATCOM can perform ice melting function when it is needed. The incremental cost for ice-melting capability is relatively small. The changeover procedure is simple and can be accomplished by remote control.

5.1 Control Configuration

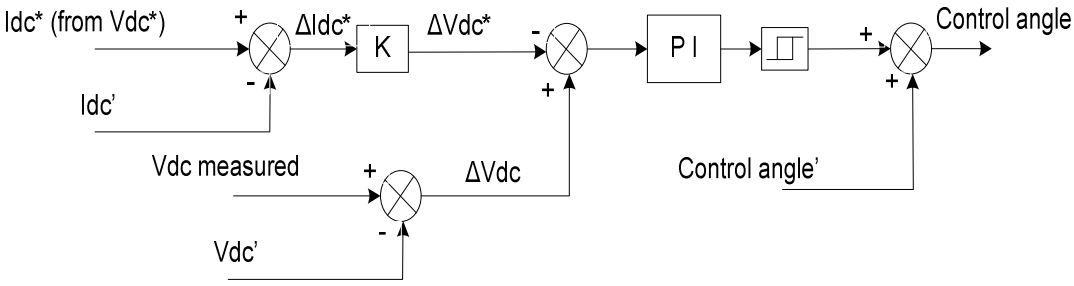


Figure 5-2 De-icer ΔI_{dc} controller block diagram

The Figure 5-2 shows de-icer ΔI_{dc} controller, where "'" means value of steady state before increase in V_{dc}. According to the type, amount and shape of ice accumulated on lines, the amount of I_{dc} needed to guarantee ice melting within a specified time is determined. To achieve this value of I_{dc}, DC capacitors of the STATCOM need to be charged to a higher voltage. Based on the angle generated by STATCOM controller, another angle to increase the DC voltage is generated by de-icer ΔI_{dc} controller. The sum of these two angles is used to achieve the increased I_{dc} needed for ice melting.

5.2 Simulation results

5.2.1 Simulation system

Figure 5-3 shows the 2-bus 345kV power system simulation with a 48-pulse VSC based +150MVA STATCOM. In a conventional application, STATCOM can be used to provide fast reactive power for voltage support and power oscillation damping. Figure 5-4 shows the

de-icer mode system simulation. By connecting via its dc terminals to a load, STATCOM can perform the ice melting function when it is needed.

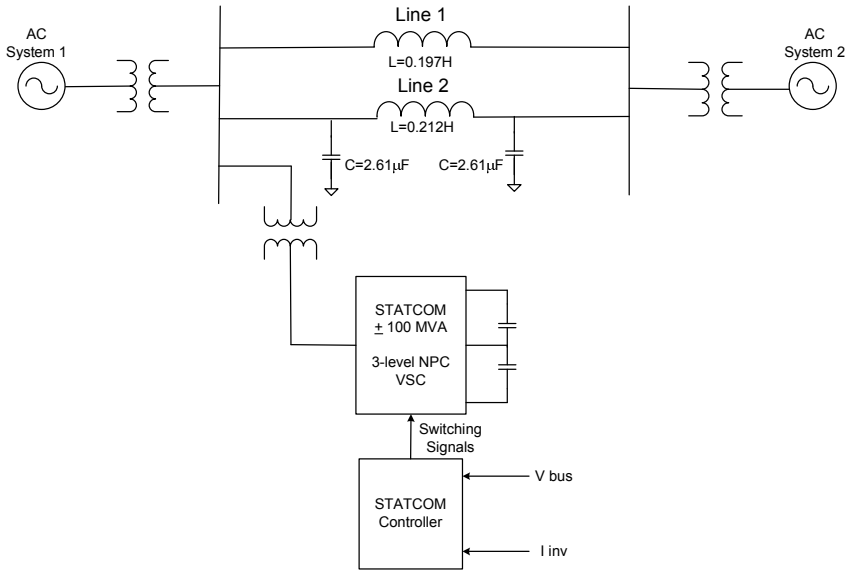


Figure 5-3 System simulation with a 48-pulse VSC based + 150 MVA STATCOM in a 2-bus power system

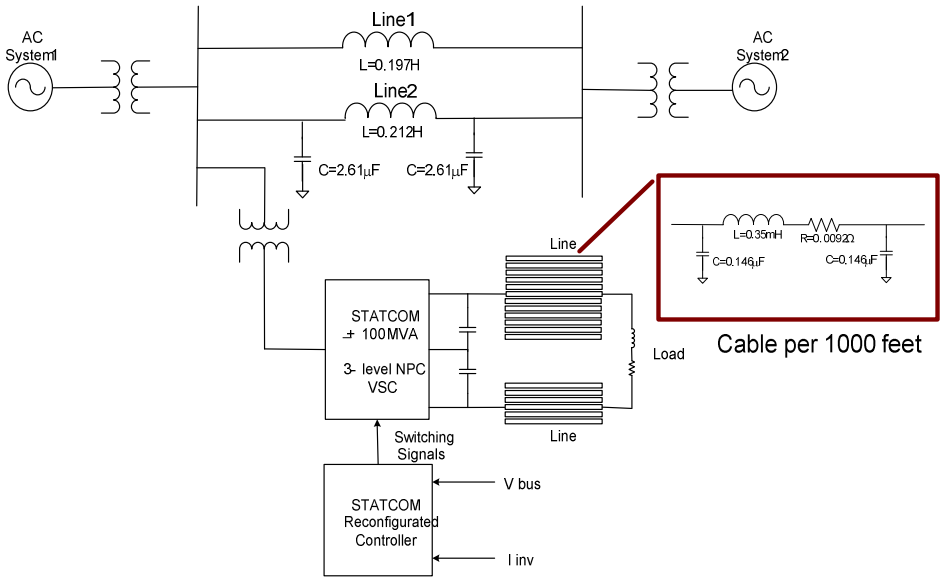


Figure 5-4 De-icer system simulation with a 48-pulse VSC based + 150 MVA STATCOM in a 2-bus power system

In some cases, ice melting needs more active power. Figure 5-5 show the de-icer system with two series-connected converters and two parallel-connected converter on the DC side, which are used as dual STATCOM and connected to the same ac voltage bus.

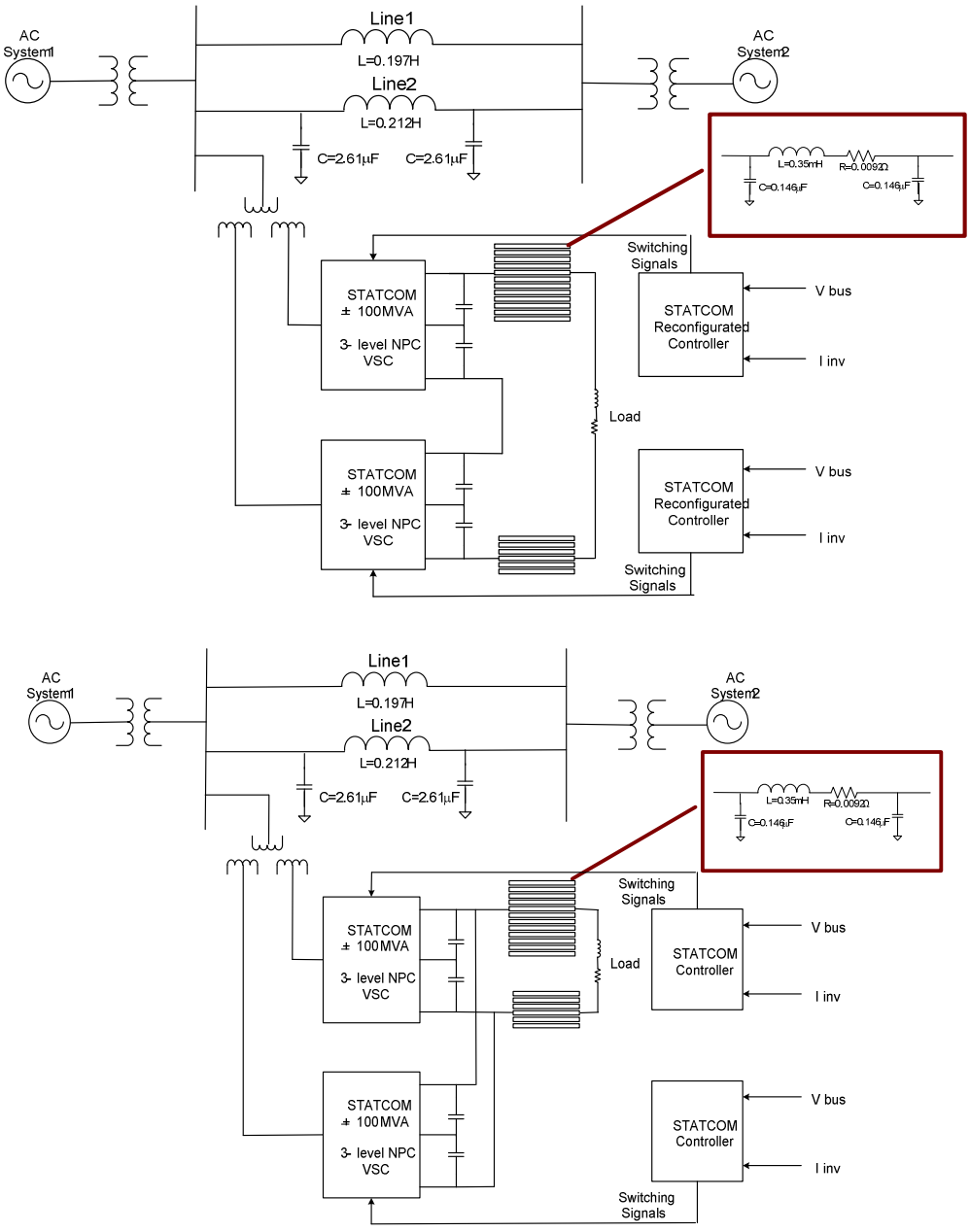


Figure 5-5 De-icer system with two (a) series (b) parallel connected converters on DC side

5.2.2 Iq regulation

To verify that STATCOM in I_q regulation mode can supply high dc voltage, Figure 5-6 shows the I_q*. To avoid GTO over-current condition due to high current during the transient period, in the first *0.1s*, all GTOs are open, and the current goes through anti-parallel diodes. At *T = 0.1s*, STATCOM operation changes to I_q regulation mode and *Iq* = 0 pu*. From *T = 0.3-0.9s*, *Iq** ramp is increased to *1 pu*, and is held at *1 pu* for *0.3s*. From *T = 0.9-1.5s*, I_q* ramp is decreased to *0 pu* and held as *0 pu* for *0.3 s*. From *T = 1.5-2.1s*, I_q* ramp is decreased to *-1 pu* and held at *-1 pu* for *0.3s*.

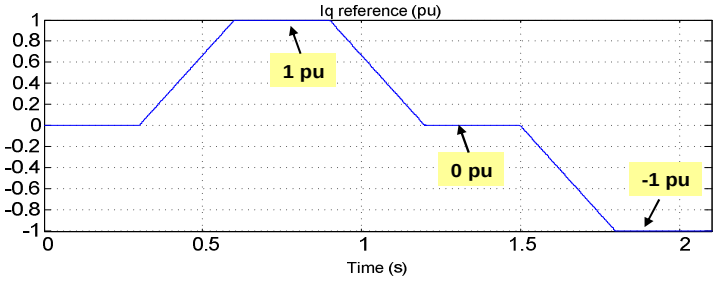


Figure 5-6 I_q reference in I_q regulation mode*

The Figure 5-7 shows the single converter STATCOM based de-icer system under I_q regulation with I_q* changing as shown in Figure 5-6. It is seen that the DC current and DC voltage are changing with the change of I_q*, causing active power flow. Increasing I_q* results in larger DC current and DC voltage. The converter is constrained to supply +100MVAR reactive power. When I_q *= 1*, the STATCOM also supplies *34.2MW* to the DC load.

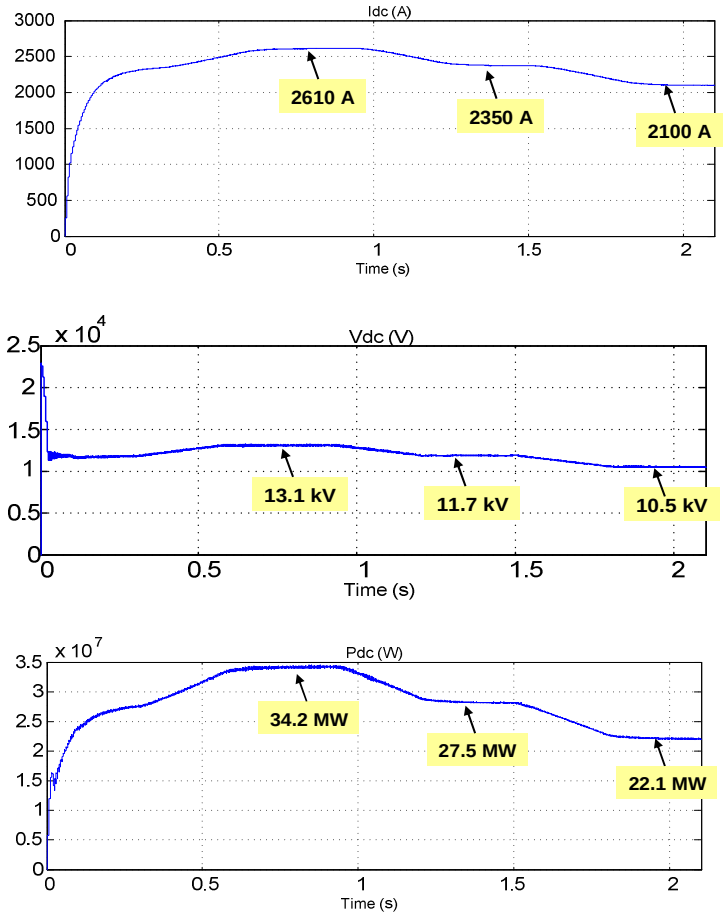


Figure 5-7 De-icer system with single converter STATCOM under I_q regulation.

The Figure 5-8 and Figure 5-9 show two series-connected converters based dual STATCOM de-icer system and two parallel-connected converters based dual STATCOM de-icer system under I_q regulation with I_q* changing as shown in Figure 5-6. It is seen that the DC current and DC voltage are changing with the change of I_q*. Increasing I_q* results in larger DC current and DC voltage.

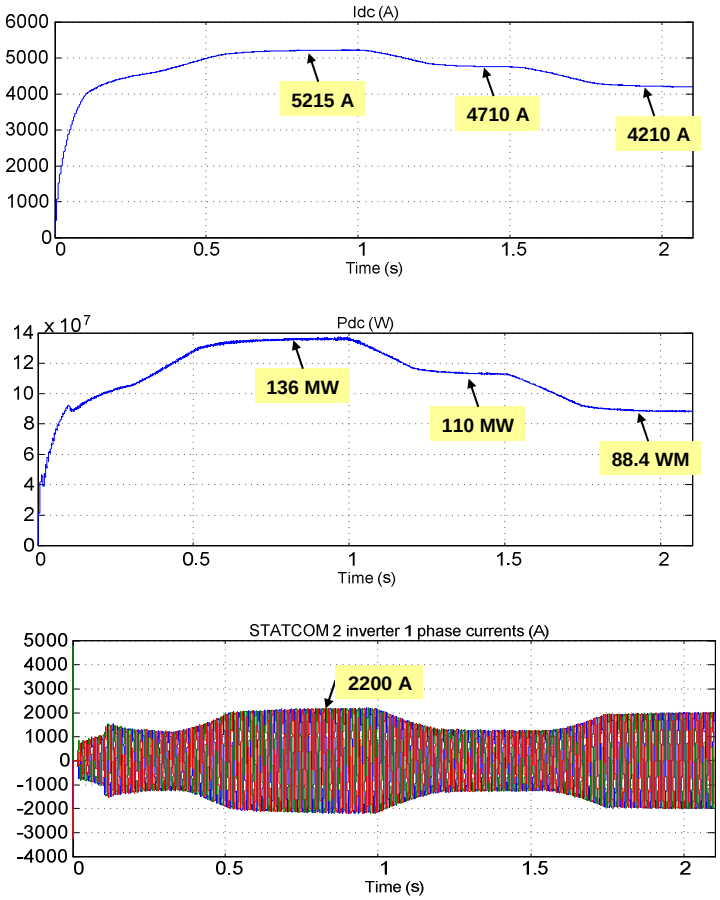


Figure 5-8 Dual STATCOM based de-icer system with two series-connected converters on DC side under I_q regulation.

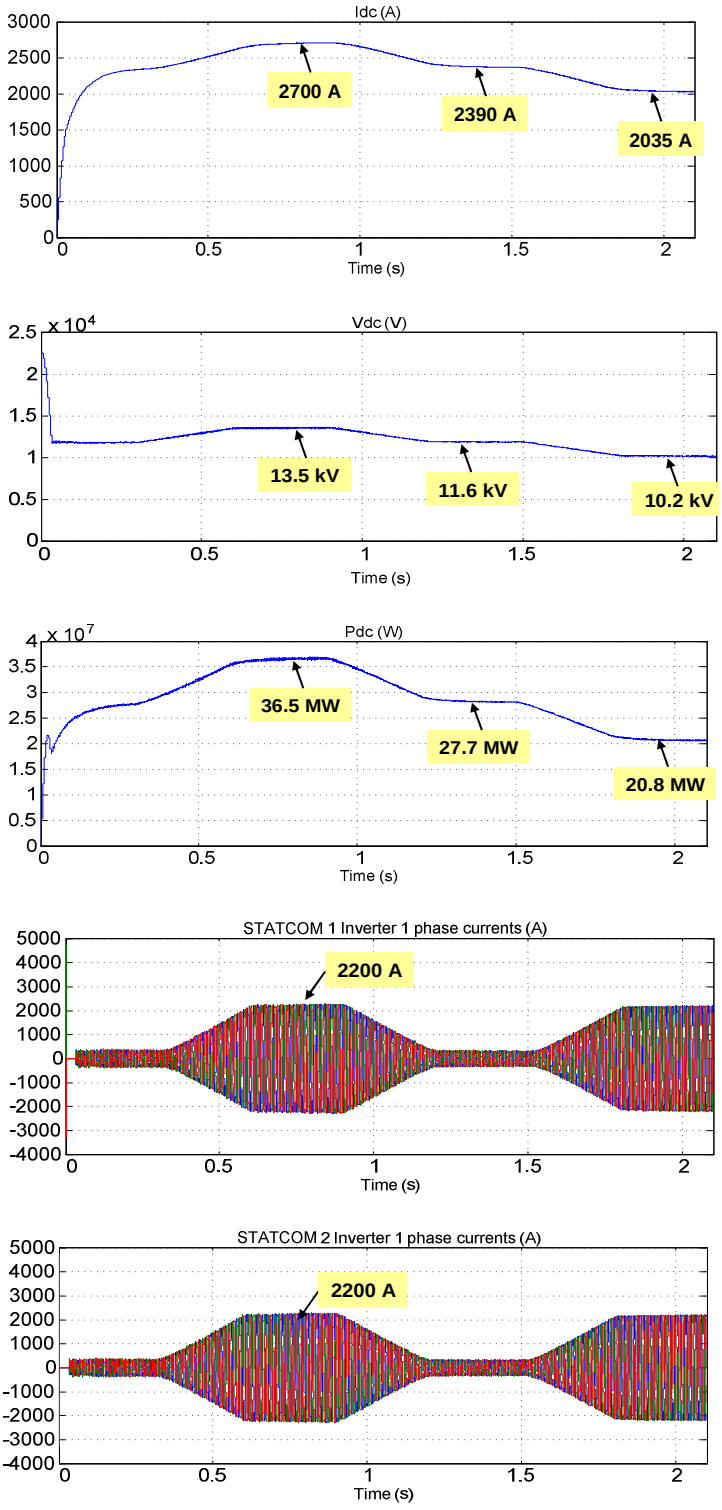


Figure 5-9 Dual STATCOM based de-icer system with two parallel-connected converters on DC side under I_q regulation.

5.2.3 Fixed angle

The STATCOM control is achieved by varying the phase angle, α, of the inverter output voltage relative to the transmission line voltage. To achieve a higher DC voltage, a fixed angle can be applied to charge the DC capacitors of STATCOM.

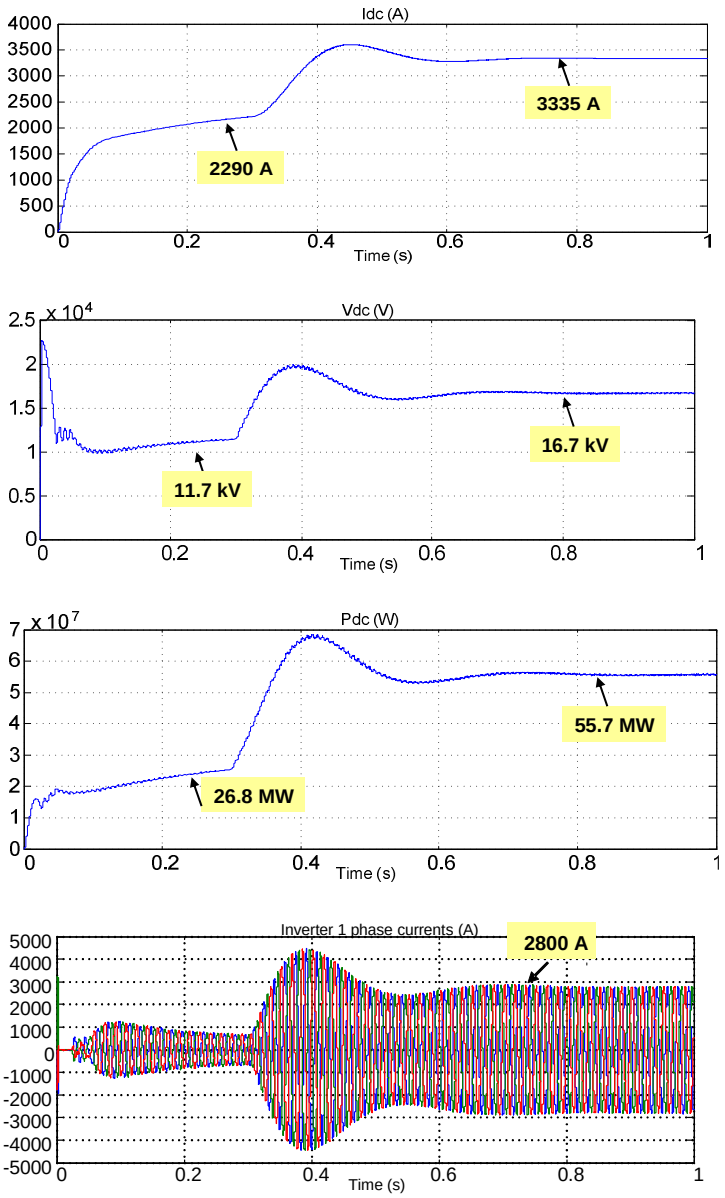


Figure 5-10 De-icer system with single converter based STATCOM under fixed angle control.

The Figure 5-10 shows single converter based de-icer system under fixed angle control. In the first *0.05s*, all GTOs of the STATCOM are open and the current goes through the anti-parallel diodes. From *T = 0.05-0.3s*, the STATCOM is operated in I_q regulation mode, as shown in Figure 5-6, with $I_q^* = 0$ *pu*. At *T = 0.3s*, a fixed angle of 7 degrees is applied as the controller signal to operate the STATCOM. It is seen that the fixed angle results in higher DC voltage of the STATCOM.

The Figure 5-11 and Figure 5-12 show dual STATCOM based de-icer system with two series-connected converters on DC side and dual STATCOM based de-icer system with two parallel-connected converters on DC side respectively, under fixed angle control. At *T = 0.3s*, a fixed angle of 4.8 degrees and 1 degree respectively, are applied as the controller signals to operate the dual STATCOM for the series connected and parallel connected system on the DC side.

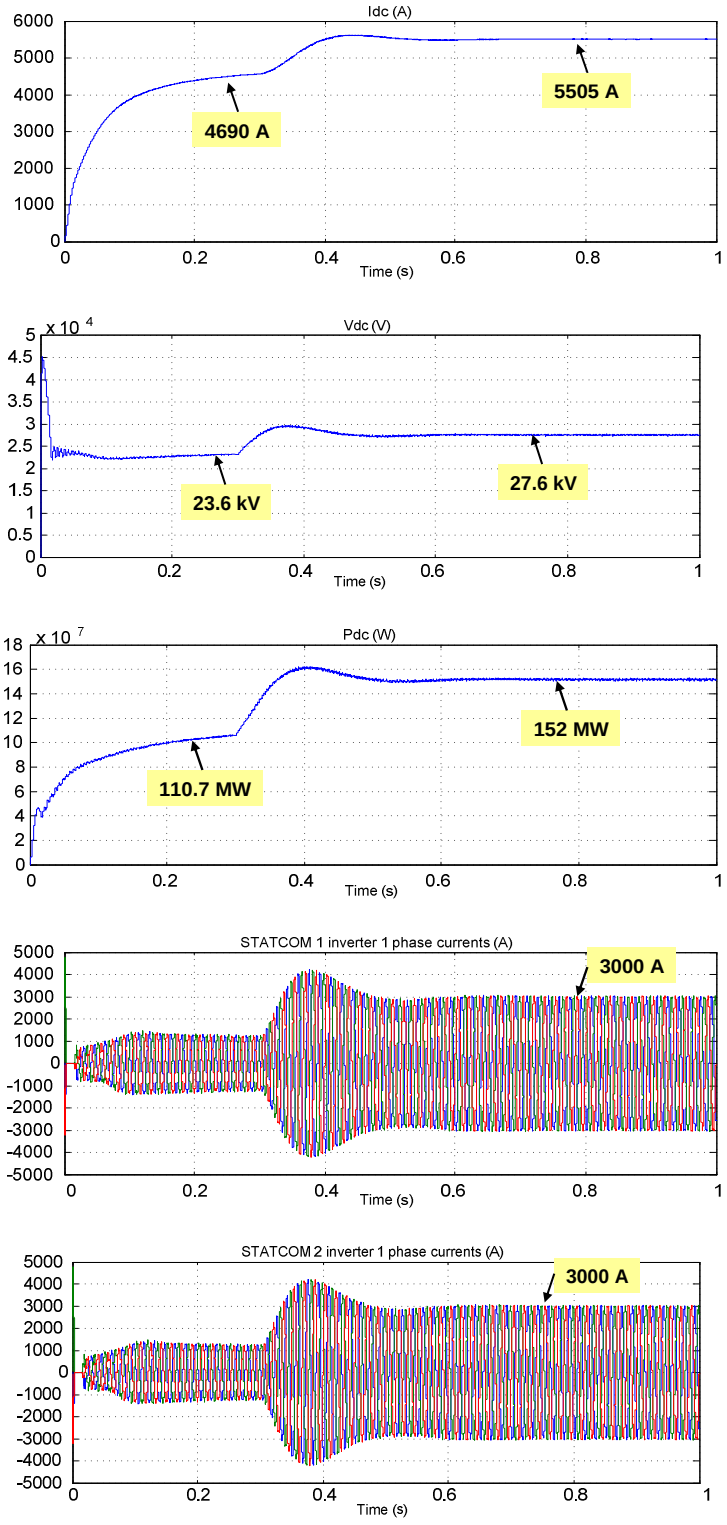


Figure 5-11 Dual STATCOM based de-icer system with two series-connected converters on the DC side under fixed angle control.

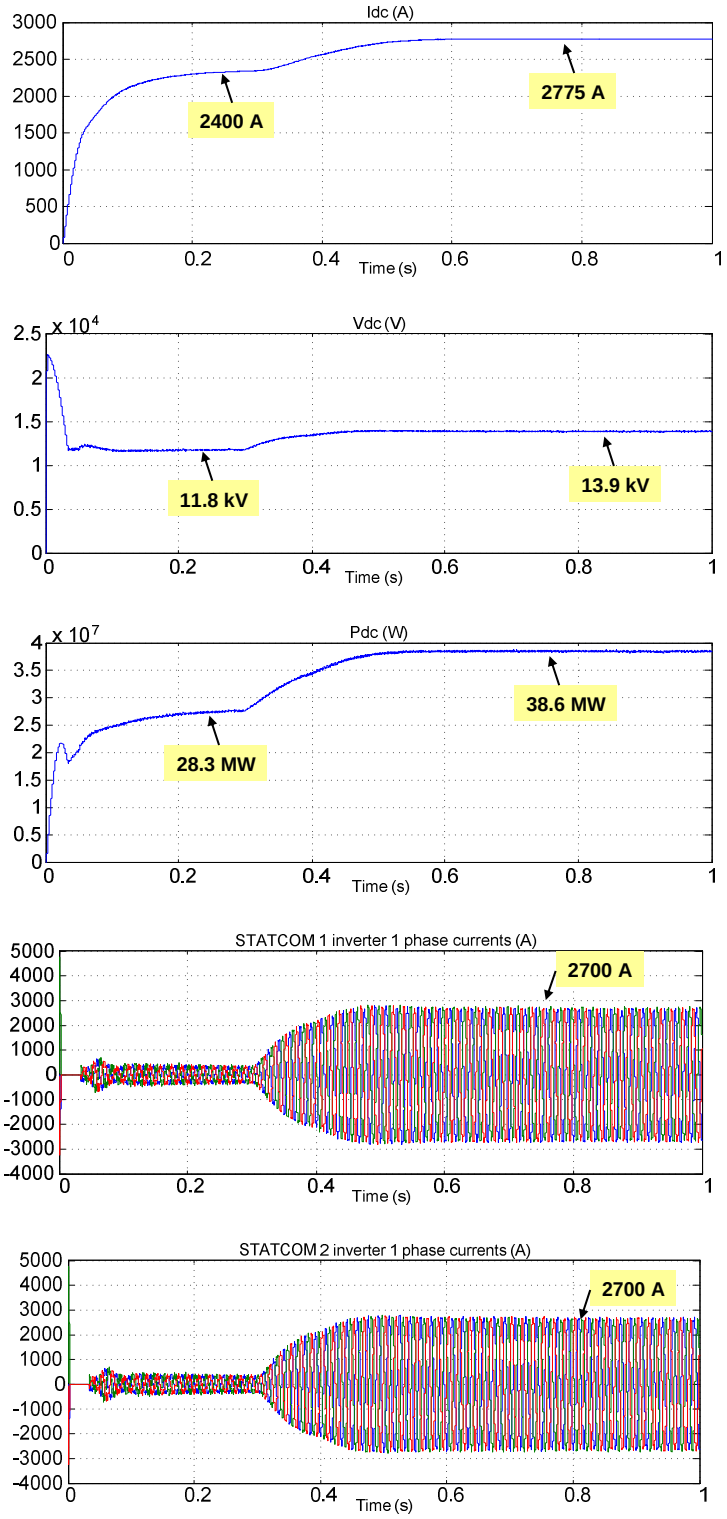


Figure 5-12 Dual STATCOM based de-icer system with two parallel-connected converters on the DC side under fixed angle control

5.2.4 ΔI_{dc} control

The Figure 5-13 shows single converter STATCOM based de-icer system under ΔI_{dc} control.

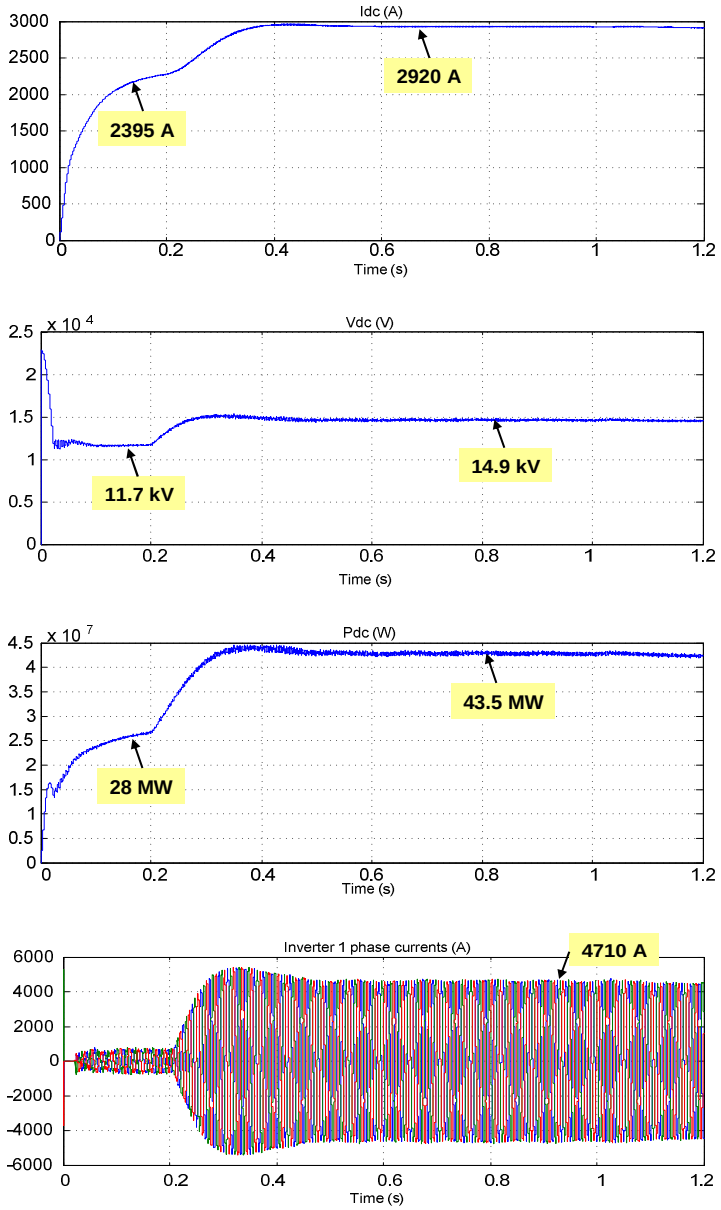


Figure 5-13 Dc-icer system with single converter under ΔI_{dc} control.

In the first *0.05s*, all GTOs are open and the current goes through anti-parallel diodes. From *T = 0.05-0.2s*, the STATCOM operates in I_q regulation mode, as shown in Figure 5-6, with $I_q^* = 0$. At *T = 0.2s*, the controller switches to ΔI_{dc} controller, as shown in Figure 5-2 and ΔI_{dc}^* is ramped up to *525A*, and kept at *525A* after *T = 0.6s*. It is seen that under ΔI_{dc} control the DC current required for de-icing can be generated by the STATCOM. These results in Figure 5-13, Figure 5-14 and Figure 5-15 validate the ΔI_{dc} controller concept and show the maximum DC current that can be generated with the given system parameters.

The Figure 5-14 and Figure 5-15 show Dual STATCOM based de-icer system with two series-connected converters on the dc side under ΔI_{dc} control. In Figure 5-14, the two converters are connected in series on the DC side and in Figure 5-15 the two converters are connected in parallel on the DC side. At *T = 0.3s*, the controller switches to ΔI_{dc} controller and ΔI_{dc}^* is increased to *525A*, and kept at *525A* after *T = 0.7s*.

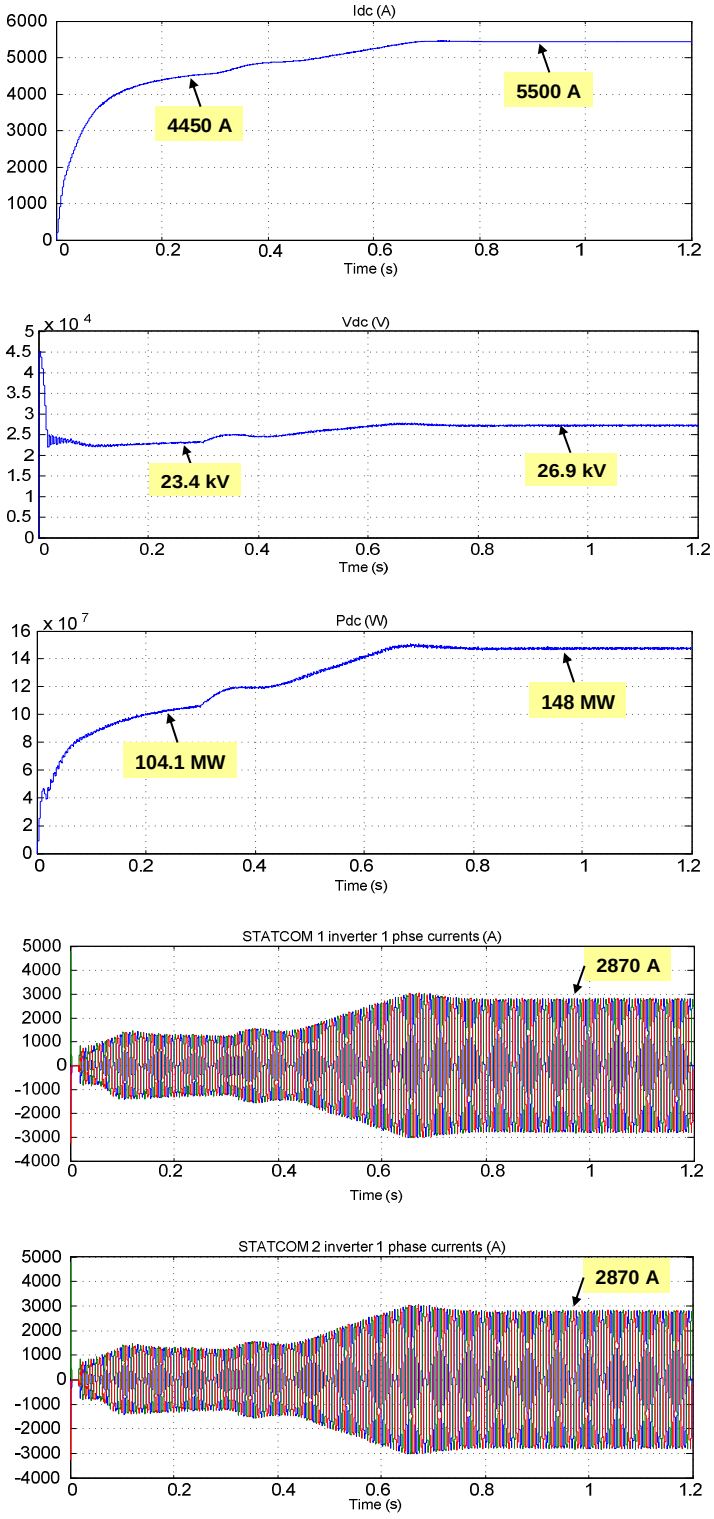


Figure 5-14 Dual STATCOM based de-icer system with two series-connected converters on the DC side under ΔI_{dc} control.

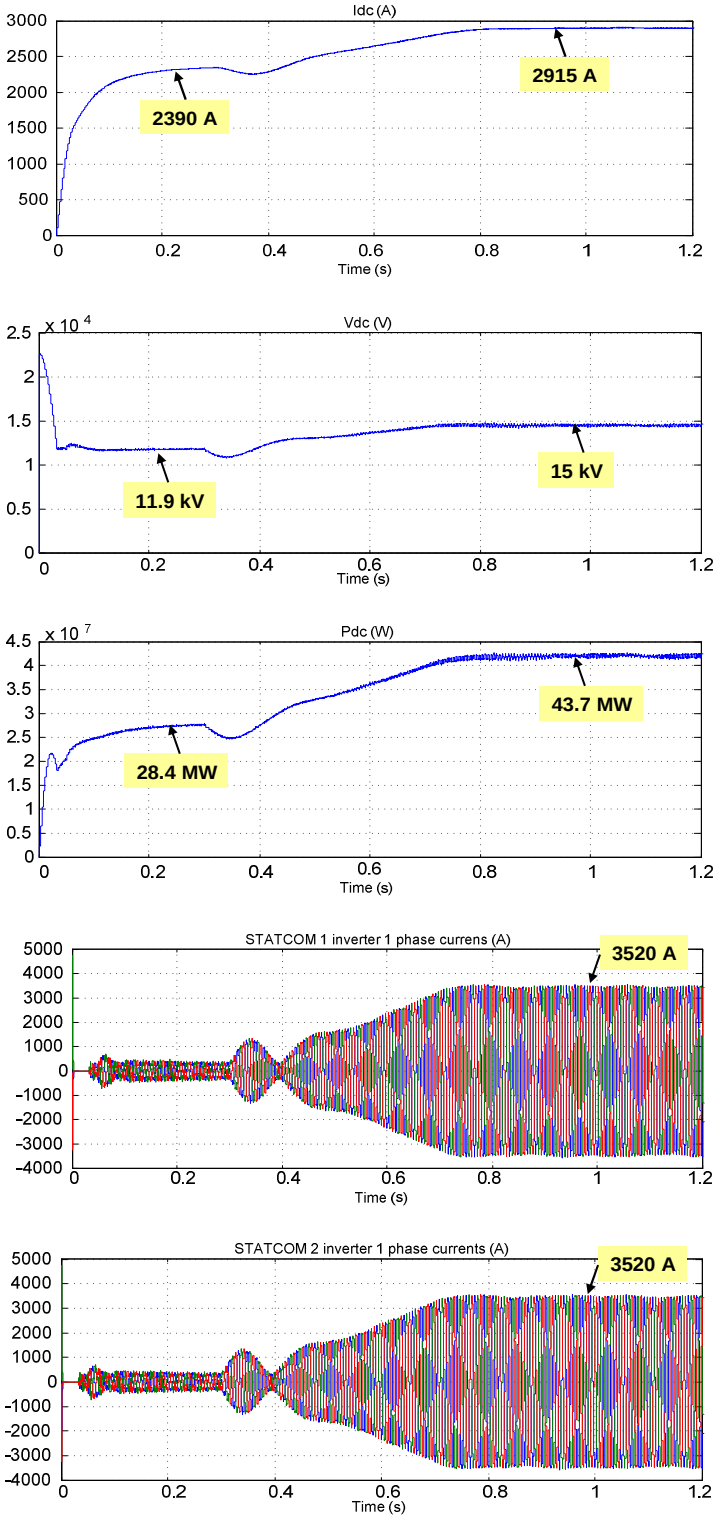


Figure 5-15 Dual STATCOM based de-icer system with two parallel-connected converters on the DC side under ΔI_{dc} control.

5.3 Conclusion

Ice accumulation on power transmission lines in winter can cause severe damage to power system. The STATCOM provides good asset utilization by providing reactive power for bus voltage support, during majority of the time when ice-melting is not required.

CHAPTER 6 IMPROVING DISTRIBUTION SYSTEM PERFORMANCE WITH INTEGRATED STATCOM AND SUPERCAPACITOR [45]

In this chapter, the integration and control of energy storage systems (ESSs), such as Supercapacitor (Ultracapacitor - UCAP) into a D-STATCOM (Distribution system STATCOM) is developed to enhance power quality and improve distribution system reliability. This paper develops the control concepts to charge/discharge the UCAP by the D-STATCOM, and validate the performance of an integrated D-STATCOM/UCAP system for improving distribution system performance under all types of system related disturbances and system faults – such as single-line to ground fault (SLG), line-line fault and 3-phase faults.

6.1 D-STATCOM Application for Distribution System

The Figure 6-1 shows a typical 12kV distribution system. A 125kVA 2-level VSC based D-STATCOM is connected to the system through a shunt coupling transformer at 480V to regulate the system bus voltage at the point of common coupling (PCC). The D-STATCOM VSC DC nominal bus voltage is 600V. A UCAP is integrated with DC capacitor, with its experimentally verified equivalent circuit characteristics.

The UCAP is rated 600V to match the DC bus voltage requirement for the D-STATCOM. The UCAP capacitance is determined by applying a constant-current discharge with

$$C = I\frac{dt}{dv}$$

Equation 6-1

Since dv/di is almost constant, UCAP capacitance can be modeled as a constant. The equivalent series resistance (ESR) is calculated by measuring the output voltage drop from no load to steady-state load and then diving by the load current. Since the open-circuit voltage has no significant effect on the ESR, the ESR can be modeled as a constant. The UCAP is modeled with *1.0F* capacitance and *320mΩ* ESR.

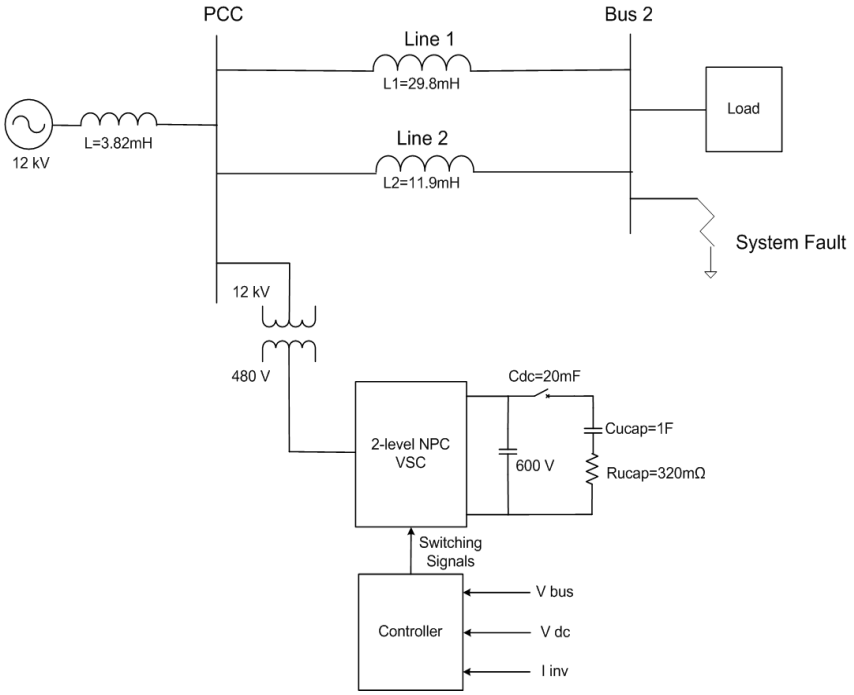


Figure 6-1 Distribution system with D-STATCOM integrated with UCAP and controller.

If there is a system fault in the distribution system, the D-STATCOM can not regulate V_{pcc} and the VSC DC bus voltage (V_{dc}). As a result, the D-STATCOM delivers I_d component of

current (corresponding to the real power component) due to this DC bus voltage disturbance. This then limits the D-STATCOM reactive power rating and limits the reactive current I_q component. To reduce the effect of fault or V_{pcc} bus voltage disturbance on the D-STATCOM system operation, a larger value of DC capacitor may be utilized, but it still can not keep DC voltage constant during the fault (as shown by simulation results in the next section).

The Figure 6-2 shows the D-STATCOM controller integrated with UCAP. In this controller, of the two D-STATCOM current components I_d and I_q, the real current component I_d regulates V_{dc}. The voltage control loop regulates V_{pcc} voltage magnitude by generating reference current I_q* for current control loop. Inside the voltage control loop, the inner current control loop regulates D-STATCOM reactive current I_q component.

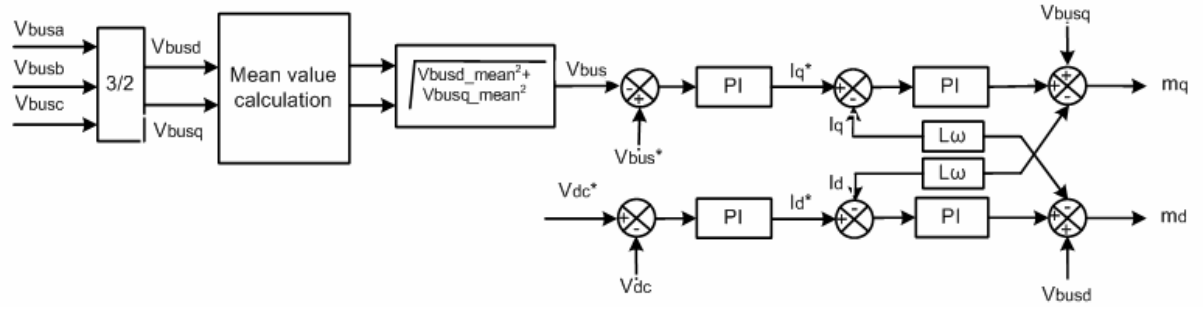


Figure 6-2 Integrated D-STATCOM and UCAP controller.

6.2 Simulation Results of the D-STATCOM Application for Distribution System

The system simulation diagram is shown in the Figure 6-1 with a 2-bus 125kV distribution system. A general fault generator is implemented at bus 2, which results in a voltage dip at

the STATCOM V_{dc}. Attention is focused on system faults and STATCOM performance with and without integrated UCAP.

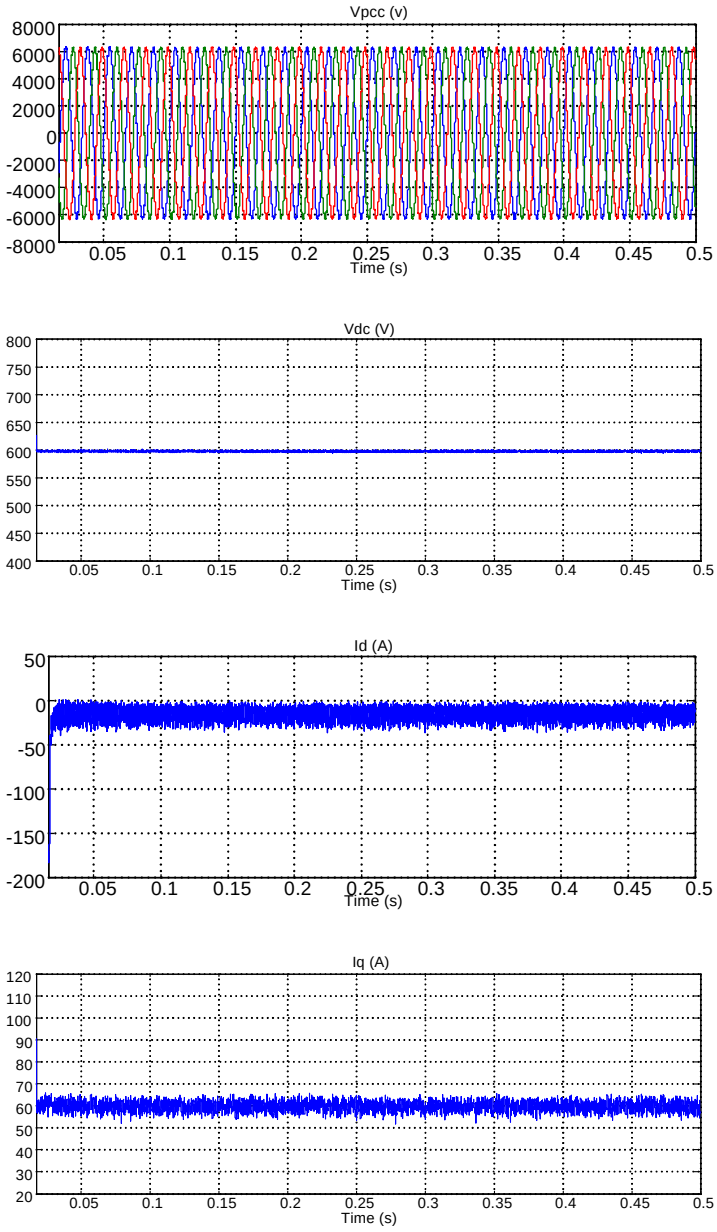


Figure 6-3 D-STATCOM operation under normal system conditions. (a) Bus voltage at the PCC, (b) DC voltage, (c) D-STATCOM real current, (d) D-STATCOM reactive current.

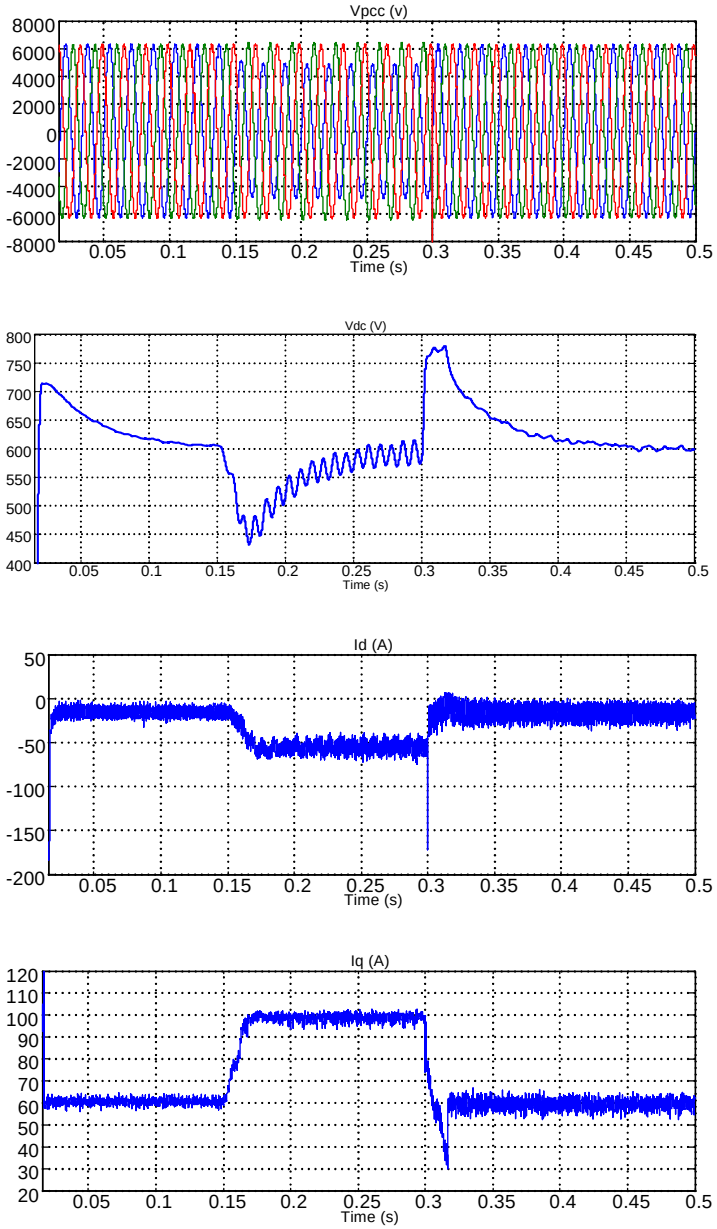


Figure 6-4 D-STATCOM operation under SLG fault with Cdc=0.2mF and without UCAP. (a) Bus voltage at the PCC, (b) DC voltage, (c) D-STATCOM real current, (d) D-STATCOM reactive current

The Figure 6-3 shows results of D-STATCOM operation under bus voltage regulation and normal system conditions. In this case, the VSC I_d current component is low as the D-STATCOM is required to provide only the VSC operating converter losses. It is seen that the

V_{pcc} voltage, I_d and I_q current components are regulated, and V_{dc} is kept constant. The D-STATCOM delivers constant $I_q = 60A$ reactive current to regulate the bus voltage.

The Figure 6-4 shows results of D-STATCOM operation under SLG fault conditions, where $C_{dc} = 0.2mF$. The V_{pcc} voltage dips due to a 6 cycle, *100ms* SLG fault on phase A as shown in Figure 6-4. The D-STATCOM is commanded to deliver I_q to regulate V_{pcc}, and I_q increases to around *100A*. During the SLG fault, the DC bus voltage is not regulated and has large voltage ripple. This requires the D-STATCOM to supply I_d current component, which limits D-STATCOM reactive power/current rating during fault or system disturbances, when it is required the most.

The Figure 6-5 shows results of D-STATCOM operation under SLG fault conditions with 10 times the DC side capacitance of $C_{dc} = 2mF$, compared to the results in Figure 6-4. In this case also the DC bus voltage is not regulated and the D-STATCOM is required to supply large I_d current component. The larger size of the DC capacitor reduces the high frequency DC bus voltage ripple, but cannot eliminate/reduce the low frequency dc bus voltage variation.

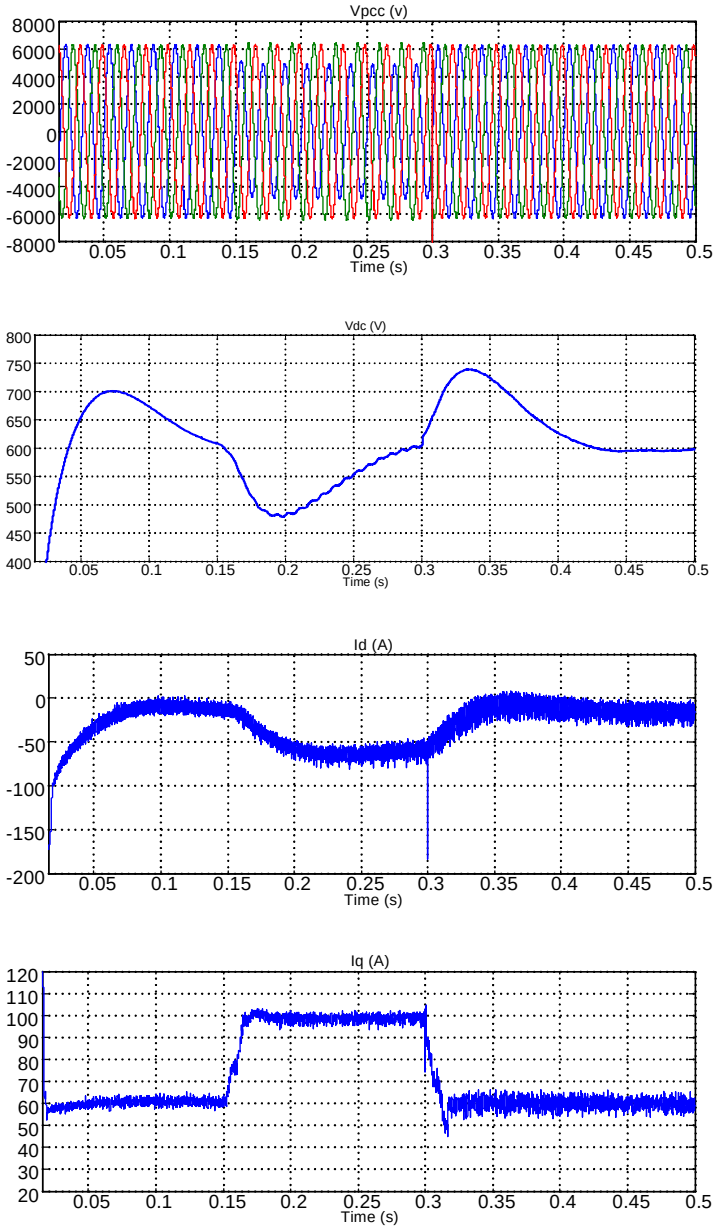


Figure 6-5 D-STATCOM operation under SLG fault with C_{dc}=2mF and without UCAP. (a) Bus voltage at the PCC, (b) DC voltage, (c) D-STATCOM real current, (d) D-STATCOM reactive current.

The Figure 6-6 shows results of the integrated D-STATCOM with UCAP system operation under SLG fault conditions – the SLG fault is on the load bus as shown in Figure 6-1. The V_{pcc} voltage (or D-STATCOM bus voltage) dips during the fault and D-STATCOM delivers

I_q current component to regulate V_{pcc}. The D-STATCOM DC bus voltage is well regulated by the D-STATCOM controller, and I_d is almost zero with UCAP connected to the dc bus.

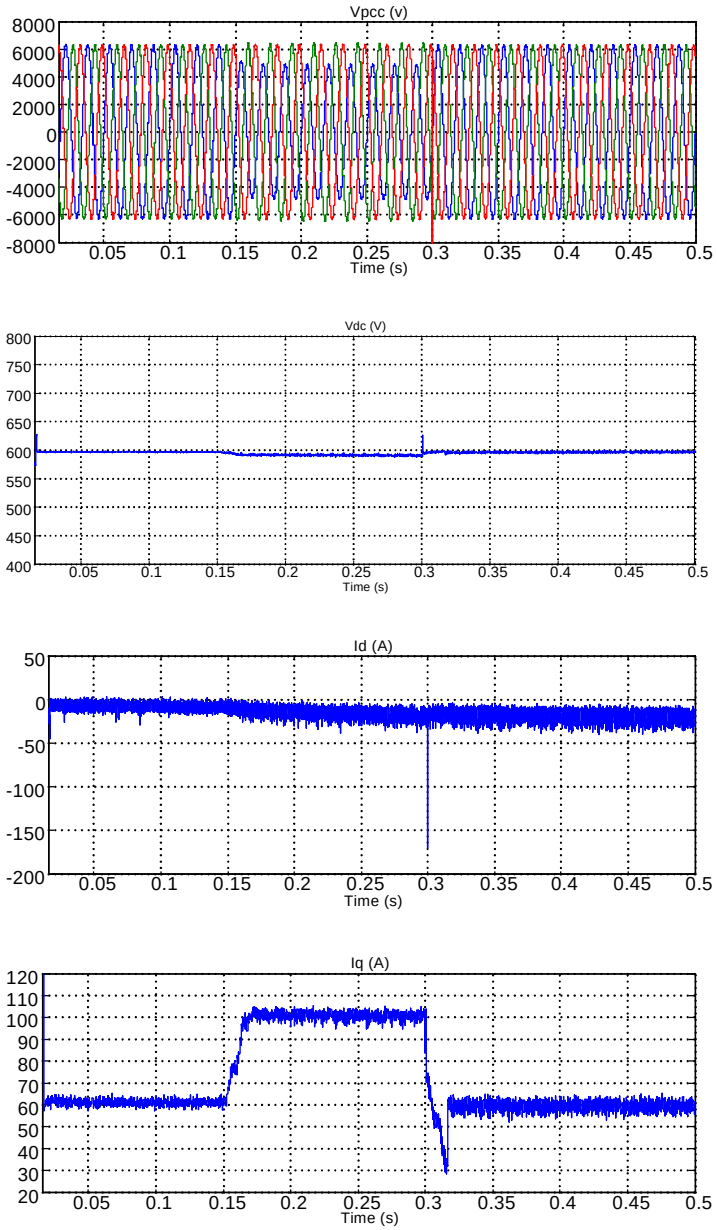


Figure 6-6 Integrated D-STATCOM and UCAP operation under SLG fault with C_{dc}=0.2mF. (a) Bus voltage at the PCC, (b) DC voltage, (c) D-STATCOM real current, (d) D-STATCOM reactive current

The Figure 6-7 shows the I_{dc} (total DC current), I_{ucap} (UCAP current) and I_{Cdc} (DC capacitor current) of integrated D-STATCOM and UCAP operation under single-line to ground (SLG) fault conditions. It is seen that the I_{ucap} follows the I_{dc} current on the low frequency basis. This is confirmed by current spectra in Figure 6-8, that high frequency components of I_{dc} are supplied by the I_{Cdc}, and low frequency components are supplied by the I_{ucap}. The D-STATCOM reactive power rating is therefore not limited by UCAP, and the integrated D-STATCOM and UCAP system is tolerant to SLG system fault or voltage dip in terms of rating.

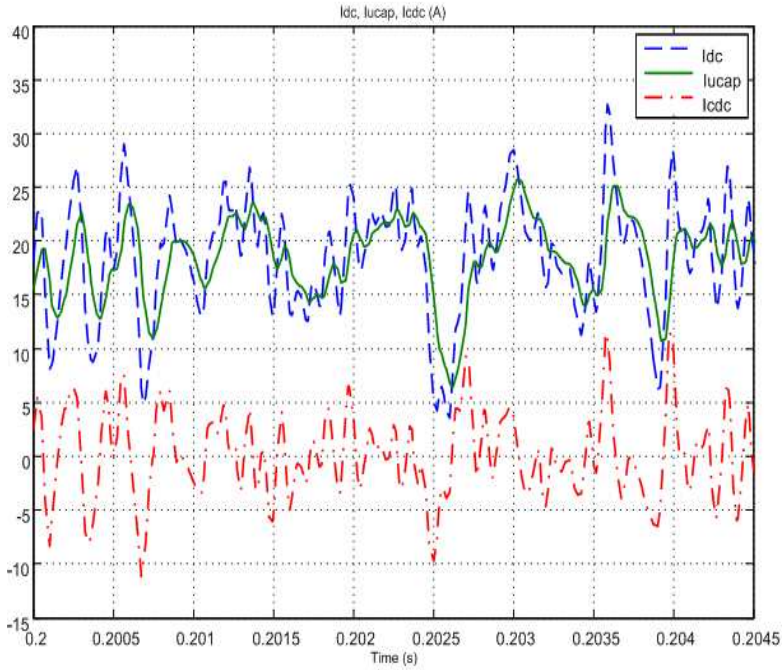


Figure 6-7 Total DC current, UCAP current and DC capacitor current of integrated D-STATCOM and UCAP operation under SLG fault conditions.

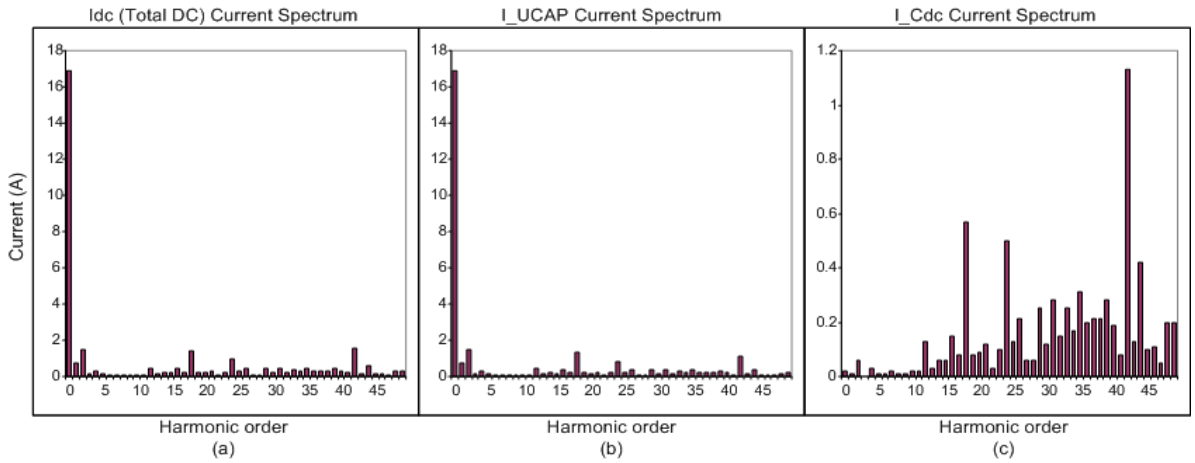


Figure 6-8 Current spectra of D-STATCOM integrated with UCAP operation under SLG fault conditions – shows that low frequency dc current components are supplied by UCAP and high frequency by DC capacitor (C_{dc})

The Figure 6-9 shows results of the integrated D-STATCOM with UCAP system operation under SLG fault conditions, with 0.1 times the DC side capacitance of C_{dc} = *0.02mF*. D-STATCOM delivers I_q current component to regulate V_{pcc} during the fault. The D-STATCOM DC bus voltage is well regulated by the D-STATCOM controller, and I_d is almost zero with UCAP connected to the dc bus. With UCAP, C_{dc} can even be reduced and the system size can be kept smaller. UCAP is also a practical solution in terms of the size.

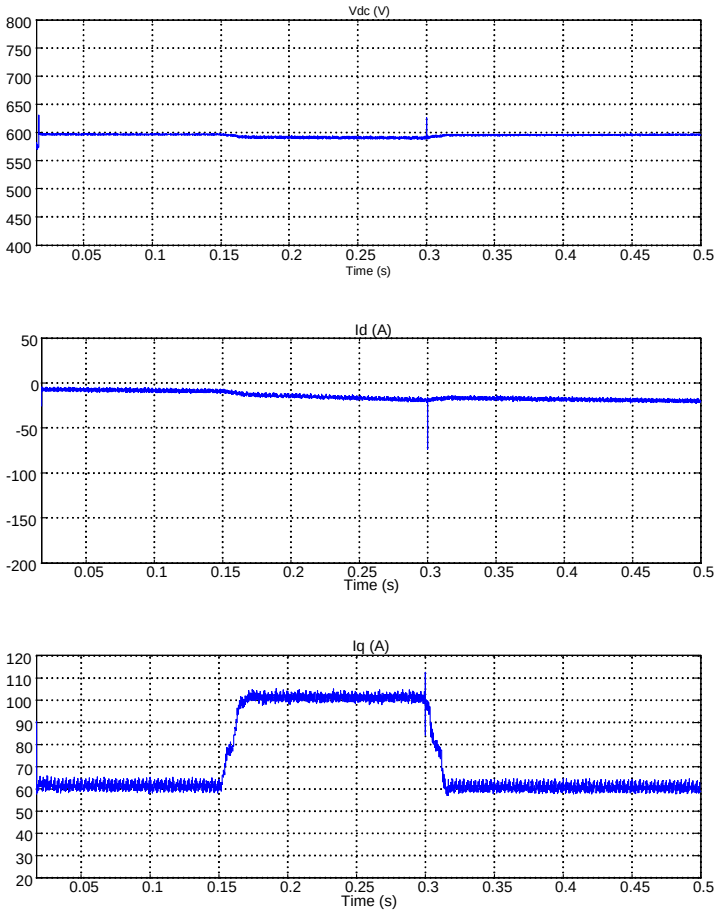


Figure 6-9 STATCOM operation under SLG fault with C_{dc}=0.02mF and without UCAP. (a) DC voltage, (b) D-STATCOM real current, (c) D-STATCOM reactive current.

The Figure 6-10 and Figure 6-11 respectively show the DC bus voltage, D-STATCOM real current and reactive current total DC current, UCAP current and DC capacitor current of integrated D-STATCOM and UCAP system operation under a 6 cycle 100ms of 3-phase fault and line-line fault conditions on the load bus, as shown in Figure 6-1. It is shown that with the UCAP, the DC bus voltages are well regulated and the D-STATCOM can supply reactive power/current rating during 3-phase and line-line fault conditions. I_{ucap} follows the I_{dc} current on the low frequency basis.

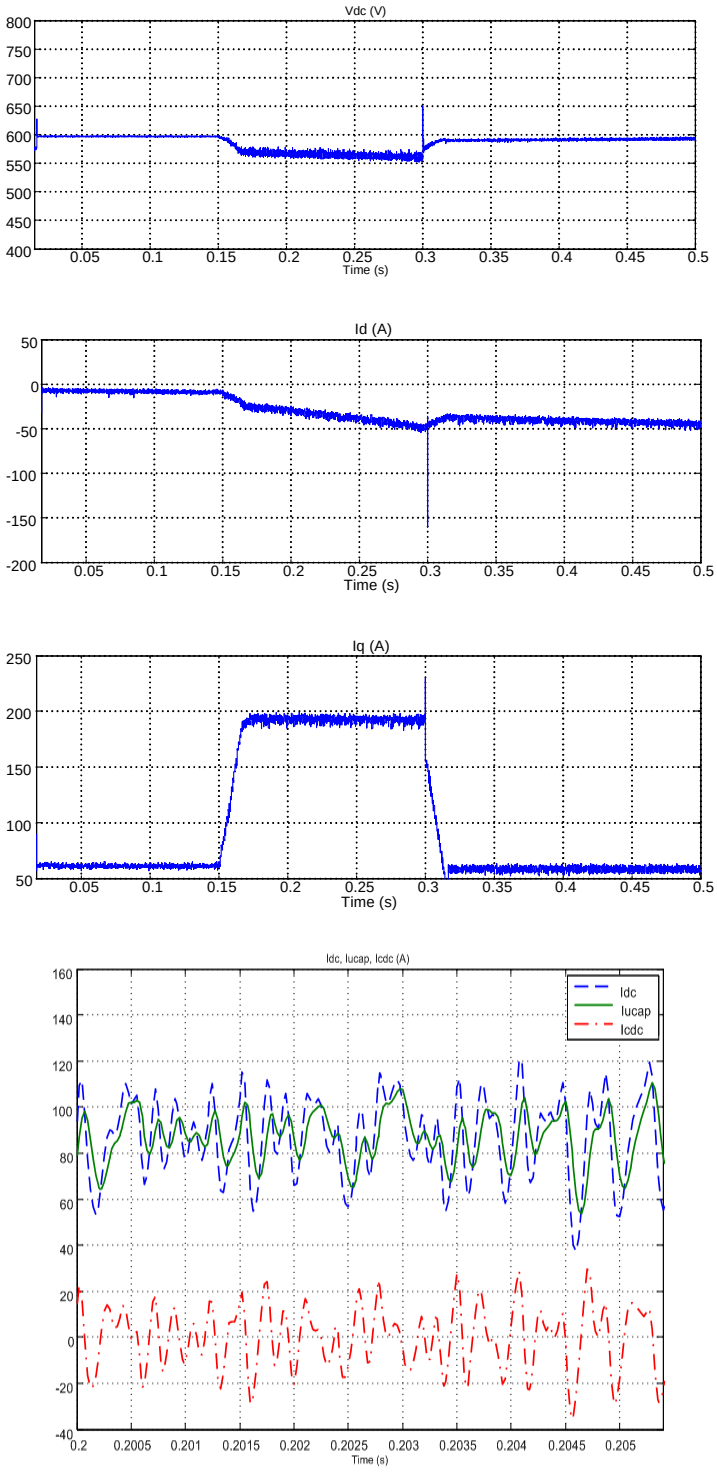


Figure 6-10 Integrated D-STATCOM and UCAP DC voltage under 3-phase fault on load bus (a) DC voltage, (b) D-STATCOM real current, (c) D-STATCOM reactive current. (d)Total DC current, UCAP current and DC capacitor current

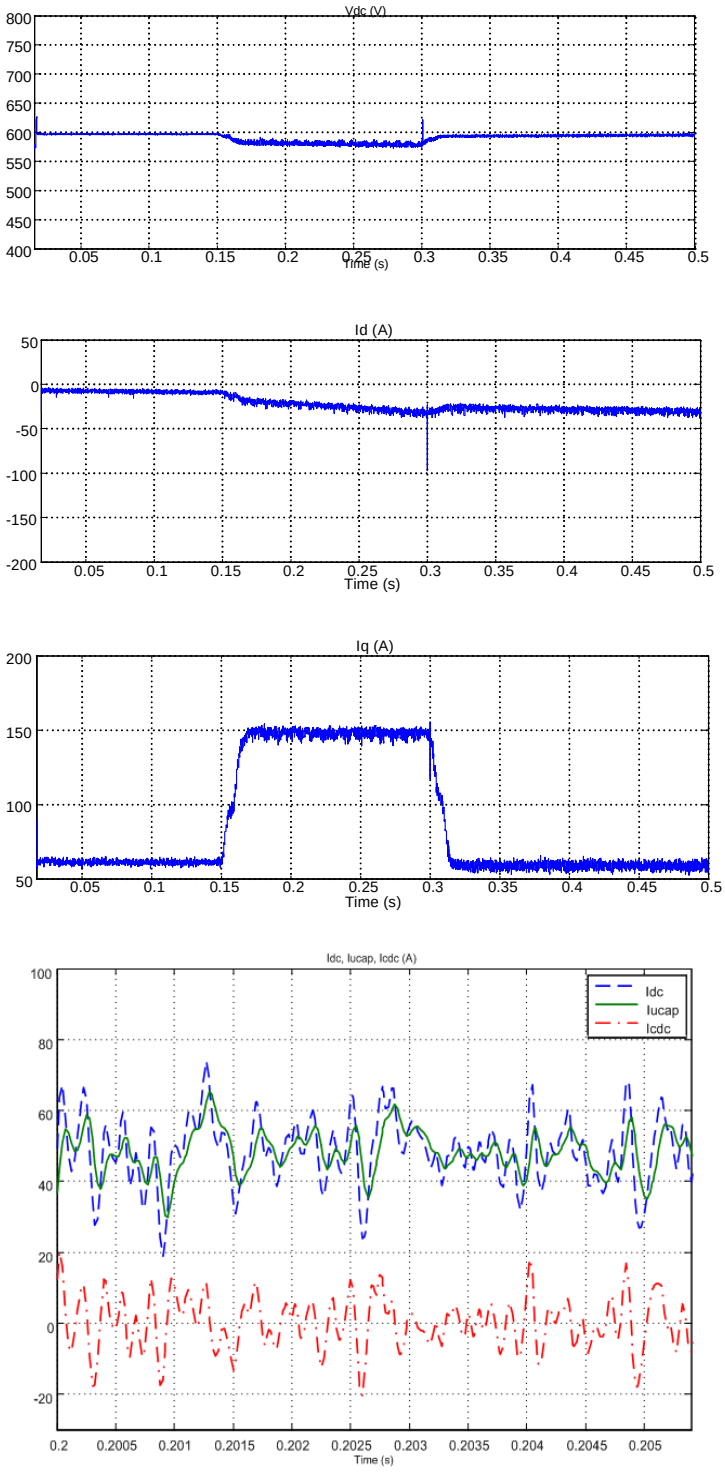


Figure 6-11 Integrated D-STATCOM and UCAP DC voltage under line-line fault on load bus (a) DC voltage, (b) D-STATCOM real current, (c) D-STATCOM reactive current. (d)Total DC current, UCAP current and DC capacitor current

The current spectra of the I_{dc}, I_{ucap} and I_{Cdc} for both these cases are shown in the Figure 6-12. The UCAP supplies the low frequency DC current variation and therefore reduces the DC voltage variation. The VSC DC capacitor then supplies only the high frequency current components, and therefore the size of the VSC DC capacitor can be reduced. In both these conditions, the I_d current component of the D-STATCOM is almost zero (except for that required to supply converter operating losses). Therefore, the UCAP integration with D-STATCOM reduces/eliminates the low frequency DC voltage variation of the VSC under any type of system disturbance and fault.

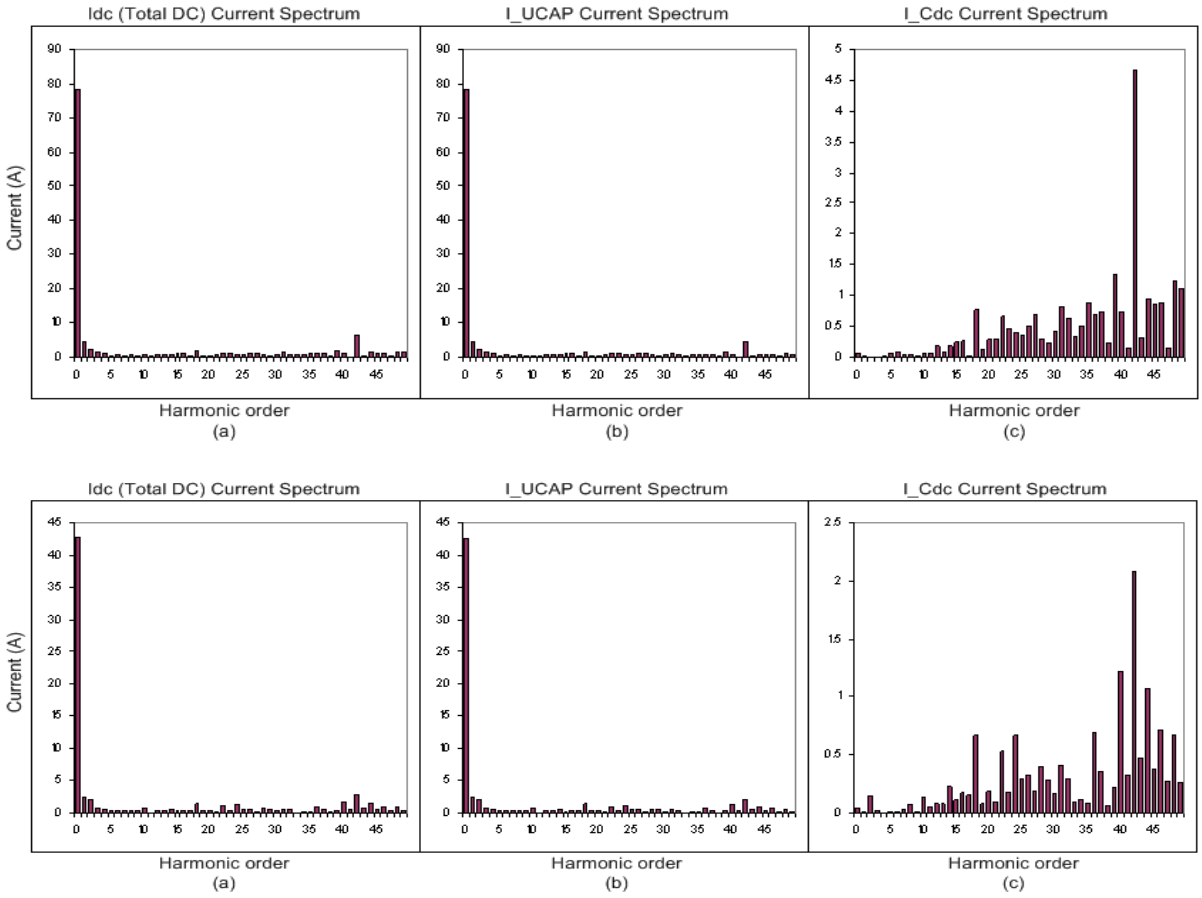


Figure 6-12 Integrated D-STATCOM and UCAP DC voltage under 3-phase fault on load bus (a) DC voltage (b) Total DC current, UCAP current and DC capacitor current

CHAPTER 7 CONCLUSIONS AND FUTURE WORKS

7.1 Conclusion

STATCOM as a shunt flexible AC transmission system (FACTS) controller has shown extensive feasibility in terms of cost-effectiveness in a wide range of problem-solving abilities from transmission to distribution levels. New inverter circuit topologies and advanced control technique promote the applications of STATCOM. However, how to control STATCOM during system faults poses the challenges to researchers.

This dissertation is dedicated to a comprehensive study of multilevel voltage source converter based STATCOM and its application, especially its operation during system fault. Firstly, the work of VSC based STATCOM modeling and control by previous researchers is reviewed. To further understand and analyze the controlled STATCOM, vector control and angle control are compared. The simulation results show the difference between these two control methods.

To solve STATCOM operation problem during system faults, “Emergency PWM” is proposed. Under normal condition, STATCOM is working with angle control. When a system fault is detected, “Emergency PWM” is implemented with angle control until the fault is removed. By this way, the switches are working in the 60Hz during normal time; there is no extra system loss. “Emergency PWM” can prevent over-current and trips in the VSC during and after system fault, and ensures that the STATCOM supplies required reactive power.

Based on normal three-phase PLL, “Instantaneous PLL” is proposed. By using the voltage vector angle as the output of PLL, “Instantaneous PLL” considers not only positive sequence, but also negative sequence, which is generated by system faults. Simulation shows that system with “Instantaneous PLL” has the same performance as system with normal PLL, and the system performance is improved by “Instantaneous PLL” during system faults. It means a system can implement normal PLL for normal operation, and switch to “Instantaneous PLL” at the fault.

Ice accumulated on power transmission lines in winter can cause severe damage to power system. VSC based STATCOM provides good asset utilization during the majority of the time when ice-melting is not required. By changing *Iq* reference under *Iq* regulation, fiving fixed angle for angle control to keep charging DC capacitors and changing DC voltage according the demanded DC current through transmission conductors, the STATCOM can perform the ice melting function when it is needed. The incremental cost for ice-melting capability is relatively small. The changeover procedure is simple and can be accomplished by remote control.

7.2 Future works

In this dissertation, the control of STATCOM is derived from the equivalent of VSC, where transformer is regarded as impedance. Due to the implementation of complicated non-linear transformer in the real system, a new model which combines STATCOM and non-linear transformer needs to be derived, and the control of this new model is an important challenge.

The current control can prevent over-current during system fault; also can control flux of saturable transformer. The study of B-H curve of saturable transformer and magniting saturation are posing challenges.

The idea of Supercapacitor as an energy storage integrated with STATCOM is presented in the dissertation. To develop a good model of Supercapaciotor and control system is one of the possible future works.

The performance of system with single STATCOM is presented in the report. The study of system with two STATCOM, such as power distribution, voltage drop, ect is a good topic.

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