

ABSTRACT

AGASHE, RUSHIKESH VIVEK. IEEE 1547 Compliant Communication Framework for a Distributed Energy Resource Interface. (Under the direction of Dr. Subhashish Bhattacharya and Dr. Mihail Sichitiu).

The Future Renewable Electrical Energy Distribution and Management (FREEDM) System is a revolutionary smart energy distribution system that has made remarkable contributions in the integration of smart energy devices, distributed renewable energy resources (DRER) and distributed energy storage devices (DESD) with the grid. The FREEDM System incorporates intelligent grid management to facilitate the seamless integration of distributed renewable energy resources with the grid. In the last couple of years, there has been tremendous research on developing an architecture for smart grids that will not only help reduce the dependence on depletable non-renewable resources but also provide a smarter energy distribution solution to maximize cost and energy savings. Distributed renewable energy resources and distributed energy storage devices have proved to be extremely valuable in situations of natural calamities where the utility grid is largely disrupted causing large areas of power outage. However, the renewable energy resources are highly dependent on natural conditions like sunlight and weather causing their energy profile to be intermittent in nature. To integrate such intermittent resources of energy with the grid requires great deal of energy management to provide a robust, reliable and efficient energy distribution solution. The distributed nature of these resources also implies that they may be manufactured by different companies, owned by different entities and even operated entirely independently. Proprietary protocols and custom interfaces make it very difficult for these resources to inter-operate.

In this thesis, we study the primary communication requirements of a smart grid and

survey existing communication technologies. We also explain the importance and need for standardizing the interface of DERs with the grid. We have picked a technology recognized as an IEEE 1547 eligible technology for a DER interface, for the study and development of a communication framework. The work for this thesis included the development of a Hardware-in-the-Loop (HIL) testbed on which the communication framework is deployed. Solid State Transformers which are an integral component of the FREEDM System were studied for the testbed development.

The developed communication framework provides full end-to-end communication between the end user and the DSP which controls the power electronics system. A two-tier scheme has been adopted which utilizes an ARM device (BeagleBone Black) as the communication end-point to the user. The BeagleBone Black runs higher level applications like data-logging and hosts a web-server which offers remote connectivity. These communication applications are deployed on the testbed for further analysis of the SST based system.

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IEEE 1547 Compliant Communication Framework for a Distributed Energy Resource
Interface

by
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DEDICATION

To my parents, Mr. Vivek Agashe and Mrs. Sneha Agashe and my brother, Mr. Pushkar Agashe. Thank you for all your support and encouragement.

BIOGRAPHY

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LIST OF ABBREVIATIONS

Abbreviation	Description
ADU	Application Data Unit
A-EPS	Area Electric Power Station
AMI	Advanced Metering Infrastructure
API	Application Programming Interface
BBBK	BeagleBone Black
CSV	Comma Separated Value
DAB	Dual Active Bridge
DER	Distributed Energy Resource
DESD	Distributed Energy Storage Device
DGI	Distributed Grid Intelligence
DNP	Distributed Network Protocol
DRER	Distributed Renewable Energy Resource
FID	Fault Isolation Device
FREEDM	Future Renewable Electric Energy Distribution and Management
HTML	Hyper Text Markup Language
HTTP	Hyper Text Transfer Protocol
IEM	Information Exchange Model
LAN	Local Area Network
MQTT	Message Queuing Telemetry Transport
PDU	Protocol Data Unit
QOS	Quality of Service
REST	Representational State Transfer
RT-HIL	Real-Time Hardware-In-the-Loop
RTU	Remote Terminal Unit
SCADA	Supervisory Control and Data Acquisition
SEP	Smart Energy Profile
SISO	Single Input Single Output
SOGI	Second Order Generalized Integrator
SPWM	Sine Pulse Width Modulation
SRF-PLL	Synchronous Reference Frame - Phase Locked Loop
SSL	Secure Sockets Layer
SST	Solid State Transformer
TCP/IP	Transmission Control Protocol / Internet Protocol
TLS	Transport Layer Security
XML	Extensible Markup Language

CHAPTER

1

INTRODUCTION

Over a hundred years ago, the electricity grid was conceived and the electricity needs then were simple. Power generation was localized and built around communities. The energy demands of most homes was small with a few light bulbs and a radio. The grid was designed for utilities to deliver power to customers and bill them monthly. The one-way interaction between the grid and the customers makes it very difficult for the grid to respond to events like power outage at the customer sites. The smart-grid technology introduces a two-way interaction to allow exchange of information between the utility and its customers. This communication facilitates monitoring and control and provides a tool to make the grid more reliable, efficient and secure. In recent years, there has been an increasing inclusion

of Distributed Energy Resources(DER) and Distributed Energy Storage Devices(DES) that depend on natural energy sources like wind and solar. This has led to tremendous research in the power electronics, communications and power systems domain to make these resources efficient and economically viable. The extensive research on Solid State Transformers(SST)[2] [25] [3] [22] [23] has contributed greatly to realize the smart grid.

1.0.1 Motivation

Utilities have realized that charging their customers at a flat rate is hardly efficient. [24] Electricity needs to be priced in a way such that it reflects the true cost and helps reduce the overall cost to provide cheaper electricity to its customers. Utilities typically adopt a scheme of time-varying pricing of electricity. Thus during hours of peak load electricity costs more. During such times DERs can act as a secondary resource and help reduce the net cost of electricity. DERs however are limited resources and it may not be possible to entirely replace the consumption from the grid. Often the most profitable solution turns out to be a combination of both. At any given time , a cost-optimal [16] ratio between grid power and power from DERs can be calculated. The consumption of grid power then, needs to be maintained at that cost-optimal power reference value. Any requirement of power over this reference value needs to be provided by the DER and this power requirement information needs to be communicated with the DER. To analyze the performance of the DER and its requirements on the communication interface a test setup is required. This motivates us to develop a DER testbed and a communication framework to analyze the communication dependent performance of a DER.

1.0.2 Contribution

The contribution toward this thesis can be categorized into two sections:

- Testbed Design and Implementation
- Implementing an IEEE 1547 Compliant DER Communication interface

During the early stages of work, the components of the DER testbed were identified and the controllers for each stage of the DER were designed. The controllers were designed using tools from MATLAB/Simulink and later implemented on microcontrollers. This was followed by the circuit simulation of the individual power electronics stages and validated using a Real-Time Hardware-in-the-Loop (RT-HIL) platform. An IEEE 1547 compliant communication framework was developed which consisted of a data-logging application and a web-application for remote monitoring and control. Finally the communication applications were deployed on the testbed for validation and testing.

1.0.3 Thesis structure

Chapter 1 provides a brief introduction to the Smart Grid technology, renewable energy resources and its growing inclusion in today's energy supply. In Chapter 2, we have identified the core communication requirements of a smart grid and identified some of the existing communication technologies in the Power Systems Industry. Chapter 2 also describes the various cost saving and energy saving applications of communications in smart grids. In Chapter 3, the design and control of a SST based system has been explained. The design of the SST system was adopted and inspired from the work of Yonghwan Cho[6]. Each stage of the SST is carefully designed for the design requirements of the system. The implementation however is flexible and can be easily adopted for a system with different specifications.

In Chapter 4, detailed descriptions of the implementation of various components of the SST based system are given. The communication framework developed as a part of this Thesis is also explained in detail. Lastly, an analysis is presented to show the impact of communication and system latency on the performance of a DER.

CHAPTER

2

COMMUNICATION IN POWER SYSTEMS

In Chapter 1, we looked at an introduction to smart grids and there has been an ongoing effort to make smart grids more efficient and ubiquitous. The need for communication between the utility, substation and consumers was recognized a few decades ago but its importance and need has drastically changed over the years. In this section, we will review the requirements of the communication infrastructure and some of the most common communication protocols in the power systems industry. This section also provides an introduction to the FREEDM Systems architecture and the communication scheme applied.

2.1 Communication Requirements

Over the last few years, various communication technologies have been used in power systems, each with its own advantages and disadvantages and thus the global market has not adopted any one particular technology. The IEEE Standards committee is making an effort to standardize or recognize as a part of the standard, the protocols that are best suited for the various components of Power Systems. The communication technology has become particularly important with the transition from a traditional grid to a smart grid. The following sections describe the communication requirements of a smart grid[13].

2.1.1 Bandwidth

A distribution substation collects information from a large number of feeders which in turn collect data from local smart energy devices. With the increasing number of smart energy devices adding to the smart grid network, the bandwidth requirement is continually increasing.

2.1.2 Latency

Given the large number of applications in a smart grid, each application has a different latency requirement. Some applications require real-time communication with hard time bounds. Typical applications that have real-time requirements are sensors, power systems controls and certain safety applications. The latency requirements of various applications are listed in the Table 2.1 as described in [13].

Table 2.1 Data Communication Latency Requirements

Application	Latency Requirement
Demand Response	2 s - 5 min
Remote connect/disconnect	2-5 s
AMI, real-time pricing	2 s
Outage Management	300 ms - 2 s
Emergency Response	10-100 ms
Protection event notification	3-10 ms

2.1.3 Interoperability

As quoted in [13], *"Interoperability is the ability of two or more networks, systems, devices, applications, or components to communicate and operate together effectively and securely, without significant user intervention"*. To provide for interoperability, manufacturers and vendors must agree on a using the same physical interface and protocol or set of protocols. Trade alliances like SunSpec Alliance are making the effort to publish specifications that are compliant with an IEEE Standard like IEEE 1547 to provide interoperability to participating entities.

2.1.4 Scalability

The smart grid involves a large number of smart energy devices, customers and sensors spanning over a large geographical area. Given the latency requirements of some critical components, the processing of data needs to be distributed instead of centralized. In spite of this distribution, the data to be handled can be very large and the communication infrastructure must be able to support the increasing data volumes.

2.1.5 Security

The distributed smart energy devices communicate personal information of customers for billing and usage history as well as system critical controls information. A network breach could cause havoc and possibly large power outages. The smart grid can operate optimally only if a reliable, robust and secure communication infrastructure is present. Network security is thus vital to a smart grid infrastructure.

2.2 Communication Protocols

A communication protocol defines a data format, a message format and may also define a communication medium as a part of the protocol. This allows different entities using the same protocol to communicate with each other. The protocols discussed in this section are pertaining to SCADA systems. SCADA stands for Supervisory Control and Data Acquisition and is a very important component of Power Systems. SCADA systems became popular in early 1960s as systems were built to monitor and control remote devices. SCADA protocols have been in use in Power Systems ever since and continue to be used very widely.

In recent years, energy production and distribution is transforming from the traditional centralized grid to a distributed smart grid. The communication requirements for a smart grid are different from the traditional grid and has led to the development of a large number of new communication protocols. Integration of Distributed Energy Resources(DER) with the traditional grid requires a robust and reliable communication interface with the DER. Table 2.2 lists the protocols eligible for a DER interface as specified in IEEE 1547.3. The following sections provide a brief overview of the protocols mentioned in table 2.2.

Table 2.2 IEEE1547.3 eligible protocols for DER interface

Protocol	Transport Layer	Physical Layer
IEEE Std 2030.5 (SEP2)	TCP/IP	Ethernet
IEEE Std 1815 (DNP3)	TCP/IP	Ethernet
SunSpec Modbus	TCP/IP	Ethernet
	N/A	RS-485

2.2.1 SEP2.0

Smart Energy Profile (SEP2) is a protocol developed for smart grid applications, particularly for the interface of smart energy devices with the grid. The SEP2 protocol was adopted as IEEE Std 2030.5 in 2013. The SEP2 protocol is designed to run over TCP/IP and follows a RESTful architecture. The protocol is built around the RESTful methods like GET, POST, HEAD, PUT, DELETE along with a lightweight subscription based mechanism. Along with the required HTTP interface for SEP2, any other RESTful Application Layer protocols can be used with SEP2. Since, SEP2 does not define the lower layer protocols, a complete end-to-end solution may involve a variety of other protocols[18]. More information about SEP2 can be found in [26].

2.2.2 DNP3

DNP was developed in the 1990s to serve the functions of transmitting data, control messages and provide services which could work with limited bandwidth. DNP is a master-slave protocol but allows for unsolicited slave response for quick notifications. Typically a master cyclically polls each slave device at regular intervals requesting specific data. DNP3.0 also known as DNP3 is the latest revision of the protocol in use and is an open and public proto-

col. DNP3 was originally developed for serial point-to-point communication but with the evolution of IP networking, DNP3 added the capability to send messages over high-speed, packet based IP networks. Some of its features are described below:

- Data Timestamp - The timestamp for the data is recorded at the device level which allows the master to generate a time sequence report.
- Message Broadcasting - Allows large number of nodes to be addressed at once.
- Data Grouping - This allows the master to selectively poll for data.
- Quality Flag - Provides information about data validity.
- Report-by-exception - Only data that has changed is transmitted thus reducing the the number of data points transmitted.

All these features have made DNP3 a very popular SCADA protocol in Power Systems especially in North America and was also adopted as IEEE Standard 1815[19] in 2010.

2.2.3 Modbus

This section provides an overview of the Modbus protocol. Information on SunSpec Modbus can be found in section 2.3.1

Modbus was developed in 1979 as a SCADA protocol to enable communication between automation devices[29]. Modbus is very widely used in a large variety of industries including the Power Systems industry. It is an open protocol developed with industrial applications in mind. Modbus is a register-based protocol and uses request-response messaging. The master-slave mechanism implies that the master device must initiate a request and wait for the slave to respond and is responsible for initiating all transactions.

The data on a slave device is stored in data banks and Modbus specifies 4 such data banks. Table 2.3 lists information about the 4 data banks. The master must poll the slave by sending a message to request for data from these data banks.

Table 2.3 Modbus Data Banks

Data Bank	Data Type	Master Access	Slave Access
Coils	boolean	read/write	read/write
Discrete Inputs	boolean	read-only	read/write
Holding Registers	unsigned word	read/write	read/write
Input Registers	unsigned word	read-only	read/write

The protocol's definition of a message comprises of a Protocol Data Unit(PDU) and a Application Data Unit (ADU). The Modbus PDU consists of a function code, and an address range of the data. The Modbus ADU defines the network protocol to be used. Three standard ADU formats are TCP, RTU and ASCII. Figure 2.1 depicts a Modbus Frame[8]. In a typical

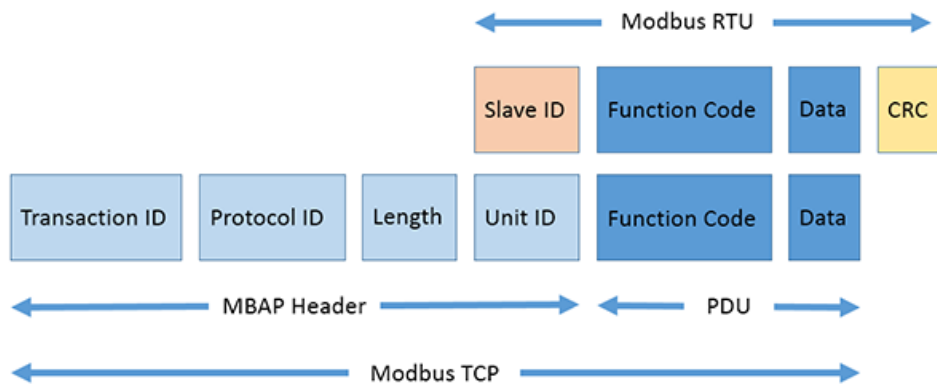


Figure 2.1 Depiction of a Modbus Frame

application, the master polls the slave and receives all data in the address range specified in the request. The master must have knowledge about the datapoint-to-address mapping in order to interpret the received data.

2.3 Information Exchange Models

In the previous sections, some of the popular communication protocols in Power Systems have been described. These protocols define the data format, message format and communication medium. The data however, is application dependent and thus the organization and interpretation of the data is left to the application developer.

An Information Exchange Model(IEM) provides data organization and structuring of information that is commonly exchanged between various entities by defining the model structure, typically in the form of an XML Schema. The main advantage of defining an IEM is that any two devices will be able to interpret data exchanged between them as long as they are using the same IEM.

To interface DERs with the grid, it is important that various DER manufacturers adopt a standardized protocol and adhere to a specification of IEMs. Some of the existing standards for IEM are IEC 61970, IEC 61968, IEC 62056 and IEEE 1547.3. IEEE 1547.3 specifies mandatory information elements that need to be supported by a DER and to ensure interoperability it states that unified information models and non-proprietary protocol encoding must be used.

Of the IEEE 1574.3 eligible protocols for a DER interface, SunSpec Modbus is based on the Modbus protocol which is very widely used in industrial applications. Due to its widespread use, industries are more interested in finding a solution that is built on top of the existing infrastructure. This makes SunSpec Modbus a popular choice. SunSpec

Modbus is an implementation of the Modbus protocol that adheres to the SunSpec Modbus Interface specification developed by the SunSpec Alliance which publishes interoperability specifications and information models that are free and open source. The following sections describes the SunSpec Modbus Interface specification in more detail.

2.3.1 SunSpec Specification

A Modbus protocol implementation that is compliant with the SunSpec Alliance's SunSpec Modbus Interface specification is termed as SunSpec Modbus. The goal of the specification is to reduce system implementation cost[28] by enabling applications to be written using a standard view, independent of the manufacturer of the component. This enables devices to inter-operate with other devices adhering to the specification.

The SunSpec Information Model Specifications govern the Modbus communication on the DER interface. The Information Model describes the set of data points that are associated within a functional block[28]. A collection of two or more models forms a device definition as shown in the diagram below: Standard Models are models identified as a part

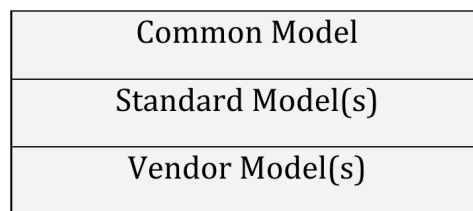


Figure 2.2 SunSpec Modbus Device Definition

of the SunSpec Specification while Vendor Models are custom to a Vendor and may be registered with SunSpec for compliance. These models help to organize and categorize the data on the slave device. The device definition, wrapped with the 32-bit 'SunS' (0x53756e53)

identifier at the top and an End Model at the bottom form the SunSpec Modbus device map. Figure 2.3 depicts the SunSpec Modbus device map. All SunSpec compatible devices

'SunS' (0x53756e53)
Common Model
Standard Model(s)
Vendor Model(s)
End Model

Figure 2.3 SunSpec Modbus Device Map

must have the 'SunS' identifier as the first element and the End Model as the last block in their device map. The Common Model and Standard Model/Vendor Model are described in the following sections.

2.3.1.1 Common Model

The Common Model is the first model in the device definition and contains static information about the device. Each data value in the model is called a data point. Table 2.4 lists the data points that make up the Common Model.

2.3.1.2 Standard Model/Vendor Model

The Common Model is followed by one or more Standard or Vendor Models. These models contain the data points specific to a device. Standard Models contain pre-defined data points identified as a part of the SunSpec specification. Vendor Models contain data points that are custom to a vendor's device. For example, Table 2.5 shows the data points of a

Table 2.4 Data Points in a Common Model

Point Id	Description	Point Type	Value
ID	Model Identifier	uint16	1
L	Model Length	uint16	65 or 66. Pad is required if L=66
Mn	Manufacturer Name	string	<user defined>
Md	Model Number	string	<user defined>
Opt	Options	string	<user defined>
Vr	Version Number	string	<user defined>
SN	Serial Number	string	<user defined>
DA	Device Address	uint16	<user defined>
Pad	Data-alignment Padding	pad	32768

Standard Model for a cellular link.

Table 2.5 Data Points in a Standard Model for a cellular interface link

Point Id	Description	Point Type	Value
ID	Model Identifier	uint16	18
L	Model Length	uint16	22
Nam	Interface Name	string	<user defined>
IMEI	International Mobile Equipment Identifier	uint32	<user defined>
APN	Access Point Name	string	<user defined>
Num	Phone Number	string	<user defined>
PIN	Personal Identification Number	string	<user defined>

2.3.2 Model definition as an XML file

XML stands for Extensible Markup Language[7] and is a very commonly used language for information formats and representing structured data. The IEMs as described in section 2.3 provide structural information and an XML format is best suitable for such application. Each information model contains data points and each data data point has a set of attributes that describe a data point. Table 2.6 lists the attributes that describe a datapoint.

Table 2.6 Attributes of a data point

Attributes	Mandatory	Default Value
id	Yes	-
len	No	-
offset	Yes	-
type	Yes	-
sf	No	-
units	No	-
access	No	read only
mandatory	No	false
category	No	measurement

2.4 Communication in the FREEDM System

2.4.1 Overview of the FREEDM System

The FREEDM System is a revolutionary distribution system that enables the integration of highly distributed and scalable energy resources with the traditional power systems.[17].

Figure 2.4 depicts the FREEDM Systems Architecture.

The SST connects to the medium-voltage(MV) grid through a Fault Isolation Device (FID). The FID is a solid-state circuit breaker and it performs the task of isolating the SST from the MV grid when a fault occurs. Figure 2.4 also shows a Distributed Energy Storage Device(DES), Distributed Renewable Energy Resources(DRER) and a Load attached to the DC grid provided by the SST. The DRER and DESD contain DC-DC converters. The SST also has an interface to the low-voltage(LV) residential AC grid. Each component of the SST has a communication interface and is controlled by a DSP and an ARM board. The ARM board runs higher level applications such as Distributed Grid Intelligence (DGI) whereas the DSP board is used to control the power electronic systems. The ARM board runs additional functions like analytics, communication with other ARM boards and data logging to make the FREEDM system more reliable and efficient. In the following section we will describe the communication functionality of the FREEDM System in more detail.

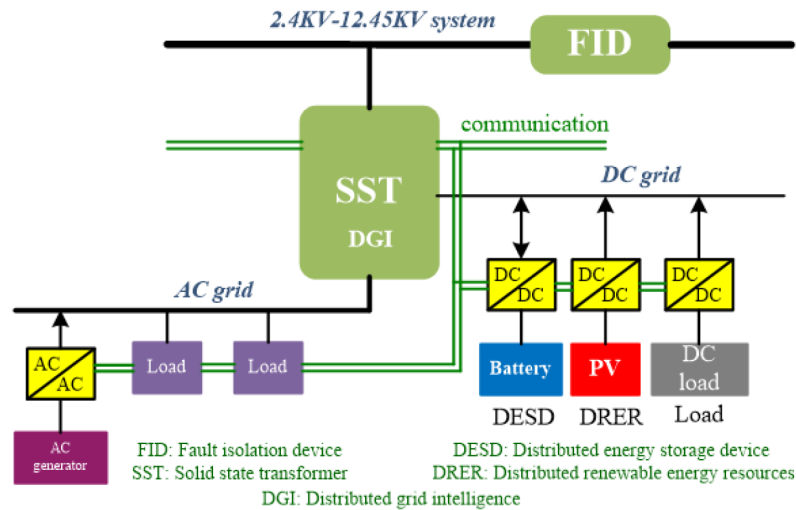


Figure 2.4 FREEDM Systems Architecture

2.4.2 DER interface communication scheme

The FREEDM system is highly dependent on a reliable and robust communication infrastructure. In context of the FREEDM system, a DER consists of the DRERs, DESD and the SST. The DER interface refers to the interface between the SST and the MV or LV AC grid. This section describes a communication scheme to communicate with a DER. Figure 2.5 depicts the communication architecture. A two-tiered communication scheme is proposed. At the Area Electric Power System(A-EPS) interface, there is a computer or microcontroller which is the communication end-point of the EPS. In this setup, a BeagleBone Black(BBBK) which is a low cost linux based ARM board is used. The BBBK communicates with the DSP using the SunSpec Modbus protocol. The BBBK - DSP communication takes place over a LAN network. The BBBK acts as a master and the DSP acts as a slave in the BBBK - DSP communication.

The BBBK acts as a data logger and must poll the slave device periodically for data. The collected data is stored in a database file on the BBBK and this data is made available at the DER interface over a LAN network. The DSP is responsible for controlling the power electronics system and must respond to the Modbus client by providing data over a serial link. An off-the-shelf Modbus RTU/TCP converter is used to provide a serial link to the DSP and an Ethernet interface to the BBBK. A network switch is introduced for scalability.

The web-interface shown in Figure 2.5 represents the interface for the operator who monitors the data and sends commands to control the power electronic system. The operator may use a HTTP or MQTT based application to request for data from the BBBK over the LAN network. Chapter 4 provides more detailed explanation and implementation specifics of this communication scheme.

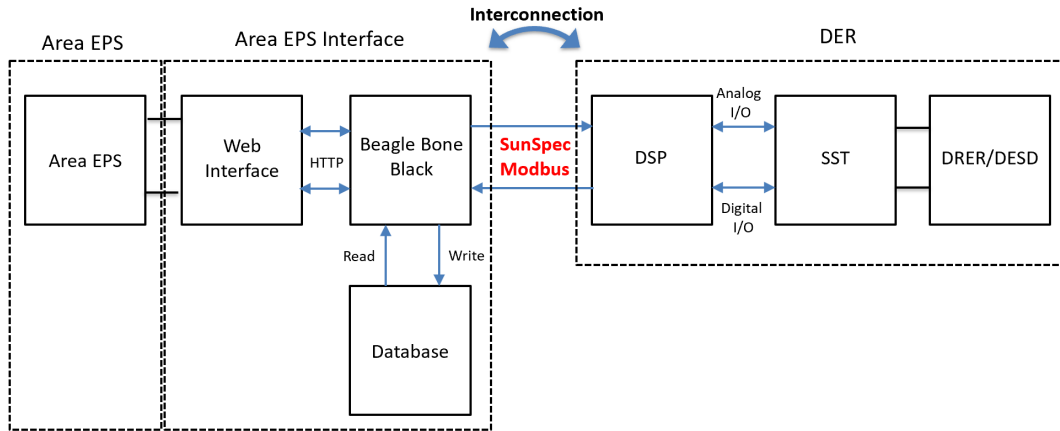


Figure 2.5 DER Interface Communication Architecture

2.5 Applications of communication in Power Systems

Communication Protocols in power systems play a vital role in realizing the smart grid. Some of the important applications are described below.

2.5.1 Automatic Power Restoration

The conventional grid does not provide for detection of power outages. The smart grid technology aims toward automatic detection of power outages and autonomous restoration. Distributed Energy Resources and Distributed Grid Intelligence(DGI) have made it possible to re-route power to areas that need it the most. Local DERs or even distant DERs can feed power into the grid to make up for the absence of the grid in a power outage. This process is highly dependent on a reliable and robust, low-latency communication infrastructure.

2.5.2 Plant Maintenance

Communication systems in smart grids provide great functionality and flexibility to energy providers. A planned shutdown for plant maintenance could cause partial or complete outage without the presence of DERs. A good communication infrastructure will allow energy providers to perform a planned shutdown, affecting its customers minimally. DERs have their own limitations and their energy production is affected by natural factors like sunlight, wind and rain. Thus, every DER feeds power into a grid based on its own capacity. A communication network allows DGI to take into consideration the limitations of DERs and make power sharing decisions to maintain optimal energy supply.

2.5.3 Grid Faults

Grid faults like over-voltage, under-voltage, over-frequency, under-frequency, high rate of change of frequency can all affect the DERs connected to the grid. Protection of DERs becomes very important in such situations and novel strategies like ones described in [1] are being implemented. Communication technology plays a vital role in monitoring the grid parameters and making decisions to autonomously disconnect and reconnect to the grid.

2.5.4 Power Factor Correction

With a large number of DERs feeding into the grid, the responsibility of maintaining a good Power Factor is not only the responsibility of the Grid but also each DER plugging into the grid. Power Factor Correction [20] becomes a very important task and the presence of a good communication infrastructure can greatly enhance the efficiency of Power Factor correction.

2.5.5 Peak Shaving

Peak shaving [12] is used to reduce energy consumption during periods of maximum demand from the utility. This saves customers substantial amount of money as the energy cost is higher during peak hours. DERs can prove to be a very economical choice to offset the reduction of energy consumed from the utility. A good communication infrastructure will facilitate optimum distribution of energy from DERs to maximize cost savings. This not only saves money for the customer but the utility too benefits from peak shaving as they are not required to use the costly peaking generators that frequently. A smart grid uses historical data and dynamic load measurements to optimally balance the operating power levels of DERs.

CHAPTER

3

DESIGN AND STUDY OF SOLID STATE TRANSFORMERS

3.1 SST Design

In this chapter the design and control strategies for the SST and DESD of the FREEDM System are discussed. The strategies for the operation of multiple SSTs in parallel are described in detail in [5].

The control strategies described in this chapter are designed with an intent to keep the control design as simple as possible. More efficient strategies can be designed as required

and can be found in [6] [10] [33] [30] [11]. The primary aim of setting up the SST system is to test the communication ability of the FREEDM System and to study the effect of latency of communication on the efficiency of the SST System. The communication capabilities of the FREEDM System help the SST system carry out tasks like islanding and reconnection efficiently.

Table 3.1 Circuit Parameters of the SST testbed

Parameter	Value
Grid Voltage (V_{g-nom})	120 V
Grid Frequency (f_g)	60 Hz
F_{ISR}	10 kHz
F_{SW-HB}	20 kHz
F_{SW-DAB}	10 kHz
F_{SW-BB}	10 kHz
V_{HDC}	250 V
V_{LDC}	150 V
V_{bat}	140 V
L_g	1 mH
L_{bat}, R_{bat}	5 mH, 0.4 Ω
L_{filter}, R_{filter}	4 mH, 0.1 Ω
L_{lkg}	24 μ H
C_{HDC}	3900 μ F
C_{LDC}	2400 μ F
$n : 1$	1 : 1
R_L	100 Ω

Figure 3.1 shows the nomenclature and the circuit diagram of the SST and DESD in detail. Table 3.1 lists the parameters of the SST System. The grid is assumed to have a nominal voltage of V_{g-nom} . The Inverter and DAB are switched at F_{SW-HB} and F_{SW-DAB} respectively while the buck-boost converter is switched at F_{SW-BB} . The control loop and

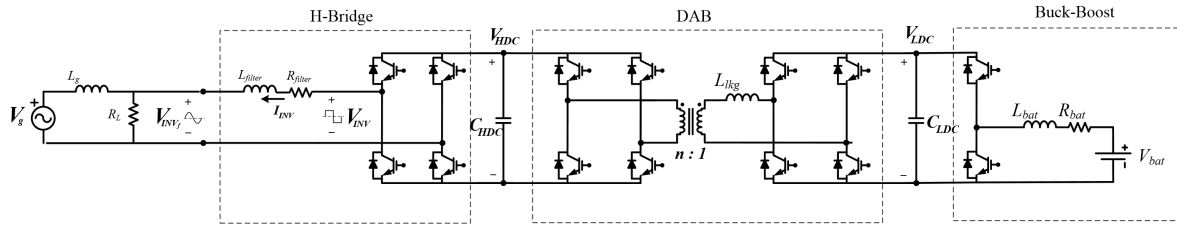


Figure 3.1 Circuit diagram of grid-connected SST and DESD

sampling runs at a frequency of F_{ISR} .

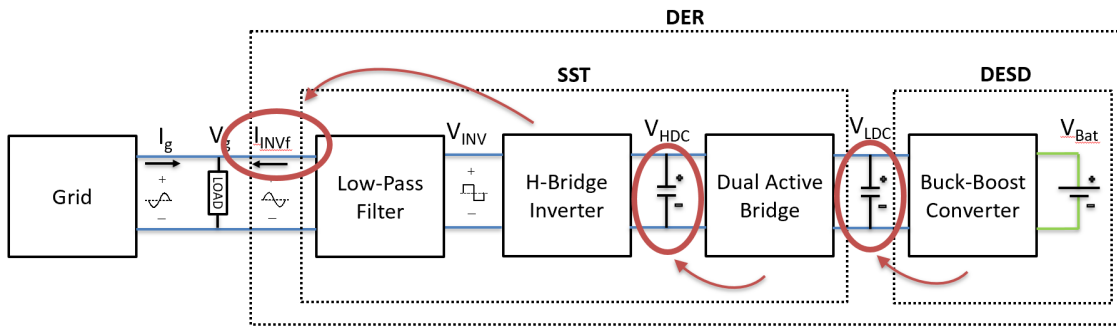


Figure 3.2 Overall control strategy

The control of the SST system is divided into 3 stages. As shown in Figure 3.2, the low-voltage DC(LVDC) link is regulated by the Buck-Boost Converter and the high-voltage DC(HVDC) link is regulated by the DAB. The H-Bridge Inverter uses a current controller to regulate the output current. The controllers for all three stages are described in detail below.

3.1.1 Bi-directional Buck-Boost Converter

The bi-directional Buck Boost converter is responsible for regulating the LVDC link and it is the interface between the battery and the LVDC link. The converter uses a bi-directional topology as the power flow in an SST system can be from the battery to the grid when the battery is discharging and from the grid to the battery while charging. The bi-directional Buck-Boost converter consists of a half-bridge, an inductor $sL_{bat} + R_{bat}$, a load R_L and an output capacitor C_{LDC} . Figure 3.3 depicts the circuit diagram of the Buck-Boost converter. The controller for the Buck-Boost converter is presented below.

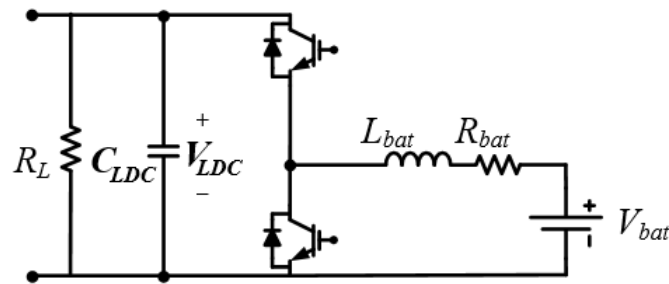


Figure 3.3 Circuit diagram of the Buck-Boost converter

3.1.1.1 Controller Design

The controller for the Buck-Boost converter uses a single-loop structure and it was designed using MATLAB's *sisotool*. From the circuit diagram of the Buck-Boost converter it is clear that it is a second order system. The control-to-output transfer function presented in equation

3.1 is a simplified version of the equation given in [31]:

$$G_{dv} = G_{do} \frac{(1 - \frac{s}{w_z})}{1 + \frac{s}{w_0 Q} + \frac{s^2}{w_0^2}} \quad (3.1)$$

where

$$G_{do} \approx \frac{V_{LDC}^2}{V_{bat}} \quad w_z \approx \frac{R_L}{L_{bat}} \left(\frac{V_{bat}}{V_{LDC}} \right) \quad w_0 \approx \frac{1}{\sqrt{L_{bat} C_{LDC}}} \left(\frac{V_{bat}}{V_{LDC}} \right) \quad Q \approx w_0 R_L C_{LDC}$$

In order to regulate the LVDC link voltage, a controller with zero steady state error is desired. This is not possible to achieve using just a proportional controller and thus, we will be using a proportional-integral controller for this stage. MATLAB's *pidTuner* is a very handy tool for tuning the PI-controller and observing its characteristics.

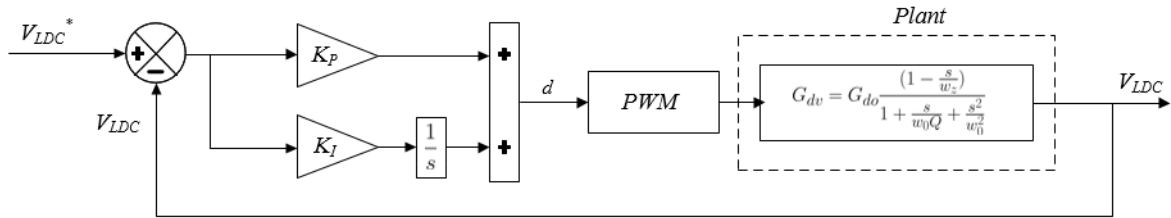


Figure 3.4 Buck-Boost PI-controller block diagram

Figure 3.4 depicts the PI-controller of the Buck-Boost converter. Table 3.2 lists the controller characteristics for the tuned PI-controller for the Buck-Boost converter.

Another very useful tool in MATLAB is the *sisotool* which allows us to analyze a SISO (single-input single-output) system and generate the bode-plot and step response of the system. Figures 3.5 and 3.6 show the bode-plot of the loop gain and the step-response of the closed-loop system respectively.

Table 3.2 PI controller characteristics for Buck-Boost converter

Parameter	Value
K_P	3.41
K_I	750
Rise Time	0.073 ms
Settling Time	0.592 ms
Overshoot	15.8%
Steady State Error	0%
Bandwidth	3 kHz
Phase Margin	62.5°

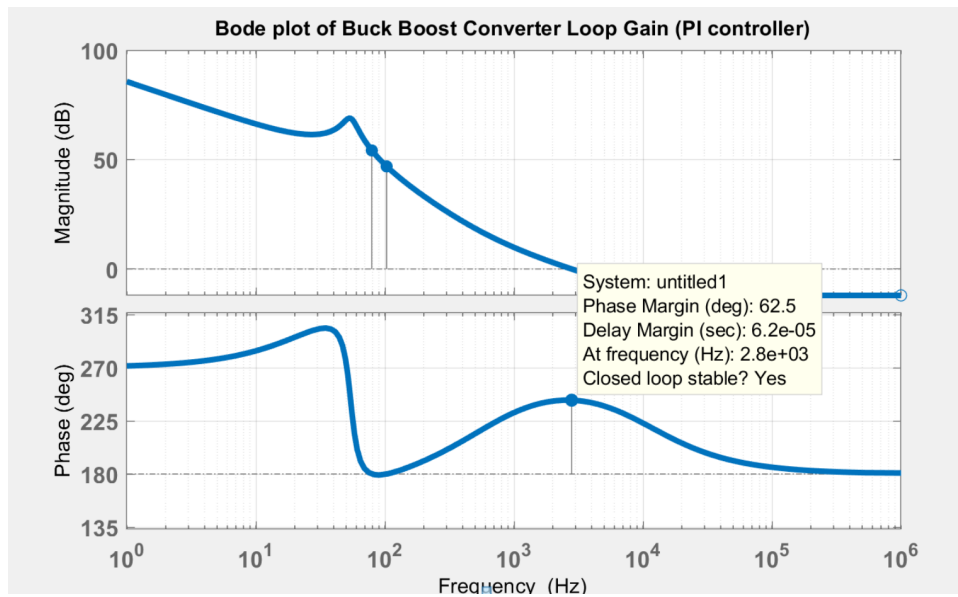


Figure 3.5 Bode plot of Buck-Boost Converter loop gain

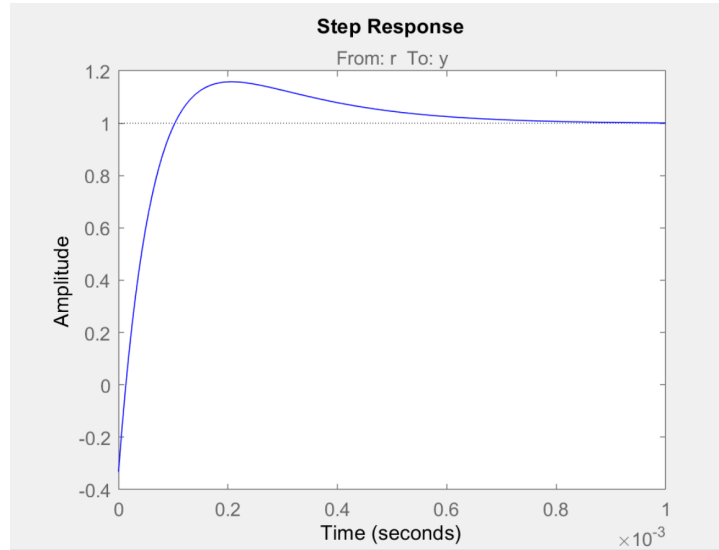


Figure 3.6 Step response of the Buck-Boost closed-loop system

3.1.2 Dual Active Bridge(DAB)

The DAB is a highly flexible bi-directional dc-dc converter. It consists of two full-bridges, a high frequency transformer, and capacitors on the DC links[14]. The symmetry of the converter enables the bi-directional power flow and makes this converter a great choice for the SST system.

The DAB is the interface between the LVDC link and the HVDC link and is responsible for regulating the HVDC link. Referring to 3.1, the HVDC link is to be regulated at a reference voltage of V_{HDC} . Figure 3.7 depicts the circuit diagram of the DAB.

3.1.2.1 Controller Design

Similar to the Buck-Boost converter's PI-controller, the DAB also uses a PI-controller with a single-loop structure and can be designed using a similar approach. The direction of power flow is determined by the phase difference between the gating pulses to the two full-bridge

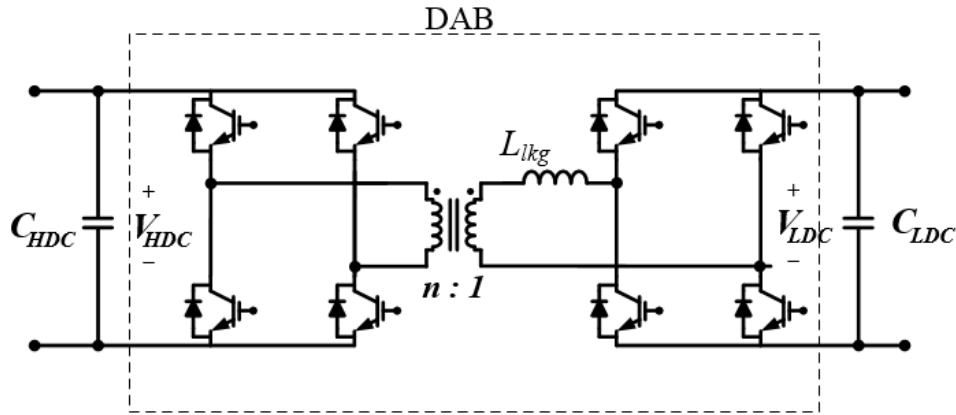


Figure 3.7 Circuit diagram of the DAB stage

legs of the DAB. The PI controller controls the phase difference of one leg with respect to the other to regulate the HVDC link voltage, V_{HDC} . Figure 3.8 depicts the PI-controller of

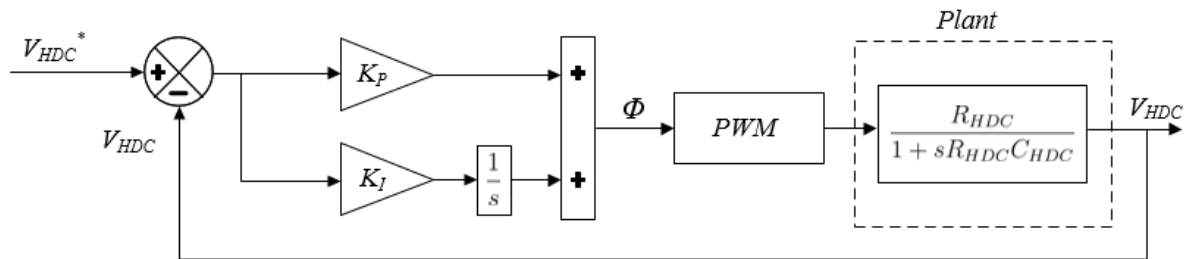


Figure 3.8 DAB PI controller block diagram

the DAB and Table 3.3 lists the controller characteristics for the tuned PI-controller for DAB.

Figure 3.9 shows the bode plot of the loop gain and Figure 3.10 shows the system's response to a step change.

Table 3.3 PI controller characteristics for DAB stage

Parameter	Value
K_P	20.0
K_I	9.241
Rise Time	0.429 ms
Settling Time	0.767 ms
Overshoot	0%
Steady State Error	0%
Bandwidth	1 kHz
Phase Margin	90°

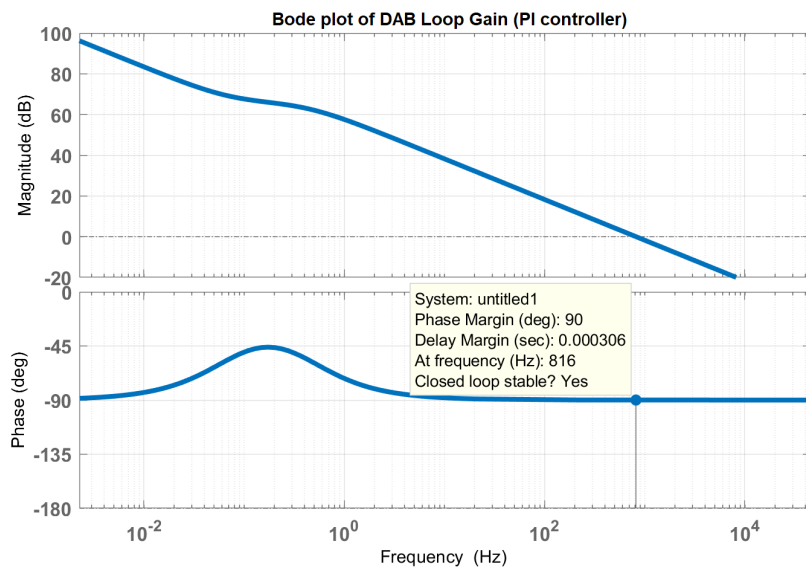


Figure 3.9 Bode plot of the DAB loop gain

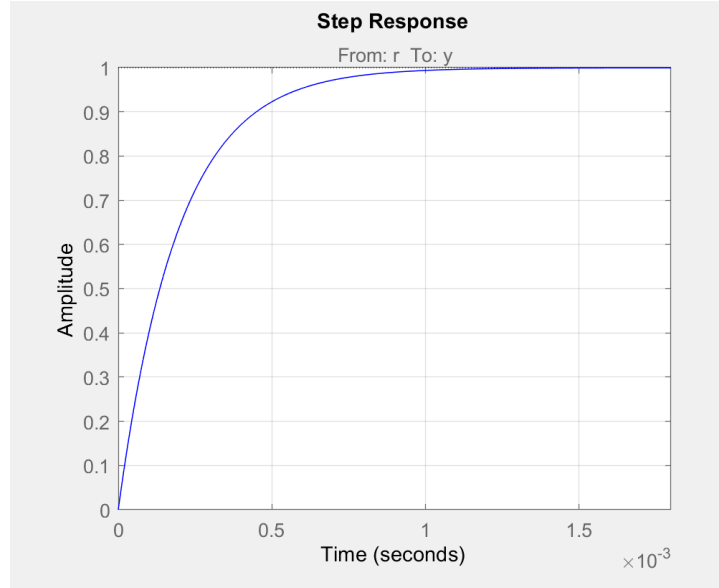


Figure 3.10 Step response of the DAB closed-loop system

3.1.3 H-Bridge Inverter

The H-Bridge Inverter consists of a H-Bridge and a LR-filter. The LCL filter is also a very popular choice and can be used as described in [32]. As mentioned previously, the goal is to design a controller as simple as possible and thus, we have chosen a LR-filter. This stage performs the task of converting the HVDC voltage to a sinusoidal AC voltage and is responsible for regulating the output current I_{INV} . Since, this stage will be connected to the grid, the voltage on the inverter’s output link will be fixed by the grid. This enables us to indirectly regulate the SST’s reference power by regulating I_{INV} . Figure 3.11 depicts the circuit diagram for the H-Bridge inverter. To generate a sinusoidal output, the inverter needs to be switched using a high-frequency triangular or saw-tooth carrier waveform and a sinusoidal waveform of the desired output frequency, f_g . This technique is commonly known as sine-PWM (SPWM). It is clear that frequency components of the output waveform

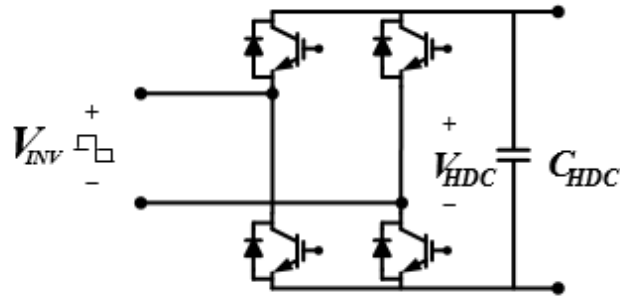


Figure 3.11 Circuit diagram of the H-Bridge inverter

will consist of the fundamental frequency, f_g , the converter's switching frequency F_{SW-HB} and its harmonics. Thus, to generate a clean sine-wave of frequency f_g , a low-pass filter of suitable bandwidth and cut-off frequency is required. The following sections describe the design of the LR-filter and the controller for this stage.

3.1.3.1 Filter Design

The LR-filter is a simple first-order low pass filter than can be used to filter out F_{SW-HB} and its harmonics. Figure 3.12 shows the circuit diagram of the LR-filter. To design an efficient filter, it is very important to decide the cut-off frequency correctly. We know that the grid frequency is f_g and the switching frequency is F_{SW-HB} . A good ballpark value for the cut-off frequency is the geometric mean of the largest frequency to be passed and the smallest

Table 3.4 PR controller parameters for H-Bridge Inverter

Parameter	Value
K_P	0.9
K_R	200

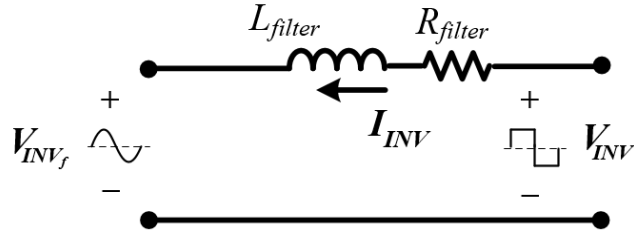


Figure 3.12 Circuit diagram of the LR low-pass filter

frequency to be filtered. Thus we get,

$$f_c \approx \sqrt{f_g * F_{SW-HB}}. \quad (3.2)$$

We also know that for a LR-filter the cutoff frequency is given by,

$$f_c = \frac{1}{2\pi} \frac{R}{L} \quad (3.3)$$

and for the parameters listed in Table 3.1, the cut-off frequency is, $f_c \approx 400Hz$

3.1.3.2 Controller Design

The H-Bridge Inverter is the interface between the HVDC link and the AC link. This stage of the SST system uses a current controller to regulate the inverter output current I_{INV} . Traditional PI-controllers are a great choice for regulating DC quantities as they provide infinite gain at DC and zero steady-state-error. For AC quantities, the PR controller proves to be superior as it can provide infinite gain at a desired frequency. For the inverter application, a PR controller tuned to provide infinite gain at the fundamental frequency, f_g will provide better performance in comparison to a PI-controller. Thus, we have chosen a PR controller for controlling the inverter output current I_{INV} .

Since, we are regulating I_{INV} which is also the current through the inductor, L_{filter} , the LR-filter essentially represents the plant model and can be represented as,

$$H(s) = \frac{1}{sL_{filter} + R_{filter}} \quad (3.4)$$

The transfer function of the PR controller is given by,

$$G(s) = K_p + \frac{K_R * s}{\sqrt{s^2 + \omega_g^2}} \quad (3.5)$$

where, $\omega_g = 2\pi f_g$ From equations 3.4 and 3.5, we can generate the bode-plot for the loop gain and is shown in Figure 3.14.

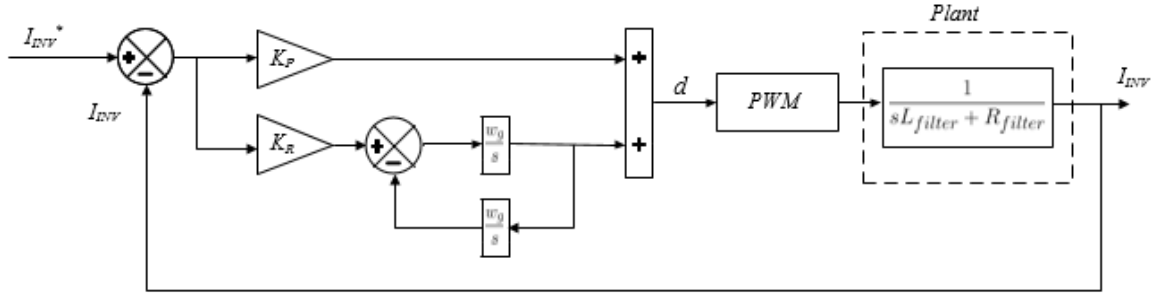


Figure 3.13 H-Bridge inverter PR controller block diagram

3.1.4 Grid-connecting the SST system

The two stages of the SST and the DESD that were described in the previous sections form an independent SST system that can function with or without connection to the grid. This section describes the grid connection strategy. The inverter as described in the previous section regulates the inverter output current I_{INV} and the voltage on the AC link is fixed by

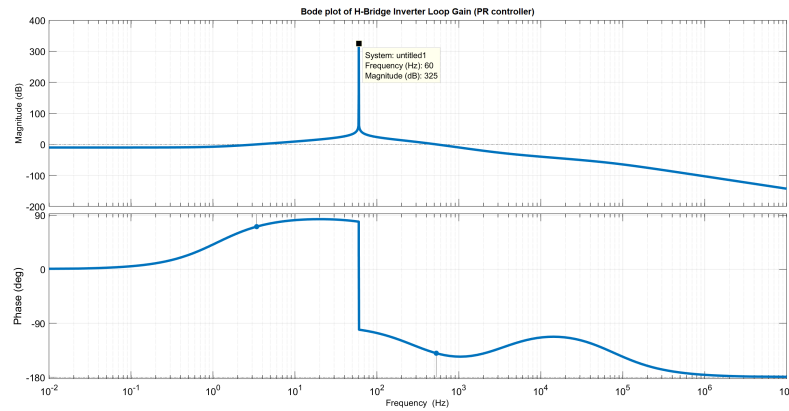


Figure 3.14 Bode plot of the H-Bridge inverter loop gain

the grid. To achieve grid connection, this system must be synchronized with the grid.

In order to synchronize the inverter output to the grid, the sinusoidal wave used in the inverter's SPWM generation must be frequency and phase locked with the grid. For this purpose, a synchronous reference frame phase-locked-loop (SRF-PLL) is used. The PLL block consists of a phase detector, loop filter and a voltage controlled oscillator as described in [21]. Figure 3.15 shows the block diagram of the PLL block and its PI-controller.

The phase detector block of the SRF-PLL includes generation of two quadrature waveforms V_α and V_β . For a three phase system this is popularly done by using Clarks Transform. As mentioned in Table 3.1 we have a single-phase system and thus a different strategy needs to be used. From several available options the most elegant one, as described in [4] is to use a Second Order Generalized Integrator (SOGI) block to generate the quadrature waveforms, V_α and V_β . The second half of the PLL block uses Parks Transform to generate two DC voltages, V_d and V_q . A closed-loop controller is required to regulate V_d to a reference of 0 Volts. When $V_d = 0$, the PLL is said to be locked. The PI-controller design is inspired from [27].

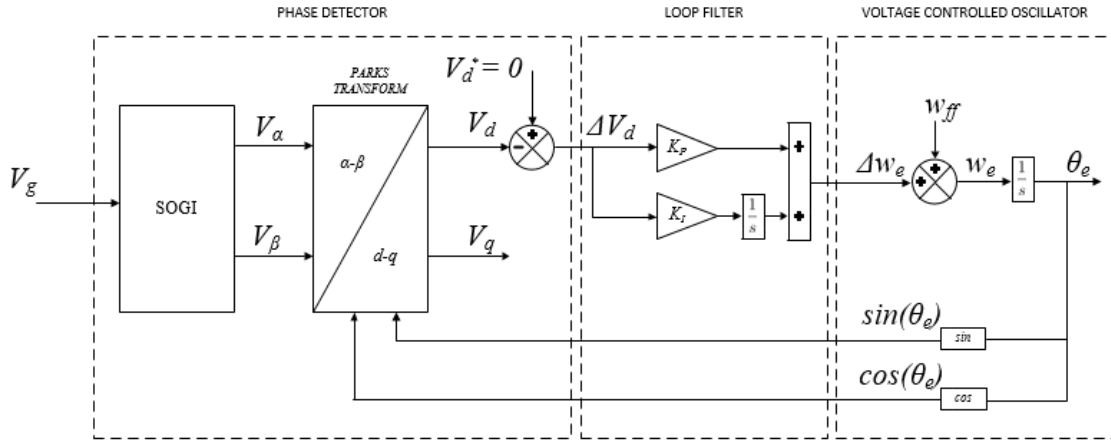


Figure 3.15 SOGI based SRF-PLL block diagram

3.1.4.1 Controller Design

The PI-controller is designed to regulate V_d to a reference of 0 Volts. Since, V_d is a DC quantity, the PI-controller is a good option as it offers infinite gain at DC and a zero steady-state error. In Figure 3.15 we can see in the Voltage Controlled Oscillator block that the plant is an integrator and can be represented as:

$$G(s) = \frac{1}{s}$$

whereas the controller is a PI controller and can be represented as:

$$H(s) = \frac{sK_p + K_I}{s}$$

Figure 3.16 and Figure 3.17 shows the bode plot and step response of the closed loop system respectively. The PI-controller coefficients were found to be $K_p = 100$ and $K_I = 10.0$.

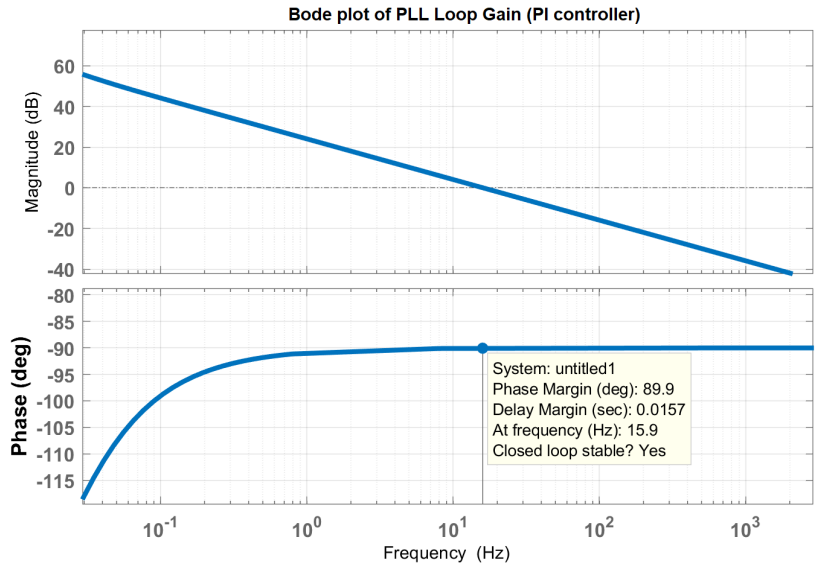


Figure 3.16 Bode plot of the PLL block loop gain

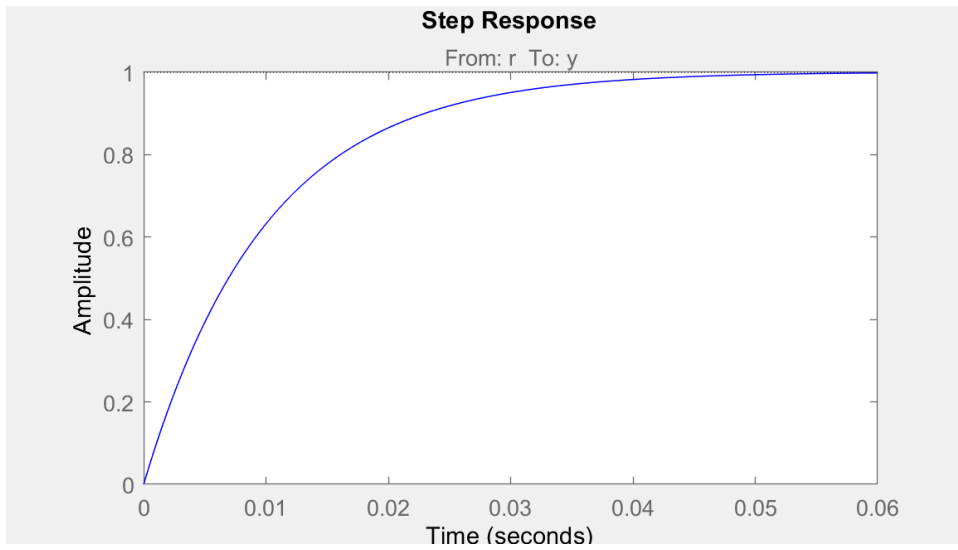


Figure 3.17 Step response of the closed-loop PLL block

CHAPTER

4

IMPLEMENTATION

Chapter 2 provides a brief summary of the communication protocols used in the Power Systems industry and gives a more detailed explanation of the SunSpec Specifications for Modbus. The proposed communication scheme for the FREEDM system is also discussed in Chapter 2. In Chapter 3, we discussed the design and control of the SST, a very critical component of the FREEDM System along with the design and control of a DESD. This chapter describes the implementation of this system which uses the concepts explained in chapters 2 and 3. The implementation is divided into two parts; one part deals with the implementation of the power-electronic system and the other part deals with the implementation of the controller and communications.

The power electronic system is first simulated using a circuit simulation software for system validation and then emulated on a real-time platform for Hardware-In-the-Loop(HIL) testing. This two step implementation of the power electronics system is a very efficient approach and saves a lot of development time. The circuit simulation software provides great utility of ensuring the correctness of the system in a short amount of time. Running a full power-electronic system along with the controls required for it, all in a simulation environment hides the complexity of the implementation of each component of the system; and yet provides a very valuable understanding of system operation. The next stage involves moving from a simulation environment to emulating the system on a real-time platform. This step is very close to an implementation on a hardware system as it attempts to emulate a hardware system as closely as possible. The HIL device connects to a microcontroller that is responsible for controlling the hardware through a set of analog and digital I/Os. The controller is oblivious of the system it is connected to and it's function remains unaltered whether it is connected to the real hardware or a device emulating the hardware.

The implementation of the controller and the communication system was done in parallel as the communication system used a modular approach, making it independent of the controls application running on the controller. The controller implementation and testing was greatly simplified by the use of tools like debug software and a logic analyzer. The communication suite is made up of a communication API for the DSP controller and a set of higher level applications that run on an auxiliary ARM device. The applications on the ARM device perform the functions of data logging and data provision over a LAN network. An HTTP based webapp was developed to collect data from the ARM device. Additionally, an MQTT based application was developed for low-latency critical data.

4.1 Circuit Simulation

A number of circuit simulation software programs like Multisim, LT Spice, PLECS, MATLAB/Simulink are used very widely to simulate power electronics system during the early stages of development. Considering the tools that help design and analyze a system, MATLAB/Simulink along with PLECS blockset was chosen as the circuit simulation software for this project. Some of the modeling strategy is inspired from [15]. Each stage of the SST was first designed and analyzed independently. This was followed by the integration of the stages starting with the integration of the Buck-Boost converter which regulates the LV DC link voltage V_{LDC} with the DAB which regulates the HV DC link voltage V_{HDC} . This subsystem was then integrated with the H-Bridge which is responsible for regulating the inverter output current I_{INV} . Figures 4.1 and 4.2 show the Simulink Model and results for the Buck-Boost converter respectively. Figures 4.3 and 4.4 show the Simulink Model and results for the DAB respectively. Figure 4.5 and 4.6 show the Simulink Model and results for the H-Bridge inverter respectively. Figure 4.7 and 4.8 show the Simulink Model and results for the PLL respectively.

4.2 HIL Emulation

In the Real-Time Hardware-in-the-Loop (RT-HIL) emulation stage, the HIL device only emulates the power electronics system and the controller that was simulated in the previous stage is replaced by a real microcontroller. An HIL device manufactured by Typhoon HIL was used for this project. Typhoon HIL provides a schematic editor to draw the circuit diagram of the power electronics system and a SCADA interface to interact with the emulated model that runs on the HIL device. The controller connects to the HIL device using an interface

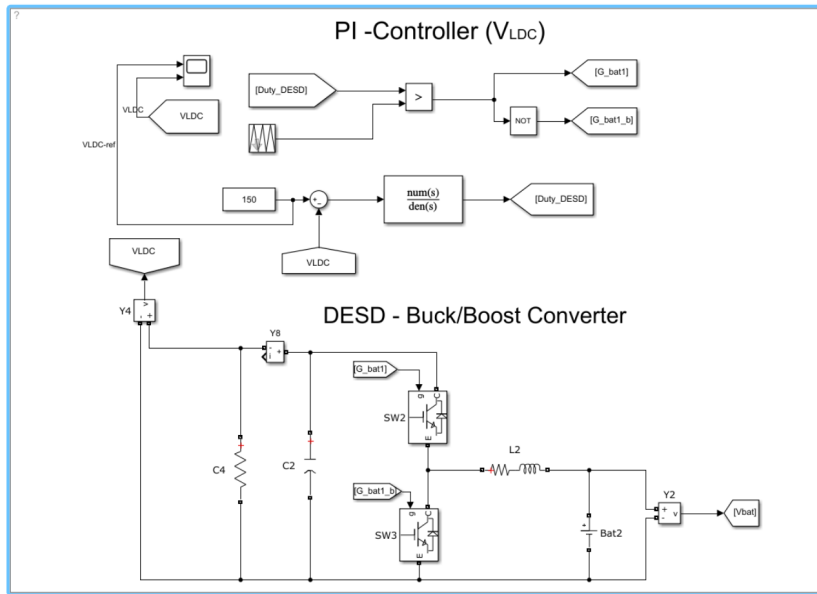


Figure 4.1 Buck-Boost converter simulation diagram

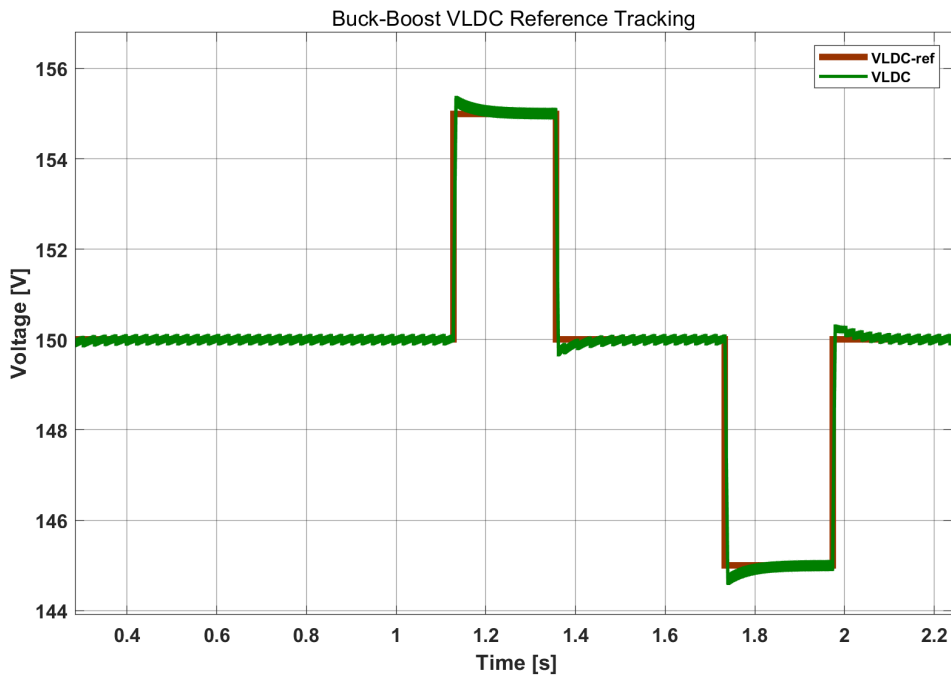


Figure 4.2 A closed loop control of Buck-Boost converter regulating the output voltage (VLDC) to a reference - VLDC-ref

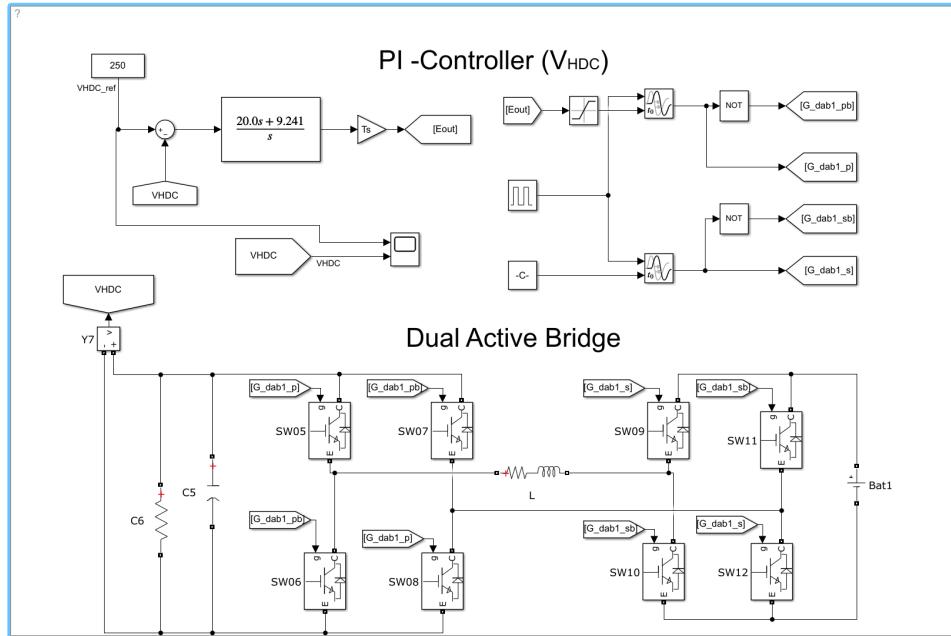


Figure 4.3 DAB simulation diagram

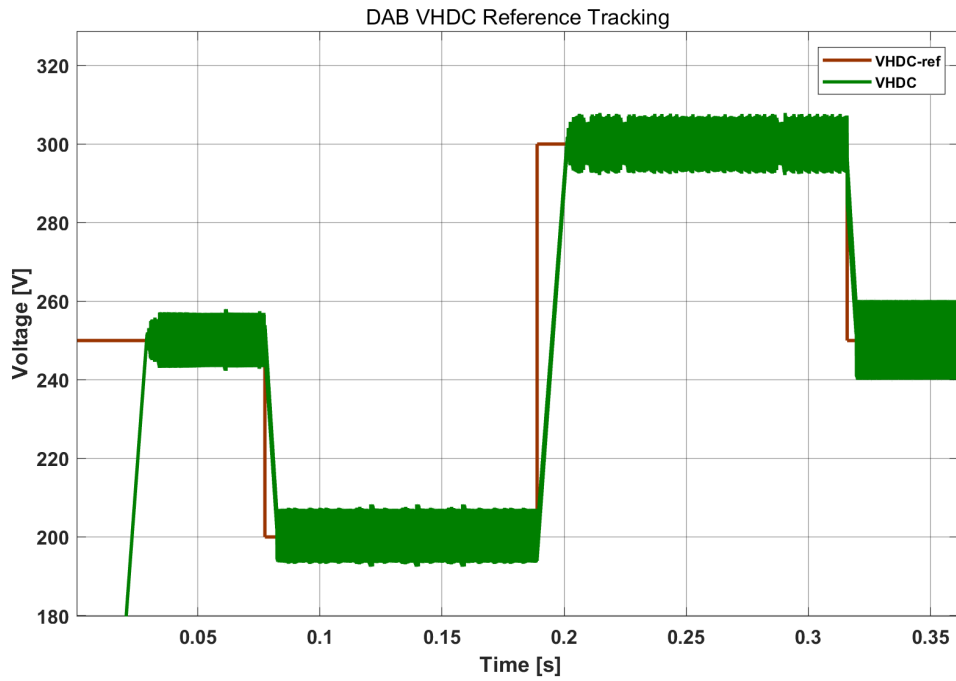


Figure 4.4 A closed loop control of DAB regulating the output voltage (VHDC) to a reference - VHDC-ref

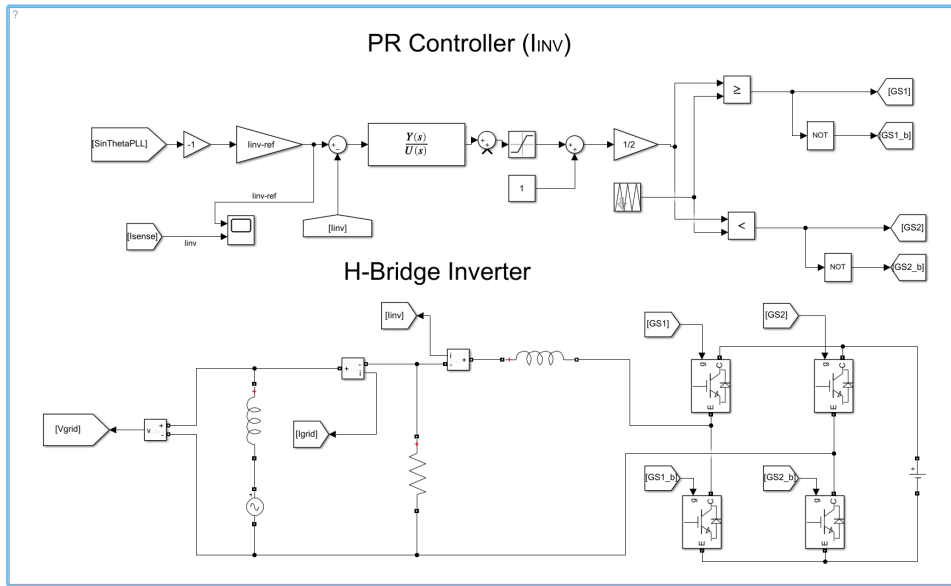


Figure 4.5 H-Bridge inverter simulation diagram

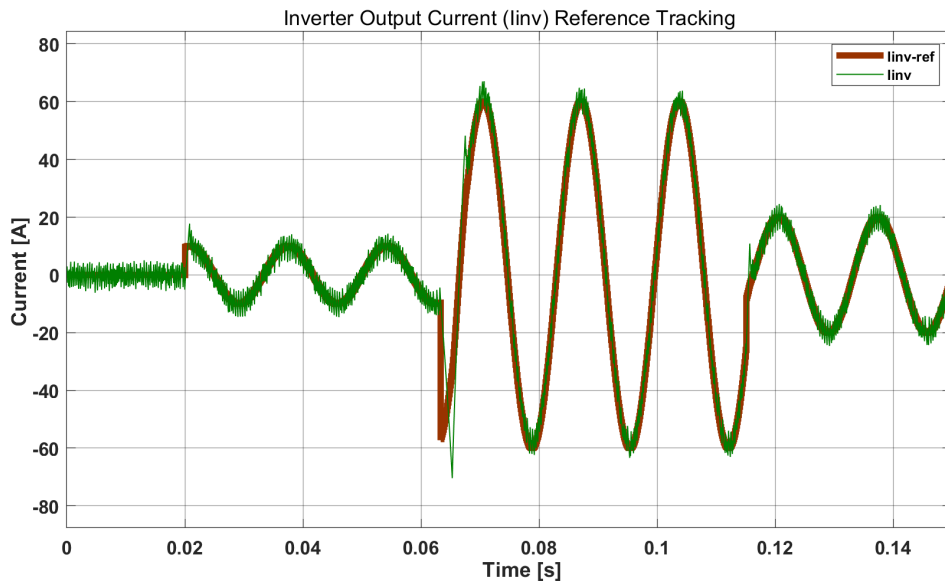


Figure 4.6 A closed loop control of H-Bridge Inverter regulating the output current (I_{inv}) to a reference $I_{inv-ref}$

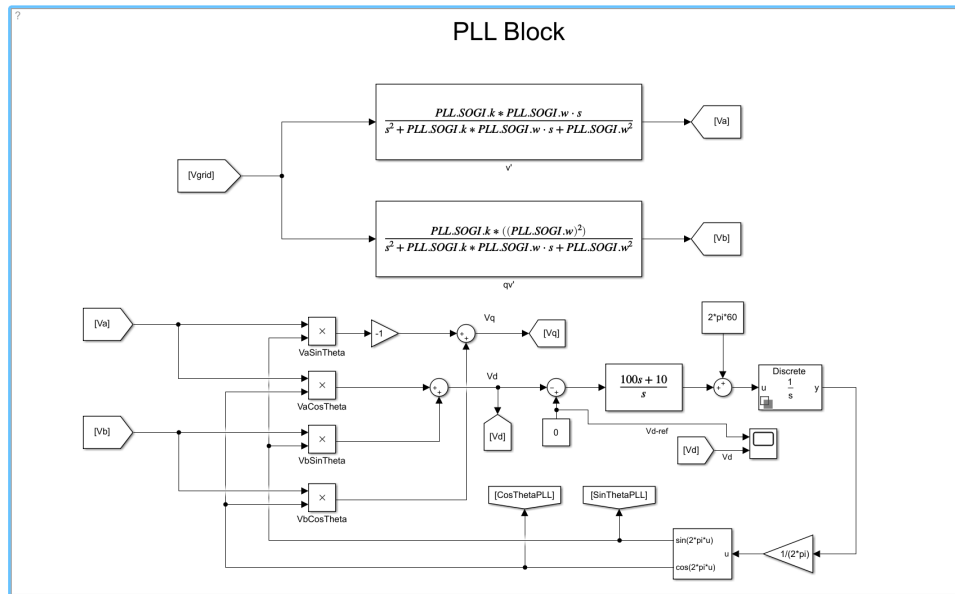


Figure 4.7 SOGI based SRF-PLL simulation diagram

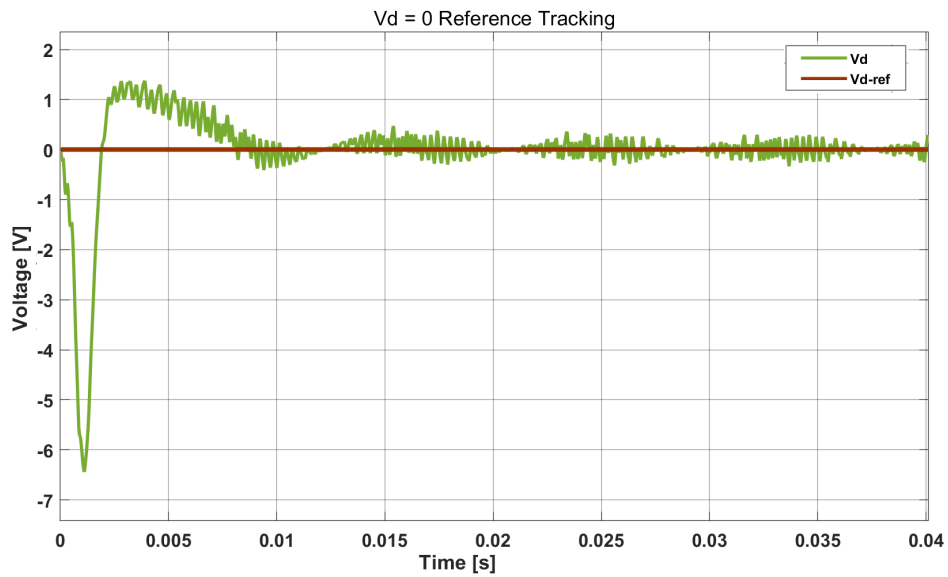


Figure 4.8 A PI controller based PLL, tracking the voltage Vd to a reference of 0 V

board which connects the HIL device's analog and digital I/O pins to the controllers digital and analog I/O pins. Figure 4.9 shows an image of the RT-HIL testbed.



Figure 4.9 Photograph of the RT-HIL testbed

4.3 Controller development

The controller is primarily responsible for controlling the power-electronics system and interfaces to the system using analog and digital I/O pins. A power electronics system typically contains solid-state switches that need to be switched at a high frequency and the implementation of a control system requires floating point mathematical calculations. A Digital Signal Processor(DSP) is best suitable for these requirements. TI F28335 DSP was chosen for this project. A single DSP implements the closed loop controller for all the stages of the SST system and DESD.

4.4 SunSpec API development

The SunSpec API is an API developed to provide a SunSpec compliant Modbus Interface. The developed API is built on top of the underlying Modbus implementation - FreeModbus. The API provides an abstraction layer transforming the traditional register based Modbus slave into a model based SunSpec device. The SunSpec Modbus device map is the abstracted model version of the underlying modbus registers which store the data. Each model is defined as a C struct and each model datapoint can thus be accessed as a variable of that struct. The interface code takes care of mapping each C struct to the appropriate address range in memory.

The interface code also provides the SunSpec datatypes as user-defined datatypes to abstract the processor's endianness and word length which affect the actual placement of data in the memory.

4.5 SunSpec-Modbus-Communication-Suite development

The developed application, termed SunSpec-Modbus-Communication-Suite is a suite of applications and services that run on the auxiliary ARM device. The ARM device used for this project is BeagleBone Black. The BeagleBone Black is a linux machine capable of running a full TCP/IP stack and also provides an Ethernet port that allows us to connect the device to a LAN network. The suite contains three applications; a SunSpec client, a webapp based on HTTPS for non-critical data monitoring and control, and an application for critical control that runs on secure web-sockets using the MQTT protocol. Figure 4.10 shows a high level block diagram of the Communication Architecture.

The SunSpec client application is a python application built on top of an open source

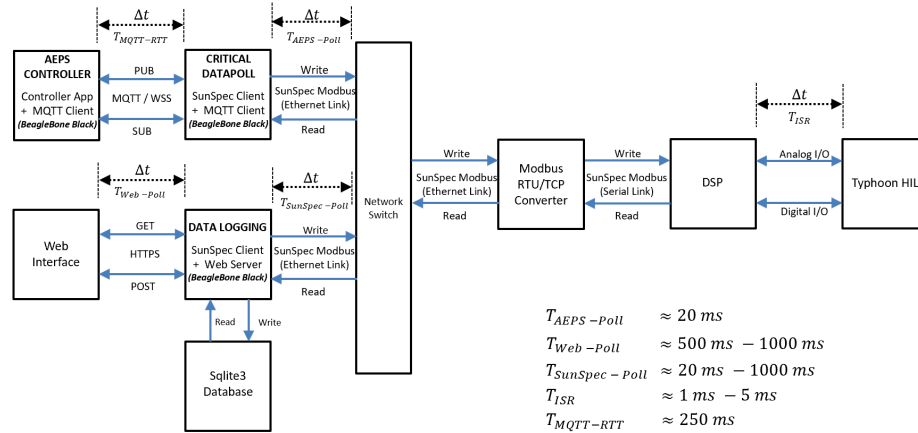


Figure 4.10 Communication Architecture block diagram

package - pysunspec, provided by the SunSpec Alliance. The pysunspec package provides a basic client code that polls for data from a SunSpec device. Note that the SunSpec Modbus abstraction is on top of the underlying Modbus protocol and so the requests and replies are still Modbus messages. The organization of the data in the form of models in the slave device allows the polling client to use the same models to interpret and encode information exchanged between the SunSpec client and the SunSpec device. The model is the key to correct interpretation of data and thus the same model must be used by the client and the SunSpec device. The SunSpec API defines models in the form of C structs whereas the model definition on the SunSpec Client is in the form of an XML file. The client can request the SunSpec device for data by sending single or periodic requests. The client application serves the function of a data logger and thus must provide for a mechanism to store the data received from the SunSpec device. A lightweight database, sqlite3 available as a Python package was chosen for this purpose. The BeagleBone Black being a linux machine with access to the internet allows us to have an accurate date/time value on the BeagleBone Black. This gives us added functionality to store the incoming data to a database along

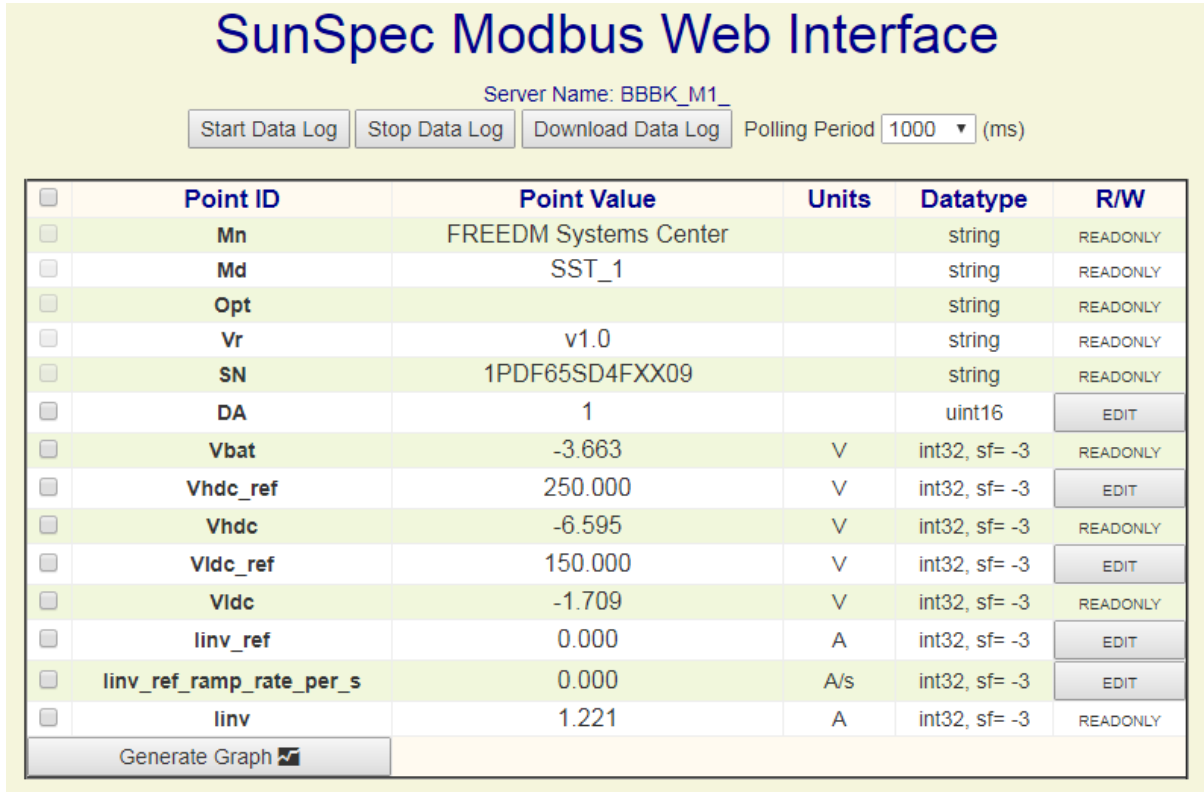


Figure 4.11 A screenshot of the SunSpec Modbus Web Interface

with a timestamp. This client application is designed in a way such that it can be used as a standalone data logging client or to be imported as a package and its API can be used in a higher level application.

The webapp is hosted on a Django web-server and provides a web interface to control the SunSpec client. Figure 4.11 shows the web interface used to control the SunSpec client. The webapp uses RESTful methods to request for data from the web-server. When a user requests to start a data log, the web interface makes an HTTP GET request to the web-server. This internally triggers the webapp to use the SunSpec client's API to start polling for data from the SunSpec device. As mentioned before, the data is stored in a sqlite3 database and thus the webapp uses the sqlite3 API to access this database and display the data on

the web interface. This forms a complete end-to-end application to control and monitor datapoints on a SunSpec device.

The web interface is designed using HTML and AngularJS making the interface a highly dynamic interface that adapts itself based on the data that is read from the database. The web interface provides functionality to monitor datapoints and optionally edit the value of a editable datapoint. The read/write access is dictated by the access field in a datapoint definition. The web interface is designed to be robust and has error checking mechanisms built into it. For example, inputting a value for a datapoint that is outside the range of its datatype will result in an error message at the interface level itself and does not require handling by the web-server. A few other error checking functions are handled by the web-server. A very useful functionality that the web interface provides is the ability to download the data logged during a session as a CSV file. The user may optionally use this data for further offline analytics.

An MQTT based application was developed for low-latency time sensitive control. A BBBK runs a SunSpec Client to poll the DSP at a high polling rate only for a very small amount of critical data. The BBBK at the DER interface publishes this data to a topic on the MQTT broker. The Area EPS which performs time-sensitive control, subscribes to the same topic and in return publishes it's responses to a different topic that the BBBK at the DER interface subscribes to. The MQTT protocol offers three Quality of Service(QoS):

- QoS 0 - At most once
 - Simplest, least-overhead messaging. The client publishes a message and does not need any acknowledgement from the broker.
- QoS 1 - At least Once

- This method guarantees successful transmission to the broker as the broker sends an acknowledgement to the sender. The Client will resend messages to the broker until it receives an acknowledgement.
- QoS 2 - Exactly once
 - This is the highest level of QoS. There is a handshake between the sender and the broker and the message is guaranteed to be sent only once.

For the time-critical control application we are interested in sending the data as fast as possible. Also data retransmission is not favorable as we are interested in the latest data, in order to take action. Considering the requirements of our application, QoS 0 or QoS 1 may be suitable. The implemented application uses QoS 1 to ensure data is delivered to the broker as it is important that the DER publishes data to the broker at all times. For the MQTT broker, a free public MQTT broker was used. The senders connect to the MQTT broker over secure web-sockets that use SSL/TLS encryption.

4.6 DER Testbed Experimental Results

The communication dependent performance of the DER was studied. This section presents the timing analysis of the communication and its implications on the performance of DER. The communication architecture deploys a time sensitive controls application and a less time sensitive data-logging and visualization application. The Area EPS may issue control commands to the DER and it is thus motivating to study the latency of communication and its effect on performance.

4.6.1 Timing Analysis

In this section a timing analysis of the communication architecture is presented. The system is analyzed for two scenarios. In Scenario-1, the control operation takes place at the BBBK labeled 'control-node' as shown in Figure 4.12. This node is connected directly on the LAN network and communicates with the DSP using Modbus. The Modbus RTU/TCP converter sits between the DER's DSP and the control-node. The Modbus RTU/TCP converter exposes an Ethernet interface to the control-node and serial interface to the DSP. The control-node is responsible for communicating time critical control information to the DSP. The control-node continuously polls for data that is critical for DER control. Since the latency on the Ethernet link is much lower than on the serial link, a timing analysis is performed to analyze communication on the serial link as shown in Figure 4.14. It is seen that at 57600 baud, it takes about 30 ms between successive writes to the DSP. The net delay is comprised of delays at various stages in the communication link. The delay δt_8 can be reduced by setting the TCP_NODELAY socket option if configurable. Figure 4.15 shows the communication latency for Scenario-1.

In Scenario-2, the control-node communicates with the DER over MQTT as shown in Figure 4.13. The BBBK connected at the DER interface continuously polls the DER for data using Modbus TCP, similar to Scenario-1. However, the control logic is present at the control-node and data must be relayed to the control-node over MQTT. A pub-sub mechanism is used for data exchange between the control-node and the BBBK. In Scenario-2, a free online public MQTT broker was used for the tests. It was observed that the MQTT RTT was approximately 250ms. This latency is much larger than the latency on the serial link and thus in Figure 4.16 it can be seen that the communication latency is dominated by the MQTT RTT. A dedicated paid or local MQTT broker may be used as an alternative to

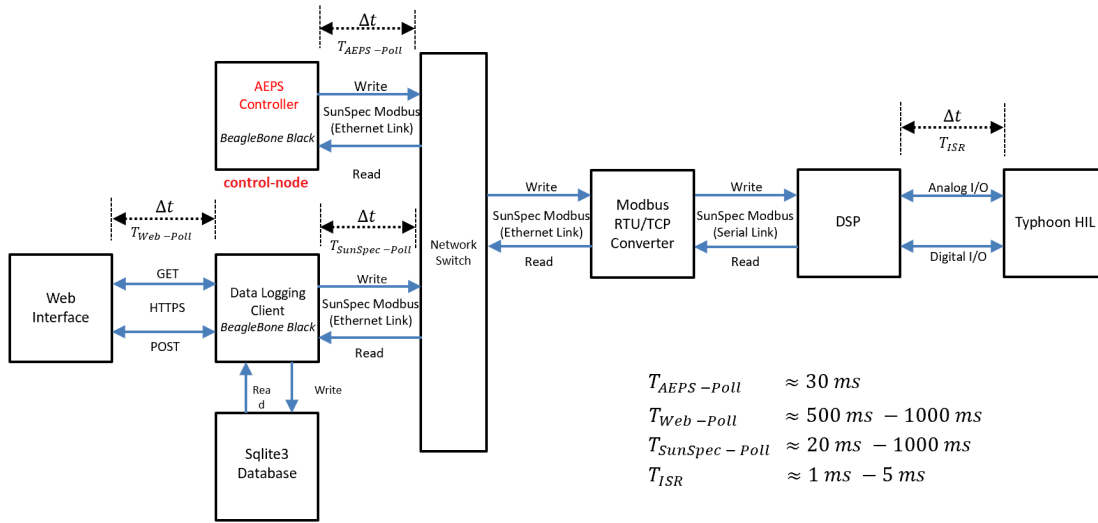


Figure 4.12 Communication Architecture Scenario-1

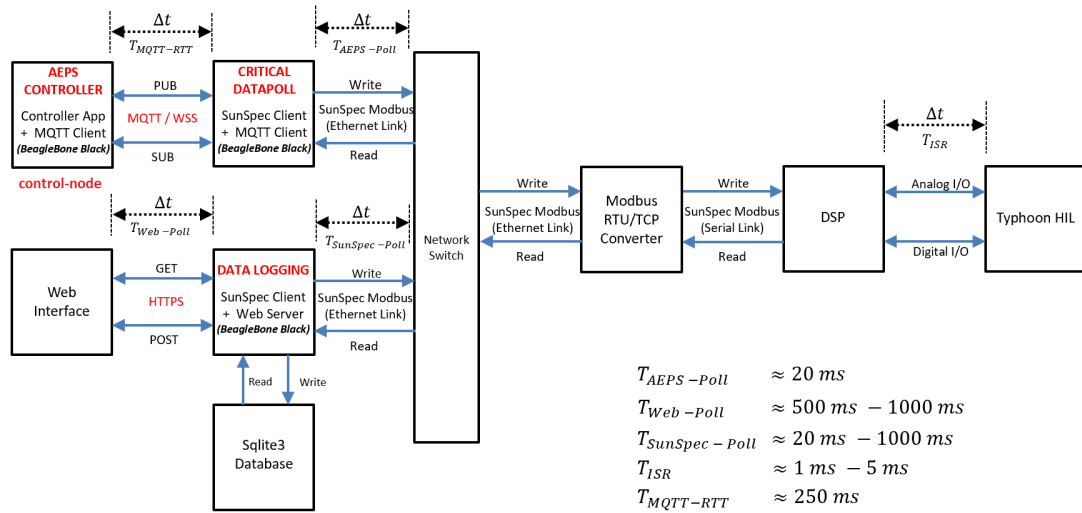


Figure 4.13 Communication Architecture Scenario-2

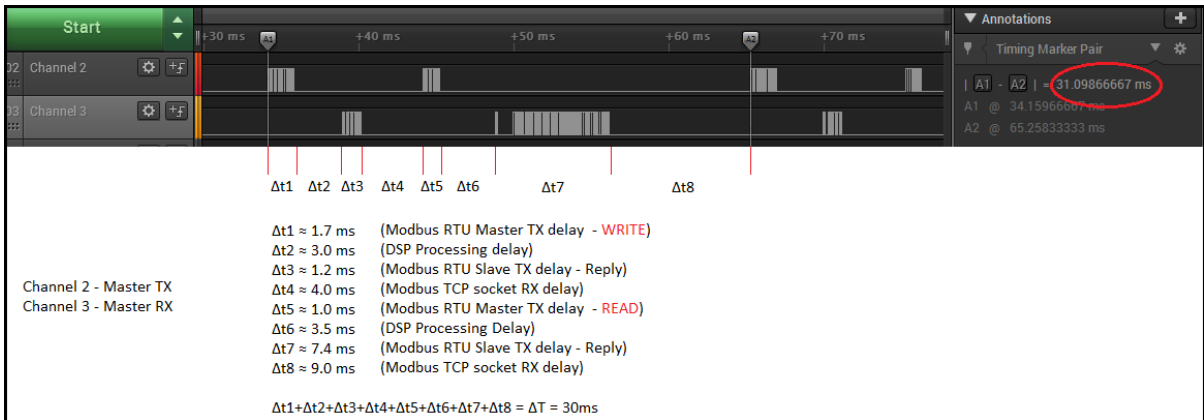


Figure 4.14 Timing Analysis of communication on the serial-link.

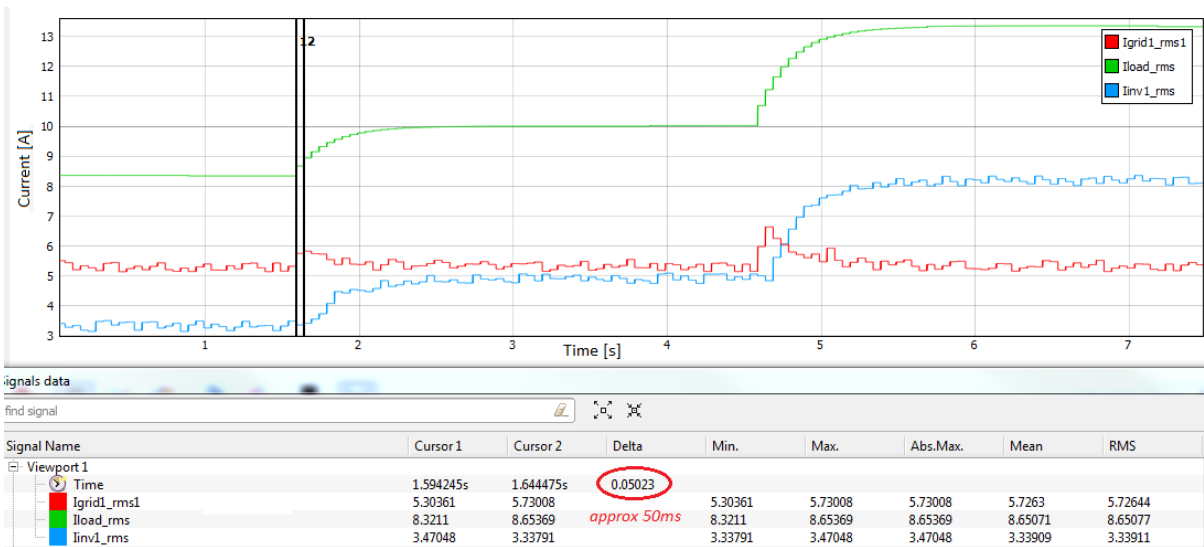


Figure 4.15 Communication Latency in Scenario-1

improve the MQTT RTT.

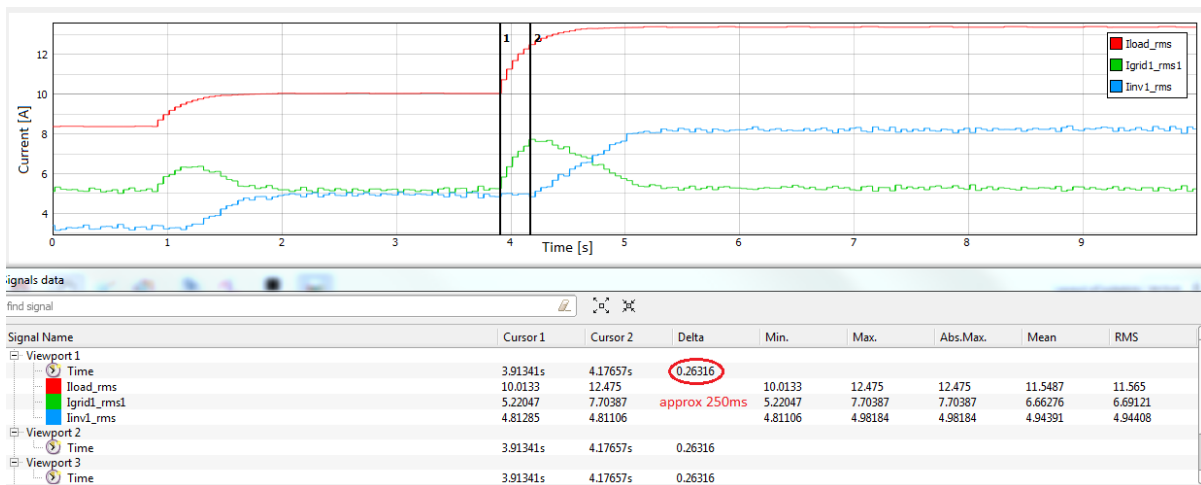


Figure 4.16 Communication Latency in Scenario-2

4.6.2 Implication of Communication Latency on DER performance

For a specific application it may be desirable to maintain the consumption of grid power at a fixed reference level. For a load that is powered by grid power and renewable energy, the total power consumed by the load is a sum of power supplied by the grid and the power supplied by an inverter. In case of an increase in load power, the consumption of grid power needs to be maintained at the same reference level and the extra power needs to be provided from the inverter. In reality however, since the inverter output power is regulated, when there is an increase in load power, the instantaneous power requirement is supplied by the grid until the inverter reference is updated to supply the extra power. In Figure 4.17 it can be seen that due to the communication delay, the grid has to provide for the extra load power until the Area EPS / Area controller changes the reference output power of the

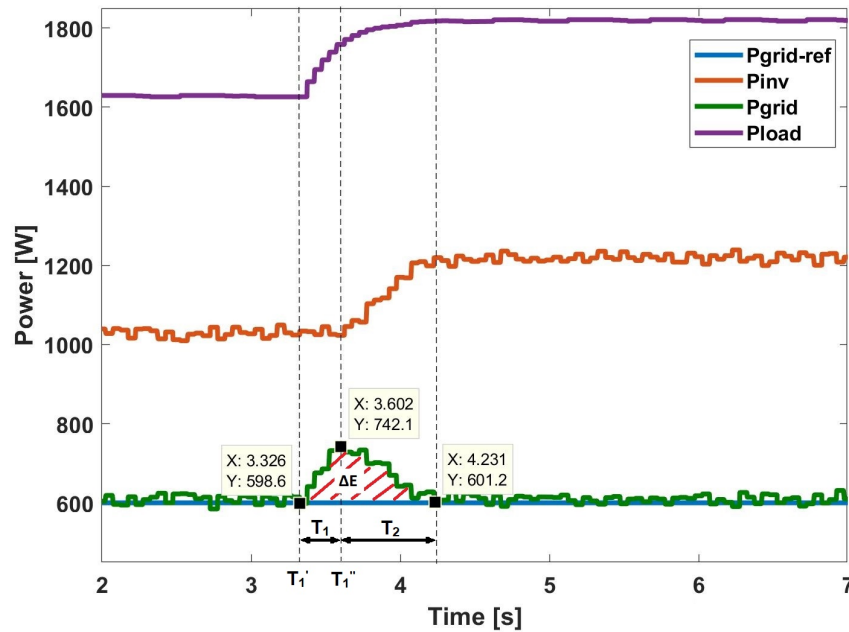


Figure 4.17 Grid power, Inverter output power, Load Power graphs

inverter. Additionally, once the new reference value has been communicated with the DER, the DER takes a finite amount of time to ramp change its output power to the new reference value. When the inverter output current increases, it causes a voltage sag on the HVDC link and care must be taken that the voltage on the HVDC link does not sag beyond the allowable limit. The voltage sag is dependent on the ramp rate, the net change in inverter output current and the speed of the controller. Figure 4.18 shows the voltage sag on the HVDC link at different ramp-rates. For all three graphs the total change in inverter output current was 20 A.

To reduce the consumption of excess grid power, the ramp rate must be as high as possible.

This shows that the total extra energy taken from the grid is a sum of energy consumed due to the communication latency and the latency of the power electronic system itself.

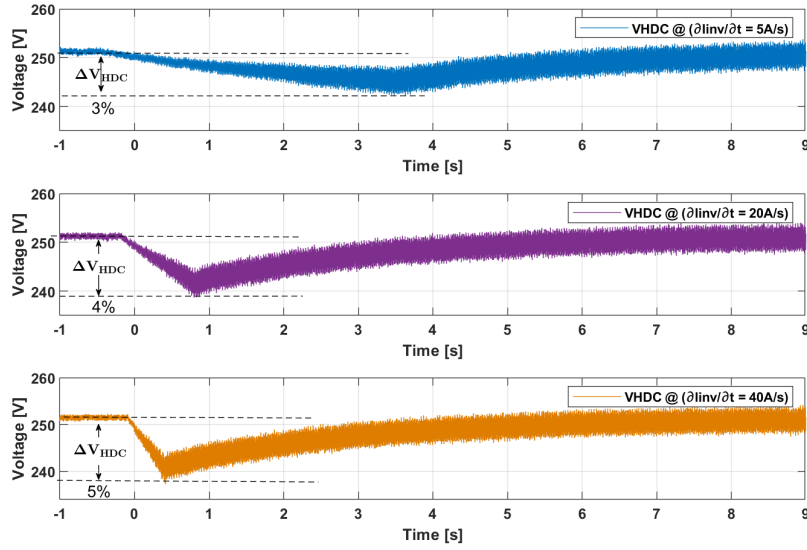


Figure 4.18 Voltage Sag on HVDC link at different ramp rates of Inverter output current

In order to minimize the system latency, an analysis of the voltage sag on the HVDC link becomes very important.

4.6.3 HVDC link Voltage Sag Analysis

In this section, an analysis of the HVDC link voltage sag is presented. In Figure 4.19, at steady state,

- $i_C = 0$
- $i_{DC'} = i_{DC}$

For a step change in the inverter output power, $\Delta P_{INV} = V_g * \Delta I_{INV}$, where V_g is the grid voltage and ΔI_{INV} is the change in inverter output current. When the inverter output power changes by ΔP_{INV} , for a lossless inverter we have $\Delta P_{INV} = \Delta P_{DC}$. Thus the power provided to the inverter needs to increase by ΔP_{DC} . Instantaneously, the capacitor begins to

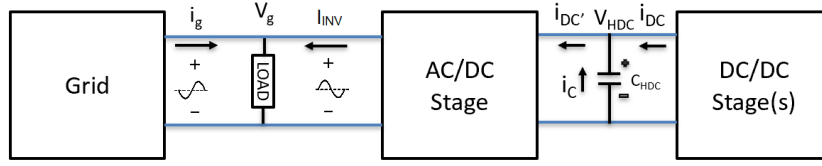


Figure 4.19 Grid connected SST system block diagram

discharge in order to provide for power , ΔP_{DC} . The capacitor discharges until the controller of the DC/DC stage catches up and the DC/DC stage starts providing ΔP_{DC} . The capacitor voltage drops as constant power is drawn from it. The discharge of a capacitor at constant power can be described as:

$$i_C(t) = C_{HDC} * \frac{dv_{HDC}(t)}{dt} \quad (4.1)$$

$$i_C(t) * v_{HDC}(t) = \Delta P_{DC} = \Delta P_{INV} \quad (4.2)$$

Solving the equations 4.1 and 4.2 we get,

$$v_{HDC}(t) = V_{HDC-ref} * \sqrt{1 - \frac{t}{\tau_1}} \quad , \tau_1 = \frac{C_{HDC} * V_{HDC-ref}^2}{2 * \Delta P_{INV}} \quad (4.3)$$

τ_1 is the total time required for the capacitor to completely discharge.

Since, the DC/DC stage controller is responsible for regulating the HVDC link voltage, the net voltage seen on the HVDC link is the sum of the decreasing voltage due to capacitor discharge and the increasing voltage as the capacitor is charged due to the controller action. Thus, the voltage on the capacitor:

- Decreases while Rate of discharge > Rate of charge
- Reaches a minimum value when Rate of discharge = Rate of charge

- Increases while Rate of discharge < Rate of charge

For simplicity, we assume a first order controller and thus the voltage on the capacitor can be written as,

$$v_{HDC}(t) = V_{HDC-ref} * (1 - e^{-\frac{t}{\tau_2}}) \quad \text{where, } \tau_2 \text{ is indicative of the controller speed} \quad (4.4)$$

The net voltage on the capacitor can be described as a sum of equation 4.3 and equation 4.4. Thus, we get,

$$v_{HDC}(t) = V_{HDC-ref} * (1 + \sqrt{1 - \frac{t}{\tau_1}} - e^{-\frac{t}{\tau_2}}) \quad (4.5)$$

Since, we are interested in the voltage sag $\Delta v_{HDC}(t)$, from equation 4.5 we get,

$$\Delta v_{HDC}(t) = V_{HDC-ref} - v_{HDC}(t) = V_{HDC-ref} * (e^{-\frac{t}{\tau_2}} - \sqrt{1 - \frac{t}{\tau_1}}) \quad (4.6)$$

The minimum value of the capacitor voltage occurs at $t = \tau_1$. Substituting, $t = \tau_1$ in equation 4.6 we get,

$$\Delta v_{HDC-MAX}(t) = V_{HDC-ref} * (e^{-\frac{\tau_1}{\tau_2}}) \quad (4.7)$$

From equation 4.3 we have, $\tau_1 = \frac{C_{HDC} * V_{HDC-ref}^2}{2 * \Delta P_{INV}}$. Thus,

$$\Delta v_{HDC-MAX}(t) \propto V_{HDC-ref} * e^{-V_{HDC-ref}^2} \quad (4.8)$$

$$\Delta v_{HDC-MAX}(t) \propto e^{-C_{HDC}} \quad (4.9)$$

$$\Delta v_{HDC-MAX}(t) \propto e^{-\frac{1}{\Delta P_{INV}}} \quad (4.10)$$

$$\Delta v_{HDC-MAX}(t) \propto e^{-\frac{1}{\Delta I_{INV}}} \quad (4.11)$$

$$\Delta v_{HDC-MAX}(t) \propto e^{-\frac{t}{\tau_2}} \quad (4.12)$$

This analysis is a good indicator of which parameters contribute to the voltage sag and how they are related. From the analysis presented above and as seen in Figure 4.17 the total extra energy consumed from the grid is a function of the communication latency and the system induced latency. We can thus write the equations for the excess energy consumed from the grid as follows:

$$\Delta E1 = \int_{T_1'}^{T_1''} P(t) dt \quad (4.13)$$

$$\Delta E2 = \frac{\Delta P * T_2}{2} \quad (4.14)$$

$$\Delta E = \Delta E1 + \Delta E2 \quad (4.15)$$

where $T_1 = T_1'' - T_1'$ is the communication latency and T_2 is the time required by the system to change it's power reference by ΔP such that the voltage sag is within allowable limits.

CHAPTER

5

CONCLUSION AND FUTURE WORK

5.1 Conclusion

This thesis involved the study of the communication requirements to support the sustenance and growth of the smart grid infrastructure. A survey of the existing communication technologies was conducted and a communication scheme compliant with IEEE 1547.3 was proposed and implemented. To test the communication framework, an SST testbed was designed and implemented. The control strategies used for the SST system were simplistic in nature and this system can be used as a base model for future implementations. Each stage of the SST system was simulated and later emulated in an HIL environment.

Finally, a timing and memory analysis of the implemented communication application was conducted to study its impact and overheads on the critical controls application.

5.2 Future Work

The work completed during this thesis consisted of setting up a fully operational complex power electronics system with the most simplistic approach. Each stage of the SST can be modified to make the system design more robust and reliable. This development serves as the base model for development of more complex systems serving more specific applications. The communication framework developed in this project can be utilized in numerous smart grid applications as described in section 2.5. Some of the areas of research presented below can greatly enhance the robustness and usability of the FREEDM System.

5.2.1 Network Security

In the communication scheme presented in this thesis, the user communicates with the ARM device through the web interface using RESTful methods. The ARM device hosts the web-server on a LAN network allowing any other device on the network to use its services. Entities communicating over this network use a SSL/TLS connection thus ensuring that data communicated over the network is secured by encryption. Another very important aspect of security is access authorization. A secure and robust architecture for DERs must take into consideration all facets of network security and thus remains an important topic of research.

5.2.2 Deployment of DGI

The communication framework developed in this project, provides a great foundation for data-logging applications, remote monitoring and control of Power Systems. The FREEDM System also implements a Distributed Grid Intelligence(DGI) application which makes distributed power sharing and controls decisions based on the data collected from all the nodes in the network. The use of DGI can greatly enhance and optimize the use of renewable energy resources and the testbed developed for this thesis serves as a good platform to deploy and test DGI. Some work with DGI over MQTT is presented in [9].

5.2.3 Data analytics

The data-logging facility provided by the webapp developed for this project, opens the doors for building online and offline data analytics applications. Studying the trends and energy usage of commercial and residential customers can provide extremely valuable information to carry out tasks like load-balancing and peak shaving more efficiently. Using data analytics for cost and energy savings remains a great topic for future research.

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