ABSTRACT

ISIK, SEMIH. Investigation of the Operation of MMC Based Point to Point HVDC System with Feed-forward Current Control Scheme (Under the direction of Dr. Subhashish Bhattacharya).

Voltage source converters (VSCs) have been commonly used due to their flexibility to control voltage and power independently and bi-directionally. Typically, (e.g. two-level converter), the control system mainly consists of two parts; outer voltage or power flow (real and reactive power) controller and inner current controller. Vector current control based dq decoupling technique enables to control active and reactive power, DC voltage and AC voltage. The $d-$ and $q-$axis of grid voltages and currents comprise AC and DC components under unbalanced grid conditions. The AC components of the d- and q- axes current make the grid current unbalanced. In this thesis, the detailed investigation of the operation of MMC based point to point HVDC system and feed-forward current controller strategy are presented. Also, the DC short circuit handling capabilities of Half Bridge SM (HBSM) and Full Bridge SM (FBSM) topologies with detailed model of grid connected point to point HVDC system is examined. The Real Time Digital Simulator (RTDS) and EMTDC/PSCAD are employed to demonstrate the results of proposed feed-forward current control strategy, applied to the Point to Point MMC based High Voltage Direct Current (HVDC) system.

Investigation of the Operation of MMC Based Point to Point HVDC System with Feed-forward
Current Control Scheme

by
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DEDICATION

To my parents and sister

Annem, Babam ve Ablam'a Itafen

BIOGRAPHY

Semih Isik was born in Turkey. He received his B.Sc. in Electrical Engineering from Nigde University, Nigde, Turkey. After working as a researcher at E.On Energy Center, RWTH Aachen University, in Aachen, Germany, he started to pursue his M.Sc. in Electrical Engineering at North Carolina State University, FREEDM Systems Center in 2016. His research interests include power converter design and control, Flexible AC devices (FACTs), and Modular Multilevel Converter (MMC) based High Voltage Direct Current (HVDC) transmission.

ACKNOWLEDGMENTS

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

Chapter 1　　　　Introduction

1.1.　Statement of problem

When Alternating Current (AC) won the competition over Direct Current (DC) transmission in the late 1880s, bulk power transmission systems have been based on AC system. There are several reasons why AC system-based transmission has been used for years. Simplicity of AC transformers, making voltage level high and reducing the losses, are some of them. However, great inventions in power electronics and commonly used of Renewable Energy Sources (RES) have brought attention to DC transmission for high power, recently. Even though Voltage Source Converter (VSC) based two level, multilevel diode-clamped converters are mostly used, Modular Multilevel Converter (MMC) is nominated a good candidate for high and medium voltage transmission because of higher power rating capacity, low Total Harmonic Distortion (THD), and modularity. Although lots of work have been done and published on MMCs, dynamic performance of a large number of Sub-Modules for Point-to-Point VSC based HVDC systems have not been fully studied on Real Time Digital Simulator (RTDS). The motivation of this thesis is to investigate of the operation of MMC based Point to Point HVDC system with feed-forward current control scheme, the DC short circuit handling capabilities of Half Bridge SM (HBSM) and Full Bridge SM (FBSM) topologies and explain ongoing five level MMC hardware implementation.

1.2.　Thesis Objective

The main objective of this thesis is to develop a suitable MMC model for point to point HVDC transmission which can be tested on real time digital simulator. The aim is to minimize the hardware requirements and replicate a real system in the platform before building on site. Along

with a working MMC model, a feed-forward current control method is implemented to reduce the unwanted disturbance in a control system and increase the dynamic of the system while reducing the dependence on Proportional Integral (PI) controllers. This thesis reaches the aim in the following ways:

In the first part of the work, (chapters 1 thorough 5), the operation principle of the MMC system is presented and explained.

In the second part of the work (chapters 6 and 7), proposed scheme is explained, presented and the results are demonstrated.

Chapter 2 Topology Evaluation

2.1. Voltage Source Based Conventional Converters

Before VSCs are commonly used on HVDC transmission, Current Source Converters (CSCs) with the Silicon Controlled Rectifier (SCR) have been extremely used.
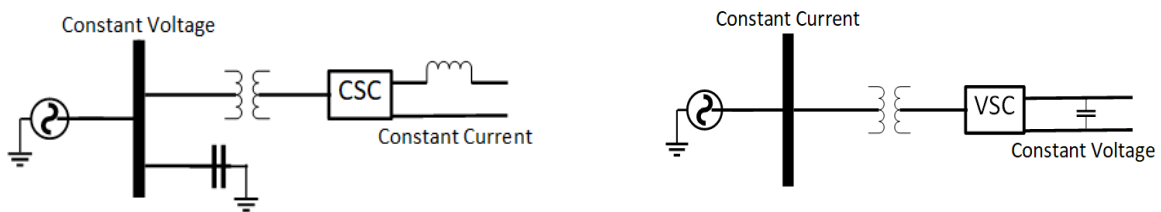
Figure 2-1: Structure of CSC and VSC

One of the differences between VSC and CSC is that the VSC maintains the DC voltage at a level and power transfer is determined by DC current [1], while the polarity of DC voltage determines the power flow between terminals, and DC current maintains at a level in the CSC applications.

CSC acts as constant voltage source on the AC side as can be seen on the left in Figure 2.1. A capacitor as an AC filter needs to be placed on AC side for harmonic elimination and a reactive power supply for power factor correction. On DC side, an inductor needs to be placed for energy storage and a DC filter. VSCs do not require an AC filter as can be seen on the right in Figure 2.1, but a capacitor is connected on the DC side, resembling a voltage source [6]. These converters consists of fully controllable self-commutating devices, e.g. Gate Turn-off Thyristors (GTOs) or Insulated Gate Bipolar Transistors (IGBTs), which can be controlled in turned on or off manner. VSCs can operate at high switching frequency. This makes VSCs possible for HVDC transmission to incorporate power electronics converters with DC cables and overhead lines to carry more than

1000 MW Power [2]. However, it has some drawbacks such as high switching power losses, requiring strong and large AC network for reactive filters and harmonics [3]. Although there are drawbacks, VSC-HVDC is still a better technology for conventional HVDC system with following reasons [4-6].

➢ Footprint requirements are lower

➢ The active and reactive power can be controlled independently

➢ An excellent dynamic response can be achieved, which is important to comply with the grid code requirements during AC fault cases.

➢ A collapsed network can be restored by means of what is referred to as the black-start capability

➢ Passive loads without generation can also be supplied

➢ Very weak power grids can be connected to the HVDC transmission system with little effort

➢ Self-commutation devices are used

➢ Little or zero risk of commutation failures in the converter

➢ Faster dynamic response because of higher switching frequency

➢ Minimal environmental effect

Before multilevel converters are introduced, conventional converter topologies, two-level, multilevel diode-clamped and multilevel floating capacitor were mostly used for DC transmission and power conversion. Some of their advantages and disadvantages can be found [2-4]. Most used conventional converter topologies before the MMC are as follow:

➢ Cascade H-Bridge type: there is no common DC link capacitor [8], [9].

➢ Diode-clamped neutral point clamped type: There is a DC link capacitor [10], [11].

➢ Capacitor-clamped type: There is a DC link capacitor as well as flying capacitors [12], [13].

2.2. VSC Based Modular Multilevel Converter (MMC)

MMCs, VSC type converters, which are used for power conversion and HVDC transmission. This topology has been proposed to prevent damaging drawbacks of traditional converters [6]. Even though the background of the MMC is similar to the conventional two-level converters, switching losses and harmonic content are much lower in the MMC. Besides, while switches must be gated simultaneously in conventional VSC based converters, they can operate individually in MMC based VSC converters without any external source. Also, active and reactive power can be controlled independently in VSC based converters. MMC is capable of changing power flow direction without reversing the voltage polarity enables the construction of multi-terminal HVDC systems and DC grid [19]. One should look in to the structure of a SM, which will be explained in Chapter 3, to understand the operation of MMC converters. Most important characteristic of the topology are;

➢ Modular structure

➢ Scalable in terms of voltage and current

➢ Transformer-less grid connection for MV voltage applications

➢ Low THD output voltages with reduced dv/dt stresses

➢ Low di/dt of arm currents

➢ Both higher and fundamental switching frequency Pulse-Width Modulation (PWM). As a result of lower switching frequency, switching losses are much lower [9].

➤ Alternative modulation technic called, Nearest Level Modulation (NLM) is introduced mostly for the high number of SMs.

The Trans Bay Cable (TCB) project has been the first industry application installed using MMC topology for VSC HVDC transmission in 2005 [30]. The main aim of TCB is to solve the long-term energy need of San Francisco. Siemens' [31] MMC modules are used. Each arm has 216 Sub-Modules (SMs). Total, there are 1392 SMs including 96 spare modules. TCB can transmit 400MW and $\pm$200 kV up to 53 miles. One of the biggest advantages of HVDC Plus is that modules and fans can be removed during the operation due to redundancy. HVDC light [32] is also one of the biggest project conveyed by ABB to transmit power over long distance under water. Upper limit of HVDC light reaches up to 3000MW $\pm$640kV. ABB also one of the producers of HVDC converter transformers. In 2012, first 1100 kV UHVDC transformer was tested. Three single phase transformers are employed in HVDC light due to redundancy reason. During SLG fault on any grid side, converter support the grid injecting reactive power. Lastly, transformers are not grounded individually instead entire system is grounded as one unit.

Chapter 3   Modular Multilevel Converter (MMC)

3.1. Structure of MMC

The structure of MMC is made up of two arms, upper and lower, per leg. These two arms are connected through two inductors (Figure 3.1) to control the power flow and protect the system in case a fault condition. Each leg contains N number of series connected SMs. If the number of SMs get higher, the output voltage become smoother and more sinusoidal such that low dv/dt can be achieved.
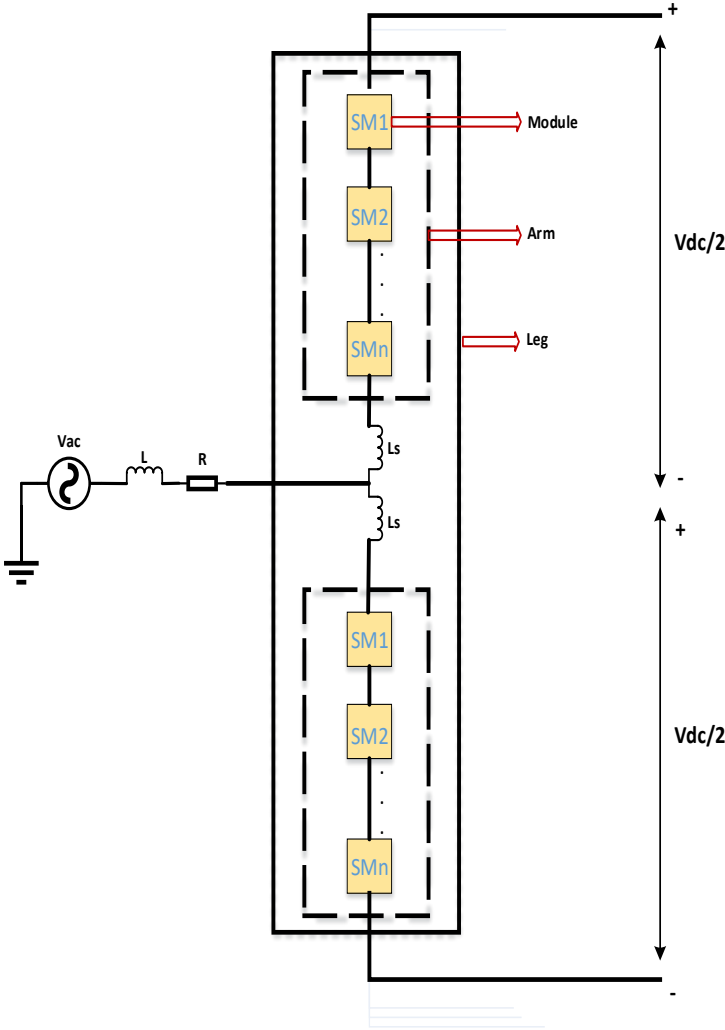
Figure 3-1: Single Phase MMC Structure
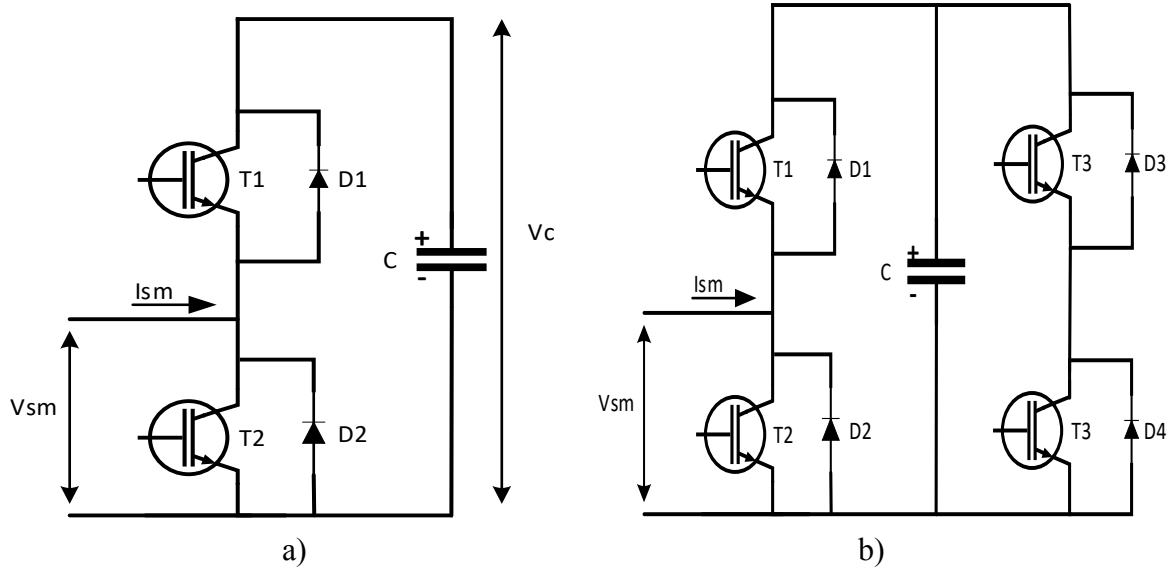
Figure 3-2: Structure of a) half-bridge SM, b) full-bridge SM

Each MMC leg is composed of N number of SMs which result into a line-to-neutral voltage waveform of (N+1) level [14]. SMs can be half-bridge in fig. 3.2 (a) or full-bridge fig. 3.2 (b). Half-bridge SMs are mostly preferred for the applications. The reason for this is that it has lower losses and cost comparing with the full-bridge SMs. Although using a full-bridge SM increases the losses and the cost almost a twice, it also has some important advantages. The most critical of the advantages is providing a counter voltage in case of dc-side short circuits to prevent the fault current flowing from the ac side to the fault on the dc side. Switches in a SM are controllable that is fired in a complementary fashion. Since the half-bridge scheme is adopted throughout this thesis, only its operation principle described. Output voltage of a SM can be equal to its capacitor voltage Vc or zero depending on the switching states [6].

Table 3-1: Switching States of Half-bridge SMs

State	T1	T2	Vsm
On State	On	Off	Vc=Vsm, Ism=Ic
Off State	Off	On	Vsm=0, $\frac{CdVc}{dt} = ic = 0$

8
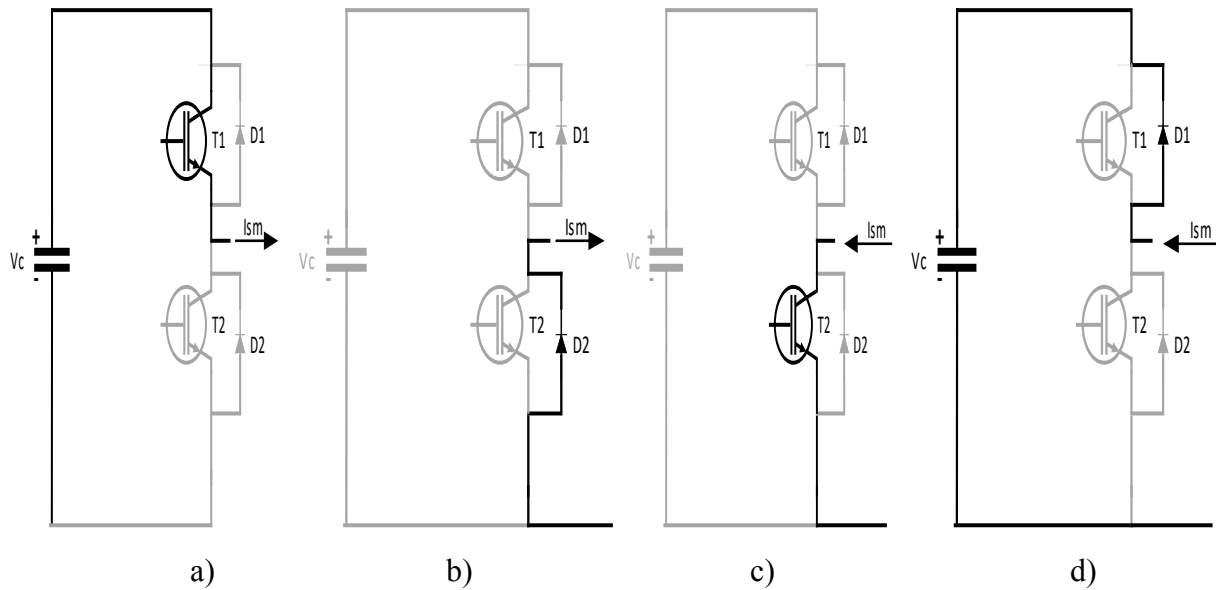
Figure 3-3: Switching States of Half-bridge SMs

For the operation of any SM, it is mandatory that the power flow is balanced over time if the normal operation conditions are desired. Thus, individual capacitor voltages need to be distributed as even as possible. The switching state of semiconductors depends on modulation waveform. If $Ism > 0$ and T1 conducts or $Ism < 0$ and D1 conducts the SM capacitor inserted and its voltage Vc is shown at the output Vsm (case a and d). Likewise, if $Ism > 0$ and D2 conducts or $Ism < 0$ and T2 conducts, the SM capacitor is bypassed. Thus, its voltage stays the same. Once the SM capacitor is inserted in the arm, it can be charged or discharged depending upon the direction of the arm current Ism.

3.2.   Modelling and operation of single and three phase MMC

In Figure 3.1 single phase MMC is shown. To extend the single phase to three phases, two more identical phases (b and c) can be added. The system becomes three upper arms, three lower arms total three legs and six arms, as seen in Figure 3.2.
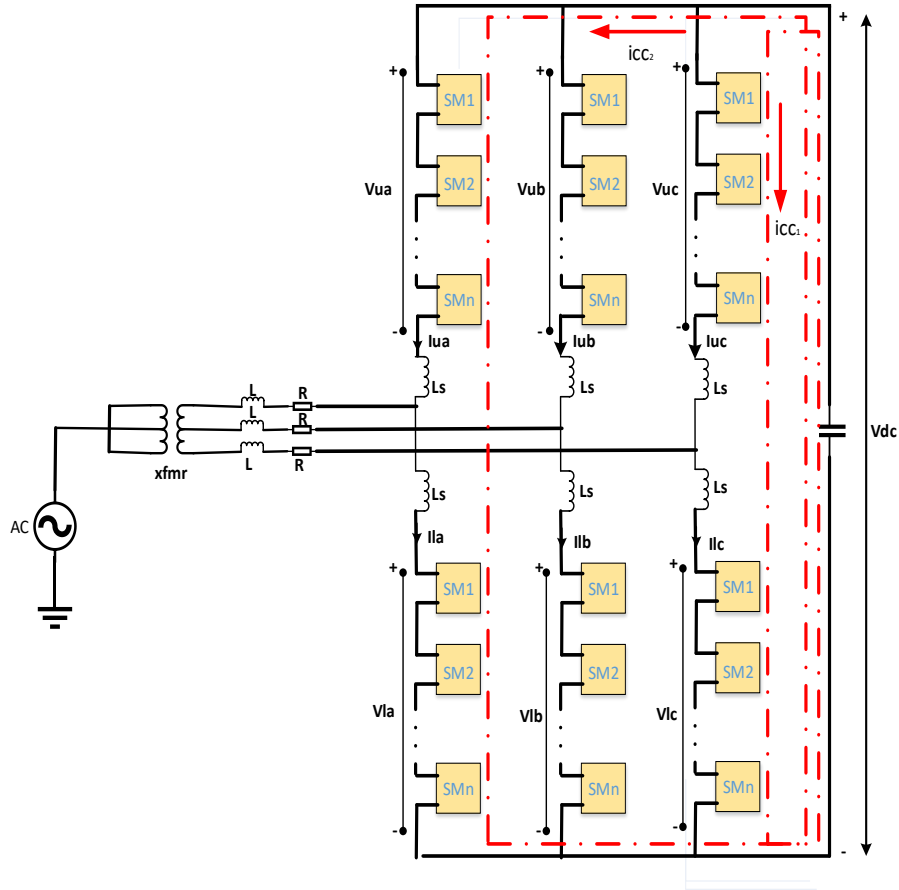
Figure 3-4: Three-phase MMC Structure

Parameters in Fig. 3.2 can be defined as following;

- Vac is the AC system source voltage

- L and R on the AC side, represent lumped impedance on the line between the MMC and AC grid

- Ls on the MMC, represent inductance of each arm of the converter

- Vux and Vlx stand for the total voltage of the upper and lower arms, respectively and x represents phases a,b and c.

- Iux and Ilx stand for the currents flow through upper and lower arms, respectively and x represents phases a, b and c.

- Red dotted lines represent circulating currents in the converter

In conventional VSC converters, the energy is stored in common link DC bus capacitor, but in an MMC converter, all submodules have their intrinsic capacitors as seen in Figure 3.2 a and b which reduces the cost and increases the reliability. With the help of modulation techniques, it is desired to keep these capacitors voltage distributions as even as possible to get smooth AC voltage waveform. The number of levels at the AC voltage waveform is the number of SM per arm plus one to account for the zero level. If all the SMs are inserted at the same time, the total DC voltage becomes $2V_{dc}$. The sum of the individual capacitor voltages in an arm is equal to Vdc.

$$V_{dc} = V_{c,u,l} \; X \; N_{sm} \tag{3.1}$$

Where N_{sm} is the number of SMs per arm and V_c is the nominal capacitor voltage. If the half of the SMs in the upper arm are inserted and half of the SMs in the lower arm inserted, the instantaneous value of the AC voltage will be zero. The average voltage can be calculated with $eq.$ (3.2).

$$V_{c,u,l} = \frac{Vdc}{Nsm} \tag{3.2}$$

Figure 3.5 shows the five level MMC output voltage in the range of 2kV and -2kV in Matlab/Simulink. In the figure, evenly voltage distribution is seen between maximum and minimum voltage peaks.
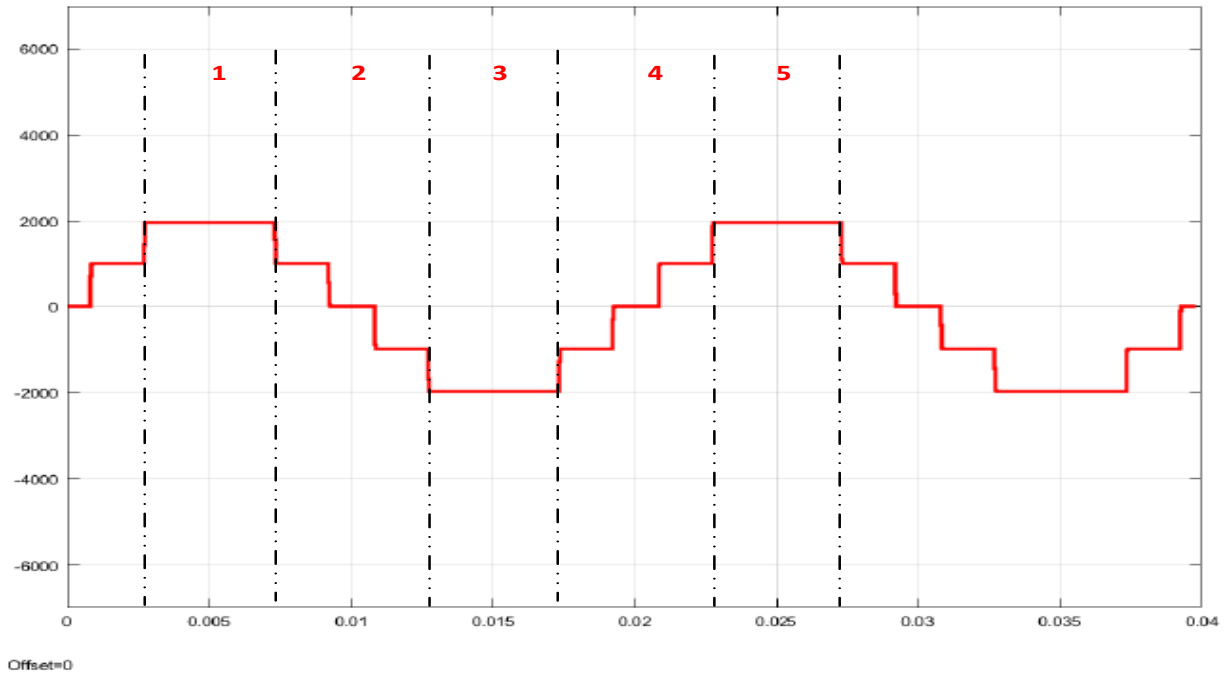
Figure 3-5: Five-level MMC Output Voltage Waveform

As can be seen figure above, although there are four SM per leg (N=4), the output will be expected N+1 level. One of the critical design consideration of modulation is that all SMs per leg cannot be operated at the same time. Only half of them are allowed to operate to give the Vdc, otherwise $2Vdc$ is seen at the output.

In section 1; the MMC gives the maximum output voltage making all the SMs in the upper arm bypassed and keep the capacitor voltages at the same level. On the other hand, all the SMs in the lower are inserted.

In section 2: output voltage seems decreasing gradually inserting some of SMs in the upper arm and bypassing some others in the lower arm. However, the total number of SMs connected per leg must be the same for any instant.

In section 3: this case is the same as section 1, yet this time all the upper SMs are inserted and all the lower ones are bypassed and keep their capacitor voltages remain.

In section 4: the output voltage reaches the minimum peak in previous section, now it gradually starts peaking again by inserting some SMs in the lower arm and bypassing some others in the upper arm.

In three phase MMC, there are three types of currents, DC current, AC current and a circulating current. Circulating current term is introduced with MMC topology and it flows through six arms. In normal conditions, DC current is divided by three among legs, AC current is evaluated per leg basis and it is divided two among arms for each phase. Circulating current occurs because of imbalances between SM voltages in each arm, yet it does not have any effect on the output of the MMC. However, it does have an effect on the efficiency, negatively so circulating current suppressing controller will be implemented in next chapters. Upper and lower arm currents mathematically expressed as follows;

$$iua = \frac{i_{ACa}}{2} + \frac{i_{DC}}{3} + i_{circ} \tag{3.3}$$

$$iub = \frac{i_{ACb}}{2} + \frac{i_{DC}}{3} + i_{circ} \tag{3.4}$$

$$iuc = \frac{i_{ACc}}{2} + \frac{i_{DC}}{3} + i_{circ} \tag{3.5}$$

$$ila = -\frac{i_{ACa}}{2} + \frac{i_{DC}}{3} + i_{circ} \tag{3.6}$$

$$ilb = -\frac{i_{ACb}}{2} + \frac{i_{DC}}{3} + i_{circ} \tag{3.7}$$

$$ilc = -\frac{i_{ACc}}{2} + \frac{i_{DC}}{3} + i_{circ} \tag{3.8}$$

Circulating current can be expressed differently for each phase;

$$i_{circa} = \frac{iua + ila}{2} - \frac{I_{dc}}{3} \tag{3.9}$$

$$i_{circb} = \frac{iub + ilb}{2} - \frac{I_{dc}}{3} \tag{3.10}$$

$$i_{circc} = \frac{iuc + ilc}{2} - \frac{I_{dc}}{3} \tag{3.11}$$

$$i_{circa} + i_{circb} + i_{circc} = 0 \tag{3.12}$$

Arm voltages can be expressed mathematically applying KVL as following;

$$V_{ua} = \frac{V_{dc}}{2} - V_{ao} - Ls\frac{di_{ua}}{dt} \tag{3.13}$$

$$V_{ub} = \frac{V_{dc}}{2} - V_{bo} - Ls\frac{di_{ub}}{dt} \tag{3.14}$$

$$V_{uc} = \frac{V_{dc}}{2} - V_{co} - Ls\frac{di_{uc}}{dt} \tag{3.15}$$

The dc-link voltage V_{dc} can be mathematically expressed as following;

$$V_{dc} = v_{ua} + v_{la} + 2Ls\frac{di_{circ}}{dt} \tag{3.16}$$

3.3. Switching and average model of MMC

To get a higher voltage output with an MMC based VSC converter, the number of levels must be higher in the case of the France – Spain HVDC link with 401 level MMC-1, used as a rectifier [16]. However, computational task also requires machines with high computing power and large memory and takes long time to simulate. Thus, switching model is very practical to capture the MMC internal dynamics in detail during abnormal conditions [17]. Nevertheless, Gnanarathna et al. [18] uses Dommel's Nortonand Thevenin equivalent circuits of for the SM capacitor, and two state resistor representation for the switching devices as seen in fig 3.6 and the single phase MMC implementation in fig. 3.7. It reduces the computation time, which increases because of detail switching models, significantly.

14
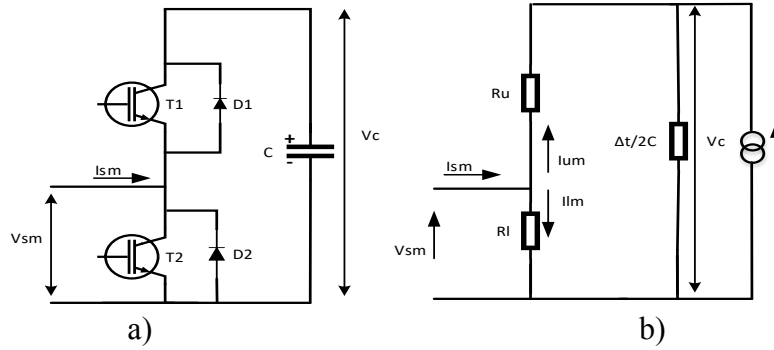
Figure 3-6: Structure of a) a half-bridge SM b) structure of Dommel EMT representation of a half-bridge

$$i_c(t) = c\frac{dV_c(t)}{dt} \tag{3.17}$$

$$V_c(t) = \frac{\Delta t}{2C}x i_c(t) + V_{ceq}(t - \Delta t) \tag{3.18}$$

$$V_{sm}(t) = i_c(t)x R_{eq} + V_{ceq}(t - \Delta t) \tag{3.19}$$
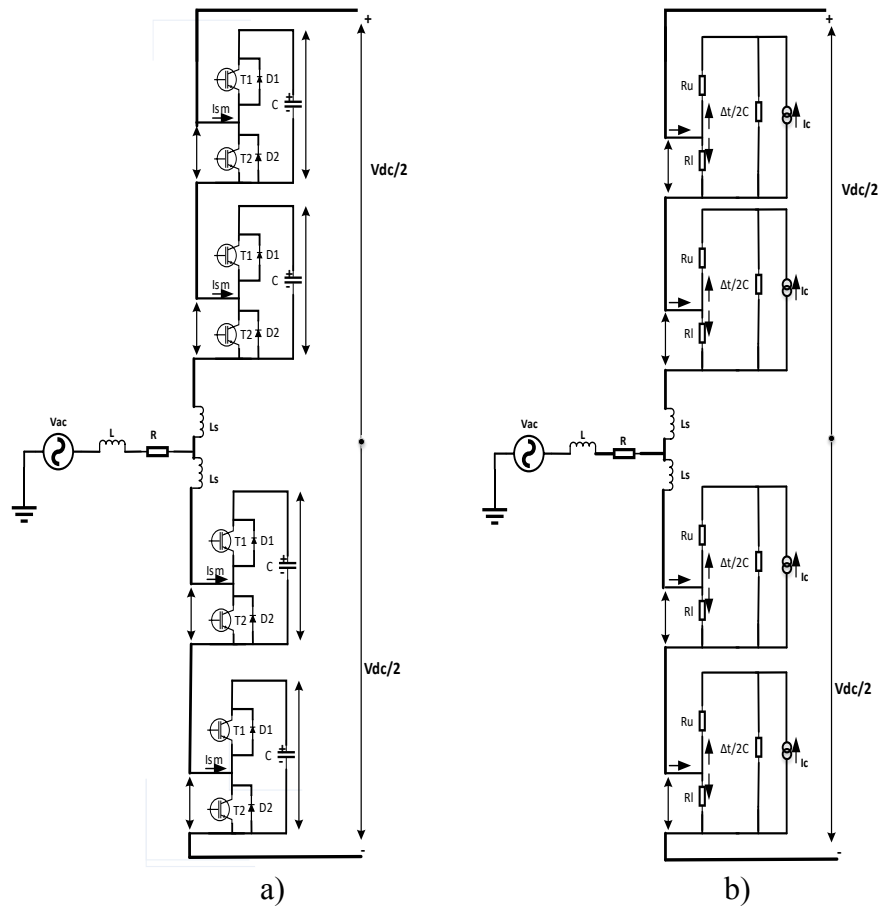
Figure 3-7: Structure of a Single Phase MMC a) Half-bridge SM b) Dommel EMT Representations

Since the SMs share the same current flows through the arm, total arm voltages can be expressed in eq. 3.21 and 3.22;

$$V_u(t) = \sum_{uk} V_{sm}(t) \tag{3.20}$$

$$V_l(t) = \sum_{lk} V_{sm}(t) \tag{3.21}$$

The operation of the structure in fig 3.6 b, is the same as in fig 3.6 a. depending upon the switching operation, on or off resistance of the controllable switches is mimicked. Dynamic of the SM within each Δt time step can be mathematically expressed as follows;

$$\begin{bmatrix} \dfrac{Rl+Ru}{RuxRl} & \dfrac{-1}{Ru} \\ \dfrac{-1}{Ru} & \dfrac{\Delta t + 2CRl}{Rl\Delta t} \end{bmatrix} \begin{bmatrix} Vsm \\ Vc \end{bmatrix} = \begin{bmatrix} Ism \\ Ic \end{bmatrix} \tag{3.22}$$

In Figure 3.8, a half-bridge SM has built with controllable voltage and current source to reduce the simulation speed for MMCs with the high number of SMs, yet the operation principle is the same.

(a)

(b)
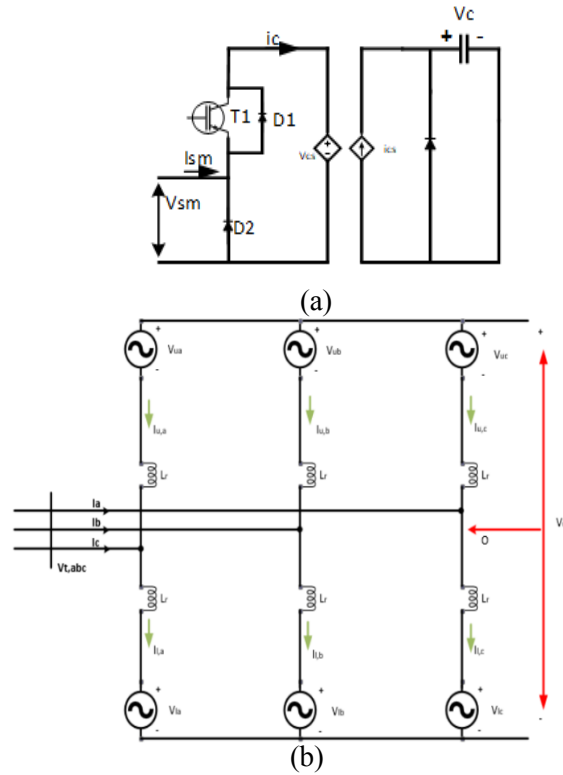
Figure 3-8: Averaged Model Half-bridge SM (a) and Three-phase MMC (b) based on Thevenin Equivalent

Chapter 4   MMC Modulation Techniques

Modulation technics for an MMC can be explained in two different categories, Pulse Width Modulation (PWM) and Nearest Level Modulation (NLM) technics. While PWM requires voltage balancing and averaging control technics for implementation in RTDS, NLM requires Circulating Current Suppressing Control (CCSC).

4.1. Sinusoidal Pulse-Width Modulation (SPWM)

There are different modulation technics for generating gate signals for controllable switches in this case for IGBTs. Sinusoidal Pulse-Width Modulation and its derivatives are most commonly used. The main idea behind this modulation technic is that a set of triangular carrier waveforms (usually 10 times faster) are generated to compare with a normalized reference sinusoidal waveform. However, it is a tradeoff that the user wants to have lower switching losses with relatively high harmonics or lower harmonics with relatively higher switching losses with higher switching frequency. PWM technic does not change for any cases when the reference is higher than the carrier, a "high" signal is sent to the switch, and otherwise a "low" signal is sent. This can be easily seen in figure 4.4. In the figure below, yellow line represents the normalized sinusoidal waveform, while the red triangular waveform is a carrier signal. As a result of this comparison, green line is produced.
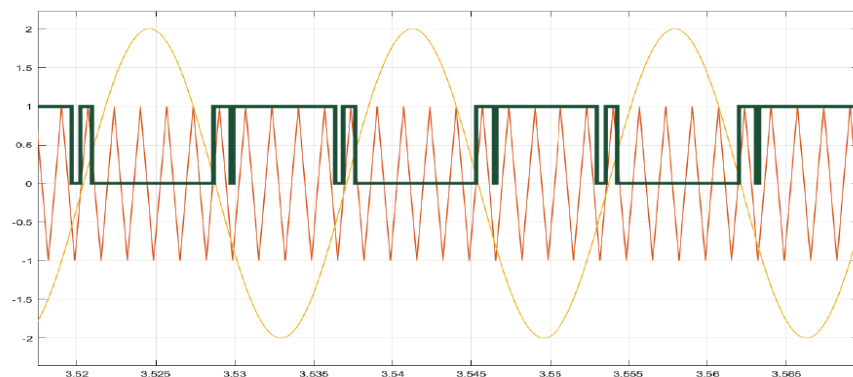
Figure 4-1: Sinusoidal PWM Pattern

4.2. Phase-Shifted Sinusoidal Pulse-Width Modulation (PS-SPWM)

In this switching technic, many different phase-shifted triangular carrier waveforms are compared with normalized sinusoidal reference waveform [24]. The carriers are phase-shifted to reduce the harmonics at the output signal. To implement this switching technic to a MMC system with higher number of SMs brings a lot of complexities because the number of carrier frequencies should increase proportionally with the modules and the scheme becomes very complex. In figure 4.5, five carrier frequencies and one reference sinusoidal sine wave are shown. The thick yellow line shows the overall number of inserted modules.
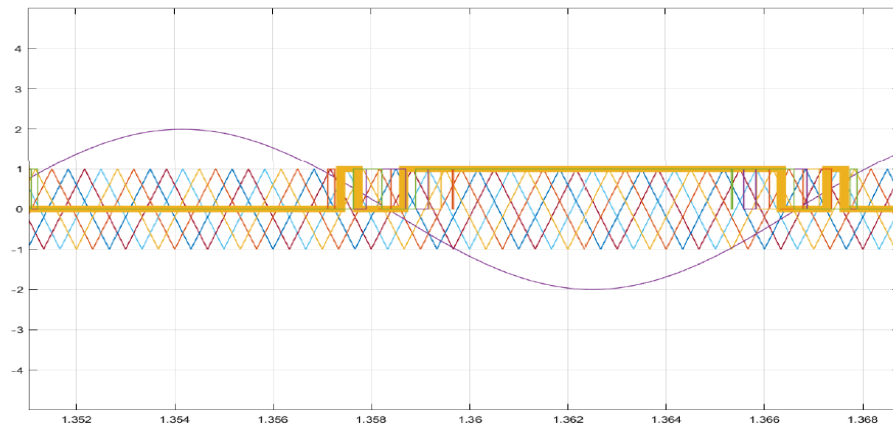
Figure 4-2: PS-SPWM Pattern

4.3. Phase-Disposition Sinusoidal Pulse-Width Modulation (PD-SPWM)

This technique is very similar to PS-SPWM, but instead of shifting phases, carrier waveform are displaced symmetrically with respect to the zero-axis [6]. N number of carrier signals are used with the amplitude of $2/N$ each and they are offset vertically.

4.4. Nearest Level Modulation (NLM) Technic

NLM is an alternative method to carrier-based PWM for modulation of MMCs. Although PWM modulation generates better voltage quality than that of NLM. Nevertheless, in case of higher number of SMs required, it is easier to implement the NLM since its computational time less than PWM. Basic idea behind NLM is to determine the number of cells to be inserted or bypassed on the comparison of the modulating signal Vref(t) with the voltage steps that represent idealized cell capacitor voltages [25]. Unlike PWM technic, there is no carrier signal in NLM modulation technic so modulation index and harmonic content in the output can be manipulated by changing the sampling frequency. Again, losses and harmonics tradeoff take in place while deciding the sampling frequency. To determine the minimum required sampling frequency eq. (4.1) can be used. In this case, f_s can be regarded as the limit for harmonic content, if f_s increases more, harmonics cannot go further.

$$f_s = f\pi N_{sm} \tag{4.1}$$

To calculate the number of SM inserted in the upper arm;

$$n_{inserted} = round\left[\left(\frac{0.5V_{dc}-V_{ref_{a,b,c}}}{V_c}\right)\right] \tag{4.2}$$

Where N=Total number of SM in an arm, $n_{bypassed} = N - n_{inserted}$.

To calculate the number of SM inserted in the lower arm;

$$n_{inserted} = round\left[\left(\frac{0.5V_{dc}+V_{ref_{a,b,c}}}{V_c}\right)\right] \tag{4.3}$$

Where N=Total number of SM in an arm, $n_{bypassed} = N - n_{inserted}$.

To determine the number of SMs inserted eq. (4.2 and 4.3) are used. The idea behind these equations is to determine the number of inserted capacitor. To do this, if the arm current is positive, the previously bypassed SMs with lowest capacitor voltages are chosen such that they start

charging. There also previously bypassed capacitor with high voltages exist. To discharge these capacitor, they need to be inserted when the arm current is negative such that they can start discharging. There are also previously inserted SM capacitors need to be bypassed to balance their voltages. Capacitors with the highest voltages are chosen if the arm current is positive so that they stop charging and capacitors with the lowest voltages are chosen if the arm current is negative such that they stop discharging. Fig. 4.3 shows the NLM algorithm flowchart.
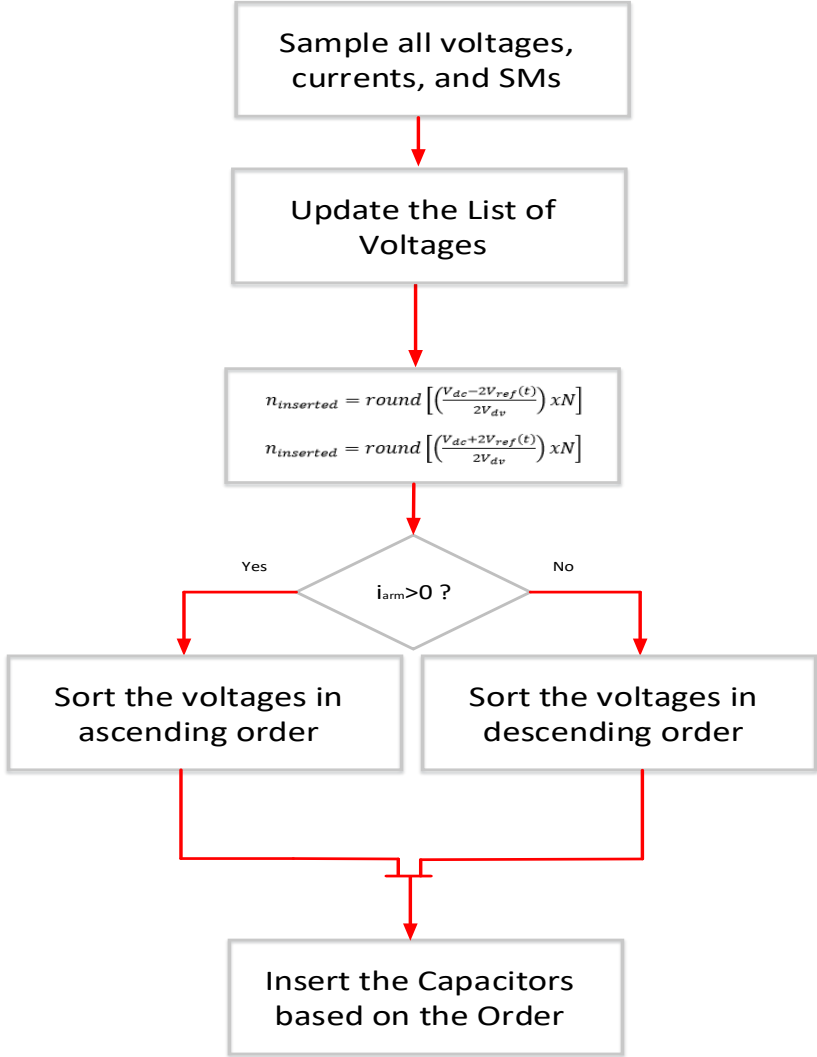

Figure 4-3: NLM Algorithm

Chapter 5 Power Flow and MMC Control
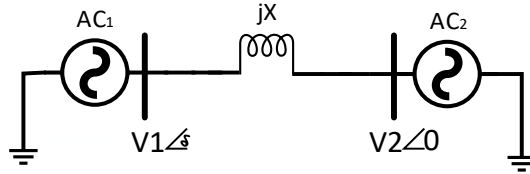
5.1. Principle of AC Power Transfer

Figure 5-1: Power flow

$$I_{12} = \frac{V_1 - V_2}{jX} \tag{5.1}$$

$$I_2 x cos(\varphi) = V_1 \sin(\delta) \tag{5.2}$$

$$S_{12} = \frac{j|V_1|^2}{X} - \frac{jV_1 V_2{}^2}{X} \tag{5.3}$$

$$P_{12} = \frac{|V_1||V_2|}{X} x sin(\delta) \tag{5.4}$$
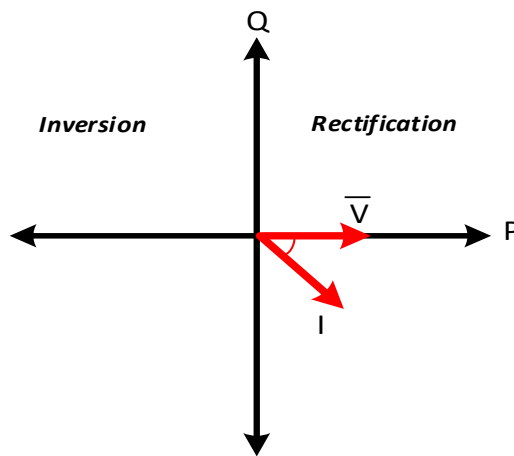
Figure 5-2: Power Transfer Scheme

If the arm voltage and the arm current is positive, power flows from DC bus to AC grid which is an inversion operation. Likewise, both current and voltage are negative, power flows the same direction. Unlike, if the arm current is positive, and the arm voltage is negative to the reference point, power flows from AC grid to DC bus, which is a rectification operation. Similarly, if the arm current is negative and the arm voltage is positive to the reference point, this is a rectification operation.

5.2. Control of MMC

Control system of an MMC for HVDC system can be complex because of high number of SMs and their control structure, shown in fig. 5.3. As mentioned before, the energy is not stored one bulk DC link capacitor, instead the energy needs to be stored as evenly as possible among the SM capacitors with the help of the specific control algorithm. A vector control technic, calculating a voltage-time area across the converter equivalent inductor $\frac{L_s}{2}$, which is used for changing the current from the present value to the reference value, is used in the MMC converters. The dq reference frame current orders to the controller are calculated from preset P and Q powers, and preset Vac and Vdc voltages. Controller of AC voltage, producing the modulated switching pattern, is controlled by the inner controller. To control the active and the reactive power independently proportional-integral (PI) controller are used [20], [21]. The control system in dq frame is used as the d axis current control for active power control whereas q axis current control for reactive power control. To control the active power, frequency or DC voltage can be controlled or a power reference can be set. Reactive power can be controlled by AC voltage control or reactive power reference can be set. V_{iq} is forced to zero by PLL and it will yield eq. 5.5 and 5.6

$$P_i + jQ_i = \frac{3}{2}\left(V_{id} + jV_{iq}\right)\left(i_d + i_q\right), \ P = \frac{3}{2}V_d i_d \tag{5.5}$$

$$Q = -\frac{3}{2}V_d i_q \tag{5.6}$$
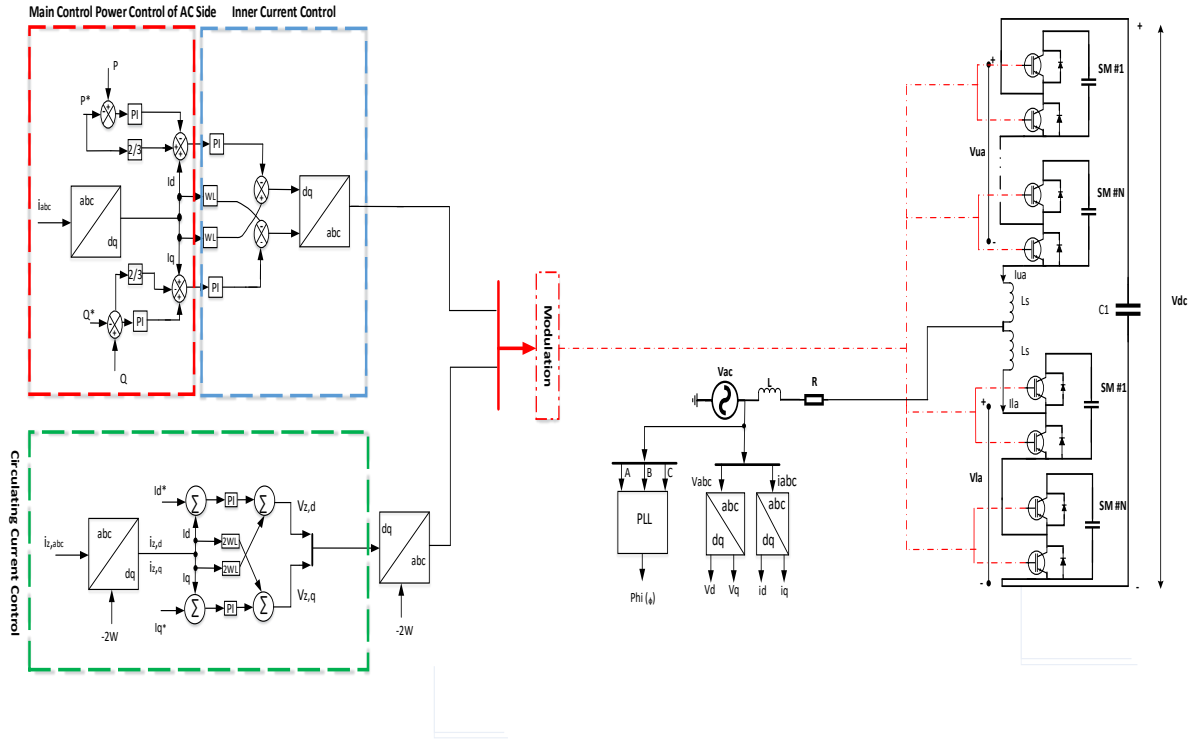
Figure 5-3: Control Scheme of Single Phase MMC

5.3. Mathematical Expressions of the operation of MMC Converters

In order to build a controller, both AC and DC sides need to be modelled mathematically [4]. Figure 3.4 is taken as a reference for the following calculations;

AC side dynamics are expressed as following where i_a, i_b, i_c are the leg currents while v_a, v_b, v_c are AC side voltages where $\frac{V_{ux} - V_{lx}}{L} = u_x$, x=(a,b,c).

$$\frac{di_a(t)}{dt} = \frac{V_a}{L} - u_x \tag{5.7}$$

$$\frac{di_b(t)}{dt} = \frac{V_b}{L} - u_x \tag{5.8}$$

$$\frac{di_c(t)}{dt} = \frac{V_c}{L} - u_x \tag{5.9}$$

If dq park transformation is applied to equations 5.7 through 5.9;

$$L\frac{di_d}{dt} = V_d - u_d + Lwi_q \tag{5.10}$$

$$L\frac{di_q}{dt} = V_q - u_q - Lwi_d \tag{5.11}$$

w in eq. (5.10 and 5.11) is the angular frequency of the system. In normal conditions, V_q in eq.
(5.11) is zero.

P in eq. (5.5) is the real power, transferred from AC side to the converter while Q in eq. (5.6) is a
reactive power, transferred from AC side to the converter. Voltage across the transformer is
generally controls the active power (P). PI controllers are used to compare active power
measurement in the system with the reference desired Preference. If Preference >P error signal (e)
will be positive and the voltage across the transformer increases. If P>Preference, e will be the
negative and the voltage across the transformer decreases. Reactive power (Q) is flows from higher
magnitude side to the lower magnitude side and it depends on the magnitude difference in the
voltage. Like real power control, PI controllers are also used for reactive control. If Qreference>Q
e will be positive and modulation index m increases. If Q>Qreference, m decreases.

$$m_d = \frac{V_d}{kV_{dc}} \text{ and } m_q = \frac{V_q}{kV_{dc}} \tag{5.12}$$

$$m = \frac{Voltage\ across\ low\ side\ of\ xmrf}{Vdc/2} \tag{5.13}$$

$$I_{dc} = \frac{3}{2}(m_d i_d + m_q i_q) \tag{5.14}$$

Where V_d and V_q are the output voltages of the MMC converter and k depends on the modulation
technique [23]. Under normal conditions, only positive sequence components of voltage and
current are seen in the system. Thus, while positive sequence components regulate the DC bus
voltage, negative sequence components keep the AC current balanced and eliminate the DC bus
double line ripples. I_d, which is a dc component of the arm current helps to exchange the power
between DC and the each leg.

5.4. Capacitor Voltage Balancing Algorithm

Capacitor voltage balancing control is one of the critical part of control systems of MMCs. As the working principle of MMCs, SM capacitors may be charged or discharged depending upon the direction of the arm current. When the I_{sm} is positive, the capacitor is charged or when the I_{sm} is negative, the capacitor is discharged. To be able to equate the sum of the individual turned on capacitor voltages to the DC link voltage, and to distribute the voltages as evenly as possible, a control algorithm is needed. There is sorting and selecting technic to decide the minimum and maximum values among the SM capacitors. The main idea behind sorting algorithm is that if the arm current Ism is positive, the SM, with the lowest voltage in the arm, will turned on and if the arm current Ism is negative, the SM, with the highest voltage in the arm, turned on [6]. In other words, if the capacitor voltages of the SM in the arm higher than the reference voltage, a positive arm power should be taken from the SMs to the DC bus.
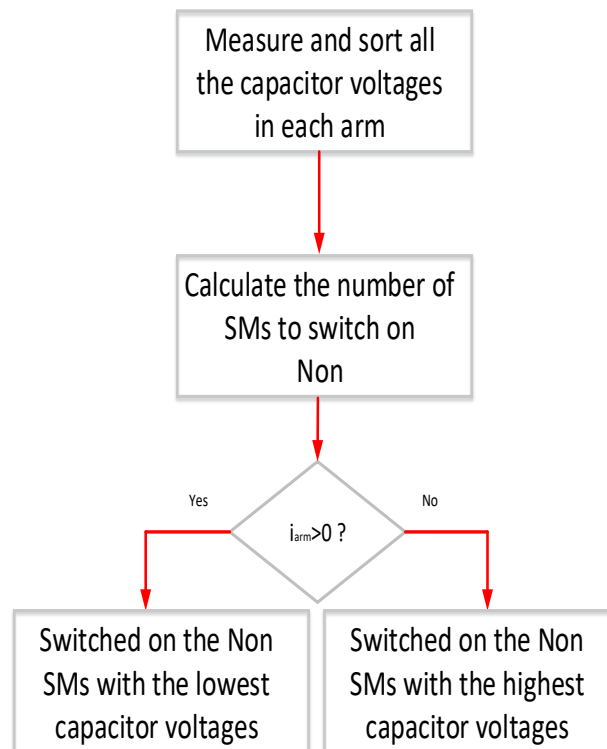
Figure 5-4: Capacitor Voltage Balancing Algorithm

5.5. Circulating Current Suppressing Controller (CCSC)

Circulating current elimination or minimization is the second important part of the control system after capacitor voltage balancing control. Circulating current exists in an MMC because of the voltage and the phase difference between the upper and lower arms. Circulating current has the second-harmonic component as can be seen in fig. 5.5. Its frequency is double the fundamental frequency and it is phases A, C and B sequence. Although it does not have any effect on the AC side and does not leave the converter, the existence of the second harmonic distorts the arm currents and causes the ripple increment in individual capacitor voltages. As a result, circulating current affects the rating of components, efficiency and losses negatively. There are some ways to suppress the circulating current.

- Increasing the size of the arm inductor which decreases the rapidness of control response and increases the system cost [27].

- Adding a parallel capacitor (resonant filter) in the middle point of a leg [19].

- Implementing the Circulating Current Suppression Control (CCSC) proposed in [28].

As claimed in [19], the CCSC eliminates the second harmonic of AC component of the circulating current and decreases the voltage ripple from 30% to 8%.
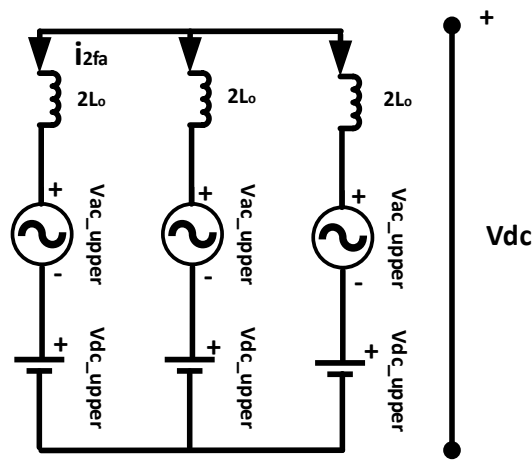
Figure 5-5: Circulating Current Equivalent

$$\begin{bmatrix} V_{circa} \\ V_{circb} \\ V_{circc} \end{bmatrix} = R \begin{bmatrix} I_{circa} \\ I_{circb} \\ I_{circc} \end{bmatrix} + L \begin{bmatrix} I_{circa} \\ I_{circb} \\ I_{circc} \end{bmatrix} \tag{5.15}$$

$$i_{diff,a} = \frac{I_{dc}}{3} + I_{2f} \sin(2wt + \varphi) \tag{5.16}$$

$$\begin{bmatrix} V_{circd} \\ V_{circq} \end{bmatrix} = R \begin{bmatrix} I_{circ-d} \\ I_{circ-q} \end{bmatrix} + L \begin{bmatrix} I_{circ-d} \\ I_{circ-q} \end{bmatrix} + \begin{bmatrix} 0 & -2wL \\ 2wL & 0 \end{bmatrix} \begin{bmatrix} I_{circ-d} \\ I_{circ-q} \end{bmatrix} \tag{5.17}$$

To create control block diagram of CCSC eq. (5.15-5.17) are used. Eq. 5.16 is derived only for Phase A.
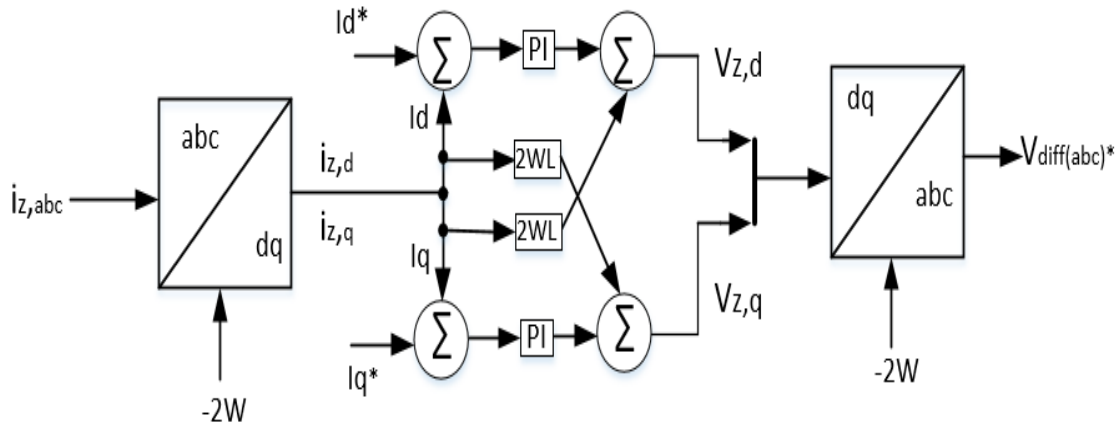
Figure 5-6: Circulating Current Suppression Control Block Diagram

Chapter 6　　　　Study Systems and Implementations

　　　　This chapter is divided in two sections. Proposed feed-forward current control scheme is implemented for MMC based Point to Point HVDC system under balanced and unbalanced grid conditions and results are demonstrated in RTDS in chapters 6.1 through 6.3. In chapter 6.4, ongoing five level back-to-back MMC implementation is presented, and simulated in EMTD/PSCAD and MATLAB/Simulink.

6.1. Feed-forward Current Control Strategy

The inner current control is a fundamental part of MMC control system. The current control allows other controls such as DC voltage, AC voltage, active power and reactive power controls. The common method to develop the current control is by modelling the AC system of the converter and applying dq transformation to represent the three-phase AC system in the synchronous reference frame. This control scheme is implemented for MMC based Point to Point HVDC system which is seen fig. 6.1 and its parameters are seen in tab. 6.1. The Bergeron transmission line model is chosen because time step is (Δt) 50 usec and it does not produce an artificial resonance at high frequencies. 400/333-kV three phase transformer with its secondary winding connected in delta to block the zero-sequence voltages generated by the MMC.

Figure 6.1: Point to Point HVDC System

$$V_{s,abc} = \begin{pmatrix} v_{s,a} \\ v_{s,b} \\ v_{s,c} \end{pmatrix} = \begin{pmatrix} \widehat{v_a}\sin(\theta_a) \\ \widehat{v_b}\sin(\theta_b) \\ \widehat{v_c}\sin(\theta_c) \end{pmatrix} \tag{6.1}$$

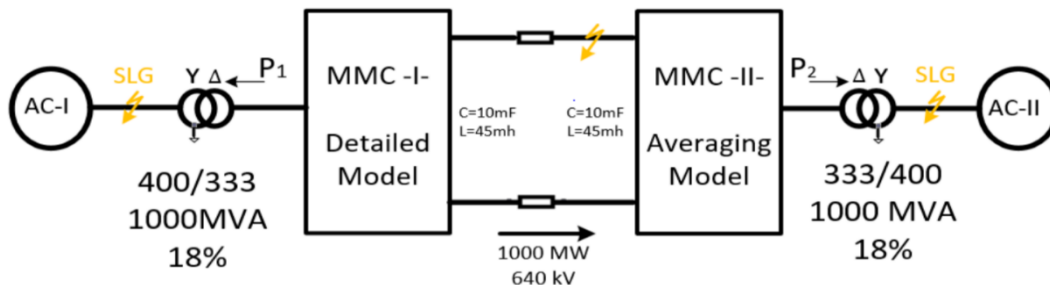$$i_{abc} = \begin{pmatrix} i_a \\ i_b \\ i_c \end{pmatrix} = \begin{pmatrix} \widehat{I_a}\sin(\theta_a + \alpha) \\ \widehat{I_b}\sin(\theta_b + \alpha) \\ \widehat{I_c}\sin(\theta_c + \alpha) \end{pmatrix} \tag{6.2}$$

$$\theta_{abc} = \begin{pmatrix} \theta_a \\ \theta_b \\ \theta_c \end{pmatrix} = \begin{pmatrix} \omega t \\ \omega t - \frac{2\pi}{3} \\ \omega t + \frac{2\pi}{3} \end{pmatrix} \tag{6.3}$$

Table 6-1: MMC Based HVDC System Parameters of Figure 6.1

Symbol	Description	Value	Unit
P	Base MVA	1000	MVA
V_{DC}	DC voltage	640	kV
$v_{s,abc}$	Line-Line AC voltage	400	kV
T	Transformer (Y_g - Δ)	400/333	kV
N	Number of SM per arm	400	-
V_c	Capacitor Voltage	1.6	kV
F	Fundamental frequency	60	Hz
L_o	Arm inductance	45 (15%)	mH (PU)
L	Transformer inductance	53 (18%)	mH (PU)
C	SM capacitance	10	mF

Where $\widehat{v_a}$, $\widehat{v_b}$, and $\widehat{v_c}$ are the peak values of the three-phase AC voltages, and $\widehat{I_a}$, $\widehat{I_b}$, and $\widehat{I_c}$ are the peak values of the three-phase AC currents. α is the phase-shift between the voltage and the current, and ω is the fundamental angular frequency. The dynamic equation of AC aside of MMC can be derived by applying Kerchief Voltage Law (KVL) as follows;

$$v_{m,abc} = v_{s,abc} + L\frac{di_{abc}}{dt} + Ri_{abc} \tag{6.4}$$

Where $v_{m,abc}$ the AC output voltages of MMC, and L and R is represent the transformer inductance and the resistance.

Assuming the d axis is in phase with the AC voltage v_{sa} and the dq transformation matrix T of the AC voltages and currents is as follows;

$$T = \frac{2}{3} \begin{pmatrix} \sin(\theta_a) & \sin(\theta_b) & \sin(\theta_c) \\ \cos(\theta_a) & \cos(\theta_b) & \cos(\theta_c) \end{pmatrix} \tag{6.5}$$

$$\begin{pmatrix} x_d \\ x_q \end{pmatrix} = T \begin{pmatrix} x_a \\ x_b \\ x_c \end{pmatrix}, x = v_{s,i} \tag{6.6}$$

The dynamic equation of AC side system of MMC is defined in the dq reference as follows;

$$v_{m,d} = v_{s,d} - wLi_q + L\frac{di_d}{dt} + Ri_d \tag{6.7}$$

$$v_{m,q} = v_{s,q} - wLi_d + L\frac{di_q}{dt} + Ri_q \tag{6.8}$$

$$i_d = \frac{1}{3}\left[\overbrace{\cos(\alpha)\left(I_{ma} + I_{mb} + I_{mc}\right)}^{i_{d,dc}} - \overbrace{\left\{I_{ma}\cos(2wt + \alpha) + I_{mb}\cos\left(2wt - \frac{2\pi}{3} + \alpha\right) + \right.}^{i_{d,ac}}\right.$$

$$\left. I_{mc}\cos\left(2wt + \frac{2\pi}{3} + \alpha\right)\right\}\right] \tag{6.9}$$

$$i_q = \frac{1}{3}\left[\overbrace{\sin(\alpha)\left(I_{ma} + I_{mb} + I_{mc}\right)}^{i_{q,dc}} + \overbrace{\left\{I_{ma}\sin(2wt + \alpha) + I_{mb}\sin\left(2wt - \frac{2\pi}{3} + \alpha\right) + \right.}^{i_{q,ac}}\right.$$

$$\left. I_{mc}\sin\left(2wt + \frac{2\pi}{3} + \alpha\right)\right\}\right] \tag{6.10}$$

The inner current control is developed to generate the command output voltage of the MMC. However, the dq currents and voltages can be decomposed into DC and AC components

in eq (6.9) and (6.10). The AC components cause the double line frequency on the DC voltage, active and reactive power [4], [5]. Thus, the dq transformation matric of the voltages T_{vs} and currents T_i grid can be written in terms of the AC and DC components as follows;

$$T_{vs} = \frac{1}{3}\begin{pmatrix} 1 & 1 & 1 \\ -\cos(2\theta_a) & -\cos(2\theta_b) & -\cos(2\theta_c) \\ 0 & 0 & 0 \\ \sin(2\theta_a) & \sin(2\theta_b) & \sin(2\theta_c) \end{pmatrix} \tag{6.11}$$

$$\begin{pmatrix} v_{s,d}^{dc} \\ v_{s,d}^{ac} \\ v_{s,q}^{dc} \\ v_{s,q}^{ac} \end{pmatrix} = T_{vs}\begin{pmatrix} \hat{v}_a \\ \hat{v}_b \\ \hat{v}_c \end{pmatrix} \tag{6.12}$$

$$T_i = \frac{1}{3}\begin{pmatrix} \cos(\alpha) & \cos(\alpha) & \cos(\alpha) \\ -\cos(2\theta_a + \alpha) & -\cos(2\theta_b + \alpha) & -\cos(2\theta_c + \alpha) \\ \sin(\alpha) & \sin(\alpha) & \sin(\alpha) \\ \sin(2\theta_a + \alpha) & \sin(2\theta_b + \alpha) & \sin(2\theta_c + \alpha) \end{pmatrix} \tag{6.13}$$

$$\begin{pmatrix} i_{d,dc} \\ i_{d,ac} \\ i_{q,dc} \\ i_{q,ac} \end{pmatrix} = T_i\begin{pmatrix} \hat{I}_a \\ \hat{I}_b \\ \hat{I}_c \end{pmatrix} \tag{6.14}$$

Substituting (6.13 and 6.14) into (6.7 and 6.8), did/dt and diq/dt are derived in terms of AC and DC components, where $i_{dq} = i_{dq,dc} + i_{dq,ac}$. Therefore, the AC system dynamic equations of MMC becomes;

$$v_{m,d} = v_{s,d} - wL\big(i_{q,dc} - i_{q,ac}\big) - e \tag{6.15}$$

$$v_{m,q} = v_{s,q} + wL\big(i_{d,dc} - i_{d,ac}\big) + e \tag{6.16}$$

The DC component of dq currents $i_{dq,dc}$ is used to control the DC components of the DC voltage, active power, reactive power, and AC grid voltages. The proposed feedforward current control is developed based on equations (6.15) and (6.16) and visualized in fig. 6.2.
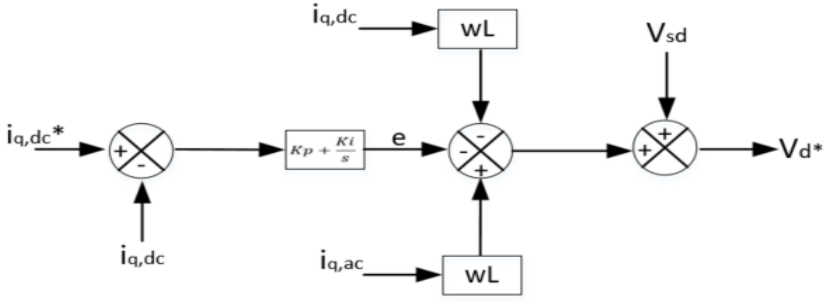
(a)
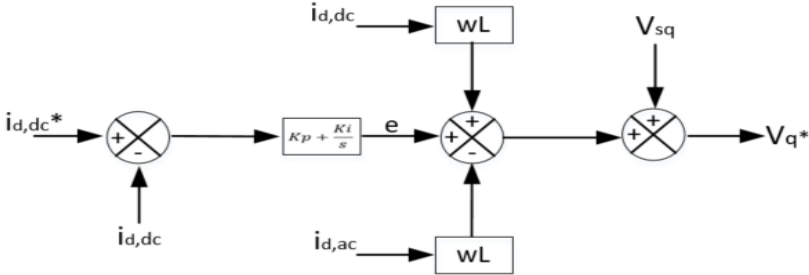
(b)

(c)

Figure 6-2: Proposed Current Controllers (a) and (b), Conventional Current Controller (c)

6.2. Real Time Simulation of Proposed Model in Real Time Digital Simulator (RTDS)

To be able to simulate the system in real time [29], RTDS hardware, which its cubical, called a rack and accompanying software, RSCAD, are used. A rack connects to various cards for different applications in real time. In fig.6.3, the system implementation is shown. To implement the system, FPGA based MMC support unit and RTDS are used.
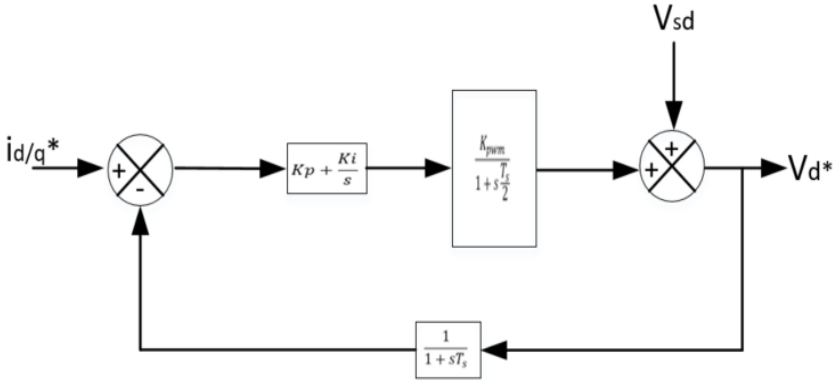

Main Computer   *RTDS Rack*   *FPGA Based MMC Support Unit*

(c)
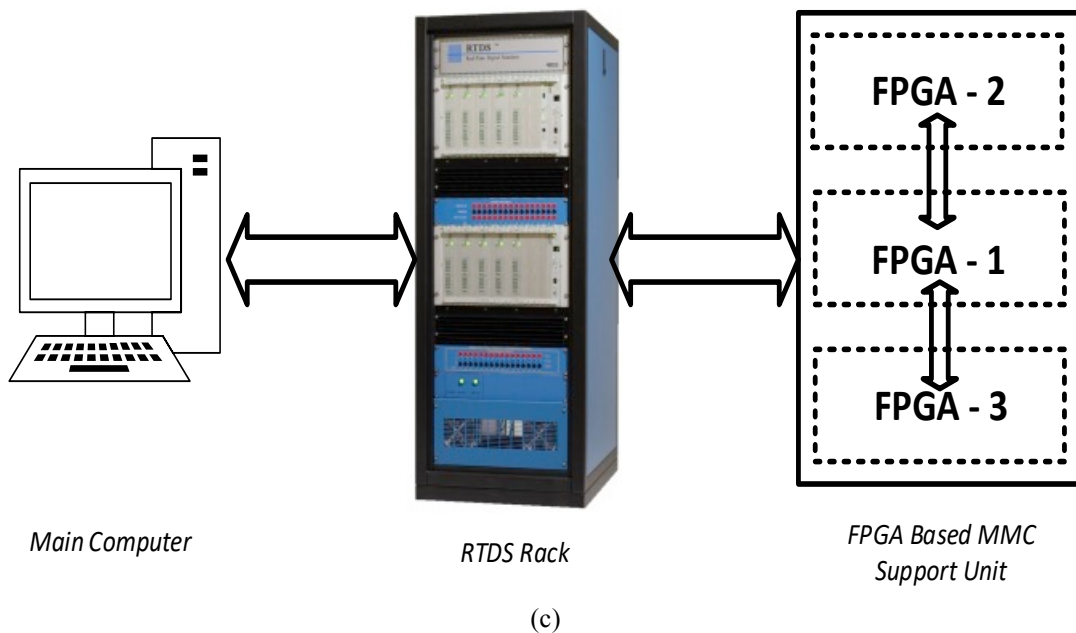
Figure 6-3: HIL Implementation of the System

There are certain rules regarding implementation a system in RSCAD. The user needs to be aware of the capacity of the rack and physical connections, as well. In the case of MMC implementations, if the number of SMs per arm is high and the switching model, explained in chapter 3.3, is used, MMC support units, will be explained later, will be used. However, if the number of level is not too many, PB5 cards generally enough to model the system. There are also other cards, which are I/O GTDO, and GTAI, along with the rack. GTDO card is a digital output

card, providing up to 64 output signals. Output signals are needed to be determined in RSCAD while the system was being build.

Figure 6-4: GTAO, GTDO and GTAI Cards

GTAO Card: The Gigabit Transceiver Analogue Output Card is for interfacing analogue signals from the RTDS to external devices such as MMC support unit. This card includes twelve, 16 bit analogue output channels with an output range of $\pm$10 V. It is input is 24V [24].

GTAI Card: The Gigabit Transceiver Analogue Input Card is for interfacing analogue signals from an external devices to the RTDS. This card includes twelve analogue input channels with each channel configure as a differential input range $\pm$10 V [24]. GTAI cards can take the voltages of MMC storage devices as long as its rated voltage in the range.

GTDO Card: The Gigabit Transceiver Digital Input Card (GTDO) is for interfacing digital signals from the RTDS to external devices. The cards includes 64 optically isolated digital output channels [24].

AC system and DC link are build similar to explained in chapter 3 and modelled in RTDS. In this case, three phase MMC simulated, its arm voltages are emulated in FPGA and sent to RTDS. This date set is used to solve the system and currents as a result sent back to the FPGA. In general, most MMC systems use small-time step (1.4 - 2.5us) interface in RSCAD rather than a large-time step (50us) to get more precise simulation. Each VSC circuit is solved as a sub and their connections are made with DC cables, providing decoupling and letting the systems to be simulated on two separate CPUs. In each time-step SM capacitor voltages are sent to controls from FPGAs. To interface a small-time step systems with the large-time step systems, interface transformers have to be used as seen figure 6.5.
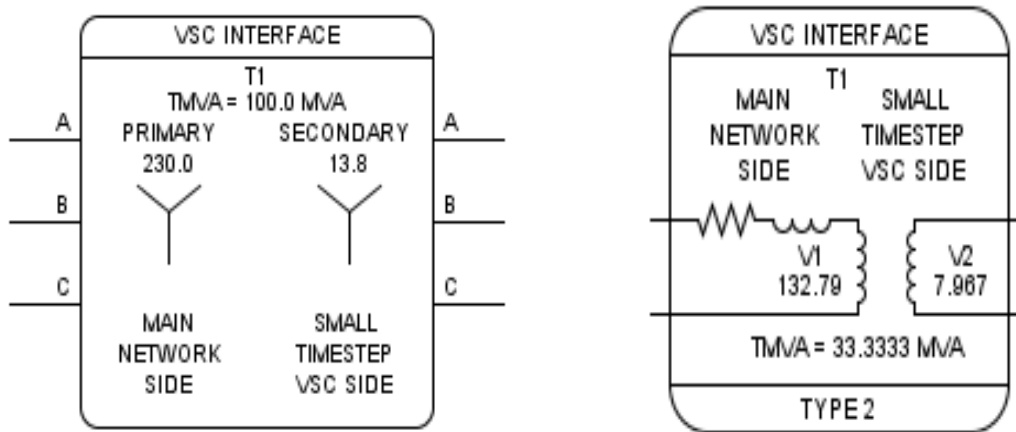
Figure 6-5: Interface Transformer between Small-time Step and Large-time Step

In this system, rtds_vsc_MMC_FPGA_U5 model, seen in figure 6.5, is used to simulate

legs as a block. Calculations are made in FPGA and interfaced into the PB5 processor card, which

is located in the rack, with a Bergeron ½ small time-step travel-time interface t-line [24]. Each SM

needs 8-bit firing pulse input word. If there are maximum eight SM, they can be packed into two

32-bit integers and sent to the FPGA from the PB5. If there are more than eight SMs, extra physical

connection needs to make to a controller.

Figure 6-6: rtds_vsc_MMC_FPGA_U5 Component

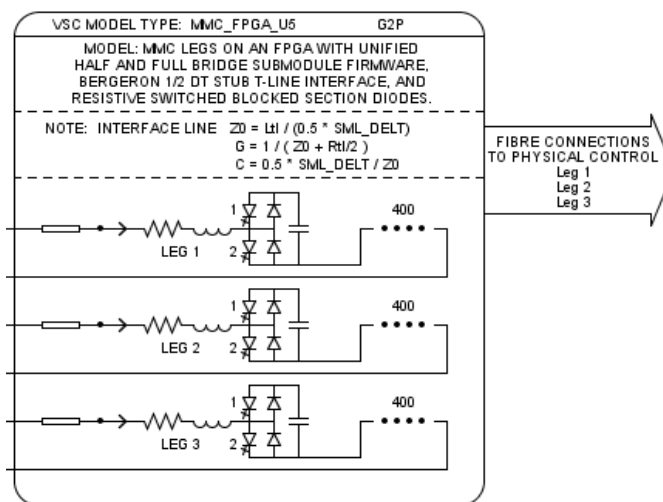The RTDS and FPGA based MMC support unit investigate the dynamic and quality performance of the proposed feedforward current control strategy. FPGAs are able to make calculations up to 512 SMs. Even if the user is modelled the system based on 400 SM per leg, like in this case and can be seen in figure 6.5, FPGAs still make the calculations for 512 SMs. The results from the superfluous 112 SMs are thrown away, but the calculations are still done. The MMC system controls the active and reactive power while the DC voltage is regulated using a controllable DC supply. Regarding the working principle of MMC models in RSCAD;

➢ At the beginning, all the SMs are blocked with no gate signal applied

➢ Intrinsic capacitors are charged through the anti-parallel diodes

➢ Once they are evenly charged and the terminal voltage is stabilized, the SMs are de-blocked

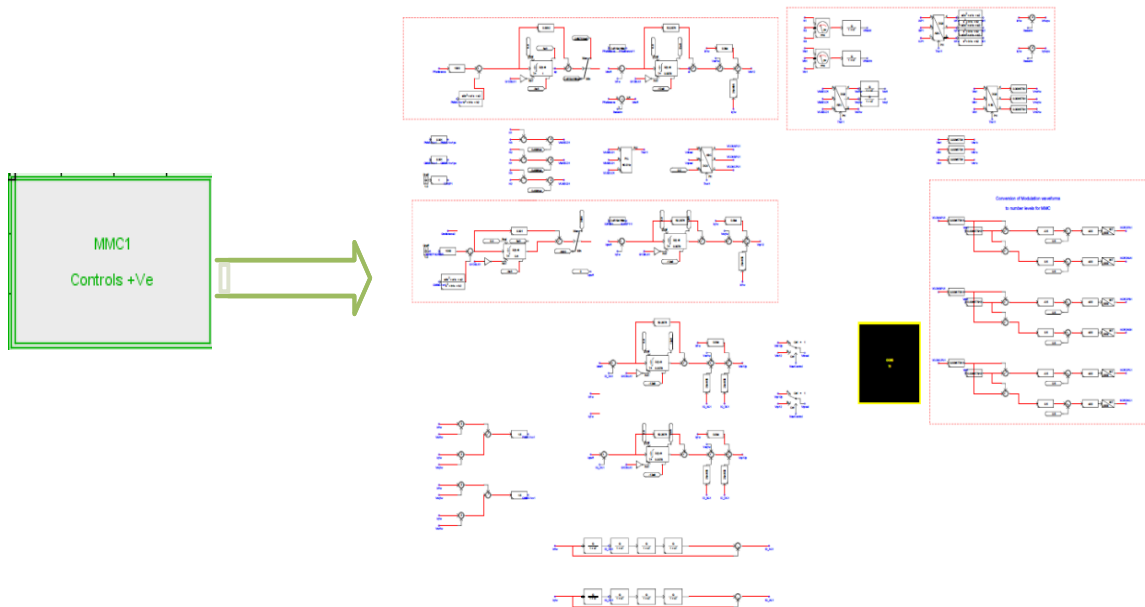➢ Then, the control scheme comes into the picture like in figure 6.6

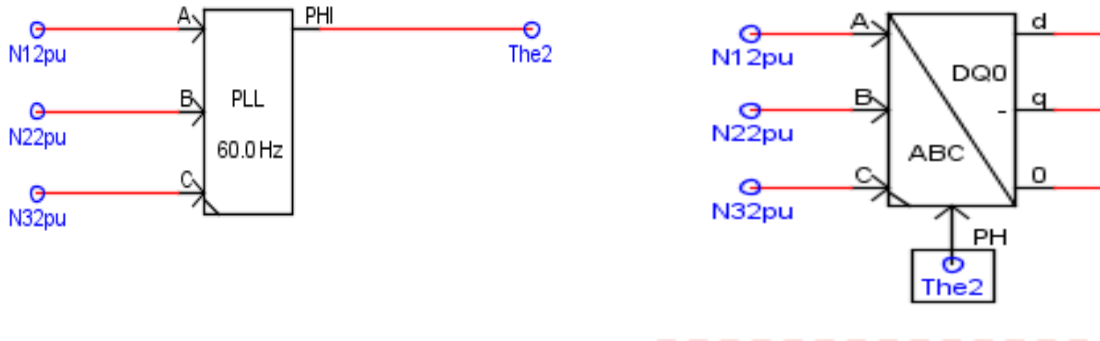Figure 6-7: General Overview of Control Circuit

Figure 6-8: Phase Lock Loop (PLL) and Park Transformation Implementation in RSCAD

The function of the PLL is to synchronize the firing pulses of the firing generator with AC system. The gain and time constant of PLL should be selected to track the changes in AC system frequency while still providing acceptable firing accuracy. Gain of PLL is made as large as possible to provide greater stability so in this MMC configuration PLL gain is 50. The PLL is a second order system, if it is given high loop gain like in this particular case, it tends to follow AC system phase with small transient error. When the PLL block is locked, the output PHI=The2 represents the phase $2\pi < PHI < 0$ of phase A input (N12pu) [24].

Three phase to DQ0 transformation is that DQ0 blocks convert a three phase rotating vector set to a stationary vector set using Park transformation [24].If The2 is fixed at 0 and inputs N12, N22 and N32 which are the bus voltages are a balanced set of positive sequence signals, the output d in figure 6.7 leads q by 90 degrees. Thus, q will be in phase with phase A voltage eq. (6.15). If q leads d by 90 degrees, then d will be in phase with phase A voltage eq. (6.16).

$$\begin{bmatrix} d \\ q \\ 0 \end{bmatrix} = \frac{2}{3} * \begin{bmatrix} \sin(The2) & \sin(The2 - 120) & \sin(The2 + 120) \\ \cos(The2) & \cos(The2 - 120) & \cos(The2 + 120) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} Va \\ Vb \\ Vc \end{bmatrix} \qquad (6.15)$$

$$\begin{bmatrix} d \\ q \\ 0 \end{bmatrix} = \frac{2}{3} * \begin{bmatrix} \cos(The2) & \cos(The2 - 120) & \cos(The2 + 120) \\ \sin(The2) & \sin(The2 - 120) & \sin(The2 + 120) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} Va \\ Vb \\ Vc \end{bmatrix} \qquad (6.16)$$

An FPGA based MMC support units, shown in figure 6.8, contain a Xilinx Virtex FPGA board (VC707) and two 8 fiber communication daughter boards from Faster Technologies (FM-S18). Additionally, there are 16 more fiber port for extra model. One VC707 FPGA board has an ability to support up to six MMC phase arms, but there are two more FPGAs are needed for the firing control for the upper and lower arms of A, B and C phases.
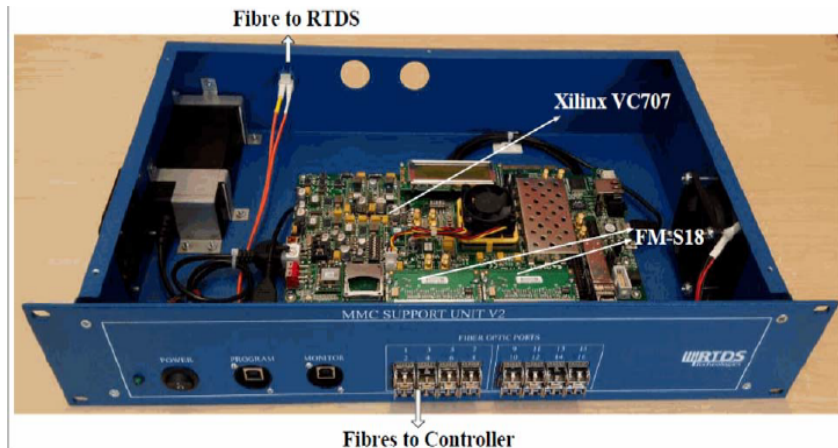

Figure 6-9: FPGA Based MMC Support Unit

6.3. Simulation Results of Point to Point MMC Based HVDC System

The Point-to-Point MMC-HVDC system, shown in Fig. 6.1 is implemented in the RTDS and FPGA based MMC support unit to investigate the dynamics and quality performance of the feedforward current control. While MMC-I controls the active power, MMC-II is responsible of DC voltage control. The AC systems and DC link are modelled and run in RTDS while three phase MMC converters and their arm voltages are emulated in FPGA and sent back to the RTDS. Fig. 6.9 shows the FPGA based MMC support unit. The MMC support unit contains a Xilinx Virtex 7 FPGA board (VC707) and two 8 fiber communication daughter boards from Faster Technologies (FM-S18). The VC707 FPGA board provides the ability to support up to six MMC phase arms. With VC707 FPGA boards, three FPGAs are necessary to model a single converter terminal. One FPGA models the six MMC phase arms while the other two FPGAs model the firing controller for the top and bottom arms of A, B and C phases. Table I lists the parameters of the MMC-HVDC system. Studies are categorized in five cases.

Case #1: Dynamic performance of t is analyzed with the feedforward controller. It can be seen in fig. 6-10 (a), the three phase grid currents, in (b) the three phase grid voltages and in (c), (d) upper and lower capacitor voltages of MMC1 and MMC2, respectively seem as expected with the feedforward current controller. Both controllers keep the DC link voltage at 1 PU.

(a)

(b)

(c)

(d)

(e)

(f)
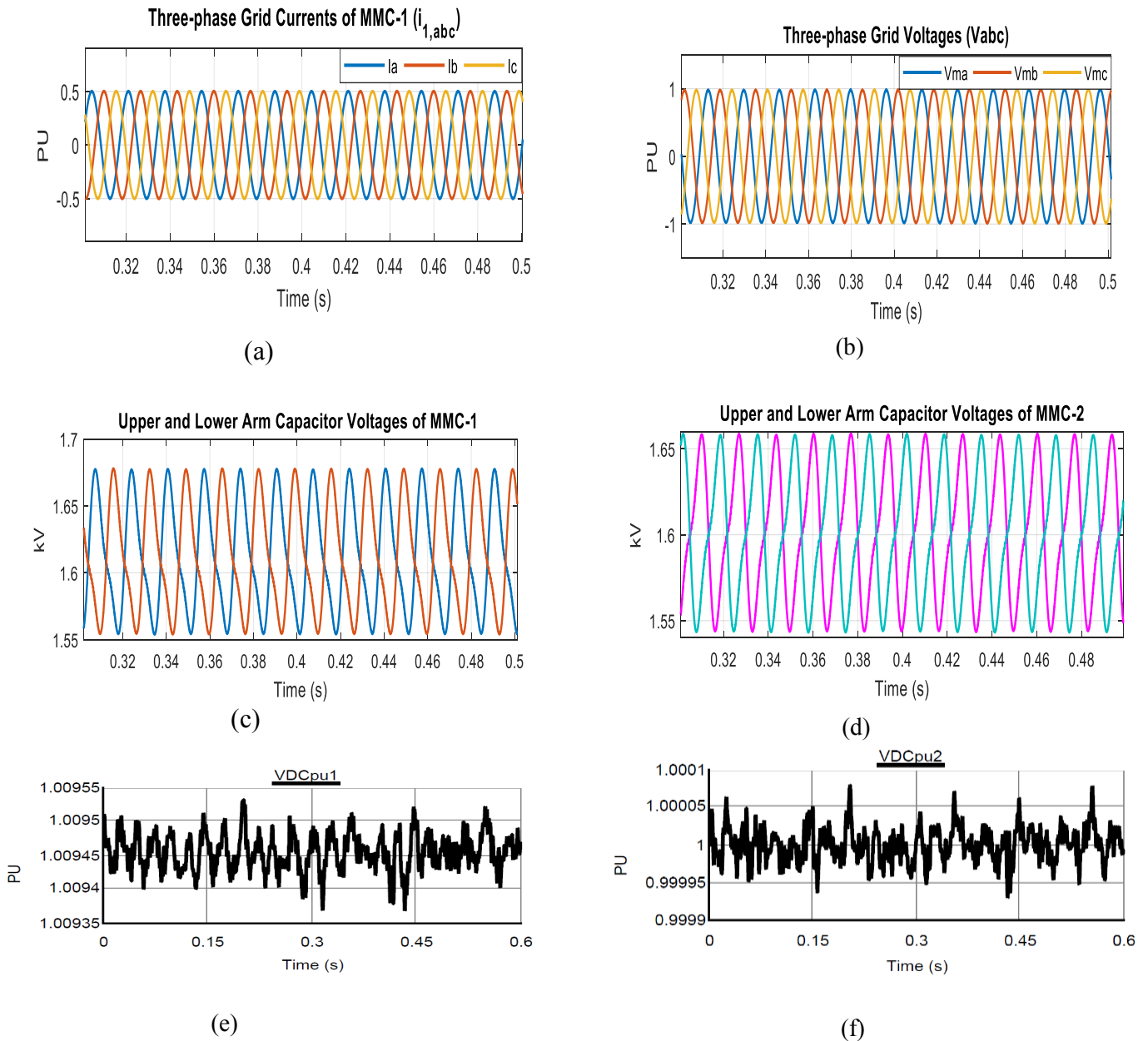
Figure 6-10: Dynamic Performance of the System under Normal Conditions

Case #2: Power reversal is tested by changing the power reference at t=0.15s from -500 MW to 500 MW using a 200 ms ramp reference. Figures show that the system can suddenly reverse the power flow direction by reversing the power set point at MMC-1. Reactive power reference remains unchanged. It reacts because of the dynamic, but it gets back to the reference value in 200ms.

Figure 6-11: Dynamic Performance in case of Power Reversal

42

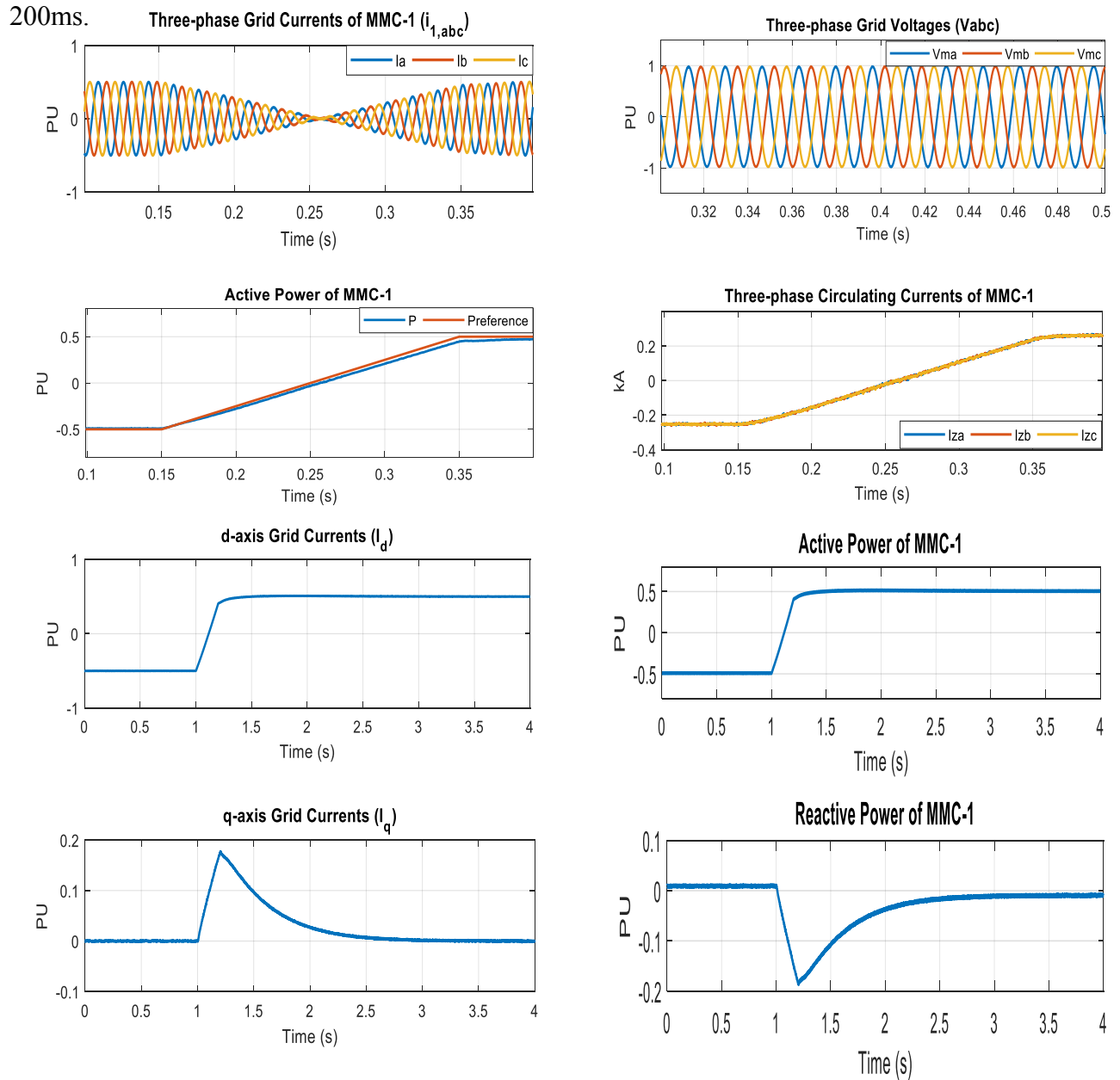Case #3: In this case, the differences between conventional and proposed controller is shown in case of balanced and unbalanced grid conditions. Power in fig. 6-12 does not track the reference as good as in fig 6-11 so the steady state error is smaller with the proposed controller. In fig. 6-12, grid currents are not quite zero at the zero crossing unlike in fig. 6-11. Although circulating current does not effect on the AC side it still has an effect on efficiency. SLG fault is applied for a second on the high voltage (HV) side of the 400/333 kV transformer of MMC-1 in fig. 6-12 with and without the proposed controller are seen, respectively. During the fault, DC overvoltage is limited to 10% by the DC voltage controller in 6-12.
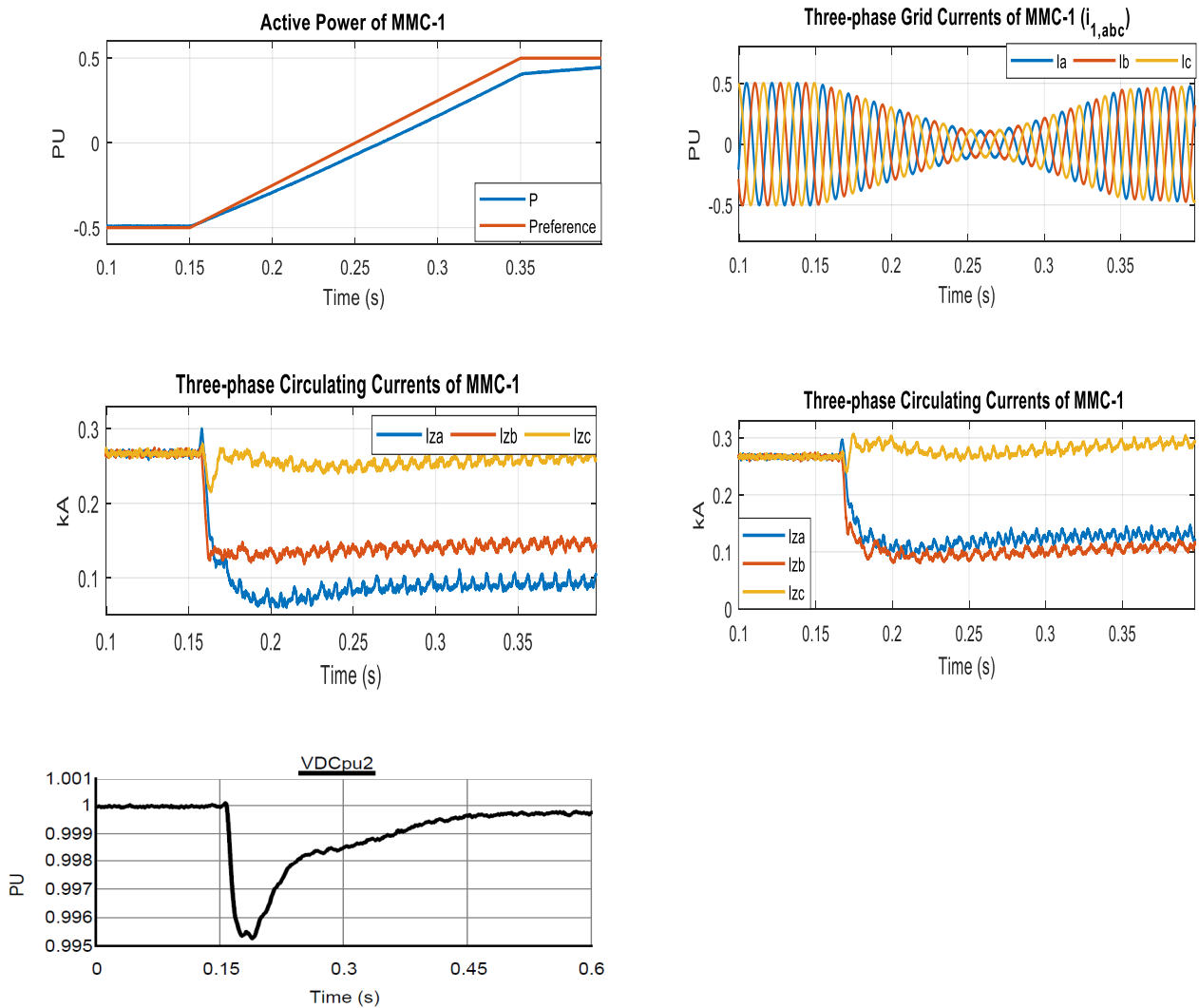

Figure 6-12: The Differences between Controllers

Case #4: Circulating current is analyzed when a SLG fault occurs at t=0.5s.

without proposed controller   *with proposed controller*
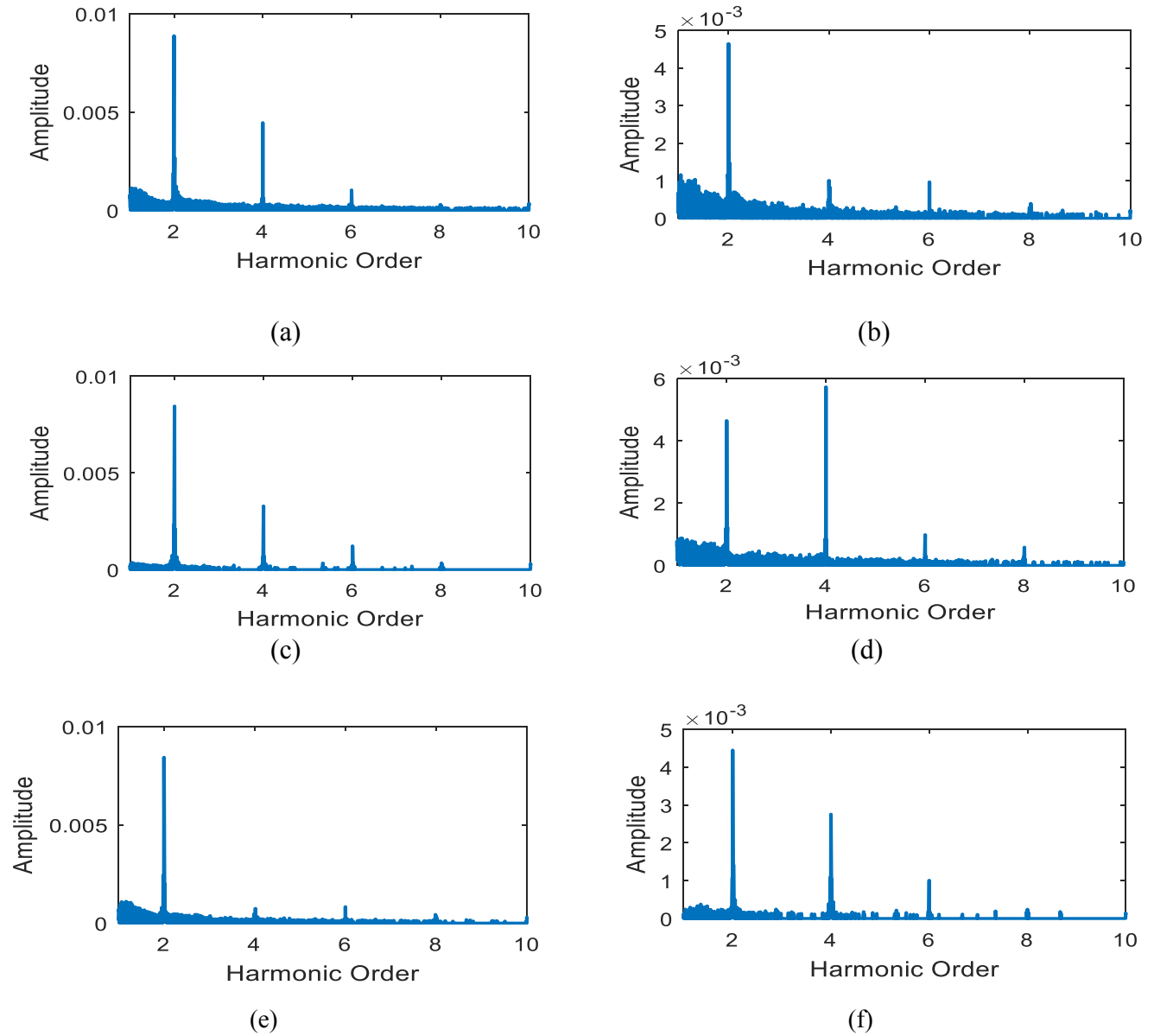

(a)

(b)

(c)

(d)

(e)

(f)

Figure 6-13: FFT Analysis of Circulating Currents

The double-fundamental frequency component is added to circulating currents. Thus, the second harmonic content is expected to be higher. Fig. 6-13 shows FFT analysis of the circulating current under SLG fault phase a, b, and c, respectively. As can be seen in fig. 6-13 (d-f), the proposed current controller helps to reduce the second harmonic content as compared to the second harmonic content results with the conventional current controller in fig. 6-13 (a-c).

Case #5: Grid current is analyzed when a SLG fault occurs at t=0.5s. Results show that the proposed current controller scheme reduces Total Harmonic Distortion (THD) in grid current. Fig. 6.14 (a) shows the dynamic performance of the three-phase grid current under SLG fault without and fig. 6.14 (b) with the proposed current control scheme. Table 6-2 shows the how the proposed current control scheme improves the THD on the secondary (Δ). Based on IEEE STD 519, 50 harmonic components are considered to calculate the THDs of the grid currents.
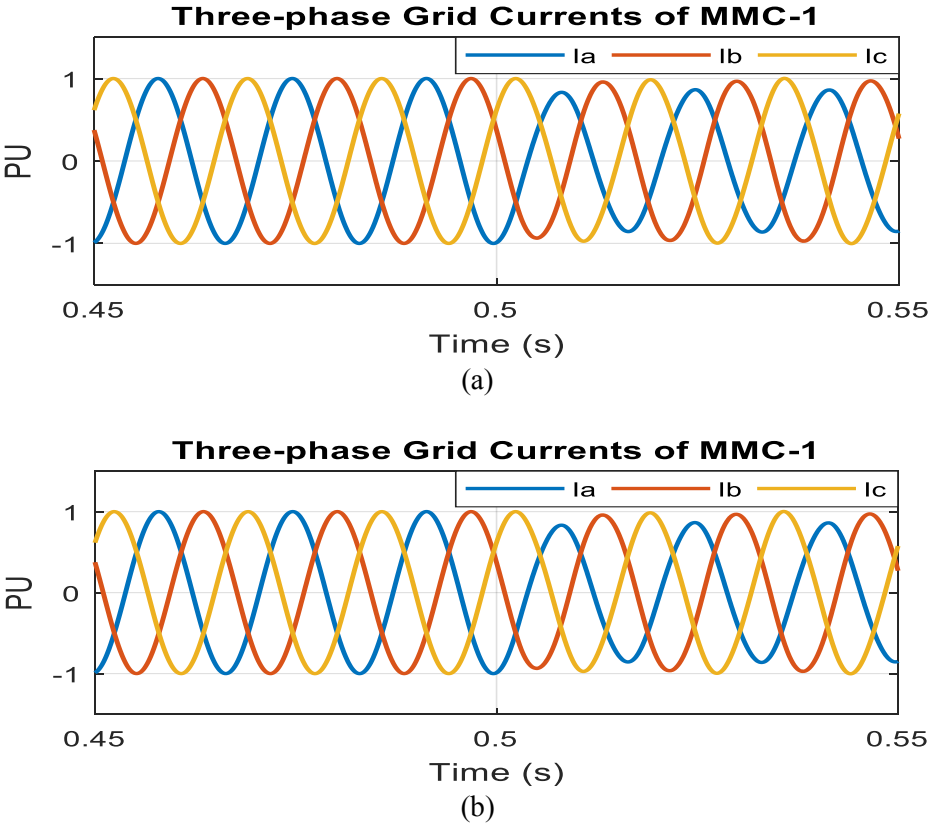

(a)

(b)

Figure 6-14: THD Analysis of Grid Currents

45

Table 6-2: Total Harmonic Distortion of the Grid Currents under SLG Fault

	THD%	
	Without feedforward Current Control Scheme	With feedforward Current Control Scheme
Phase-a (Faulty Line)	1.41%	1.1%
Phase-b	1.35%	0.45%
Phase-c	1.55%	1.36%

Case #6: For the fig. 6.15 and 6.16, both converters are employed the detailed model and DC fault capabilities of HBSM, and FBSM are evaluated. Fig. 6.15 DC short circuit occurs at where the green dotted line is located. Right after the short circuit happens; all the inserted HBSM capacitors discharge and magnitudes of DC currents and three-phase currents of the converter increase while three phase voltages of the converter decrease. In the case that gate signals of both converters are immediately blocked right after the DC short circuit happens, but DC currents still do not become zero with HBSM converter topology. Study cases are the same in fig. 6.16, but three-phase converter currents, circulating currents and DC currents suddenly start decaying and becoming zero after the short circuit if the converters are blocked. This proves that FBSM topology is capable of limiting the DC fault current without any expensive DC circuit breakers.
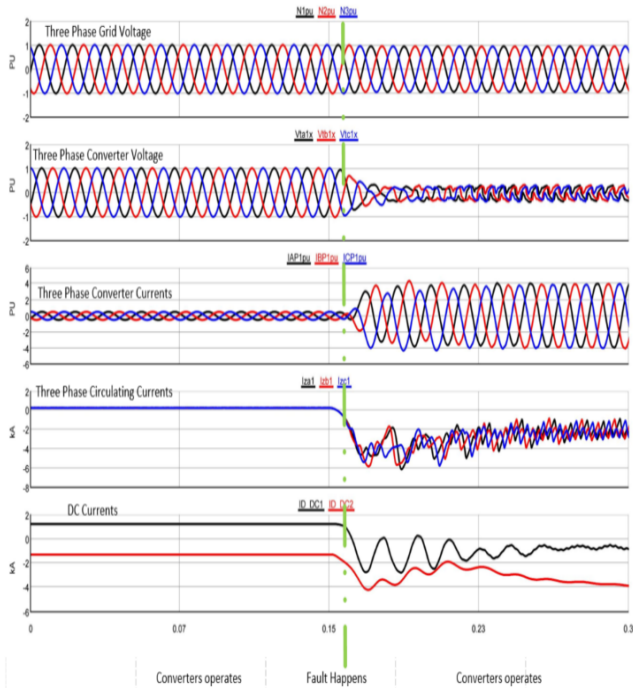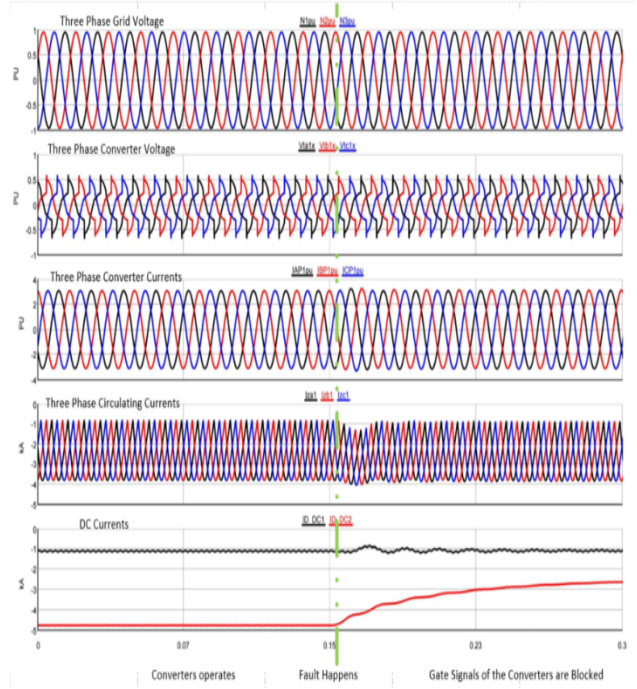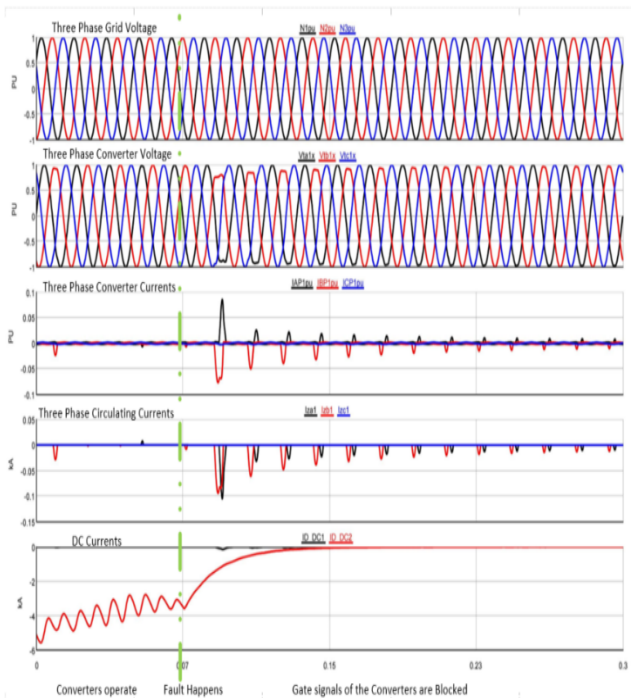
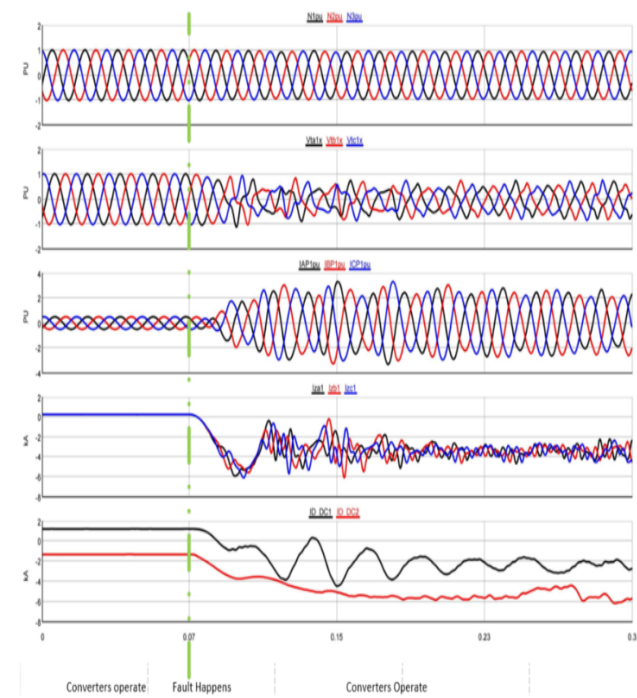Both Converters Operate   Both Converters are Blocked

Figure 6-15: System Dynamics under DC Fault with Half Bridge SM Topology

Both Converters Operate   Both Converters are Blocked

Figure 6-16: System Dynamics under DC Fault with Full Bridge SM Topology

VSC behaves as harmonic load from grid point of view if a proper control scheme is not employed. Filters cannot eliminate harmonics since the MMC is designed for high frequency. Implementing the feed-forward current control scheme allows;

- Not to concern about bandwidth and stability due to its open loop characteristics

- Less dependence on PI controllers while improvement on system dynamic

- To suppress the second harmonic in the circulating current

- No negative effect on main control objects of the system

- To decrease THD in the grid currents of the converter

Feedforward current control is a powerful method to reduce the unwanted disturbances in a control system. It is also more efficient in time-varying systems for tracking. In this thesis, feedforward current control method is presented and investigated for Point to Point MMC based HVDC system under normal and abnormal operation conditions. A feed-forward control scheme is introduced for helping to reduce the dependence on the PI controllers and improving the dynamic response of the system. The dynamic performance of MMC has been proved by the RTDS and MMC support unit based FPGAs. The proposed current control strategy is developed based on the DC and AC components of grid currents, and its results are demonstrated in five different cases. Additionally, FFT analyses of three phase circulating currents and THD analysis of grid currents are examined under SLG fault condition.

6.4. Five Level Back to Back MMC Hardware Implementation

In this chapter, ongoing back to back MMC implementation is discussed. Hardware implementation is a collaborative work with Mr. Mohammed Alharbi who is a Ph.D. student at NC State university under Dr. Subhashish Bhattacharya. The main purpose of this implementation is to transfer energy between converters. While MMC –I controls the DC voltage, MMC- II controls the active power as seen in fig 7.6.

$$V_{dc} = N_{sm} x V_c = 2 x V_c = 300V => V_c = 150V \tag{6.17}$$

The SM capacitance $C = \frac{2E_{mmc}S}{6N_{arm}V_c^2}$ where $\mathrm{E_{mmc}} = 0.5 C_{sm} v_{dc}^2$ \hfill (6.18)

Where S is the nominal capacity of the MMC, $\mathrm{E_{mmc}}$ is the energy per megavolt-ampere (MVA). $\mathrm{N_{arm}}$ is the number of SM per arm.

The capacitor rating is usually designed considering the amount of energy that the capacitor can store. The capacitor time constant is often used as a measure of the amount of capacitor energy which is defined as follows;

$$\tau = \frac{C x e_{1r}^2}{2 x P_{1r}} = 24\text{ms} \tag{6.19}$$

It is claimed that the total energy stored per rated power is typically 30-40kJ/MVA, which leads to a capacitor time constant of 40ms. In this thesis, 24ms is assumed.

To calculate the arm inductor, some approximations have to be done as follows;

$w_0 = 314 rad/s\ in\ case\ L_o < 0.2pu$ This assumption mostly valid for VSC based HVDC project [25]

$$\frac{V_{dc} x V_{2f}}{8 x w_0^2 x L_0} > 10 \frac{I_{dc} x V_{2f}}{6 x w_0} \gg \frac{I_{dc} x V_{2f}}{6 x w_0} \tag{6.20}$$

When calculating the arm inductor, double fundamental frequency AC component because of circulating current, explained in chapter 5.5, needs to be considered. Thus, capacitor voltage of an individual SM;

$$V_c(t) = V_c + \frac{V_{2f}}{2N} x sin(2w_o t + \alpha) \tag{6.21}$$

Then, double fundamental frequency becomes;

$$U_{2f} = \frac{P}{6xw_0} / (CxV_c - \frac{V_{dc}}{8xw_0{}^2 xL_0}) \tag{6.22}$$

Since the peak value of the circulating current at double fundamental frequency, explained in chapter 5.5, it is easy to calculate the first design criteria of the inductor.

$$L_{arm} = (\frac{P}{3xI_{2f}} + V_{dc}x\frac{1}{CxV_c x8w_0{}^2}) \tag{6.23}$$

One of the reasons why the arm inductor is used because of limiting the fast current rise in abnormal situations.

$$V_{dc} = L_{arm}\frac{di_u}{dt} + L_{arm}\frac{di_l}{dt} \tag{6.24}$$

To calculate the second criteria of the arm inductor, fault current rise α needs to be expressed mathematically [25].

$$\alpha = \frac{di_u}{dt} = \frac{di_l}{dt} = \frac{V_{dc}}{2L_{arm}} \tag{6.25}$$

$$L_{arm} = \frac{V_{dc}}{2\alpha} \tag{6.26}$$

Where the unit of α is kA/s and the unit of V_{dc} *is kV*.

Table 6-3: List of Parameters

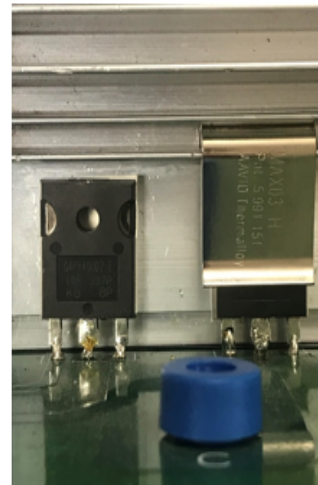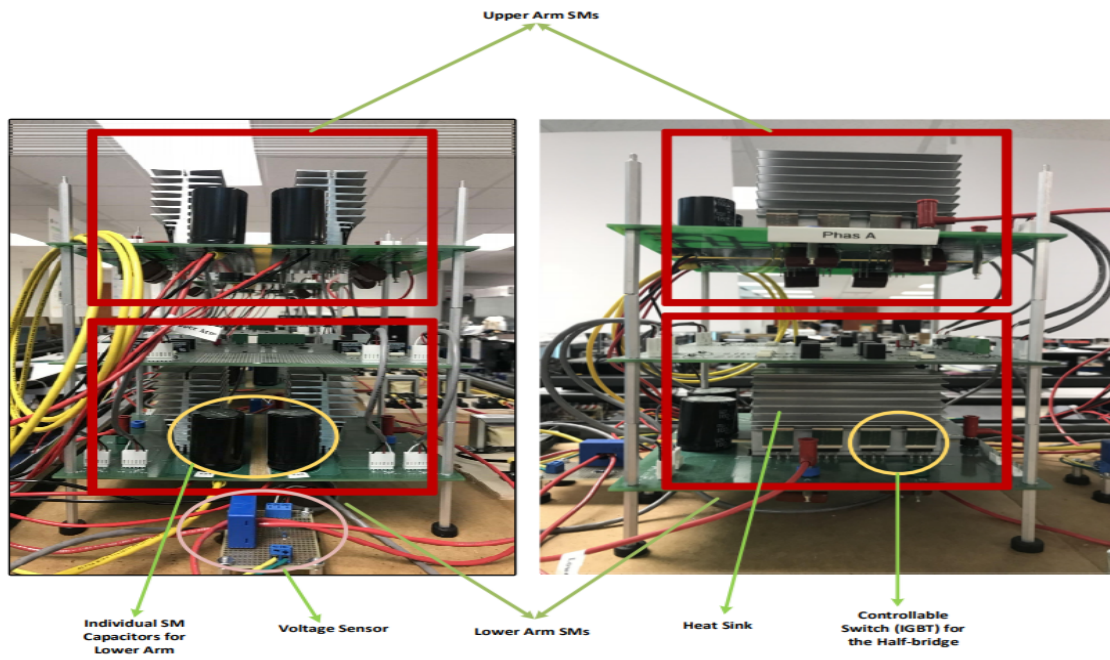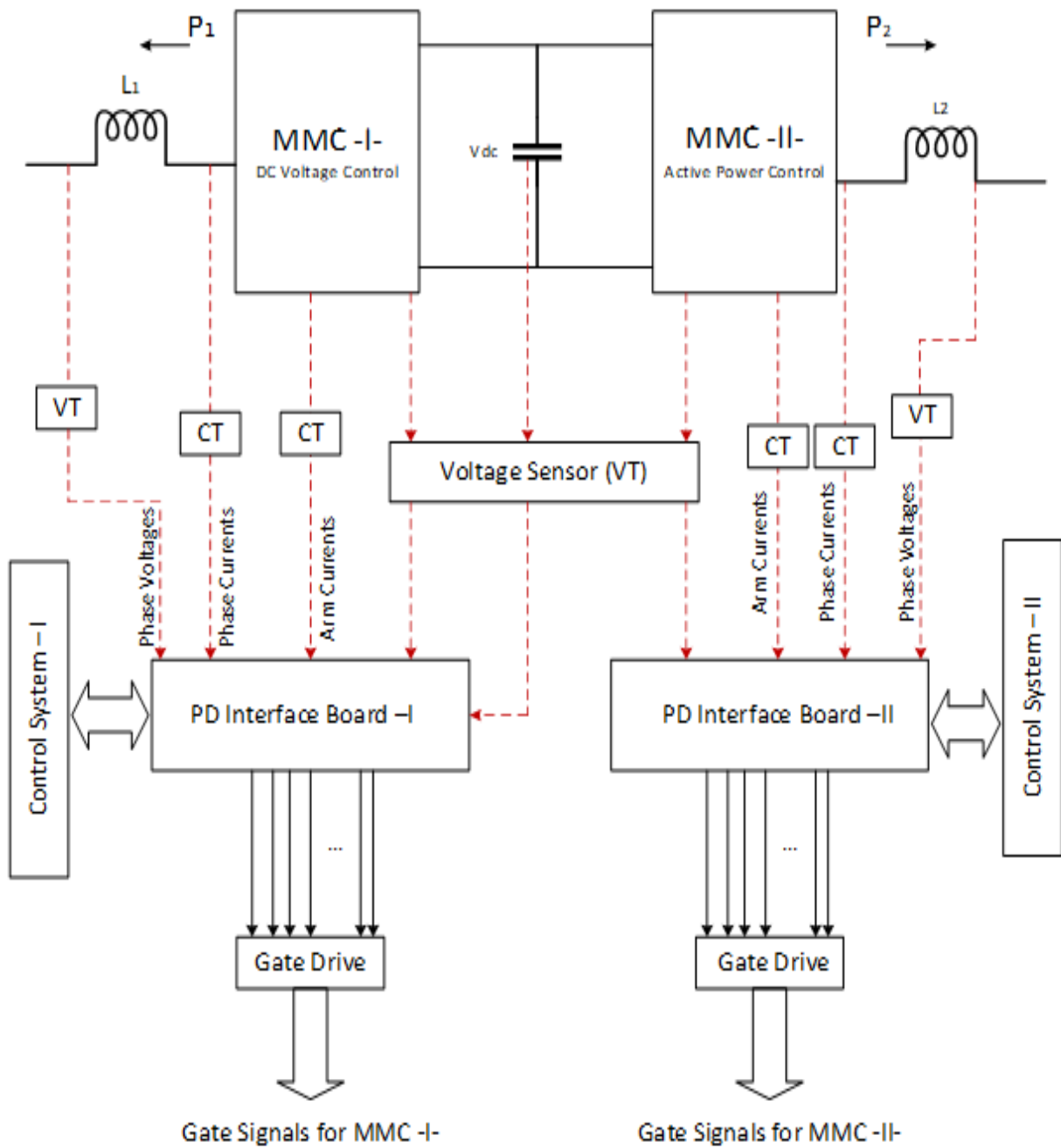|	
Rated Power (W)	2000
Rated L-L Voltage (V) and V_{peak} (V)	160 $V_{LL} = \dfrac{138kV}{\sqrt{3}} x\sqrt{2} = 130.6$
Modulation	$m = \dfrac{Voltage\ at\ the\ Low\ Side}{Vdc/2} = \dfrac{160\ x\frac{\sqrt{2}}{\sqrt{3}}}{150} = 0.87$
DC Voltage (V)	300
Rated Current (A)	$I = \dfrac{P}{\sqrt{3}xV_{LL}} = 7.21$
Rated Frequency (Hz)	60
Number of SMs per Arm (N)	2
DC Capacitor Voltage (V)	150
Carrier Frequency (Hz)	2000
Arm Inductance L_{arm} (mH)	1
AC Side Inductance L (mH)	2.5

Figure 6-17: Hardware Parts Overview

Figure 6-18: Overall Schematic of Five Back-to-Back MMC Implementation

Table 6-4: Analog Measured Parameters

Analog Inputs from the Hardware Implementation					Calculated Parameters
Grid Voltages					
Vab	Vbc				$Vca=Vbc+Vab$
Grid Currents					
Ia	Ib				$Ic=Ia+Ib$
Capacitor Voltages					
Phase A	v_{a1}	v_{a2}	v_{a3}	v_{a4}	
Phase B	v_{b1}	v_{b2}	v_{b3}	v_{b4}	
Phase C	v_{c1}	v_{c2}	v_{c3}	v_{c4}	
DC Voltage					
Vdc					
Circulating Currents					
Phase A	i_{circ-a}				$I_{ua} = 0.5x(i_{circ-a} + I_a)$
Phase B	i_{circ-b}				$I_{la} = 0.5x(i_{circ-a} - I_a)$
Phase C	i_{circ-c}				$The\ calculations\ for\ phase\ B\ and\ C$

6.4.1. Control System of the Hardware

The main controller of the system is the fault-tolerant controller for MMCs [29] with the following features;

➢ Network controlled architecture in which slave controllers are managed by the master controller.

➢ Failure in slave controller can be bypassed by adjacent slave controller.

➢ To avoid single point of failure, master controller and communication link must be redundant.

➢ Any failure in a SM will be solved by bypassing it through parallel switch.

➢ The board is seen Fig 6.23 has 13 DSP controller boards, which are distributed as 3 slave phases (four controllers for each phase) and 1 master controller

➢ The board has 3 FPGA controllers, used for fault detection and routing between different controllers. All the routing takes between the controllers takes place via FPGAs.

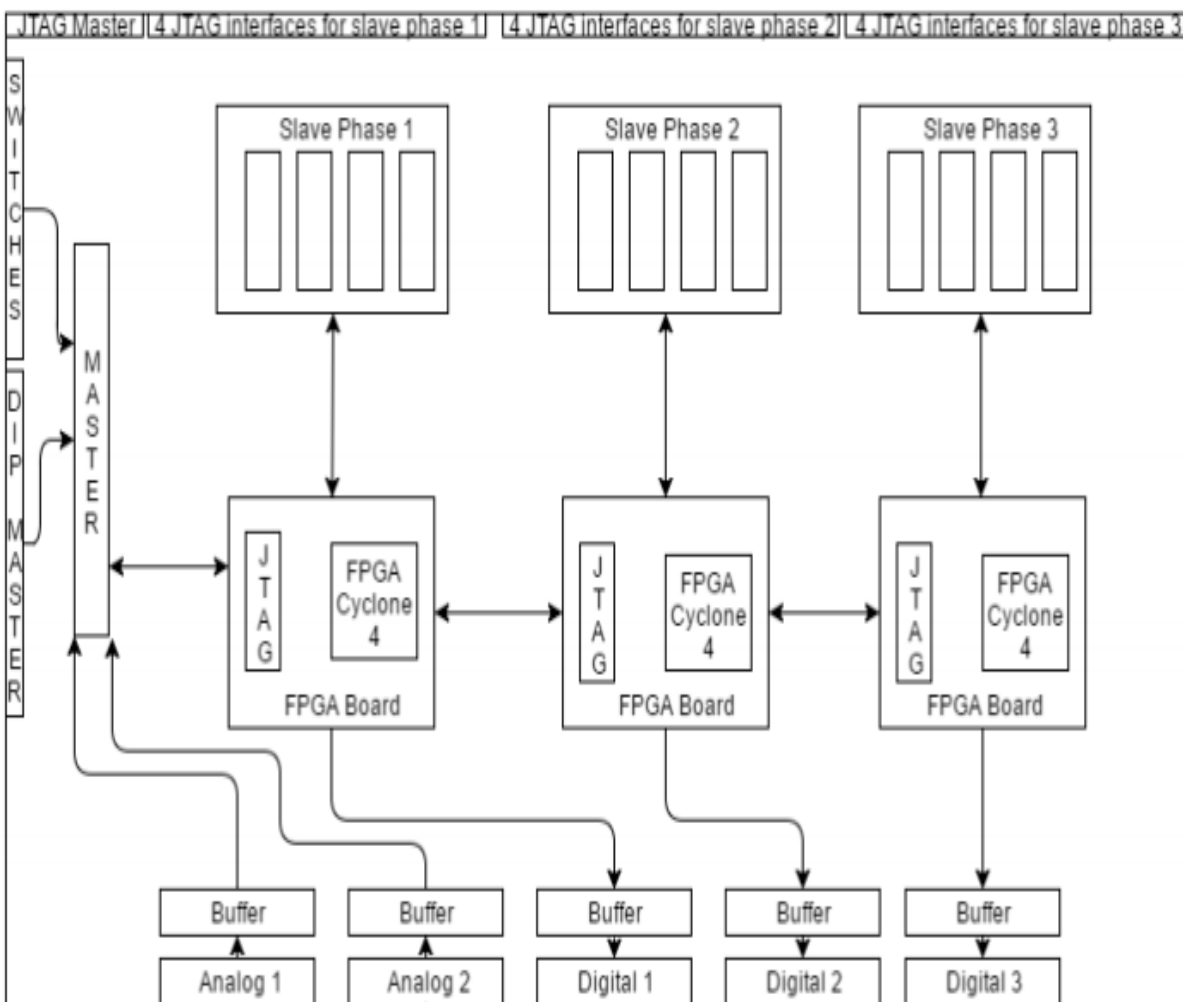➢ None of the controller is connected to the other directly.

Figure 6-19: Schematic of the Main Board
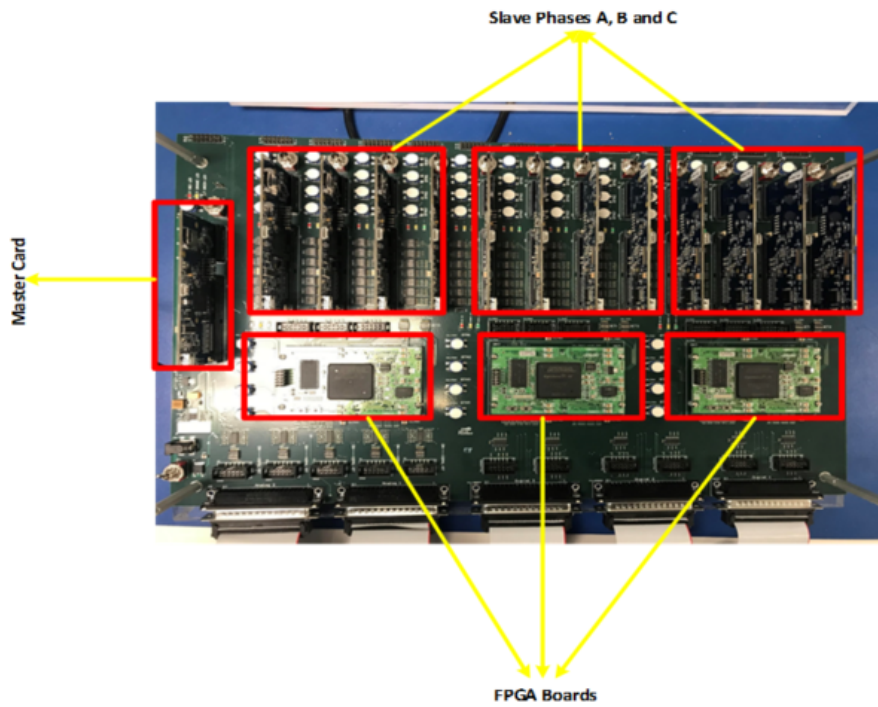
Figure 6-20: Fault Tolerant Controller Main Board

6.4.2. Main Control of the System

PLL is generated as mathematically explained in the previous chapters.

$$Theta\_b = Theta\_a - \frac{2\pi}{3}$$

$$Theta\_c = Theta\_a + \frac{2\pi}{3}$$
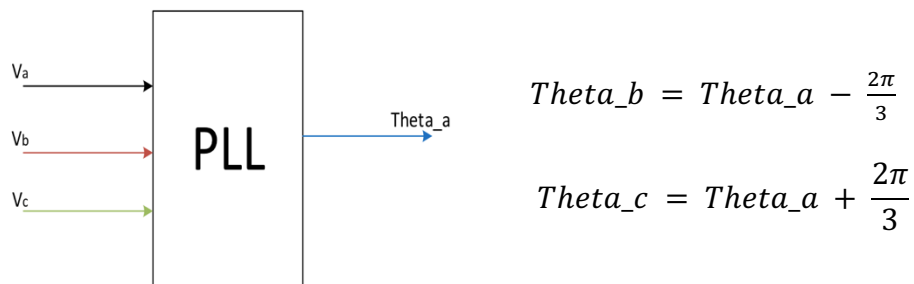
Three phase voltages and currents are transformed into *dq* reference frame.
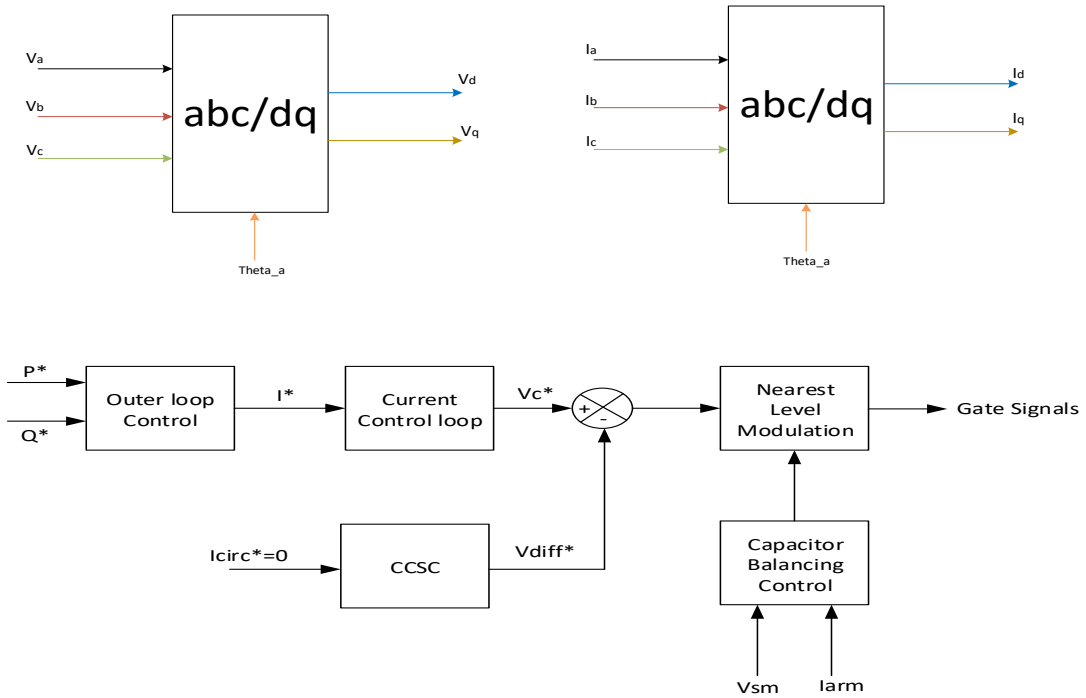

Figure 6-21: General Overview of Control Algorithm

Outer control block diagrams;
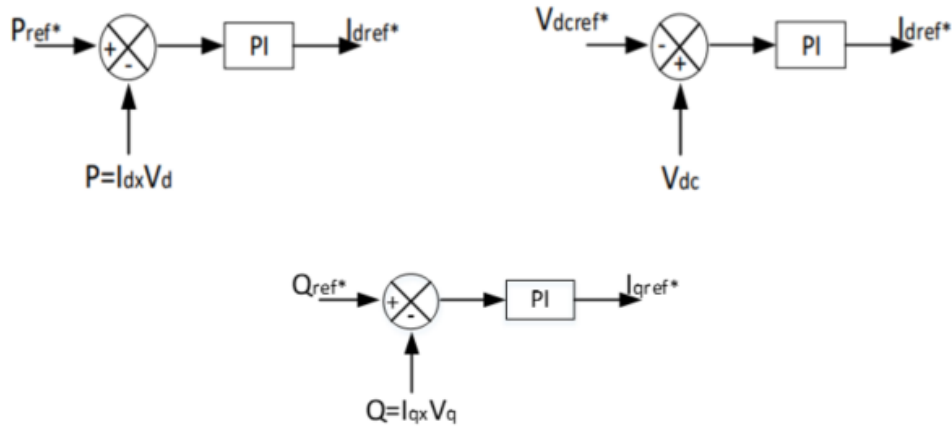
Figure 6-22: Outer Control Block Diagrams

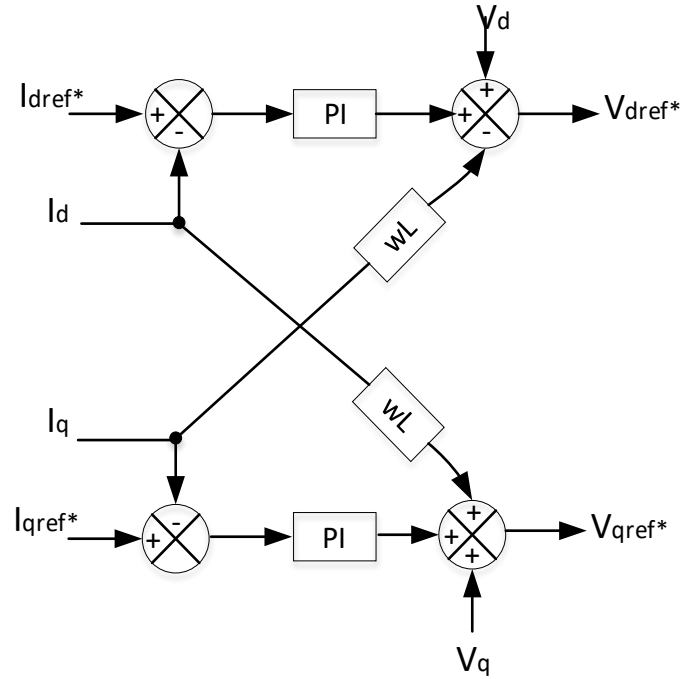Inner Current Control (ICC) block diagram;

Figure 6-23: ICC Block Diagram

$$V_{dref^*=V_d} - wL * i_q + PIx(I_{dref} - I_d) \quad\quad\quad (6.27)$$

$$V_{qref^*=V_q} + wL * i_d + PIx(I_{dref} - I_d) \quad\quad\quad (6.28)$$

$$PI = K_p + \frac{K_i}{s} \quad\quad\quad (6.29)$$

Getting the output response from the inner current control block diagram, then transform them to abc reference frame;
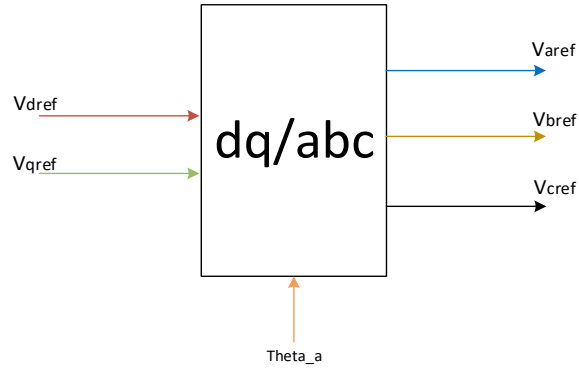
Figure 6-24: DQ0 to ABC Conversion Block Diagram

One of the most important step in the control algorithm is to control of individual SMs. To do this, averaging and balancing control methods are used [26]. The fig. 6.29 shows the circulating and averaging control for only phase A, but it is the same for phases B and C. The averaging control is used to force the average capacitor voltage of all SMs per leg to follow the reference value $\dot{V}_{c,a}$
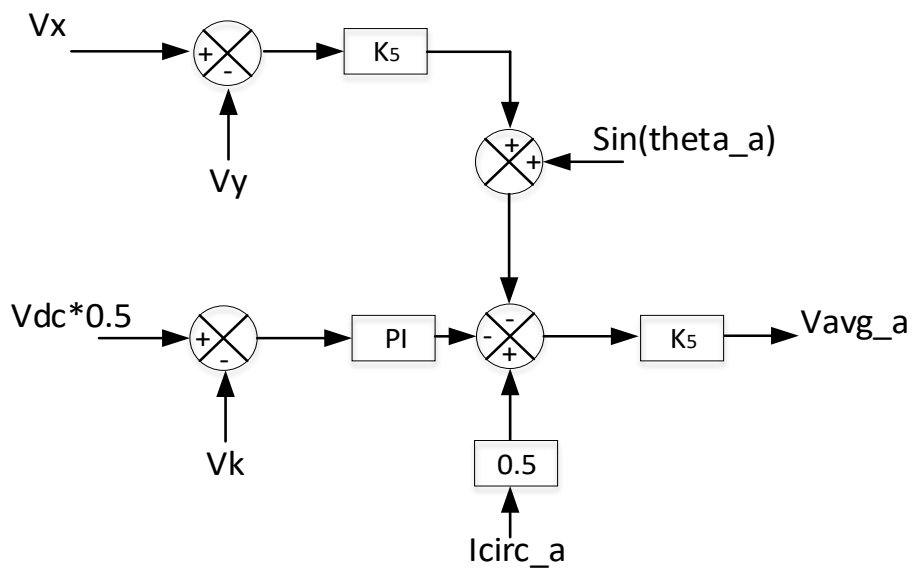
Figure 6-25: Circulating and Averaging Control for Phase A

$$V_x = \frac{V_{c1a} + V_{c2a}}{2} \tag{6.30}$$

59

$$V_y = \frac{V_{c3a}+V_{c4a}}{2} \tag{6.31}$$

$$V_k = \frac{V_{c1a}+V_{c2a}+V_{c3a}+V_{c4a}}{4} \tag{6.32}$$
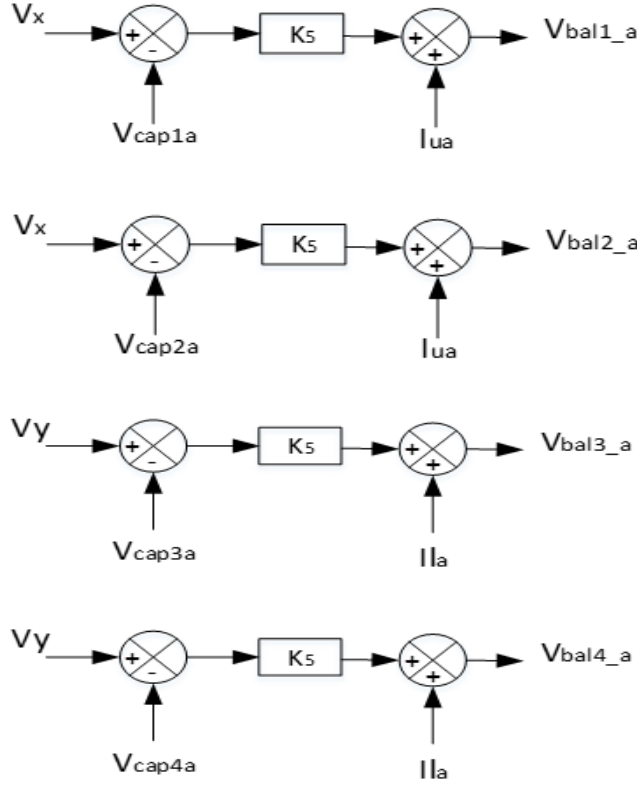
Figure 6-26: Block Diagrams for Capacitor Balancing Algorithm for Phase A

Voltage command to each SM, can be calculated as follows for phase A.

$$V_{refa1} = \frac{V_{dc}}{4} + V_{avg\_a} + V_{bal1} - {V_{aref}}/{2} \tag{6.33}$$

$$V_{refa2} = \frac{V_{dc}}{4} + V_{avg\_a} + V_{bal2} - {V_{aref}}/{2} \tag{6.34}$$

$$V_{refa3} = \frac{V_{dc}}{4} + V_{avg\_a} + V_{bal3} + {V_{aref}}/{2} \tag{6.35}$$

$$V_{refa4} = \frac{V_{dc}}{4} + V_{avg\_a} + V_{bal4} + {V_{aref}}/{2} \tag{6.36}$$

6.4.3. Simulation Results of Five Level MMC Converter

The system was tested in PSCAD/EMTC and MATLAB/Simulink.

Figure 6-27: PSCAD and Simulink Results of Back to Back System

Since the hardware system has not been fully finalized, the results are extracted in PSCAD EMT simulation tool as in fig. 6-27. The reason why PSCAD was chosen rather than RSCAD because the system does not necessarily run in real time since it has only five levels. PSCAD is more than enough if the number of SMs are low per arm.

Chapter 7   Conclusion

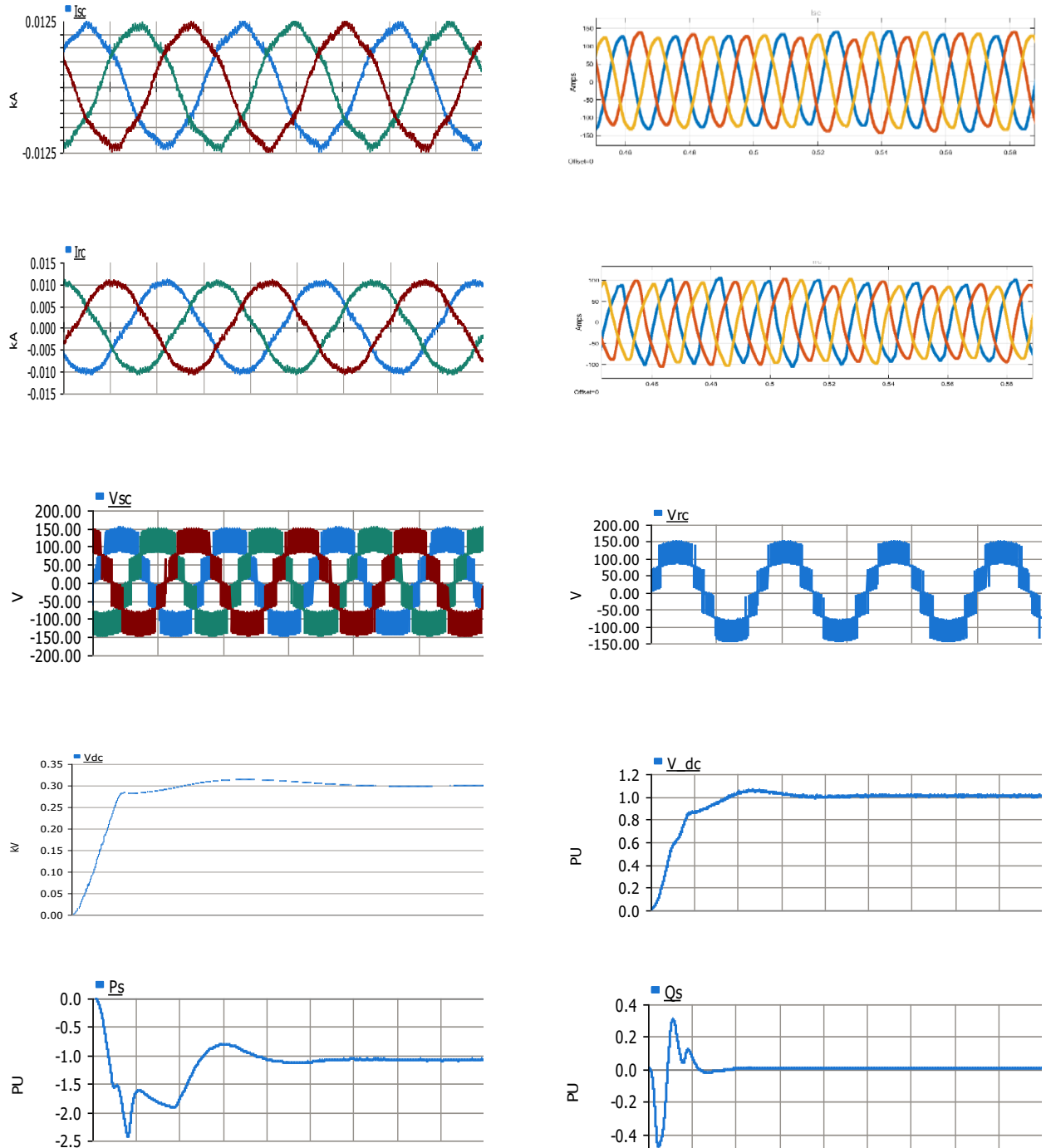Feed-forward current control is a powerful method to reduce the unwanted disturbances in a control system. It is also more efficient in time-varying systems for tracking. In this thesis, feedforward current control method is presented and investigated for Point to Point MMC based HVDC system under normal and abnormal operation conditions. VSC behaves as harmonic load from grid point of view if improper control scheme is not employed and filters cannot eliminate harmonics since the MMC is designed for high frequency.

Implementing the feed-forward current control scheme allows;

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The dynamic performance of MMC has been proved by the RTDS and MMC support unit-based FPGAs. The proposed current control strategy is developed based on the DC and AC components of grid currents, and its results are demonstrated in five different cases. Additionally, FFT analyses of three phase circulating currents and THD analysis of grid currents are examined under SLG fault condition. FBSM topology proves an advantage over HBSM in the study, it increases the cost and losses by 80%. It is a tradeoff whether employing a HBSM topology and implementing expensive DC circuit breakers or employing a FBSM with higher installation cost and higher semiconductor losses. Also, currently ongoing five level back-to-back hardware implementation is explained.

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