

ABSTRACT

RENGARAJAN, SATISH. Characterization and Analysis of 10 kV Generation-3 Silicon Carbide Power MOSFET Model. (Under the direction of Dr. Subhashish Bhattacharya.)

The semiconductor industry is primarily dominated by devices made out of Silicon (Si). However, great deal of research and recent developments in the technology of Silicon Carbide (SiC) have opened multiple doors for their use in various applications which were earlier utilizing Silicon. A quick comparison between Si and SiC would reveal superior characteristics of the SiC counterparts like higher critical electric field, thermal conductivity, operating temperature, current density etc [2]. Observing these trends, it is possible to predict that the future of the semiconductor industry would see a tremendous increase in SiC devices and progressive replacement of the existing technology as the cost drops over the years. This calls for proper modelling and analysis of SiC power devices to accurately predict their performance in power electronic converters. In this thesis, a detailed study of the 10 kV 18 A Generation-3 SiC model is performed in SABER software and compared to an existing model in the market. The module (maximum current capacity of 240 A) is manufactured by WOLFSPEED and is the latest addition to the previous generation of MOSFETs. SABER is a platform for modelling and simulating physical systems which enables full system prototyping for applications in analog/power electronics, electric power generation and mechatronics. SABER simulations are carried out to obtain results that characterize and predict the behaviour of the 10 kV device. This includes obtaining the static, dynamic, gate charge and body diode characteristics of a single MOSFET die model. In addition, the actual die of the Gen-3 MOSFET is characterized with the Power Device Analyzer/Curve Tracer B1505 of Keysight Technologies. The results obtained from the Saber model are compared with the ones from the curve tracer. The accuracy of the model can be ascertained in this process and corrections can be made to obtain a better Saber model in the future. The work presented here would include complete characterization and modeling of parasitics, development of device models, comparison of these device models and analysis of power electronic converters with these devices. Once complete characterization data of the model is obtained through SABER, the focus would be in calculating losses, transient times and modelling series connection in high voltage circuits. As the input voltage in the converter is increased close to or beyond the ratings of the module, multiple series connected models are used in such applications. Voltage sharing between the devices becomes a matter of concern due to slight differences in device parameters. The thesis also sheds some light on this issue and details the design of a balancing snubber circuit to minimize the voltage mismatch. The final chapter provides a comparative study of the switching losses in the half bridge configuration through hardware testing and Saber simulations for different values of DC input voltage and switching currents. The differences caused by parasitic ringing during the transitions can be understood in further detail.

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Characterization and Analysis of 10 kV Generation-3 Silicon Carbide Power MOSFET Model

by
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DEDICATION

We are all driven forward in our journey to happiness and success by the people who really care about us. Over the course of this journey, my family has been a pillar of great support helping me carry on past the temporary hurdles and challenges that I faced while working on this project. I was also lucky to be surrounded by bright minds over the past two years of my graduate studies at NC State University. I would like to dedicate this work to my family and those dear friends who supported me throughout the thesis work.

Amma, Appa this is for you!

BIOGRAPHY

Satish Rengarajan was born in the town of Madurai in Tamil Nadu located in South India. He grew up in Mysore and Chennai and completed his Bachelor's degree in Electrical and Electronics Engineering from National Institute of Technology, Tiruchirappalli (NIT- Trichy). After his graduation, he worked with Larsen and Toubro Power Transmission and Distribution in Doha, Qatar and was involved in substation projects of KAHRAMAA and Qatar Petroleum. Later, he joined SunEdison Energy India Pvt Limited in Chennai and started his work in the company's design engineering department. In 2016, he joined North Carolina State University to pursue his Master's in Electrical Engineering and specialized in Power Electronics. He has worked at the Future Renewable Electric Energy Delivery and Management (FREEDM) Systems Center as a graduate researcher. In 2017, he completed his internship at Johnson Controls Inc. located in New Freedom, PA in its Power Electronics and Motor Drives department.

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CHAPTER

1

INTRODUCTION

A power Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is a specially designed type of device that can handle higher levels of power compared to the lateral logic-level MOSFET. To surpass the constraints on blocking voltage capability and current ratings due to the traditional planar structure, the power MOSFET was built to be vertical [2].

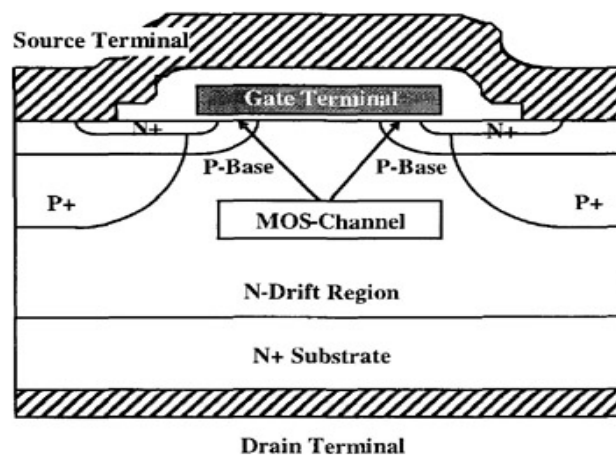


Figure 1.1 Basic Power MOSFET Structure

Consider the basic structure of a power MOSFET shown above (Figure 1.1). The presence of the lightly doped N-drift layer enables the device to block high voltages. When the device is in the blocking state, the voltage drop is supported across the P-base/N- drift junction. The ON-state resistance (R_{ON}) of a power MOSFET is obtained by the summation of the contributions due to the channel, accumulation region, JFET region, drift region and the substrate.

$$R_{ON} = R_{CH} + R_A + R_{JFET} + R_D + R_{SUBS} \quad (1.1)$$

To support a higher breakdown voltage, the thickness of the drift region must be increased in proportion. This leads us to understand that the resistance contributed by the drift region (R_D) of the device would dominate over the other regions in determining the overall R_{ON} of the device. Thanks to the development of Silicon Carbide (SiC) technology in the late 1980's, there are now ways of achieving voltage ratings of the order of tens of kV for the power devices [4]. This was mainly possible by the utilizing the extremely low value of on-state resistance offered by SiC devices for the same blocking voltage. This helped in substantially reducing the device area and made it possible to manufacture SiC devices as a compact die. With regards to the specific on-resistance of the device, it is related to the breakdown voltage by the following equation:

$$R_{ON,sp} = \frac{4BV^2}{\epsilon_s \mu_n E_c^3} \quad (1.2)$$

where, μ_n is the mobility of electrons, BV is the breakdown voltage, E_c is the critical electric field and ϵ_s is the permittivity of Si/SiC. The critical electric field of SiC is about 10 times higher than that of silicon. This becomes the most important parameter in calculating the on-state resistance as it is raised to the third power in the equation. Substituting the values, it was found that the typical value of on-resistance of SiC is about 2000 times smaller than that of Si counterparts blocking the same voltage. Thus, silicon carbide became a great choice to fabricate power devices which required high blocking voltages. The denominator of this equation is referred to as Baliga's Figure of Merit and it directly relates the properties of the semiconductor material to the resistance of the drift region.

The energy band gap of silicon carbide is about three times (3.26 eV) higher than that of silicon (1.10 eV) thus putting it in the category of wide bandgap semiconductor. Another important advantage of using SiC for manufacturing power devices is that the leakage current at a particular temperature is much lower compared to the devices made out of Silicon [2]. The intrinsic carrier concentration of 4H-SiC is only $6.11 \times 10^{-11} \text{ cm}^{-3}$ compared to $1.4 \times 10^{10} \text{ cm}^{-3}$ of Silicon at room temperature (300 K) [2]. This clearly shows that the bulk generation current is negligible in the case of silicon carbide devices.

High power, high frequency converters that are used in motor drive applications, for example, must employ power devices that are capable of blocking high voltages and also incur lower switching

losses during their operation. Higher number of switching cycles per unit time means a better sinusoidal current output to the motor which eventually leads to reduction in the total harmonic distortion (THD) of the current. This improves system performance in terms of torque per unit ampere and efficiency. Silicon Carbide devices also provide better switching characteristics and dissipate lower energy during the switching transients. This subsequently reduces the constraints related to heatsink requirements.

1.1 Motivation

As mentioned earlier, in order to fully understand a power device and deduce its suitable applications, one has to have a good understanding of its basic characterization curves. In this thesis, a single die model of the Gen-3 10 kV 240 A SiC module is first completely characterized using the **Saber software of Synopsys**. The current rating of one die model is 18 A and is designed to have an active area of 0.312 cm^2 . To achieve the full current rating, the active area in the simulation must be increased to 4.16 cm^2 . Saber is a platform for modeling and simulating physical systems, enabling full system prototyping for applications in analog/power electronics, electric power generation/conversion/distribution and mechatronics. It is highly cross-functional as it can model systems ranging from top level mechanical blocks to digital control circuits that go as a part of a big top to bottom topology. The user has the ability to view signals through multiple levels of system hierarchy which facilitates the simulations to be carried out under one platform without the need to execute sub-system blocks using different software tools.

While characterizing the model, important plots relating to the output and transfer characteristics must be obtained to get an idea about the on-state resistance and threshold voltage of the device. The variation of these parameters with temperature needs to be analysed along with the computed value of temperature coefficients. Alongside to this work, the characteristics of an actual die are obtained from the Keysight Technologies B1505 Power Device Analyzer/Curve Tracer and compared with the results from Saber. The leakage current in the die model and the associated variations between modules is an important cause for voltage imbalance during series connected operation. This also needs to be analyzed as a function of the drain-to-source voltage to get an understanding of the blocking characteristics. To understand the switching behaviour of these devices, parasitic capacitances (C_{iss} , C_{rss} , C_{oss}) needs to be extracted through small signal analysis and then plotted as a function of the drain-to-source voltage. The MOSFET die is generally packaged with an inbuilt body diode whose forward I-V curves and reverse recovery characteristics needs to be analysed. As SiC devices can potentially operate at a higher switching frequency compared to their Si counterparts, exact computation of switching losses becomes imperative to quantitatively understand the improvement in efficiency by using the SiC device over the silicon device.

Once the characterization part is complete, the model can be evaluated in terms of its accuracy

by comparing its switching losses with the experimental values obtained from Double Pulse Test (DPT). Once the model is shown to be fairly accurate, it can then be used in the simulations of various converters to identify its advantages over other Silicon devices. The obtained simulation results can serve as motivation to build a complete model of another device at a later stage. SABER Power MOSFET tool is a great feature of the software that lets the user create a complete model of the MOSFET using non-linear curve fitting algorithms. This would be the matter of discussion at a later point in this thesis.

1.2 Assumptions and introduction to SABER:

The MOSFET model that is extensively characterized in this thesis is built with MAST Hardware Description Language. In the starting phase of the thesis, it was assumed that the modeling replicates the actual behaviour of the device within a reasonable range of error. After obtaining each of characterization curves, comparison was made with the plots provided by the manufacturer and the ones obtained from curve tracer. As the model predicted the parameters well, it became clear that further analysis can be done through simulation to validate more results. The work presented in this thesis is after making careful comparison with the experimental results.

Although Saber is a powerful simulation platform, with the online tutorial package currently available for the users, it may be difficult to fully tap its analysis and computational functionality. Saber can perform the following types of analyses:

- (1) DC Operating point
- (2) Small signal AC
- (3) DC Transfer
- (4) Transient
- (5) Operating point/Transient
- (6) Pole-Zero
- (7) Parametric variation
- (8) Monte Carlo
- (9) Sensitivity
- (10) Worst-Case
- (11) Experiment (nested loops of any of the above mentioned analyses)

This work primarily utilized the transient and small signal analysis features of Saber. The signal list to be generated after the analysis can be made as exhaustive as possible going to the lowest level digital control signals in a big hierarchical model. Each model in Saber is terminated by pins in the software and the waveforms at these pins can either be "across" or "through." For electrical systems, the across variable would typically be a voltage and the through signal at the pin would

typically be the current. The truncation error in the simulation should be chosen such that the error in each iteration is low. For power electronic systems, anything in the order of $10\ \mu$ to $100\ \mu$ would provide accurate results. If the switching frequency of the converter is over 20 kHz, the transition times become smaller requiring shorter time steps. Saber calculates the required time step on its own but it is useful to declare the initial time step value to avoid convergence errors. The default settings for the truncation error type would be "dynamic" and the time resolution would be 1p. Both of these can be modified by the user based on the circuit for simulation, however, it is observed that the simulator provided best results when the time resolution is decreased to 0.01p for power converters working at high switching frequencies. It is also worth noting that the simulation time might correspondingly increase with greater precision of computation. All simulation parameters and components in Saber software like resistors, capacitors, inductors are declared only as values without their associated units. The standard units of Ω , Farad and Henry are assumed for passive elements along with seconds for the simulation times. The maximum and minimum time step overrides the default values and forces Saber to calculate multiple points even when the system converges to a solution faster. The default algorithm for transient analysis is "Newton-Raphson" but it can be modified to "Katzenelson" to judge what works best for the specific power converter simulation. Target iteration would be the typical iteration per data point and the maximum iterations fixes the limit after which Saber displays an error. The Newton Step Density is the accuracy in each iteration and directly relates to the total simulation time of the system.

Through experience it was learnt that there were no common set of simulation settings that worked for all the converters. Based on the complexity and the type of the system, the required parameters to obtain accurate results with optimum simulation time can be understood after working with the software for a while. The following subsection provides some notes on the simulation settings used in this thesis. These parameters typically work for simulations of power converters:

To do a basic Operating point/Transient Analysis:

- (1) End time - As required by the user.
- (2) Time Step- Typically from 1n to 0.01p.
- (3) Monitor Progress- 1 (This shows the percentage of the simulation completed to the user).
- (4) Plot After Analysis- Yes (or any other option).
- (5) Signal List- Can either choose required signals/get all possible signals in the circuit.
- (6) Waveforms at Pins- Across/Through/Across and Through.
- (7) Truncation Error- Typically varies between 0.05 to 10u depending on the level of accuracy required.
- (8) Truncation Error Type- "Dynamic" by default, but can be set to the other options.
- (9) Sample Point Density- Varies from 10 to 1000 depending on the calculations required per iteration.

- (10) Time Resolution- 1p is the default setting.
- (11) Max Time Step- Can be defined by the user to limit the time step between successive iterations. Setting a smaller value increases the simulation time but does not guarantee an improvement in the accuracy.
- (12) Min Time Step- Similar to the maximum time step, this parameter fixes the lowest time step between successive iterations.
- (13) Integration Order, Integration Method- The integration method can be set to either "Gear" or "Trapezoidal". The order of the integration is set as 2 by default and generally produces better convergence than the first order option. However, the user can change to either option to check the suitability for a particular simulation.
- (14) Algorithm- As mentioned in the previous paragraph, Newton-Raphson is the most common method for circuit simulations. If there are issues encountered with this, Katzenelson can be used.
- (15) Target Iterations- Saber typically tries to find a solution within this specified value but increases it till the maximum specified iterations for a solution. For power converters, target iterations can be a value around 50 and the maximum can be set to 2500.
- (16) Newton Step Density- It accounts for the accuracy in each Newtonian iteration. Higher the value, higher the simulation time.

1.3 Organization of Thesis

Chapter 1: Introduction and discussion of motivation behind doing the research detailed in this thesis work.

Chapter 2: Complete characterization of one 10 kV 18 A SiC die model in Saber. Comparison with the plots obtained from the Power Device Analyzer. Analysis and extraction of the following parameters/plots:

1. Output Characteristics (I_{DS} vs V_{DS}) and calculation of ON-state resistance.
2. Transfer Characteristics (I_{DS} vs V_{GS}) and computation of threshold voltage.
3. Gate-charge characteristics and evaluation of minimum gate driver power.
4. Discussion of Miller Effect and extraction of parasitic capacitance (C_{iss} , C_{oss} and C_{rss}).
5. Estimation of leakage current.
6. Analysis of body diode characteristics.

Chapter 3: Analysis of switching losses and comparison of delay, rise and fall times of the 10 kV device model.

Chapter 4: Series connection, voltage mismatch due to parameter variations and gate driver delay and design of passive RC snubber.

Chapter 5: Building a MOSFET model using Saber Power MOSFET tool and accuracy comparison with experimental results.

Chapter 6: Hardware validation (10 kV Gen-3 SiC MOSFET)

Chapter 7: Conclusion and future work

CHAPTER

2

CHARACTERIZATION OF 10 KV DIE MODEL

In Chapter 1, the motivation and the outline of the thesis was presented along with an introduction to Saber. This chapter analyses the static and the dynamic characteristics of the die model. Saber simulation schematics and plots are provided alongside each test circuit. To understand the accuracy of the model, similar tests are carried out with the Gen-3 10 kV die on a Power Device Analyzer.

2.1 Output Characteristics

The output characteristics of a MOSFET is plot of the drain current (I_D) vs drain-to-source voltage (V_{DS}) with the gate-to-source voltage (V_{GS}) as a parameter [10]. The graph mainly consists of three regions: cut-off, active and ohmic. In the cut-off region, the applied gate-to-source voltage is lower than the threshold voltage (V_{TH}). With the maximum applied V_{DS} maintained below its rating, the current flowing through the device would be negligible. In the ohmic region, the current in the device linearly increases with the applied drain-to-source voltage. The inverse of the slope of this part of the output characteristics represents the ON-resistance of the device. The imaginary line of separation dividing the ohmic and the active region is given by the following relationship:

$$V_{GS} - V_{TH} = V_{DS} \quad (2.1)$$

When the device is turned on ($V_{GS} > V_{TH}$) and the drain-to-source voltage is less than $V_{GS} - V_{TH}$, the device is said to be in the ohmic region. Figure 2.2 shows the ohmic region (where current is directly proportional to the voltage drop) for $V_{GS} = 15$ V. On further increasing the applied voltage (V_{DS}), the drain current does not increase steadily with the same slope but saturates at some final value. This implies that the MOSFET cannot support any more increase in current and hence presents the maximum resistance in this region. The device is now said to be in the active region of operation. The following figure shows the schematic used for simulating the output characteristics of the 10 kV SiC MOSFET model:

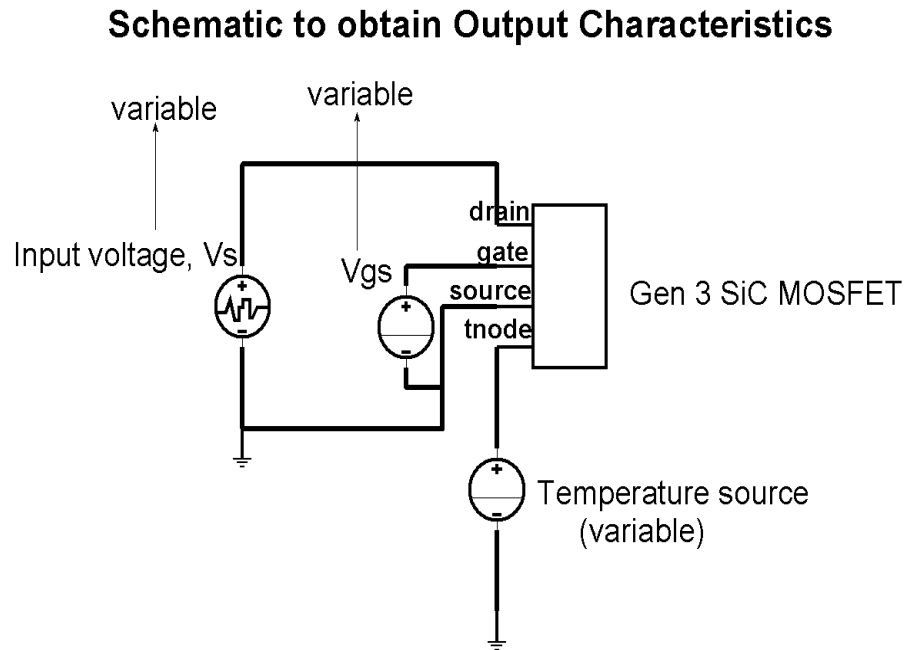


Figure 2.1 Saber simulation to obtain output characteristics

The drain-to-source voltage is increased from zero with a piece-wise linear voltage source as shown above. Once the model current reaches the saturated limit, the gate-to-source voltage is increased till 19 V. The inverse of the slope of I-V characteristics is the ON-resistance of the model during operation.

From the plot shown below (Figure 2.2), the ON-resistance at 25°C can be calculated as $\frac{1}{2.2328} = 447.86 m\Omega$ (at $V_{GS} = 15$ V and $I_D = 2$ A). The active area used to obtain this value is at of one die of the MOSFET model. The thick lines in the plot are the corresponding values of voltages and currents obtained from the Power Device Analyzer. At the same operating point ($V_{GS} = 15$ V and $I_D = 2$ A), the

actual die exhibits a slightly higher resistance of 529.057 m Ω . At higher junction temperatures, it can be expected that the ON-resistance must increase as per the general behaviour of a power MOSFET.

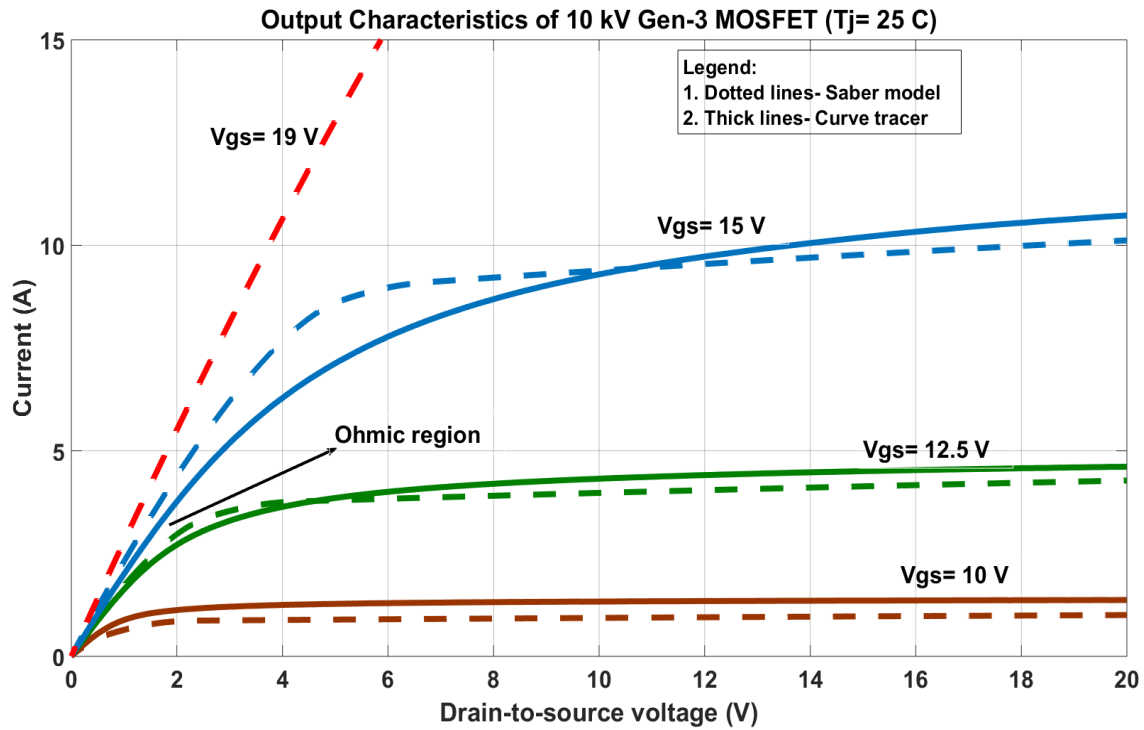


Figure 2.2 Output Characteristics when junction temperature= 25°C (Saber model vs curve tracer)

The maximum junction temperature of safe operation recommended by the manufacturer is 175°C. At this temperature, prolonged operation might damage the device and thus in this thesis comparison between the Saber model and the results from the Power Device Analyzer is only carried out at room temperature. In addition, to get accurate results, the junction temperature has to be increased and maintained at this higher temperature with a heat gun which might further introduce measurement errors due to unavoidable temperature fluctuations.

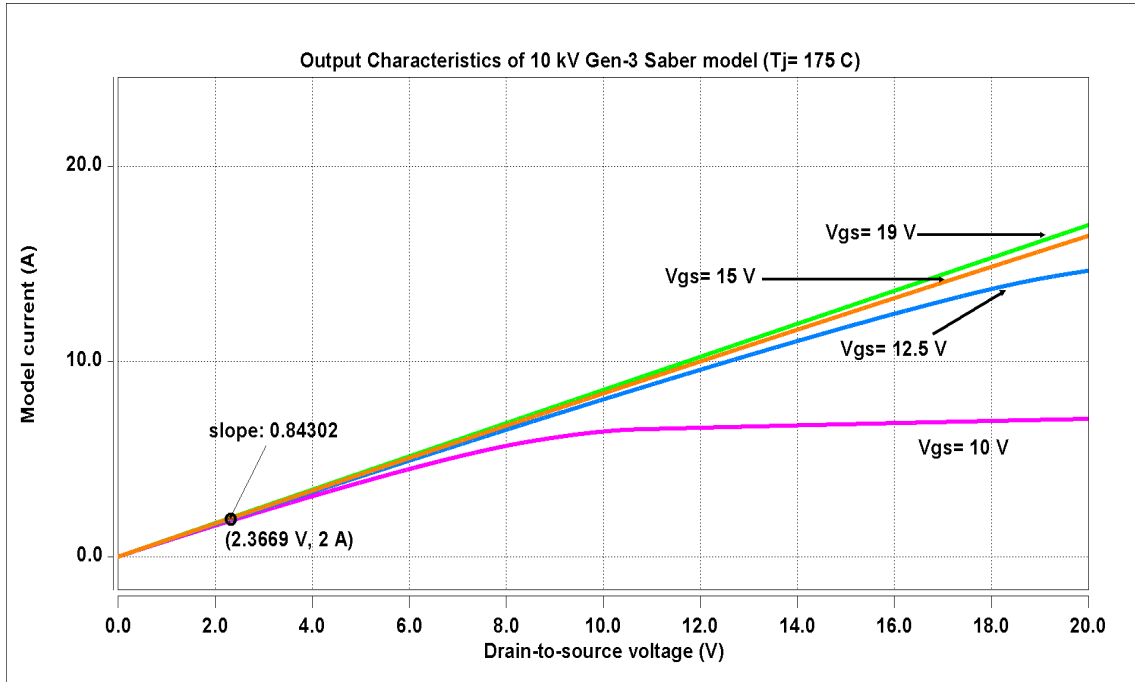


Figure 2.3 Output Characteristics when junction temperature= 175 °C (Saber model)

The Saber model is simulated at a junction temperature of 175 °C as shown above (Figure 2.3). At this temperature, the ON-resistance of the MOSFET has increased to approximately 1.186Ω at the same operating point ($V_{GS} = 15 \text{ V}$, $I_D = 2 \text{ A}$). Table 2.1 shows the values of $R_{DS,ON}$ of the Saber model as a function of temperature and this clearly exhibits a positive temperature coefficient. Figure 2.4 is a graphical plot of the same data.

Table 2.1 $R_{DS,ON}$ vs temperature (calculated at $V_{GS}=15$ V and $I_D=2$ A)- Saber model

S.No	Junction temperature °C	$R_{DS,ON}$ (m Ω)
1	25	447.86
2	50	511.63
3	75	615.006
4	100	740.79
5	125	880.049
6	150	1029.081
7	175	1186
8	200	1351.041

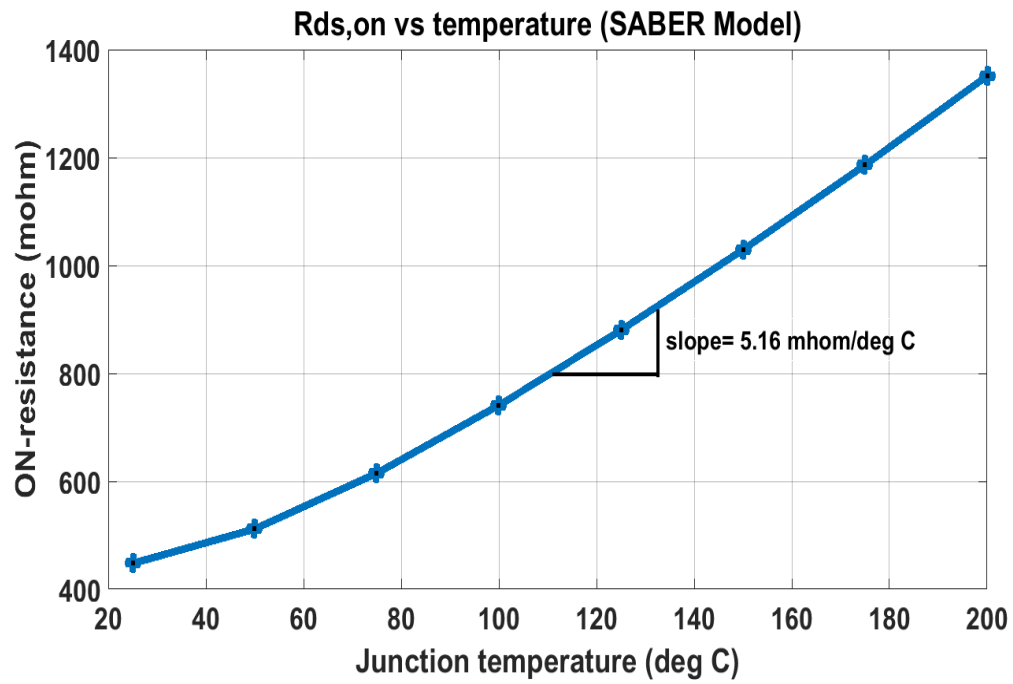


Figure 2.4 ON- resistance ($R_{DS,ON}$) of Gen-3 SiC MOSFET Saber model vs temperature

It is important to fully characterize the on-state resistance under different temperatures as the conduction losses incurred in power converters directly depend on these values. In situations where a particular value of efficiency must be achieved, the designer can get to know the requirements on the heatsinks to be used for the devices. Sometimes to overcome the limitations caused due to higher on-resistance, multiple devices are connected in parallel [34]. With these SiC devices providing a great reduction in R_{ON} , paralleling of multiple devices can be avoided which lowers the parts count and the assembly cost.

2.2 Transfer Characteristics

This plot shows the relationship between drain current (I_D) and gate-to-source voltage (V_{GS}) with the drain-to-source voltage (V_{DS}) taken as the parameter. This is one of the important plots to be obtained for any device, as it helps the engineer identify the threshold voltage (V_{th}) needed to get the device from the OFF state to the conduction state. This characteristic point on the graph is highly sensitive to temperature, generally following a decreasing trend as temperature increases. Thus, one would end up with a negative temperature coefficient when computing the values.

The schematic used for simulation in Saber is same as the one used to obtain the output characteristics. Instead of varying the drain-to-source voltage (V_{DS}) to obtain changes in current (I_D), V_{GS} is varied for a given value of V_{DS} . Three different curves are obtained for $V_{DS} = 5, 10, 15$ V. The plot obtained when junction temperature $T_j = 25^\circ\text{C}$ is shown below (see Figure 2.5). From Figure 2.5, it can be observed that the threshold voltage for the model is 5.85 V when the junction temperature is maintained at 25°C . In this work, V_{th} is defined as the value of gate-to-source voltage that makes a current of 1 mA flow through the channel of one die model when the applied drain-to-source voltage is 10 V. Generally, the temperature at the junction is much higher than 25°C due to the heat generated by switching and conduction losses in the MOSFET. Thus, in practical converter application, the device would be switched on at a voltage lower than 5.85 V. The plot obtained from curve tracer/power device analyzer is shown in Figure 2.6 and it can be seen that the threshold voltage is only 4.2 V. Thus, the threshold voltage in the Saber model is not very accurate and varies quite a lot at the defined operating point. The modelling at very low values of channel current does not accurately predict the actual behaviour of the device.

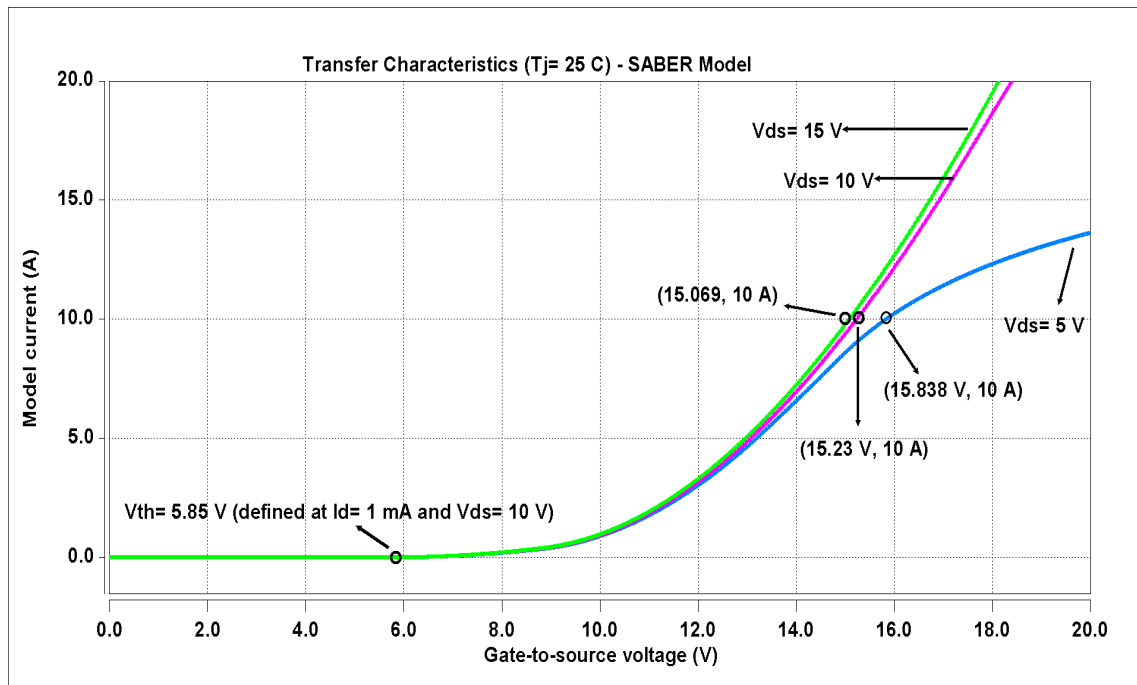


Figure 2.5 Transfer Characteristics when $T_j = 25^\circ\text{C}$ - from Saber model

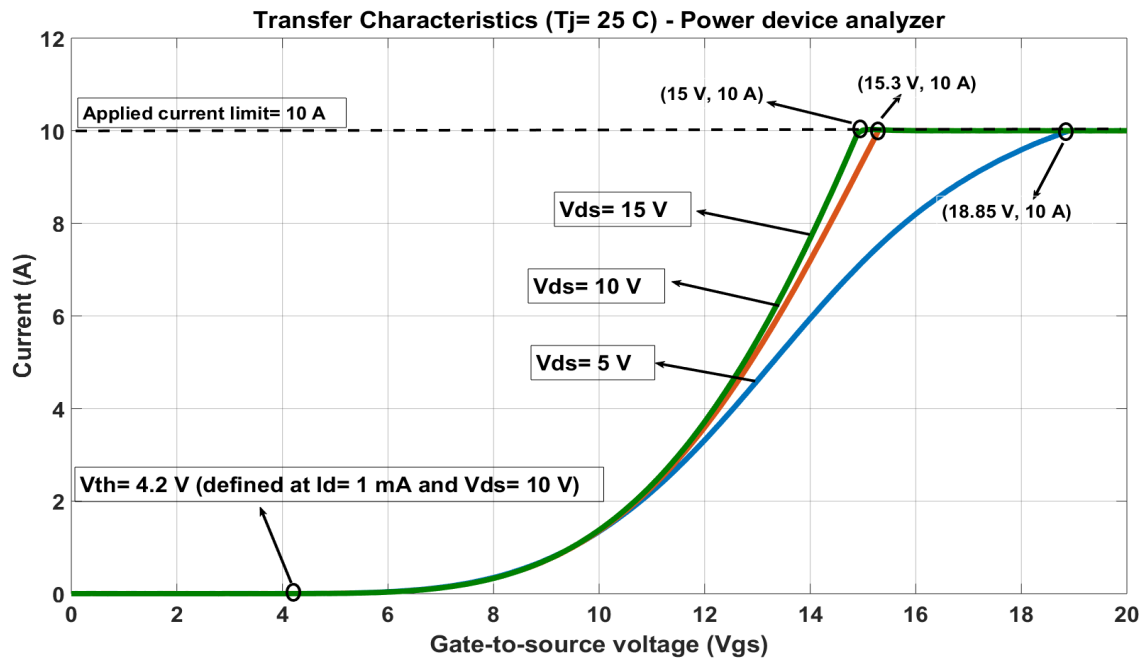


Figure 2.6 Transfer Characteristics when $T_j = 25^\circ\text{C}$ - From power device analyzer/curve tracer

On the other hand, the plots look similar for higher values of die current. The gate-to-source voltage that causes a current of 10 A in the channel is 15 V in both graphs when V_{DS} is 15 V. Similarly, annotations are made on the plots to easily check the resemblance of the Saber model with the actual characteristics. The model would have to be improved to predict the threshold voltage better. In the end of the thesis, comments on the accuracy and the shortcomings of the Saber model would be tabulated in detail. It is to be noted that the current in the actual die is limited to 10 A using the compliance factor in the power device analyzer to prevent going beyond its current rating. If needed, additional points can be extrapolated from the provided plots. The Saber model is simulated at a higher junction temperature to find the reduction in the threshold voltage.

When the graph is plotted again at $T_j = 175^\circ\text{C}$ (refer Figure 2.7), it is observed that the model current saturates and reaches the maximum at a value of gate-to-source voltage lower than that observed at 25°C . Also, the threshold voltage of the power device has decreased to 3.21 V. Simulations are carried out in Saber at multiple junction temperatures to quantitatively understand the variation of threshold voltage (V_{th}) with respect to temperature. Figure 2.8 shows that the threshold voltage decreases almost linearly as a function of temperature. Over this range, the value of the temperature coefficient is calculated to be $-17.55 \text{ mV}/^\circ\text{C}$. Practically it can be expected that the Gen-3 MOSFET would exhibit a threshold value of 3 to 4 V when used in power converters taking the typical junction temperature in consideration.

Now that the Output and Transfer curves of the Gen-3 die model are obtained and compared with the actual characteristics from the curve tracer, we can shift gears into exploring the switching behaviour of the device. The next section details the method in finding the gate charge characteristics and each of the parasitic capacitance of the Saber model.

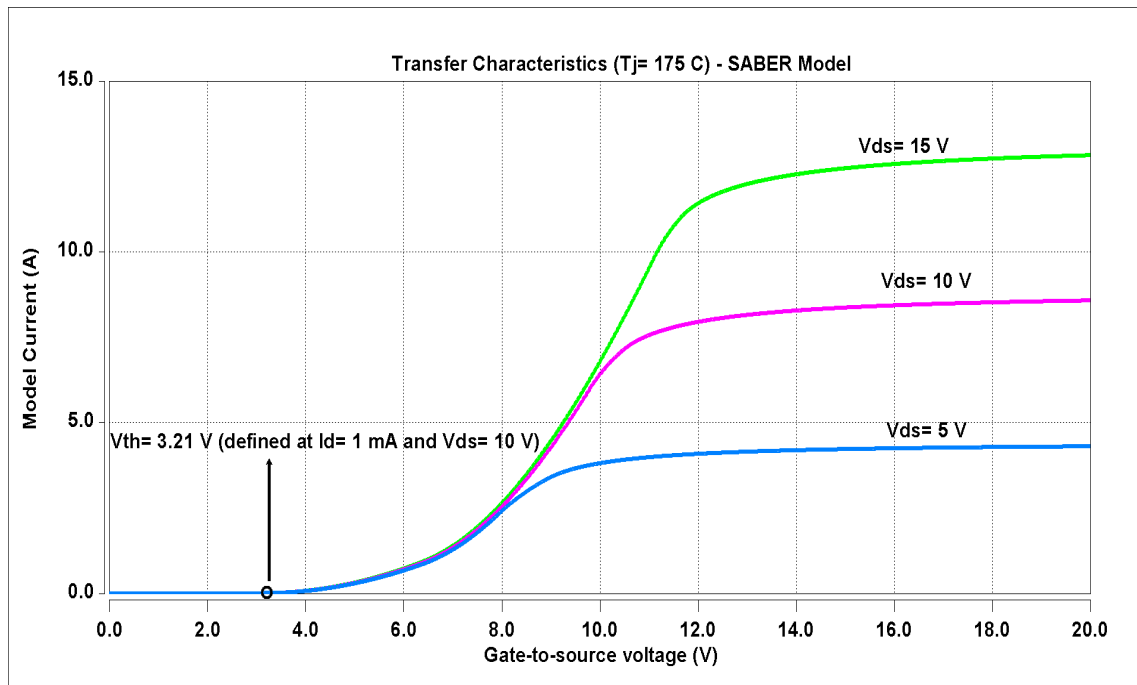


Figure 2.7 Transfer Characteristics when $T_j = 175^\circ\text{C}$ (Saber model)

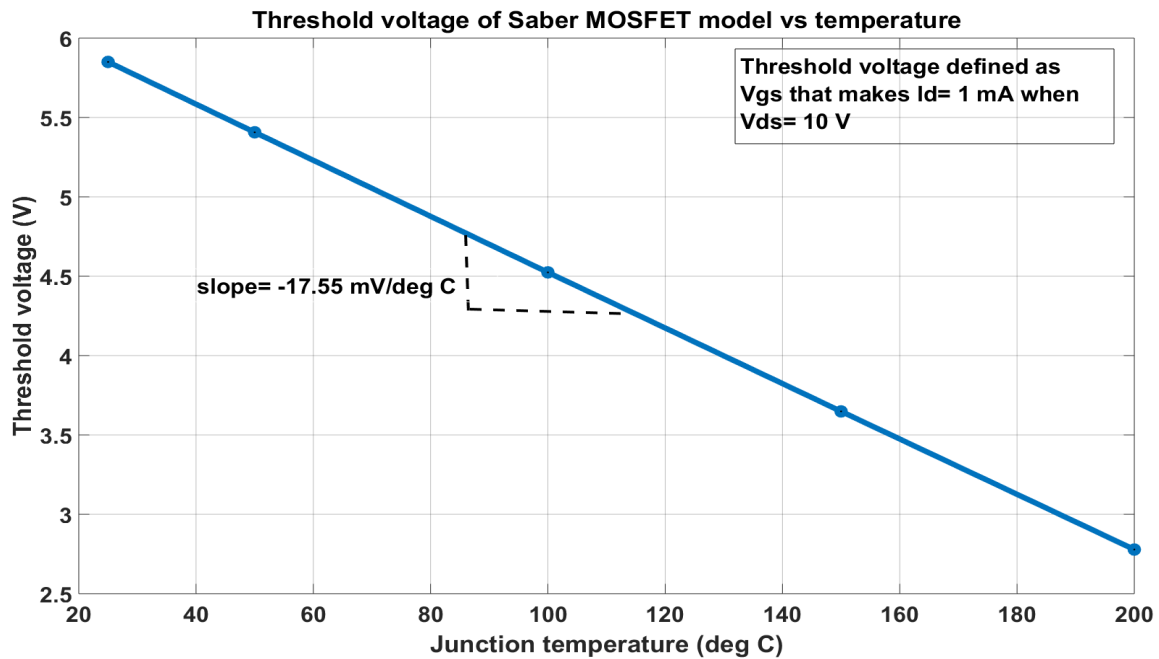


Figure 2.8 Variation of Threshold voltage (V_{th}) with respect to temperature

2.3 Gate Charge Characteristics

The gate charge characteristic is very important in starting to analyze the switching behaviour of a MOSFET. The parasitic capacitances (C_{iss} , C_{oss} and C_{rss}) can be used to predict a much more accurate version of the switching performance but due to the highly non-linear nature of the curves, the gate charge plot provides a simpler understanding of the turn-on/turn-off mechanisms [26]. One thing to note while using these plots is that they vary according to the test condition. For example, when the drain-to-source voltage is increased, the position of the Miller plateau voltage can slightly alter and the total value of gate charge (Q_G) at $V_{GS,max}$ can increase. This is because the reverse transfer capacitance (C_{rss}) is function of the applied drain-to-source voltage and the value of charge obtained by integrating the C-V curve between the switching conditions change with V_{DS} . Conversely, the total value of Q_G would reduce when the applied drain-to-source voltage is reduced. Generally, the gate charge characteristic does not vary much with the device current and stays constant from the threshold value to the rated value. To obtain this characteristic, a simple test circuit of the SiC MOSFET model driving a resistive load would suffice. Apart from predicting the switching behaviour, the gate charge curve can provide an understanding of the gate driver requirements of the device under test (DUT). The amount of charge required for the total input equivalent capacitance (C_{eq}) must be delivered by the driver during turn-on. The same amount of charge needs to be withdrawn from the capacitances to completely turn-off the device. The driver's ability to do both of these actions per unit time determines its minimum power rating for satisfactory performance. The gate drive power can be computed by the following relationship:

$$P_{drv} = Q_{gate} \times freq \times \Delta V_{Gate} \quad (2.2)$$

where,

Q_{gate} is the total charge required for the turn-on process

$freq$ is the switching frequency of the gate driver and

ΔV_{Gate} is the gate driver voltage swing

For the simulation in Saber, the gate charge was computed as a time integral of the gate current (output current of the gate driver) and plotted as a function of the gate to source voltage (V_{Gate}). Even though a constant gate current can be used to simplify the analysis, this work computes the time integral with the corresponding instantaneous values obtained from Saber (see equation 2.3). By following this procedure, it was observed that the total charge fairly remained constant for different values of drain current (I_D).

$$Q_{gate} = \int_0^{t_{ON}} I_{gate} dt \quad (2.3)$$

As shown in equation 2.3, the integration is carried out from the time of switching ON the driver (assumed to be $t=0$) until the time required to deliver the charge to the MOSFET model for complete turn-on. The time elapsed is called the turn-on time (t_{ON}). The maximum gate drive current is computed by dividing the highest gate drive voltage swing and the lowest gate resistance that can be used for the power MOSFET.

$$I_{drv,max} = \frac{\Delta V_{Gate}}{R_{Gate,min}} \quad (2.4)$$

In practical situations, the gate circuit includes some inductance in the loop and the maximum current rise is also limited by this parasitic inductance. The equivalent can be represented as a series RLC circuit by considering the device capacitance as C_{eq} during turn-on. The solution considering non-oscillating gate current yields that the maximum current of the gate driver is 0.7 times the value calculated from equation 2.4 [14]. All of these results can now be utilized in calculating the driver power required for the Gen-3 device model.

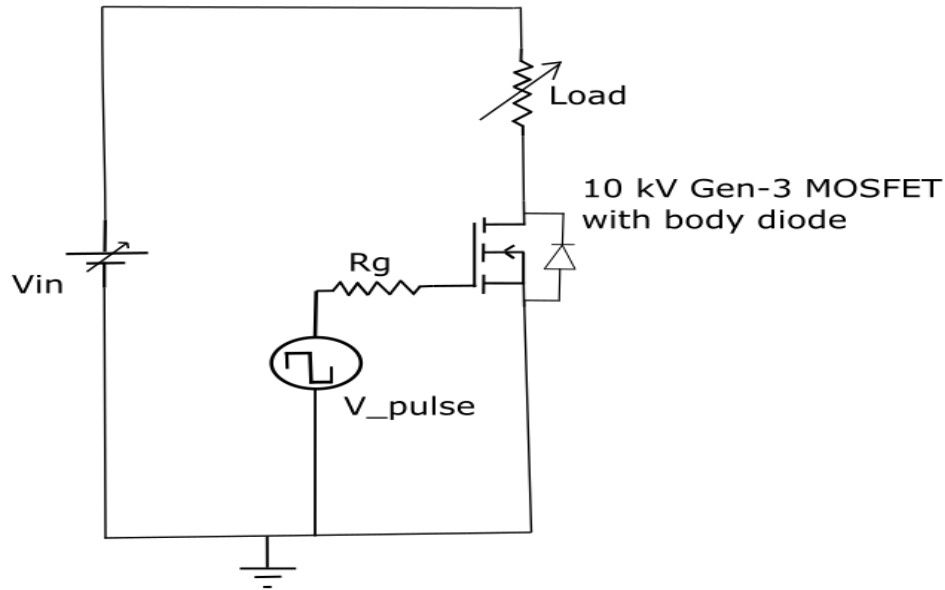


Figure 2.9 Simulation Schematic to obtain gate charge characteristics

The schematic (Figure 2.9) shown for the simulation uses the 10 kV Gen-3 device driving a resistor. The value of V_{in} decides the drain-to-source voltage swept between the ON and the OFF states. The value of R_G is 20 Ω in the simulation. The drain current is arbitrarily chosen to be 10

A. The charge flowing through the gate terminal of the MOSFET is obtained by integrating the current during the turn-on transition. From the plot (Figure 2.10), it is evident that the gate voltage increases steadily until it reaches the Miller plateau at about $V_{gp} = 11.1$ V. At this point, the gate current gets diverted into the Miller capacitance (C_{gd}) and the incoming charge is used to charge this capacitance. Crossing the Miller plateau, the gate-to-source voltage increases again until the total gate charge is sufficient enough to fully turn on the device.

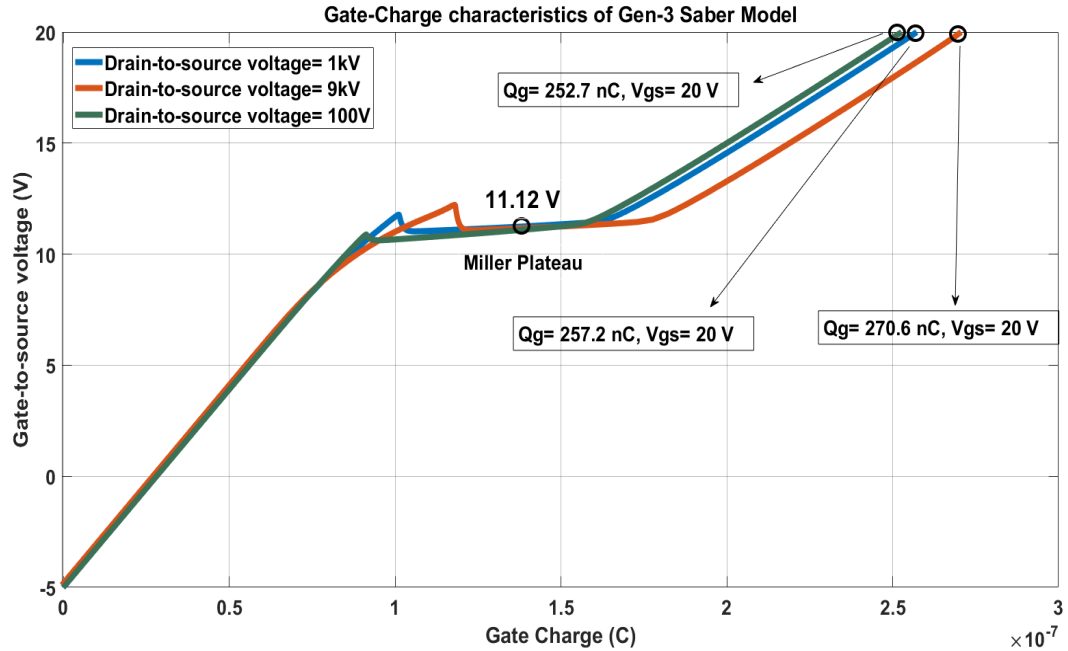


Figure 2.10 Gen-3 Saber device model: gate charge characteristics

To reiterate to the reader, this plot is the characteristic for just one die model (rated 18 A) which has an active area of 0.312 cm^2 . To obtain the characteristics of the entire module (rated 240 A), several of these dice have to be connected in parallel or the active area must be increased to 4.16 cm^2 in the simulation. It is observed from the above plot that the total gate charge required when V_{GS} reaches 20 V is 271 nC when V_{in} (V_{DS}) is 9 kV. The total change in the gate voltage is $20 - (-5) = 25$ V. The value of the required gate charge is slightly short of 253 nC when V_{DS} is decreased all the way to 100 V. The subtle difference is caused by the area under $C_{rss} - V_{DS}$ graph from 100 V to 9 kV. Assuming that the Gen-3 die is operated in a converter running at 20 kHz, the minimum gate driver power predicted by the model is:

$$P_{drv,min} = 271nC \times 25V \times 20kHz = 135.5mW \quad (2.5)$$

This value would have to be multiplied by the number of dice used in parallel to obtain the overall rating of the driver. Likewise, the peak current capability is computed for a minimum gate resistance of 2Ω .

$$I_{drv,max1} = \frac{25}{2} = 12.5A \quad (2.6)$$

With the reduction factor of 0.7, the peak value becomes,

$$I_{drv,max} = 12.5 \times 0.7 = 8.75A \quad (2.7)$$

The turn-on transition plots obtained from Saber while simulating the schematic are shown in Figures 2.11 and 2.12. The input voltage is changed from 1 kV to 9 kV with other parameters remaining the same. The device model is switched ON at time $t = 50 \mu s$ by applying a gate-to-source voltage. Since the switching is done with a resistive load, the transients (di/dt and dV/dt) happen simultaneously. It should be noted that the model current settles at 10 A without any overshoot in this case. The gate-to-source voltage increases steadily from -5 V to about 11 V where it hits the characteristic Miller plateau as shown in Figure 2.11. The initial spike in the gate current when $R_G = 20 \Omega$ is 1.25 A. The time required to hit the Miller plateau would increase as the value of V_{DS} increases to supply the extra gate charge. For the Gen-3 MOSFET die model, this time ranges from 120 ns to 200 ns for the first transition. For both the 1 kV and 9 kV case, the second transition time is fairly the same after which the gate current begins to drop exponentially.

Saber predicts that the gate driver would have to provide $3.6 \mu C$ of charge to drive the whole module (10 kV, 240 A) of Gen-3. To use the module in a power circuit switching at 20 kHz, the minimum power rating of the driver should be approximately 2 W.

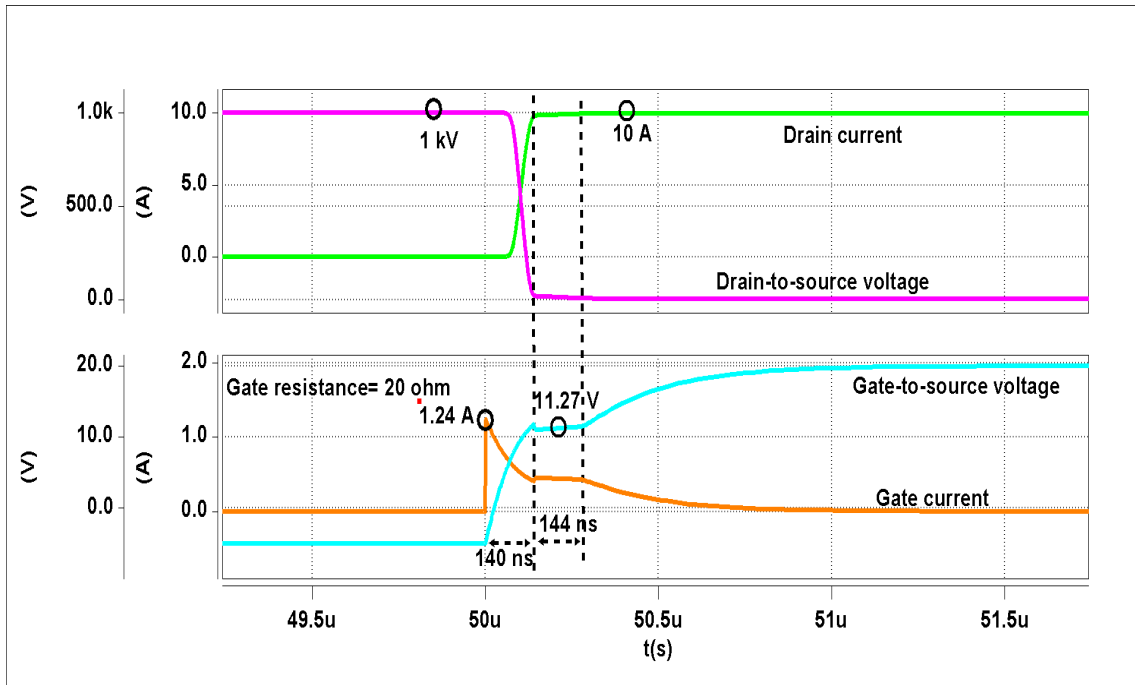


Figure 2.11 V_{DS} , I_D , V_{GS} and I_G when $V_{in} = 1$ kV, current = 10 A and $R_G = 20 \Omega$ (Saber model)

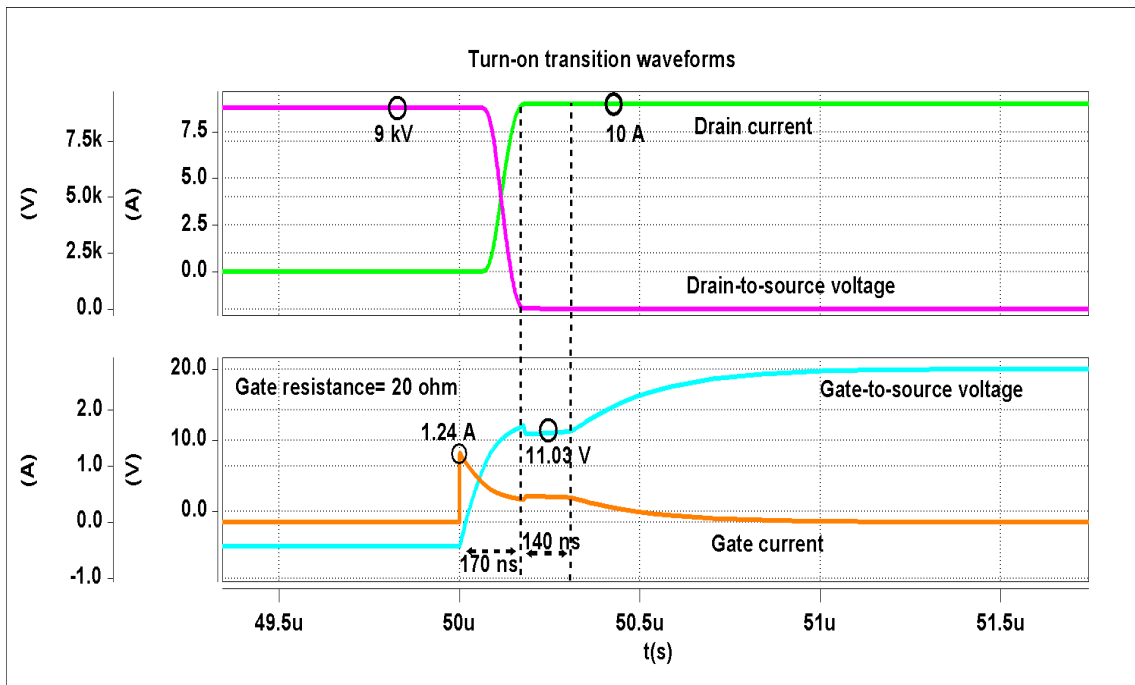


Figure 2.12 V_{DS} , I_D , V_{GS} and I_G when $V_{in} = 9$ kV, current = 10 A and $R_G = 20 \Omega$ (Saber model)

2.3.1 Miller Effect and estimation of gate charging time

For the Gen-3 MOSFET die model, it was observed that the required gate charge to completely turn-on the device varied quite a bit depending on the applied drain-to-source voltage. This section details analysis on how the Miller effect decides the equivalent capacitance during turn-on and the time required to completely turn on the 10 kV die model. Even for a very low value of C_{rss} , the gate driver "sees" a much larger value as it gets multiplied by a factor of $\frac{V_{DS}}{V_{GS}}$ due to Miller Effect. Consider the following discussion,

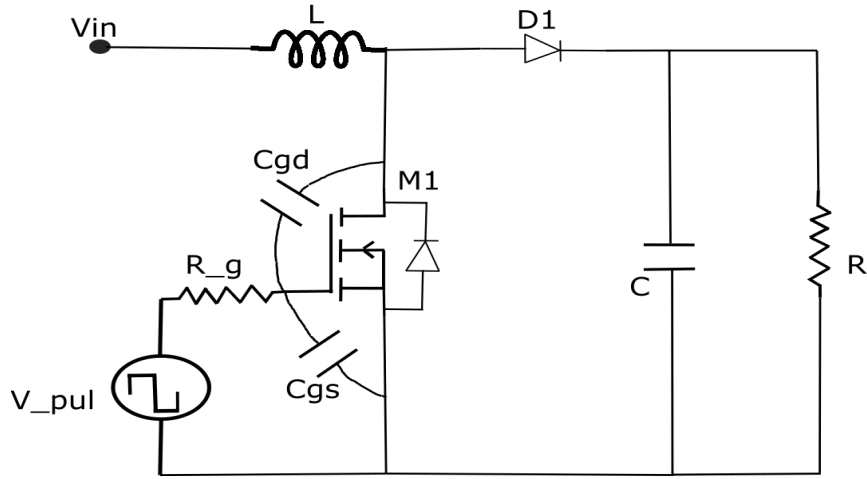


Figure 2.13 Schematic- equivalent capacitance

The total equivalent capacitance can be derived by taking the ratio between the total amount of charge delivered during turn-on and the total change in the value of gate-to-source voltage. Let the values of V_{GS} before turn-on be $V_{GS,min}$ and that after complete turn-on be $V_{GS,max}$. Similarly, let the blocking voltage during turn-off be V_o and the ON-state voltage be zero (ideal case). Thus, the voltage change across C_{gs} is $V_{GS,max} - V_{GS,min}$ and that across C_{gd} would be $V_o + V_{GS,max} - V_{GS,min}$. For simplicity in representation, let the total change in the gate-to-source voltage be represented by V_{GS} . Thus,

$$C_{eq} = \frac{Q_{tot}}{V_{GS}} \quad (2.8)$$

Also the total charge is the sum of the charges present in C_{gs} and C_{gd} ,

$$Q_{tot} = V_{GS}C_{gs} + (V_{GS} + V_o)C_{gd} \quad (2.9)$$

Substituting equation 2.9 in 2.8, we obtain

$$C_{eq} = C_{gs} + C_{gd} \left(1 + \frac{V_o}{V_{GS}}\right) \quad (2.10)$$

Equation 2.10 clearly shows the boost due to Miller effect on the gate-to-drain capacitance. Assuming the ideal case of a constant gate current I_g , one can write the following equation,

$$t_{on} = \frac{C_{eq} V_{GS}}{I_g} \quad (2.11)$$

where t_{on} represents the gate charging time. A more realistic estimation of the charging time is to consider the equivalent circuit shown in Figure 2.14. " V_{pul} " provides an ideal source of PWM pulse and acts like a step input to the R-C circuit during turn-on. The voltage across the equivalent capacitor is the gate-to-source voltage across the MOSFET as indicated. To reach about 98 % of the applied voltage, the elapsed time is about 4 time constants. From multiple iterations of simulation in Saber, it is observed that " Q_{tot} " varies from 250 nC to 275 nC as V_{DS} is increased till the rated value. Using equation 2.8, the maximum value of C_{eq} is found to be 11 nF. Thus, the time constant of the charging circuit for a value of 20 Ω gate resistance would be 220 ns. Thus the model predicts that the 10 kV Gen-3 device would take about 900 ns until the parasitic capacitances are fully charged with a gate resistance of 20 Ω . In the next section, a detailed method for finding the parasitic capacitance (C_{iss} , C_{oss} and C_{rss}) of the model is derived through small signal analysis. The test is also performed with the device in the curve tracer and the values are compared as a function of V_{DS} .

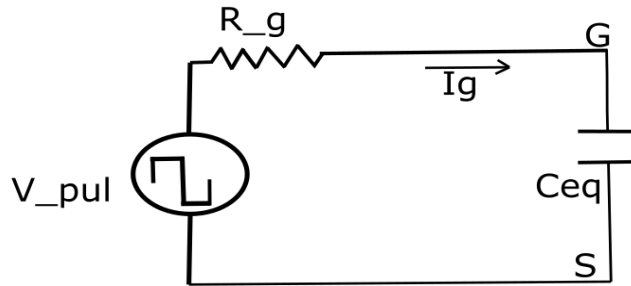


Figure 2.14 Equivalent circuit representation during turn-on

2.4 Parasitic Capacitances

To calculate the input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances of a device model through Saber, small signal analysis has to be carried out at various dc operating points. The method used in this thesis work computes the impedance between two terminals of the model at a frequency of 1 MHz as the capacitance values are generally reported at this frequency in datasheets. The three main parasitic capacitances are defined as follows:

$$C_{iss} = C_{gs} + C_{gd}; C_{oss} = C_{ds} + C_{gd}; C_{rss} = C_{gd} \quad (2.12)$$

As shown in the figure below (refer Figure 2.15), the input capacitance (C_{iss}) is obtained from the reflected impedance between the gate and source terminals by applying a small signal voltage of 25 mV at a frequency of 1 MHz. A large capacitor (compared to drain-source capacitance, C_{ds}) of $5\mu\text{F}$ is connected across the drain-source terminals of the MOSFET model. At the simulated frequency, the $5\mu\text{F}$ capacitor acts as a short in parallel with C_{ds} . All the small signal current bypasses C_{ds} and flows through the short created by the external $5\mu\text{F}$ capacitor. Thus, the equivalent circuit is the parallel combination of C_{gs} and C_{gd} which is the equivalent input capacitance C_{iss} . The impedance calculated by dividing the small signal voltage and currents between the gate source terminals represents the impedance of C_{iss} at that frequency. The other $5\mu\text{F}$ capacitor is just used for isolation purposes and would be required in the hardware setup to block any dc voltage changing the dc operating point of the system. To obtain the output capacitance (C_{oss}) of the Saber model, the gate and source terminals are shorted as shown. The small signal voltage is applied between the drain-source terminals and the current is obtained from the output of the voltage source. The current produced by the small signal source has two paths to flow, one through C_{gd} and the other through C_{ds} . Thus, the total impedance seen from the drain-source terminals is that of the parallel combination of C_{ds} and C_{gd} , which is the equivalent output capacitance (C_{oss}). To calculate the reverse transfer capacitance (C_{rss}) of the Saber model, the gate-source terminals are shorted and the voltage source is placed on the drain of the MOSFET. Like the previous case, the small signal current has two paths to flow. But, only the current coming out of the gate terminal is of importance in this case, which is represented as $ic1$ in the figure. By dividing the values of the applied small signal voltage and current $ic1$, one can obtain the impedance presented by C_{gd} alone as it excludes $ic2$ which flows through C_{ds} . From the value of the impedance, the value of the reverse transfer capacitance can be obtained.

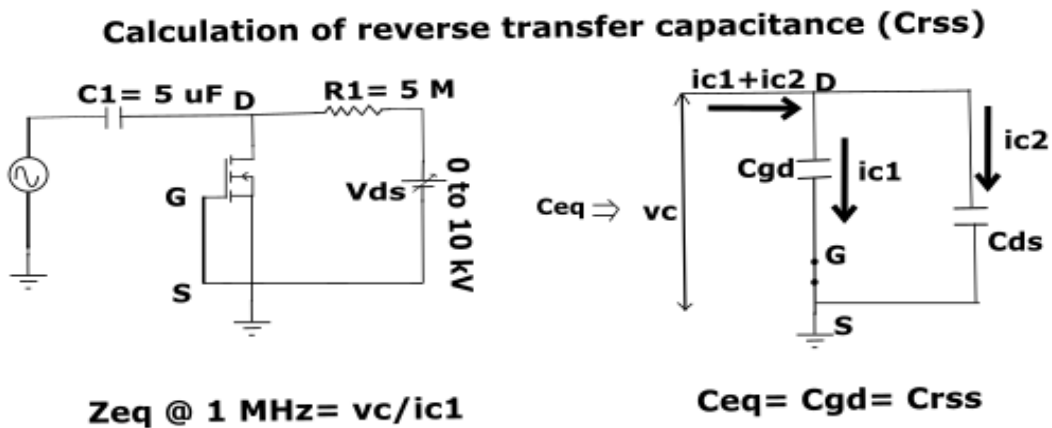
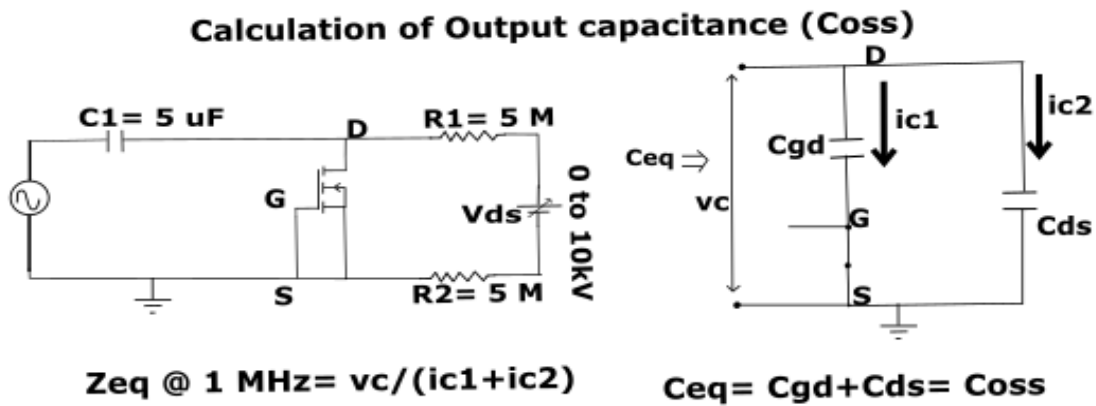
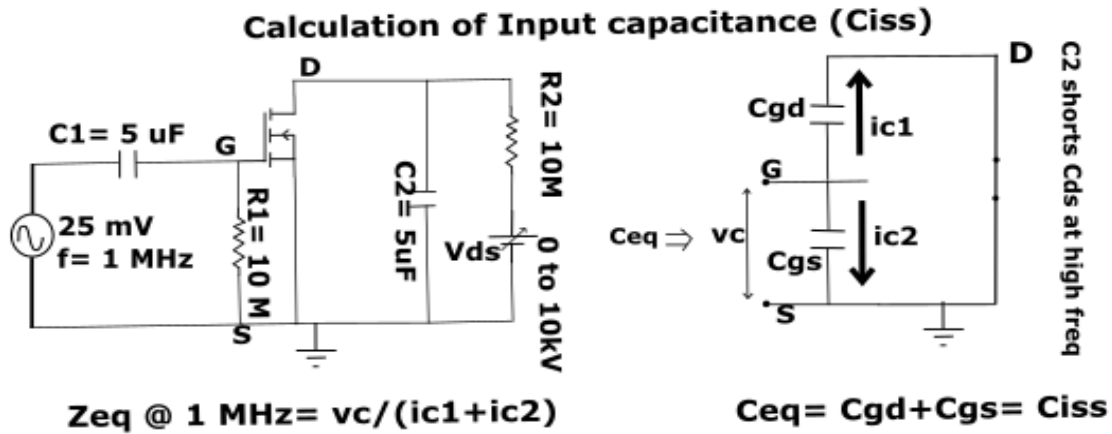


Figure 2.15 Calculation of parasitic capacitances of the Saber model

2.4.1 C_{iss} Calculation

Saber simulation is conducted over 0-1000 V range of the drain-to-source voltage (and later extended to 10 kV). The schematic used for simulation is shown in Figure 2.16. Plotting the small signal voltages and currents from Saber, one can clearly see the phase difference between the waveforms confirming that the impedance is capacitive in nature. From the plot of currents and voltages in Figure 2.17, it can be seen that the impedance offered by C_{iss} is 36.06Ω when $V_{DS} = 500V$ and frequency of interest is 1 MHz. From these results, the value of the equivalent input capacitance can be easily calculated as shown:

$$C_{iss}(\text{when } V_{DS} = 500V) = \frac{1}{2 \times \pi \times 1 \times 10^6 \times 36.06} = 4.41 nF \quad (2.13)$$

Similar analysis can be extended for various voltages in this range. The final plot of the values of parasitic capacitances is shown at the end of this subsection.

Schematic to obtain small-signal input capacitance (C_{iss})

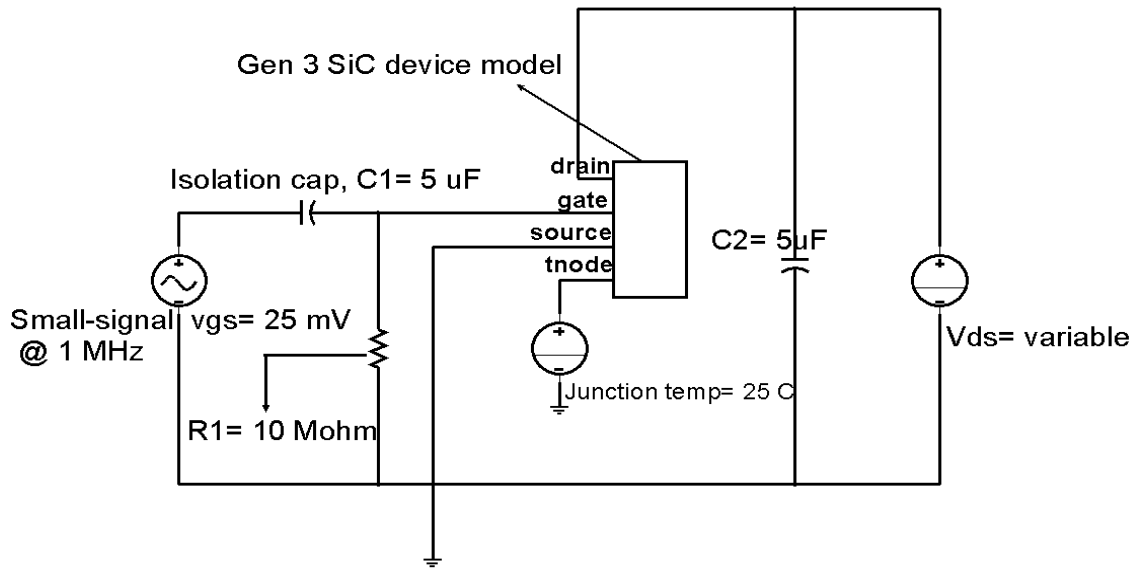


Figure 2.16 Saber simulation to obtain C_{iss}

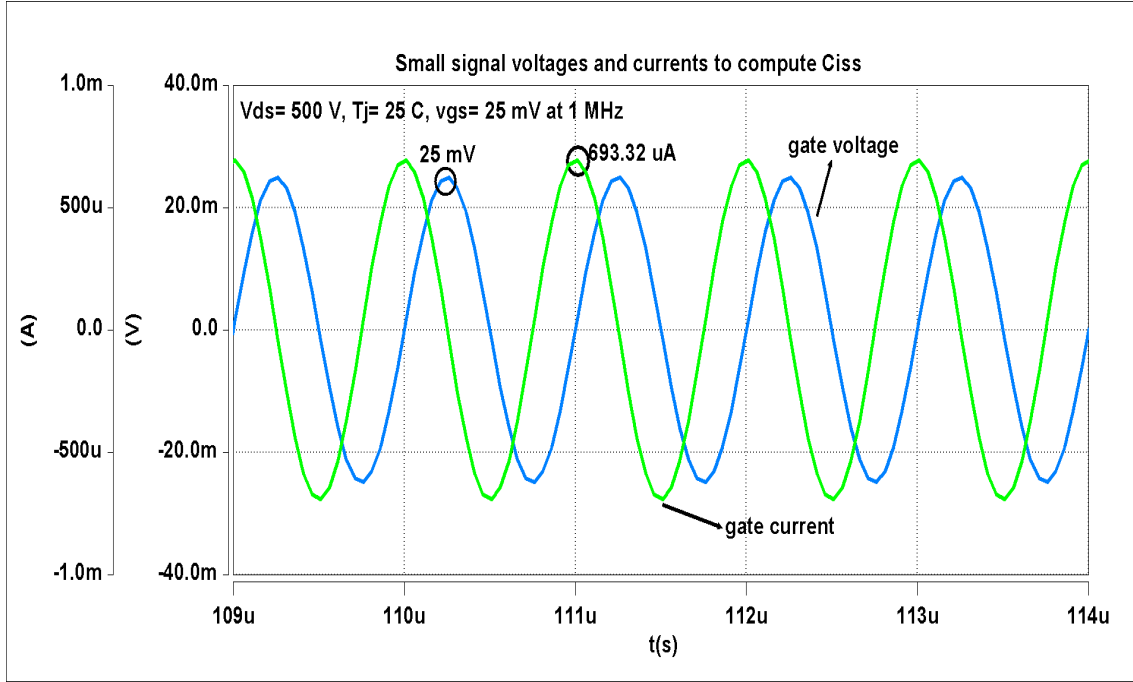


Figure 2.17 Small-signal voltages and currents- C_{iss} calculation of Saber model

2.4.2 C_{oss} Calculation

As explained in the introductory section, the equivalent output capacitance is calculated by finding the impedance seen across the drain-source terminals after shorting the gate and source. The following plot shows the waveforms of the small signal voltages and currents when the DC biasing voltage is 500 V. The peak value of current is $24.58 \mu A$ for an input small signal voltage of 25 mV as shown in Figure 2.19. Thus, the equivalent output impedance is 1016.75Ω . The value of the equivalent output capacitance corresponding to this value of impedance is

$$C_{oss}(when V_{DS} = 500V) = \frac{1}{2 \times \pi \times 1 \times 10^6 \times 1016.75} = 158.39 pF \quad (2.14)$$

Saber schematic to obtain small signal Output Capacitance(C_{oss})

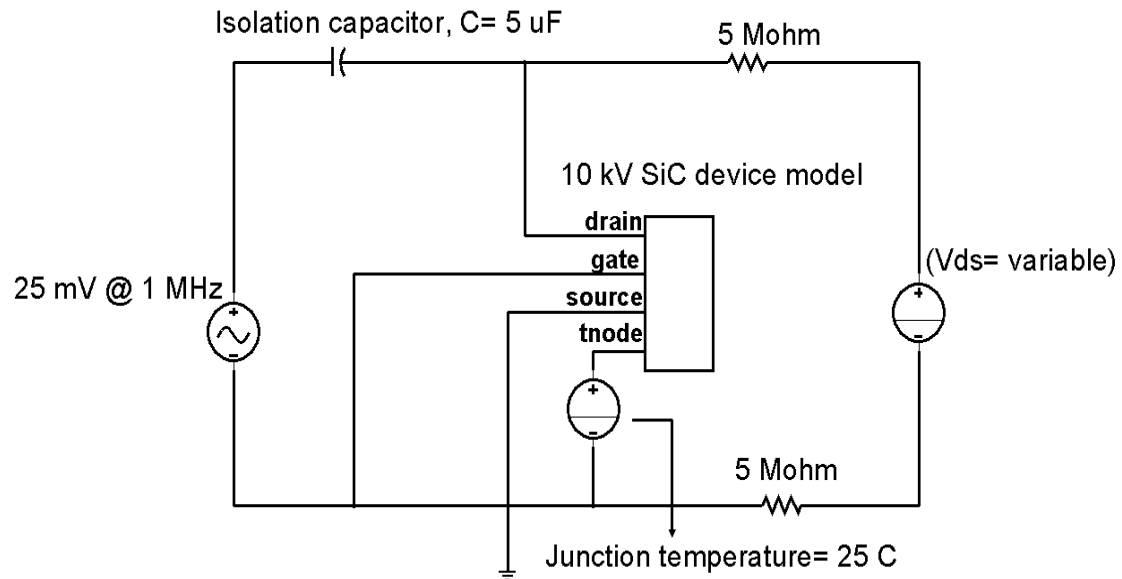


Figure 2.18 Saber simulation to obtain C_{oss}

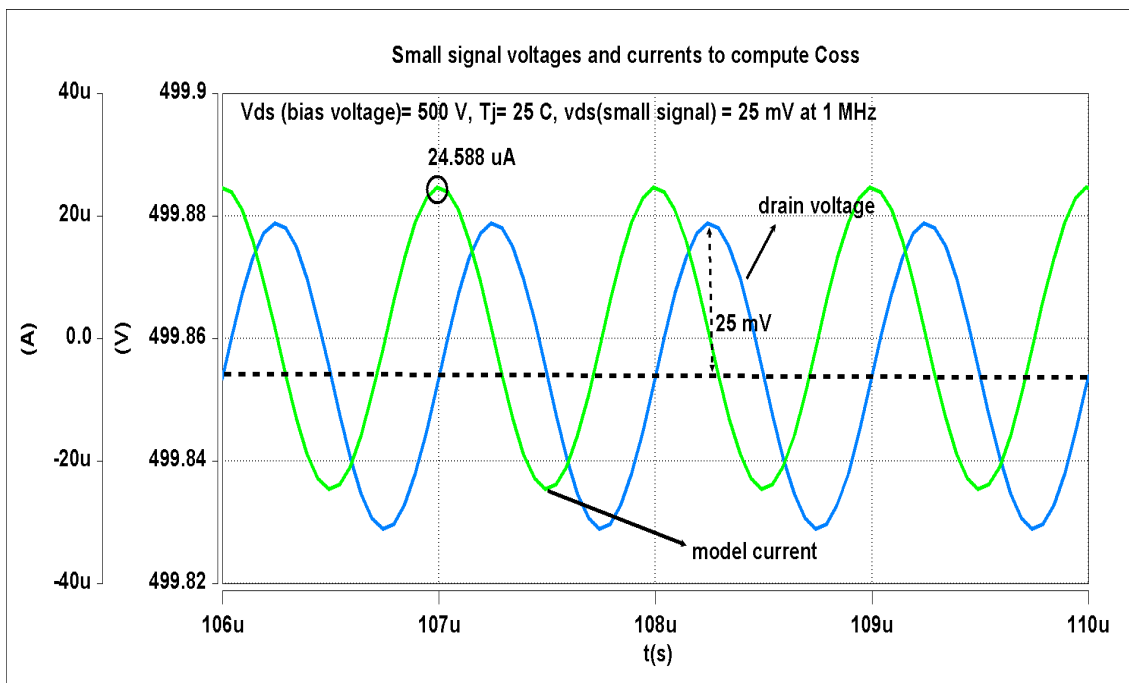


Figure 2.19 Small signal voltages and currents- C_{oss} calculation of Saber model

2.4.3 C_{rss} Calculation

The schematic used in the simulation is shown in Figure 2.20. The small signal current flowing through the Miller capacitance is obtained through simulation by finding the current through the zero voltage source marked as "ig" in the figure. The small signal voltage across the capacitance is 25 mV. The impedance is calculated across the drain-gate terminals. Figure 2.21 shows the values of the small signal voltages and currents when $V_{DS} = 1000$ V. The peak current observed in this case is 639.53 nA corresponding to a voltage drop of 25 mV. The reverse transfer capacitance is obtained by the following computation:

$$Z_{eq}(when V_{DS} = 1000V) = \frac{25mV}{639.53nA} = 39091.207\Omega \quad (2.15)$$

$$C_{rss}(when V_{DS} = 1000V) = \frac{1}{2 \times \pi \times 1 \times 10^6 \times 39091.207} = 4.07pF \quad (2.16)$$

Saber schematic to obtain Crss as a function of Vds

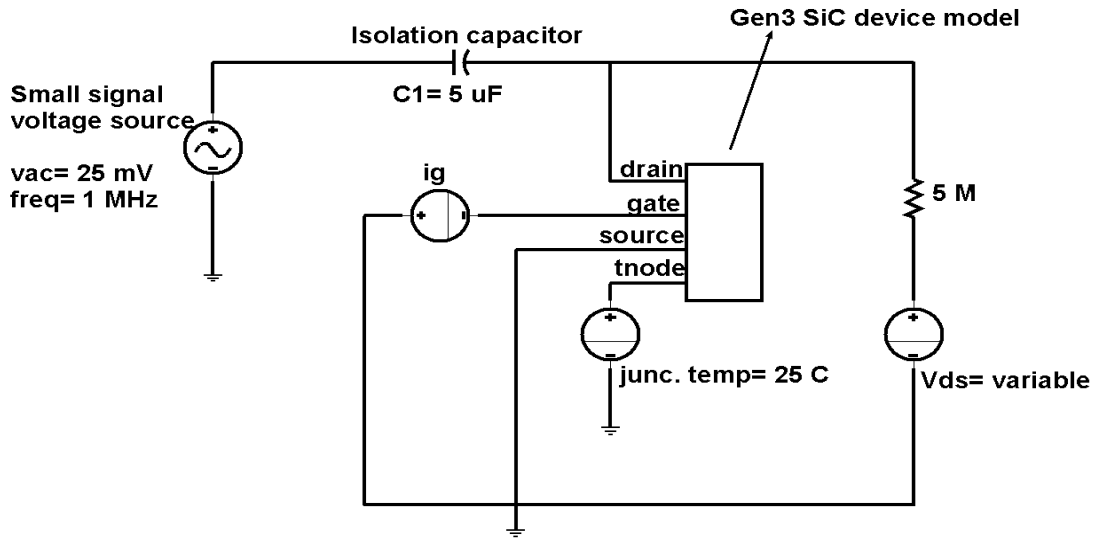


Figure 2.20 Saber simulation to obtain C_{rss}

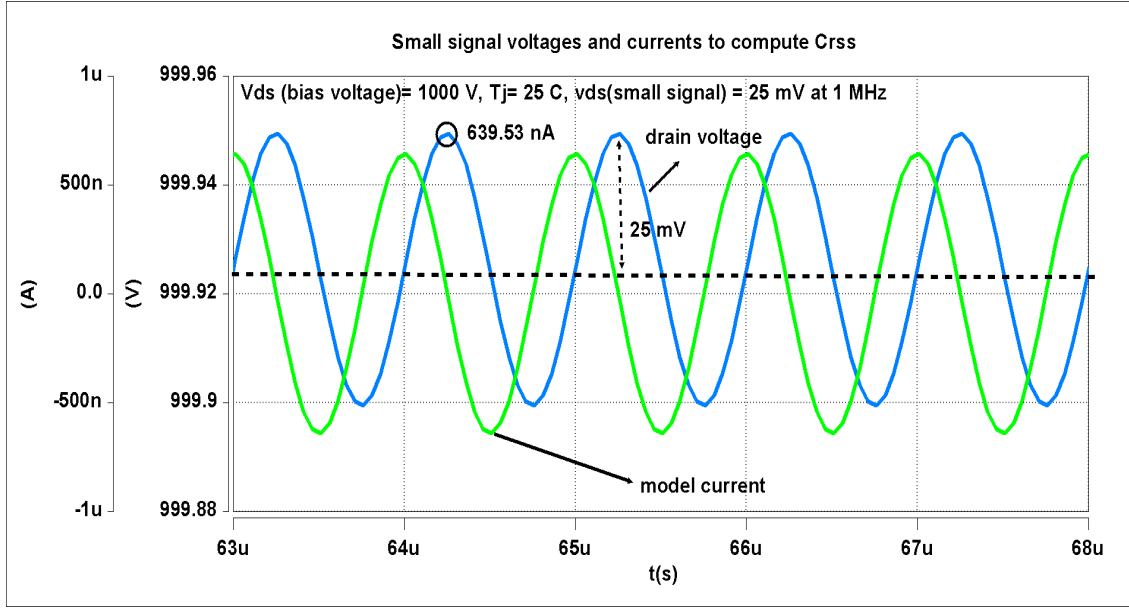


Figure 2.21 Small signal voltages and currents- C_{rss} calculation of Saber model

Plotting the parasitic capacitance obtained from Saber in a semi-log graph vs drain-to-source voltage, the following values are obtained which are presented in Figure 2.22. The equivalent input capacitance (C_{iss}) is seen to more or less constant at about 4.5 nF over the entire range of V_{DS} sweep except the initial portion. The output capacitance (C_{oss}) is observed to vary from 7 nF at $V_{DS} = 0$ V to 106 pF as V_{DS} is increased to 1 kV. The value drops further and reaches to about 44 pF when V_{DS} is 8 kV. The reverse transfer capacitance (C_{rss}) varies from just over 3 nF to 4 pF across a V_{DS} sweep of 1 kV. It more or less stays constant at a few pF for V_{DS} ranging till 10 kV which is the rated voltage of the device. It should be noted that all the calculations are carried out at 1 MHz for one die model with no large signal bias voltage applied across gate and source. As the values of capacitance are important for lower value of the drain-to-source voltage, a zoomed-in plot is also shown for reference from 0 V to 1 kV V_{DS} . The integration of the C-V curve results in the maximum amount of charge for values V_{DS} closer to zero volts. Figure 2.23 also shows the values obtained from the curve tracer (drawn with thick lines and Saber values with dotted lines). The values calculated from the Saber model provide a reasonable match to the actual values. However, it can be expected that the error in the parasitic capacitance would result in variation in the switching losses of the device and this would be analyzed in more detail in the final chapter.

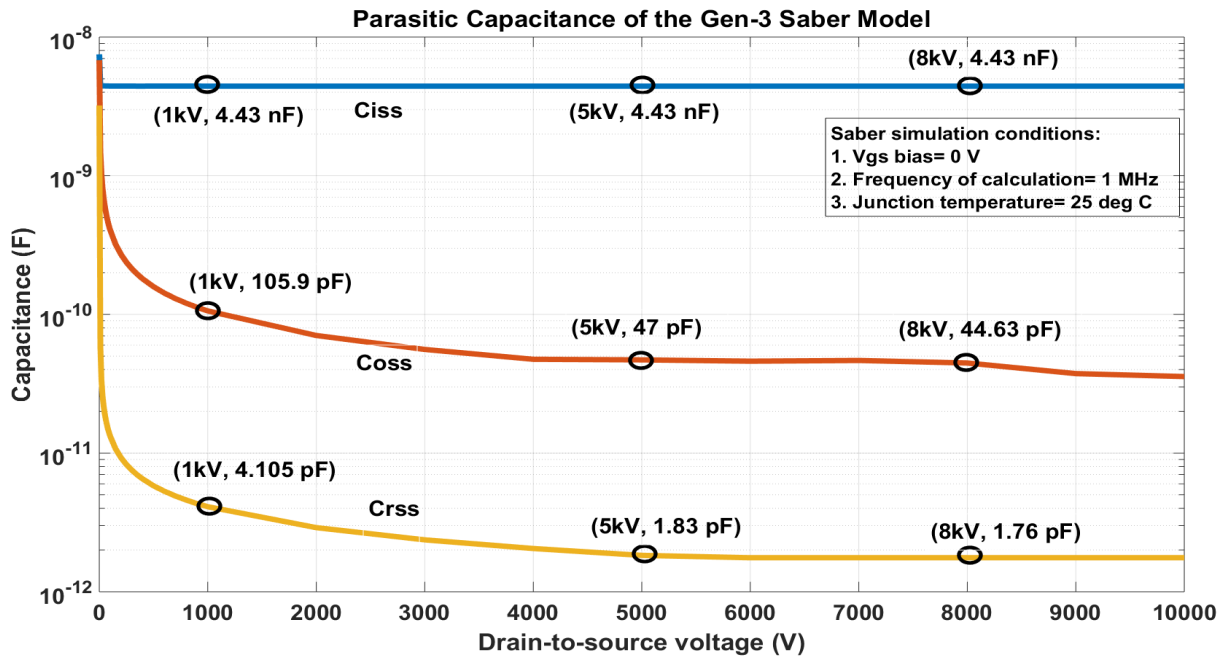


Figure 2.22 Parasitic capacitance of Saber model vs V_{DS}

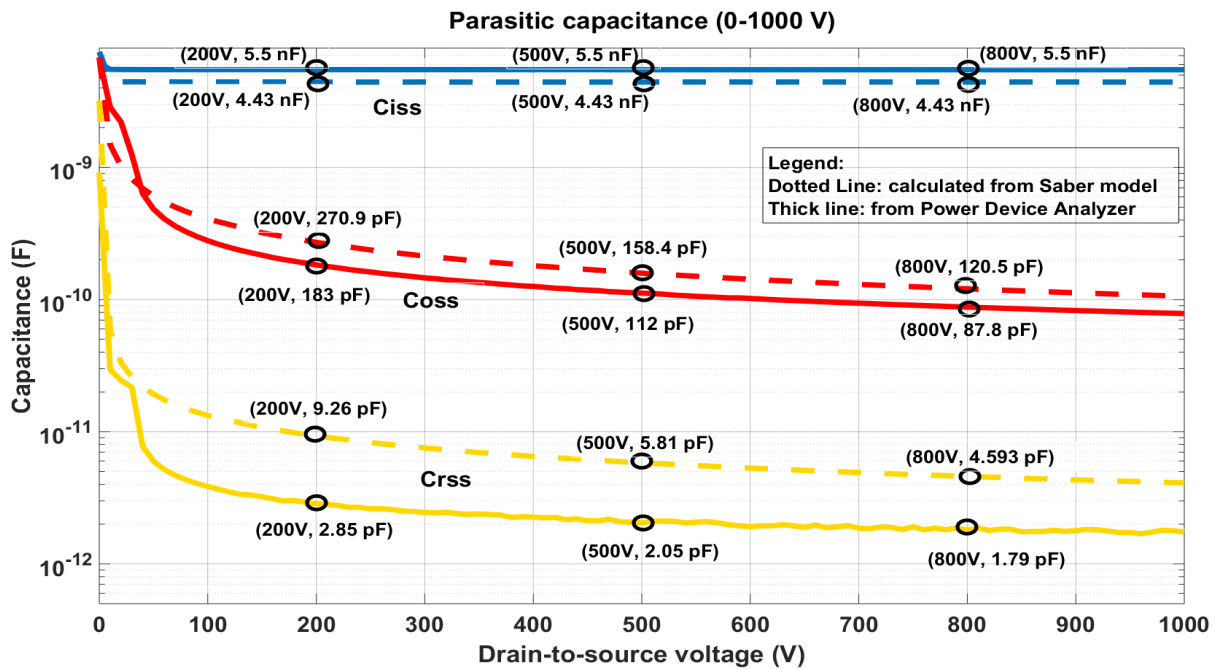


Figure 2.23 Parasitic capacitance vs V_{DS} (zoomed-in plot) (Saber vs Curve Tracer values)

2.5 Leakage Current

The leakage current flowing through the 10 kV Gen-3 MOSFET die model is evaluated by shorting the gate and source terminals and varying the drain-to-source voltage from zero to the rated blocking voltage of the device. The schematic used in the simulation is shown in Figure 2.24.

Circuit schematic to obtain drain-to-source leakage current

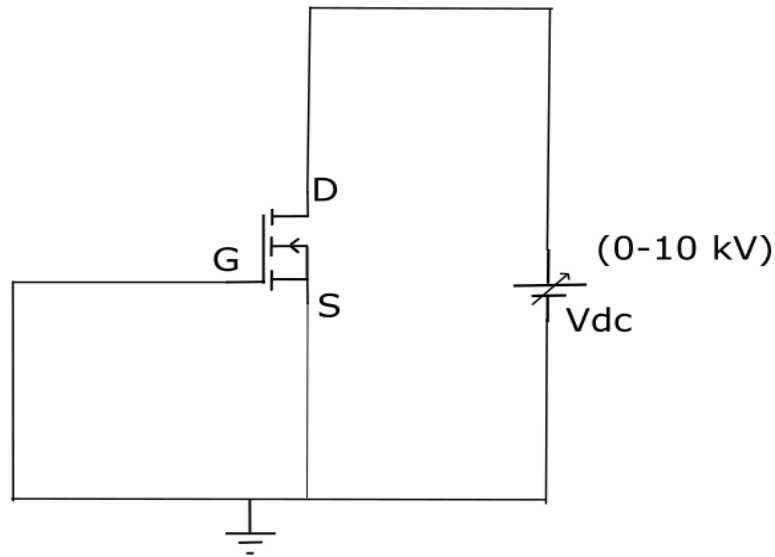


Figure 2.24 Schematic- leakage current

As the 10 kV Gen-3 MOSFET is a Silicon Carbide device, it is natural to expect a very low value of leakage current. At elevated temperatures, the power dissipation in the device during the OFF state may become significant and cannot be ignored when compared to other sources of losses in the system. The leakage current multiplied by the blocking voltage of the power device would result in the OFF state power loss. To conduct this analysis, two different packaged dice of Gen-3 are also tested with the B1505 curve tracer. Even though the equipment has the ability to go up to 3.3 kV, the drain-to-source voltage is only increased till 2 kV for safety reasons. The following plot shows the results obtained with the Saber model and the actual dice on one semi-log graph.

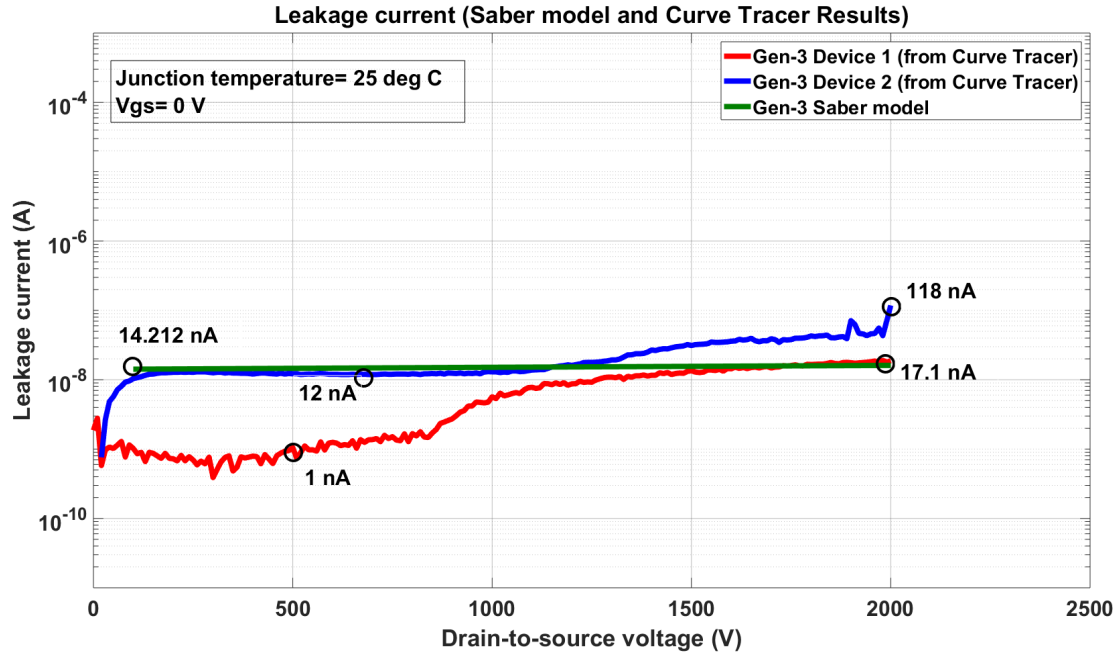


Figure 2.25 Schematic- leakage current: Saber model and actual device

At room temperature, the Saber model predicts a leakage current that is fairly constant over the V_{DS} range of 0 to 2 kV. The model provides an approximation to the actual behaviour but this can still be used to predict the OFF-state losses in a power converter. The two devices differ quite significantly in their leakages and this may be attributed to the inherent variations during the manufacturing process and the device usage until then. Nevertheless, the leakages show a similar increasing trend after 2 kV blocking voltage and this can be studied further by doing simulations in Saber.

The leakage current of the Saber model (see Figure 2.26) shows an increase at $V_{DS} = 2$ kV and increases with a steeper slope from 3 kV. The consistent exponential trend produces leakage in the order of μA when the blocking voltage across the model is 5 kV. Figure 2.26 illustrates the variation due to junction temperature on the model. It is to be noted that the simulation did not converge for drain-to-source voltages greater than the values shown in the plot. The temperature node of the model experienced large instantaneous fluctuations outside the defined sample points on the high end. Since this is a model for the 10 kV device, it can be expected that the results be obtained until its full voltage rating. By performing this analysis, it is concluded that even though the model does not predict the leakage current over the full range of the blocking voltage, it does provide fairly consistent data to calculate the losses in the system and emulates the behaviour of a typical Gen-3 device.

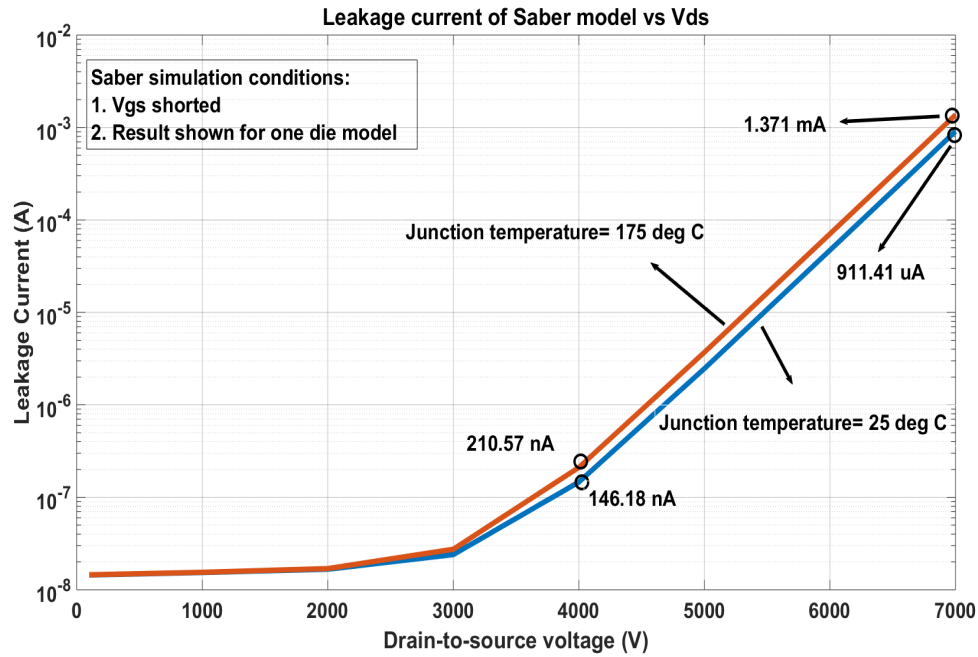


Figure 2.26 Leakage current vs V_{DS} (Saber model)

2.6 Body Diode Characteristics

As seen earlier, the Gen-3 MOSFET has an associated body diode in its package. This section outlines the circuit schematic and plots of the I-V characteristics, reverse recovery charge, changes due to temperature variations and subsequent effect on the turn-on of the complementary device model.

Saber Simulation to obtain the I-V characteristics of the body diode model

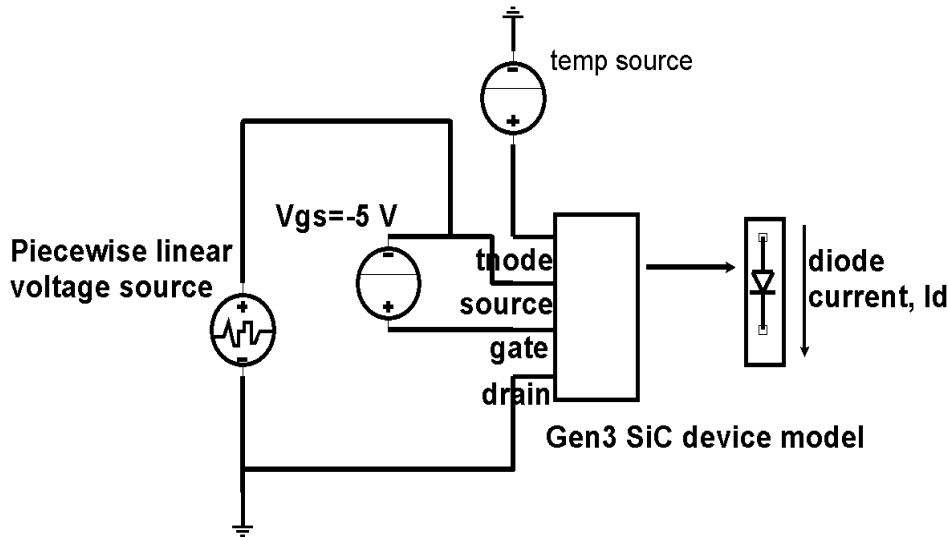


Figure 2.27 Schematic body diode forward characteristics

The gate-to-source voltage is maintained at -5 V to suppress the conduction of the MOSFET channel (Figure 2.27). The applied input voltage is a piecewise linear function and it is increased to study the current flowing through the body diode. The internal diode characteristics are also obtained from the curve tracer and the two are compared in Figure 2.28. The knee voltage for the diode conduction is seen to be 2.32 V from the Saber model. The ON-state resistance of the model/actual device is obtained by taking the inverse of the slope of the graph. At 25 °C, Saber predicts 355 mΩ when the actual body diode exhibits a resistance of 390 mΩ.

The relationship between the diode current and the forward voltage drop is given by the following equation:

$$I = I_o \left(e^{\frac{qV}{nkT}} - 1 \right) \quad (2.17)$$

where,

I is the diode current

I_o is the dark saturation current

V is the applied voltage

k is the Boltzmann's constant

N is the ideality factor (number from 1 to 2)

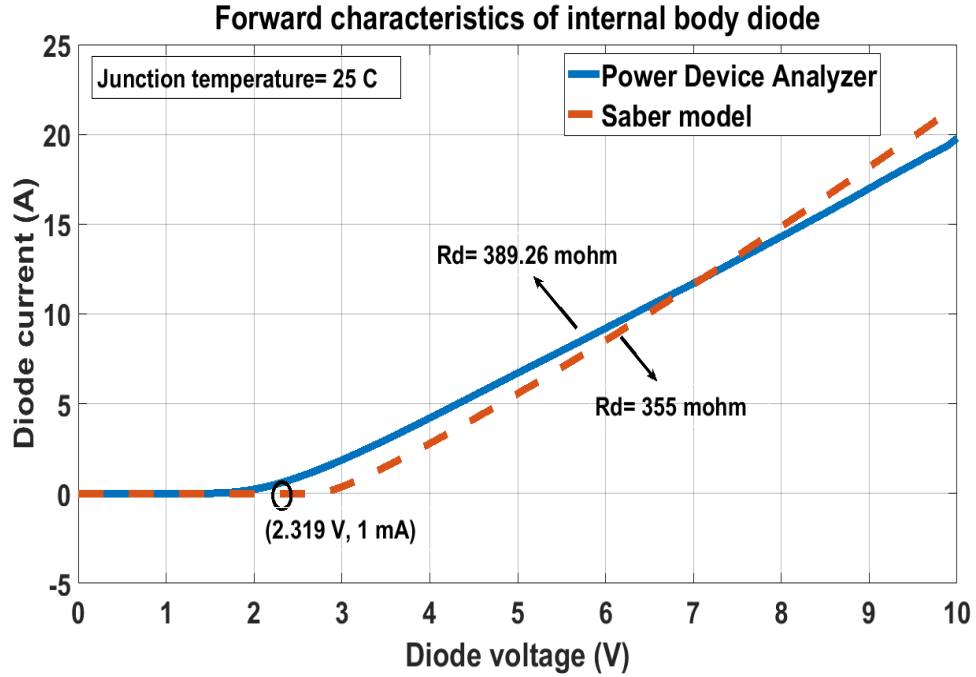


Figure 2.28 I-V Characteristics of the Gen-3 internal body diode

The factor kT/q is called the thermal voltage and approximately equals 26 mV at 300 K. The exponential relationship can be linearized as [6]:

$$V_f = V_d + I_d R_d \quad (2.18)$$

where, V_f is the total on state voltage drop, V_d - the forward voltage drop across the diode, I_d - the on state current and R_d - the series resistance of the diode obtained by piece-wise linear approximation.

The internal body diode model in Saber accounts for changes due to temperature and exhibits a positive temperature coefficient for the diode resistance. Practically, the conduction losses increase at higher temperatures and it turns out to be useful for current sharing and paralleling of devices if the application requires a larger value of current compared to the rating of the device. Figure 2.29 shows the Saber simulation results at different junction temperatures. The value of ON-resistance at 25°C is,

$$R_d = \frac{9.17 - 2.78}{18} = 355 m\Omega \quad (2.19)$$

At 150°C,

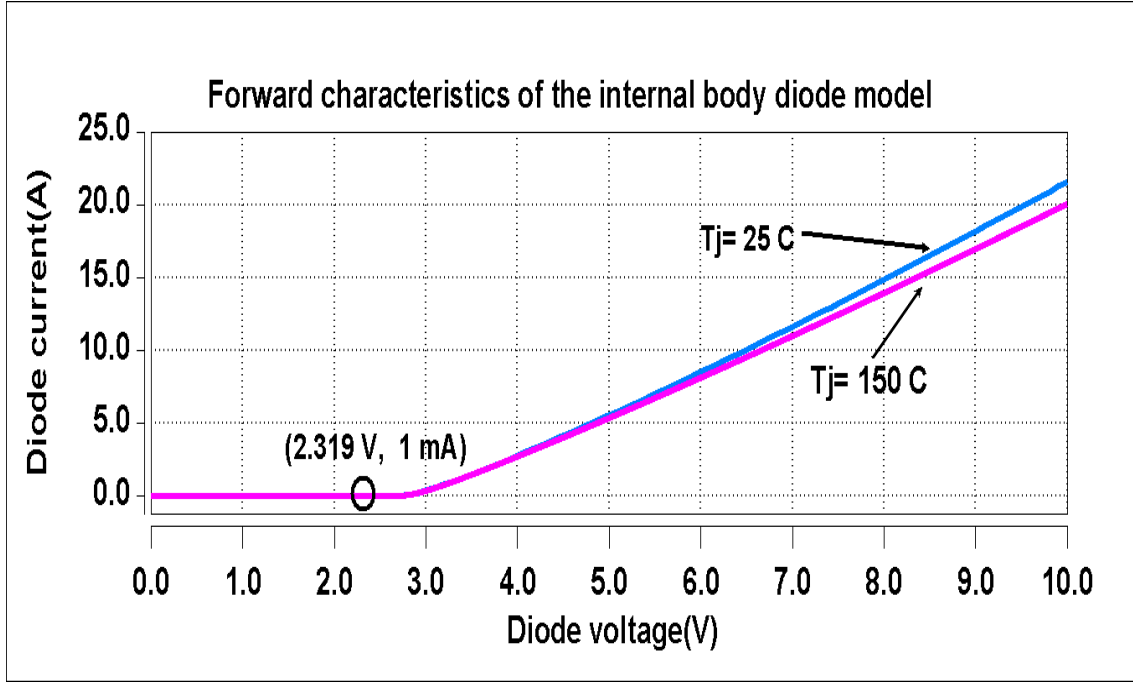


Figure 2.29 I-V Characteristics (Saber model): body diode

$$R_d = \frac{9.36 - 2.78}{18} = 365.5 m\Omega \quad (2.20)$$

As per equation 2.17, it can be deduced that as temperature increases, the value of the knee point of the I-V curve must decrease. But looking at Figure 2.29, it is clear that the device model does not predict this behaviour. The diode model has to be made more accurate for values of current close to the knee value. In this thesis, for the sake of analysis, 1 mA is taken as the minimum value of model current that determines the knee voltage.

In a half-bridge configuration, the junction capacitance and the process of diode reverse recovery of the top device interacts with the switching of the bottom MOSFET during its turn-on and contributes to an increase in the turn-on losses. For studying this behaviour, a half-bridge configuration of the Gen-3 model is simulated in Saber. The top device is connected with its V_{GS} maintained at -5 V so the conduction mainly happens through the diode and not the MOSFET channel. The characteristics are obtained for an on-state current of 15 A, and a DC bus voltage of 8 kV. The junction temperature in the simulation is adjusted to 25°C and 150°C.

Refer schematic shown in Figure 3.7 for the following discussion.

At the instant when the bottom device model is turned on, the ON-state current of 15 A shuttles to this device with a ramp rate of -167 A/ μ s in the diode when the gate resistance is 20 Ω . It overshoots zero and reaches a negative peak of -10.75 A. Only after this time, the diode would be able to block

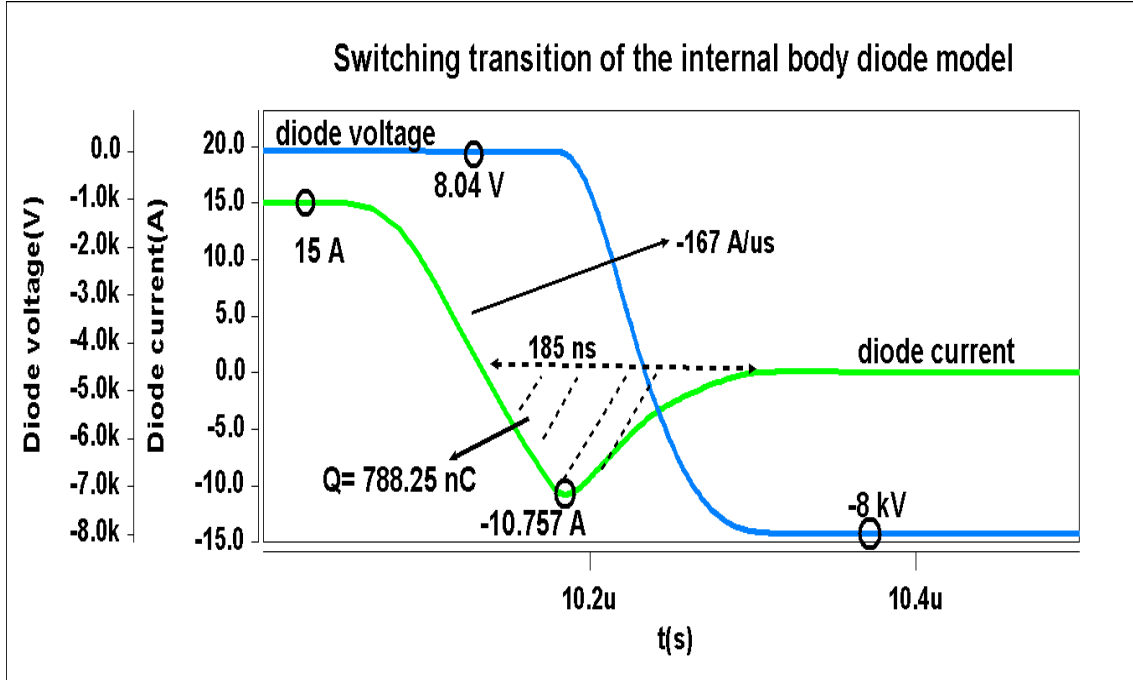


Figure 2.30 Switching currents and voltages in the body diode Saber model- 25°C

voltage across its terminals. The diode drop of 8 V starts to decline at the instant current reaches its negative peak. The blocking voltage in this case is the applied DC bus voltage of 8 kV. The current comes back to zero after a time of 185 ns of the first zero crossing. This time interval is generally referred to as the recovery time (t_{rr}). It can be seen that 788 nC of charge has to be removed from the diode model in order to completely bring it to the blocking state. This value is highly dependent on the values of the operating points (V_{DS} and I_{DS}), junction temperature and active area of the device. To illustrate this, the same simulation is carried out at 150°C. The values of the current ramp rates and peak negative current increase with temperature whereas the recovery time (t_{rr}) decreases with temperature.

2.6.1 Charge analysis of the Saber body diode model

As seen previously, the accumulated charge in the body diode would discharge through the bottom device during its turn-on transition. This would increase the turn on losses when compared to a resistive load that would not require a freewheeling diode. Turn-off losses, on the other hand, can be expected to remain more or less the same. Let " Q_{rr} " denote this reverse recovery charge contributed by the body diode. Q_{rr} would be responsible for the total increase in the turn-on losses of the bottom device.

The reverse recovery characteristic is a function of the ON-state current, the switching current

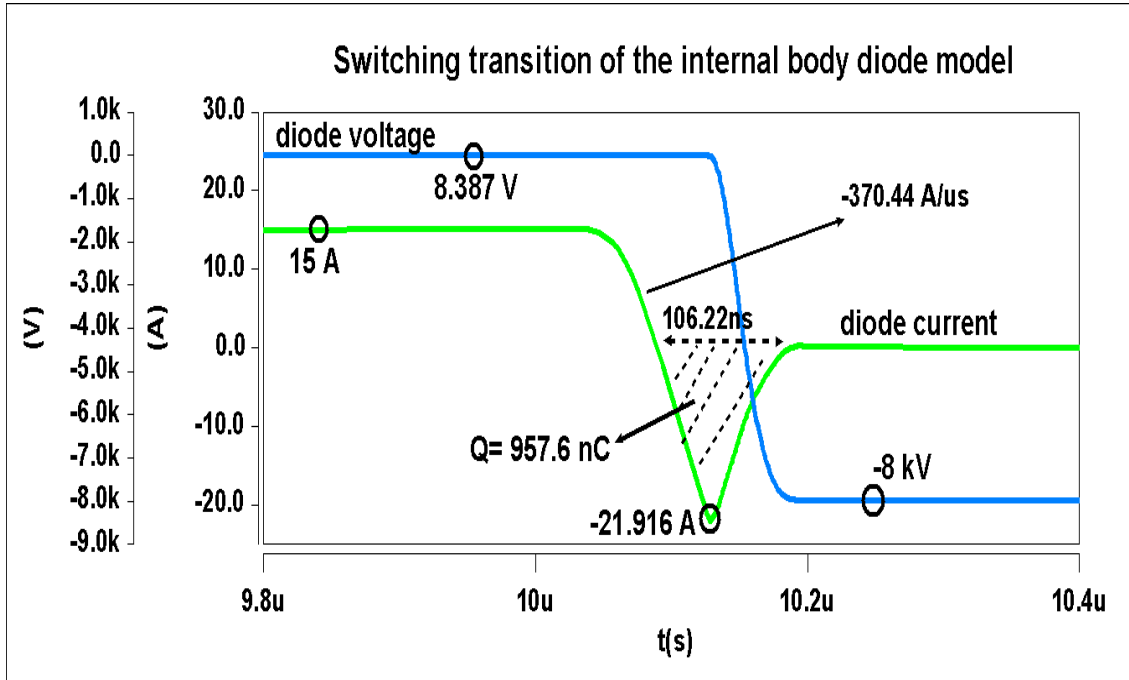


Figure 2.31 Switching currents and voltages in the body diode Saber model- 150 °C

ramp rates and the amount of time that the diode is conducting to accumulate charge in its body. By changing the value of gate resistance, one can achieve desired values of di/dt through the device. The negative peak during this transition can vary accordingly thus changing the value of the net charge flowing through the bottom device.

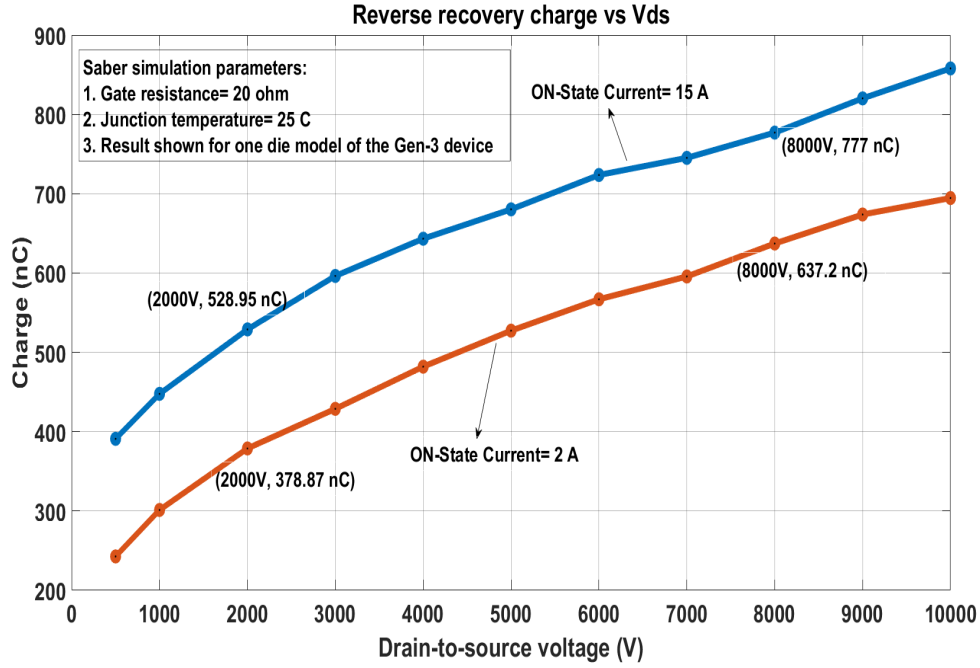


Figure 2.32 Total recovery charge (Q_{rr}) vs V_{DS} : Saber simulation

Figure 2.32 shows the Saber results of the Gen-3 MOSFET die model used in a double pulse circuit in half bridge configuration. The blue and the red lines indicate the total charge (Q_{rr}) flowing into bottom device model as a function of drain-to-source voltage and ON-state current. At 8 kV, Q_{rr} is about 640 nC when the model current is 2 A and increases to 780 nC when the current is increased to 15 A. The final chapter of this thesis would discuss the switching losses of the Gen-3 device in detail comparing the experimental results at different device currents and blocking voltages with the results obtained from Saber. Figure 2.33 shows the effect of changing the gate resistance for a particular value of model current when the junction is at room temperature.

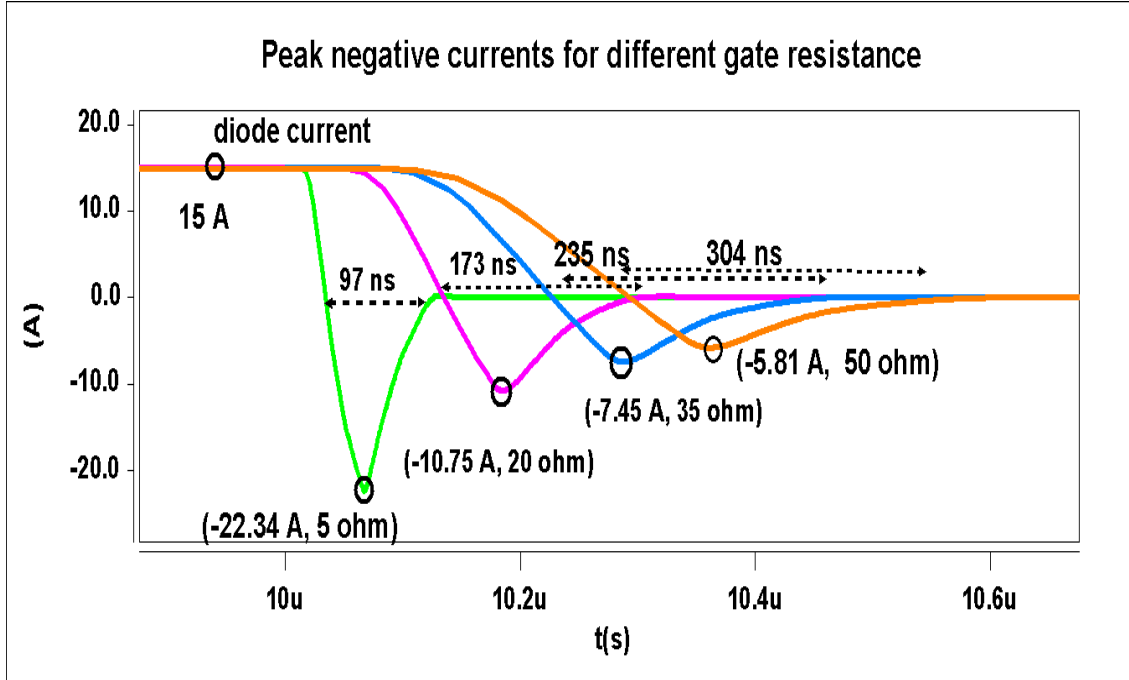


Figure 2.33 Diode turn-off characteristics: Saber simulation

As gate resistance is decreased from 50 Ω to 5 Ω , the magnitude of the peak negative current increases. The peak value adds to the on-state current in the lower device sometimes making it well exceed the continuous current rating. This phenomenon can be taken as the basis for placing an optimum value for the gate resistance so that the overshoot of current in the bottom device is limited under a particular maximum value. For instance, the peak current in the device under test (DUT) will be $15 + 22.34 = 37.34$ A during its turn-on transition for a gate resistance of 5 Ω . The value of the recovery time (generally denoted as t_{rr}) is another quantity of interest when the device is used in circuits working at higher frequencies. The area obtained by integrating the current during this time equals the total charge that is removed from the body diode model during the turn-off transient. Table 2.2 shows some important results obtained by simulating the double pulse test on Gen-3 device model in a half-bridge configuration. The turn-off characteristic of the diode can be understood by analyzing it in two parts. The initial component ' t_a ' is the time required for the forward current to reach the negative maximum after the first zero-crossing of the current. From a physics standpoint, this time is primarily decided by minority carrier lifetime control. The latter half of the cycle ' t_b ' is the time required for the current to go back to almost zero (sometimes defined as 10% or 5% of the maximum value) from the negative maximum value attained at the end of ' t_a ' transition.

Table 2.2 Gen-3 internal body diode switching characteristics: Saber simulation

S.No	$R_G(\Omega)$	di/dt (A/ μs)	Peak reverse current (A)	$t_a(ns)$	$t_b(ns)$	$t_{rr}(ns)$	Softness factor (t_b/t_a)
1	2.2	-1130.88	-28.133	26.362	48.891	75.235	1.854
2	10	-371.13	-16.177	40.101	79.557	119.658	1.983
3	20	-197.87	-10.743	50.132	116.19	166.322	2.317
4	40	-100.294	-6.83	62.98	192.93	255.91	3.06
5	60	-56.91	-5.098	73.117	281.08	354.197	3.844
6	100	-53.48	-3.661	91.265	440.37	531.635	4.825

Softness factor is defined as the ratio of the times t_b and t_a (t_b/t_a). The higher this value, the softer the recovery. Intuitively, one can understand that as the current drops to zero more smoothly in the t_b region for the same value of t_a , the transition becomes more "soft". Conversely, an abrupt transition is characterized by a very low value of ' t_b ' for a given value of ' t_a '. A soft recovery behaviour is beneficial in reducing the voltage spikes in a power converter [2]. However, this is usually accompanied by an increase in the recovery time which leads to higher power dissipation and lower overall efficiency. Table 2.3 shows Saber simulation results of the reverse recovery charge as a function of ON-state current keeping the current ramp rate constant at -200 A/ μs . Looking at the pattern, it can be understood that the reverse recovery charge at a particular di/dt increases with the ON-state current through the body diode. Similarly, Q_{rr} increases with di/dt for a constant test value of ON-state current. Table 2.4 shows the effect on the reverse recovery charge when the magnitude of current ramp rate through the diode is increased from 76 A/ μs to 500 A/ μs by varying the gate resistance. Generally, body diode conduction happens during the dead time of a power circuit. This gives the designer some leverage in adjusting the conduction time (dead time of the converter) to decrease the value of turn-on loss in the MOSFETs. Another possible way to decrease the energy loss is by changing the topology of the circuit itself, but this may not be practical in several circumstances.

If the ramp rate of current is decreased (see Figure 2.35) for the same ON-state value, the switching losses contributed by diode reverse recovery can potentially be decreased. However, the di/dt in a circuit is determined by the parasitic inductance of the commutation loop. Thus, to achieve lower di/dt , the parasitic inductance has to be made intentionally higher but this goes against a good design guideline of a PCB. This means that the best solution would only be to improve the device level mechanics of the internal diode which causes this phenomenon. Figures 2.34 and 2.35 are Saber simulation results that illustrate how it is inevitable in circuits using the body diode of the Gen-3 device in experiencing additional switching losses. Note that this only applies to hard

Table 2.3 Q_{rr} as a function of ON-state current when $di/dt = -200$ A/ μ s: Saber simulation

S.No	ON-state current (A)	DC bus voltage (kV)	Reverse recovery charge (nC)
1	1.5	8	625.75
2	5.05	8	706.88
3	8	8	751.46
4	12	8	779.91
5	15	8	783
6	17.5	8	794.65

Table 2.4 Q_{rr} at $V_{DC} = 8$ kV and diode current = 15 A: Saber simulation

S.No	$R_G(\Omega)$	Current ramp rate (A/ μ s)	Reverse recovery charge (nC)
1	50	-76.4	657.58
2	30	-122.06	730.51
3	20	-192.43	787.11
4	15	-258.23	828.39
5	10	-378.25	879.56
6	7.5	-494.68	920.96

commutation and does not take ZVS or ZCS into consideration.

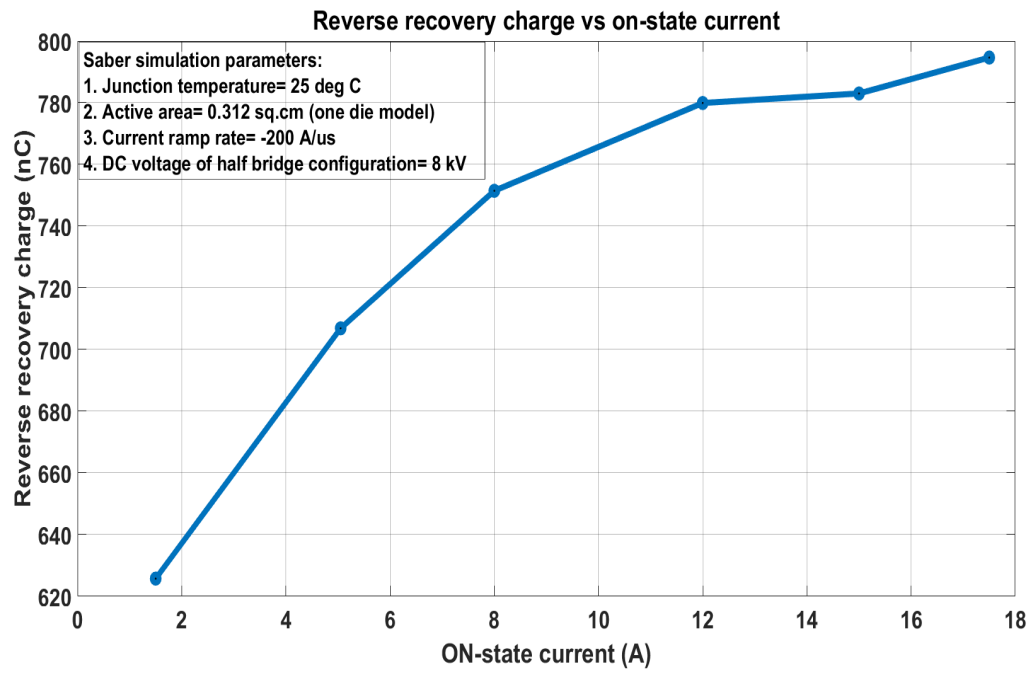


Figure 2.34 Q_{rr} as a function of internal diode ON-State current: Saber results

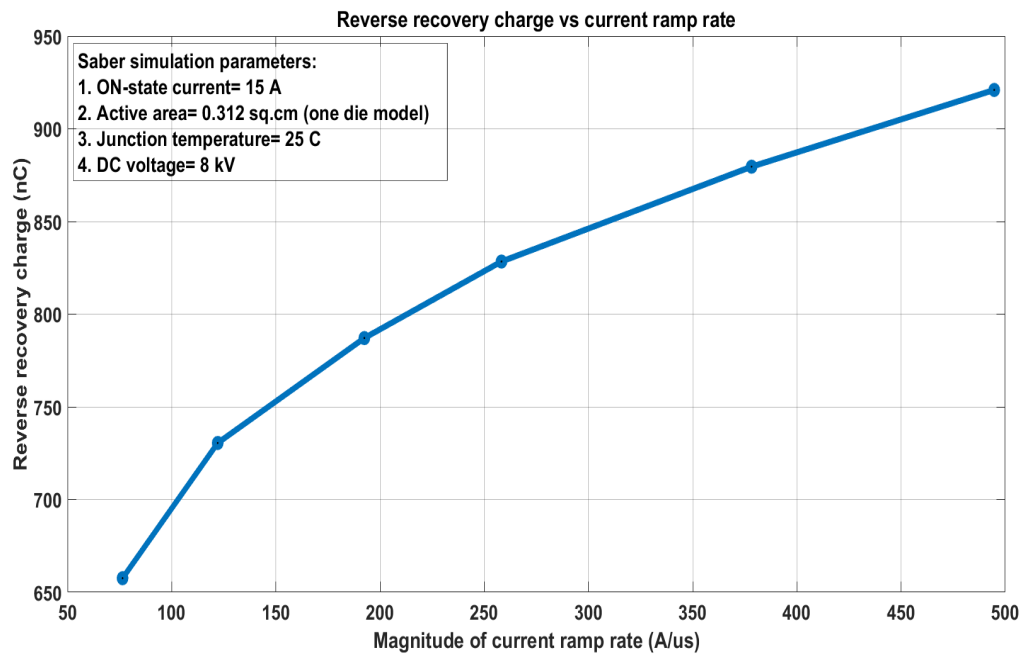


Figure 2.35 Q_{rr} as a function of di/dt : Saber results

CHAPTER

3

SWITCHING LOSSES AND TRANSITION TIMES

Characterizing switching behaviour in terms of transition times and switching losses is important for understanding the suitable operating frequency and temperature rise of the device when used in power electronic converters. This thesis work studies the detailed switching behaviour of the Gen-3 model with three different cases.

Case I: The 10 kV Gen-3 device model is used in a double pulse circuit with an ideal power diode model available in Saber. When the device under test (DUT) is turned-off, the inductor current freewheels through this diode.

Case II: The same model is utilized with just a resistive load instead of the inductor as used in the previous case. There is no requirement of a freewheeling diode in this case.

Case III: The 10 kV 18 A Gen-3 MOSFET model is then used in a half bridge configuration in a double pulse circuit by utilizing the internal body diode of the device for inductor freewheeling action.

All three cases would be useful in predicting the switching behaviour of the device and can be taken as a basis to compute losses (hard commutation). The turn-on and turn-off delay times, switching times and energy loss are consolidated and plotted as a function of gate resistance to finally compare the results obtained from the three cases.

The following terms are used throughout this section and later in this thesis and thus the defini-

tions of each of the terms are revisited for clarity:

Rise time (t_r): Time interval elapsed between the applied drain-to-source voltage (V_{DS}) falling from 90% to 10% of its value. The time interval is computed during the turn-on transition of the device under test (DUT).

Fall time (t_f): Time interval elapsed between the drain-to-source voltage (V_{DS}) rising from 10% of the applied voltage to 90% of the value. This is computed during the turn-off transition of the device under test (DUT).

Turn-on delay time ($t_{d,on}$): Time interval elapsed between 10% of gate-to-source voltage (V_{GS}) rising from zero and 90% of drain-to-source voltage (V_{DS}) falling from applied voltage to on-state value.

Turn-off delay time ($t_{d,off}$): Time interval elapsed between 10% of drain-to-source voltage (V_{DS}) rising from on-state value and 90% of the applied gate-to-source voltage (V_{GS}).

3.1 Case I

Saber simulation with inductive load and external diode:

The need to study the losses of this configuration stems from the fact that the Gen-3 device may be used in conjunction with an external diode in applications that require lower switching losses. As will be explained in case III, when the body diode of the 10 kV MOSFET model is used for the freewheeling action of inductor current, the bottom device (DUT) experiences additional losses during its turn-on transition due to diode reverse recovery. By using a inbuilt power diode available in Saber, this phenomenon is substantially reduced if not completely eliminated. Thus, the values obtained in this case will resemble more with that of the ideal case (resistive switching). The junction temperature is maintained at 25°C and the active area of the device used in the simulation is 0.312 cm² which can handle an ON-state current of 18 A. The losses are measured for V_{DS} at 8 kV and the device current I_D at 10 A. The gate resistance is varied from 2.2 Ω to 100 Ω. From the following plot, it is observed that the turn-on losses vary from 2 mJ to about 22 mJ when the gate resistance is increased. The turn-off losses, on the other hand, increases with a lower slope with gate resistance. The higher value of the turn-on losses can be attributed to the reverse recovery of the external power diode. The total losses (summation of the turn-on and turn-off) in this device is plotted in green in the same graph (refer Figure 3.2). The simulation conditions are annotated in the plot.

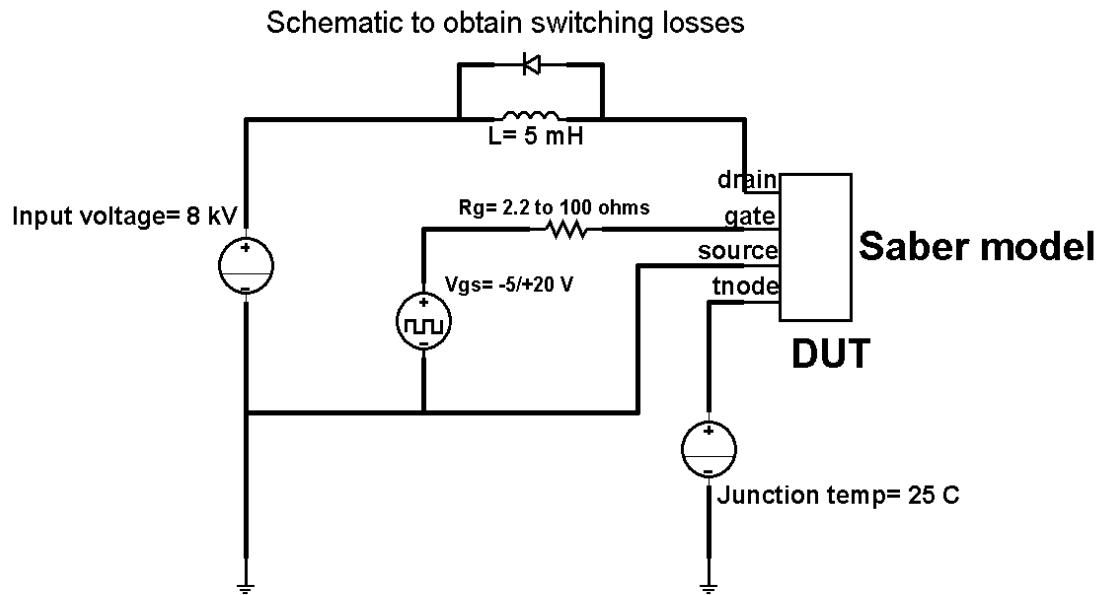


Figure 3.1 Switching loss schematic with inductive load and external diode

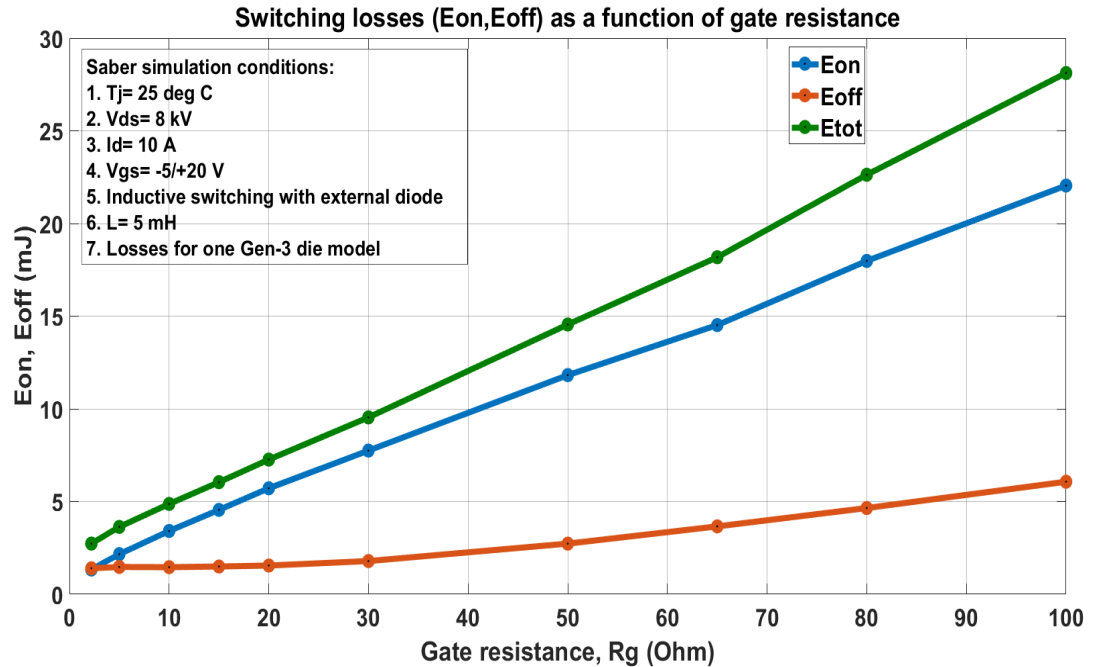


Figure 3.2 Switching losses with inductive load and external diode

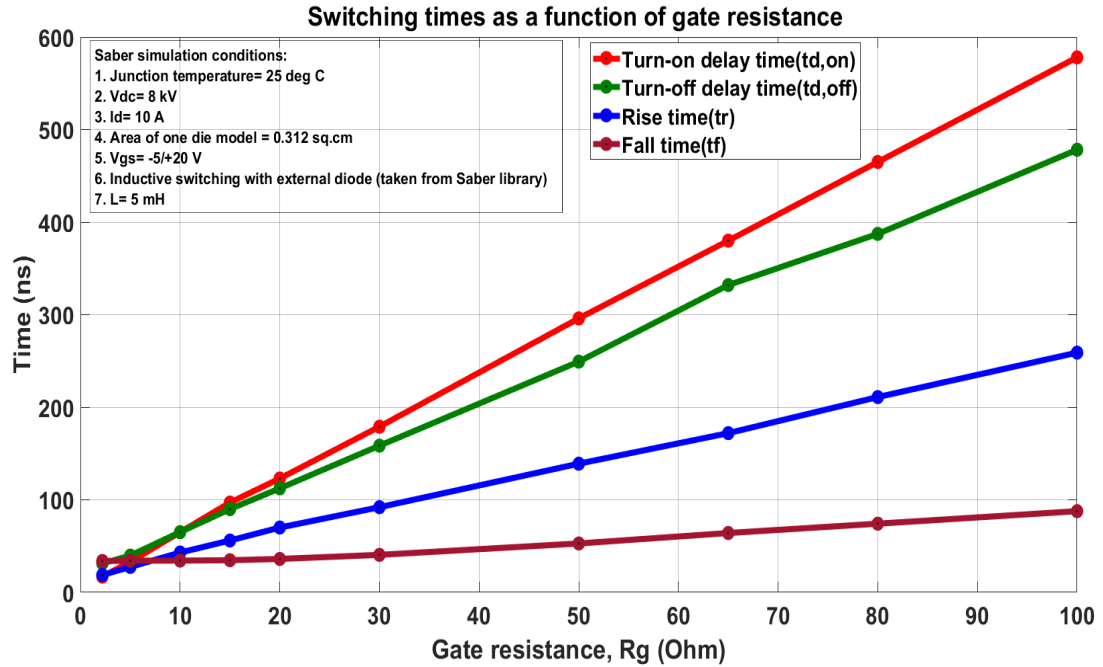


Figure 3.3 Switching times with inductive load and external diode

The above graph shows the transition times of the device model when used in conjunction with an external diode. The obtained values of rise, fall, turn-on delay and turn-off delay times are plotted with respect to gate resistance. As can be predicted, the fastest transition times in the order of tens of nanoseconds can be observed when the gate resistance is the least (2.2Ω). The net RC time constant in the gate circuit reduces for lower external resistances. However, when the value is increased to more than 20Ω , the delay times become higher than 100 ns. Correlation between the switching times and the losses will be deduced in the following subsections once the results for the other cases are also presented.

3.2 Case II

Saber simulation with resistive load

The simulation is repeated with a resistive load for the same operating voltage and current values. Even though the 10 kV device would mostly be used for driving inductive loads like a motor, they might also be used in situations where the load is purely resistive. The switching losses and transients would vary substantially under such circumstances and the circuit designer must be equipped with the changes in the losses to predict the system behaviour.

In this case, the phenomenon of reverse recovery is completely eliminated as there is no involve-

ment of a power diode [1]. Thus, the switching losses are expected to be much lower during turn-on. As there are no major changes during turn-off, it can be predicted that the losses should remain more or less the same compared to case I. The Saber simulation schematic for this case is shown below:

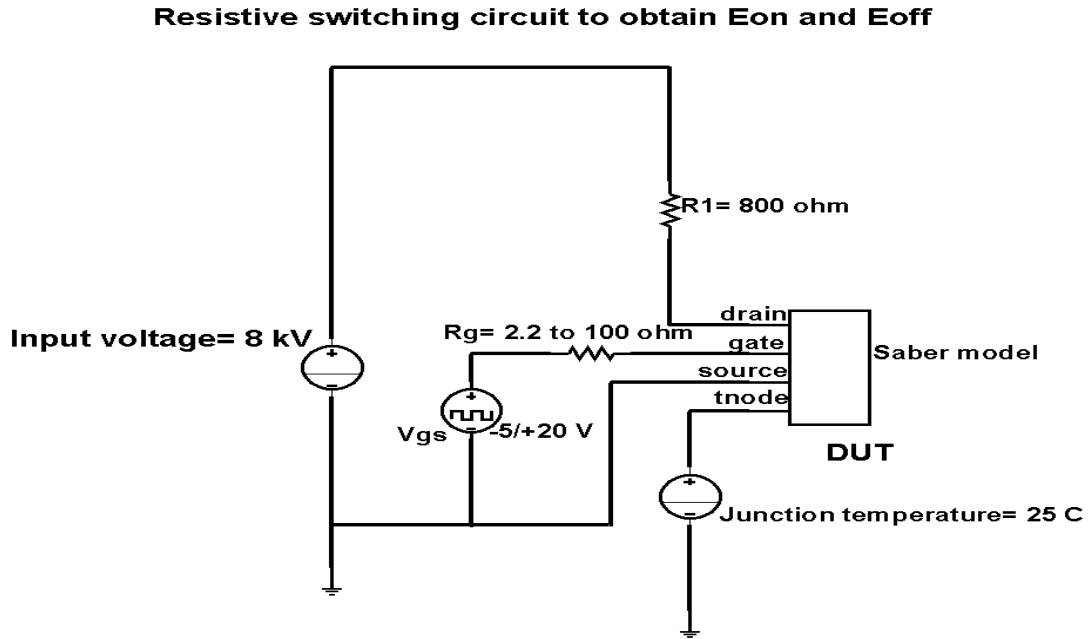


Figure 3.4 Switching loss schematic with resistive load

The value of the series resistance is decided by the simple division of the applied voltage and the required current of interest in the model during its on state. The values of turn-on (E_{ON}), turn-off (E_{OFF}) and total switching losses (E_{TOT}) are shown in the plot below:

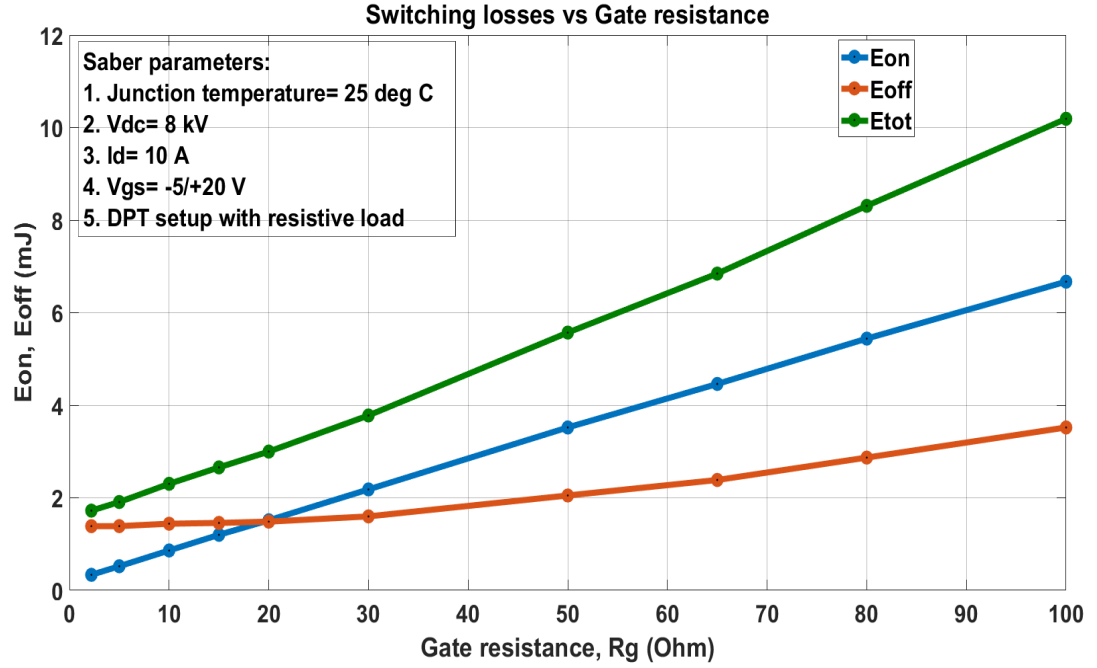


Figure 3.5 Switching losses with resistive load

It is apparent that the turn-on losses have reduced significantly compared to the previous case. For instance, the total switching energy loss when the gate resistance is 20Ω is about 3 mJ compared to 7.5 mJ in the previous case. The turn-on losses have reduced by more than half the value due to the complete elimination of diode reverse recovery. In terms of the turn-off losses in particular, the values have decreased only by a small fraction compared to case I (as expected).

The switching transient times as a function of R_g is shown in Figure 3.6. Comparing the rise and fall times, it can be seen that the corresponding values are higher for the resistive load case. This is because the DPT circuit with inductive load has to constantly support 10 A either in the main device or the diode. During transitions, the current has to be shuttled between the device and the diode making the rise and fall times comparatively less with respect to the resistive load case. Current in this circuit exists only when the main device is ON and not otherwise. On the other hand, the turn-on delay time for the inductive case is higher than the resistive case. The value is determined by the time elapsed between 10 % V_{GS} and 90 % V_{DS} of the main device. When a power diode is used across the inductor, it cannot block any voltage until it is depleted of all its charge that was accumulated during its conduction. This extra delay is not present in the resistive switching case, thus making the turn-on delay time lesser when compared to the inductive load case. The turn-off delay fairly remains the same for both the cases.

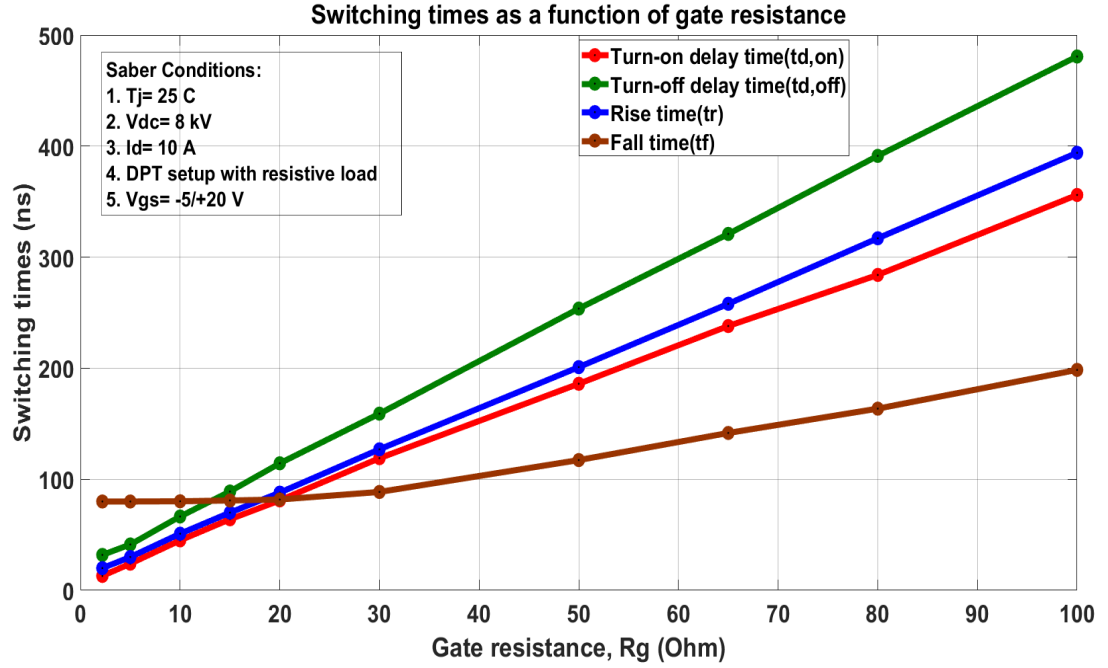


Figure 3.6 Switching times with resistive load

3.3 Case III

Saber simulation with internal body diode of Gen-3 MOSFET model:

In the final case, the Gen-3 device model is used in a half bridge configuration utilizing the internal body diode of the model. This configuration is the most important case, as this would have direct applications in multiple converters. The turn-on and turn-off energy losses are obtained for this case and compared to the previous two cases. The schematic used for Saber simulation is shown in Figure 3.7. The gate-to-source voltage of top device is held at -5 V to suppress the conduction of the MOSFET channel during its operation. The direction of current conduction would be from source to drain in the top device during freewheeling which aligns with the internal body diode. The junction temperature is maintained at 25°C for the calculation of losses.

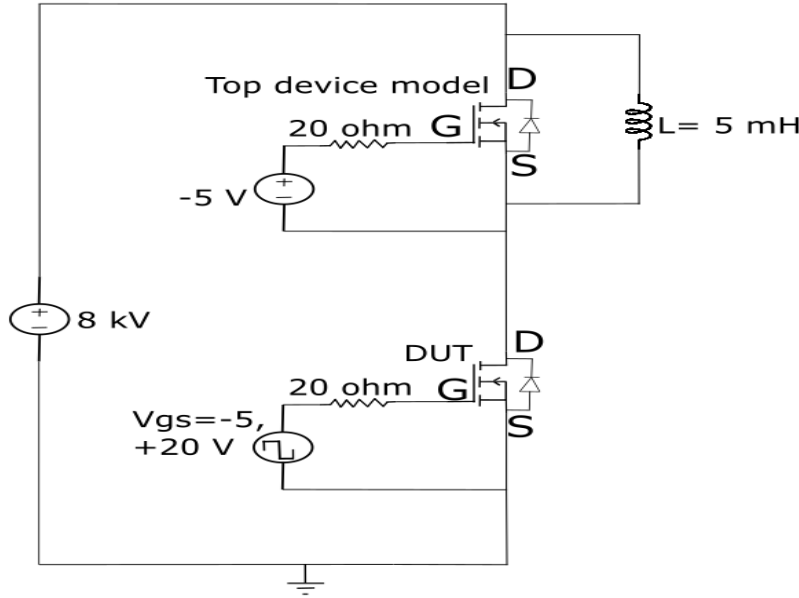


Figure 3.7 Switching loss schematic with half bridge configuration

Saber plots of the currents and voltages across the DUT during the first and the second pulse are shown. From the plots, it can be understood that during turn-on, the accumulated charge in the internal body diode model adds to the on-state current of 10 A to produce the overshoot. The top device (acting like a diode) cannot block any voltage until all of its charge is removed. The time duration for this process with the gate resistance of 20 Ω is approximately 114 ns. Once the remaining charge is completely removed from the top device (diode), it can block voltage across its terminals. At the end of time t_1 , both the voltage and current in the bottom device model are at their maximum values producing high turn-on losses. After time t_1 , the drain-to-source voltage of the bottom device (DUT) drops from the supply voltage to the small on-state drop value. The area under the product of current and voltage waveforms is the total energy lost during turn-on. The rates of current rise and voltage fall are in the order of hundreds of amperes per microsecond and tens of kilovolts per microsecond respectively. In the turn-off process, the voltage rise and current fall happen simultaneously as shown in the plot (Figure 3.8). This process does not vary much when compared to cases (I) and (II) and thus the losses remain fairly constant. The turn-off losses only vary within a small bracket of about 30% but the turn-on losses vary as much as 4x times from one case to another. In this case, E_{ON} at 20 Ω gate resistance is 16.525 mJ (see Figure 3.10) compared to 1.75 mJ for the resistive switching case and 6 mJ for the external diode case. The total switching power loss of the device with $R_G = 20 \Omega$ when operated at 20 kHz with V_{DC} of 8 kV and I_D of 10 A is:

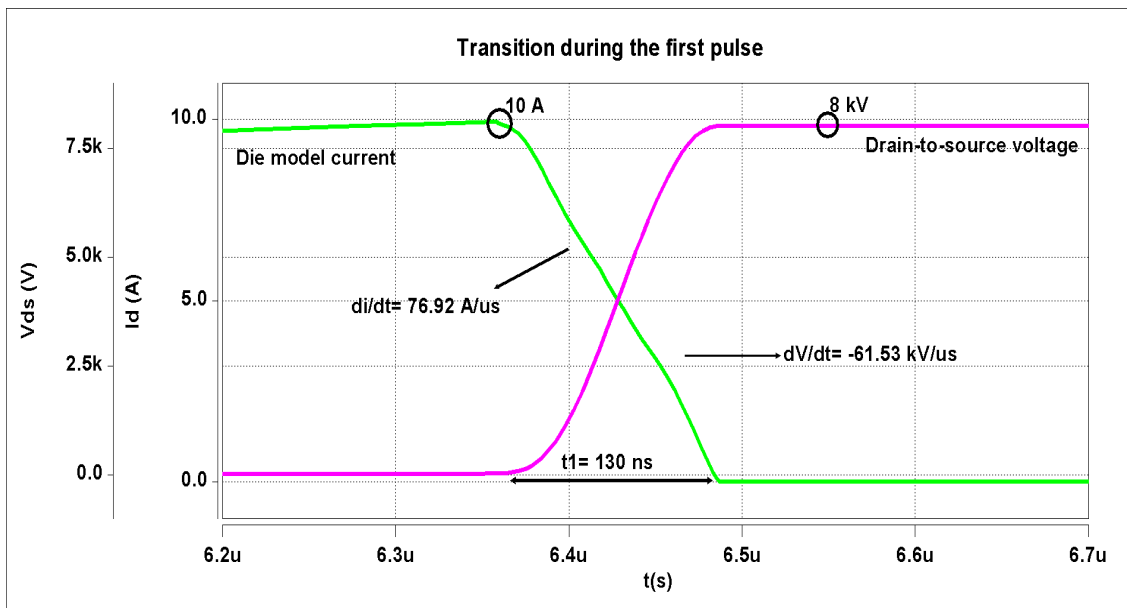


Figure 3.8 Switching voltage and current- with internal body diode (1^{st} pulse)

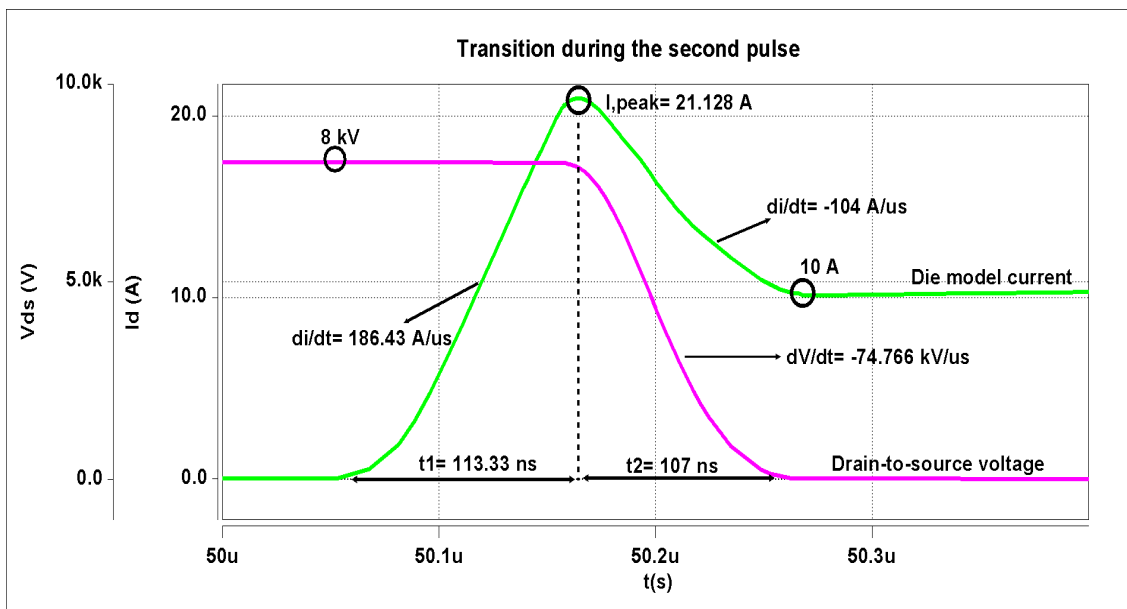


Figure 3.9 Switching voltage and current- with internal body diode (2^{nd} pulse)

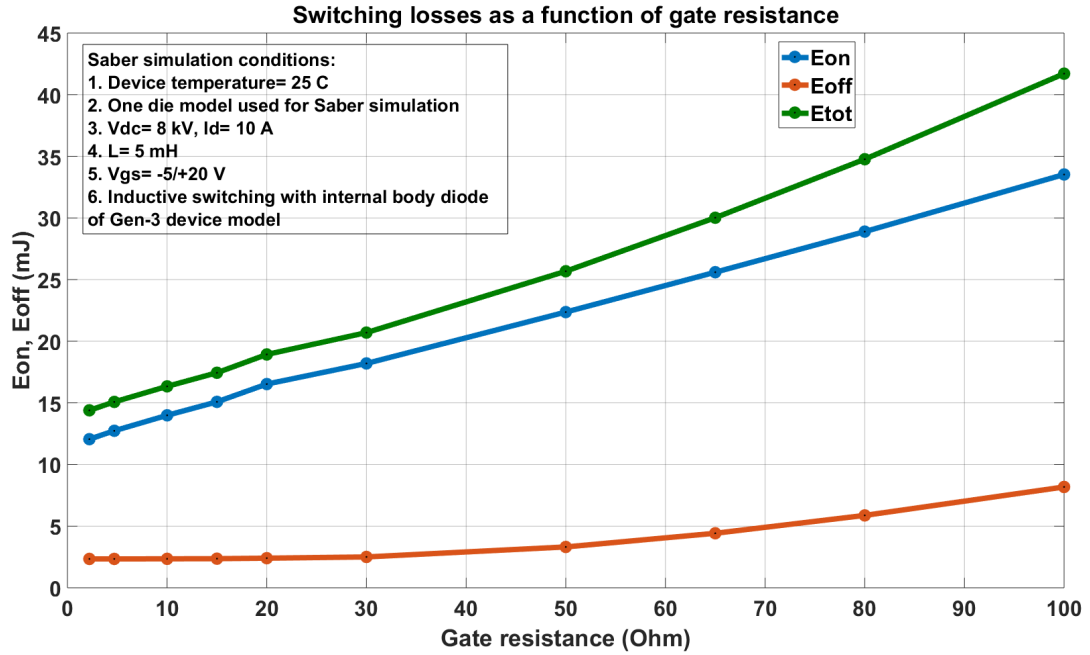


Figure 3.10 Switching Losses in half-bridge configuration

$$\begin{aligned}
 P_{sw} &= (E_{ON} + E_{OFF}) \times frequency \\
 &= (16.525 + 2.401)mJ \times 20kHz \\
 &= 378.52W
 \end{aligned}
 \tag{3.1}$$

From the plot of the different transition times obtained for this case, it can be observed that the values are very similar to the ones obtained in case (I). This is because both of the networks consist of an inductive clamped switching configuration thus producing comparable results. The rise and fall times for both of inductive loads are lower compared to the resistive load case. Again as explained above, the turn-on delay time is higher for both inductive clamped circuits when compared to the resistive load due to time elapsed for reverse recovery. It is also worthy to note that for the same value of turn-on current, the associated di/dt is also higher for inductive loads that incorporate an external diode/body diode compared to the resistive load. In all the three cases, the turn-off delay time fairly remains constant.

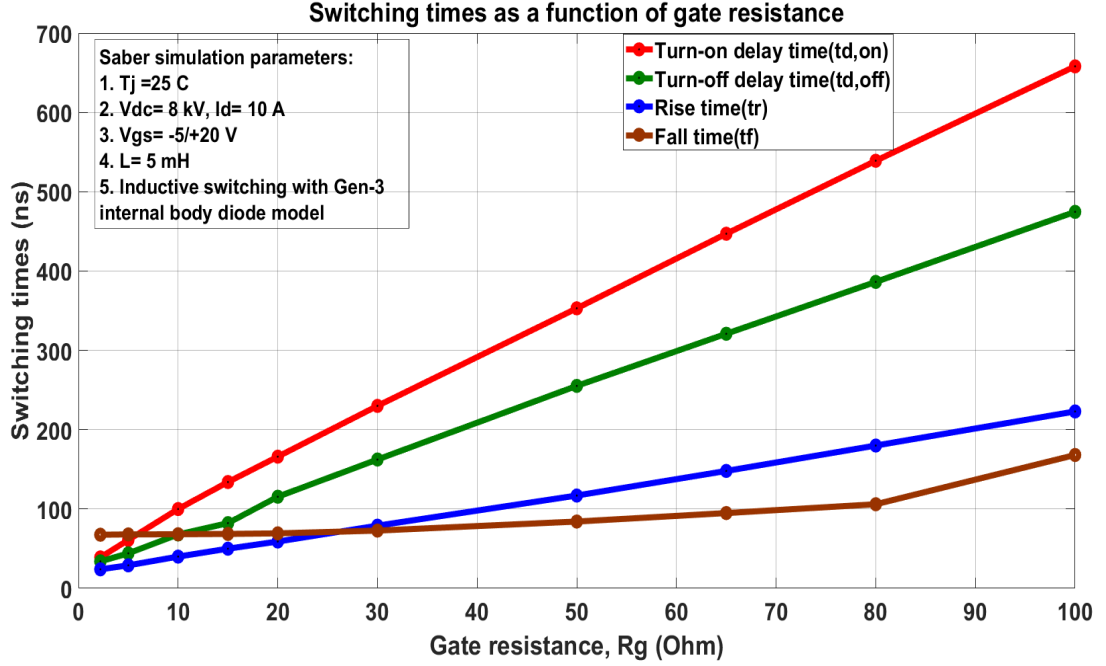


Figure 3.11 Switching times with the half bridge configuration of internal body diode

The half bridge configuration can also be used in understanding the influence of the body diode in shaping the losses and switching transients of the Gen-3 10 kV MOSFET. For each value of the gate resistance, the value of the reverse recovery time, total recovered charge and magnitude of the peak reverse current are plotted below for analysis (refer Figure 3.12):

The y axis on the left shows the values of the peak reverse currents and the one on the right plots both the recovered charge in nanocoulombs and reverse recovery time in nanoseconds. When gate resistance is minimum at $2.2\ \Omega$, the peak reverse current in the diode model is about 30 A for an on-state current of 10 A (3x times higher). The time elapsed between the two zero crossings of the current referred to as the recovery time is 65 ns. The total charge that has to be removed from the internal diode before it can attain blocking state is 937 nC. When $R_g = 20\ \Omega$, the corresponding values of I_{peak} , Q_{rr} and t_{rr} are 10.8 A, 764 nC and 155 ns respectively. The peak reverse current decreases with increase in gate resistance and the reverse recovery time increases with gate resistance. The overall removed charge decreased from 937 nC to 637 nC as the gate resistance is increased from $2.2\ \Omega$ to $100\ \Omega$. All the above reported values are for the dc bus voltage of 8 kV and ON-state current of 10 A.

This section of the thesis analysed the complete switching behaviour of the 10 kV 18 A Gen-3 die model in Saber. The important conclusion is that the characteristics are different under varying circuit topologies and that the internal body diode alters the transients in half bridge arrangement.

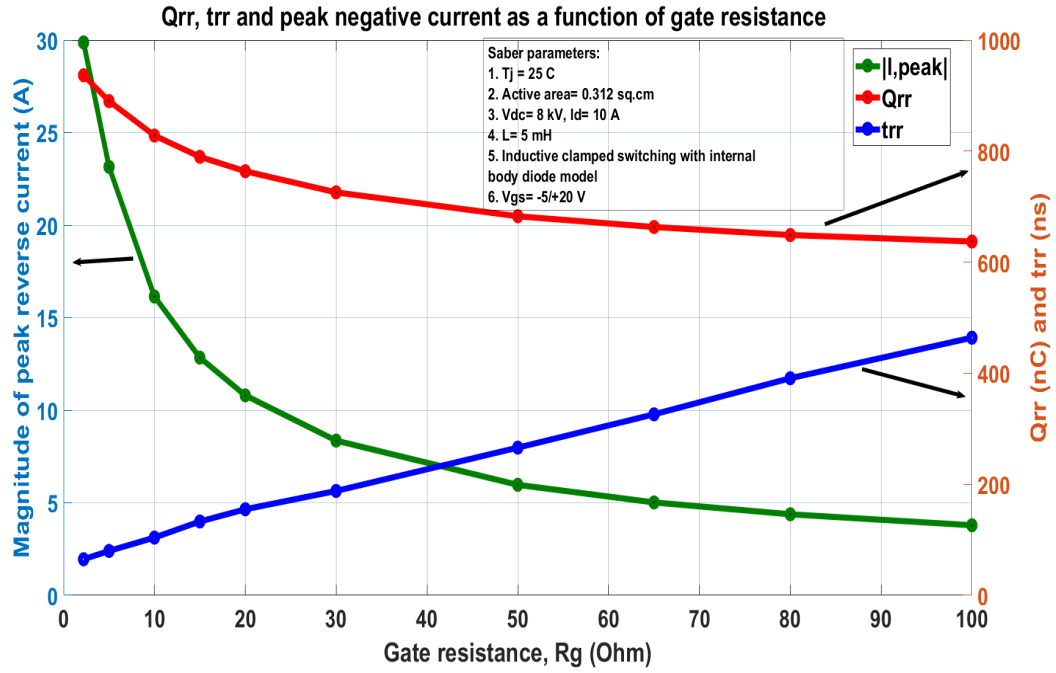


Figure 3.12 Q_{rr} and t_{rr} as a function of gate resistance

The effect of gate resistance is studied thoroughly in this section which can be taken as a basis for using appropriate values in different converters. The dV/dt and di/dt are in the range of several tens of $kV/\mu s$ and hundreds of $A/\mu s$. In the next chapter, series connection of 10 kV Gen-3 device models will be analysed in Saber with an added balancing snubber to mitigate problems related to voltage mismatch.

CHAPTER

4

SERIES CONNECTION AND SNUBBER DESIGN

The main motivation to venture into series connection of SiC devices is to understand the capability of using these devices for medium voltage (MV) and high voltage (HV) applications. However, series connection is not very straightforward and comes with certain challenges that needs to be overcome. Mismatch in voltage sharing in these power devices can result when using a number of them in a power converter. Dynamic voltage mismatch is the unequal distribution of the DC bus voltage during the turn-on and turn-off transients of the MOSFETs. Static voltage mismatch is the difference in the blocking voltages of the devices during the OFF state. From the research done in several papers before [32], it can be understood that the static voltage mismatch mainly happens due to differences in the leakage current of the different MOSFET samples. Dynamic voltage mismatch happens due to:

- (1) Differences in the parasitic capacitance of the series devices which leads to changes in dV/dt and turn-off, turn-on times
- (2) Additional delay time caused by external gate drive circuitry.

Since this thesis is majorly concerned with emulating the characteristics and issues through **Saber simulation**, the analysis due to parameter variations cannot be carried out as the generic die model would not account for manufacturing tolerances. Taking this into consideration, the

analysis in this section becomes fairly limited in understanding the overall influence on the device performance due to the combination of the factors mentioned above. The following subsection will provide some insight on the effects of gate driver delays by conducting Saber simulations on series connected 10 kV Gen-3 MOSFET models. Following this, a brief description on optimization of passive snubber to decrease the voltage mismatch will also be presented.

4.0.1 Double Pulse Test

The schematic shown in Figure 4.1 uses 3 series connected Gen-3 device models in a basic double pulse tester and the circuit is simulated in Saber. A single die having an active area of 0.312 cm^2 is used for analysis. This can be extended to several dice in parallel. The input DC bus voltage is 20 kV and the current in the circuit is maintained at 12 A when the MOSFETs are hard commutated during the end of the first pulse. To understand the challenges of voltage mismatch in series connection, the gate drive pulses are intentionally delayed in tens of nanoseconds to observe the effect [25]. The gate-to-source voltage of the top three devices are clamped at -5 V so that the channel of the MOSFET model does not conduct anytime during circuit operation. The internal body diode of the Gen-3 model is used for the freewheeling of the inductor current. These devices essentially function as diodes and are named D1, D2, D3 (top to bottom). The gate-to-source voltages of the bottom 3 MOSFETs models are pulsed from -5 V to +20 V as depicted. The gate resistance used in this simulation is 20Ω . The bottom three devices function as switches and are named S1, S2, S3 (top to bottom). To illustrate the voltage mismatch, the gate pulses of S1 is delayed by 10 ns and the one of S2 is delayed by 5 ns with respect to that of S3. During the OFF state, the drain-to-source voltage of the device models S1, S2, S3 are 5233 V, 6646 V, 8142 V respectively (see Figure 4.2). The dynamic voltage is also not shared equally causing a change in the observed dV/dt . The voltage rise time is approximately 103 ns which means the associated voltage ramp rates are $50 \text{ kV}/\mu\text{s}$, $65 \text{ kV}/\mu\text{s}$ and $80 \text{ kV}/\mu\text{s}$ for S1, S2, S3 respectively. The static voltage imbalance in this case is 15% when expressed as a ratio of the DC bus voltage.

Another important challenge due to the voltage mismatch is that the switching loss in the devices would be unequal. The device with the higher blocking voltage would contribute more to the losses and this might lead to different junction temperatures of the MOSFET. This can possibly worsen the differences in the leakage current as it is a strong function of temperature. Voltage mismatch also increases when the delay in the gate pulses are increased.

The forth coming analysis considers gate driver delay to device model S2 alone while S1 and S3 are triggered without any delays in Saber. One possible way to mitigate the voltage mismatch is to design passive RC snubber circuits for the MOSFET models. Various trade-offs while picking an optimal snubber circuit to mitigate the mismatch will also be discussed.

Series Connected 10 kV Gen-3 models: Double pulse test

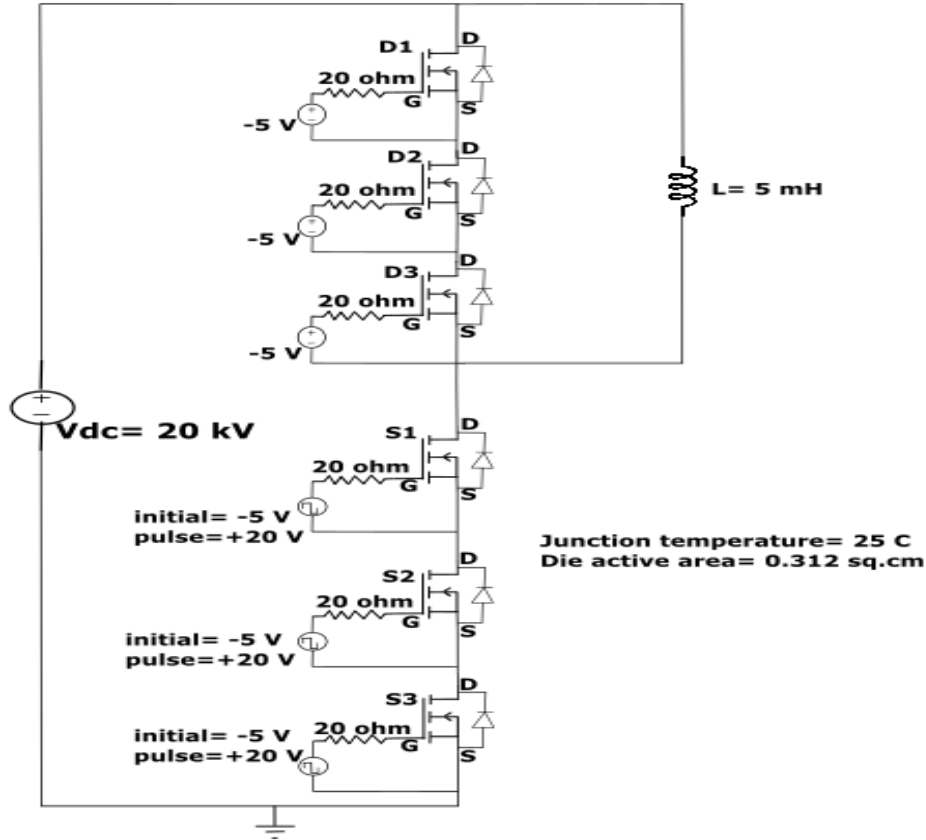


Figure 4.1 Double Pulse test- series connected Gen-3 MOSFET Saber models

The general structure of the snubber consists of a large resistance R_s , used for static voltage balancing, in parallel with a series combination of a capacitor (C_d) and resistor (R_d) mainly used for dynamic voltage matching. The general guidelines for deciding the values of R_d and C_d are given below [17]:

- (1) Ideally the maximum value of voltage unbalance has to be within 10% of the applied DC bus voltage.
- (2) The total switching losses should be as low as possible.

The snubber capacitor (C_d) should be selected such that it is much greater than the output capacitance (C_{oss}) of the MOSFET model. As seen in chapter 2, the value of the C_{oss} can range from 6 nF to tens of pF with changes in the drain-to-source voltage (V_{DS}). However, in high voltage applications, the value of C_{oss} for a Gen-3 device is only a few picofarads. Thus, a good point in starting to optimize C_d would be a few nanofarads. Putting a bigger capacitor across the Gen-3 MOSFET can reduce the associated dV/dt and subsequently reduce false triggering and shoot-

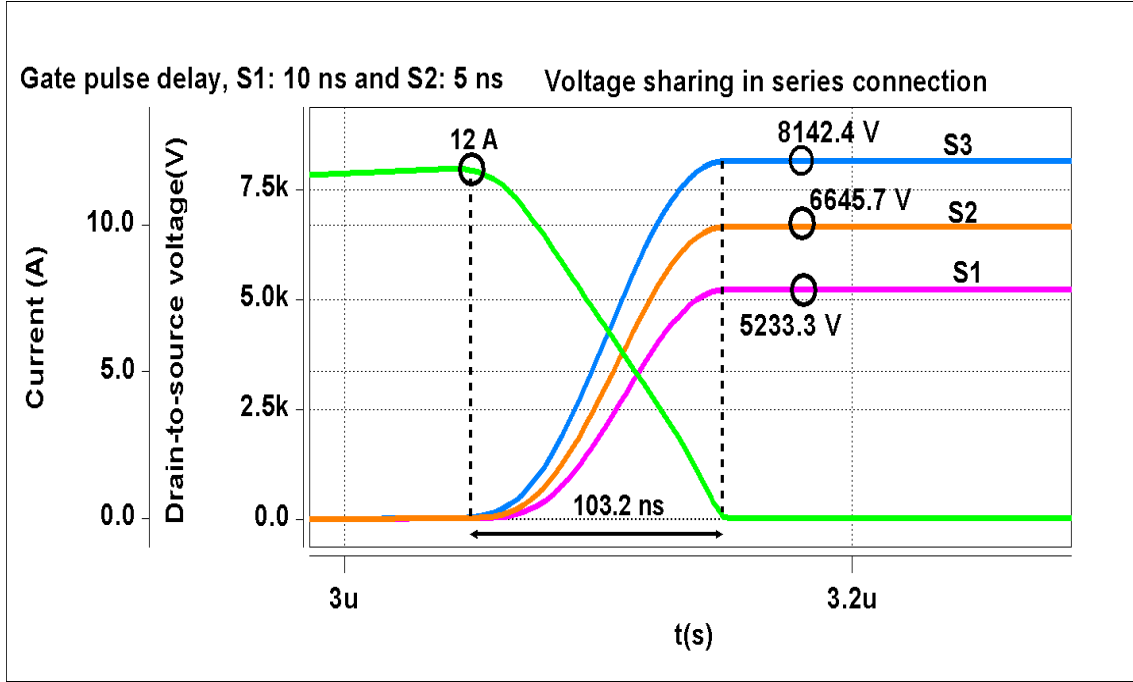


Figure 4.2 Voltage mismatch- DC bus voltage= 20 kV and current= 12 A

through fault in half bridge configuration [35]. The capacitance can decrease the turn-off switching losses by making the transition soft switched. However, the energy stored in the capacitor (C_d) would be released into the channel of the MOSFET during turn-on. This will increase the turn-on switching losses and the total switching losses can be higher or lower depending on the parameters of the balancing snubber. This calls for optimization of the capacitance value. The series resistance (R_d) decides the snubber time constant. The discharge time must be such that it is less than the on-time of the MOSFET so that the entire charge stored in C_d is discharged in the channel of the corresponding MOSFET before the next switching cycle. The parallel resistance of R_s makes the value of leakage current comparable between devices and hence helps in reducing the static voltage mismatch. An arbitrary choice of $R_s = 1 \text{ M}\Omega$, $R_d = 5 \text{ }\Omega$ and $C_d = 1 \text{ nF}$ is used as the starting point. Table 4.1 shows the Saber simulation results for this case and it can be seen that the voltage mismatch has substantially reduced. The delay time measured in nanoseconds is the intentional delay in the gate pulses of switch S2 with respect to that of switches S1 and S3. This is done to emulate the non-ideal sequential turn-on/turn-off commands from the gate driver circuit due to parasitics. The reported values of switching losses (last column of the table) is the sum of all the turn-on and turn-off losses of the three device models S1, S2, S3 when $V_{DC} = 20 \text{ kV}$ and $I_D = 12 \text{ A}$. The average switching loss per device can be obtained by dividing the values by three. The voltage mismatch is only 2% (expressed as ratio of the input voltage) when the delay is 50 ns as against 15% when the gate driver delay is

only 30 ns without any snubber. With such a design, the system would be able to tolerate sequential switching and share the blocking voltage without much mismatch for higher values of driver delays.

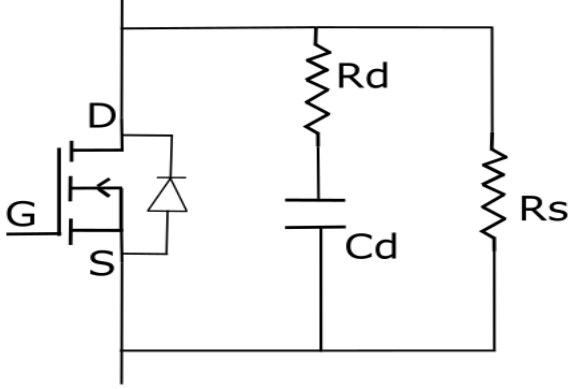


Figure 4.3 Balancing snubber circuit in parallel with the device model

An important detail to note in this analysis is that the switching losses are still not completely balanced in all the devices S1, S2, S3 and that C_d charges and discharges every cycle of the MOSFET switching. Since such a network typically has a voltage ramp rate in the order of tens of $\text{kV}/\mu\text{s}$, the voltage rise time would be a few hundred nanoseconds. This would be similar to the case of applying a step voltage to an RC series network every cycle and thus R_d controls the time constant for a fixed value of capacitance (C_d).

Table 4.1 Voltage mismatch with $R_d = 5\ \Omega$, $R_s = 1\ \text{M}\Omega$, $C_d = 1\ \text{nF}$, $R_G = 20\ \Omega$ (Saber results)

S.No	Delay time (ns)	V_{DS} (S1 and S3) (V)	V_{DS} (S2) (V)	Voltage unbalance (V)	E_{sw} (mJ) (Total)
1	5	6690.7	6641.6	49.1	248.22
2	10	6705.7	6611.6	94.1	251.52
3	20	6734.5	6554	180.5	239.336
4	30	6762.9	6497.2	265.7	236.156
5	40	6788.4	6446.2	342.2	233.849
6	50	6813.7	6395.7	418	230.451

Effect of changing R_d :

The total charge on the capacitance C_d is only dependent on the voltage across the terminals, in this case the drain-to-source voltage of S1, S2, S3. When R_d is reduced the same charge appears in the channel of the MOSFETs in a shorter time during turn-on. This means that the turn-on loss per device would increase when reducing the value of R_d for a fixed C_d . Since, the turn-off losses are much lower compared to the turn-on losses, the net device switching losses would increase. On the contrary, the losses in the snubber circuit would decrease as the value of R_d decreases. This again presents an optimization problem which would involve analysis across different device currents. However, this thesis only proposes a guideline in estimating the snubber parameters for a given operating point which can be easily extrapolated to other operating points.

Changing R_d without changing C_d has no effect on voltage sharing. It would thus be prudent to choose C_d first, which would fix the maximum voltage mismatch, before changing R_d for optimizing switching losses.

Effect of changing C_d :

C_d mainly controls the maximum voltage unbalance, turn-on switching losses of the MOSFETs and the associated dV/dt during transitions. Increasing C_d for a given value of R_d increases the switching losses but reduces the voltage mismatch. Also, the higher value of parallel capacitance helps in reducing dV/dt across the MOSFETs when used in power converters working at high switching frequencies.

In the upcoming discussion, three other snubber networks are proposed with the analysis of voltage sharing and circuit losses. The gate resistance for all the cases is $20\ \Omega$ and the DC bus voltage and die model current are 20 kV and 12 A. Table 4.2 lists the simulation results for $R_d = 1\ \Omega$, $R_s = 1\ M\Omega$ and $C_d = 1\ nF$. The voltage unbalance is comparable to table 4.1 but the total switching losses in the device models have increased slightly.

When the snubber capacitance is decreased, the value of voltage unbalance increases as expected. The total switching loss in the three devices S1, S2, S3 for the parameters shown in table 4.3 is about 139 mJ. This is a considerable reduction when C_d was 1 nF. Finally the value of R_d is changed to $5\ \Omega$ keeping the other parameters same. The voltage mismatch remained the same with a slight reduction in device switching loss.

The snubber circuits dissipate some power on their own which adds up to the net switching loss of the power circuit. The following figure shows the case of RC charging and discharging when the gate voltage of S2 is delayed by 40 ns (Figure 4.4). The direction and value of dV/dt directly corresponds to the capacitor current. The peak value of V_{DS} reaches 7250 V. When $C_d = 0.5\ nF$, the total charge flowing in and out every cycle is about $2.9\ \mu C$ as shown. The charge value becomes more relevant if the snubber is used across an entire module. In such a case, the value of C_d would be several times higher which would translate to higher losses. For instance, when the same circuit

Table 4.2 Voltage mismatch with $R_d=1\ \Omega$, $R_s=1\ \text{M}\Omega$, $C_d=1\ \text{nF}$, $R_G=20\ \Omega$ (Saber results)

S.No	Delay time (ns)	V_{DS} (S1 and S3) (V)	V_{DS} (S2) (V)	Voltage unbalance (V)	E_{sw} (mJ) (Total)
1	5	6691	6641.1	49.9	253.368
2	10	6705.7	6611.7	94	253.472
3	20	6734.3	6554.4	179.9	244.113
4	30	6761.2	6500.5	260.7	240.175
5	40	6786.8	6449.4	337.4	236.752
6	50	6812.4	6398.3	414.1	232.284

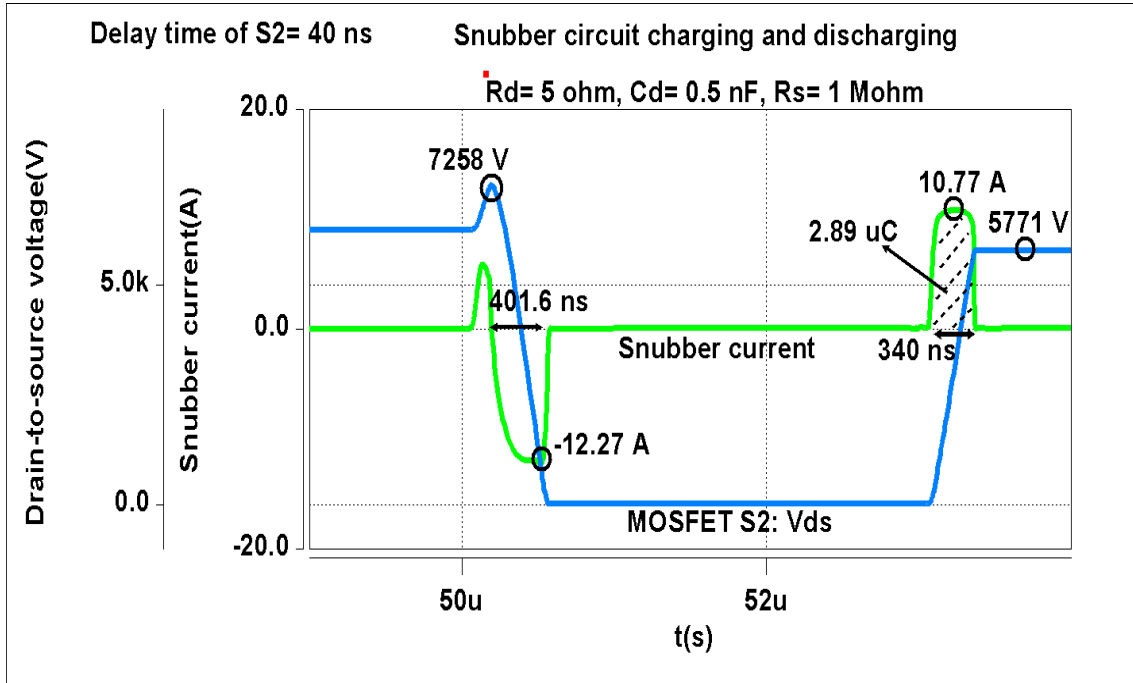
Table 4.3 Voltage mismatch with $R_d=1\ \Omega$, $R_s=1\ \text{M}\Omega$, $C_d=0.5\ \text{nF}$, $R_G=20\ \Omega$ (Saber results)

S.No	Delay time (ns)	V_{DS} (S1 and S3) (V)	V_{DS} (S2) (V)	Voltage unbalance (V)
1	5	6704.9	6612.4	92.5
2	10	6734.7	6552.8	181.9
3	20	6789.2	6443.9	345.3
4	30	6840.6	6341	499.6
5	40	6890.9	6240.4	650.5
6	50	6937.2	6147.8	789.4

Table 4.4 Snubber circuit losses (Saber results)

S.No	Snubber parameters	E_{sw} of snubber per cycle (mJ)
1	$R_d = 1 \Omega$, $C_d = 0.5 \text{ nF}$, $R_s = 1 \text{ M}\Omega$	0.067
2	$R_d = 5 \Omega$, $C_d = 0.5 \text{ nF}$, $R_s = 1 \text{ M}\Omega$	0.350
3	$R_d = 1 \Omega$, $C_d = 1 \text{ nF}$, $R_s = 1 \text{ M}\Omega$	0.150
3	$R_d = 5 \Omega$, $C_d = 1 \text{ nF}$, $R_s = 1 \text{ M}\Omega$	0.750

uses 10 kV 240 A SiC module, then the designed balancing capacitor would be 20 nF or even higher which would incur higher switching losses. The loss associated with just the balancing snubber network when the gate resistance is 20 Ω in shown in table 4.4.

**Figure 4.4** Snubber current and MOSFET S2 drain-to-source voltage

The dV/dt in the circuit before adding the compensating network is around 100 to 150 $\text{kV}/\mu\text{s}$. After adding the snubber network the dV/dt has dropped down to only 20 $\text{kV}/\mu\text{s}$. This reduces the likelihood of false triggering of complementary MOSFET when the DUT is fired with gate pulses. This avoids the problem related to shoot-through fault which means that the required dead time in

the half bridge topology can be reduced for more efficient operation. The graph shown in Figure 4.5 summarizes the voltage mismatch and losses for different snubber circuits. It can be inferred that there is a great deal of improvement in the voltage sharing at the cost of increased switching losses but this might serve as a requirement to use these devices to their full capacity in medium and high voltage applications.

So far the discussion was with respect to the impact of sequential turn-on and turn-off of multiple Gen-3 MOSFETs. This can be extended to parametric variation in one device with respect to the other in terms of leakage current, parasitic capacitance and other intrinsic quantities that characterize the device. The snubber would be able to mitigate voltage imbalance caused by these effects in addition to the gate driver delay. Since the analysis in this thesis is based on Saber modeling, it is not possible to study the other effects as the model for the Gen-3 device remains the same and does not account for changes from one device to another.

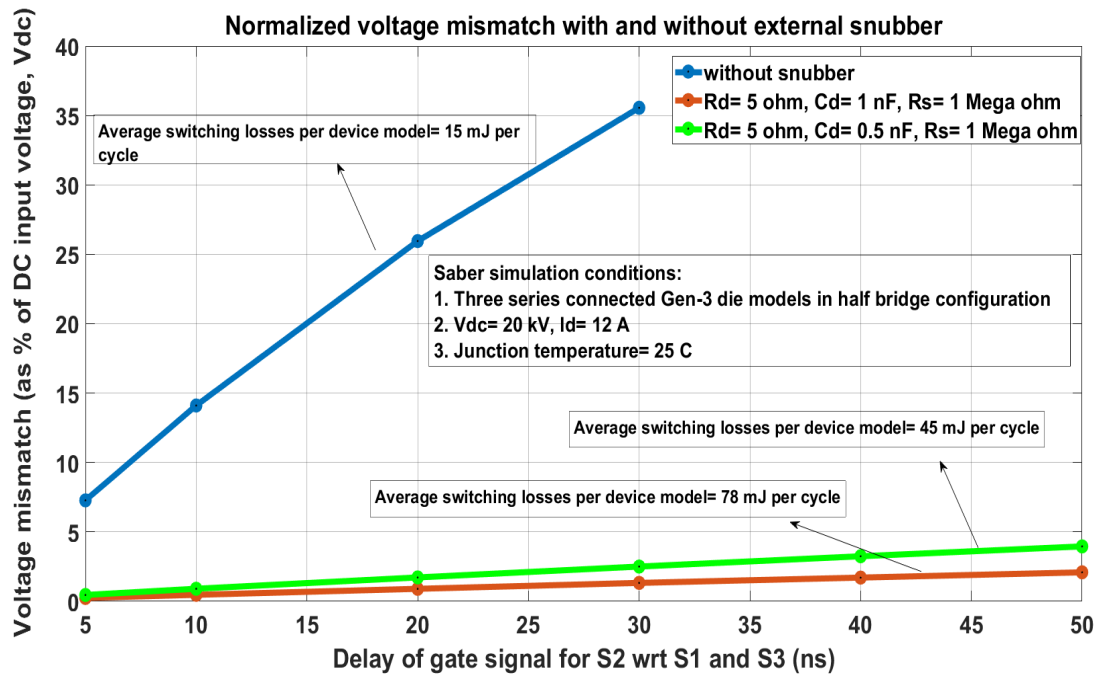


Figure 4.5 Voltage mismatch and switching losses with and without snubber

The next chapter talks about Saber Power MOSFET tool and how this very powerful feature of Saber software can be utilized in creating complete models of devices with characterization data. Since the discussion so far was based on obtaining curves of the die model of 10 kV 18 A Gen-3 device, the next logical progression would be to use the results in power converter simulation and compare

the features of the device model with existing commercial products in terms of performance at different switching frequencies.

CHAPTER

5

SABER POWER MOSFET TOOL

The curve fitting feature of Saber helps the designer to accurately predict the MOSFET behaviour in terms of switching energy losses, dV/dt 's and parasitic transients [20]. The behavioural model that is obtained can be used as an excellent starting point in predicting the efficiency of converters using the devices. The important characteristics/data required by the tool are listed below:

- (1) Output Characteristics (I_D vs V_{DS})
- (2) Transfer Characteristics (I_D vs V_{GS})
- (3) Parasitic capacitance (C_{iss} , C_{oss} and C_{rss})
- (4) Gate- charge characteristics (V_{GS} vs Q_G)
- (5) Internal diode I-V characteristics
- (6) Internal diode reverse recovery characteristics
- (7) Switching loss at one particular test point (V_{DS} and I_D)

A sample screen capture of the Saber tool is shown in the following figure (refer 5.1). The interface is user friendly and allows the curves listed above to be entered sequentially and optimized to get the best possible fit. The detailed information about the device curves can be obtained from the datasheet of the manufacturer. These plots can be imported into the Saber tool. The x and y axis of the plots need to be defined to be within the appropriate range. Data points can be traced out in each plot to make the model resemble the curves of the actual device. The parametric curve feature of the software allows the user to trace out multiple curves on the same graph to elucidate

differences as a function of temperature, V_{GS} , V_{DS} or any other parameter contributing to variations.

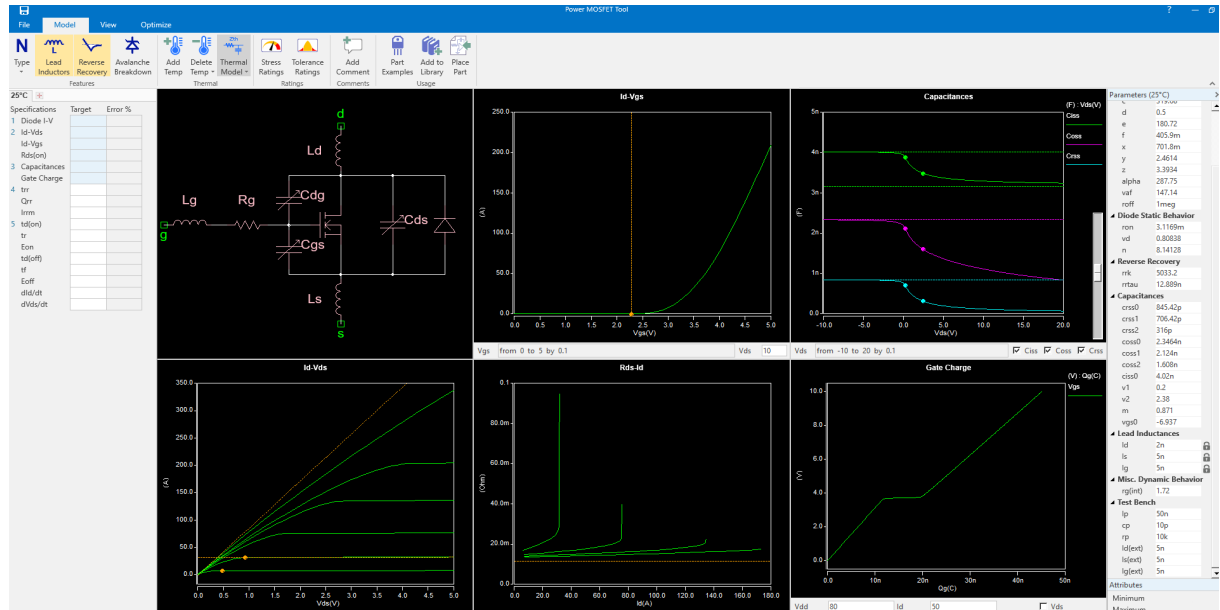


Figure 5.1 Saber Power MOSFET tool

Using the MOSFET tool, a model of the 3.3 kV 400 A SiC device is built in Saber. The static and the dynamic characterization data for this device is taken from the work done at the Centre for Power Electronics Systems in Virginia Tech [23]. The comparison on the accuracy of the model predicted by Saber with the hardware results obtained from the reference would serve as a good indication about the correctness of the model. Figure 5.2 shows the plots after all the characteristics are optimized. The maximum error encountered in this process is less than 10% and hence would be in good agreement if the data points are extrapolated. The final MOSFET model would have the characteristics of the channel modelled in the device while the parasitic inductance (causing ringing during fast switching) are modelled externally. The values of the parasitic lead inductance is a result of the curve fitting process. A good setup to validate the model created in Saber is to check switching losses as a function of all the possible currents and gate drive resistance from one point taken as a reference to build the Saber model.

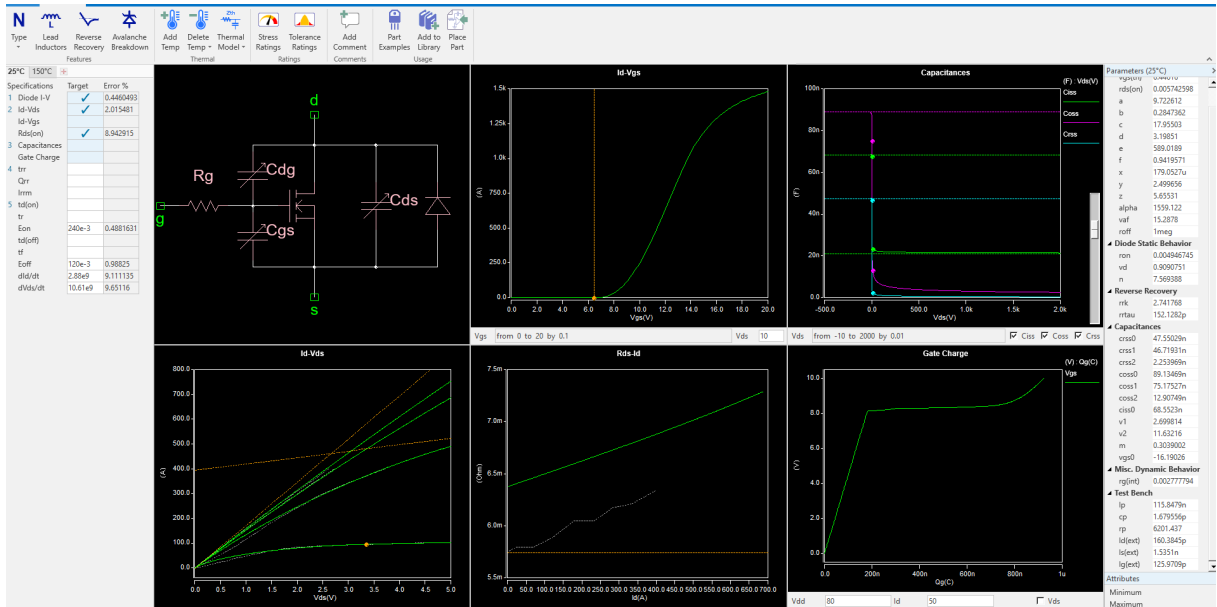


Figure 5.2 Optimized MOSFET tool- 3.3 kV 400 A device

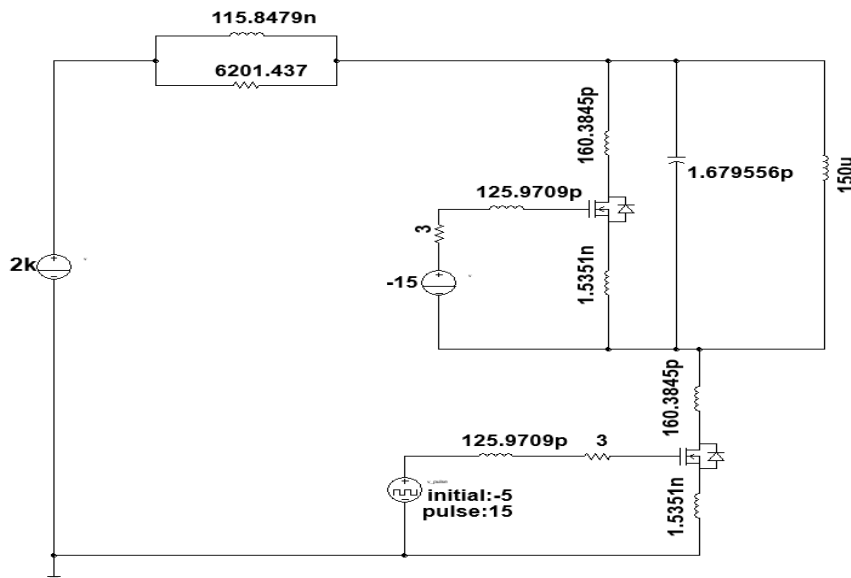


Figure 5.3 Double pulse setup- 3.3 kV 400 A SiC device in Saber

A double pulse test (DPT) is simulated with this device in a half bridge configuration (see Figure 5.3). The predicted parasitic inductance along with the capacitance are shown external to the MOSFET. C_{iss} , C_{oss} and C_{rss} are modelled internally. The gate pulse for the bottom model (device under test) is varied from -5 to +15 V and the V_{GS} for the top device is held at -15 V. The DC bus voltage is 2 kV and the current through the device is varied from 50 A to 400 A. The gate resistance is varied from 3 Ω to 5 Ω . The values of the actual results with the ones obtained from Saber are plotted in the same graph to understand the accuracy of the device model. From Figures 5.4 and 5.5, it can be seen that the model created by Saber predicts the losses in the device within 10% error. The deviation could be caused because the losses associated with the parasitic elements might differ with second order effects like ringing along the current and voltage transients. Nevertheless, the MOSFET tool can be a great starting point in understanding the device performance in power electronic converters. The 3.3 kV 400 A device can be used in similar applications of the 10 kV 240 A MOSFET if they are connected in series to increase the blocking capability. As an illustration, the next section would shed some light on a H bridge inverter using the Gen-3 device model and series connected 3.3 kV MOSFET models.

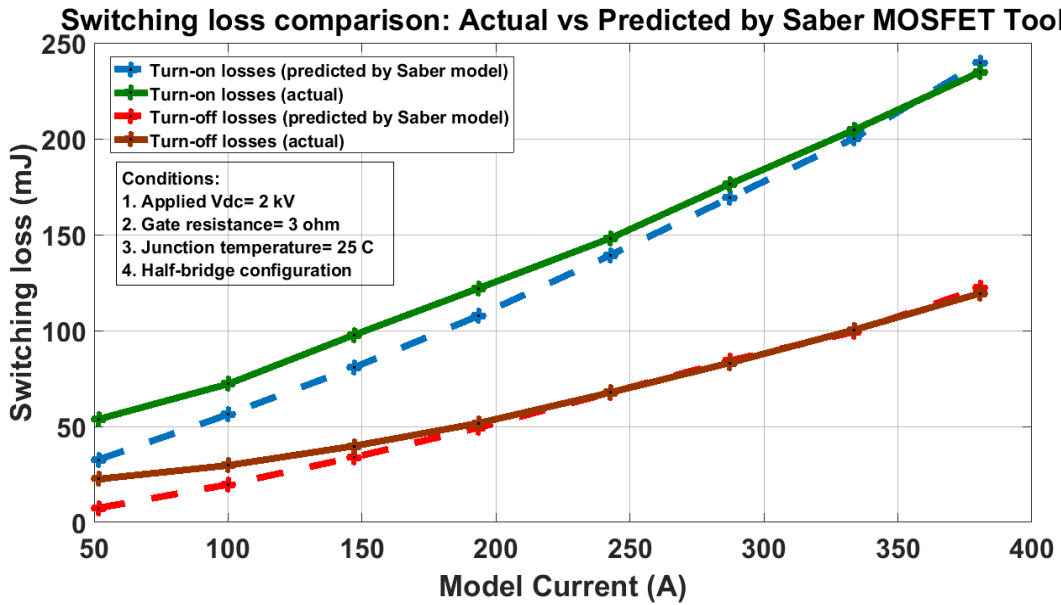


Figure 5.4 Switching loss comparison- gate resistance = 3 Ω

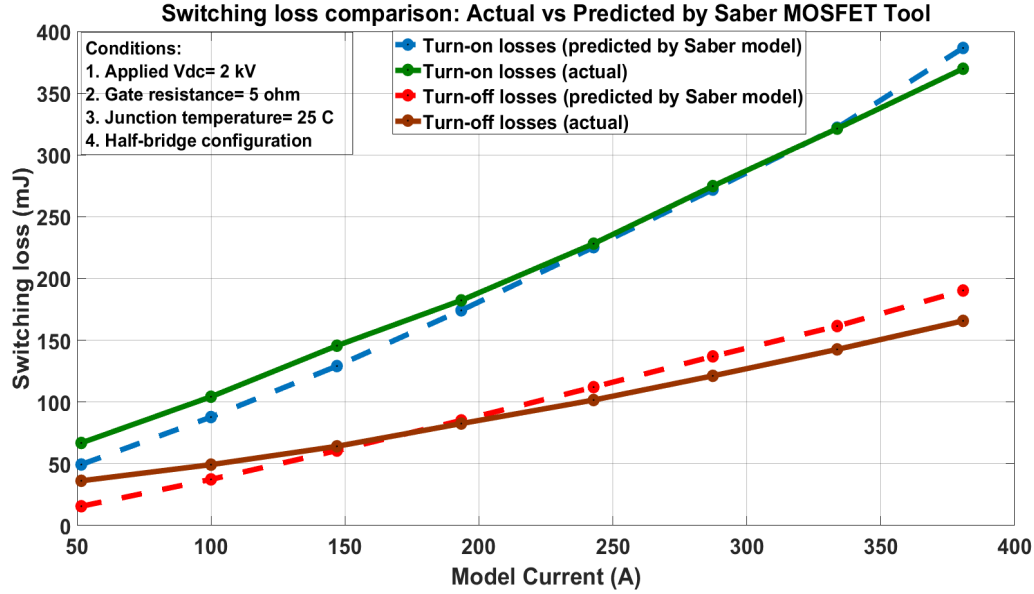


Figure 5.5 Switching loss comparison- gate resistance = 5Ω

5.0.1 Power Converter Simulation:

The input voltage of the H-bridge is maintained at 5 kV and the load is inductive with $R= 25\Omega$ and $L= 5$ mH. The switching frequency is varied from 1 kHz to 20 kHz and the gates are fired with SPWM signals. The modulation index is designed to be 0.8. Figure 5.6 shows the circuit used in Saber that implements two series connected 3.3 kV device models per switch. M11 and M12 are fired with the same gate pulses and are considered to be one switch from a circuit standpoint. Similarly M21, M22 form another switch and so on. The load current in this circuit is made to be around 80 A. The same simulations are carried out with the 10 kV Saber MOSFET model to study the trend of efficiency vs switching frequency. In this case M11, M12 are replaced with one 10 kV switch, similarly replacing the other devices. Figure 5.7 shows the trend and suggests that the 10 kV Gen-3 MOSFET fairs very well with the devices in market. The efficiency plot of the 10 kV Gen-3 model using 10Ω gate resistance is located between the series connected 3.3 kV models using 2Ω and 10Ω gate resistance.

In a similar manner, device models built using the characterization results can be compared across different power electronic converters in terms of their performance. Saber provides in depth analysis of conduction and switching losses in each switch and can predict possible voltage imbalances between series connected devices if the internal parameter variations are correctly modelled.

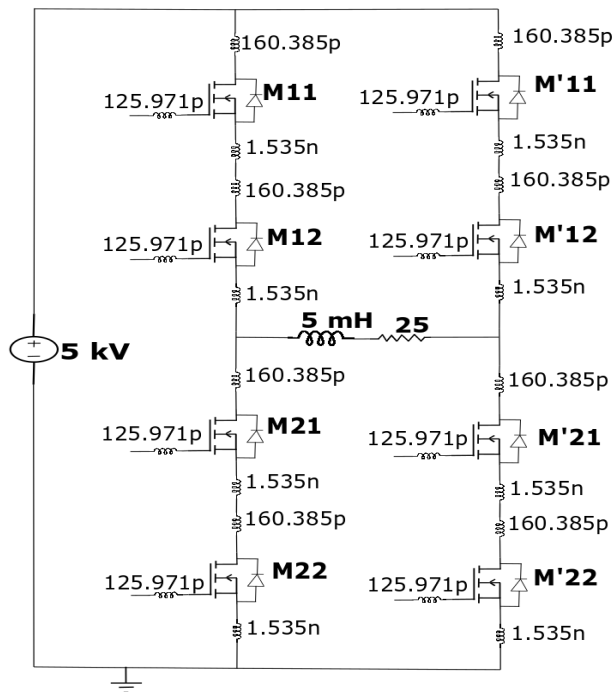


Figure 5.6 Circuit used in Saber simulation

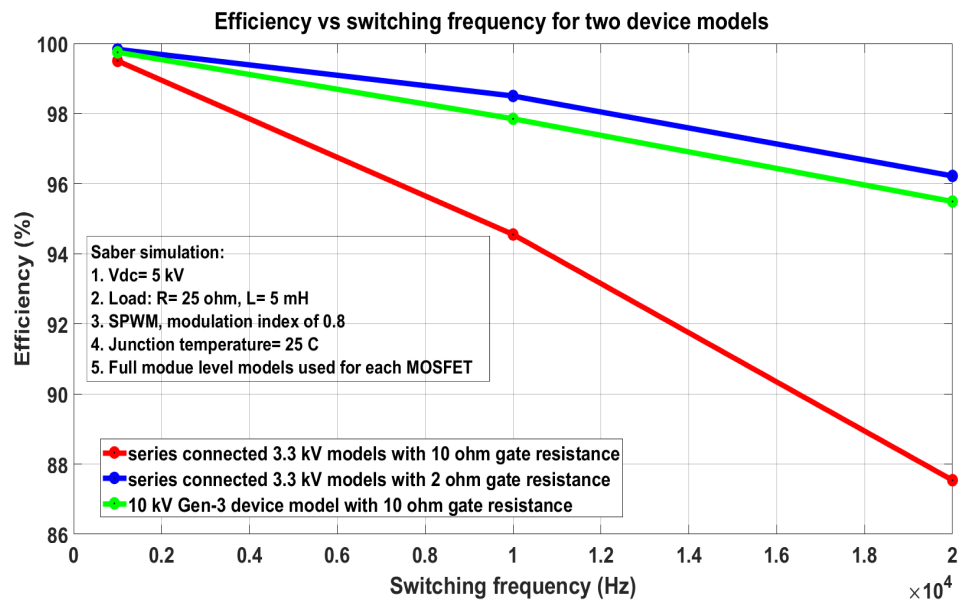


Figure 5.7 Efficiency vs switching frequency (comparison of device models)

CHAPTER

6

HARDWARE VALIDATION (10 KV GEN-3 SIC MOSFET)

Switching losses are obtained experimentally at 2 kV and 5.5 kV and compared with the values from Saber. The plots for E_{ON} and E_{OFF} are compared in the same graph to know the accuracy of the Saber model.

The hardware setup consists of the half-bridge configuration of the two Gen-3 10 kV dice. An air core inductor of 6.6 mH is used for the testing. This avoids problems related to core saturation which would have an influence on the test results. High voltage differential probes DP03-1K-50 are used to capture the drain-to-source voltage of each device. The bandwidth of the voltage probes is 75 MHz and any ringing/oscillation during the transition can be captured if it is within this frequency limit. High bandwidth Pearson current monitor 6600 is used to capture the current through the device under test (bottom device). The current monitor has a 3 dB bandwidth of 120 MHz and can measure currents till 40 A. This arrangement would thus provide a faithful replication of the device current. Teledyne LeCroy HDO6104 oscilloscope is used to observe the captured waveforms of the voltage and current. The experimental results are taken as csv files and plotted in MATLAB again for accurate calculation of the losses.

The gate drivers apply a voltage of +19 V during turn-on and -5 V during turn-off of the device under test (DUT). The top device in the setup is kept turned-off during the whole testing by applying a gate-to-source voltage of -5 V. Its internal body diode in the package is utilized during the

freewheeling time of inductor current. The experimental setup is shown in Figure 6.1. To simulate a similar condition in Saber, parasitic inductance between the source of DUT and the supply ground is taken as approximately 20 nH as it is connected with wire in the experimental setup.

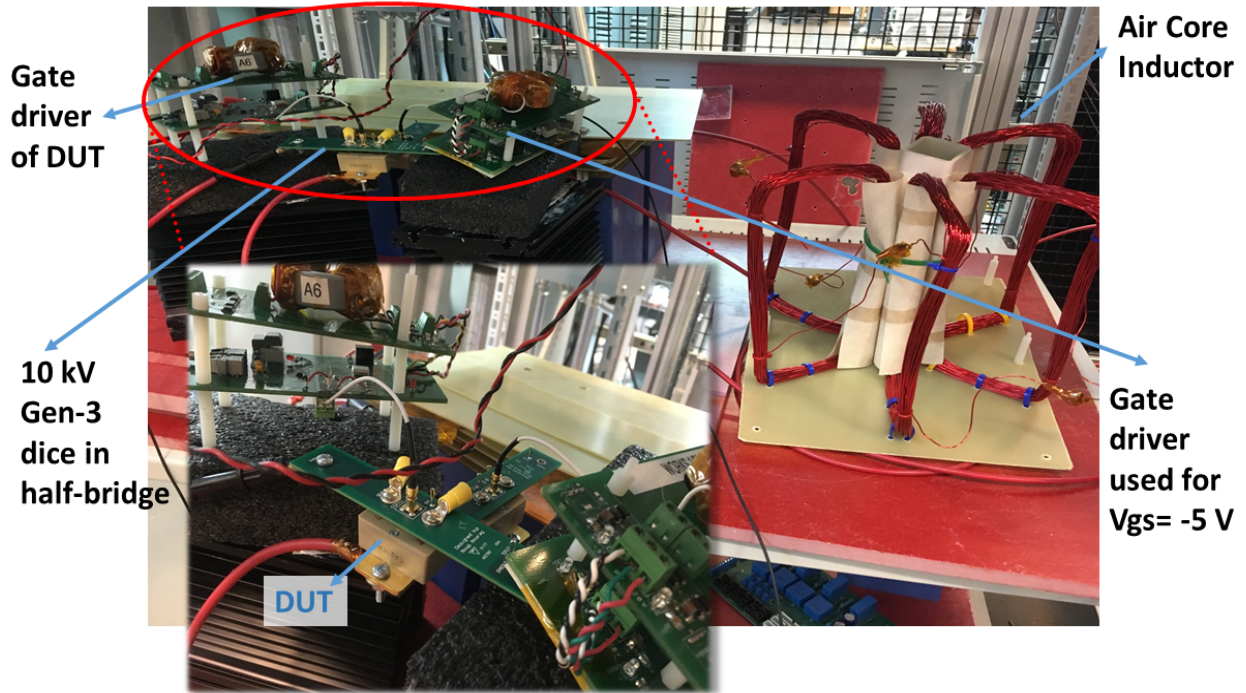


Figure 6.1 Double Pulse Test Setup

The dotted lines on the plots are the values obtained from Saber and the thick lines are the actual results from the experiment. The turn-on and turn-off gate resistance for both the top and the bottom device is 20 Ω . The gate-to-source voltage is varied from -5 V to +19 V in Saber. The turn-on and turn-off losses are obtained as a function of drain current as shown below (Figures 6.2, 6.3).

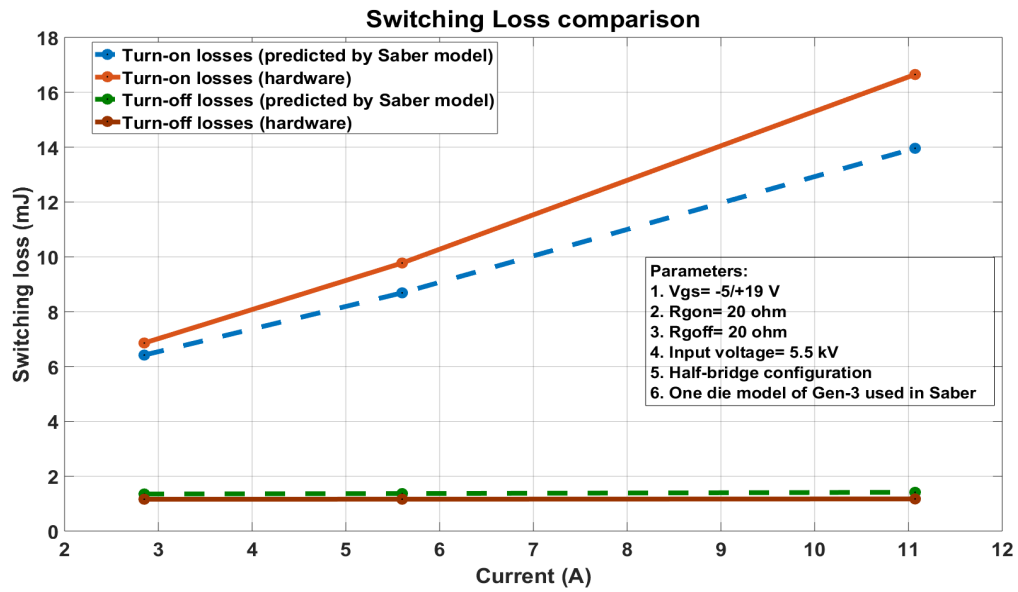


Figure 6.2 5.5 kV DC bus DPT setup- Experimental vs Saber results

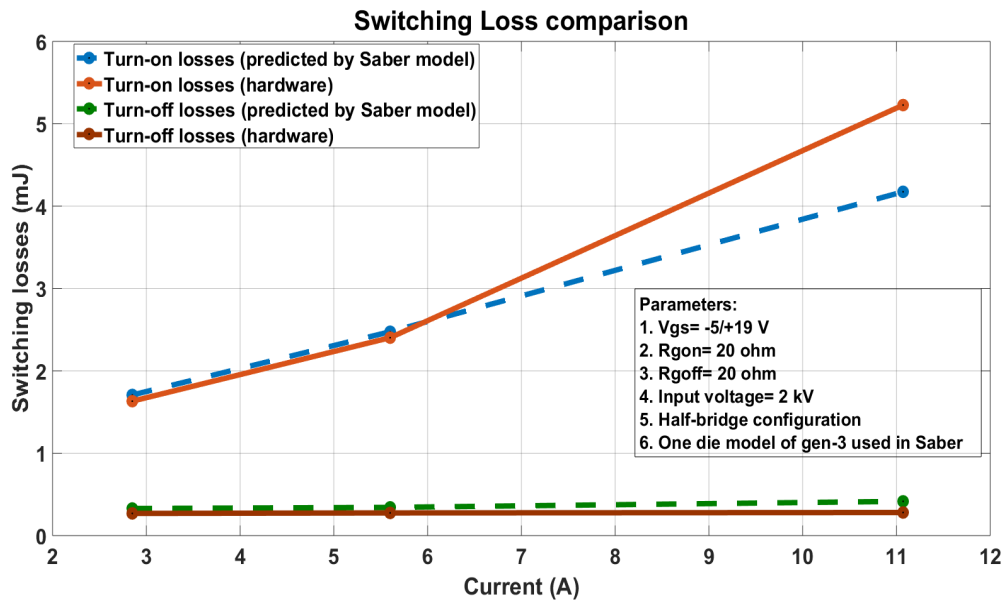


Figure 6.3 2 kV DC bus DPT setup- Experimental vs Saber results

To understand the cause of deviations between the Saber model and the hardware results, the switching transitions have to be studied. Consider the turn-off transition at 5.6 A when the input voltage is 5.5 kV. The blue line shows the drain-to-source voltage and the red line shows the plot of the device current. The green line shows the energy loss in the device calculated by integrating the product of instantaneous values of current and voltage. The ringing at the end of current turn-off is included when calculating the turn-off losses. The energy loss is computed by taking the difference of the two numbers annotated in the green line.

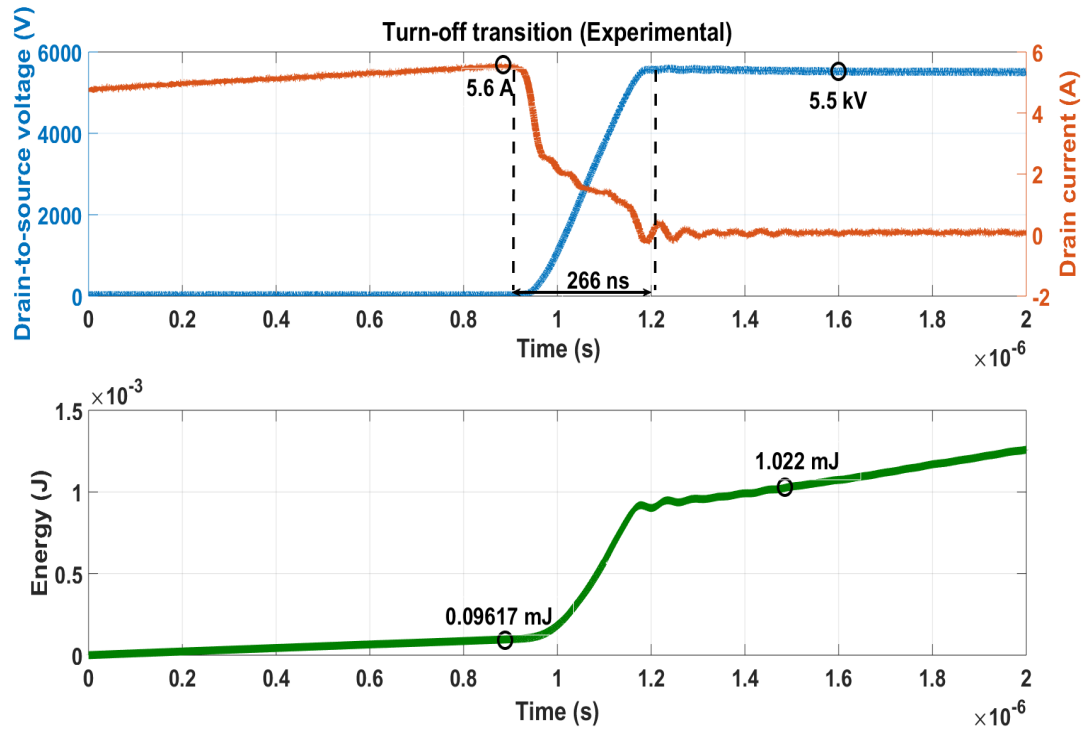


Figure 6.4 5.5 kV, 5.6 A, $R_g = 20 \Omega$, turn-off transition (experimental)

The same operating condition is captured in Saber and the turn-off transition is shown below (Figure 6.5). The plots do not reflect the oscillations seen in a practical setup. The transition times are not predicted exactly but the model nevertheless provides a good approximation in predicting the device behaviour. The current in the Saber model is drawn in pink and the blue and green lines represent the drain-to-source voltage and the energy.

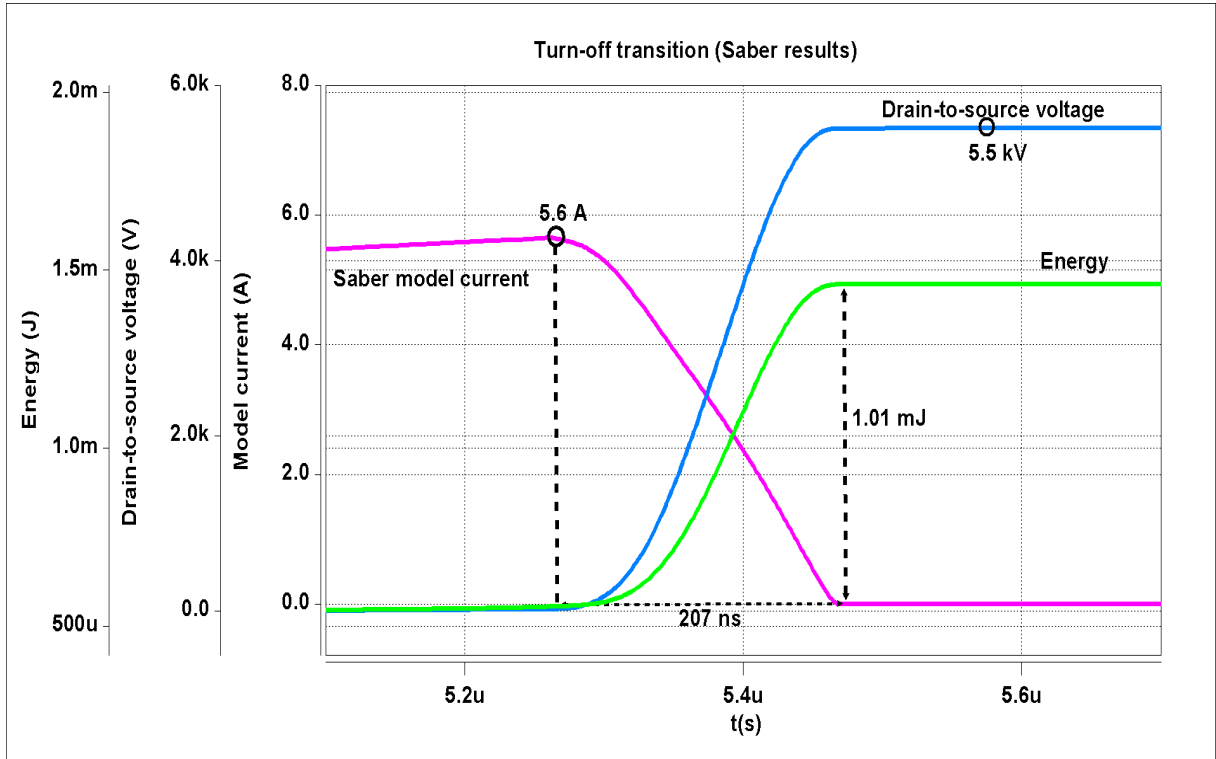


Figure 6.5 5.5 kV, 5.6 A, $R_g = 20 \Omega$, turn-off transition (Saber)

During turn-on, the Saber model is underestimating the losses in the 10 kV Gen-3 device. The turn-on waveform obtained through experiment is shown in Figure 6.6. The peak current due to the reverse recovery of the top device, transition times and the switching losses are annotated in the figure. The Saber results, shown in Figure 6.7, predicts turn-on losses of only 8 mJ. The reasons for the differences in the losses are listed below:

- (1) The parasitic capacitances of the Saber model do not exactly match the parameters of an actual die as seen in Chapter 2. This causes variations in the transition times which finally lead to deviations in the switching losses.
- (2) The reverse recovery of the diode model predicts higher values of negative peak current with correspondingly lower recovery time. This alters the behaviour of the bottom device and changes the value of its turn-on losses.
- (3) The dV/dt across the bottom device is higher than the actual values obtained through experiment. This causes very short voltage fall times which also lead to underestimating the turn-on losses.

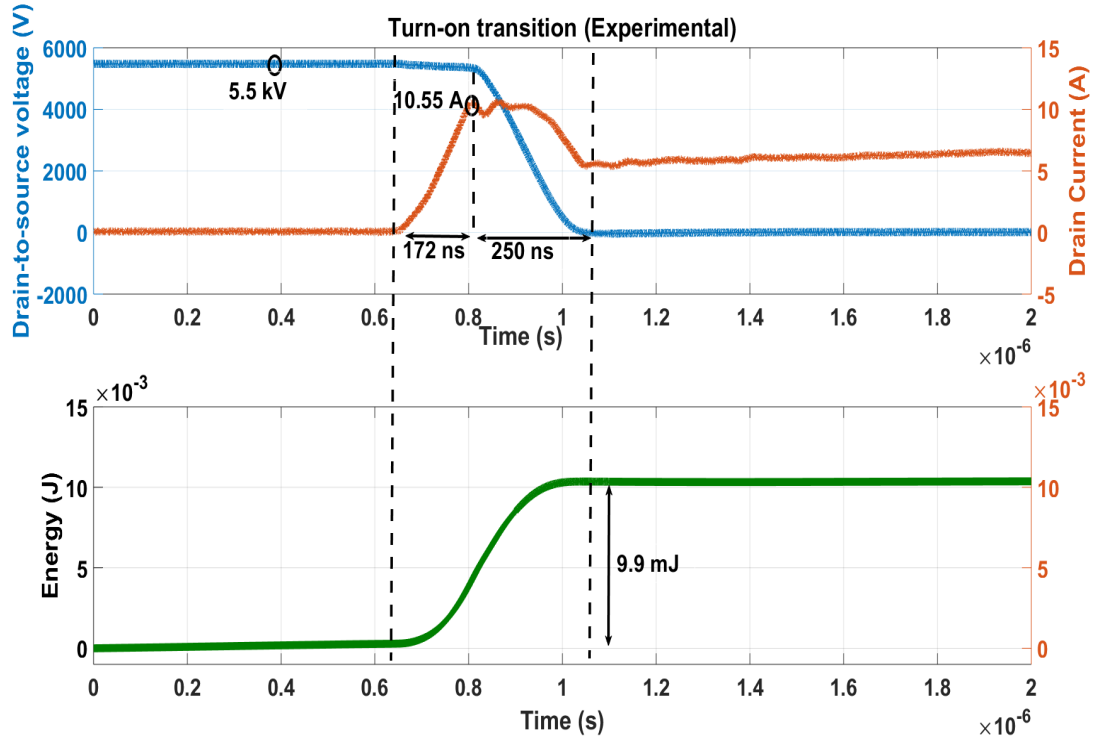


Figure 6.6 5.5 kV, 5.6 A, $R_g = 20 \Omega$, turn-on transition (experimental)

Further to this discussion, the accuracy of the Gen-3 Saber model will be discussed in all respects in the concluding chapter. The characterization results will be consolidated from the Saber model's perspective with the actual results taken the Power Device Analyzer. Improvements in the model would also be highlighted to make this a valuable tool in understanding the behaviour of the 10 kV Gen-3 device.

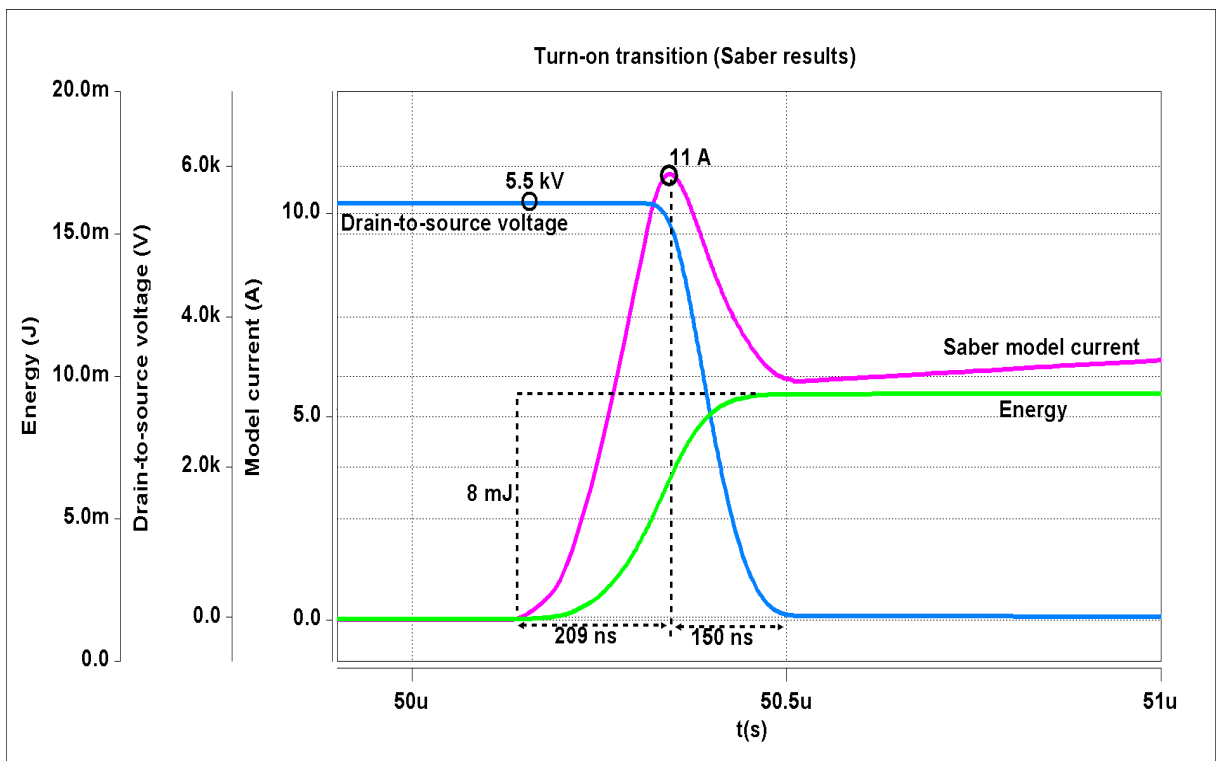


Figure 6.7 5.5 kV, 5.6 A, $R_g = 20 \Omega$, turn-on transition (Saber)

CHAPTER

7

CONCLUSION AND FUTURE WORK

This thesis work provided an approach to completely characterize and model a high voltage power MOSFET in the software tool, Saber. Chapter-2 presented useful data related to input, output characteristics, parasitic capacitance, leakage current, gate charge characteristics and computation of threshold voltage and ON-resistance as a function of temperature. Loss calculation and efficiency is crucial for power devices and Chapter-3 provided an insight on the breakdown of turn-on and turn-off losses along with the transition times in Saber. Chapter-4 presented a discussion on gate driver delays on a power converter using several such high voltage MOSFET models. To combat issues related to voltage mismatch, a simple design procedure of a passive RC snubber was elaborated with trade-offs between turn-on losses and dV/dt across the devices. Finally, the Saber Power MOSFET tool was utilized in building a device model of a 3.3 kV 400 A MOSFET manufactured by Sumitomo Electric. The accuracy of the created model was examined by comparing the switching losses across different device currents and gate resistance with the values of hardware results taken from reference [23]. A close match was shown between the results and maximum error of only 10% was observed.

Future improvements on the 10 kV Gen-3 Saber model:

(1) The output characteristic of the model shows a good match to the device behaviour over different values of gate-to-source voltages. The model exhibits ON-resistance of 447.86 m Ω ($R_{DS,ON}$) at $V_{GS}=15$ V and $I_D=2$ A. Percentage error with an actual die is about 15%. Making the model accurate over

different V_{GS} can be helpful to better predict the conduction losses.

(2) The threshold voltage of the Saber model is significantly higher than that of a typical device. The transconductance of the model is fairly accurate for $V_{GS} > 5$ V over different values of drain-to-source voltage.

(3) The value of C_{iss} is lower whereas the corresponding values of C_{oss} and C_{rss} are overestimated by the Saber model compared to a typical Gen-3 device. This would translate into small errors in predicting the switching losses as seen in Chapter 6.

(4) The voltage drop across the internal body diode is estimated with good accuracy by the Saber model. The effect due to temperature variation on the knee voltage of the model does not faithfully reflect the expected negative temperature coefficient.

(5) The switching transition times are underestimated in the model which leads to excessive di/dt and dV/dt . Hence, the turn-on losses in particular, are lower for the Saber model when compared to an actual device.

(6) The peak negative current through the diode model of the top device in a half-bridge configuration is very large for low values of gate resistance. A better fit for this model would be to lower the peak currents with some corresponding increase in the recovery time. The total recovery charge in this process is fairly consistent with that of a typical device.

(7) The leakage current in the Saber model is fairly simplistic and does not account for variations from one device to another. The OFF state losses can still be calculated with this model and the value of leakage is about $1000 \mu A$ for blocking voltages greater than 7 kV. The convergence issues for voltages greater than 8 kV is a matter of concern and should be resolved to carry out simulations close to the rating of the actual device.

One comprehensive extension to this work would be to create MAST HDL model of the device from scratch. Saber offers options for creating models based on mathematical equations, statistics and graphs. The equation based model would be easy to make changes or add extra features like the parameter variations with respect to temperature. The statistical modeling approach gives a degree of freedom to the user to implement the parameters with tolerances to mimic the real life applications. The approach with graphical modeling is the quickest to implement out of all the options and allows utilization of existing building blocks to create composite models.

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APPENDICES

ABBREVIATIONS

C_{GS} - Gate-to-source capacitance

C_{DS} - Drain to-source capacitance

C_{GD} - Gate-to-drain capacitance (Miller Capacitance)

DUT - Device Under Test

t_{rr} - Recovery time

Q_{rr} - Reverse recovery charge