ABSTRACT

RAHEJA, UTKARSH. Design of a GaN FET Based LLC Resonant Converter for Point Of Load Conversion. (Under the direction of Dr. Subhashish Bhattacharya).

This thesis presents the converter and control design for an LLC resonant converter based on GaN devices for Point-Of-Load (POL) conversion applications. This topology has been extensively developed in literature for POL applications for Data Centers. However, due to advantages like ability to achieve primary-side ZVS (Zero-Voltage Switching) throughout the load range and input voltage range, high efficiency even at light loads (10%), operate at high switching frequencies allowing improved power densities, it has become a popular candidate for automotive POL applications. The converter developed in this thesis is the prototype for a POL converter in a Distributed Power System of a Heavy-Duty vehicle like Tractor.

With the ability to operate under ZVS, the switching losses can be reduced to negligible values. However, conduction losses are not mitigated, which can reduce achievable efficiency. This provides the motivation to use GaN devices, due to the extremely low on-state resistance, especially for the low-voltage, high current devices on the secondary-side. There is an additional advantage of absence of reverse recovery losses, which can reduce efficiency above resonant frequency operation. This thesis work presents a design methodology for the selection of the resonant tank parameters, an approach for small-signal modelling and voltage-mode control design based on variable frequency control. Also, in order to take advantage of the low on-state resistance of the GaN devices, a digital implementation approach is also detailed. Finally, specifics of the hardware implementation, including the layout recommendations for Gate-drive design and Power-loop design are illustrated, as an aid for future work using similar GaN devices. The control and modelling have been verified by comparison between response from hardware results, simulation results and the small-signal model developed.

Design of a GaN FET Based LLC Resonant Converter for Point Of Load Conversion Applications

By
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DEDICATION

Dedicated to my Family

BIOGRAPHY

Utkarsh Raheja was born on March 14, 1992 in New Delhi, India. He did his schooling from DPS R.K. Puram School, New Delhi. He graduated from Delhi Technological University, New Delhi with a Bachelor in Electrical and Electronics Engineering. He joined North Carolina State University in 2016 for M.S. in Electrical Engineering with specialization in Power Electronics. Since Feb 2016, he has been associated with Future Renewable Electrical Energy Delivery and Management (FREEDM) Systems Center during his study at North Carolina State University. His research focuses on design of control and converters based on Wide-Band Gap (WBG) devices.

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CHAPTER 1 INTRODUCTION

1.1 Background and Motivation

The conventional power supply architecture consists of a centralized power unit which distributes power throughout the system via a network of cables or bus-bars. However, with increasing power consumption and reducing load voltage level requirements, in applications like data centers, laptop power supplies, etc., Distributed Power Architecture (DPA) has become popular. The distributed architecture can spread the concentration of heat throughout the system, reduce distribution losses, support high currents at very low voltages and provide improved transient response to varying loads, while also providing better system reliability when one of the Point-Of-Load (POL) converters fails.

Owing to the advantages stated above, DPA is being employed widely in EV and HEV applications. In an Electric Vehicle system, there are many different types of loads including electronics, air-conditioning, lighting, etc. These loads are located in different parts of the vehicles and fed by one or more sources. Also, due to the limited space and weight that can be carried in the vehicle, power supplies with minimal volume and weight are desired. These requirements make a favorable case for a distributed architecture.

Figure 1.1 shows the supply architecture and voltage levels for a heavy-duty vehicle. The Centralized converter is an isolated, 6kW, Bidirectional DC-DC converter based on Dual-Active Bridge topology, interfaced with a high voltage battery bank. Multiple Point-Of-Load (POL) converters feed the auxiliary loads in the vehicle. With the input to the POL converter regulated

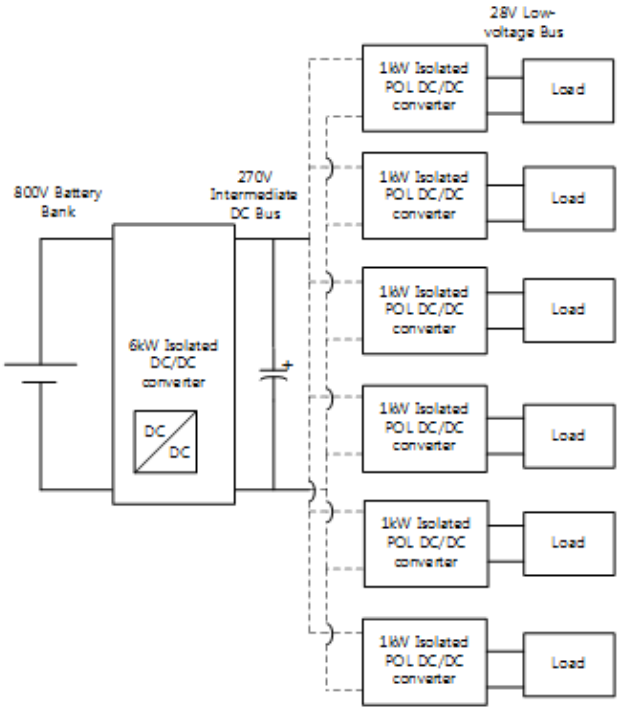
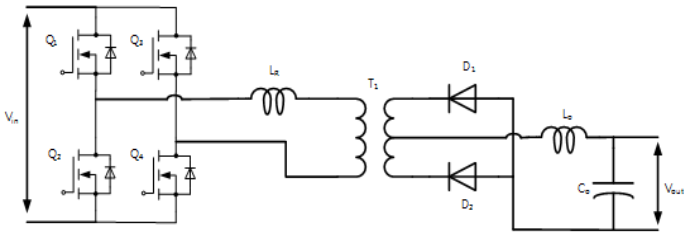


Figure 1.1 Power Supply Architecture for a Heavy-Duty Vehicle

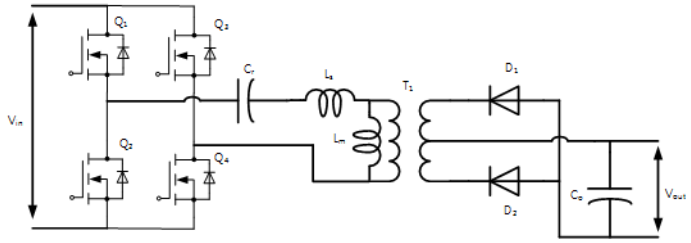
by the centralized converter, the POL can be optimized for the nominal operating point, allowing for higher efficiencies to be achieved. Energy efficiency is of pivotal importance for Electric Vehicles due to limited energy storage available on-board. Hence, from efficiency stand-point, it is not just the peak efficiency that is important but the efficiency for a wide range of loading conditions must be high. This limits the possible topologies that can be used as the POL stage.

One of the common topologies for the second stage is a Phase shifted full-bridge converter, shown in Figure 1.2(a). Another common candidate is the LLC resonant converter, shown in Figure 1.2(b), owing to the capability to achieve soft switching over a wide range of input voltages and also, for the entire load range. The two topologies have been compared in literature [1] for a 1kW prototype, based on ZVS range, size and efficiency. In terms of the ZVS range, Phase shifted full-bridge converter loses ZVS in light load conditions due to low inductive stored energy, whereas LLC can achieve ZVS throughout load range. From efficiency stand-point, the reported efficiency for LLC converter is slightly lower than the Phase shifted full-bridge converter. However, the

design specifications used for the comparison has a wide input voltage range, which means a wide gain requirement. This makes it difficult to optimize the design for resonant tank. This is not the case for a POL application, having an input DC bus which is well regulated within a narrow voltage band, allowing the tank design to be optimized accordingly. Hence, for such applications, the difference in efficiency can be even lower. Size considerations find the LLC at an advantage due to the fact that the LLC gets rid of the higher order harmonics in the transformer current, reducing the output filter requirements, whereas the Phase shifted full-bridge converter requires an output filter inductor to reduce the output current ripple. With a POL, this filter inductor will have a high current rating and hence, can be large.



(a)



(b)

Figure 1.2 (a) Phase-shifted Full-Bridge converter (b) LLC resonant converter. Two possible candidates for POL applications in Heavy Duty Vehicle applications

Based on the above comparison, LLC resonant converter is a strong candidate for the POL applications in EV auxiliary supplies. Hence, a further investigation of the LLC converter for EV applications is required. This thesis presents an LLC resonant converter for POL conversion in a DPA for EV auxiliary power supplies.

1.2 Thesis Outline

This thesis is divided into five chapters.

The first chapter briefly discusses the advantages of a Distributed Power Architecture for EV applications. Two topologies were considered for the application: Phase Shifted Full-Bridge converter and LLC Resonant converter. Discussion on the two topologies based on a literature review is presented.

Second chapter discusses about the design of an LLC Resonant Converter based on a set of specifications, adopted from the power supply requirements of a heavy-duty vehicle.

Third chapter discusses the small-signal modelling and controller design for the LLC converter. Variable frequency control is used here and a discussion of the digital implementation is presented.

Fourth chapter deals with the issue of synchronous rectification in resonant converters. A literature review of existing methods is presented and a reported digital implementation is explored.

Fifth chapter deals with the details of the hardware implementation and results for open-loop and closed-loop control.

CHAPTER 2 OPERATING PRINCIPLE AND DESIGN OF LLC RESONANT CONVERTER

The circuit schematic of the LLC resonant converter is shown in Figure 2.1. The converter is called so due to the elements of the resonant tank: C_r (series resonant capacitor), L_r (series resonant inductor, can be included in the leakage inductance of the transformer) and L_m (shunt resonant inductor, same as the magnetizing inductor of the transformer). A half-bridge or full-bridge circuit is used to apply a square wave input voltage to the resonant tank at a particular switching. There are two resonant frequencies associated with this type of converter: F_L, between C_r and (L_m+L_r) and F_H, between C_r and L_r. The behavior of the circuit changes with the relation of the switching frequency to the tank resonant frequency, F_H. Hence, it is important to understand the operation of the circuit at different switching frequencies, to be able to generate a model for the converter and develop a controller to regulate the output voltage.

2.1 Principle of Operation

2.1.1 Operation below Resonant Frequency (F_s<F_0)

Considering one half cycle in Figure 2.2 for analysis, there are two different states.

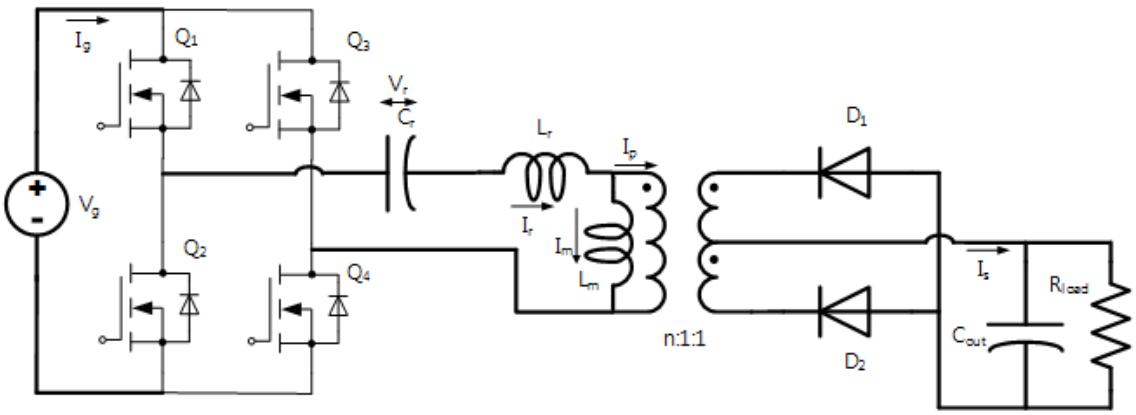


Figure 2.1 Schematic for LLC resonant converter

The first state is from t=0 to t_1, during which power transfer from primary side to the secondary side takes place. During this state, the magnetizing inductance is not part of the resonant tank since it is clamped to the output voltage (+ diode drop) times the transformer turns ratio, n.

The second state is from t_1 to $T_s/2$, during which the tank current freewheels through the devices Q_1 and Q_4. The load resistance is fed from the output capacitor. In this interval, the magnetizing inductor becomes part of the resonant tank and the resonant frequency is decided by (L_m+L_r) and C_r.

Thus, within one half switching cycle, there are two different resonant frequencies and hence, the converter is a multi-resonant converter.

The duration from t=0 to t_1 corresponds to the diode conduction on the secondary side. This duration is very close to the resonant half period, $T_0/2$. The reason is that during one half cycle, a fixed DC voltage is applied to the resonant tank and so, the tank current starts oscillating at resonant frequency, f_0. However, when it reaches I_m at t_1, the primary winding current becomes 0 and the secondary diode gets reverse biased, which means that the resonant tank changes. Since, the resonant frequency during this period is low, change in tank current is small during this period.

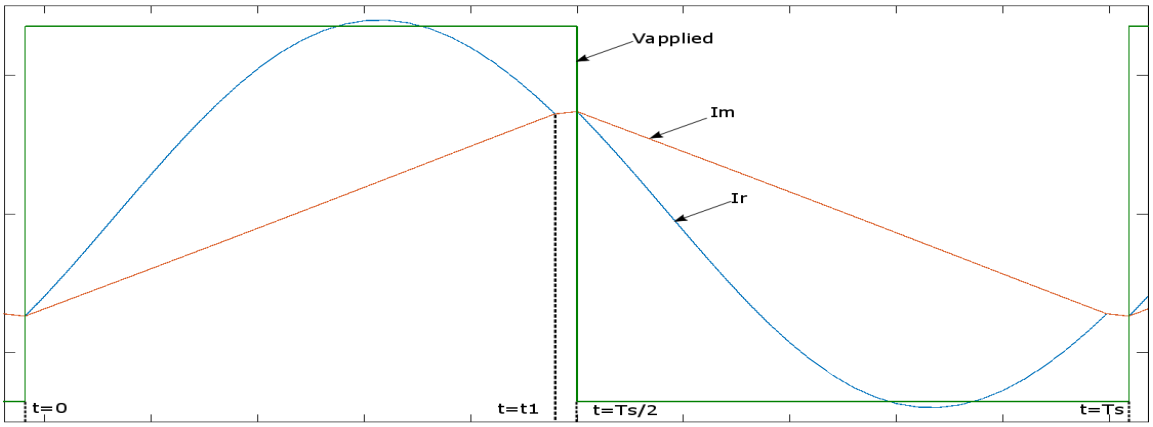


Figure 2.2 output voltage from H-bridge, resonant tank current and magnetizing current ($f_s<f_0$)

Hence, the currents at t=0 and t_1 are almost equal in magnitude, but of opposite sign. It is well known that the duration between two points with equal magnitude but opposite signs on a sinusoidal waveform is equal to the half period. Hence, the duration from t=0 to t_1 is approximately $T_0/2$. The deviation of the actual duration from $T_0/2$ becomes more prominent as the switching frequency becomes lower. This approximation is sometimes used for synchronous rectification on the secondary side, when the secondary side devices are MOSFETs rather than diodes.

2.1.2 Operation at Resonant Frequency ($F_s = F_0$)

The waveforms of the voltage applied to the resonant tank, the resonant tank current and the magnetizing current for one switching cycle is shown in Figure 2.3. In this mode of operation, the resonant current equals the magnetizing current at the end of the switching half cycle. This means that the duration of secondary diode conduction is equal to $T_0/2$. At the end of the half cycle, the diode current has reached zero and hence, we get ZCS or soft commutation of the current on the secondary side. Also, throughout the half period, the magnetizing inductor is clamped to the reflected output voltage (+ diode drop). Hence, the entire half cycle corresponds

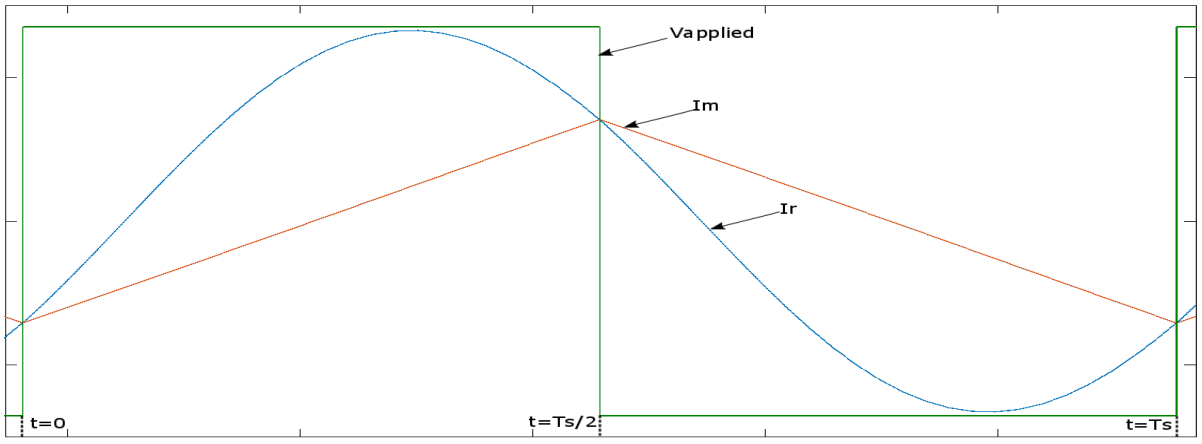


Figure 2.3 Output voltage of H-bridge, resonant tank current and magnetizing current ($f_S=f_0$)

to the power delivery operation and there is no freewheeling operation. This means reduced conduction losses on the primary side devices. Also, we have ZVS on the primary side devices.

Hence, this mode of operation leads to the best case efficiency. When designing the converter, it is reasonable to design the converter to operate in this mode of operation for the nominal conditions (i.e. conditions under which the converter is expected to operate for more duration of time), to achieve better energy efficiency.

2.1.3 Operation above Resonant Frequency ($F_s > F_0$)

The waveforms of the voltage applied to the resonant tank, the resonant tank current and the magnetizing current for one switching cycle is shown in Figure 2.4. In this mode of operation, the resonant tank current is higher than the magnetizing current at the end of the switching half cycle, since the resonant half cycle period is now greater than the switching half period. This means increased turn-off losses for the primary side H-bridge devices. Also, the secondary diode current, which is equal to the reflected primary winding current, is non-zero at the commutation instant. This means that the reverse recovery losses of the secondary diodes also come into the picture now. This can be an issue if the devices used are based on Si technology. In case of GaN based

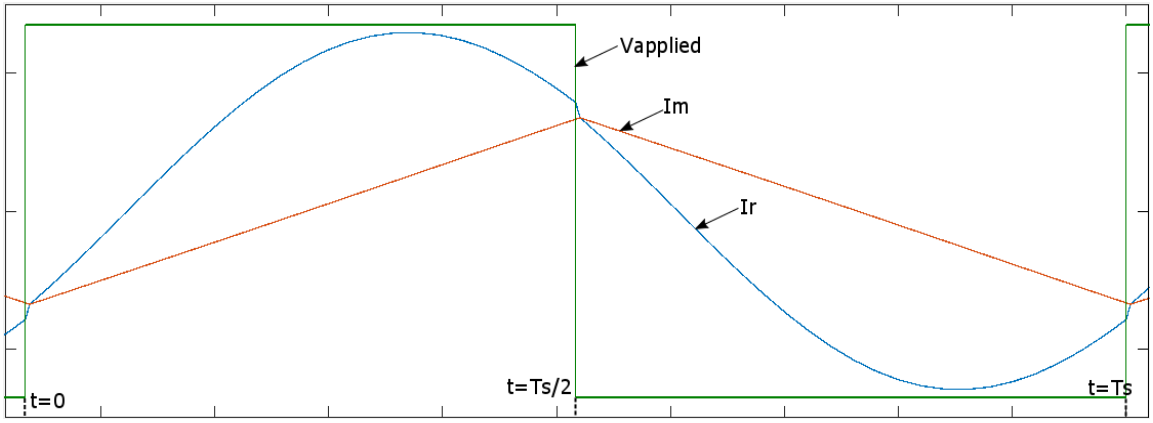


Figure 2.4 Output voltage of H-bridge, resonant tank current and magnetizing current ($f_S > f_0$)

devices, the reverse recovery loss is zero which can help improve the efficiency for operation above resonant frequency.

At the end of the switching half cycle, at t=Ts/2, the switches Q2 and Q3 are turned off. Due to the tank current being in positive direction, the anti-parallel diodes of Q1 and Q4 conduct during the dead-time (neglecting the time taken to discharge the respective device output capacitance) and the applied voltage switches from +Vg to –Vg. Since the secondary diodes are still conducting, the magnetizing inductor is clamped to the reflected output voltage (+ diode drop) and the voltage across the capacitor cannot change instantaneously, which means that the resonant inductor, Lr, sees the (2*Vg) change in voltage across it, which allows the steep drop in resonant current, till it meets the magnetizing current. This is shown in Figure 2.5 for clarity. Note that these waveforms are extracted from an ideal PLECS simulation to aid the explanation of the converter operation. The applied voltage across the resonant tank is now –Vg and the resonant tank current starts oscillating in the reverse direction according to the resonant frequency, till it is interrupted by the turning off of the switches Q1 and Q4.

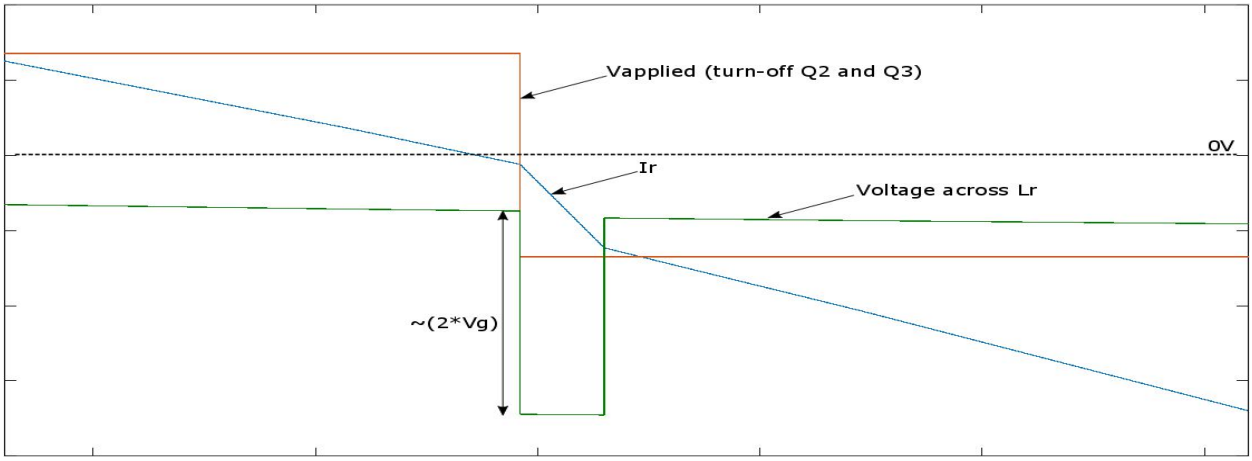


Figure 2.5 Drop in resonant current at turn-off instant of Q2 and Q3 switches

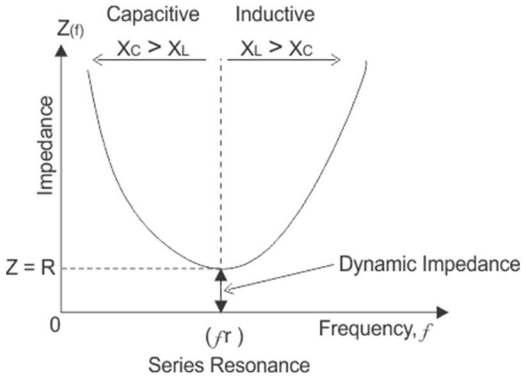


Figure 2.6 Impedance curve for series resonant tank
Source: https://www.electrical4u.com/resonance-in-series-rlc-circuit/

2.2 Design Equations and Methodology

The impedance characteristics of a series resonant tank is as shown in Figure 2.6.

Hence, it acts like a filter for the switching frequency component of the current and power transfer happens through the fundamental component of the current. Thus, we can analyze the circuit considering only the fundamental component of the various signals. This is known as the Fundamental Harmonic Approximation (FHA) and gives a sufficiently accurate model to allow us to design the converter.

In order to obtain the DC gain of the resonant tank, the equivalent circuit shown in Figure 2.7 can be considered.

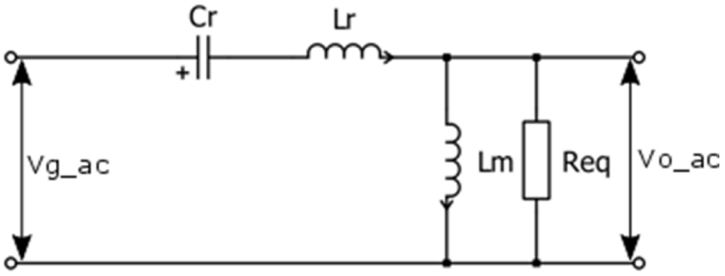


Figure 2.7 Equivalent resonant circuit for computing DC gain

Here, R_{eq} is the load resistance referred from the DC side to AC side of the rectifier and then, from secondary side of the transformer to the primary side:

$$R_{eq} = \frac{8}{\pi^2} * n^2 * R_L \tag{2.1}$$

Where,

$n = N_p/N_s$ (Primary turns/Secondary turns)

R_L = load resistance

The above circuit can be solved for the resonant tank gain to get the following expression:

$$K(Q, m, F_x) = \left|\frac{V_{o_{ac}}(s)}{V_{g_{ac}}(s)}\right| = \frac{f_n^2 * m}{\sqrt{((1+m) * f_n^2 - 1)^2 + (f_n^2 * (f_n^2 - 1)^2 * m^2 * Q^2)}} \quad (2.2)$$

Where,

$$f_0 = \left(\frac{1}{2\pi * \sqrt{L_r * C_r}}\right)$$

$f_n = f_S/f_0$ = normalized switching frequency

$$Q = \left(\frac{1}{R_{eq}}\right) * \sqrt{L_r/C_r}$$

$m = L_m/L_r$

It can be observed from the above gain equation that it depends on the normalized switching frequency along with two parameters: the tank Q-factor and the ratio of the magnetizing to the resonant inductance, m. Based on these two parameters, we can compute the tank component values, L_r, C_r and L_m. Thus, a design methodology needs to be outlined to decide the two parameters, Q and m.

2.2.1 Design Methodology

The first step is to decide the turns-ratio for the transformer. There can be different ways to design this parameter. The turns-ratio decides the gain requirement of the resonant tank, based on the range of input voltages. One of the ways is to decide the turns-ratio based on the nominal input and output voltages since, this would lead to the converter operating at resonant frequency (best efficiency of operation) at the nominal operating voltages. Since, the converter is expected to operate most of the time at nominal conditions, this selection of turns-ratio leads to improved energy-efficiency. The specifications for the converter prototype developed in this thesis are given in Table 2.1.

The second step in the design procedure is to decide the gain requirement from the resonant tank based on the output voltage and input voltage range of regulation. Based on the specs, the gain requirement of the resonant tank is as follows:

Table2.1 Converter prototype specifications

Parameter	Target Value
Input Voltage	250-280 V
Output Voltage	28 V (Nom.)
Max. Load Power	1 kW
Switching Frequency	>100kHz
Output Voltage ripple (pk-pk)	<1.5 V
Efficiency	> 97%
Power density	5kW/L

Minimum Gain (at V_{in} =280V) = 270/280 = 0.964

Maximum Gain (at V_{in} =250V) = 270/250 = 1.08

However, we need to keep some margin in the peak gain to allow operation in the inductive region during transient conditions. Keeping a margin of nearly 20% in the peak gain, we get a maximum gain requirement of 1.31, which should be met at maximum load conditions. The worst case for

the peak gain is the maximum load conditions. Hence, we need to ensure that the maximum gain requirement is met at maximum load conditions i.e. at Q_{max}.

The third step in the design procedure is to decide the values for Qmax and m. It is important to understand the qualitative effect of the two parameters to be able to decide on optimal values of the two.

Higher Q_{max} leads to a tighter frequency range of regulation since the minimum gain is achieved with less increase in frequency. However, a higher Q_{max} limits the peak gain in which case, the peak gain requirement might not be met. A lower Qmax might be able to achieve the peak gain requirement, but is less sensitive to frequency modulation in the region above resonance frequency.

A lower m might be able to meet the gain requirement. However, this means a reduced L_m which leads to higher circulating currents and conduction losses, which affects converter efficiency drastically, especially at light loads. Also, a lower m also leads to steep gain curves, which means a large gain variation for a small change in frequency. This can cause issues in digital implementations of control which are limited by the resolution of the controller platform being used for the implementation. A higher m is better from the point of view of efficiency, due to lower magnetizing circulating current. However, the peak gain reduces with increasing value of m.

We can plot the peak gain vs Q_{max} at different values of m, as shown in Figure 2.8. Also marked in the Figure is the max gain requirement, including the safety margin. This will allow us to get a few combinations of Q_{max} and m which can meet the gain requirements. Thus, we have a sample space from among which we need to select the best design values.

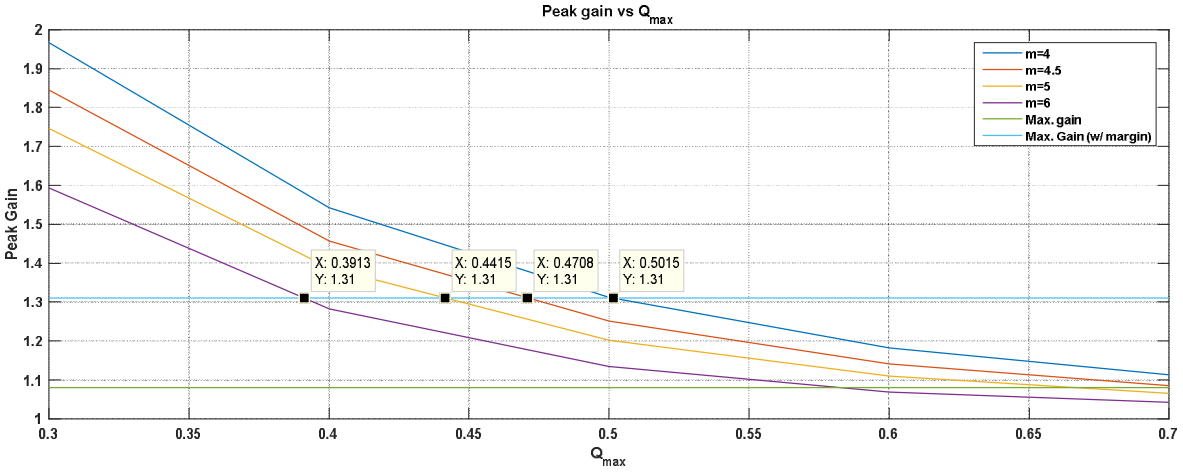


Figure 2.8 Plot of peak gain vs Qmax for different values of m

A common range for the value of m is between 4 and 10. As a starting point, a moderate value of Q_{max} i.e. close to 0.5 is reasonable. Considering the different combinations in the sample space and with a range of Q_{max} and m in mind, we can narrow down to a few designs, shown in Table 2.2. For each of the selected designs, we compute a few parameters such as the minimum and maximum frequency of operation over the input voltage range and the load range, resonant tank component values i.e. L_r, C_r and L_m. Note that the values mentioned here are based on a resonant second resonant frequency of 200kHz, decided according to the specifications in Table 2.2. The target is to minimize the frequency range of operation (since it allows for better regulation along with ensuring a lower size of magnetics, being dictated by the minimum frequency of operation though, this effect may not be very pronounced) and the maximize the magnetizing inductance (since it results in lower circulating currents and hence, boosts efficiency at light loads).

Table2.2 Frequency range of operation, Peak magnetizing current and resonant tank parameter values for different designs under consideration

	Q_{max}	$m(=L_m/L_r)$	f_{min}	f_{max}	Δf	L_r	L_m	C_r	I_{mpeak}
Design I	0.44	5	166kHz	220kHz	54kHz	20.7µH	103.45µH	30.6nF	3.2A
Design II	0.47	4.5	170kHz	218kHz	48kHz	22.1µH	99.45µH	28.65nF	3.39A
Design III	0.5	4	175kHz	214kHz	39kHz	23.54µH	94.2 µH	27nF	3.58A

Based on the above target, the selected design is highlighted in the Table 2.2. Note that the selected design has a very narrow range of frequency for operation, compromising a little on the magnetizing inductance, L_m. This is based on the peak magnetizing current computation for the three design cases, shown in the last column of Table 2.2. The increase in magnetizing current in design III is nearly 12% with respect to design I whereas the reduction in the range of operating frequency is nearly 28%.

This completes the design of the converter. One more important component to be designed is the output capacitor value. It is not only important from the perspective of the voltage ripple but also from the perspective of the control and stability. This will be discussed in the next chapter.

CHAPTER 3 SMALL-SIGNAL MODELLING AND CONTROLLER DESIGN

The various loads in an electric vehicle such as electronic loads, air-conditioning loads, etc. require a well-regulated supply for their operation. However, the operating profile of the loads are varied. To ensure a stable regulation at all load and input voltage conditions, the controller must be designed considering the model of the converter system at the various operating conditions. Usually, an averaged model is enough for the control design. However, such a modelling approach is not valid for resonant converters since, some of the state variables do not have DC components but have strong switching frequency components and its harmonics. Due to the strong oscillatory nature of the states, the switching frequency interacts with the natural resonant frequency of the system which results in the phenomena of beat-frequency dynamics. Different methods have been proposed in literature [2-5, 7] for modelling of resonant converters. One of the most successful models is the extended describing function method. This method is discussed further in this chapter to derive the equivalent circuit model. This model is then utilized to design the feedback network for stable regulation.

3.1 Extended Describing Function Method

The first step towards modelling the LLC resonant converter is to describe the converter as a set of non-linear state equations using Kirchhoff's Laws. The non-linear or quasi-sinusoidal terms are represented as by their harmonic components as the next step. Usually, the order of the harmonics is restricted to the first harmonic component. This step of representing the non-linear terms with their harmonic components is termed as the Extended Describing Function (EDF) method. The following analysis uses only the first harmonic component for simplicity. The current and voltage of the output filter are approximated with their DC components. The next step is to plug in the harmonic representations of the non-linear components in the non-linear equations and separate

out the DC, sine and cosine components. The sine and cosine circuits are together represented in the form of a large signal model which is then perturbed and linearized to obtain the small-signal model of the converter.

The procedure outlined above is used as follows. The detailed derivation is provided in [2] and is reproduced here for convenience of the reader, with some modifications to take into account the full bridge converter for generating the input pulses for the resonant tank, instead of the half-bridge converter considered in [2].

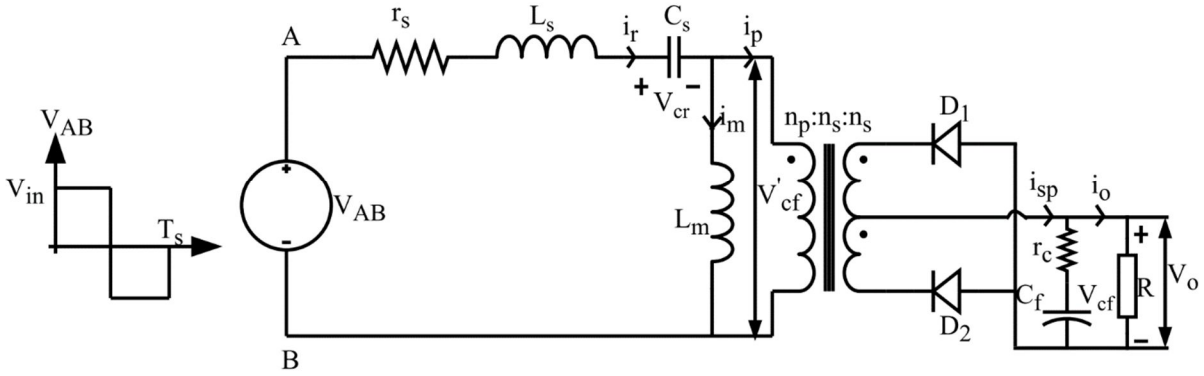


Figure 3.1 Equivalent circuit of LLC resonant converter

Based on the equivalent circuit shown in Figure 3.1, we can write the following equations:

$$V_{AB} = r_s i_r + L_s \frac{di_r}{dt} + V_{cr} + sgn(i_p) V'_{cf} \tag{3.1}$$

Where,

$$\text{sgn(ip)} = \begin{cases} +1, \text{if V'cf} \geq 0 \\ -1, \text{if V'cf} < 0 \end{cases}$$

$$i_r = C_s \frac{dV_{cr}}{dt} \tag{3.2}$$

$$V'_{cf} = L_m \frac{di_m}{dt} \tag{3.3}$$

$$i_{sp} = C_f \frac{dV_{cf}}{dt} + \frac{V_{cf} + r_c C_f \frac{dV_{cf}}{dt}}{R} = \left(1 + \frac{r_c}{R}\right) C_f \frac{dV_{cf}}{dt} + \frac{V_{cf}}{R} \tag{3.4}$$

$$V_o = r_c' abs(i_{sp}) + (\frac{r_c'}{r_c})V_{cf} \tag{3.5}$$

The quasi-sinusoidal terms in the above equations can be approximated with their harmonic components as part of the next step. Here, only the fundamental harmonic is used to represent the following terms:

$$\begin{aligned} i_r(t) &= i_s(t)sin(\omega_s t) - i_c(t)cos(\omega_s t) \\ i_m(t) &= i_{ms}(t)sin(\omega_s t) - i_{mc}(t)cos(\omega_s t) \\ V_{cr}(t) &= v_s(t)sin(\omega_s t) - v_c(t)cos(\omega_s t) \end{aligned} \tag{3.6}$$

Similarly, the non-linear components can be expressed as:

$$\begin{aligned} V_{AB}(t) &= f_1(V_{in})\sin(\omega_s t) \\ sgn(i_{sp})V_{cf}' &= f_2(i_{ss}, i_{sp}, v_{cf}')\sin(\omega_s t) - f_3(i_{sc}, i_{sp}, v_{cf}')\cos(\omega_s t) \\ i_{sp} &= f_4(i_{ss}, i_{sc}) \end{aligned} \tag{3.7}$$

Where,

$$f_1(V_{in}) = \frac{4}{\pi}V_{in}$$

$$f_2(i_{ss}, i_{sp}, v_{cf}') = \frac{4n}{\pi}\frac{i_{ps}}{i_{pp}}v_{cf} = v_{ps}$$

$$f_3(i_{sc}, i_{sp}, v_{cf}') = \frac{4n}{\pi}\frac{i_{ps}}{i_{pp}}v_{cf} = v_{pc}$$

$$i_{pp} = \sqrt{i_{ps}^2 + i_{pc}^2}$$

Where,

$i_{ps}, i_{pc} = sine\ and\ cosine\ components\ of\ transformer\ primary\ current$

$i_{pp} = resultant\ transformer\ primary\ current$

$i_{ss}, i_{sc} = sine\ and\ cosine\ components\ of\ transformer\ secondary\ currents$

$i_{sp} = resultant\ transformer\ secondary\ current$

$v_{ps}, v_{pc} = sine\ and\ cosine\ components\ of\ transformer\ primary\ voltage$

$n = n_p/n_s$

Plugging the above harmonic approximations, equations (3.6)- (3.7) in the non-linear equations of the system, equations (3.1)-(3.5), we can separate the DC, sine and cosine terms to get separate circuits, representing the large signal model of the LLC resonant converter, as shown in Figure 3.2.

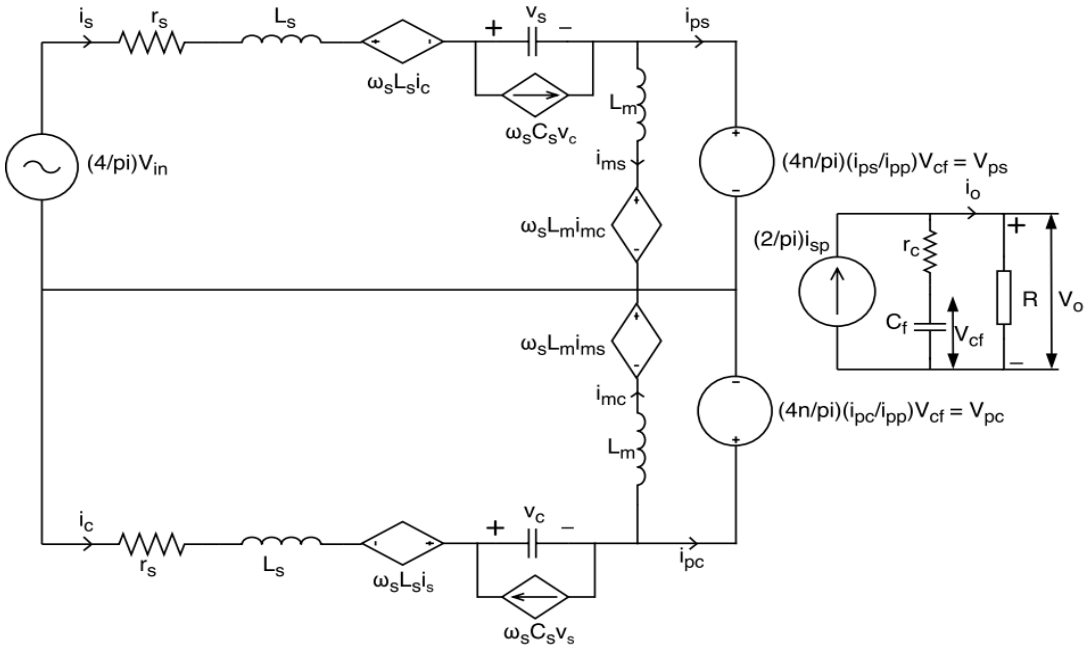


Figure 3.2 Large-signal model of LLC resonant converter

Using the large-signal model shown in Figure 3.2, we can get equations for the steady-state operation. The small-signal model can then be obtained by perturbing and linearizing the large-signal model, around the steady-state operating point.

Steady-state operating point:

Filter cap voltage, V_{cf}:

$$\frac{V_{cf}}{R} = \frac{2}{\pi} i_{sp} = \frac{2n}{\pi} i_{pp}$$

$$V_{cf} = \frac{2n}{\pi} i_{pp} R = \frac{\pi}{4n} i_{pp} R_e \tag{3.8}$$

$$V'_{cf} = \frac{\pi}{4} i_{pp} R_e$$

Where,

$$R_e = \frac{8n^2}{\pi^2} R = Equivalent\ primary\ referred\ load\ resistance$$

Sine circuit:

$$V_{es} = \frac{4}{\pi} V_{in} = r_s I_s + \omega_s L_s I_c + V_s + I_{ps} R_e = (r_s + R_e) I_s - R_e I_{ms} + \omega_s L_s I_c + V_s$$

$$I_s = \omega_s C_s V_c \tag{3.9}$$

$$\omega_s L_m I_{mc} = I_{ps} R_e = (I_s - I_{ms}) R_e$$

Cosine circuit:

$$0 = r_s I_c - \omega_s L_s I_s + V_c + I_{pc} R_e = (r_s + R_e) I_c - R_e I_{mc} - \omega_s L_s I_s + V_c$$

$$I_c = -\omega_s C_s V_s \tag{3.10}$$

$$-\omega_s L_m I_{ms} = I_{pc} R_e = (I_c - I_{mc}) R_e$$

Thus, the steady-state operating point for the various state variables can be found by solving the following matrix equation (3.11):

$$\begin{bmatrix} I_s \\ I_c \\ V_s \\ V_c \\ I_{ms} \\ I_{mc} \end{bmatrix} = inv\left(\begin{bmatrix} (r_s + R_e) & L_s\omega_s & 1 & 0 & -R_e & 0 \\ -L_s\omega_s & (r_s + R_e) & 0 & 1 & 0 & -R_e \\ 1 & 0 & 0 & -C_s\omega_s & 0 & 0 \\ 0 & 1 & C_s\omega_s & 0 & 0 & 0 \\ R_e & 0 & 0 & 0 & -R_e & -L_m\omega_s \\ 0 & R_e & 0 & 0 & L_m\omega_s & -R_e \end{bmatrix}\right) \begin{bmatrix} V_{es} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{3.11}$$

The next step is to perturb the state variables (both sine and cosine components), input, output and control signals. The perturbed signals are as follows:

$$v_{in} = V_{in} + \widehat{v_{in}}, \omega_s = \omega_s + \widehat{\omega_s}, v_{ps} = V_{ps} + \widehat{v_{ps}}, v_{pc} = V_{pc} + \widehat{v_{pc}}, i_{ps} = I_{ps} + \widehat{\imath_{ps}}$$

$$i_{pc} = I_{pc} + \widehat{\imath_{pc}}, i_{pp} = I_{pp} + \widehat{\imath_{pp}}, v_{cf} = V_{cf} + \widehat{v_{cf}}, i_{ms} = I_{ms} + \widehat{\imath_{ms}}, i_{mc} = I_{mc} + \widehat{\imath_{mc}} \quad (3.12)$$

$$i_s = I_s + \widehat{\imath_s}, i_c = I_c + \widehat{\imath_c}, v_s = V_s + \widehat{v_s}, v_c = V_c + \widehat{v_c}, v_{es} = V_{es} + \widehat{v_{es}}, v_o = V_o + \widehat{v_o}$$

Plugging the perturbed signals above to the large-signal equations and linearizing, we get the following small signal model. For details about the linearization, please refer [2].

$$\frac{d\hat{x}}{dt} = A\hat{x} + B\hat{u}$$
$$\hat{y} = C\hat{x} + D\hat{u} \quad (3.13)$$

Where,

$$\hat{x} = [\widehat{\imath_s} \quad \widehat{\imath_c} \quad \widehat{v_s} \quad \widehat{v_c} \quad \widehat{\imath_{ms}} \quad \widehat{\imath_{mc}} \quad \widehat{v_{cf}}]$$

$$\hat{u} = [\widehat{f_{sn}} \; or \; \widehat{\omega_{sn}}]$$

$$\hat{y} = [\widehat{v_o}]$$

$$\widehat{\omega_{sn}} = perturbation\ in\ normalized\ switching\ frequency$$

$$A = \begin{bmatrix} -\frac{(H_{ip}+r_s)}{L_s} & -\frac{(\omega_s L_s + H_{ic})}{L_s} & -\frac{1}{L_s} & 0 & \frac{H_{ip}}{L_s} & \frac{H_{ic}}{L_s} & -\frac{H_{vcf}}{L_s} \\ \frac{(\omega_s L_s - G_{ip})}{L_s} & -\frac{(G_{ic}+r_s)}{L_s} & 0 & -\frac{1}{L_s} & \frac{G_{ip}}{L_s} & \frac{G_{ic}}{L_s} & -\frac{G_{vcf}}{L_s} \\ \frac{1}{C_s} & 0 & 0 & -\omega_s & 0 & 0 & 0 \\ 0 & \frac{1}{C_s} & \omega_s & 0 & 0 & 0 & 0 \\ \frac{H_{ip}}{L_m} & \frac{H_{ic}}{L_m} & 0 & 0 & -\frac{H_{ip}}{L_m} & -\frac{(H_{ic}+L_m\omega_s)}{L_m} & \frac{H_{vcf}}{L_m} \\ \frac{G_{ip}}{L_m} & \frac{G_{ic}}{L_m} & 0 & 0 & -\frac{(G_{ip}+L_m\omega_s)}{L_m} & -\frac{G_{ic}}{L_m} & \frac{G_{vcf}}{L_m} \\ \frac{K_{is}r_c'}{C_f r_c} & \frac{K_{ic}r_c'}{C_f r_c} & 0 & 0 & -\frac{K_{is}r_c'}{C_f r_c} & -\frac{K_{ic}r_c'}{C_f r_c} & -\frac{r_c'}{RC_f r_c} \end{bmatrix}$$

$$B = transpose\left(\left[-\frac{(L_s\omega_0 I_c)}{L_s} \quad \frac{(L_s\omega_0 I_s)}{L_s} \quad -\frac{(C_s\omega_0 V_c)}{C_s} \quad \frac{(C_s\omega_0 V_s)}{C_s} \quad -\frac{(L_m\omega_0 I_{mc})}{L_m} \quad \frac{(L_m\omega_0 I_{ms})}{L_m} \quad 0\right]\right)$$

$$C = \left[K_{is}r_c' \quad K_{ic}r_c' \quad 0 \quad 0 \quad -K_{is}r_c' \quad -K_{ic}r_c' \quad \frac{r_c'}{r_c}\right]$$

$$D = [0]$$

Where,

$$H_{ip} = \frac{4nV_{cf}}{\pi}\frac{I_{pc}^2}{I_{pp}^3}$$

$$H_{ic} = -\frac{4nV_{cf}}{\pi}\frac{I_{ps}I_{pc}}{I_{pp}^3}$$

$$H_{vcf} = \frac{4n}{\pi}\frac{I_{ps}}{I_{pp}}$$

$$G_{ip} = -\frac{4nV_{cf}}{\pi}\frac{I_{pc}I_{ps}}{I_{pp}^3}$$

$$G_{ic} = \frac{4nV_{cf}}{\pi}\frac{I_{ps}^2}{I_{pp}^3}$$

$$G_{vcf} = \frac{4n}{\pi}\frac{I_{pc}}{I_{pp}}$$

$$K_1 = \frac{4}{\pi}\sin(\frac{\pi}{4})$$

$$K_2 = 2V_{in}\cos(\frac{\pi}{4})$$

$$K_{is} = \frac{2n}{\pi}\frac{I_{ps}}{\sqrt{I_{ps}^2 + I_{pc}^2}}$$

$$K_{ic} = \frac{2n}{\pi}\frac{I_{pc}}{\sqrt{I_{ps}^2 + I_{pc}^2}}$$

Thus, based on the above equation, we can solve for the control (ω_{sn}) to output (v_o) transfer function as a seventh-order transfer function. For simplicity, the equation is truncated to a fourth

order transfer function as shown below. This can then be used to design the closed loop control for the converter. It must be noted that the above equations are for a 50% duty cycle of the applied voltage and for a full-bridge converter at the primary-side of the transformer. Some of the terms will need to be modified in case the duty cycle is also varied or if the converter at the primary-side of the transformer is a half-bridge.

For the design parameters selected in Chapter 2, the control to output transfer function at 50% load is computed as below. Note that this is the reduced-order transfer function.

$$G_p(s) = \frac{3.2266 * 10^{10}(s + 2.6849 * 10^6)(s - 2.4197 * 10^6)}{(s^2 + 2.4992 * 10^5 s + 64.07424 * 10^{10})(s^2 + 0.1116 * 10^5 s + 2.00845 * 10^{10})} \quad (3.14)$$

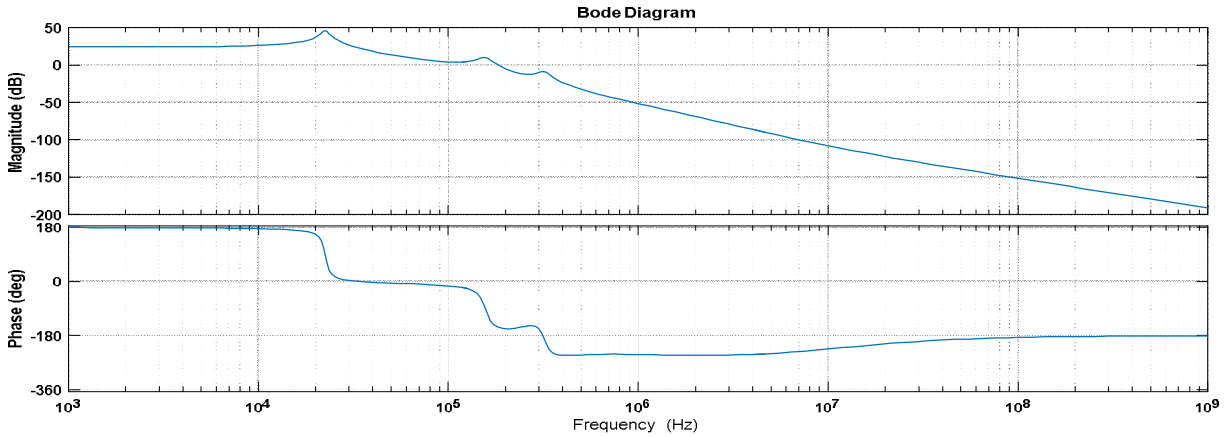


Figure 3.3 Bode plot for converter control-to-output transfer function (@V_{in} = 270V, P_{load} = 500W)

The bode plot corresponding to this transfer function is shown in Figure 3.3. We can observe a few important points from this. First, the system has the presence of one right-half plane zero at 385 kHz. Since, this is much beyond our resonant frequency and hence, the range of switching frequencies, it will not affect the Phase Margin of the control loop. Second, the system has two complex double poles. The dominant complex double pole represents the beat frequency dynamics of the system. At frequencies much above the resonant frequency, it is present at the beat frequency i.e. the difference of the switching frequency and the resonant frequency. However, as the

switching frequency becomes closer to the resonant frequency, one of the beat frequency pole moves to lower frequencies and forms a double pole with the output filter pole. This is the case in the transfer function shown above. Thus, as the output capacitor value is increased, this double pole frequency moves to lower frequencies. Moreover, the double pole is damped by the equivalent load resistance. Higher the load, greater is the damping provided to the dominant complex double pole.

Now that we have the control to output transfer function, we can design the closed-loop control for the converter. Different control strategies have been applied in literature [8-11]. However, variable frequency control is the most commonly used strategy.

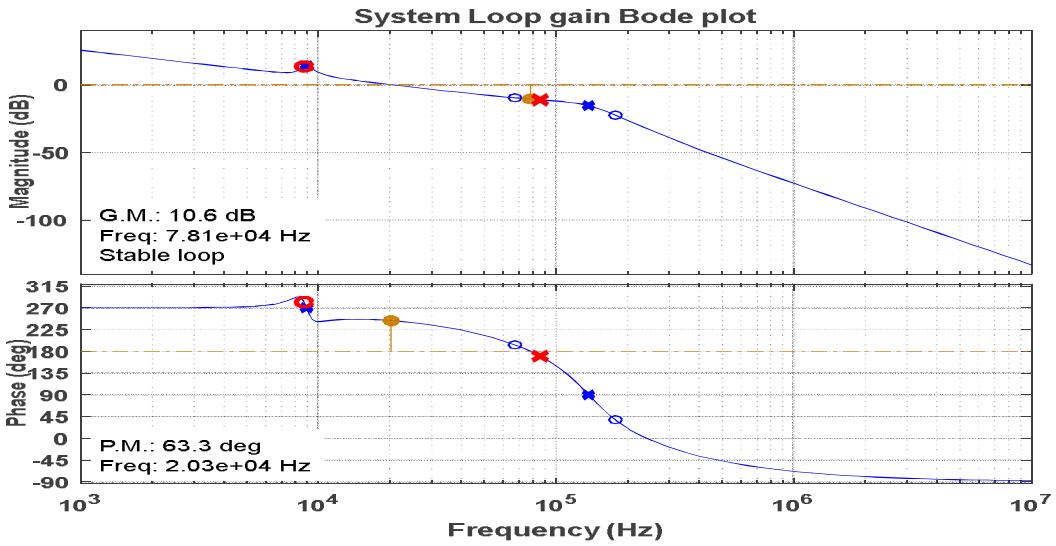
3.2 Controller Design

To ensure stability of the controller at all operating conditions, it is necessary to decide the worst-case conditions for the design. These are the conditions under which the Phase-Margin and gain-Margins can be reduced. At the double pole frequency, the phase-drop is steep. The slope of the phase-drop depends on the damping at the double-pole frequency. Hence, the worst-case scenarios are the cases for minimum input voltage (lowest frequency range of operation), maximum and minimum load, as well as maximum input voltage (highest frequency range of operation). Ensuring adequate phase margin and gain margin in all these cases can ensure stable operation at all operating conditions.

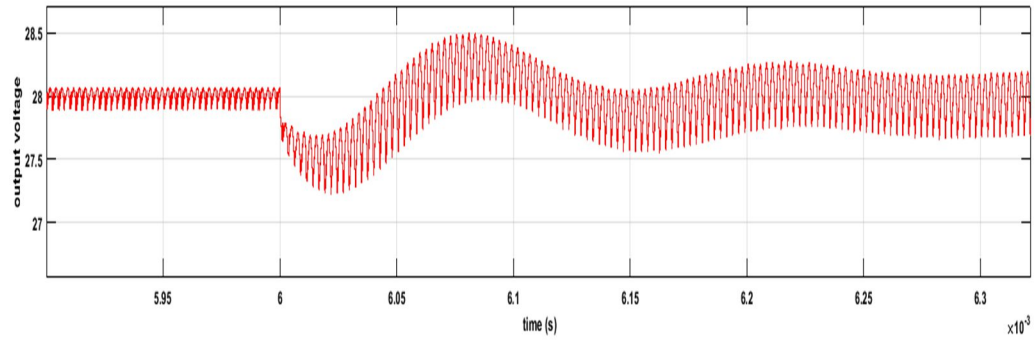
When designing the controller for a particular system, we need to decide the required cross-over frequency based on the desired transient response. While designing the converter prototype, we had not been provided with any transient specifications. However, it is desirable to reduce the effect of any disturbance, either in the input voltage or load, as seen in the output voltage. This means that the transfer function of the output voltage to the respective disturbance must be much

less than 0dB at all frequencies. In case the magnitude of the transfer function goes above 0dB for any frequency, we can observe ringing in the output response at the same frequency, for a step disturbance to the system. For a closed loop system, the transfer function from the output voltage to disturbance is reduced by the loop-gain below the cross-over frequency. On plotting the output impedance of the converter, we observe that the response has a steep increase in impedance at the double pole frequency. In order to reduce the effect of a step change in load, we must ensure that the cross-over frequency is above the double pole frequency. Note that even when the double-pole frequency is below the cross-over, the effect of the double pole can be seen as an oscillation in the output for a step disturbance in load, though the amplitude of the oscillation will be reduced due to the attenuation by the loop gain. This can be observed in Figure 3.4(b).

As a general design practice for PWM converters, the cross-over is usually selected between 1/10 to 1/5 of the switching frequency. Following a similar design approach in case of the LLC resonant converter, we can decide for a cross-over frequency of say, 20-30 kHz (1/10 of resonant frequency). This means that the double-pole frequency must be below 20 kHz. Since, the double-pole frequency is decided by the equivalent resonant inductance and the reflected output capacitance, it implies a large output capacitor. This is a limitation in many cases where size is a major constraint. Such a design is illustrated in Figure 3.4 for a 470µF output capacitor along with the simulation results for the output voltage response with a step change in load.



(a)



(b)

Figure 3.4 (a) Loop-gain bode plot for converter design with output capacitor of 470µF and cross-over frequency beyond double pole frequency. (PM: 63.3 deg, GM: 10.6dB, cross-over: 20.3 kHz) (b) Simulation results for step change in load from 30% to 100% @ Vin=270V (undershoot: 0.5V, settling time: 100µs)

Another limitation to this implementation comes from the digital implementation of the controller. It must be ensured that the sampling frequency for the output voltage is at least 10 times higher than cross-over frequency to ensure that the phase margin at cross-over is not affected by the sampling. However, in many cases, the sampling can get limited due to the computation time requirement for the control implementation. It is due to these two constraints that the control bandwidth for the prototype implementation has been designed to be below the complex double-pole frequency. Note that the value of output capacitor has been reduced in this case to 72µF based on output ripple requirements and space constraints on the PCB. This design is illustrated in Figure

3.5 and the achieved phase margins and gain margins for the corner cases mentioned above, are provided in Table 3.1.

One important point to keep in mind while designing the controller is to ensure that the magnitude plot of the loop gain does not have a second 0dB cross-over, which is possible at the dominant complex double-pole frequency. Such a scenario can lead to a conditionally stable system i.e. the system can become unstable with changes in the operating point or with disturbances of sufficiently large amplitude. In the bode plot shown in Figure 3.5, the double pole is 32.9dB below the 0dB line.

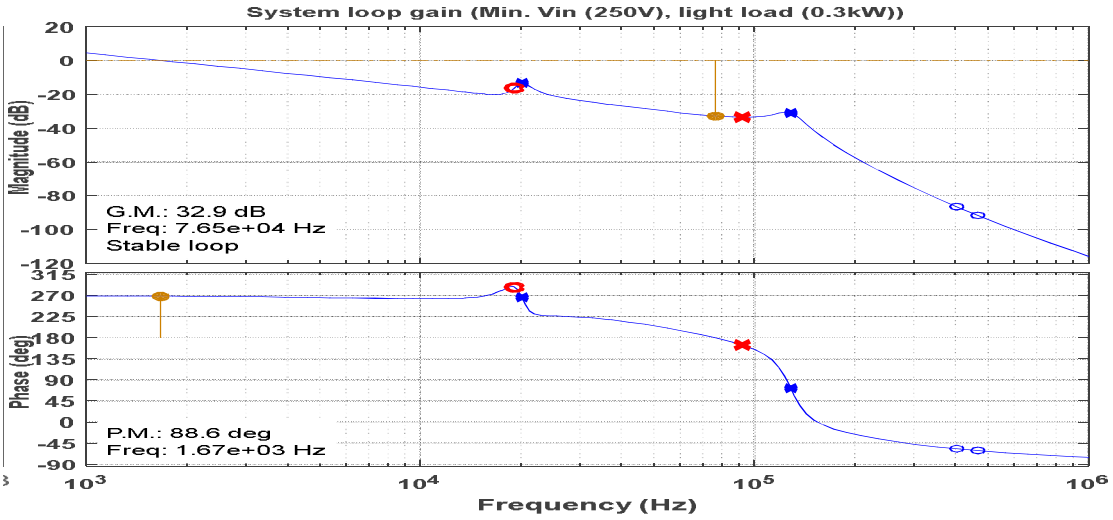


Figure 3.5 Loop-gain bode plot for converter design with output capacitor of 72µF and cross-over frequency below double pole frequency. (PM: 88.6 deg, GM: 32.9dB, cross-over: 1.67 kHz)

Table 3.1 Loop gain parameters for the designed controller for the four corner cases

	Max. Vin (280V), High load (1kW)	**Max. Vin (280V), light load (0.3kW)**	**Min. Vin (280V), High load (1kW)**	**Min. Vin (280V), light load (0.3kW)**
Gain Margin	31.3 dB	35.4 dB	30.9 dB	32.9 dB
Phase Margin	88.7 deg	89.4 deg	86.8 deg	88.6 deg
$\mathbf{f_{cross}}$	1.08 kHz	0.983 kHz	1.39 kHz	1.67 kHz

The control architecture used here is a two-zero, three-pole structure, consisting of one complex zero, one complex pole and an integrator. The complex zero and pole combination forms a complex lead-compensator. This is used here to reduce the overshoots caused by the double-pole and also, to compensate for the associated steep phase drop. This structure has a disadvantage from the perspective of sensor noise attenuation. The bode plot of a complex lead compensator is shown in Figure 3.6 [6]. It has an increased high-frequency gain, which can amplify any noise coming from the output voltage sensing, which can then be reflected in the output voltage. Hence, it is important to ensure low noise in the sense circuitry.

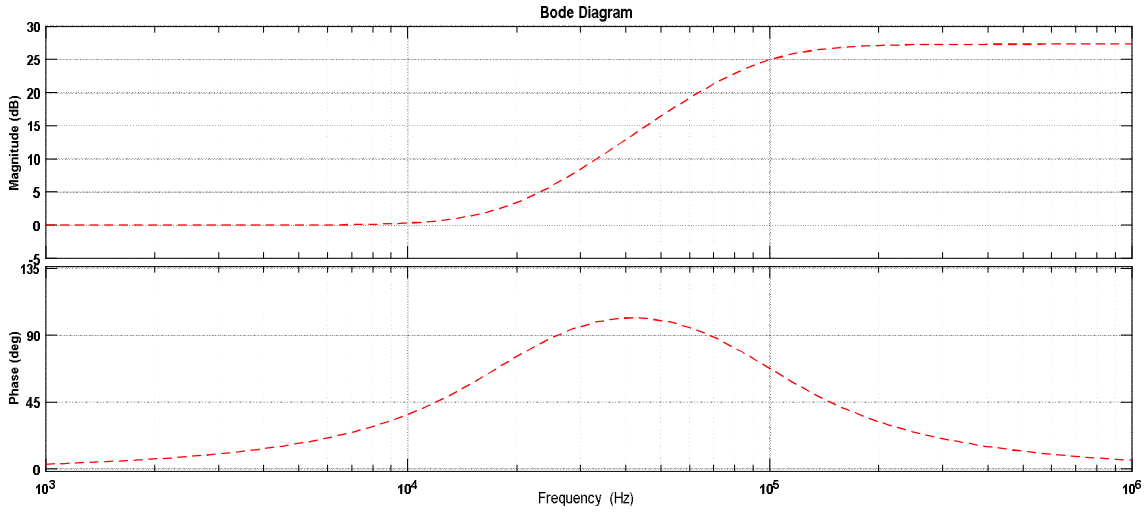


Figure 3.6 Bode plot of a complex lead compensator (damping constant: 0.707)

3.3 Discretization and Digital Controller Implementation

Digital implementation of a controller is often preferred over analog implementation due to greater flexibility, elimination of dependence on component tolerance, ability to implement complex control algorithms, reduced interference due to signal noise. However, it is dependent on sampling a continuous time system and performing control computations on the samples. Sampling a continuous time system changes the model of the system based on the rate of sampling. There are two commonly used approaches for controller design for a discretized system. One approach can

be to design the controller based on the continuous time model of the system and then discretize the controller by expressing it as a combination of integrators and using a discrete approximation such as backward Euler, forward Euler or Tustin approximation. The second approach is to discretize the model of the system, using any of the above mentioned approximations and then design the controller based on the discretized model. This approach is useful for systems which have second-order effects at frequencies close to the sampling frequency of the system. Sampling a continuous time system has a secondary effect called aliasing. As an example, a high frequency double pole beyond half of the sampling frequency (Nyquist frequency) is aliased to a lower frequency and can have an effect of reducing the phase margin of the control loop at cross-over frequency, in case the cross-over is less than a decade away from the aliased double pole frequency. Hence, this effect must be considered during control design, for cases where the sampling frequency is close to ten times the cross-over frequency and the system model reveals presence of second order effects close to the sampling frequency. Thus, the second approach to controller design can allow a more accurate controller design compared to the first approach. This is used for designing the controller in this work, even though the cross-over frequency has been limited to nearly 1.6 kHz.

For the discretization of the system, Tustin approximation is used here since it has a 90 deg phase lag characteristics for an integrator till the sampling frequency whereas the phase characteristics for backward and forward Euler diverge away from 90 deg lag as we move closer to the sampling frequency. This becomes more important as the sampling frequency moves closer to the cross-over frequency. In the present case, the sampling frequency is equal to the switching frequency (175 kHz – 215 kHz), which is much higher than the cross-over frequency (1.6 kHz) and hence, the effect of using Tustin approximation is not very significant.

The discretized model of the converter is shown in Figure 3.6 for V_{in} = 250V, light load (0.3 kW). Also plotted on the same plot is the bode plot of the continuous domain model. The sampling frequency used in this case is 175 kHz. The bode plot of the system loop gain, including the controller designed based on this discretized model is shown in Figure 3.7.

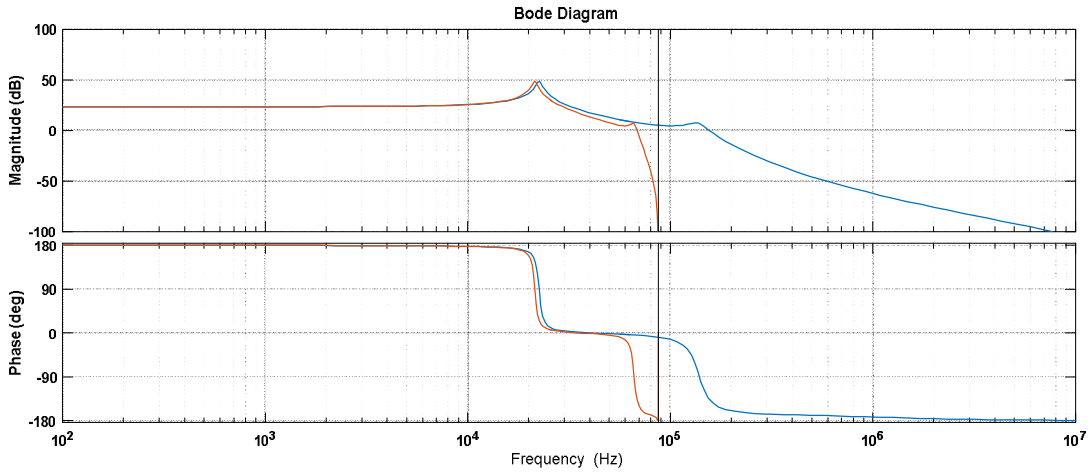


Figure 3.7 Discretized model of the converter system using Tustin approximation (sampling frequency: 175 kHz) along with continuous domain model

This controller is implemented in a Digital Signal Processor by converting the 'z' terms in the controller to 'z^{-1}' and forming a difference equation, where each 'z^{-1}' term means a delay of one sample. The hardware results based on this designed controller are presented in a later chapter.

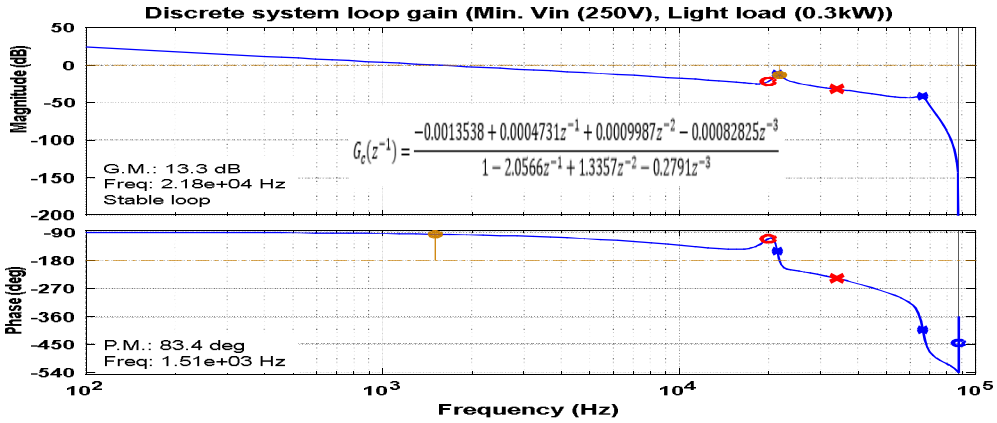


Figure 3.8 Loop-gain bode plot for controller designed with discretized system model (PM: 83.4 deg, GM: 13.3dB, cross-over: 1.51 kHz)

CHAPTER 4 SYNCHRONOUS RECTIFICATION

The LLC resonant converter, being a soft switched converter, is able to reduce the switching loss to being nearly negligible. However, conduction losses are not mitigated. A major contribution to the total device losses comes from the diode conduction in the secondary side rectifier where a current which is much higher than the primary-side (due to the high step down ratios usually present with these converters) conducts through a diode. This diode is often replaced with a device. In order to reduce these conduction losses, the device can be turned-on synchronously with the diode conduction. This means the channel of the device conducts the current, leading to the losses being the I^2R losses, which are usually much lower than the V_F*I losses in the diode. This helps improve the efficiency of the converter.

In order to further reduce the losses, efforts have been made to reduce the $R_{DS(ON)}$ of the device. With the introduction of Wide-Band Gap (WBG) devices based on GaN and SiC, a significant reduction in $R_{DS(ON)}$ has been observed. Hence, for the current prototype, GaN based devices have been used for both the primary and secondary side of the converter.

With the use of GaN devices, an issue which arises is the increase in reverse conduction drop due to the negative voltage used during turn-off (for noise immunity at the gate terminal due to high dv/dt), being added to the threshold voltage during reverse conduction. This means that synchronous rectification becomes a requirement due to thermal considerations. Moreover, with the reduced size of the devices, thermal management becomes very difficult. This points towards a need to optimize the synchronous rectification pulse duration, to minimize the period of reverse conduction in the device.

One of the main challenges to synchronous rectification in the LLC resonant converter arises for operation below resonant frequency. In this region of operation, the diode current falls to zero before the end of the switching half period. The synchronous rectification pulse must be withdrawn before the diode current falls to zero. In case the device is allowed to conduct beyond this instant, it can allow a current to flow in the reverse direction, meaning that the output capacitor is discharged. This leads to additional losses in the device and can also lead to instability in the designed controller. Thus, the SR pulse turn-on can be synchronized with the primary pulses with some constant delay whereas the turn-off needs to be tuned based on an algorithm.

Many methods of active synchronous rectification have been proposed in literature [12-16], based on sensing the tank current or sensing the secondary device V_{ds}. Many ICs are present in the market, which depend on sensing the device V_{ds} to optimize the synchronous rectification pulse. A digital implementation of synchronous rectification based on V_{ds} sense was proposed in [12]. This method has been used in the current prototype.

4.1 Digital Implementation Algorithm

The method detailed below is proposed in [12]. It is based on a diode conduction detection circuit, shown in Figure 4.1. When the diode of Q_5 is conducting, the drain of Q_5 is at a lower potential than the source node, which is the ground reference for the secondary-side circuits. This causes the diode D_1 to become forward biased and the potential at the inverting terminal of the comparator becomes equal to the drain voltage of Q_5 + the forward drop of diode D_1.This is compared with a reference voltage V_{REF}, which is selected to be slightly higher than the reverse conduction drop of

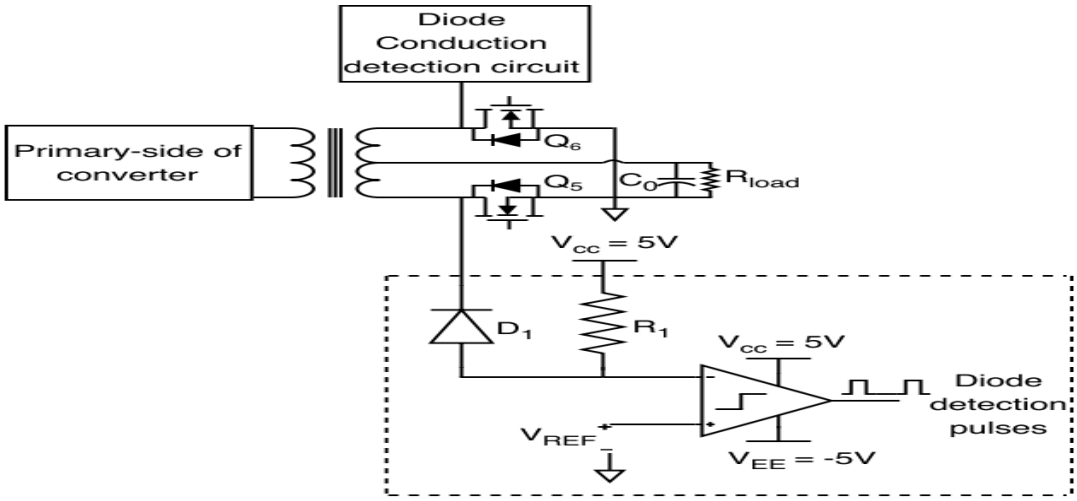


Figure 4.1 Diode conduction detection circuit (enclosed in dashed rectangle)

the device. This causes the output of the comparator to be latched high when the diode starts conducting. The output of the comparator can then be taken to a digital signal processor (DSP) using a digital isolator, to ensure isolation between the power ground and the DSP ground.

The algorithm used to optimize the synchronous rectification pulse widths using the pulses from the circuit in Figure 4.1, is shown in Figure 4.2. In the beginning, a fixed pulse width is used for the synchronous rectification pulses. The pulses from the diode conduction detection circuit are taken to a GPIO on the DSP, the state of which is monitored at the falling edge of the synchronous rectification pulses. If a high is detected, it means that there is diode conduction, in which case, the pulse width is incremented by a small value Δt, which should correspond to the minimum resolution of the controller platform used. If a low is detected, it implies lack of diode conduction, in which case, we need to reduce the pulse width, since we have gone beyond the desired diode conduction duration.

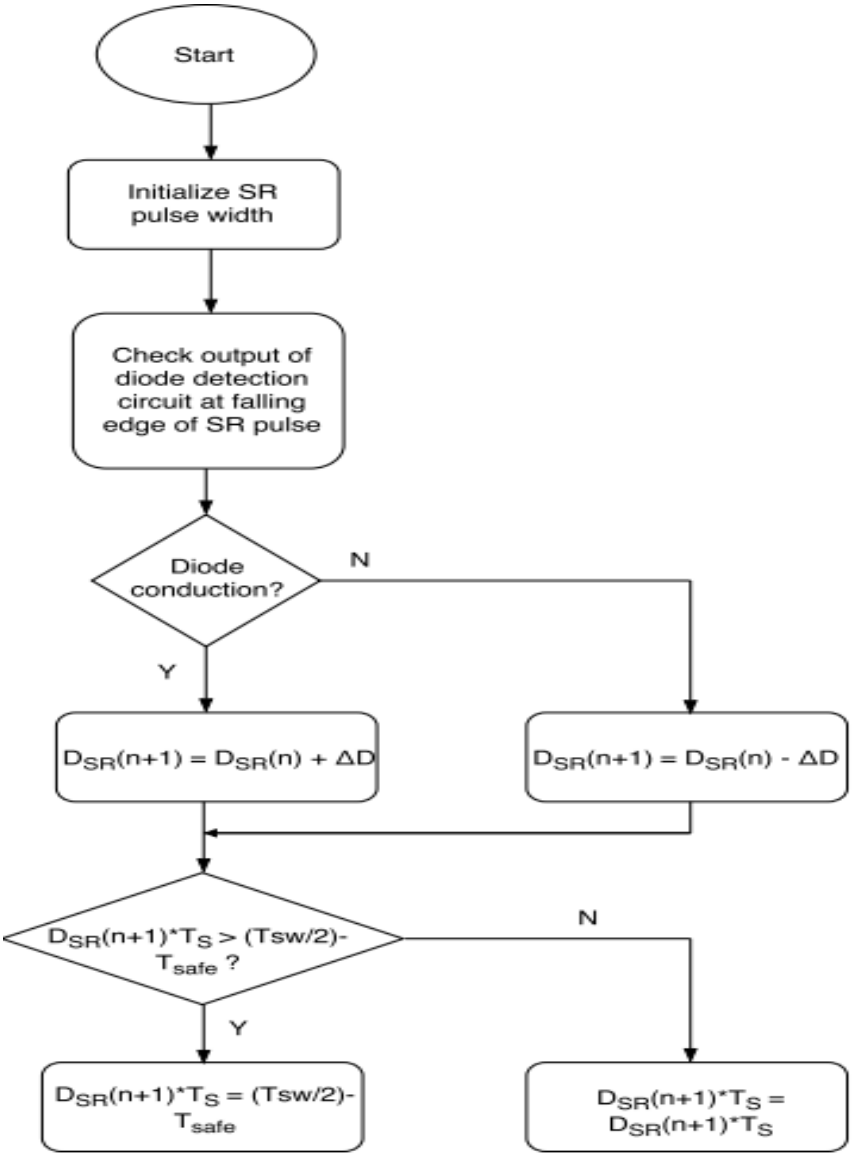


Figure 4.2 Synchronous rectification algorithm flow chart

Towards the end of the diode conduction period i.e. at the instant when the load component of tank current equals the magnetizing current, we shall observe a jitter, merely due to the logic of the algorithm. The duration of this jitter is equal to the duration of increment, Δt. It is desirable to keep this jitter at minimum, to avoid going beyond the desired diode conduction period since this can lead to circulating currents in the secondary due to the device being turned on even after the current has gone to zero, allowing the current to reverse direction and hence, discharge the output capacitor. Hence, it is desirable to keep Δt equal to the minimum resolution of the controller

platforms. As Δt increases, it can increase the duration for which the switch allows the negative current to flow, which can cause the control to become unstable. This can be a major drawback of this approach.

Moreover, the optimal pulse width is achieved after a large number of cycles since we want Δt to be small. Hence, this method can have poor transient performance.

4.2 Layout Recommendation

One important point to be considered during the layout of the diode conduction detection circuit in the above algorithm is to ensure that the drain connection and the corresponding return connections are routed as kelvin connections, i.e. the drain connection for this circuit is routed directly from the drain of the device (path 1 in Figure 4.3) rather than branching out from the power circuit drain connection (path 2 in Figure 4.3). This is to reduce the interference

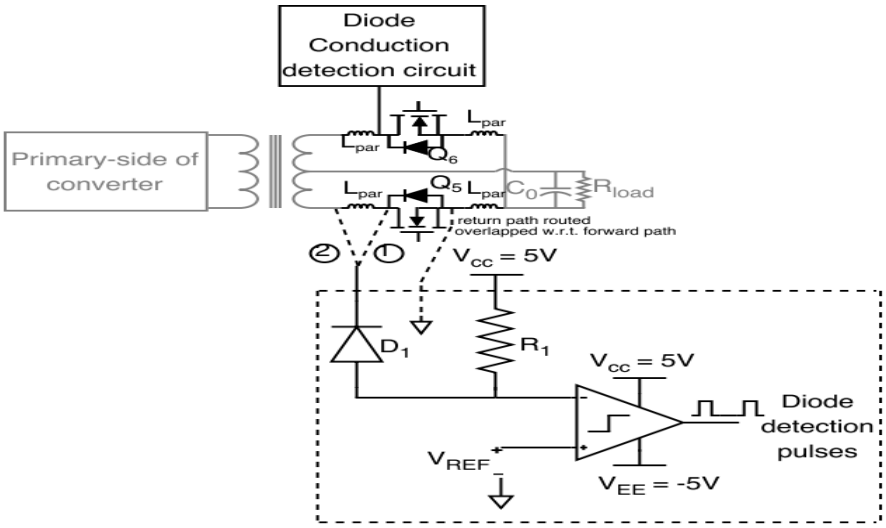


Figure 4.3 Layout recommendation for Diode conduction detection circuit. Path 1 should be used for forward path with kelvin connected return path overlapped with forward path

between the power circuit and the V_{ds} sense circuit so that it does not lead to false trigger of the comparator. This is shown in Figure 4.3.

4.3 Implementation on TI-TMS320F28335

The algorithm for Synchronous rectification using Vds sense detailed above has been implemented on TI-TMS320F28335. Two EPWM channels are used for generating the SR pulses. The counter for these channels are synchronized to the primary-side EPWM channel and a rising edge delay is provided using the DB module. The initial pulse-width is kept equal to one third of the resonant period. The two channels are 180 deg. Phase shifted from each other. The generated pulses are fed back to two GPIO pins which are designated for external interrupt at the falling edge. The Vds sense pulses are fed to two other GPIO pins which are monitored inside the respective interrupts generated by the external triggers.

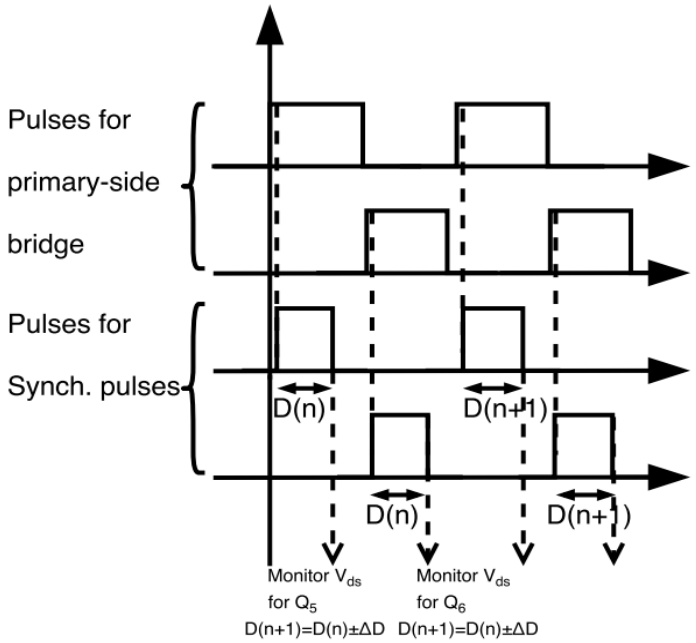


Figure 4.4 DSP implementation of synchronous rectification algorithm

CHAPTER 5 HARDWARE IMPLEMENTATION AND RESULTS

A prototype of the LLC resonant converter was developed in the laboratory. This prototype has an H-Bridge to generate the pulses to be applied to the resonant tank. As mentioned in Chapter 2, this helps reduce the device conduction losses on the primary side to half of the value compared to a half-bridge. The devices used for this H-Bridge are the GaN Systems GS66516T. These devices are rated for 650V, 60A (@25ºC) and 47A (@100ºC). The current rating for this device is much higher than required. However, the on-state resistance is very low, of the order of 25mΩ. This further helps to reduce the conduction losses on the primary side.

The secondary side rectification is using a center-tap transformer and two devices. This also helps to reduce the secondary-side conduction losses to half of the value achievable for full-bridge rectification. Moreover, it is preferable over full bridge rectification in cases where the output voltage is low since we have voltage drop from a single device instead of two devices in full-bridge rectification.

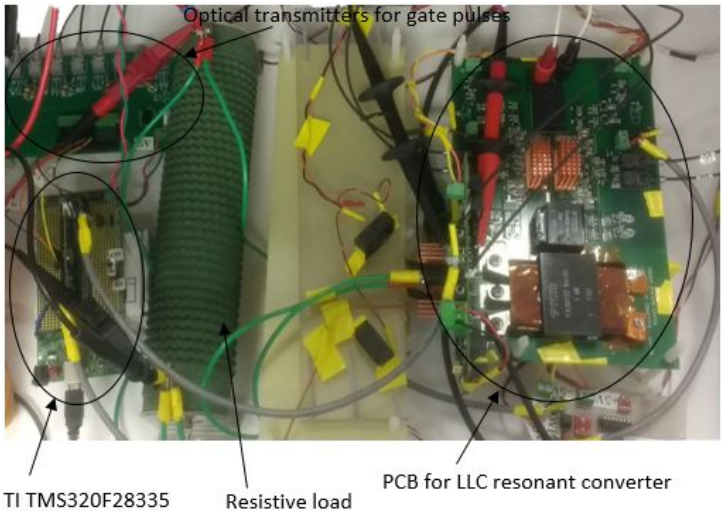


Figure 5.1 Picture of the Hardware test setup for LLC resonant converter

The image for the hardware setup is shown in Figure 5.1. The PCB for the converter has the secondary-side as a plug-in daughter card. There are two reasons for such a design. First, it helps

equalize the parasitic inductance in the secondary terminals of the transformer, which helps match the overshoots seen by the secondary devices. Second, as a future task for the project, it shall be modified for bi-directional operation, which requires the secondary side to be replaced by an H-Bridge. Hence, the daughter card design used here allows a modular design where the secondary card can be modified based on the desired application. The next section describes the specifics of the board layout.

5.1 Gate Drive Design

The gate drive design for the GaN devices used in the prototype is shown in Figure 5.2. The Figure highlights the turn-on and turn-off path for the gate terminal of the device. The gate driver IC used here is SI8271 [17]. This IC has a low UVLO (Under Voltage Lock-out) of 3V, high CMTI

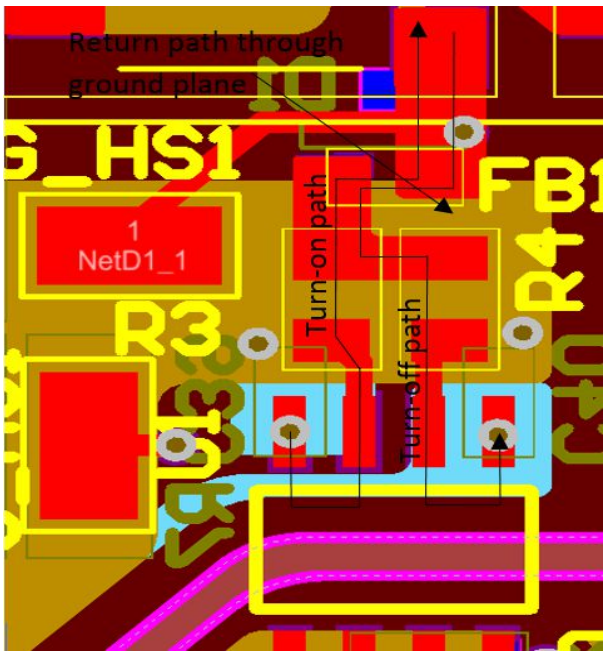


Figure 5.2 Gate Loop Design

(Common Mode Transient Immunity) of >200 kV/µs. Moreover, it has separate pins for the turn-on and turn-off processes. This eliminates the need to use anti-parallel diodes to provide separate turn-on and turn-off resistances.

Due to the high dv/dt of the GaN devices, the C_{GD} of the devices sees the high dv/dt at the turn-on of the complimentary device. This causes a current to flow through C_{GD} which can charge the C_{GS} of the device and if it is charged above the threshold of the device (which is of the order of 1.1-1.3 V for the GaN devices under use), it can lead to false turn-on of the device and partial shoot-through condition. In order to improve the gate immunity towards a false turn-on, negative gate bias is used during turn-off. Moreover, a low gate resistance is used during turn-off, compared to turn-on. This provides a parallel path for the C_{GD} current and hence, reduces the charge pushed through C_{GS} of the device, preventing it from getting charged to the threshold. Also, due to the current flowing through the C_{GD} of the device, it provides an excitation to the parasitic inductance of the gate loop and the input capacitance of the device. This is seen as a ringing in the gate of the device during turn-off. In order to damp this ringing in the gate, a ferrite bead is added in the gate path. This ferrite bead is a frequency dependent series RL component, which provides high impedance at higher frequencies and hence, helps to damp the oscillations in the gate.

Another important point to be taken care of during the layout is to minimize the area of the gate loop. A good design practice is to overlap the forward and return paths for the drain currents. This causes flux cancellation between the two paths and hence, helps reduce the effective inductance of the gate loop. Here, the return path is provided through an inner ground layer.

It must be noted that in case of the GaN devices used in this prototype, no kelvin connection has been provided for the source terminal. Hence, it must be ensured that the source connection for the gate loop is tapped from the nearest pin on the source pad, to the inner layer, where it is routed separate from the power circuit source connection. This is extremely necessary otherwise, the parasitic inductance common to the gate loop and power loop can increase. Since a high current is flowing in the power circuit, even a small common-source inductance can lead to an additional

voltage seen by the gate loop at the commutation instant. If this voltage is higher than the negative bias by the threshold voltage, it can lead to false turn-on of the device. Hence, it must be ensured that the source connection is made as a kelvin connection, even if one is not provided in the device.

5.2 Power Loop Design

The layout of the power loop has become very essential with the increased usage of Wide-Band Gap (WBG) devices. Due to the high switching speeds of these devices, the operating di/dt can be very high, especially for high current operation. This can lead to high voltage overshoots in the device V_{ds} at turn-off. Hence, it is preferable to minimize the power loop inductance, for better device reliability.

One of the techniques used for power loop inductance is to place decoupling capacitors having low ESL, right next to the top device. The high frequency switching currents required to charge the output capacitors of the devices are provided by these decoupling capacitors and the path for these currents have low inductance since they are placed very close to the devices. In the current prototype, low-ESL ceramic capacitors from TDK Ceralink series is used for the decoupling. They have a specified ESL of 2.5nH and four of these are used in parallel, reducing the effective parasitic inductance to a very small value (<1nH).

Another important concept used to reduce the power loop inductance is that of flux cancellation of the forward and return current carrying paths, when routed differentially. This can help reduce the loop inductance. The above two ideas are combined in the current prototype for the primary side H-Bridge design as shown in Figure 5.3.

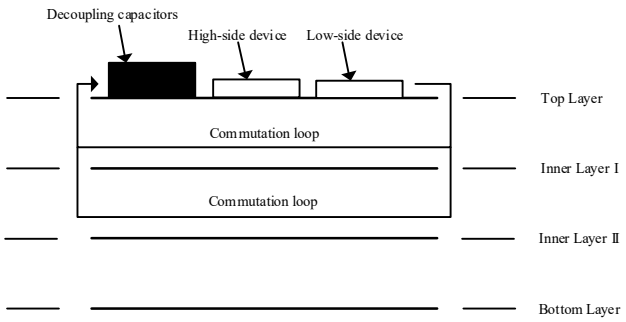


Figure 5.3 Power Loop design for Primary-side H-Bridge

5.3 Parameter Measurement of Transformer and Inductor

The center-tapped transformer and inductor used for the prototype development are acquired from Payton Planar magnetics. The reason for using a separate inductor for the resonant tank is that to allow more accurate design for the value of the resonant inductor. Moreover, we need to reduce the leakage on the secondary side to reduce overshoots in the device V_{ds}, especially above resonant frequency operation. Hence, the transformer was designed to have low leakage inductance and the inductor was designed as per the required value of L_r.

To get a low leakage inductance, and also to get a better thermal performance, an interleaved winding design was used for the transformer. Before using the transformer and inductor in the circuit, we need to extract the parasitic elements of the same, which can then be used in the simulation and analytical models to observe their effect. For this, an impedance analyzer was

utilized. The impedance curve for the inductor is shown in Figure 5.4. The parameters extracted from the curve are given in Table 5.1.

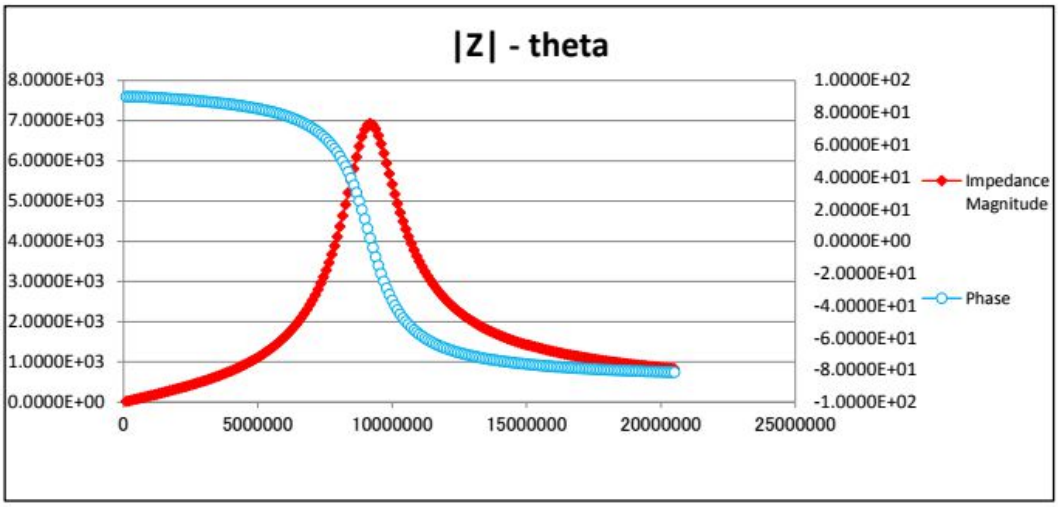


Figure 5.4 Impedance plot for resonant inductor

Table 5.1 Measured parameters for the transformer and inductor used in the prototype

INDUCTOR PARAMETERS	
Self-resonant frequency	9.28 MHz
Nominal inductance value (@ 250 kHz)	24.8µH
Effective parasitic capacitance	13 pF
Peak current rating	7.5 A
TRANSFORMER PARAMETERS	
Magnetizing inductance	94 µH
Primary referred leakage inductance	0.62 µH
Primary referred intra-turn capacitance	150 pF
Inter-winding capacitance (between primary and secondary windings) (@ 250 kHz)	3 nF

For the transformer parameters, the secondary was kept open – circuited and the impedance at the primary terminals was measured. This impedance curve is shown in Figure 5.5. Also, the nominal inductance measured in the inductive region of the impedance curve, at 250 kHz, is equal to 94.6 µH. This corresponds to the magnetizing + the leakage inductance. Moreover, from the self-resonant frequency, we can estimate the value for the primary intra-winding capacitance, which

can be modeled as an element in parallel to the primary winding. This value is computed as nearly 150pF. Next, impedance is measured with the secondary short-circuited.

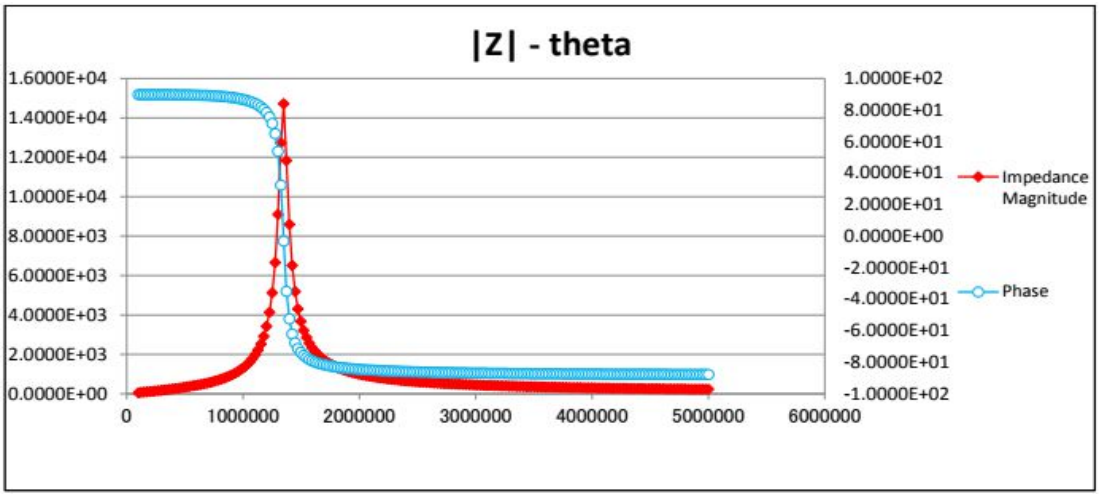


Figure 5.5 Impedance plot for transformer (secondary open-circuited)

This plot is shown in Figure 5.6. By short-circuiting the secondary winding, the magnetizing inductance and the parallel capacitance are short-circuited. Hence, from the impedance plot, we can estimate the leakage inductance value, by measuring the impedance value in the inductive region of the plot. This value is computed as 0.62 µH, referred to primary. The estimated transformer parameters are tabulated in Table 5.1. Another parasitic of importance is the inter-winding capacitance between the primary and secondary windings. This is measured between the shorted primary and shorted secondary windings. The measured value at 250 kHz is 3nF. This can be modelled between the primary and secondary winding and is important for the common-mode analysis of the circuit [18]. The model of the resonant tank with the transformer is shown in Figure 5.7.

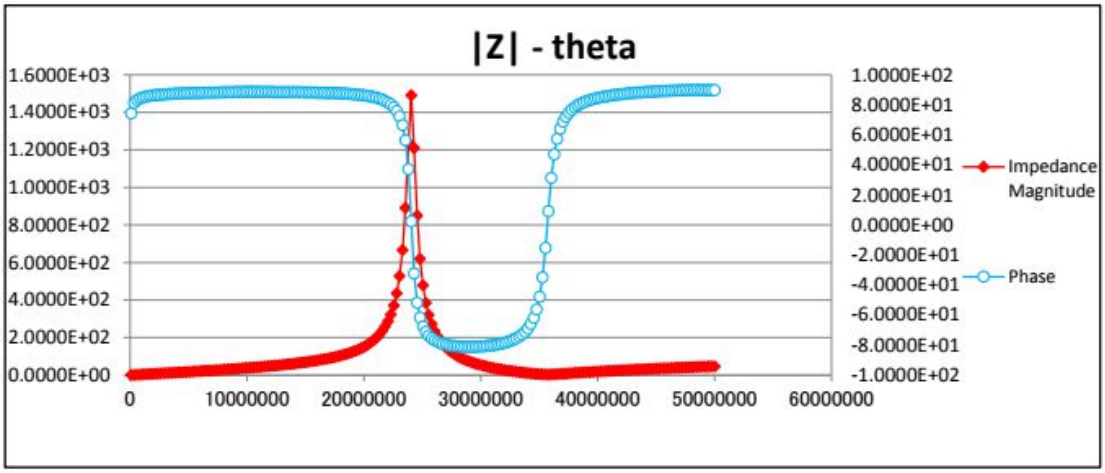


Figure 5.6 Impedance plot for transformer (secondary short-circuited)

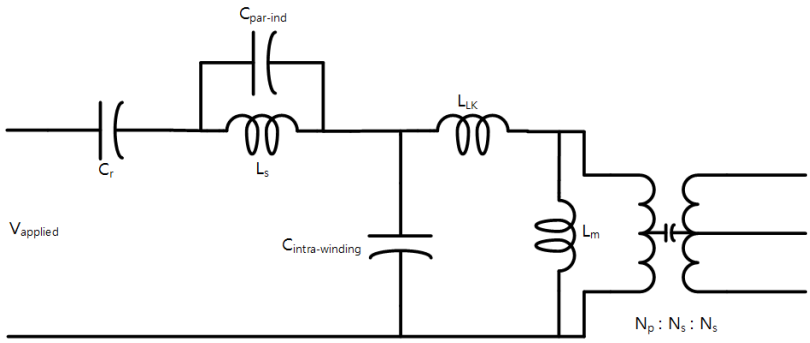


Figure 5.7 Resonant tank and transformer model extracted from measurements

Due to the deviation in the measured inductor value from the designed value, the leakage inductance of the transformer and the tolerance in the resonant capacitor value, a deviation in the resonant frequency was observed, from the designed value of 200 kHz. The estimated resonant frequency from the tank current waveforms is around 185 kHz. The revised estimated values for L_s and C_r are 25.8µH and 28.7nF respectively.

5.4 HARDWARE RESULTS:

5.4.1 OPEN-LOOP RESPONSE (V_{in} = 270V, P_{load} = 500W (approx.))

F_{sw} = 175 kHz

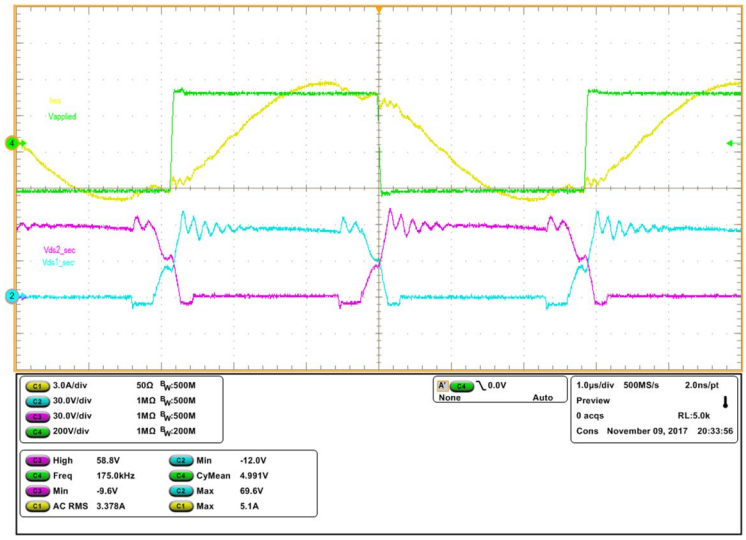


Figure 5.8 Converter operation at V_{in} = 270V and R_{load} = 1.4Ω. Resonant Tank current (Yellow), Voltage applied to resonant tank (Green), V_{ds} of secondary side devices (blue and pink). Fixed Synchronous rectification pulses are given equal to resonant half period minus safety margin

Fsw = 185 kHz

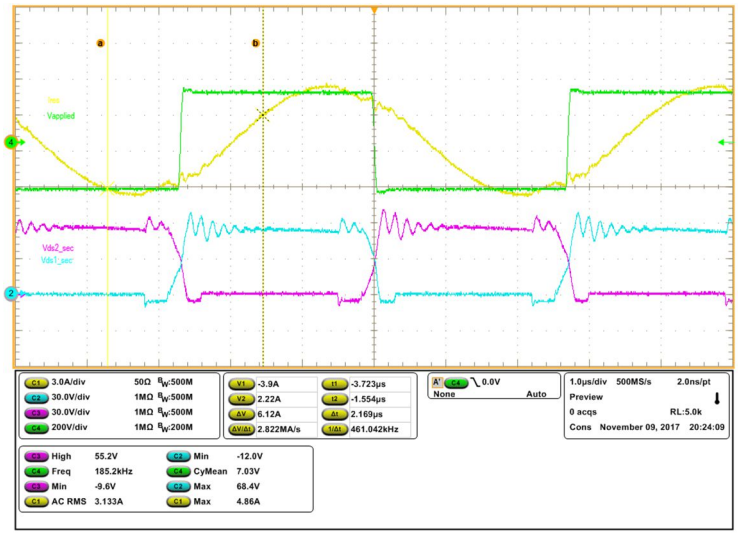


Figure 5.9 Converter operation at V_{in} = 270V and R_{load} = 1.4Ω. Resonant Tank current (Yellow), Voltage applied to resonant tank (Green), V_{ds} of secondary side devices (blue and pink). Fixed Synchronous rectification pulses are given equal to resonant half period minus safety margin

Fsw = 195 kHz

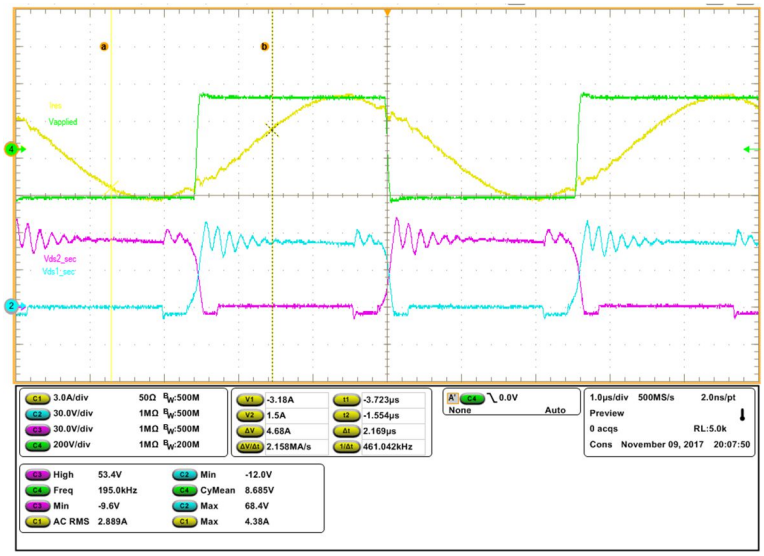


Figure 5.10 Converter operation at V_{in} = 270V and R_{load} = 1.4Ω. Resonant Tank current (Yellow), Voltage applied to resonant tank (Green), V_{ds} of secondary side devices (blue and pink). Fixed Synchronous rectification pulses are given equal to switching half period minus safety margin

Fsw = 200 kHz

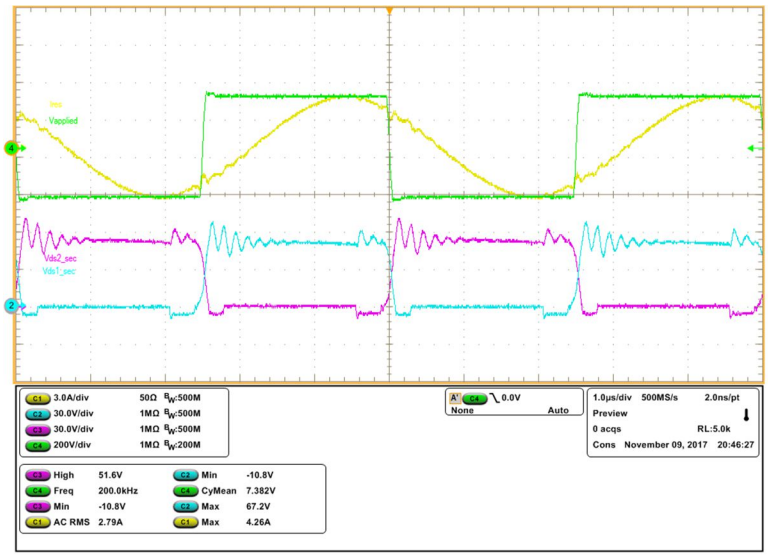


Figure 5.11 Converter operation at Vin = 270V and R_{load} = 1.4Ω. Resonant Tank current (Yellow), Voltage applied to resonant tank (Green), Vds of secondary side devices (blue and pink). Fixed Synchronous rectification pulses are given equal to switching half period minus safety margin

5.4.2 CLOSED-LOOP RESPONSE

5.4.2.1 STEP CHANGE IN V_{REF} (V_{in} = 280V, R_{load} = 1.4 Ω)

VREF from 26V to 28V

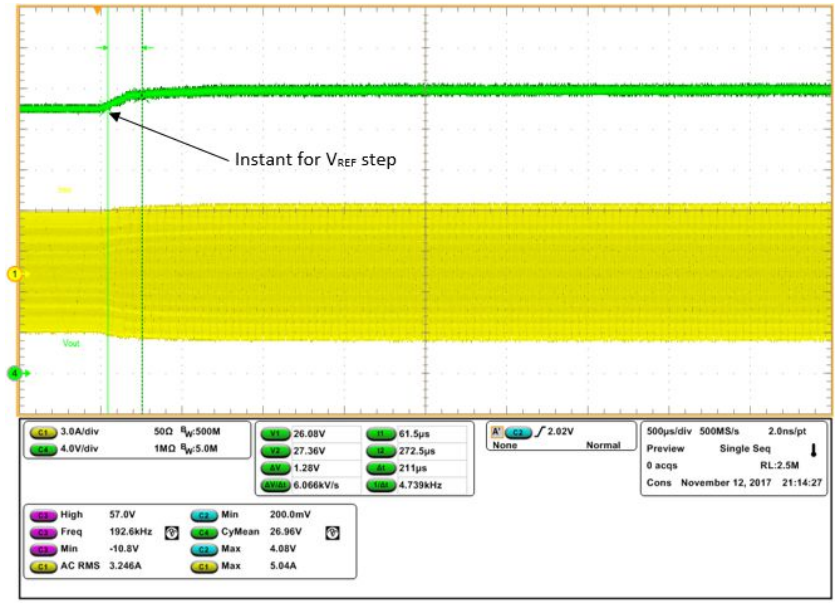


Figure 5.12 Output voltage response for step change in reference voltage from 26V to 28V. Output voltage (Green) and resonant tank current (Yellow) are shown

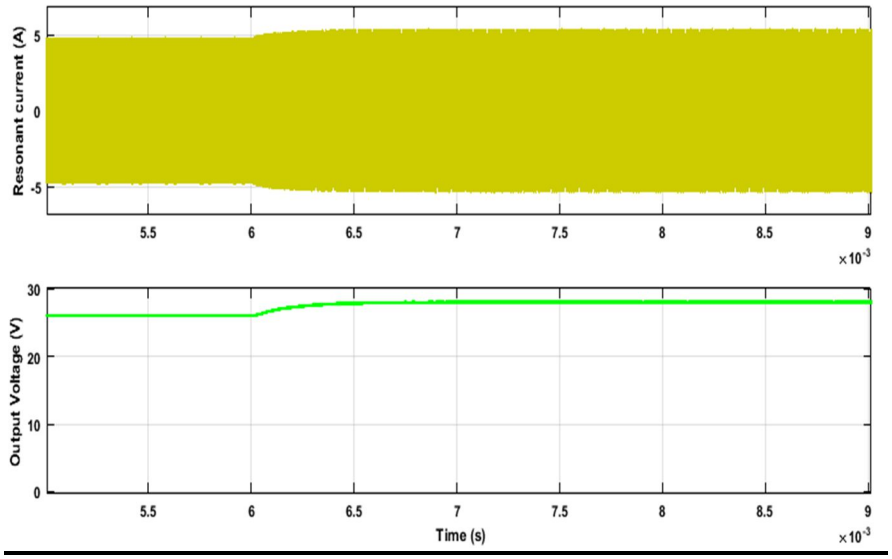


Figure 5.13 Simulation result for the output voltage response for step change in reference voltage from 26V to 28V

VREF from 28V to 26V

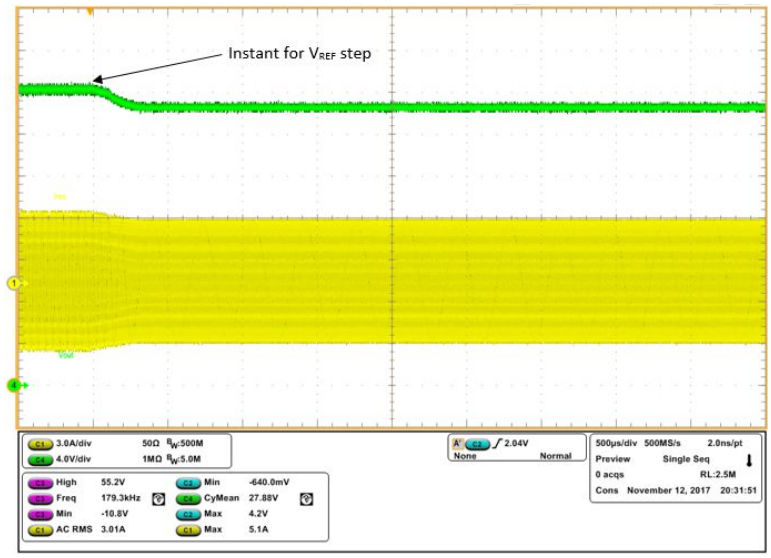


Figure 5.14 Output voltage response for step change in reference voltage from 28V to 26V. Output voltage (Green) and resonant tank current (Yellow) are shown

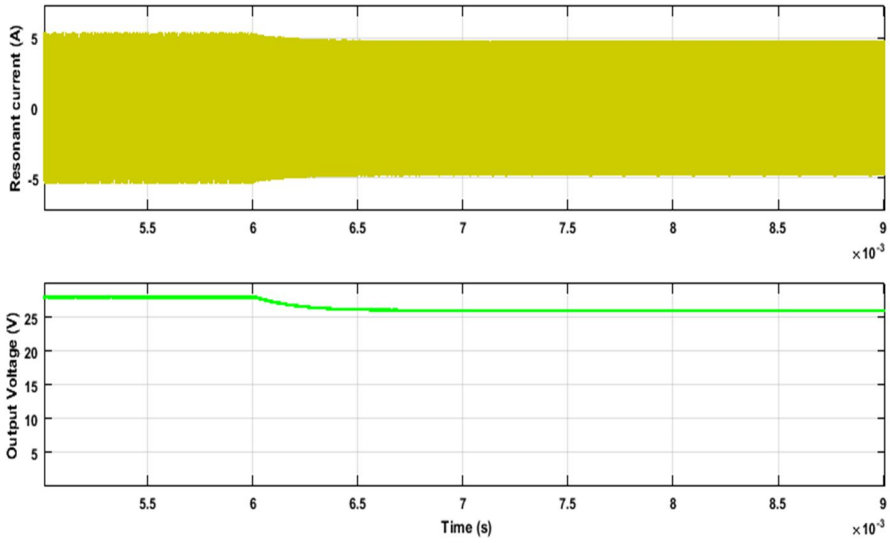


Figure 5.15 Simulation result for the output voltage response for step change in reference voltage from 28V to 26V

As can be observed from Figures 5.12 to 5.15, the hardware results and the simulation results conform very closely with each other. The settling times extracted from hardware results and simulations are 210µs and 280µs respectively. This validates the estimated resonant tank parameters and the control implementation.

5.4.2.2 STEP CHANGE IN LOAD (V_{in} = 290V, V_{REF} = 28V)
R_{load} = 1.4Ω to 1.2Ω

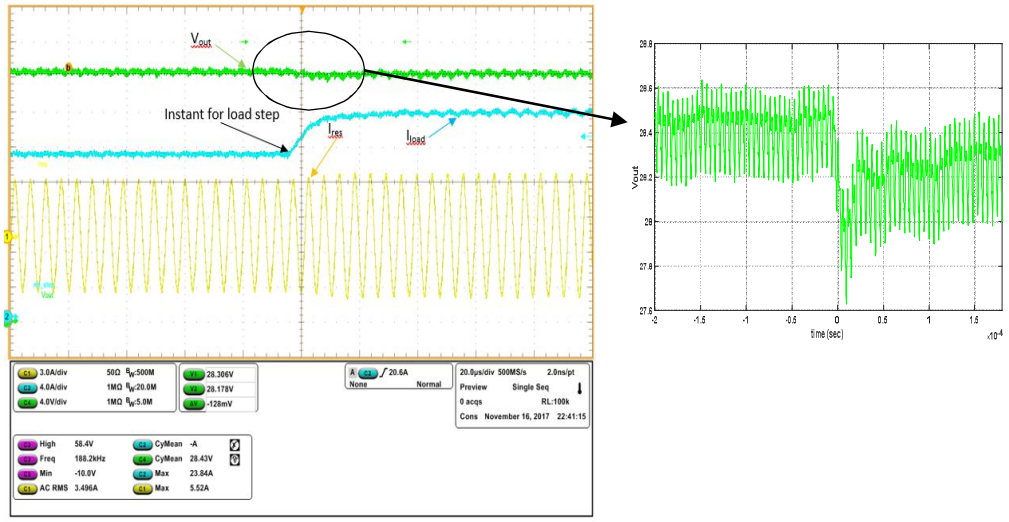


Figure 5.16 Hardware results for step change in load from 1.4 ohm to 1.2ohm. Output Voltage (Green), Load current (Blue) and resonant current (Yellow) are shown. Plot on right generated using MATLAB for clarity

It must be noted that the above result has been taken at a V_{in} of 290V. This is due to the reduction in resonant frequency from the nominal value, due to which, the minimum operating frequency is also reduced. However, since the inductor and transformer are rated for a minimum frequency of 175 kHz, the control is saturated at 177 kHz to ensure safe operation. Hence, the operating voltage is increased, to reduce the gain requirement and hence, prevent the control from saturating.

5.4.2.3 MEASURED EFFICIENCY

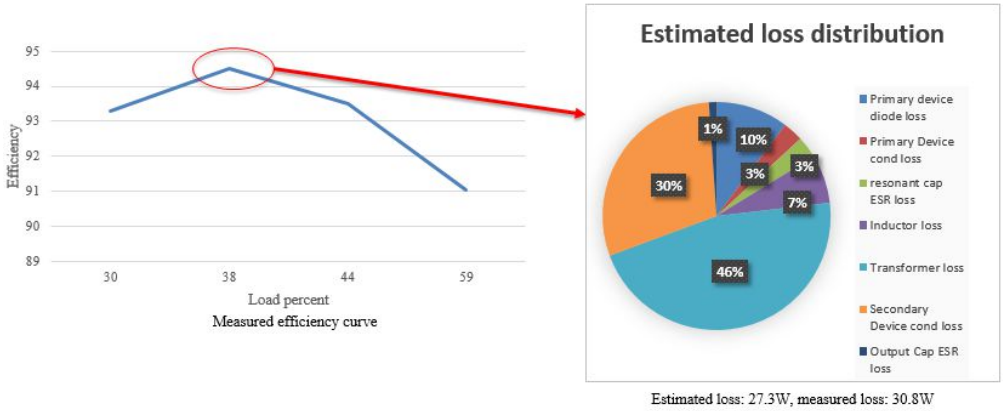


Figure 5.17 Measured Efficiency curve and estimated loss distribution for peak efficiency operating point

The converter prototype is operated with closed-loop control for different load values and the measured efficiency is plotted as shown in figure 5.17. The peak efficiency observed is 94.5% at nearly 40% loading conditions. The estimated loss distribution is also shown in the figure for the peak efficiency point. It can be observed from this plot that the transformer and secondary device losses dominate the total measured losses. It must be mentioned here that the secondary device conduction losses include the losses due to the diode conduction (i.e. duration for device off-state reverse conduction). This duration is deliberately kept large to ensure safe operation of the converter. However, by reducing the safety margins, these losses should come down.

The difference between measured and estimated losses is 3.5W. These losses may be attributed to the combination of switching losses of the devices (usually neglected for soft-switching) and losses in the snubber connected across secondary-side devices (to reduce overshoots in V_{ds}). These losses have not been included in the estimate above.

CHAPTER 6 APPLICATIONS AND CHARACTERIZATION OF FOUR-QUADRANT GaN SWITCH

A large fraction of the consumed electricity is processed by power electronics converters in modern power systems. Therefore, the efficiency of the power electronics converter is very crucial for energy efficiency. Efficient power converters can lead to better utilization of the generated electricity. Therefore the cost of energy and green-house gas emissions can be reduced. Moreover, the trend is to increase the power density of the converter in many applications (such as in automobiles, telecommunications, data centers, motor drives, and micro-inverters), since size reduction offers significant advantages in terms of the lowering the cost of the overall system. One of the ways to achieve higher power density is to increase the switching frequency, thereby reducing the size and weight of the passive components. However, due to the material limitations of the state-of-the art Silicon (Si) devices, maximum allowable switching frequency is limited. The recent advancements in the development of cost-effective Wide Bandgap (WBG) devices, such as with Silicon Carbide (SiC) and Gallium Nitride (GaN), offer significant advantages over Si devices and being seriously considered in many applications.

The on-state resistance of the WBG devices is significantly smaller than Si devices, thanks to the higher breakdown field of WBG semiconductor. In addition, high electron mobility in GaN leads to very small ON state resistance compared to SiC and Si devices [19]-[21]. As a result, smaller die size can be achieved using GaN semiconductor for a given current rating. The inherent advantage of the small die size is the reduction in the input, output, and reverse transfer

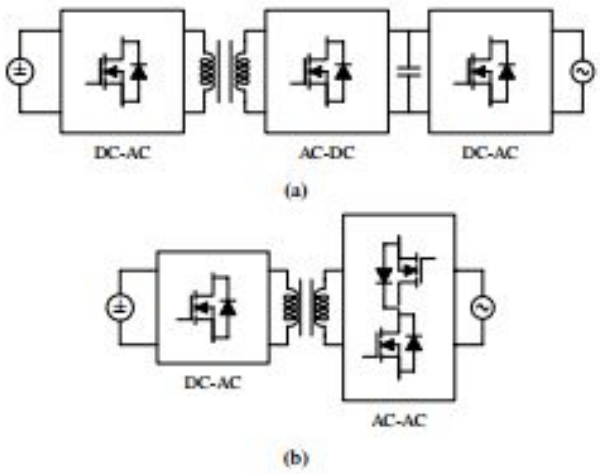


Figure 6.1 (a) Conventional AC-DC power architecture and (b) High-frequency link inverter using cyclo-converter

capacitance, which enable faster switching transients and lower switching losses. These properties of GaN devices make them very favorable in high efficiency, high power density applications.

The use of GaN devices can significantly improve the efficiency and power density of converters. Further improvement can be obtained by adopting power conversion architectures with the least number of cascaded stages. Conventional approaches of ac-dc conversion (ac source feeding the dc load), ac-ac conversion (motor drives), and dc-ac conversion (renewable energy integration) involve multiple power stages. These multiple stages are often decoupled from each other using intermediate passive elements, which occupy significant volume and compromise the power density and reliability. The conventional approach of isolated dc-ac power conversion is shown in Fig. 6.1(a). Three cascade stages are used, which compromise the efficiency. DC-link capacitors are used to decouple the dynamics of ac-dc rectifier stage

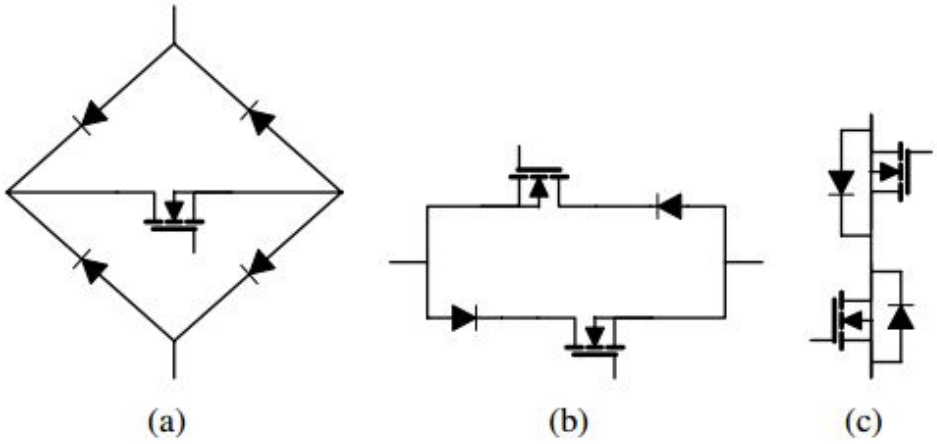


Figure 6.2 Conventional arrangements for four quadrant switch realization. (a) Using diode bridge and single switch, (b) Current switch, realized using series connection of switch and diode, (c) Common drain configuration

and dc-ac inverter stage, which reduces reliability and power density. A high frequency link inverter to realize the same functionality [22] is also shown in Fig. 6.1(b). A cyclo-converter is used on the secondary side of the medium frequency transformer, which combines the functionality of rectifier and inverter stages. A basic building block of the cyclo-converter is the four quadrant switch, as shown in Fig. 6.1(b). In addition to the high frequency link inverter shown in Fig. 6.1(b), this switch also finds its application in matrix converters, power supplies, solid-state transformers, Vienna rectifiers, battery chargers, etc.

The conventional approaches for realizing the four-quadrant switch are shown in Fig. 6.2. For the switch arrangement shown in Fig. 6.2(a), current flows through three devices for any direction of current flow. This leads to higher semiconductor losses. However, only one switch is used in this arrangement and thereby greatly simplifies the gate drive arrangement. In the other two arrangements shown in Fig. 6.2(b) and Fig. 6.2(c), four devices are used to realize the switch and current flows through one switch and one diode for either direction of the current flow. The size and semiconductor losses of the bi-directional switch can be greatly reduced by using a single die to realize the bi-directional switch.

This paper discusses GaN based four quadrant switch (FQS). The high voltage lateral design enables this FQS to be made as a single device. As a result, cost reduction and smaller size can be achieved. Experiments were performed to obtain static and dynamic characteristic of the FQS. The on-state resistance at different junction temperatures are obtained along with the switching energies. This chapter is organized as follows: The switch is introduced in section 2. Switch characterization is presented in section 3. Static characterization is performed, where the on-state resistances are obtained along with the output characteristics. In addition, the transfer characteristics and leakage current are also measured. A double pulse test setup has been built, as discussed in Section 4. Dynamic characterization has been performed where the turn-on and turn-off switching energies are obtained.

6.1 Four-Quadrant Switch

An FQS GaN switch in a SOIC-16 package, manufactured by Transphorm Inc. is shown in Fig. 6.3(a). The switch has a voltage blocking capability of 600V and current handling capability of 5A. It has 8-pins and two thermal tabs, provided to facilitate heat extraction from the device. The pin configuration is shown in Fig. 6.3(a) and the symbol is shown in Fig. 6.3(b). FQS has two current carrying terminals T_1 and T_2. The current can flow in either direction when the device is on and can be blocked, irrespective of the polarity of the applied voltage across the switch when the device is off.

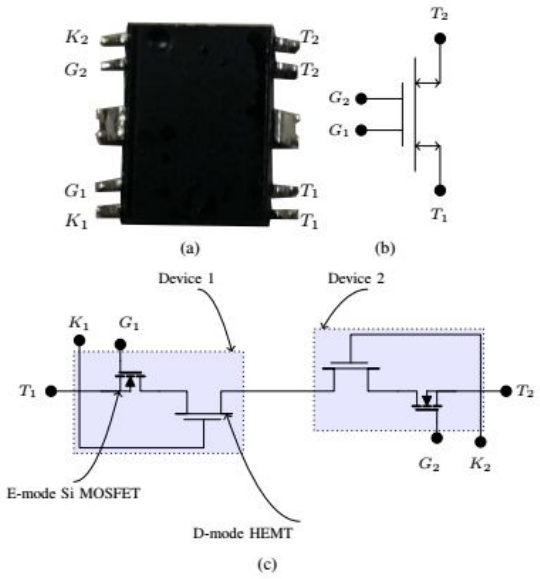


Figure 6.3(a) Four quadrant switch in SOIC-16 package, (b) Pin configuration of the four quadrant switch, (c) Four quadrant switch realization using a depletion mode gallium nitride high electron mobility FQS and enhancement mode low voltage silicon MOSFETs -- the single chip GaN FQS has been schematically broken in two to facilitate explanation of device operation

The detailed description of the FQS is shown in Fig. 6.3 (c). The FQS is realized using a 600 V depletion mode (D-mode) GaN High Electron Mobility Transistor (HEMT), configured in a common drain configuration with gates on opposite sides of the shared blocking region. Since a normally-on D-mode GaN FQS is used, to make the FQS a normally off switch, additional low voltage enhancement mode (E-mode) silicon MOSFETs are connected in series with the D-mode GaN FQS to realize a cascoded FQS, as shown in Fig. 6.3(c). The E-mode silicon MOSFETs are used to gate the D-mode GaN FQS. Therefore, the low voltage silicon MOSFET has very small influence of the on-state resistance of the FQS. Moreover, the loss associated with the reverse recovery of the body diode is also relatively small.

When positive voltage is applied across the terminals T_1 and T_2 of the FQS ($V_{T1} > V_{T2}$), the device 2 acts as a controlled switch that can block the applied voltage when low gate-source bias is applied ($V_{G2K2} \leq 0$). With the E-mode silicon MOSFET of the device 2 off, negative voltage gets applied across the gate terminal of the D-mode GaN HEMT of the device 2. As a result, electrons in the

two-dimensional electron gas (2DEG) are depleted and the GaN FQS blocks in this direction. The applied voltage appears across the device 2 and is mainly blocked by the 600 V GaN HEMT. The bias voltage across the gate of device 1 (V_{G1K1}) does not have any major influence on the basic operation during this state. The current can be allowed through the FQS by turning on the E-mode silicon MOSFET of the device 2. By turning on E-mode MOSFET of device 2, almost zero voltage is applied across the gate terminal of the D-mode GaN HEMT of the device 2 and the 2DEG forms and the device conducts. On the side of device 1, the body diode of the MOSFET conducts if the MOSFET is off. The drop across the full device can be reduced by turning on the E-mode MOSFET of device 1.

When negative voltage is applied, i.e $V_{T2} > V_{T1}$, device 1 acts as a controlled switch. Current through the FQS can flow by applying high gate-source bias to the device 1. Similarly, the current can be interrupted by turning off the device 1 by applying low gate-source bias.

The typical application of the FQS in a cyclo-converter is shown in Fig. 6.4. Two FQSs (FQS 1 and FQS 2) are used to realize the half-bridge converter. Terminal T_1 of the 1st FQS switch (referred to as a FQS 1) is connected to the line terminal of the ac source, whereas the neutral terminal is connected to terminal T_1 of the FQS 2. Terminal T_2 of both the FQSs are connected to form the common connection point c, which is connected to the inductive element, as shown in Fig. 6.4. The other end of the inductive element is connected to the reference node (which is at the mid-point of the ac supply voltage) as shown in Fig. 6.4. To clamp the common point to the line

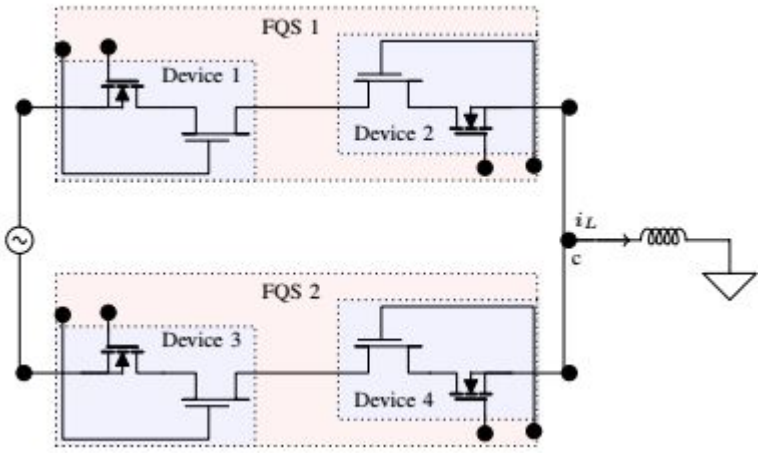


Figure 6.4 Four-Quadrant Switch in typical cyclo-converter applications.

terminal of the ac source, FQS 1 must conduct. On the other hand, FQS 2 has to conduct to clamp the common point to neutral terminal. For the positive direction of inductor current i_L during the positive half cycle of the ac voltage, the device 2 of FQS 1 acts as a controllable switch and blocks the voltage. During the conduction of FQS 1, high gate-source bias is applied to device 2 of FQS 1. The Device 1 of FQS 1 is also subjected to the high gate-source bias to reduce the device drop. To clamp the common connection point to the neutral point, the inductor current needs to be transferred from FQS 1 to FQS 2 without interruption. One of ways to achieve this is to apply following sequence:

- Apply low gate-source bias to the device 1 of FQS 1.
- Apply high gate-source bias to the device 4 of FQS 2.
- Withdraw gate pulse from device 2 of FQS 1.
- Apply high gate-source bias to device 2 of FQS 2. This helps in reducing the voltage drop across the device.

6.2 Static-Characterization

The static characterization of the FQS was performed using B1505A Power Device Analyzer from Keysight Technologies. The voltage across the two power terminals (V_{T1T2}) and current through the device were measured. Since the FQS comprises two devices, the voltage across the FQS is given as

$$V_{T1T2} = V_{1DS} + V_{2SD} \tag{6.1}$$

where V_{1DS} is the drain to source voltage of device 1 and V_{2SD} is the source to drain voltage of the device 2 of the FQS. Negative voltage is applied across the FQS. Gate-source bias voltages of 3.75 V is applied to the device 1 of the FQS, whereas the gate and source terminals of the device 2 are shorted. As a result, the D-mode GaN HEMT of the device 2 conducts in a reverse direction which is in series with the body diode of the device 2. As a result, the voltage drop across the body diode is clearly visible in the output I-V characteristic, shown in Fig. 6.5. The voltage drop across the body diode of the silicon MOSFET of device 2 determines the channel enhancement of the D-mode HEMT of the device 2. On the other hand, device 1 of the FQS conducts in a forward direction and enhancement of the D-mode HEMT depends on the gate source voltage applied.

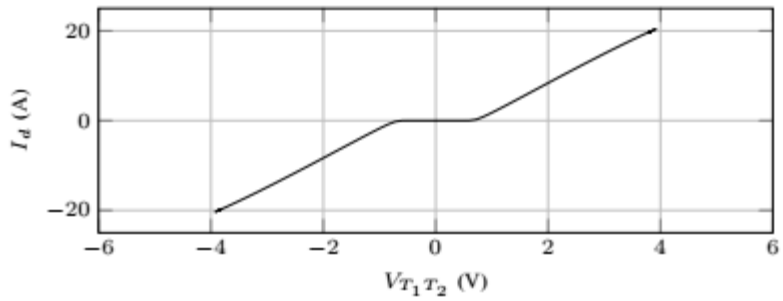


Figure 6.5 Output I-V characteristic at room temperature. The gate-source bias voltage of 3.75 V (V_{G1K1}=3.75 V) is applied to device 1, whereas the gate source terminal of the device 2 are shorted (V_{G2K2}=0 V)

Similar results with the positive voltage applied across the FQS are also obtained, as shown in Fig. 6.5.

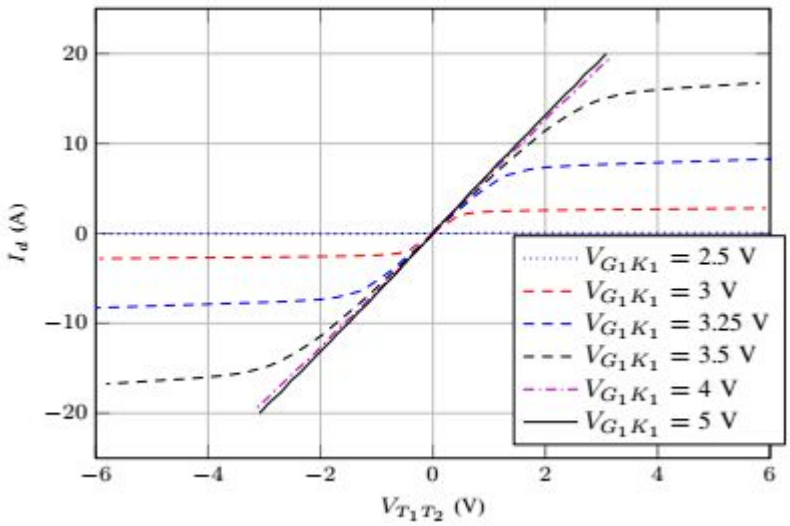


Figure 6.6 Output I-V characteristic, measured at room temperature. Variable gate-source bias voltage applied to the device 1 and high gate-source bias is applied to device 2 (V_{G2K2}=6 V).

The voltage drop across the device can be reduced by allowing current to flow through the MOSFET channel rather than let body diode conduct. This can be achieved by applying high gate-source bias to device 2 and the corresponding output I-V characteristic is shown in Fig. 6.6. The gate-source bias voltage of 6 V is applied to device 2, so that the MOSFET channel conducts. Variable gate-source bias voltage is applied to device 1 and the voltage drop across terminals T_1 and T_2, as well as device current are measures, as shown in Fig. 6.6.

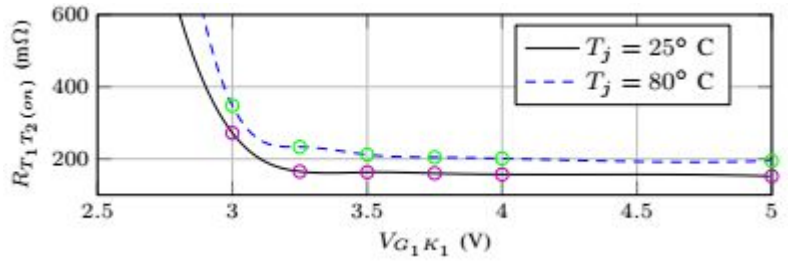


Figure 6.7 On state resistance of the four-quadrant switch as a function of the gate-source bias voltage of the device 1 for different junction temperatures. High gate-source bias is applied to device 2 (V_{G2K2}6 V).

The on-state resistance of the FQS $R_{T1T2(on)}$ as a function of the gate-source bias voltage of the device 1 is shown in Fig. 6.7. High gate-source bias is applied to the device 2. The on-state resistances are obtained for different temperatures. The on-state resistance is significantly lower once the gate-bias voltage is higher than 3.5 V. With full channel enhancement at V_{G1K1}=5 V, the on-state resistance at the junction temperature of 80°C is 197 mΩ, which is 28% higher than the on-state resistance at room temperature with the similar gate-source bias conditions.

The transfer characteristics of the FQS is measured at room temperature and it is shown in Fig.

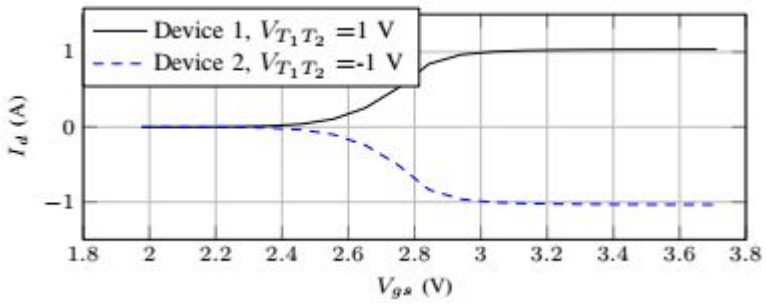


Figure 6.8 Transfer characteristic of both the devices of the four-quadrant switch at room temperature.

6.8. The relationship between the device current and the gate source voltage is obtained for both the devices of the FQS. The leakage current as a function of the blocking voltage at the room temperature is shown in Fig. 6.9. Variable voltages are applied to the terminals of the FQS and the device current is measured for both positive and negative blocking voltages, with the leakage being below 25nA to 500V.

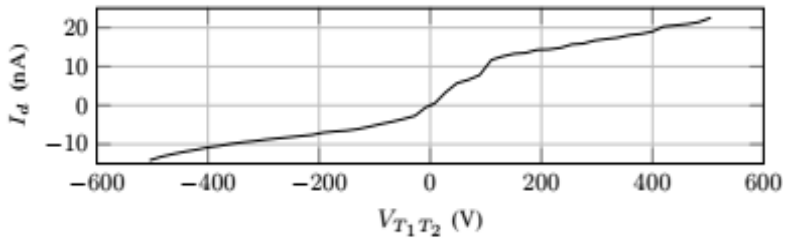


Figure 6.9 Leakage current as a function of the blocking voltage. The measurement was done at the room temperature

6.3 Dynamic-Characteristics

The dynamic characterization of the FQS is performed to evaluate switching performance. The Double Pulse Test (DPT) test circuit has been built and the switching energies evaluated. The detailed discussion on the test setup and the results are presented in this section.

6.3.1 Double Pulse Test Circuit

Fig. 6.10 shows the double pulse test circuit for the switching loss characterization. Two FQSs are used in a bridge leg configuration, where one of the FQSs is used for the switching loss characterization (DUT) and the other FQS is used for free-wheeling the inductor current. Current shunt is used for the device current measurement. Surface mount package is used to minimize the impact of the inductance on the power loop. The voltage across the DUT (FQS 1) was measured using a single ended voltage probe, which is probed with respect to the negative terminal of the dc-link. The device voltage is then obtained by subtracting the voltage drop across the current shunt from the measured voltage. The voltage drop across the shunt was also measured using a single ended probe. Since same type of single ended probes are used for both the voltage and current measurement, the measurement error due to the probe de-skew is minimized.

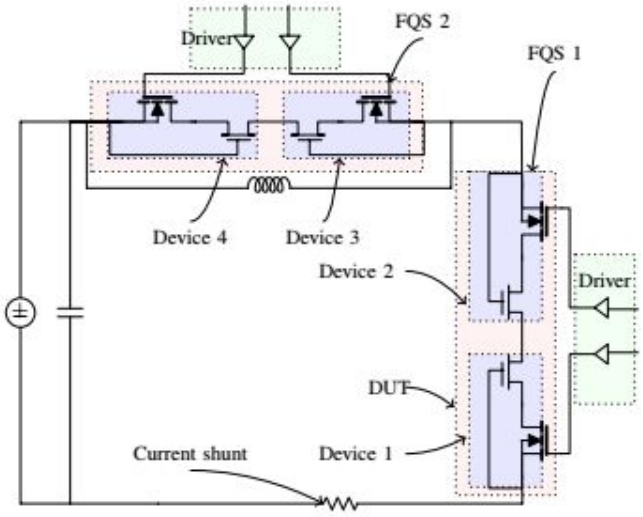


Figure 6.10 Test setup for switching loss characterization

Two channel gate drivers with digital isolator from SiliconLabs is used to drive the E-mode silicon MOSFET. GaN based FQS is subjected to very high rate of change of voltage during the switch transition. High dv/dt could lead to the interference with the control signals due to the flow of the common-mode current through the parasitic capacitance of the gate driver power supply. Isolated power supplies with low inter-winding capacitance from Murata power solutions are used.

The PCB layout for the DPT board is shown in Fig. 6.11(a), with the gate loop and power loop encircled. Due to the fast switching speed and low threshold voltage of the device, the power loop and gate loop design need to be very tight to get cleaner waveforms and reliable operation. The power loop is shown in the Fig. 6.11(c). The bottom device is placed on the top layer and the top device is placed on the bottom layer. This allows the current carrying terminals, T_1 and T_2 for the two devices to be placed one on top of the other, enabling a very low inductance connection to be made between the two devices through multiple vias. This placement also helps reduce the commutation loop area, in turn reducing the power loop inductance. Ceramic decoupling caps are kept very close to the T_1 terminal of the bottom device to help reduce the parasitic inductance.

The gate loop design is shown in Fig. 6.11(b). Decoupling caps are kept just below the gate driver power pins, on the layer opposite to the gate drive IC. This minimizes the distance of the caps from the power supply pins. The kelvin source connection provided in the device helps eliminate the common source inductance. The return path is provided through a ground plane on the second layer, allowing mutual inductance cancellation between the forward and return paths, ensuring a low gate loop inductance. The image of the Characterization setup is shown in Fig. 6.12. The air core inductor used for the testing is also shown. It is a hand-wound inductor with single layer of winding using AWG #24 wire and spacing between the turns to ensure lower parasitic inter-turn capacitance for the inductor.

However, using a higher gauge wire leads to increased winding resistance which can lead to the currents at the two ends of the free-wheeling period to be unequal. A solution can be to reduce the duration of the freewheeling period to lower the drop in current during this interval.

Figure 6.12 Double pulse test setup for the dynamic characterization.

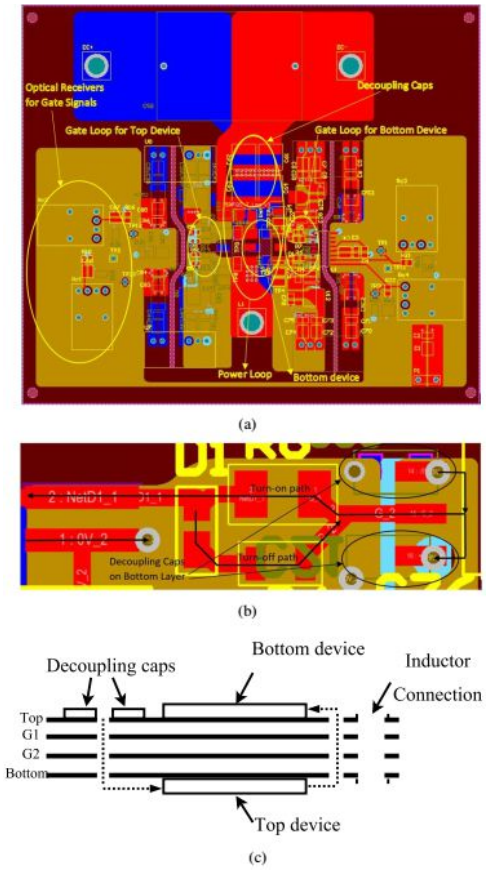


Figure 6.11 (a) DPT board layout showing gate loop and power loop, (b) Gate loop design for the Bottom device, (c) Power Loop design

6.3.2 Switching Energies

The double pulse test was done with device 1 of FQS 1, whereas the gates of device 2 and device 3 were biased off. Positive bias was applied to the gate of the device 4 to provide the free-wheeling path. The DPT was performed at the room temperature. Gate-source bias voltage of ±9 V is used. Separate turn-on and turn-off resistances gate resistances were used. The turn-off resistance is kept constant at 1Ω, whereas the turn-on resistance values were varied. Two sets of readings with turn-on resistance of 15Ω and 20Ω are obtained for different drain currents. The dc-link voltage is maintained at 350V.

The turn-on and the turn-off transients for the drain current of 4.8 A are shown in Fig. 6.13 and Fig. 6.14, respectively. The associated instantaneous power loss during the transient are also shown in Fig. 6.13(b) and Fig. 6.14(b), respectively. The variation of the turn-on energy loss with the device current for two different gate resistances are shown in Fig. 6.15. The turn-on energy loss with a gate resistance of 20Ω is lower compared to the turn-on energy loss with gate resistance of 15Ω. This is due to the higher current overshoot, which is proportional to the initial rate of change of voltage dv/dt.

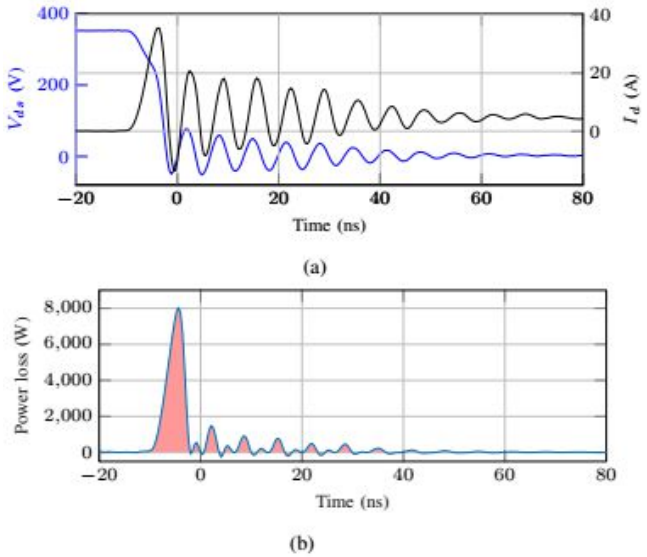


Figure 6.13 Voltage and current waveforms during the turn-on switching transient. The dc-link voltage is 350 V and the drain current is 4.8 A. The turn-on gate resistance is 15Ω

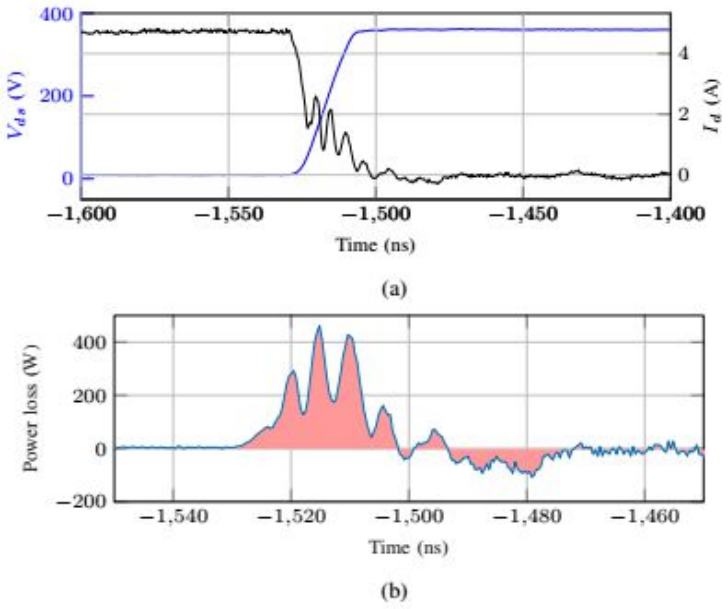


Figure 6.14 Voltage and current waveforms during the turn-off switching transient. The dc-link voltage is 350 V and the drain current is 4.8 A. The turn-on gate resistance is 15Ω

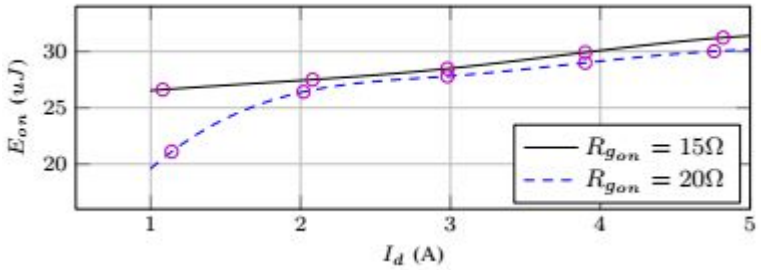


Figure 6.15 Turn-on energy loss variation with drain current. The DC bus voltage is 350V.

Just before the DUT is turned on, the FQS 2 (upper device) was free-wheeling the inductor current. As a result, the voltage across FQS 2 was almost zero, which also leads to higher output capacitance (917 pF at 1 V) for FQS 2 as shown in Fig. \ref{cv}. When DUT is turned on, the output capacitance of upper device FQS 2 has to charge to the dc-link voltage. As a result, the upper device output capacitance along with the parasitic capacitance of the inductor draws current, which is proportional to the dv/dt. The initial rate of change of voltage dv/dt with 15Ω turn-on gate resistance is measured to be 21.3 V/ns as against the dv/dt of 16 V/ns for the turn-on gate resistance of 20Ω. Initial dv/dt for both the cases are also shown in the Fig. 16(a). Higher dv/dt with turn-on resistance of 15Ω leads to higher current overshoot, as shown in Fig. 16(b). In addition, the diode

reverse recovery current of the body diode of the silicon MOSFET of FQS 2 also contributes to the current overshoot. The current overshoot with turn-on resistance of 15Ω is measured to be 35.5 A as against 30.7 A in the case of 20Ω turn-on resistance.

To determine the contribution of the parasitic capacitance of the inductor towards the current overshoot, the inductor current during the turn-on transient was measured, as shown in Fig. 6.18. The inductor current remains almost constant during the turn-on transient, thanks to the unique design and winding arrangement of the inductor. Therefore, it has been verified that the high dv/dt along with the high output capacitance of the device and the reverse recovery current of the MOSFET.

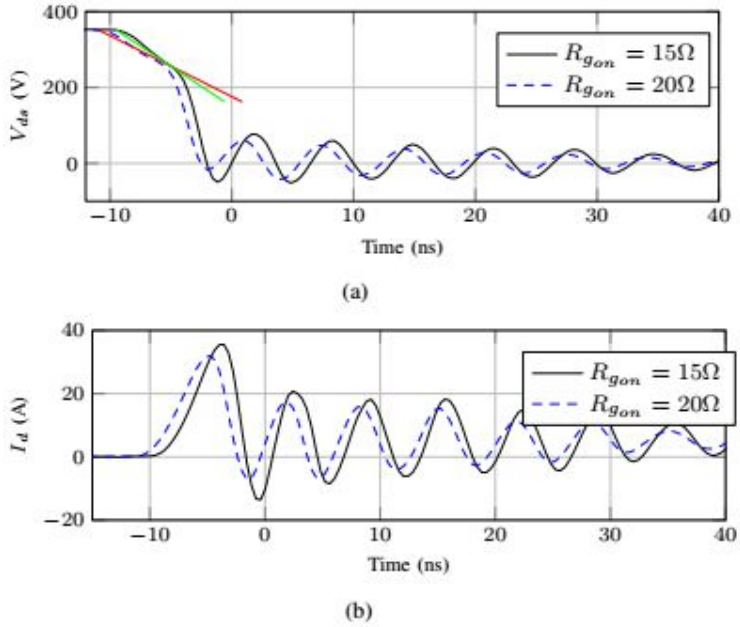


Figure 6.16 Voltage and current waveforms during the turn-on switching transient for different values of the turn-on gate resistances. The dc-link voltage is 350 V and the drain current is 4 A.

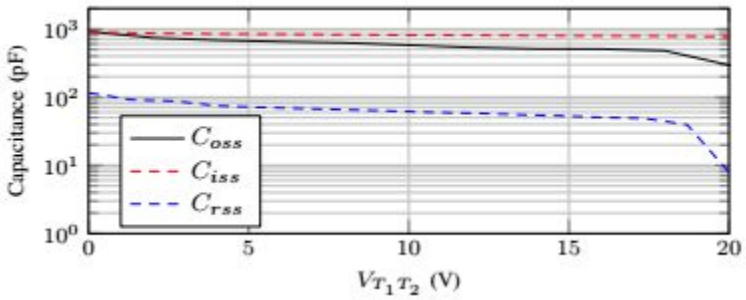


Figure 6.17 Variation of the reverse transfer capacitance C_{rss}, input capacitance C_{iss}, and output capacitance C_{oss} with the terminal voltage V_{T1T2}.

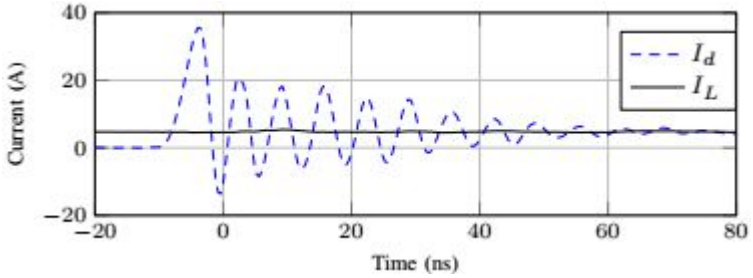


Figure 6.18 Inductor current during the turn-on transient. The oscillations in the inductor current is small and the inductor current remains almost constant.

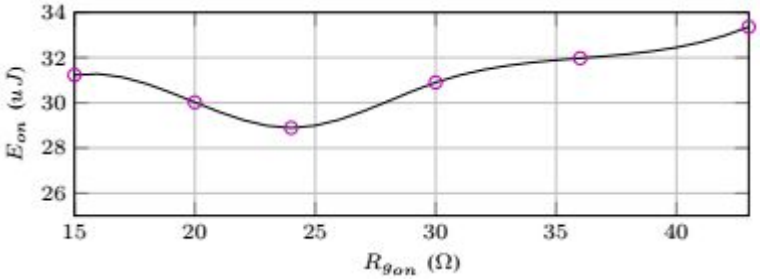


Figure 6.19 Turn-on energy loss variation with the turn-on gate resistance. The dc-link voltage is 350 V and the inductor current is 5 A.

To obtain an optimal turn-on gate resistance, turn-on energy loss is measured for different turn-on gate resistance values, as shown in Fig. 6.19. With increase in gate resistance values, the initial dv/dt decreases. This leads to reduction in the current overshoot. On the other hand, it increases the turn-on transient time. The reduction in current overshoot has a positive impact on turn-on switching loss reduction, whereas turn-on switching loss is negatively impacted by the increase in the turn-on transient time. The best compromise between the current overshoot reduction and turn-on transient time results into lowest turn-on loss and it is obtained for the gate resistance of 24Ω, as shown in Fig. 6.19.

The turn-off energy loss variation with the drain current is shown in Fig. 6.20. The turn-off resistance for both the cases are taken to be 1Ω, whereas two different values of the turn-on gate resistances are considered. As expected, the turn-off energy losses are very similar in both the cases.

The turn-off energy loss decreases with increase in the device current, which is evident in Fig. 6.20. This happens due to the fact that the device capacitances charge at a higher rate with the high load/inductor current. As a result, the rate of change of the voltage and the turn-off time varies inversely with the load/inductor current, as shown in Fig.6.21. The corresponding current waveforms are also shown in Fig. 6.22. The turn-off switching losses are relatively small compared to the turn-on switching loss. For the load current of 5 A and the turn-on gate resistance of 15Ω and turn-off gate resistance of 1Ω, the turn-on and turn-off switching energies are measured to be 30.16µJ and 4.9µJ, respectively. The total switching losses for various load currents are also shown in Fig. 6.23.

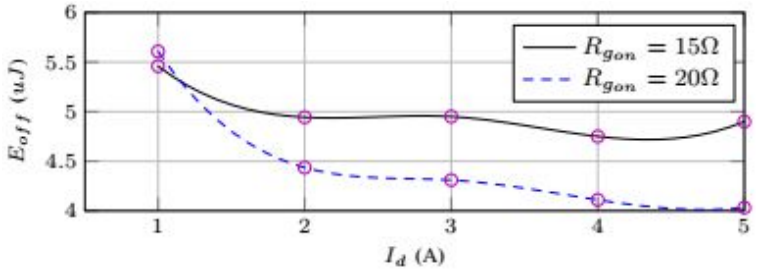


Figure 6.20 Turn-off energy loss variation with the drain current. The dc-link voltage is 350 V.

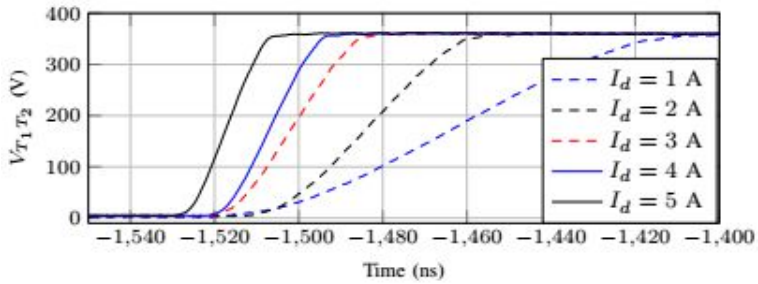


Figure 6.21 Rate of change of voltage dv/dt and turn-off time with respect to the inductor current.

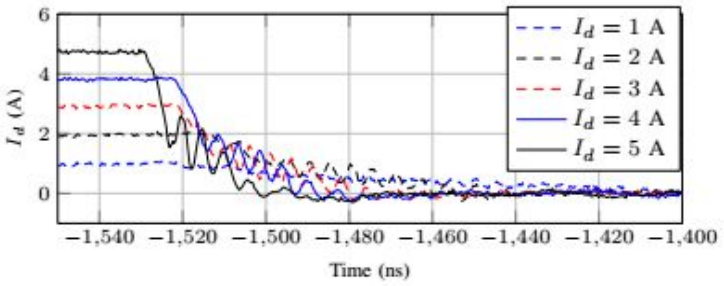


Figure 6.22 Rate of change of current during turn-off transient as a function of inductor current

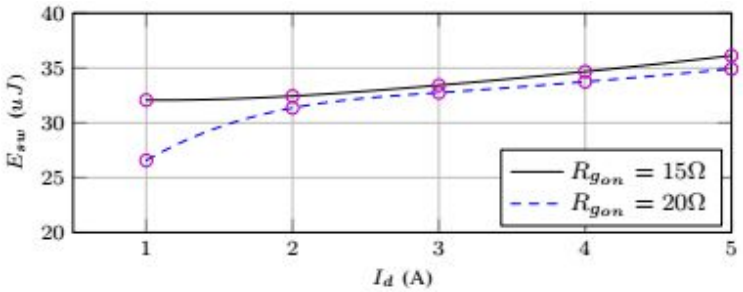


Figure 6.23 Total switching loss variation with the device current. The measurement was done at room temperature

6.4 Conclusion

Initial characterization results of four quadrant GaN switches is presented in this paper. The FQS can conduct in either direction and current conduction can be blocked, irrespective of the polarity of the applied voltage across the switch. The static and dynamic characterization of the GaN FQS was performed. The on-state resistances were obtained for different temperatures. With full channel enhancement, with gate-source bias voltage of 5V for both the devices, the on-state resistance at the junction temperature of 80˚C is 197 mΩ, which is 28% higher than the on-state resistance at room temperature with the similar gate-source bias conditions. The experimental setup to perform the double pulse test has been built and the switching losses were measured for different drain current and different turn-on gate resistances. The turn-off switching loss is significantly smaller compared to the turn-on switching loss. The current overshoot during the turn-on is the main contributor towards the higher turn-on switching loss. The high current overshoot is present due to relatively high dv/dt and high output capacitance of the device.

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