ABSTRACT

MATHUR, SHASHANK. Real -Time Inverter Simulation with Grid Support Capability to meet IEEE 1547 Compliance. (Under the direction of Dr. Subhashish Bhattacharya).

This research focuses on grid connected voltage source inverter and performance evaluation under test scenarios for grid support functions based on the guidelines specified by IEEE 1547 grid standard. A real-time simulation environment with Hardware-in-the-loop, using OPAL RT platform, is designed to emulate real hardware of grid connected system and the operating characteristics at the PCC interconnection of DER with the Area EPS were analyzed. There has been a growing interest related to incorporating grid support functions capability into the DER which is complimented by the most recent advancements in the grid codes and interconnection standards specifically in new versions of IEEE 1547. OPAL RT is chosen as the real time simulator for its robust capabilities to model complex power electronic systems switching at high frequency, model design and test scenarios of power electronic and power systems under the same platform, and for its rapid adoption as a popular Hardware-in-the-loop (HIL) technology for system validation, debug and subsystem tests for early design phase before implementing real hardware thus saving time and cost. Set used is robust, flexible and re-usable for more advanced testing and evaluations of multiple system configuration, multi-level topologies and more advanced control functions. The controller hardware can be validated and after successful run, can be deployed to operate the real hardware. This work can be used for design, test and validation purposes as a template for interconnection, grid tied inverters and implementation of grid support functions under a single platform.

Real -Time Inverter Simulation with Grid Support Capability to meet IEEE 1547 Compliance

by
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DEDICATION

To my family for their unconditional love, support and prayers.

To my professors, teachers and mentors for their guidance and inspiration.

To my friends and colleagues for all their help, care and motivation.

BIOGRAPHY

Shashank Mathur was born in Jaipur, India. He received his Bachelor of Technology degree in Electrical Engineering from Indian Institute of Technology Mandi in May 2014. He started pursuing Master of Science in Electrical Engineering at North Carolina State University from August 2015. His research interests in the area of power electronics include DC-AC converters, DC-DC converters, digital control, grid connected systems, Microgrids, solar photovoltaic system integration with grid support capabilities and smart grids.

ACKNOWLEDGMENTS

I would like to express my sincere gratitude and regards to my research advisor Dr. Subhashish Bhattacharya for giving me the opportunity to work on recent advancements in the area of grid connected inverters. With his continuous guidance and feedback, I was able to achieve considerable level of conclusion and closure towards the scope of my Master Thesis work. I am grateful for his advice and technical discussions during the entire course of research, and also his constant encouragement despite some hardships on working with some issues and learning the concepts and implementing on the real time simulator platform. Overall, working under his supervision has always inspired me to work harder with the specific goal and focus.

I would also like to convey my sincere thanks to Dr. David Lubkeman and Dr. Mesut Baran for providing me with broader perspective of the problem addressed and their feedback on the work. The discussion I had with my committee members significantly enhanced my knowledge of the subject addressed in this work, and I have been very fortunate to learn a lot from their experience and expertise in this area. Again, I would to thank them sincerely for serving on my thesis committee and with the addition of their guidance, I believe my work would have a better credibility for future use.

My best wishes and thanks to my seniors and project mates Srinivas Gulur, Viju Nair, Dr. Ghanshyamsinh Gohil and Ritwik Chattopadhyay for their guidance and help, especially to Srinivas Gulur from whom I learnt a lot about inverters and controls. I would also like to thank my friends working in other projects at FREEDM Vishnu Mahadeva Iyer, Sayan Acharya, Mahsa Kashani, Heonyoung Kim, Arvind Kumar, Valliappan Muthukaruppan, Thomas Dotson, Rishabh Jain, Keith Dsouza and Qian Long. The valuable suggestions and discussion with my peers have contributed a lot towards my research.

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LIST OF ABBRVIATIONS

EPS	Electric Power System
DER	Distributed Energy Resource
PCC	Point of Common Coupling
PV	Photo-Voltaic
HIL	Hardware-In-the-Loop
MV	Medium Voltage
HV	High Voltage
SRF	Synchronous Reference Frame
PLL	Phase Locked Loop
GSF	Grid Support Function
MBD	Model Based Design
THD	Total Harmonic Distortion
SPWM	Sine Pulse Width Modulation
NPC	Neutral Point Clamped
UPF	Unity Power Factor
VVC	Volt VAR Control
VWC	Volt Watt Control
FWC	Frequency Watt Control
DAQ	Data Acquisition
MMC	Modular Multilevel Converter
DR	Distributed Resource

CHAPTER 1: Introduction and Motivation

There is an increase in penetration of renewable energy resources (such as PV) to support power generation. Distributed Energy Resources (DERs) are interfaced with the Electric Power System (EPS) through a power electronic converter. This requires for the system to adhere interconnection guidelines specified in IEEE 1547 Std. [4, 5]

Hardware-in-the-loop (HIL) real time simulation is implemented to develop an environment to test controller design and validate physical system with virtual representation of plant model to mimic real hardware offering benefits of cost and practicality, being more flexible to design changes and easier to debug subsystems at an early stage of design.

IEEE 1547 standard (under progress) [5] is intended to be established as a single document of consensus standard technical requirements for DER interconnection providing uniform criteria and guidelines related to operation, test, safety and maintenance of interconnection. It fundamentally covers performance requirements, power capabilities, response to EPS abnormal conditions, power quality and islanding issues [4, 5], among other requirements. This work is an attempt to develop a robust and reusable design and test architecture for interconnection abiding IEEE 1547 guidelines and be used as a foundation template for grid connected systems locally connected to Area EPS.

1.1. DER – Grid Interconnection

For renewable energy systems such as Solar PV, the output power is DC in nature. An inverter stage is connected to convert the DC power from the renewable energy source into useful AC power that can be connected to the load for the purpose of consumer applications or can be injected into the grid. One of the objectives is to operate the system at good power quality so that it meets the compliance requirement with the standards and grid codes.

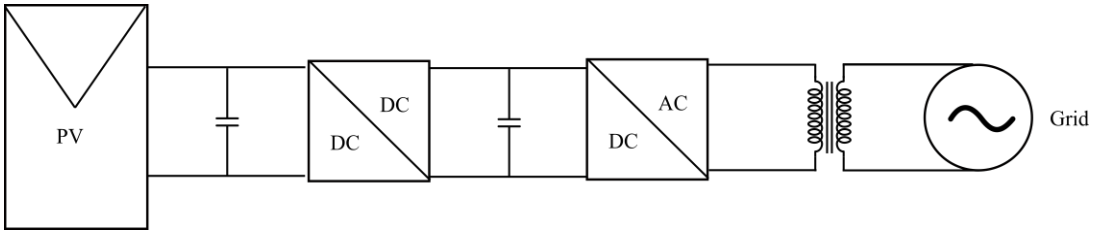


Figure. 1. PV Inverter with grid integration

This chapter discusses about motivation of this work and applications of recent advancements in the inverter – grid integration. A control strategy is developed that monitors the parameters at the point of common coupling, and regulates based on the control design. These advancements are rapidly getting adopted by the utilities and recent changes has been discussed in the new drafts of IEEE 1547 standard [4, 5]. Evaluation of the system design and performance modelling using real time simulator provide an early stage validation procedure for the system before testing the hardware and utilize it during initial phases of design and development due to constraint of time, cost, space and resources. The steps followed include system modelling and then implementing hardware in the loop to test the control hardware providing a complete and consistent system level verification and validation procedure of power stage and controller using software and hardware components.

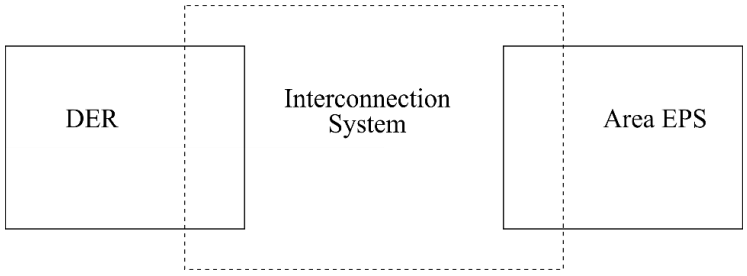


Figure. 2. DER-EPS Interconnection system

This works could contribute to the system level modelling and validation of the MV and HV grid connected systems [13]. This is a robust and flexible model with the ability to run multiple parallel simulations and to create and test scenarios from basic to complex in order to evaluate the DER performance. The test scenarios are directly addressed to the guidelines provided in

the IEEE 1547 standards incorporating the new control functions. The objective to achieve interconnection requirements [5] along with regulation of PCC voltage while operating in the specified range of operation as specified by the Area EPS.

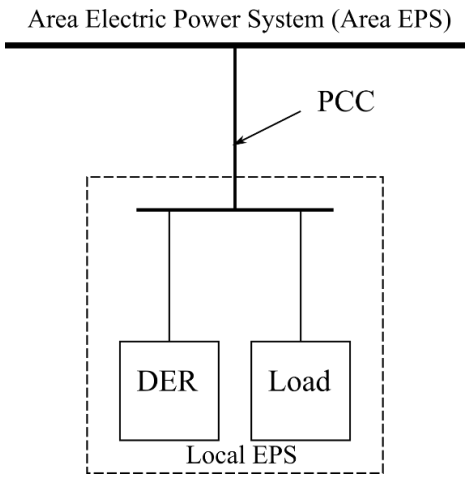


Figure. 3. Local EPS connected to Area EPS

Three phase loads are common in the industrial applications such as induction motor drive for heavy duty loads which when connected may affect the voltage at the PCC due to sudden demand of power (active and reactive) by the load. These issues are addressed and a control architecture is proposed that would meet some specific requirements of grid support functions.

1.2.Grid Support Functions

Implementation of grid support functions (GSF) is supported [3, 6] by standards for EPS-DER interconnection at PCC, e.g. California Public Utilities Commission Rule 21 and Hawaii Rule 14H [1, 2], as well as updates to UL1741 Supplement SA and ongoing revisions to IEEE 1547 [4, 5] as some of the initial work towards this area. It is encouraged by the utilities with a growing trend, as mentioned in the new guidelines from standards.

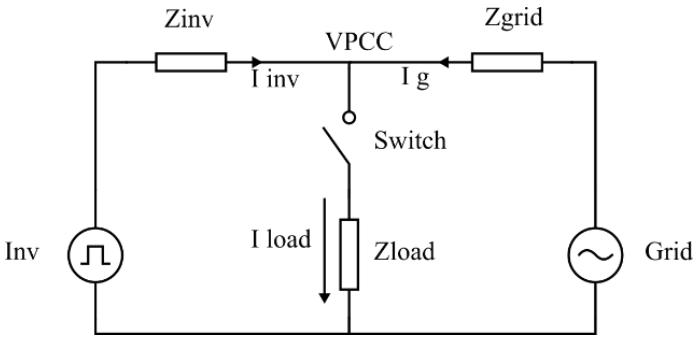


Figure. 4. Reference diagram for load connection at PCC

For integration of DER with the Area EPS, there are certain requirements to follow and restrict disturbances at the node of Point of Common Coupling (PCC). Some of these requirements include grid synchronization, voltage and frequency maintenance [4, 5], power quality (allowable under THD limits).

In brief, this work aims to design and validate a robust real time simulation environment for converters interconnecting DER with EPS. This study can be used as a template for early design stage evaluations of grid connected inverter plant model & controller hardware, with capability of increased complexity of DER network to be simulated with a model-based-design (MBD) with closer reality. Modelling of individual DER i.e. inverter (front end converter) system is demonstrated and impact on PCC is analyzed. Specific grid support capabilities of DER provided in IEEE 1547 are implemented. Real time simulations are performed on OPAL RT platform used in HIL testing for controller validation.

CHAPTER 2: Grid Tied Inverter Design

2.1. Topology

2.1.1. Two level voltage source inverter

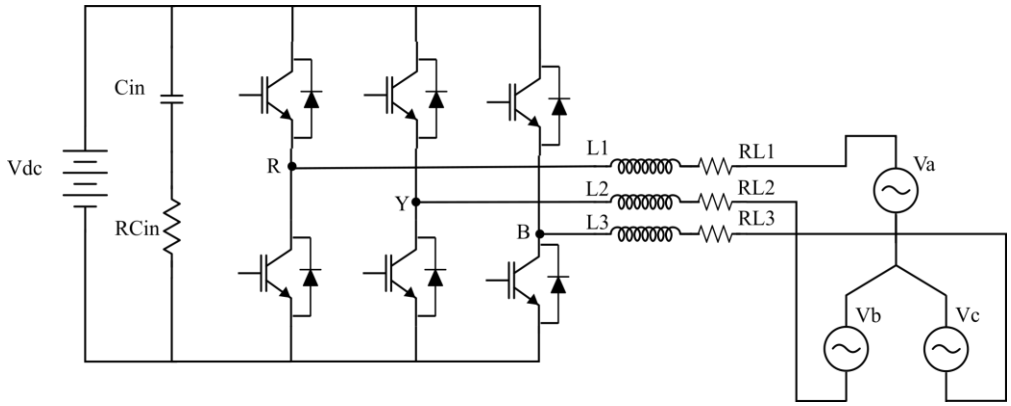


Figure. 5. Two- Level grid connected inverter

Table 1: Inverter and grid parameters.

Parameters	
Rated output power	1.7 MVA
Rated AC voltage	4160 V grid voltage (L-L)
Rated frequency	60 Hz
Rated AC current	600 A
Power factor range	0 – 1 (lagging/leading)
Current THD	< 5 %
Grid-connected Inverter parameters	
Inverter Topology	Two Level Voltage source inverter
Switching frequency	10 kHz
DC-link voltage	10 kV
DC-link capacitance	Cin = 200uF, R = 0.1 m Ω
Modulation scheme	Sine PWM
Harmonic filter	L filter
Filter parameter	Inductance L = 20 mH, R = 0.2 Ω

2.1.2. Three Level NPC voltage source inverter

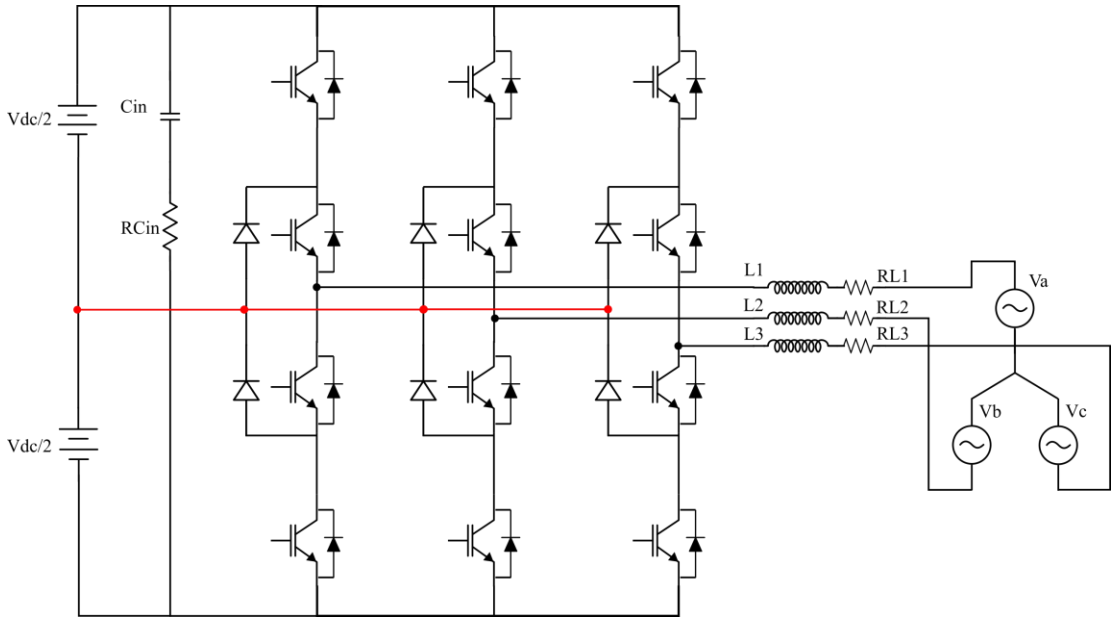


Figure. 6. Three Level NPC grid connected inverter

The maximum current (capacity) can be found based on nameplate rated power.

$$S = \sqrt{3} \times V_{L-L\,(rms)} \times I_{L(rms)}$$

$$1.7\,MVA = \sqrt{3} \times 4160 \times I_{L(rms)}$$

$$I_{L(rms)} = 235.7\,A$$

$$I_{L(peak)} = 333.3\,A$$

2.2.Phasor Diagram and Power Flow

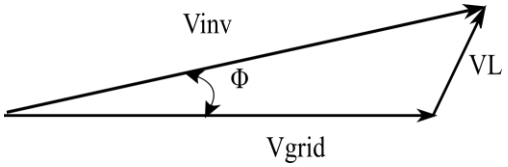


Figure. 7. Phasor diagram

Φ is used to control active power P and reactive power Q.

$$P = \frac{V_{grid}}{\omega L} \times V_{inv} \times Sin\Phi$$

$$Q = \frac{V_{grid}}{\omega L} \times (V_{inv} Cos\Phi - V_{grid})$$

$$Power\ factor = Cos\,\Phi = \frac{V_{inv} Sin\,\Phi}{V_L}$$

Vinv is directly related to modulation index m by the following relation:

$$m = \frac{V_{inv}}{(\frac{V_{DC}}{2})}$$

Note that only half of DC voltage is seen at each node.

For unity power factor,

$$V_{inv} = \sqrt{{V_L}^2 + {V_{grid}}^2}$$

$$\Phi = \tan^{-1} \frac{V_L}{V_{grid}}$$

P and Q calculation are implemented using the following relations:

$$P = v_a i_a + v_b i_b + v_c i_c$$

$$Q = \frac{1}{\sqrt{3}} (v_{bc}\, i_a + v_{ca}\, i_b + v_{ab}\, i_c)$$

2.3.Load Connection:

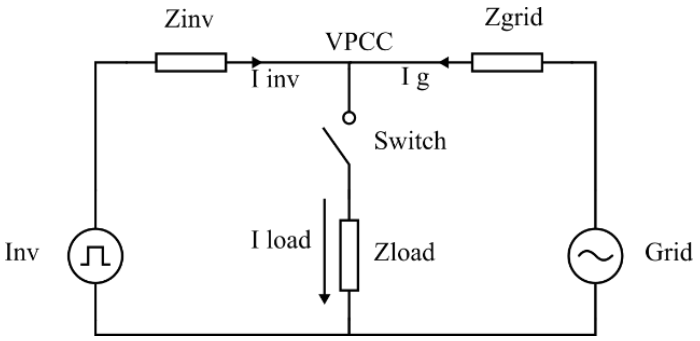


Figure. 8. One line diagram to represent grid connected inverter with load

When the load gets connected, we are interested to find out the active, reactive and apparent power flow at the PCC node into the three branches i.e. inverter, load and grid. The power flow equations hold true for this scenario as well, however the analysis is more complex. To simplify the analysis, another approach is followed, as described in later parts pf this chapter. But, before that it is important to understand frame transformation.

2.4.Frame Transformation

The idea behind frame transformation is to represent the three phase quantities into two mutually perpendicular components that both rotate with the grid angular velocity ω, so that from the rotating frame of reference, both appear to be constants. Also, since they are perpendicular, it is easier to de-couple [14] the effects from real and imaginary quantities. These transformation strategies are popularly known as Clarke's Transformation and Park's transformation.

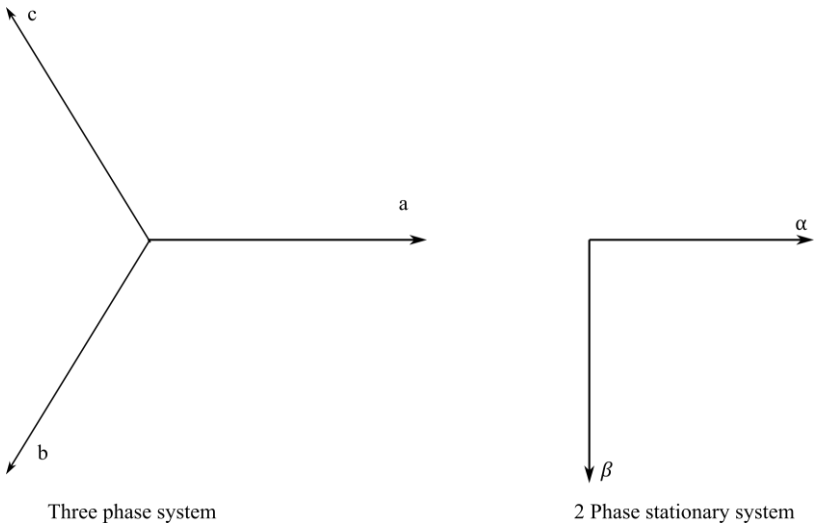


Figure. 9. Clarke's transformation

$$\begin{pmatrix}\alpha\\ \beta\end{pmatrix} = \begin{pmatrix}1 & -\frac{1}{2} & -\frac{1}{2}\\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2}\end{pmatrix}\begin{pmatrix}a\\ b\\ c\end{pmatrix}$$

We represent the 3 phase grid voltage with the following relation taking positive sequence.

$$V_a = V_m Sin\,(\omega t)$$
$$V_b = V_m Sin\,(\omega t - 120°)$$
$$V_c = V_m\, Sin\,(\omega t + 120°)$$

Then,

$$V_\alpha = \frac{3}{2} V_m Sin\,(\omega t)$$
$$V_\beta = -\frac{3}{2} V_m Cos\,(\omega t)$$

As discussed, the objective of the transformation is equivalent representation in 2 phase [14]. So, we define vector V as,

$$V = V_\alpha + j\,V_\beta$$

$$V = \frac{3}{2} V_m e^{j(\omega t - 90°)}$$

Clearly, the grid voltage vector V is rotating with time as seen from the, β frame. So, next step is to design a synchronous reference frame (d, q).

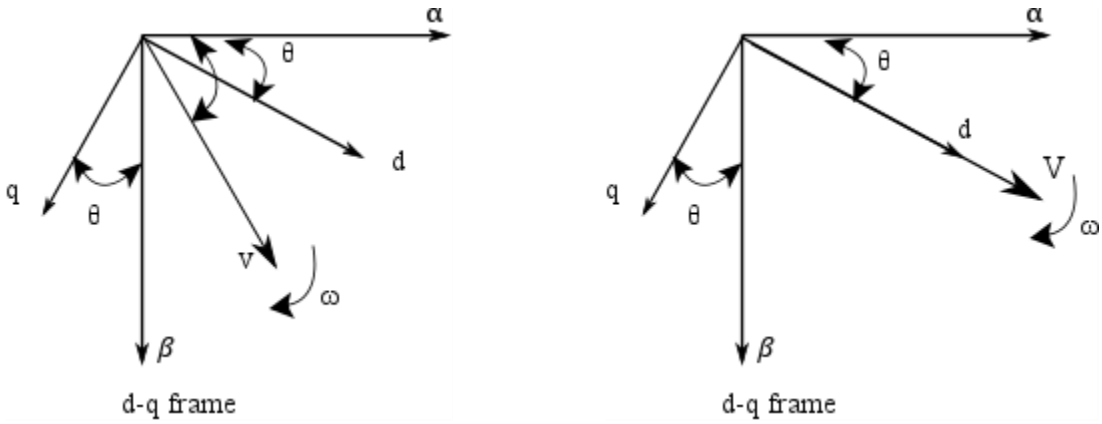


Figure. 10. Park's transformation

$$\begin{pmatrix} d \\ q \end{pmatrix} = \begin{pmatrix} Cos\,\theta & Sin\,\theta \\ Sin\,\theta & -Cos\,\theta \end{pmatrix} \begin{pmatrix} \alpha \\ \beta \end{pmatrix}$$

2.5.PLL Design

Phase, amplitude and frequency of the grid voltage are important parameters to achieve grid synchronization with the inverter system. Some performance matrix would how accurately and fast inverter can be synchronized to the grid in terms of angle, amplitude and frequency.
We desire the inverter to operate close to unity power factor (UPF).

Among the most popular strategies for grid synchronization is Phase Locked Loop [8, 9]. It is a feedback control scheme that automatically adjusts the phase. It is used to synchronize the inverter current angle with the grid phase to reach the power factor close to 1. Inverter phase angle is used to calculate the reference current to be compared with the output current.

The idea is to transform the three phase voltages into two orthogonal voltages in rotating d, q frame. This works using abc to dq transformation block. The idea is to align the voltage vector with one of the d or q component and the other with 0. The PLL structure is an SRF (Synchronous Reference Frame)-PLL [9] and consists of two major parts – phase detection, handled by abc-dq transformation and loop filter that determines the dynamics of the PLL [8, 9]. The bandwidth of the filter will determine the time response to lock the phase and there will be trade off with the filtering action.

Since now we have established the transformation matrices, there is an important step in order for currents to be operating at grid frequency and to minimize the phase error. An SRF-PLL PLL is used for this purpose. The objective is to align vector V with the d axis or d component. This will provide an estimate of the phase angle θ. The d component would provide magnitude and q component provide the information of the phase error between V vector and d axis.

A feedback loop is implemented for the purpose of locking the loop and the dynamics of the controls govern how quickly the voltage vector is able to track the reference d axis. The parameters of the controller [11] would be estimated by comparing the plant transfer function with the fixed coefficients of a PI controller with second order transfer function.

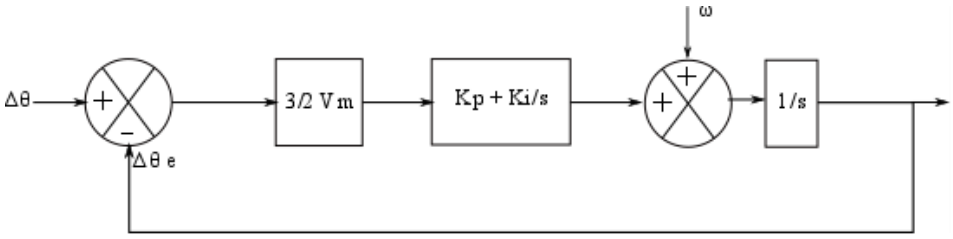


Figure. 11. PLL closed loop control (Phase error)

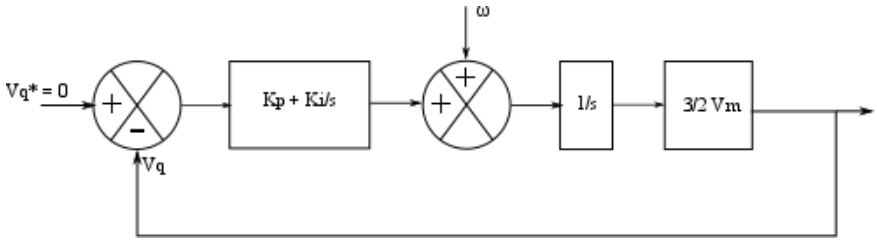


Figure. 12. PLL closed loop control (Vq error)

$$T(s) = \frac{\omega_n^2 + 2Q\omega_n s}{s^2 + 2Q\omega_n s + \omega_n^2}$$

Here ω_n and Q are the natural frequency and damping coefficient respectively for the second order transfer function.

Table 2: PLL controller coefficients.

Vm	Q	ω_n	K_p	K_i
$4160 \times \frac{\sqrt{2}}{\sqrt{3}}$	0.707	62.8 rad/s	$\frac{4 \times \omega_n \times Q}{3 \times V_m}$	$\frac{2 \times \omega_n^2}{3 \times V_m}$

Implementation of PLL:

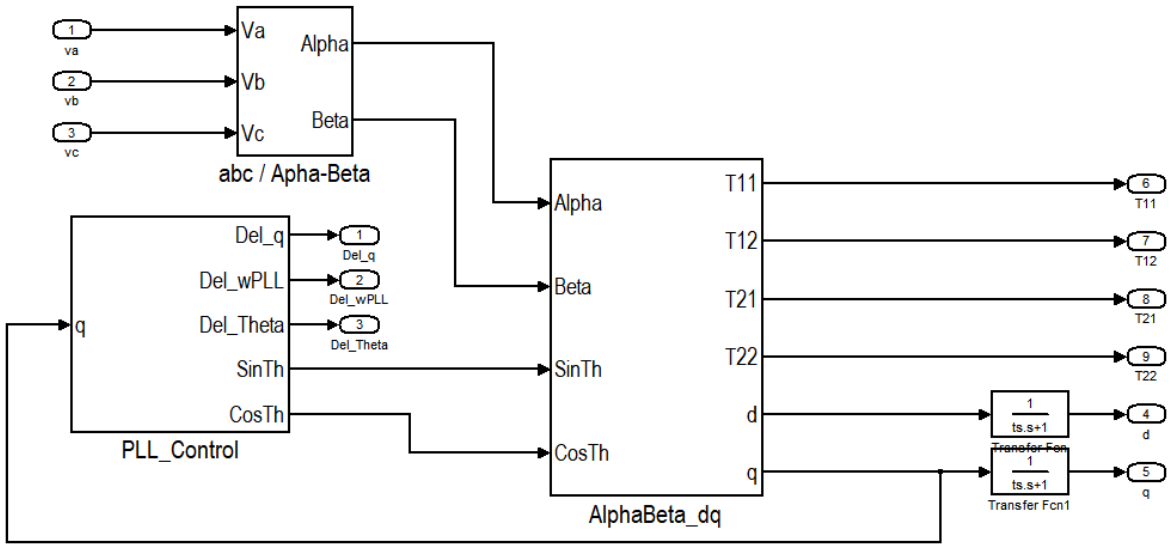


Figure. 13. PLL with transformation blocks

As depicted in the figure, output of the PLL is Vd and Vq, and also Sin and Cos functions.

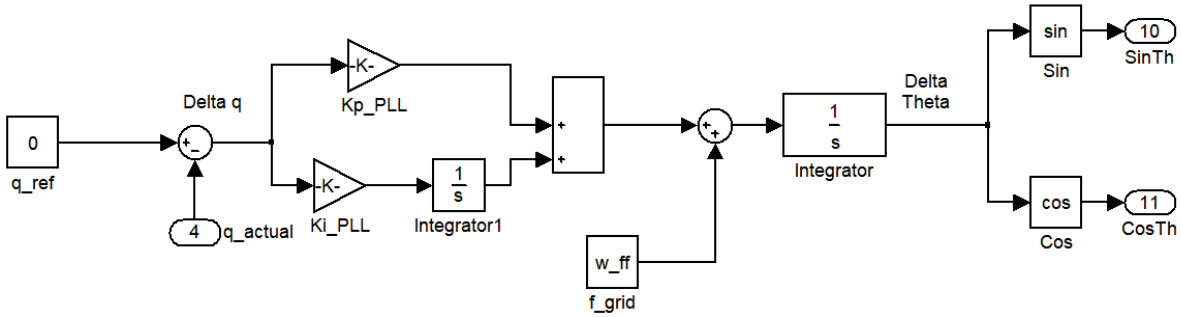


Figure. 14. PLL controller detailed

Grid frequency is provided as feedforward to converge faster, however it is not included in the closed loop.

2.6.Closed loop design of current controller

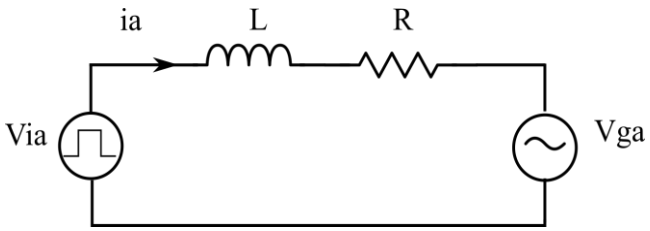


Figure. 15. Per phase equivalent diagram

$$V_{ia}(t) = L\frac{di_{ia}}{dt}(t) + Ri_{ia}(t) + V_{ga}(t)$$

$$V_{ib}(t) = L\frac{di_{ib}}{dt}(t) + Ri_{ib}(t) + V_{gb}(t)$$

$$V_{ic}(t) = L\frac{di_{ic}}{dt}(t) + Ri_{ic}(t) + V_{gc}(t)$$

When we represent these equation in the d-q frame, we get

$$V_{id} = L\frac{di_{id}}{dt} + Ri_{id} - \omega Li_{iq} + |V|$$

$$V_{iq} = L\frac{di_{iq}}{dt} + Ri_{iq} + \omega Li_{id}$$

It is observed that the d component of voltage has contribution from both id and iq [14], and likewise for q component of voltage.

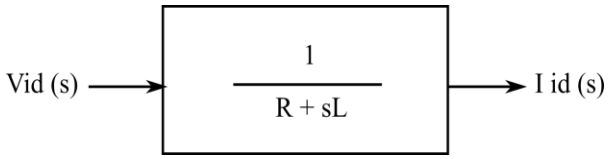


Figure. 16. Plant transfer function in d-q plane

Compensation:

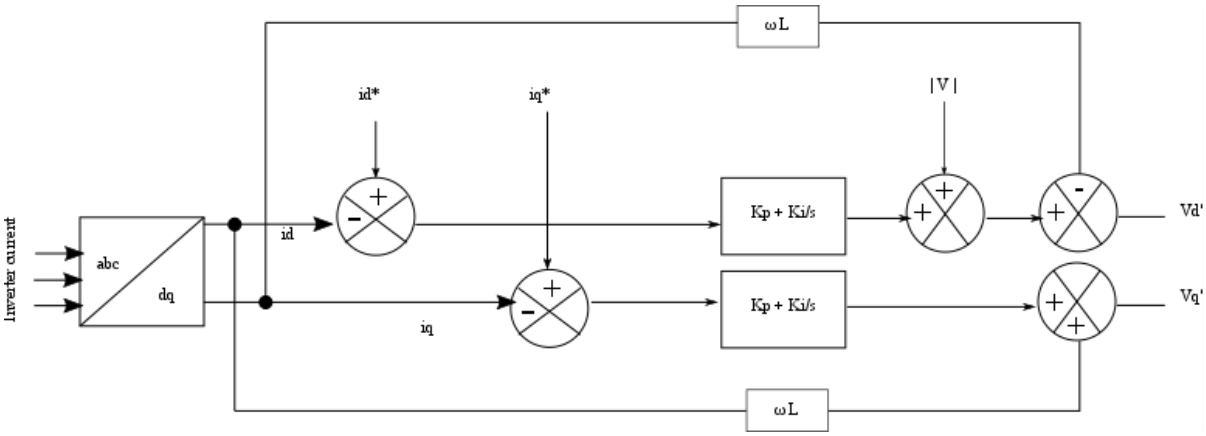


Figure. 17. Current control structure

$$G_c(s) = \frac{L}{\tau} + \frac{\frac{R}{\tau}}{s}$$

$$G_c(s) = K_p + \frac{K_i}{s}$$

So, $K_p = L/\tau$; $K_i = R/\tau$

Here τ is directly related to the cut off frequency [14] and hence this becomes a design choice. One constraint is from the switching frequency, as we want to attenuate high frequency component of the switching frequency and pass only the line frequency. Also, it is preferred to keep the bandwidth (B.W.) as high as possible without injecting harmonics. So, a good ball park zone is to select B.W. = $1/\tau = (1/20) * f_{sw}$

In this system, f_{sw} = 10 kHz. Also, L, R values are specified in the system architecture.

So, K_p = 62.84; K_i = 628.32. Here as selected, B.W is 500 Hz.

Implementation of current control loop:

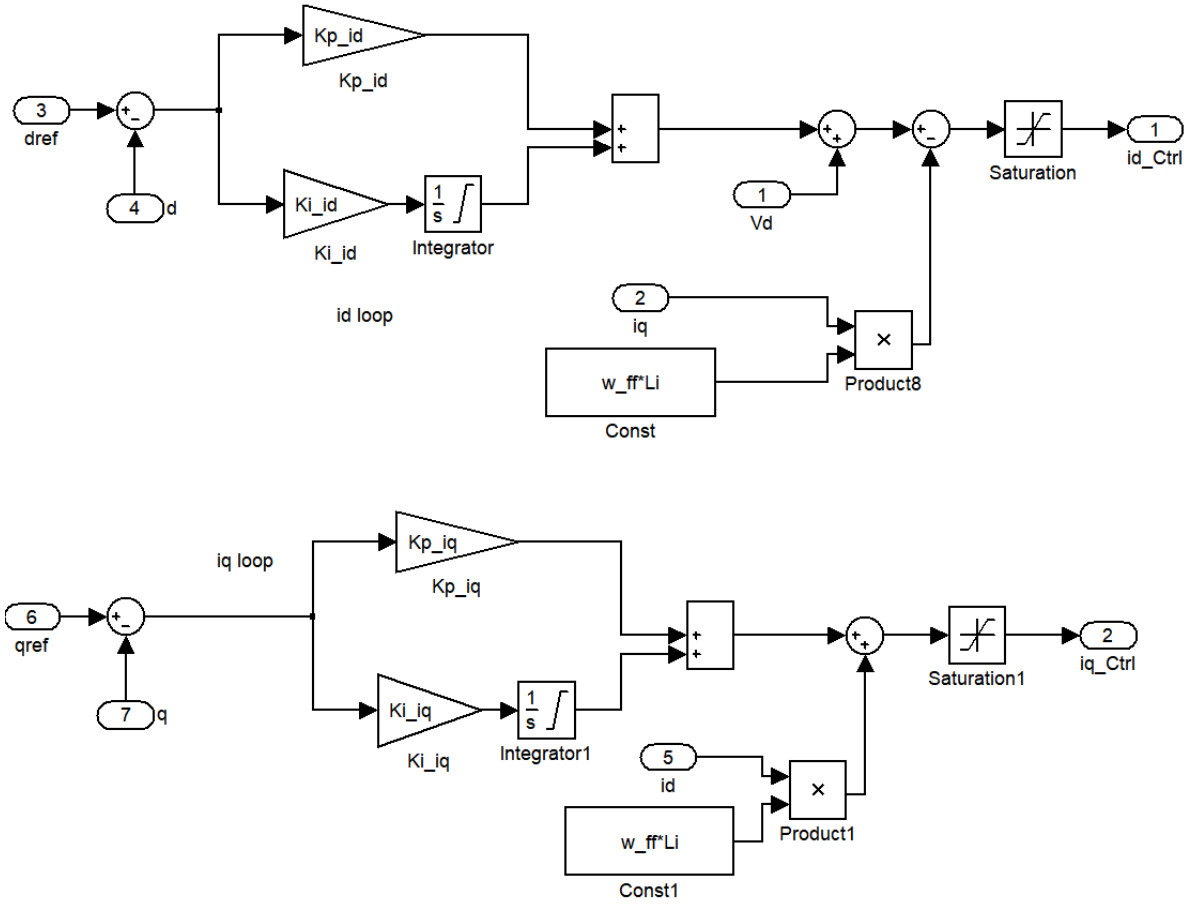


Figure. 18. id and iq current control loop

CHAPTER 3: Survey of Similar Work

There has been continued interest in inverter response to abnormal conditions on the grid side. One of the primary area of discussion is grid support capability and how does it affect the dynamics complying with grid codes.

3.1. Literature Survey

3.1.1. NREL Report

Experimental Evaluation of Grid Support Enabled PV Inverter Response to Abnormal Grid Conditions [6]

Analysis in this work included comparative experimental evaluation on four commercially available, three-phase PV inverters, GSF capability and its effect on abnormal grid condition response and impact on run-on times during islanding, peak voltages in overvoltage scenarios, and peak currents during fault events. Some of the functions discussed are voltage ride through, frequency ride through, fixed power factor, volt-var control and frequency watt control. Main focus was on VVC, VWC and FWC control methods and their limitations on run on times.

3.1.2. UL 1741 SA

Small Commercial Inverter Laboratory Evaluations of UL 1741 SA Grid-Support Function Response Times [3]

This work is similar to NREL in terms of grid support functions, low/ high voltage ride through, dynamic Volt-VAR operation and implacability of these functions in presence of voltage transients. They evaluated risks of grid support functions conflicting with traditional distribution system, quantified EPS support function response times for voltage regulation functions and response of support functions to voltage transient.

3.1.3. Inverter Controls

Literature on grid connected inverter and control scheme [7,12,15] has been referred as listed in the references section. Researchers have looked into specific areas of inverter operation and modelling and design related to filter, modulation techniques, controller design, PQ control, etc.

3.2.Focus of this work

This work mainly focusses on the performance of the grid tied inverter for grid support control modes Volt-VAR and Volt-Watt. The objective is to look into the voltage sag and swell cases covering major test scenarios corresponding to the regions of operation in the specific voltage ranges from minimum under voltage to maximum over voltage.

This work proposes a fundamental framework on real time simulation for grid connected switching models with the capability of real time testing and evaluation of control functions. An algorithm for disturbance detection is proposed based on measurement of voltage at the point of common coupling, based on which the reference points for P and Q are set. Another algorithm is designed to calculate the load conditions and parameters required to model inductive or capacitive loads of given rated power demand. This algorithm can also be used for vector analysis of the currents, voltages and impedance parameters within the inverter, load and grid branch and also the nodal analysis at PCC.

Hardware-in-the-loop (HIL) real time simulation is performed to develop an environment to test controller design and validate physical system with virtual representation of plant model to mimic real hardware offering benefits of cost and practicality, being more flexible to design changes and easier to debug subsystems at an early stage of design.

CHAPTER 4: Real-time HIL Simulation Platform

4.1. Software: RT – Lab software interface

4.1.1. Subsystem Representation

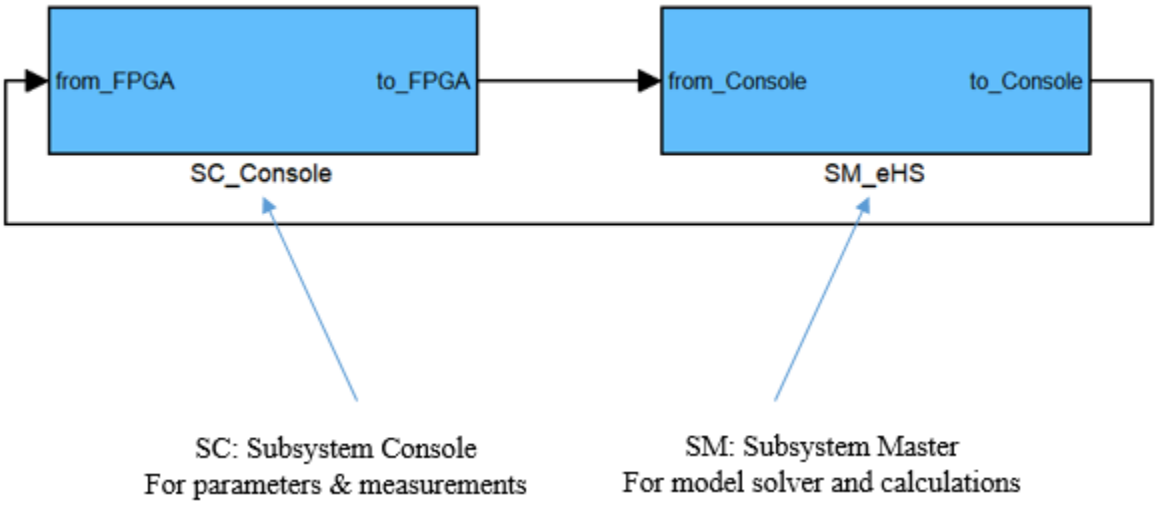


Figure. 19. High Level Subsystem Model on OPAL RT

4.1.2. Measurement and Parameter Setup

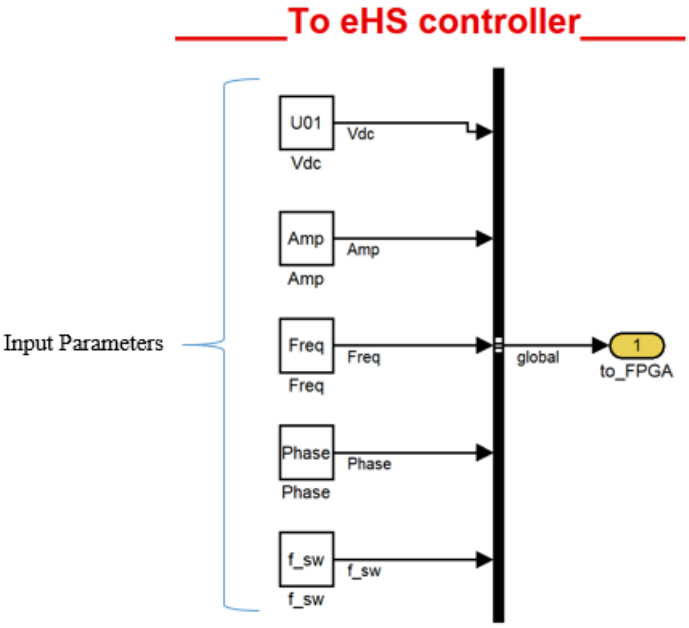


Figure. 20. Input Parameters

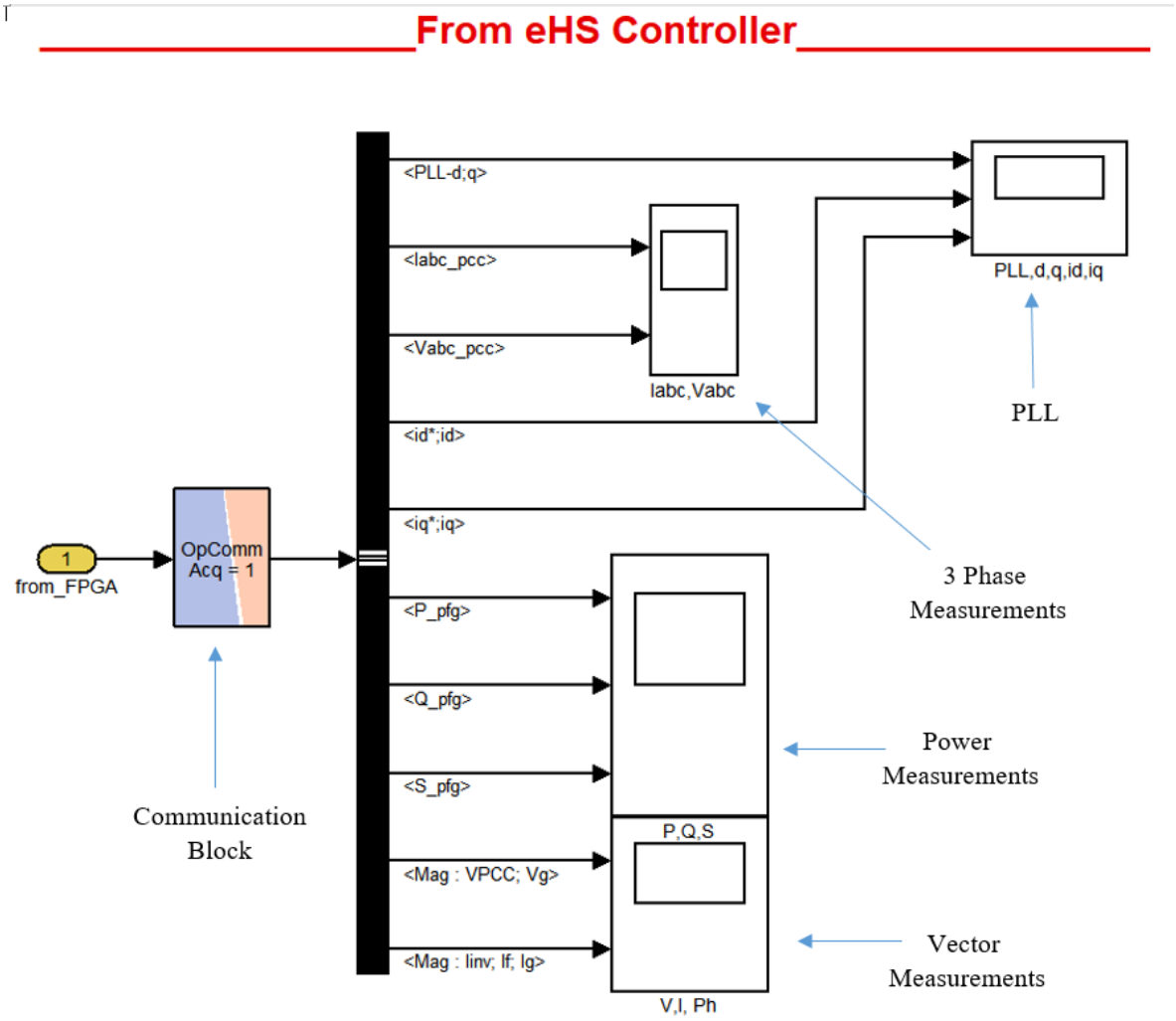


Figure. 21. Output Measurements

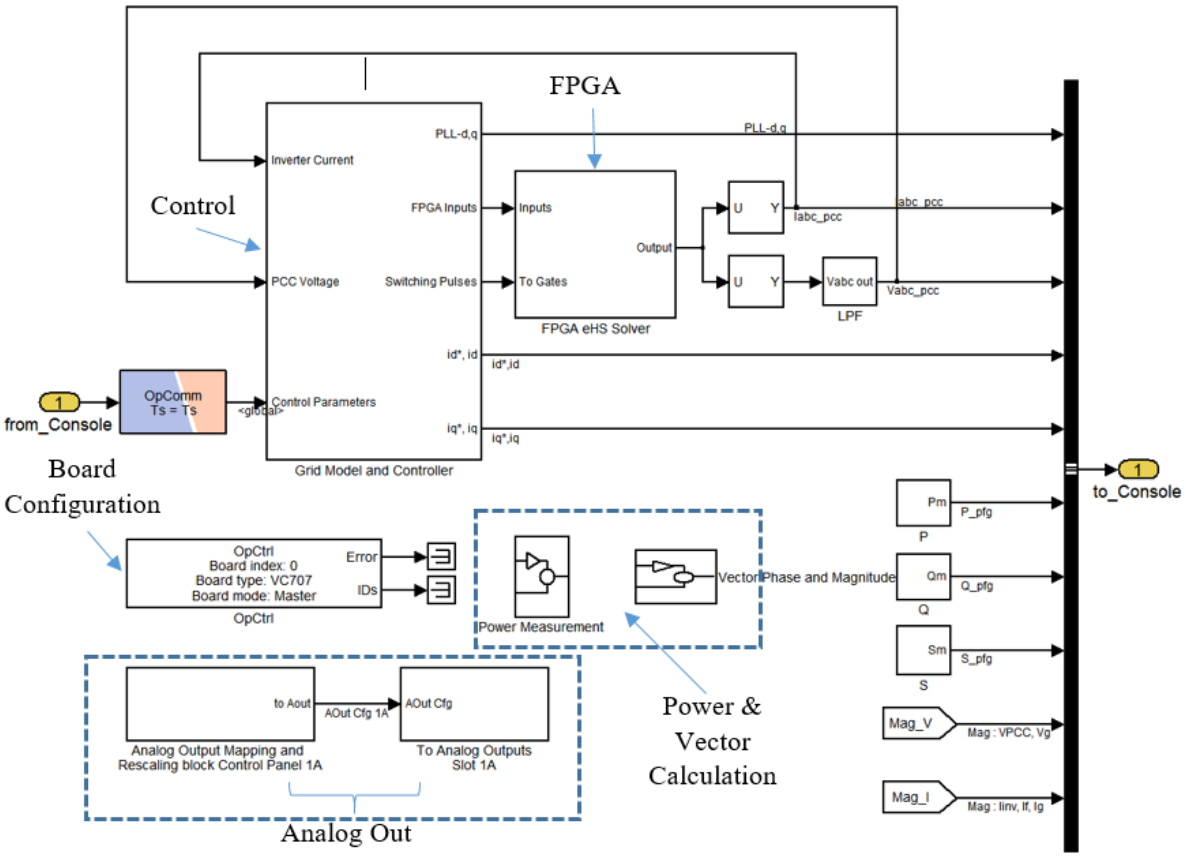


Figure. 22. Master Subsystem Block

The Master subsystem is the main block that houses the FPGA model, monitors analog and digital out and used for signal conditioning and control purposes. The input parameters given from console goes into the controller through an OpComm block. eHS solver block emulates the operation of FPGA and uses the bit stream file to assign ports and peripherals for signals during run time. The power stage consisting of all switches, and voltage sources are included in FPGA model and its netlist is declared with the details of inputs, switches, outputs, gate settings etc. The output of the eHS block is used to capture real time Analog output for e.g. to capture 3 phase inverter currents, and also to feedback the analog signals in the controller. A low pass filter is used at the sense point of PCC voltage in order to filter out high frequency ripple for better sensing and detection of abnormal operations at the PCC.

4.1.3. Grid Emulation in CPU

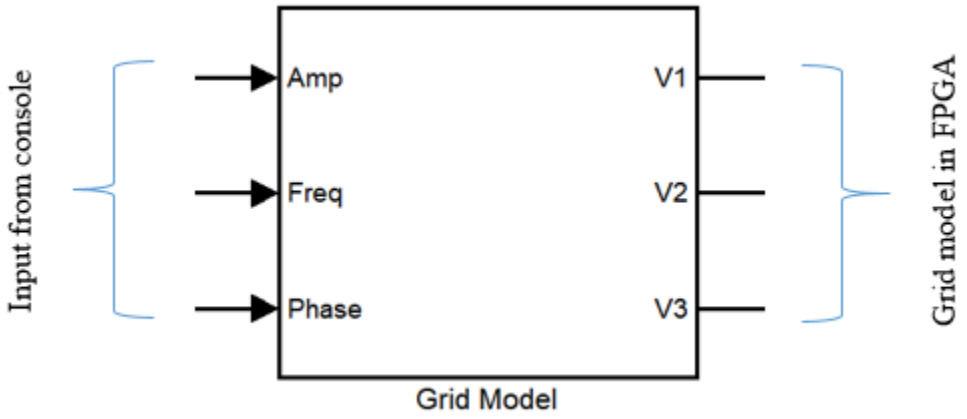


Figure. 23. Block diagram of grid model

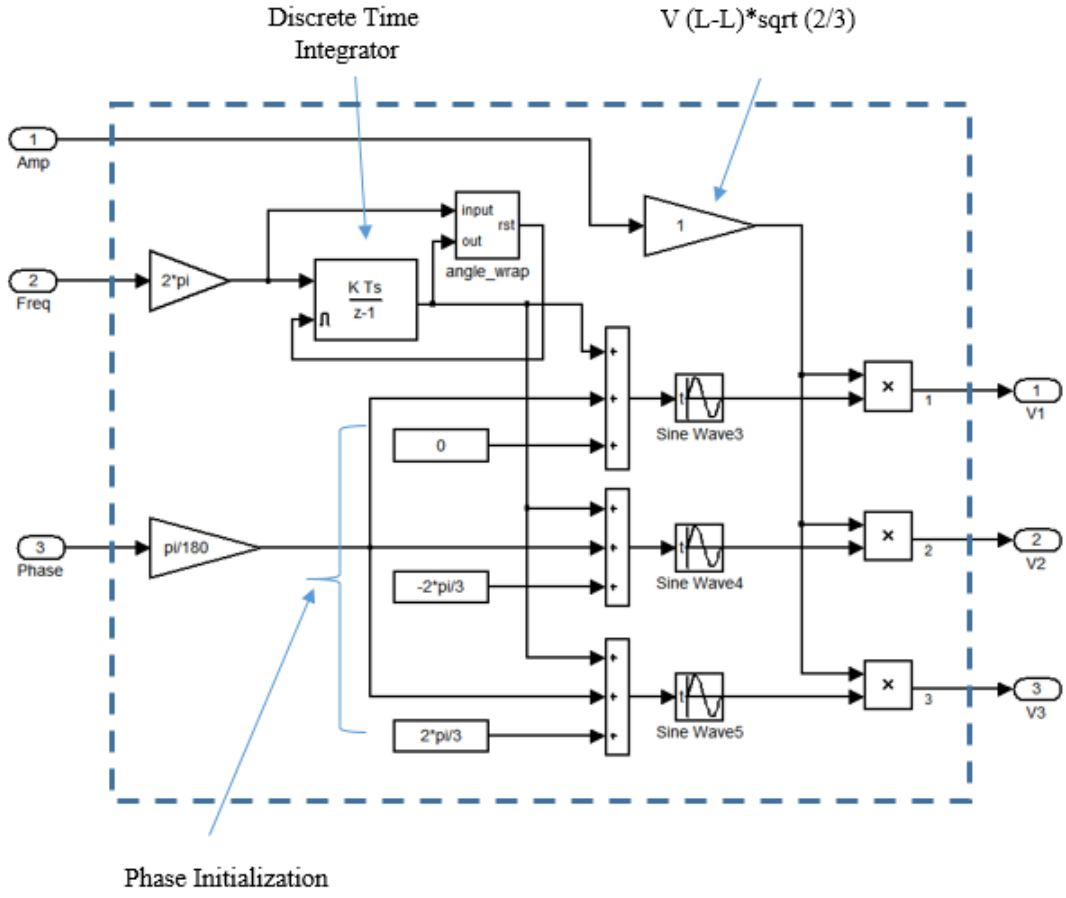


Figure. 24. Detailed grid model

The parameters of grid voltage amplitude, frequency and phase that would emulate grid as a 3 phase voltage source is shown in the figure. In the parameters, initial phase angle of phase A is 0 deg and amplitude is set to 4160*sqrt(2/3). The purpose of giving these variables as parameters is not to control them externally during operation, but for design flexibility.

4.1.4. Switching Model in FPGA

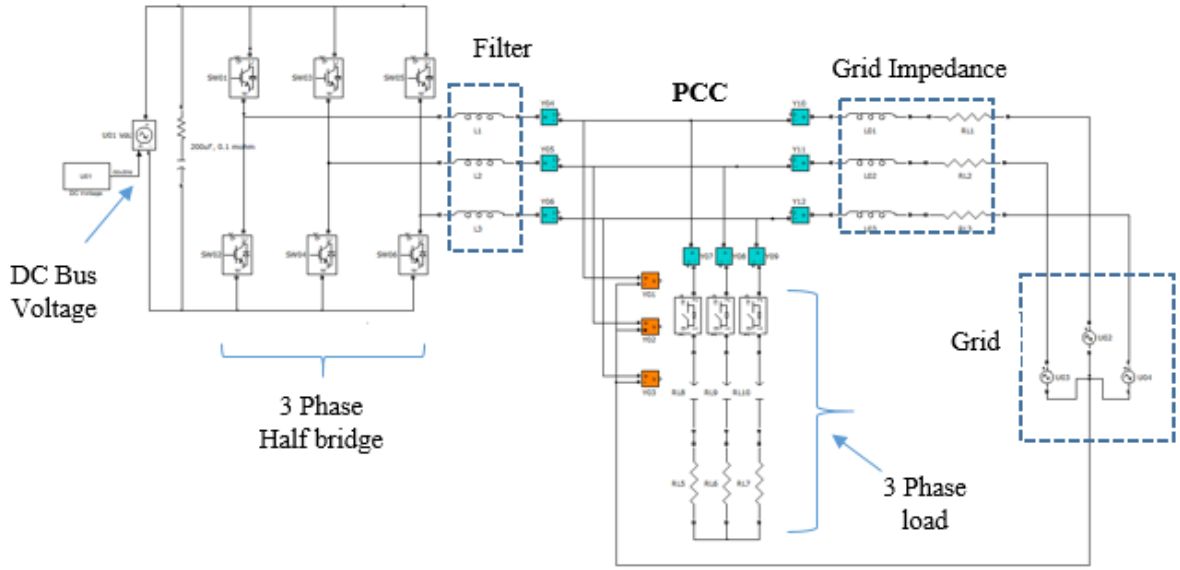


Figure. 25. Two Level Inverter model with grid and load on FPGA

The inverter switching frequency is 10 kHz. The switching model is running at 250 ns time step allowing high frequency simulation with good data acquisition. The CPU time step is 10 us. The reason FPGA is used for power stage is because to run the high switching power stage on CPU, the minimum step observed to show results without data loss is 15 us for a single core.

4.2. Hardware of OPAL RT

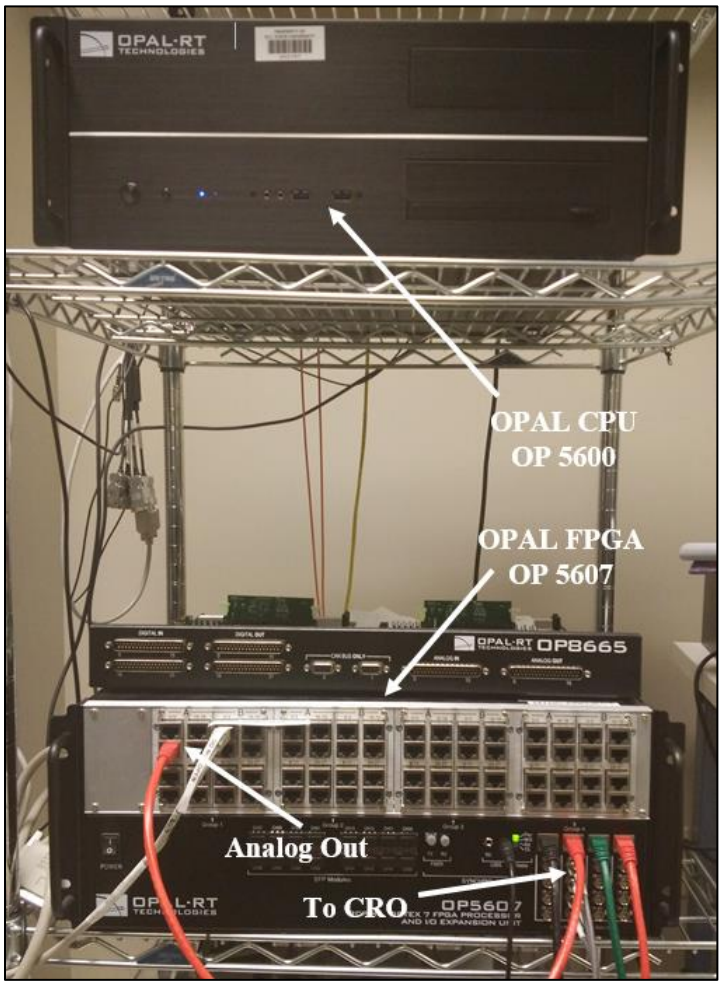


Figure. 26. Real Time Simulator OPAL RT Hardware

The laboratory setup for the OPAL RT HIL real time platform is shown in figure. The setup includes OPAL units OPAL 5600 and OPAL 5607 interconnected using optical cables for synchronization and using data cables to transfer analog and digital signals. The front chassis of the OPAL 5607 shows Analog out channels used to capture results on an Oscilloscope. Each group has 8 ports with 4 channel each, so total 32 channels available for data capture.

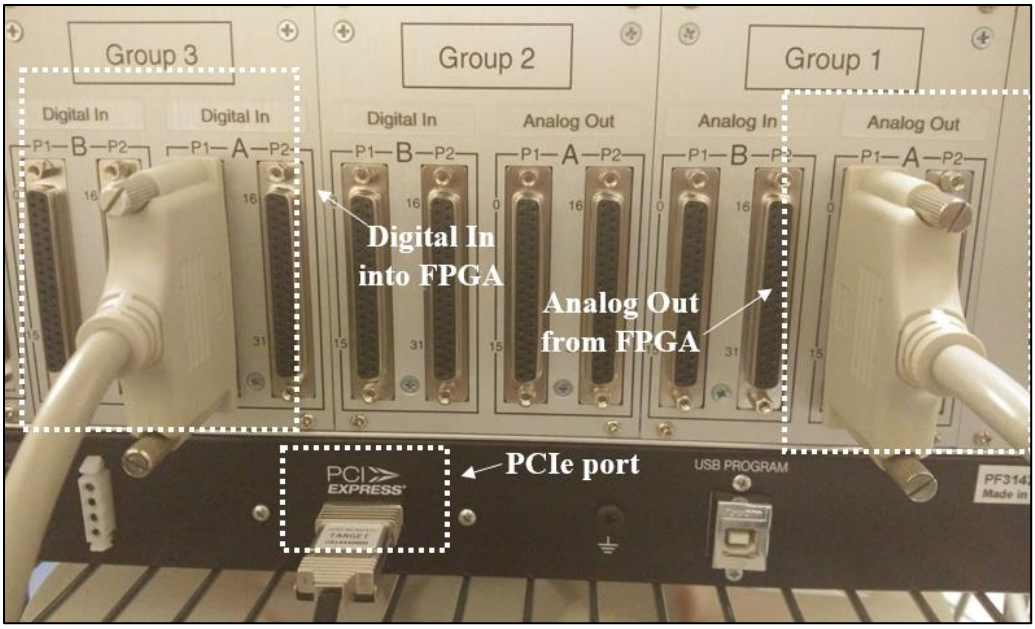


Figure. 27. I/O port for Analog and Digital signals

The output from the FPGA, for instance PCC voltage, is sensed as feedback by the CPU using the Analog Out channel, and then based on the controller output, FPGA receives the gate signals from the controller using Digital In channel.

In the figure shown here, there are multiple groups each specified for Analog or Digital data transfer. For synchronization of OP5600 and OP 5607 units, PCIe is used as shown in the figure above.

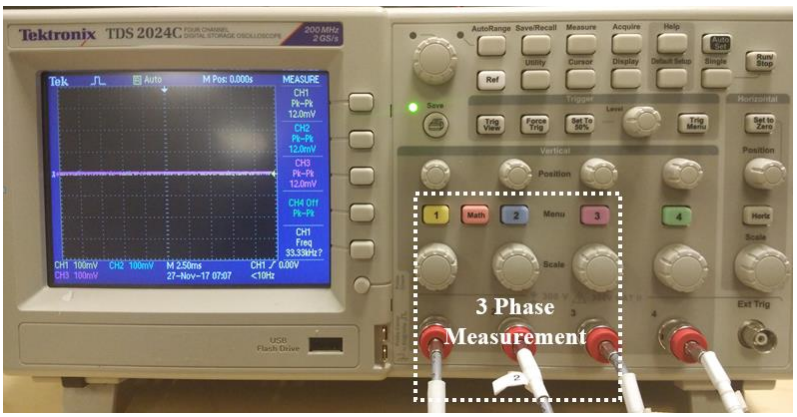


Figure. 28. Tektronix Oscilloscope for DAQ

For purpose of real time measurements, Tektronix TDS 2024C oscilloscope is used with 4 channels and resolution of 2G Sample/ sec at 200 MHz

4.2.1. Hardware-in-the-Loop Platform of OPAL RT

Features include Analog and digital channels on OPAL 5706 (FPGA): 16 Analog In, 32 Analog Out, 128 Digital In and 32 Digital Out ports. eHS Gen3 solver is used to emulate the FPGA model and interface with CPU and is capable of incorporating 72 switching models in a single simulation per eHS. For high order switching models, multiple eHS solver emulating multiple FPGA could be used for applications like MMC using a single core.

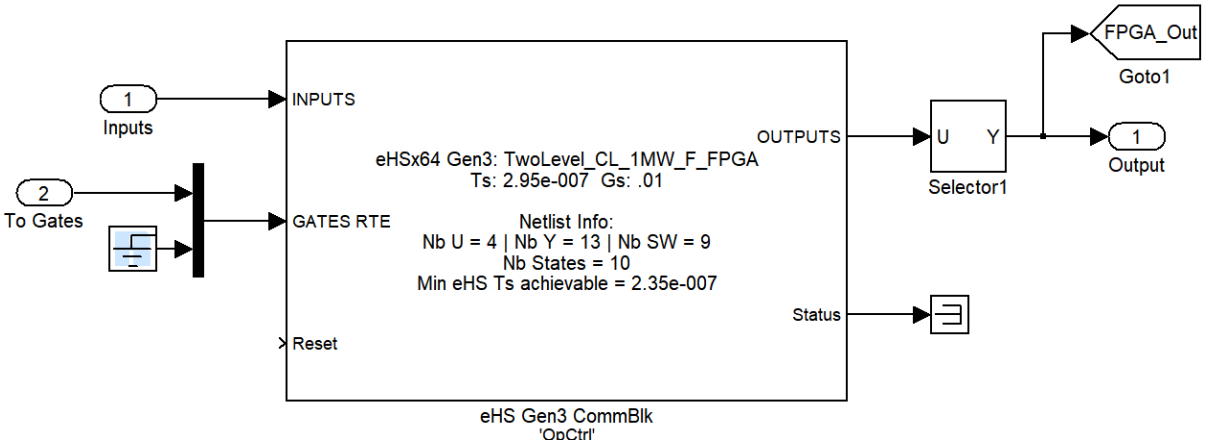


Figure. 29. eHS Gen 3 solver

A binary file (.bin) or a bit stream file is programmed using Xilinx Design tools like Vivaldo and System Generator configured using OPAL RT RT-XSG library. The bin file specifies the hardware mapping of the data and I/O pins used during run time. The bin file is fairly complex to generate and for simplicity, for this work bin file is generated that incorporates Data In, Load In and Data Out blocks in the Xilinx system generator. Data In inputs and Data Out blocks are updated every time step of CPU, while Load In block is not critical and is updated only at the beginning. The output bin file is capable to process I/Os and eHS solver that emulates the FPGA interface with CPU.

4.2.2. Synchronization and Data Communication

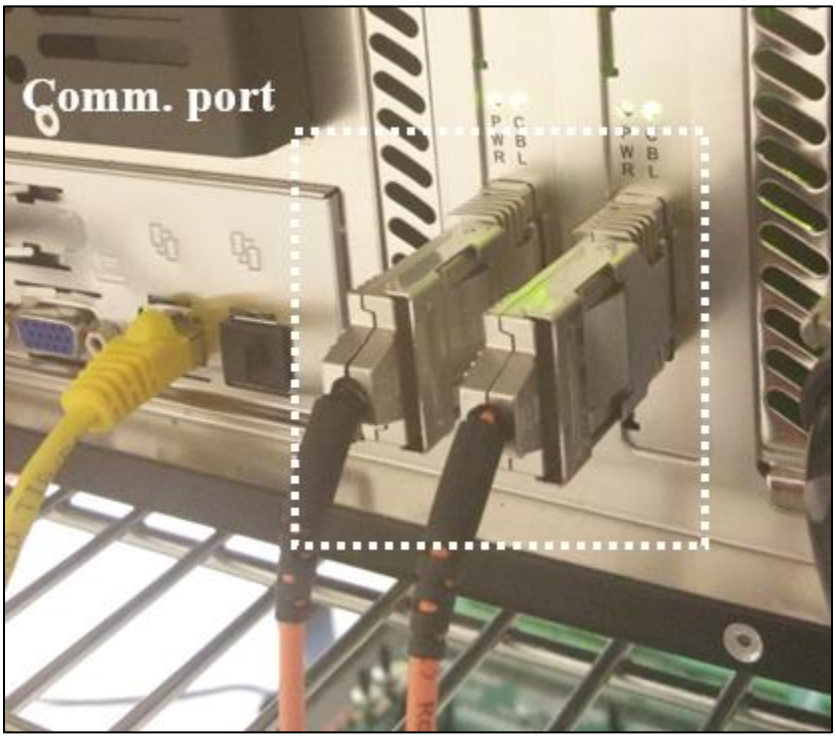


Figure. 30. Communication port (PCIe port for Optical, LAN port for host)

The PCIe (PCI express port) is used to connect PCIe board on FPGA with OPAL CPU using a fiber optic cable. Also, to capture updates from CPU, host is connected to CPU using LAN.

CHAPTER 5: IEEE 1547 Compliance and Proposed Scheme

5.1. IEEE 1547

The series of IEEE 1547 documents are standards for grid integration of Distributed Energy Resource (DER). This standard provides interconnection technical specifications and requirements. It establishes major criteria and requirements for interconnection of distributed resources (DR) with Electric Power System (EPS).It could be used to evaluate performance, operation, testing etc. of the system interconnection. The important node is the point of common coupling.

5.2.Test Environments and Scenarios

Recent changes in IEEE 1547 standards [4,5] provide guidelines for reactive power capability of DER both in terms of injection and absorption. Continuous operation of DER is acceptable provided with grid support during abnormal conditions. For abnormal voltage conditions, reactive power shall be provided subject to DER capacity and is required to be back to normal operation, when voltages become normal. The terminology used when DER injects reactive power is ‘overexcited’ and when DER absorbs reactive power is ‘under-excited’. The amounts of reactive power injection would also depends on the active power output during operation. The DER would inject reactive power only in the case when active power output is at least minimum steady state active power capability, or 5 % of rated power, whichever is greater. For operation greater than the minimum level of active power, the minimum reactive power injection or absorption capability is given in the Table below:

Table 3: Minimum reactive power capability.

Injection capability as % of nameplate S rating (kVA)	Absorption capability as % of nameplate S rating (kVA)
44 %	44 %

Minimum reactive power requirement [5] is as shown in figure below. It is allowed to curtail active power in order to meet reactive power.

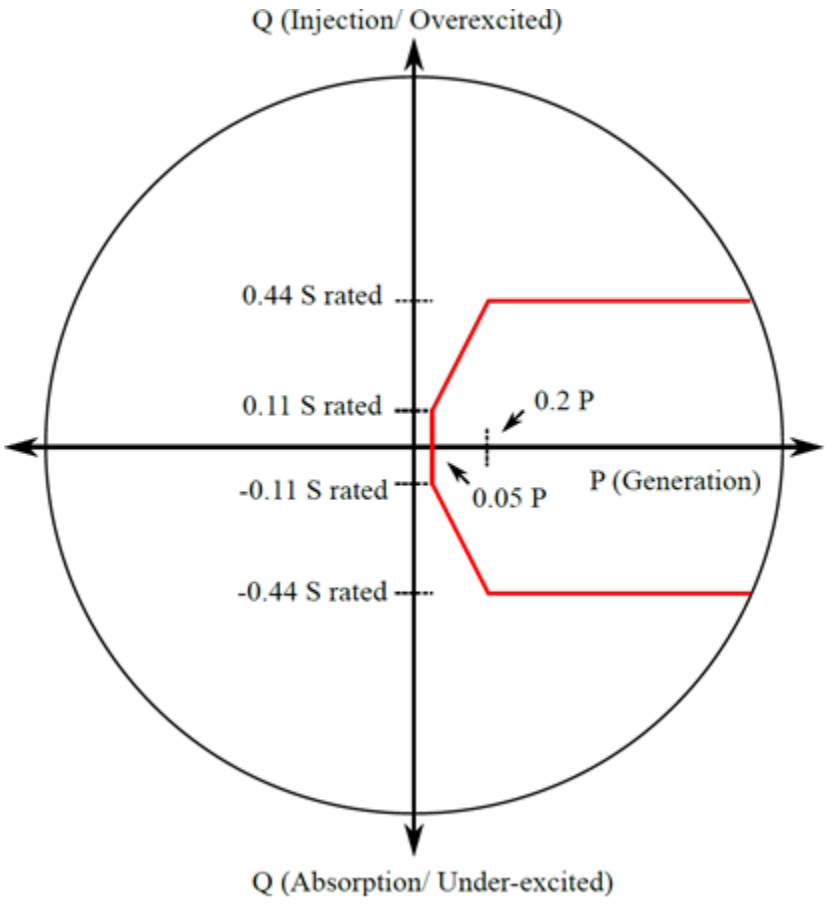


Figure. 31. Minimum P-Q capabilities

Note: The studies shown in this work is taking into account the minimum reactive power requirement. It is to be noted that the set points can be adjusted as specified by the Area EPS operator. Hence, for all results shown for reactive power support, 44% is the benchmark that is followed.

5.2.1. Voltage and Reactive Power Control

Before implementation of the control strategies to provide grid support, it is to be noted that the incorporating the control function does not put a requirement for DER to operate at operating points that are outside the minimum capabilities as specified in the table above. However, it is required for DER to have capabilities to provide the following control modes that support reactive power compensation. These modes [5] are activated in a mutually exclusive fashion based on the requirement.

- Constant power factor mode (Default: Unity power factor)
- Voltage-reactive power (Volt-VAR) mode
- Active power-reactive power mode (Watt-VAR)
- Constant reactive power mode

5.2.2. Voltage and Active Power Control

This control method provides limitation on maximum active power as a function of voltage. This can be enabled and could remain active when active while the V-Q modes are enabled. Only overvoltage scenarios are dealt using this scheme provided the DER do not absorb real power.

- Voltage-active power mode (Volt-Watt)

It is to be noted that DER can operate at a power factor other than specified by Area EPS operator if there is a demand for reactive power by local EPS. Also, the mode selection and changing mode settings is the responsibility of the DER operator as specified by Area EPS operator within given time.

5.2.3. Implementation of Control Modes

In the subsequent work, the main focus is on Volt-VAR mode. Also, scenarios of operation of Volt-Watt mode is also discussed and implemented.

- Volt-VAR mode: This specifies reactive power as a function of voltage. Key guidelines are:
    - DER must follow the piecewise linear Q-V characteristic as shown in figure
    - These characteristics would be based on the parameters in the table. Please note that the table provided only mentions the default parameters. However, these parameters are adjustable.
    - Open loop response time is 5 s.

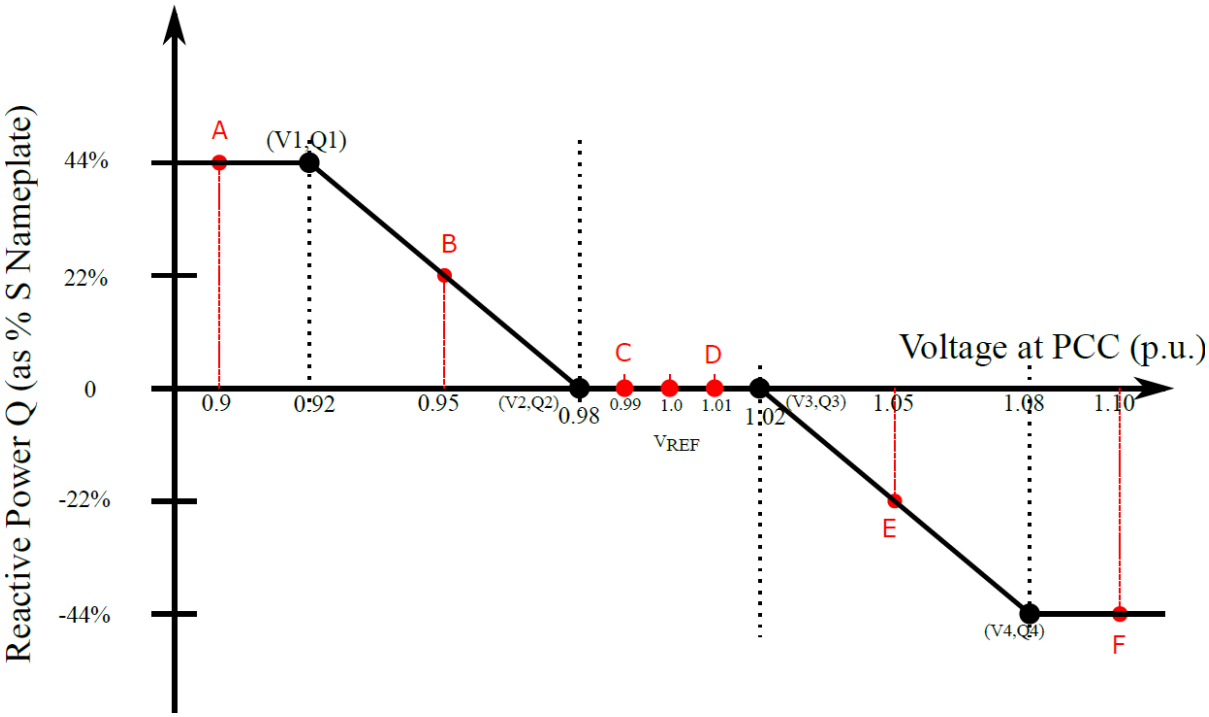


Figure. 32. Q-V Characteristics

(Note: The points marked A, B, C, D, E, F are for evaluation purposes only)

Table 4: Q-V Parameters.

V		Q	
V1	0.92 p.u.	Q1	44% of nameplate S rating, injection
V2	0.98 p.u.	Q2	0
V3	1.02 p.u.	Q3	0
V4	1.08 p.u.	Q4	44% of nameplate S rating, absorption

Certain cases are tested to evaluate the control function in the Volt-VAR mode. The points of interest, in general, are in between the boundary condition for each voltage range. Broadly, there are six zones. For generality sake, the names of these zones are kept same as that of the points marked on the figure above, and hence would be called as follows:

Note: VL and VH are low and high set points. For this study these are 0.90 p.u. and 1.10 p.u.

Table 5: Set points based on Q-V characteristics.

Operating Point	Zone
Point A	$VL < V \leq V1$
Point B	$V1 < V \leq V2$
Point C	$V2 < V \leq Vref$
Point D	$Vref \leq V < V3$
Point E	$V3 \leq V < V4$
Point F	$V4 \leq V < VH$

5.3.Proposed Scheme

Following are some of the test scenarios programmed to create certain voltage sag or swell and based on the detection strategy, controller design is proposed.

In order to create a test scenario, we require some data on the load that gets connected accidentally that might affect the voltage magnitude. However, this is very uncertain as the PCC voltage is affected by multiple factors and effect of multiple load configuration. Here for the sake of simplicity, we assume just one load getting connected accidentally that affects the voltage to a considerable extent (Amount relative comparable to the p.u. number in the table). For generality sake, and for testing purposes it is a good assumption to model the load using an R-L-C branch. It is intuitive that when the load is predominately inductive (R-L), for e.g. industrial induction motor drive, the PCC would observe a sag in the voltage, whereas, when the load is predominately capacitive (R-C) for e.g. a large capacitor bank, the PCC would observe a swell in the voltage. The amounts of sag and swells would depends on how much reactive power is demanded by the load.

Before looking into the load modelling, let's divert the attention to compensation schemes. There are two schemes that are proposed. The first utilizes the PLL results to estimate the amount of sag or swell in the PCC voltage and once it is detected, directs the controller to set the new references in order to follow the V-Q characteristics.

The second schemes also assume to have information on the load currents, in addition to the amount of PLL output. Using this extra information, the controller would be able to take a more informed decision of the amount of reactive power to be transacted in order for the voltage compensation. Subsequent sections in this chapter demonstrates the implementation of both the schemes.

5.3.1. Controller:

The grid connected inverter is controlled to inject or absorb active and reactive power to the grid. Rotating reference frame (d-q frame) is used to control the reference and actual variables. The sequence of events begin with the operation of a Phase Locked Loop (PLL) [8,9]. This detects the grid phase and frequency and tries to align one of the direct or quadrature

component of the rotating voltage vector with the grid voltage. Once the two phase angles catch each other, the phase is locked. After this is achieved, then the inverter operation is started by supplying the gate pulses to the power switches in three phase half bridges. This depicts the normal operation of the inverter. After a pre-determined amount of time, the load is connected at the PCC between the inverter and the grid. This create a change in the PCC voltage, depending on sag (inductive load) or swell (capacitive load). Grid codes allow some response time, within which DER is required to take action for the voltage compensation. Keeping this in mind and evaluating the controller dynamic response, another pre-determined setting is activated to update the reference set points in order for Volt-VAR control.

5.3.2. Algorithm to find load parameters

Since, in order for evaluation of inverter performance and purpose of grid compliance, we are simulating some scenarios of disturbance in the PCC voltage, it would not be easy to predict the amount of change in PCC voltage with the given load [16]. This is because, as soon as the load is connected the current vectors change instantaneously and based on the redistributed grid current, the drop across the grid side impedance will determine the change in PCC voltage.

An iterative scheme is developed to determine the affect due the load connection and illustrated as the logic flow as shown below and implemented using an iterative MATLAB C code.

This mechanism assume prior information of the following: Filter inductance, grid side impedance, grid voltage, inverter current reference set point. We aim to figure out the impact of connecting a load with given power rating, S and power factor. This is fundamentally an error correction technique where the actual values are compared with calculated values to determine errors and update in every iteration until error becomes minimal. The idea is to begin with aligning the PCC currents with grid voltage. Also, to begin, it is assumed that PCC voltage magnitude is equal to grid voltage magnitude.

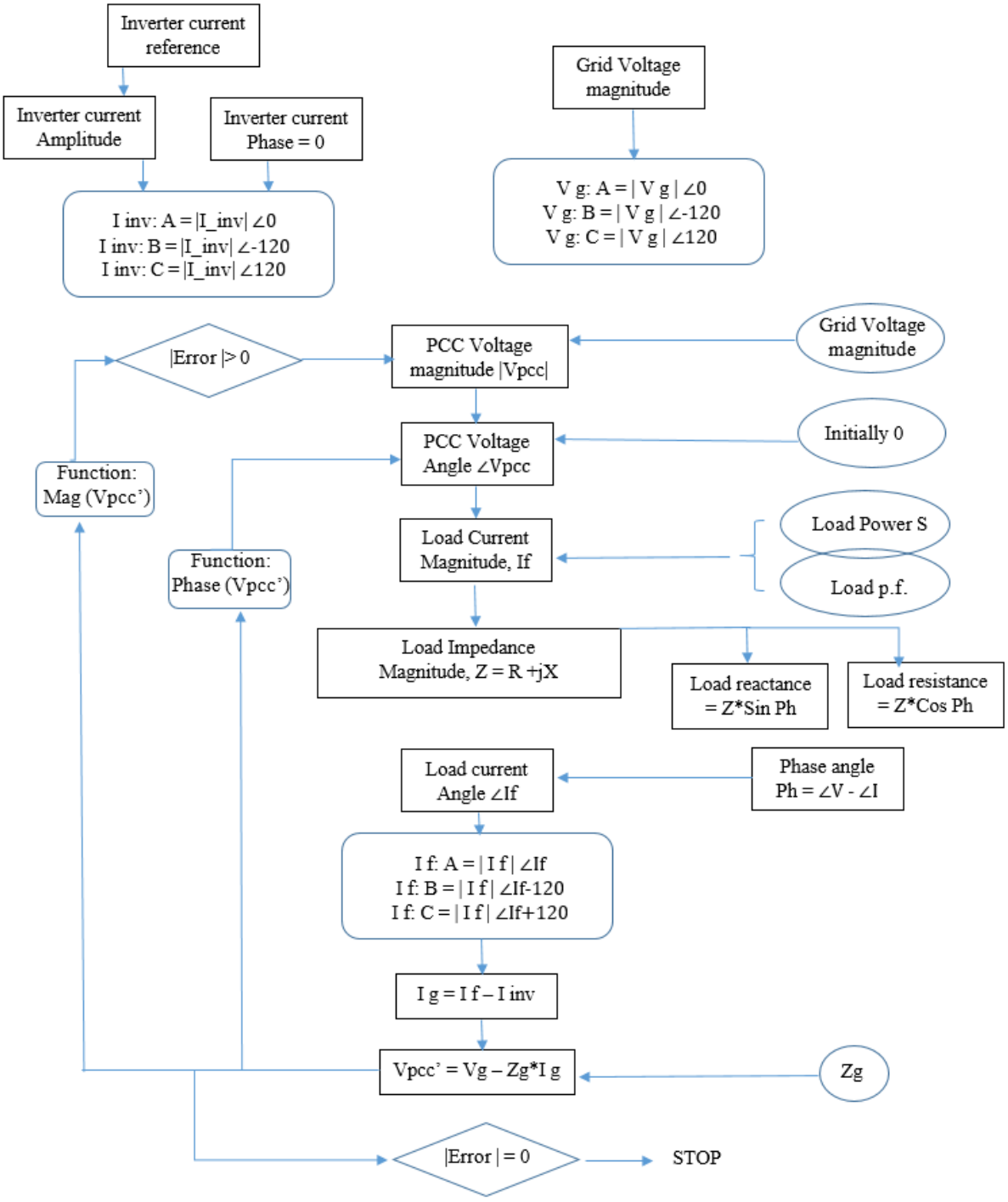


Figure. 33. Algorithm for load model parameters

5.3.3. Mode Selection based on PLL Output

Based on the Q-V characteristics and Set point table, a look up table is referred.

Table 6: Look up table for controller.

Operating Point	Values
Point A	0.90 p.u. $< V \leq$ 0.92 p.u.
Point B	0.92 p.u. $< V \leq$ 0.98 p.u.
Point C	0.98 p.u. $< V \leq$ 1.00 p.u.
Point D	1.00 p.u. $\leq V <$ 1.02 p.u
Point E	1.02 p.u. $\leq V <$ 1.08 p.u
Point F	1.08 p.u. $\leq V <$ 1.10 p.u.

5.3.4. Logic Sequence for Controller

The logic block takes input from the detection scheme as the ratio of PLL output and reference voltage. Based on the ratio, the logic looks for the value in the look up table and using the selector switches, takes appropriate action to trigger the change in set point reference of q component of the inverter current. The case shown in the figure depicts the case of overvoltage. Fundamentally, there are three regions of interest, when Vref $\leq V <$ V3, V3 $\leq V <$ V4 and V4 $\leq V <$ VH. Once the region is triggered, there is an instantaneous update as the digital blocks have very less latency. In this work, the activation time settings is set externally using a step block.

5.3.5. Under-voltage or Over-voltage Detection

The PLL output Vd is compared with a reference PLL voltage and the ratio depicts the percentage sag or swell. Below is the block diagram for detection scheme and control mode selection.

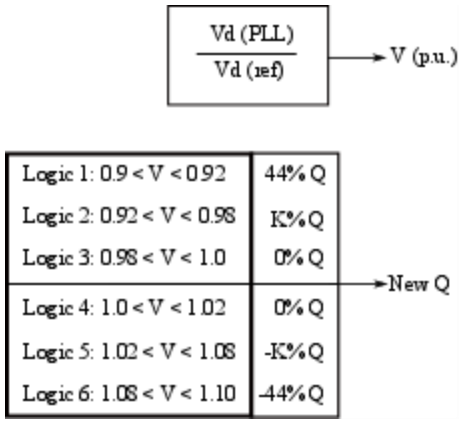


Figure. 34. Detection Logic

Value of K is calculated from the following relation:

$$K = \frac{0.44}{0.06}(0.98 - V), undervoltage \quad or \quad K = \frac{0.44}{0.06}(V - 1.02), overvoltage$$

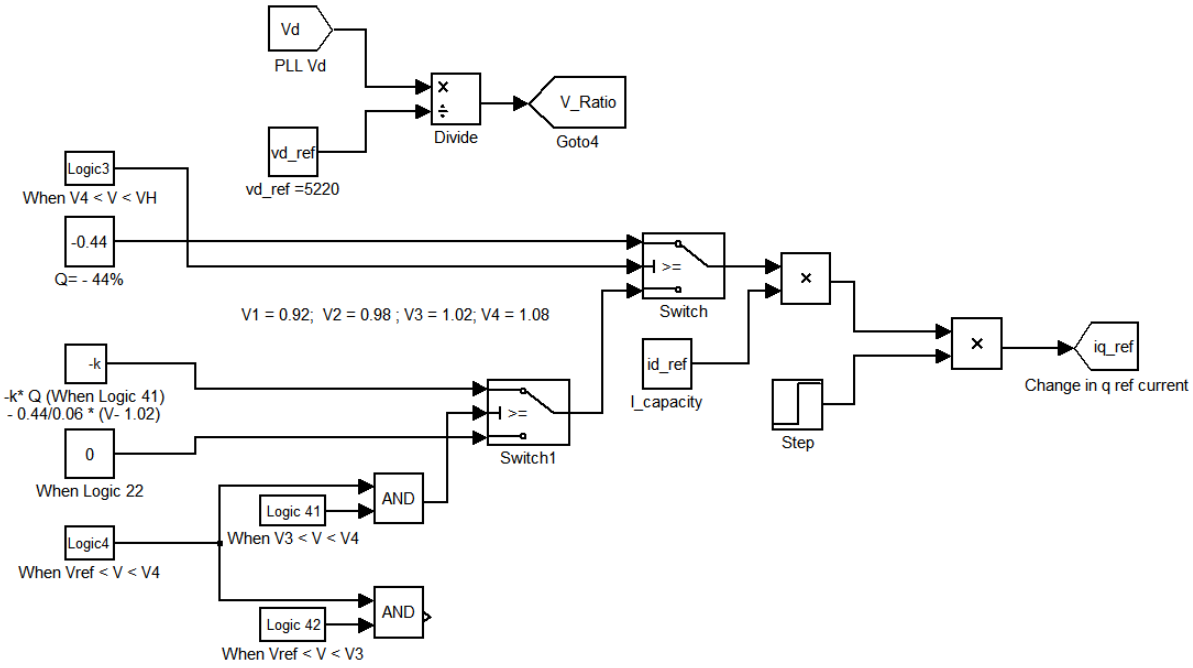


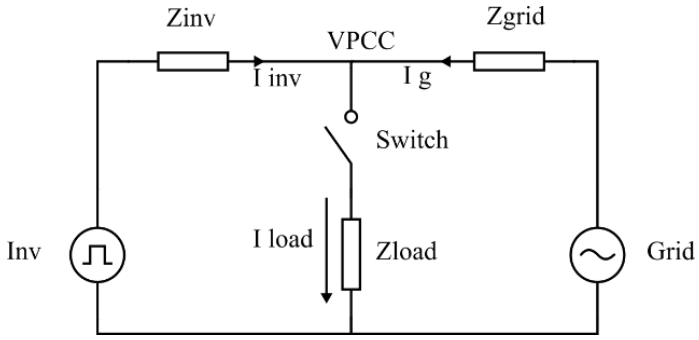
Figure. 35. Detection of overvoltage and corrective action on set points

CHAPTER 6: Test Scenarios and Results

Following tests were conducted to evaluate the performance for grid support Volt-VAR function so as to meet grid code compliance. These tests are studied as different cases based on the level or severity of the disturbance.

6.1. Case 1: Volt-VAR Control (VVC) when V < 0.92 p.u.

The inductive load modelled is of S = 2.6 MVA rating and p.f. 0.3 (L = 13.3 mH, R = 1.57 Ω) The waveforms captured on oscilloscope are scaled down in magnitude. The scaling factor for current and voltages are 0.01x and 0.001x respectively. In addition OPAL RT has an internal attenuation of 0.1 x.



The spikes in PCC voltages are due to the high frequency ripple.

6.1.1. Inverter currents and PCC voltages

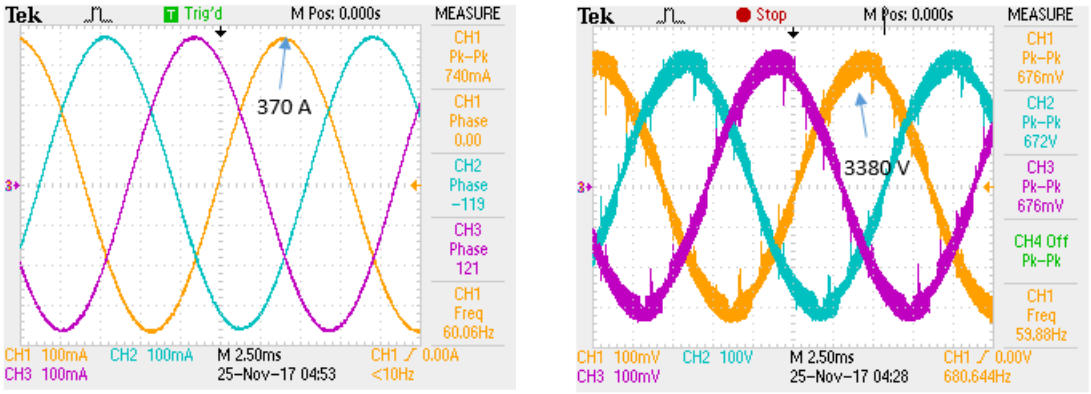


Figure. 36. Case 1: Inverter currents and PCC voltages

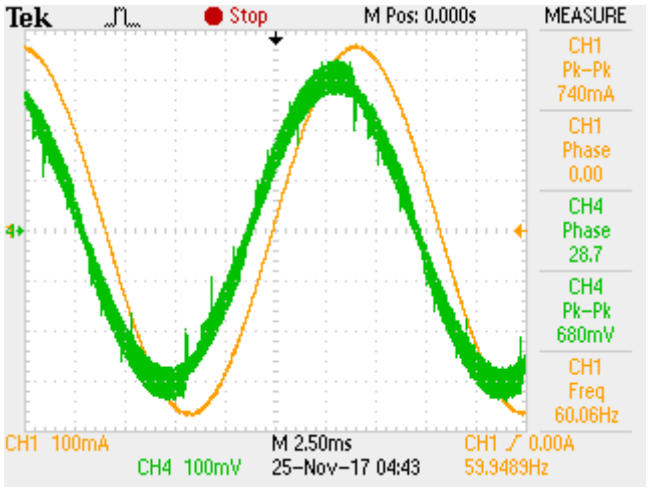
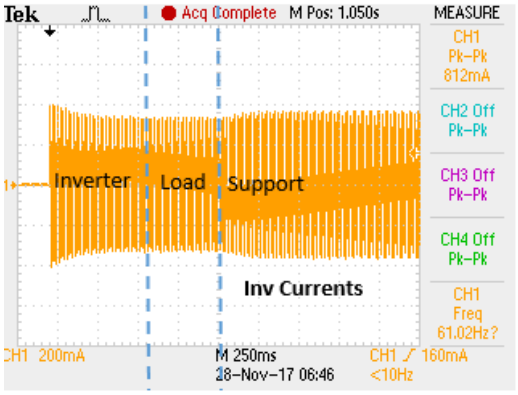


Figure. 37. Case 1: Phase Difference between 3 phase voltage & currents ~ 29 °



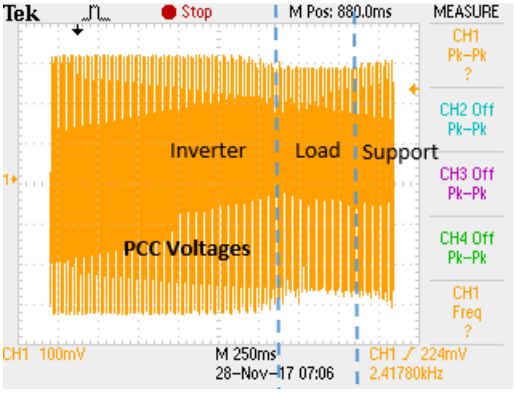


Figure. 38. Spectrum of different operating points for reactive VPCC support

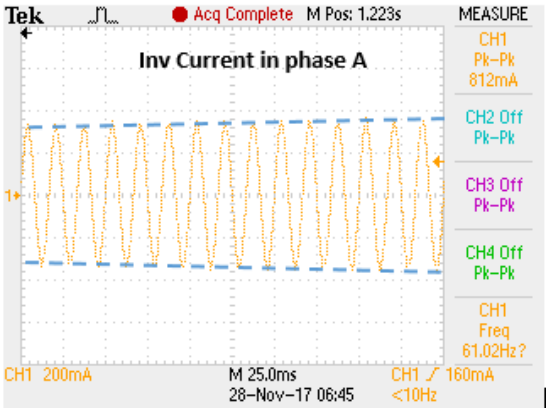


Figure. 39. Inverter current (zoomed) increases as reference set point is increased

6.1.2. Results from eHS Scope:

The time stamps for each event in simulation explicitly defined is pre-defined and coded in the control loop after careful consideration of steady state intervals

The time scale is from 0 to 5 s to demonstrate the comparative response of the controller with real time variations (fastest)

The region of operation is depicted as a step function i.e. from inverter to grid connected region instantaneously (worst case). However, it reality the transition would take place within few fundamental cycles. Here a comparison of fast and slow transition is depicted. Fast transition results in overshoot due to bandwidth limitations and imperfect de-coupling of P and Q. The transition can be triggered over a ramp function instead of a step function thus allowing multiple fundamental cycles for the new set points to settle.

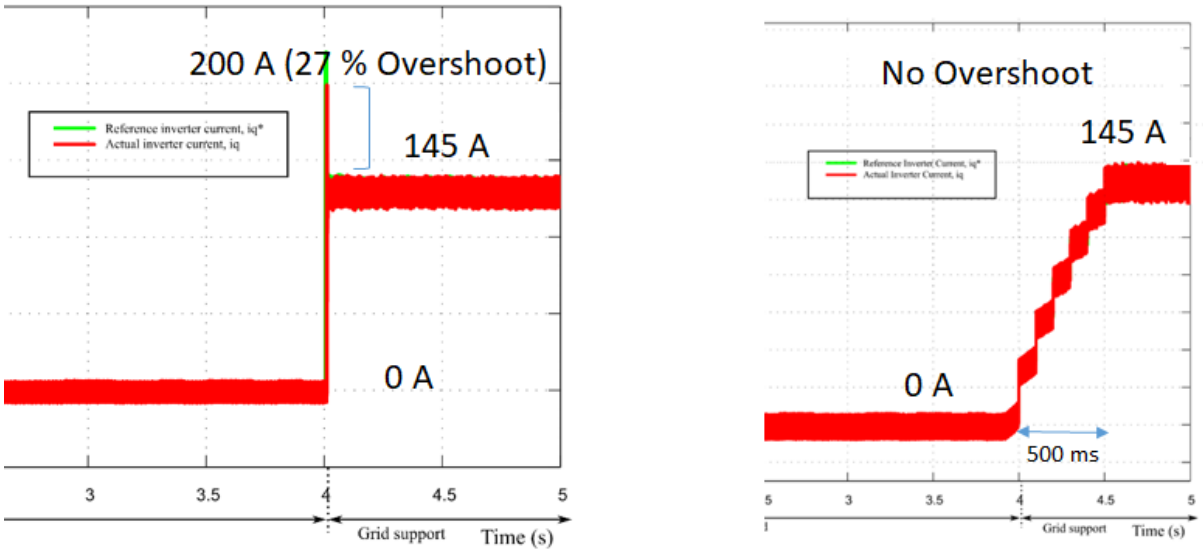


Figure. 40. Slower transition of reactive power compensation

The amount of P and Q transaction in simulation demonstrate the minimum capability of the DER. The reference set points can be modified as demanded & specified by Area EPS

It is to be noted that the time intervals are externally set to < 0.5 s, 2 s and > 4s for measurements. These are NOT the response times.

6.1.2.1. Magnitude of voltage vector

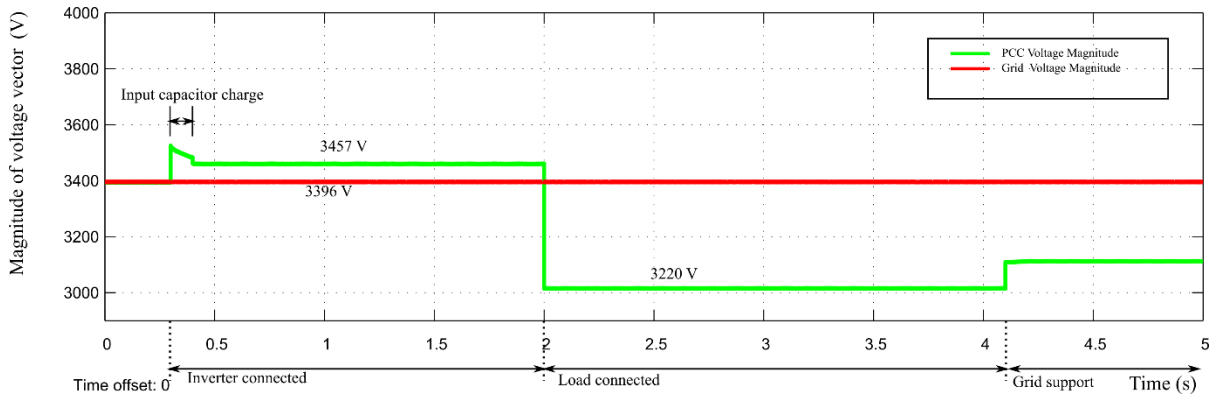


Figure. 41. PCC Voltage Dip

6.1.2.2. Magnitude of Current vector

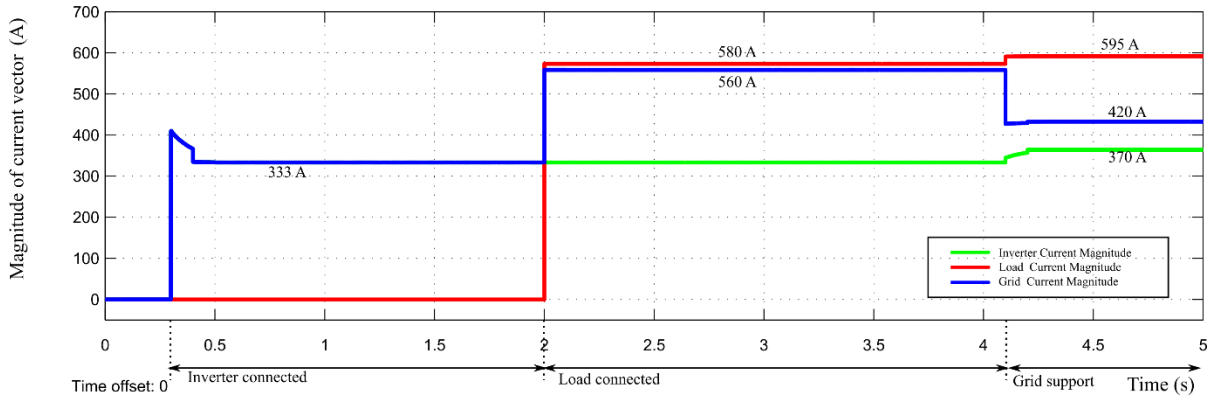


Figure. 42. Current vector magnitude

6.1.2.3. PLL Output Vd, Vq

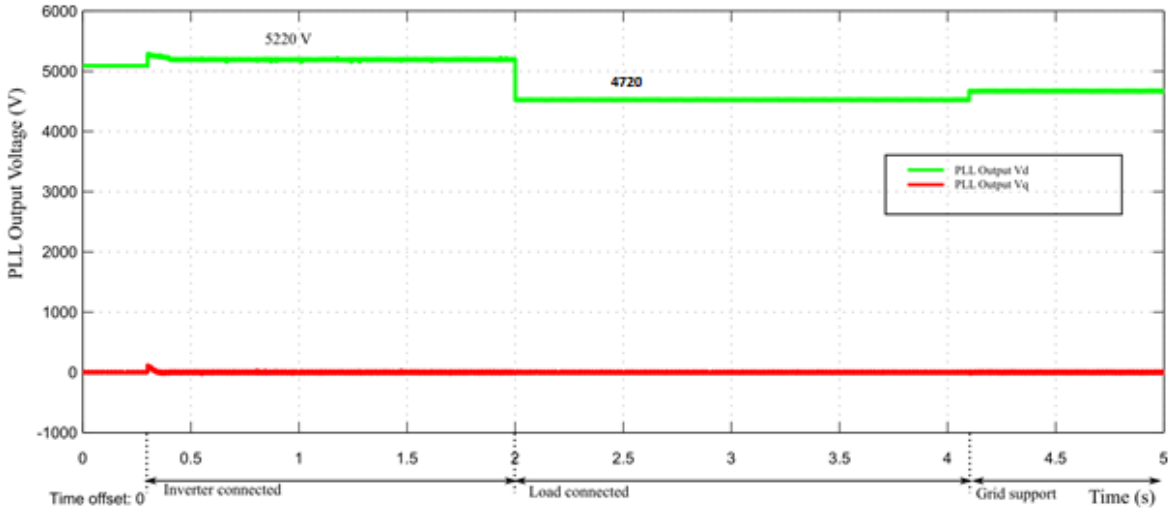


Figure. 43. Detection of Sag from PLL Output

Sag is detected from 5220 V to 4720 V (0.904 p.u.). We inject 44% of Q.

6.1.2.4. Inverter current in d axis

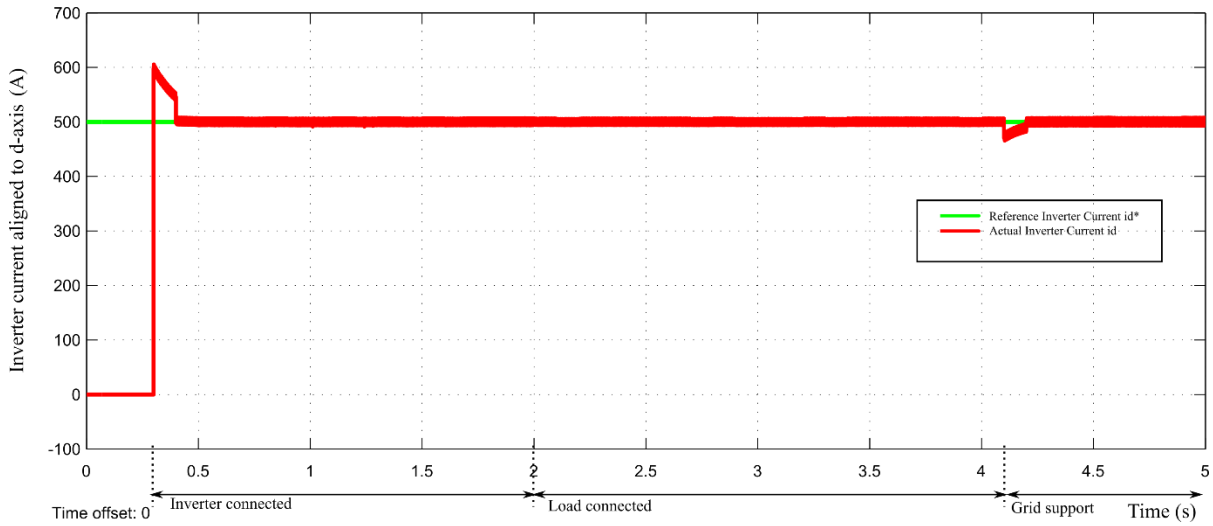


Figure. 44. Inverter Current in d axis

6.1.2.5. Inverter Current in q axis

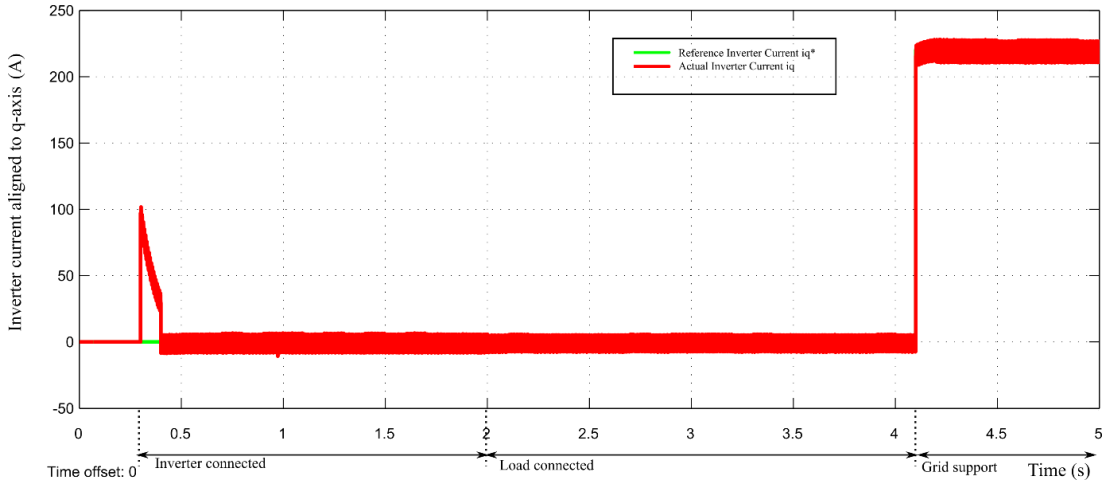


Figure. 45. Change in q component of inverter current to support grid

This shows that iq reference has now been updated to 220 A (44% of 500 A). The actual q component of inverter current tracks the reference.

6.1.2.6. Transition of iq ref (Expanded View)

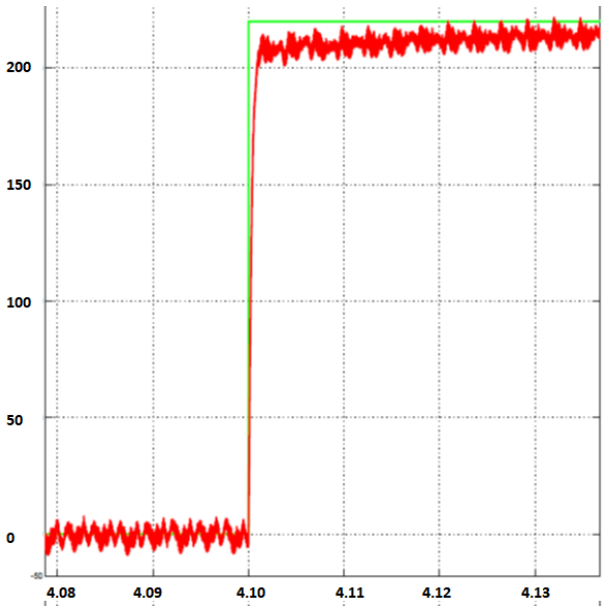


Figure. 46. Zoomed iq showing transition transients

Current loop update every quarter cycle and bandwidth decides settling time (20% of 0.01s = 2 ms). From controller bandwidth i.e. 500Hz, it also confirms the settling time of 2 ms.

6.1.2.7. Active Power P

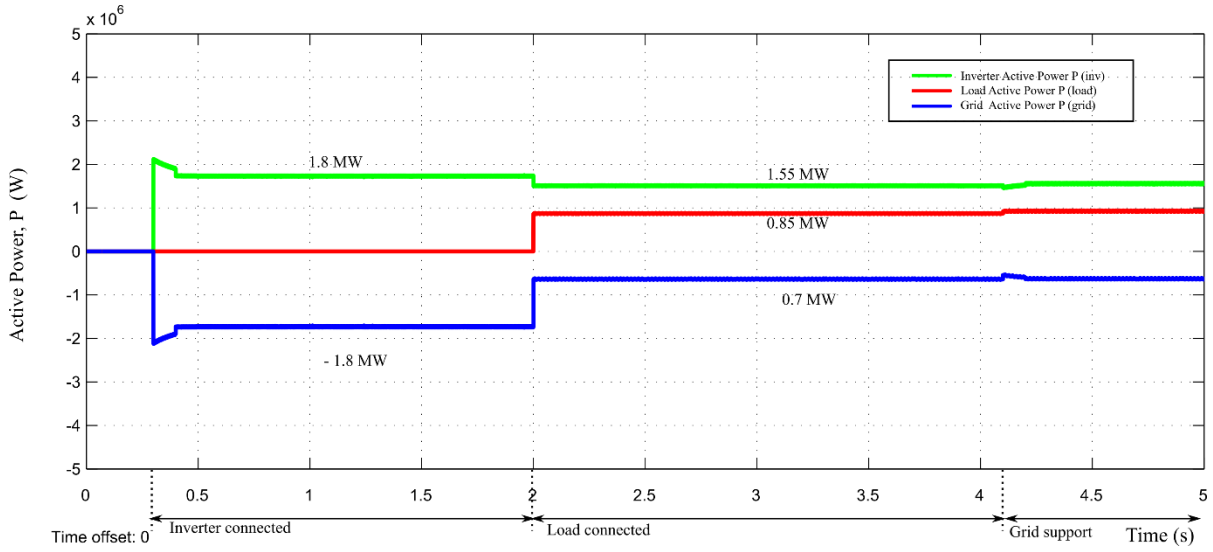


Figure. 47. Active power transitions

6.1.2.8. Reactive Power Q

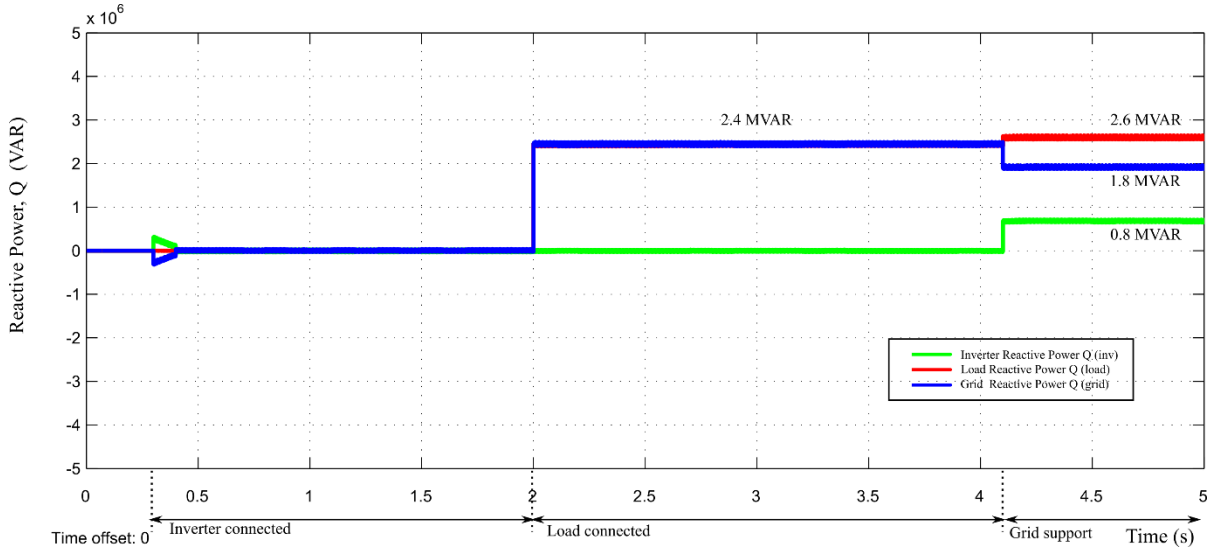


Figure. 48. Reactive power transitions

6.1.2.9. Apparent Power S

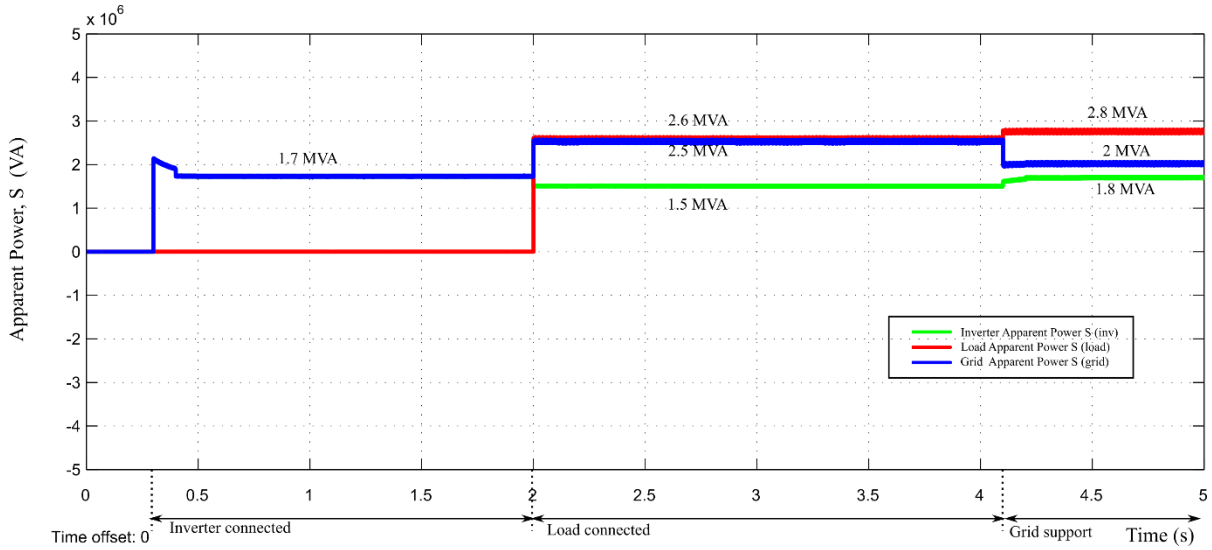


Figure. 49. Apparent power transitions

6.1.2.10. PCC Currents

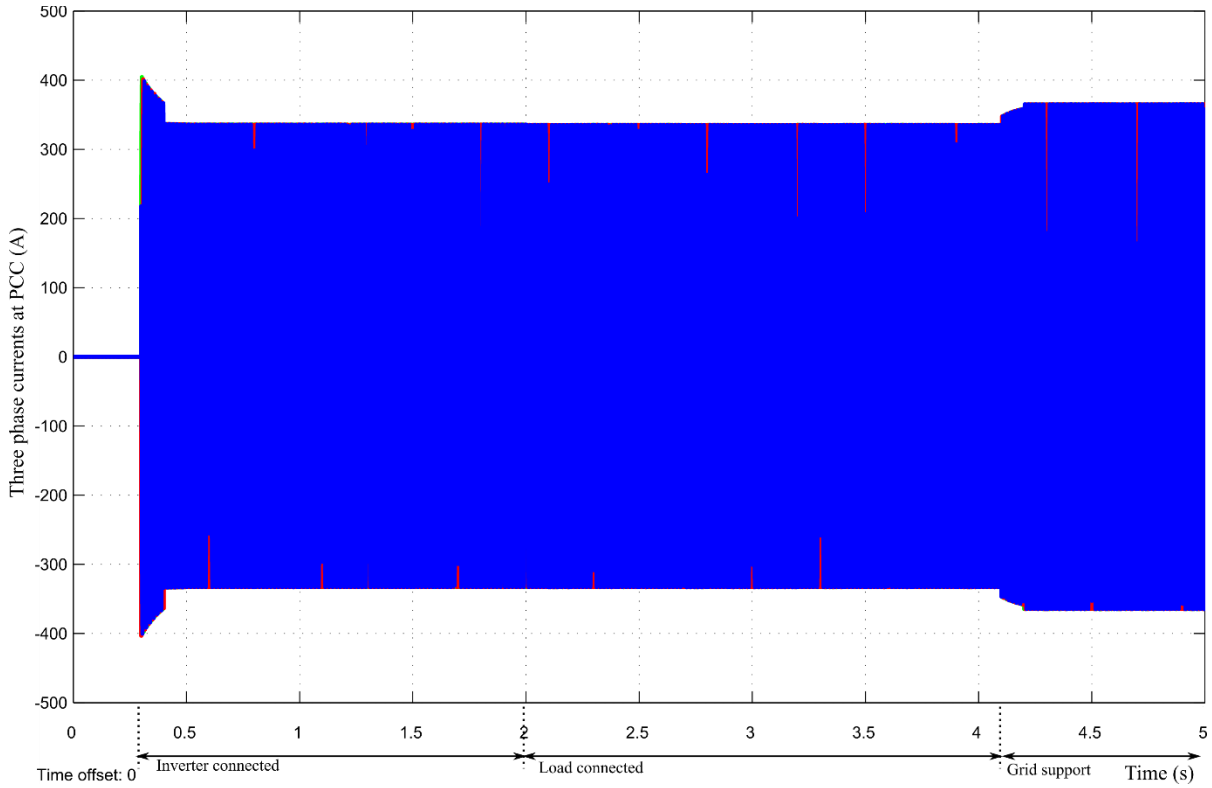


Figure. 50. Inverter currents transitions

6.1.2.11. PCC voltages

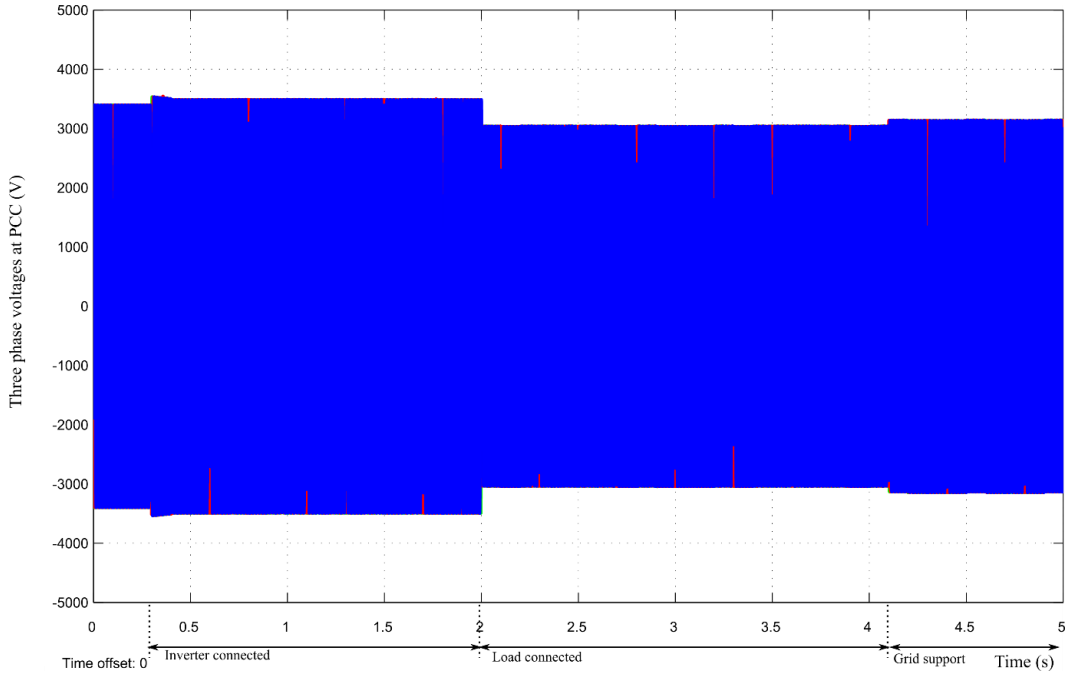


Figure. 51. PCC Voltage transitions

6.1.2.12. Phase variation in currents

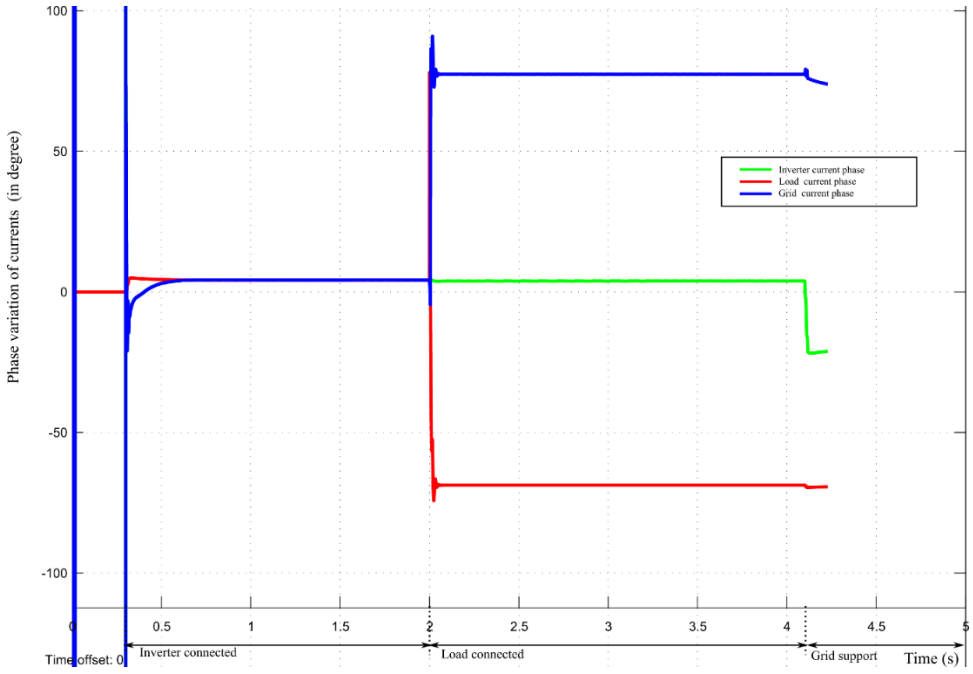


Figure. 52. Phase angles of different current vectors in inverter, load and grid branch

6.1.2.13. Phase variation in voltages

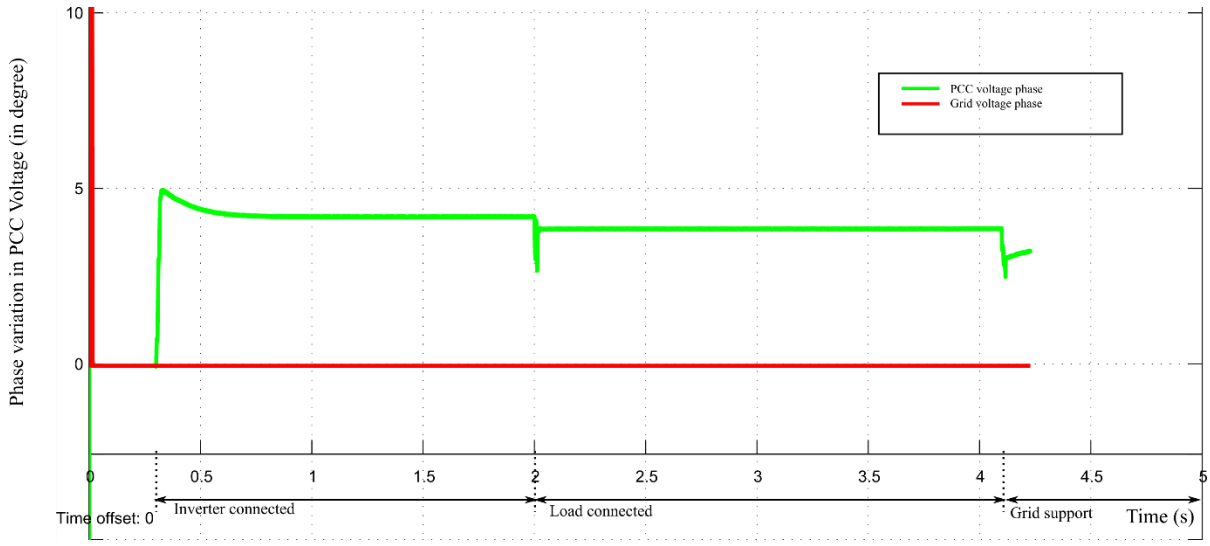
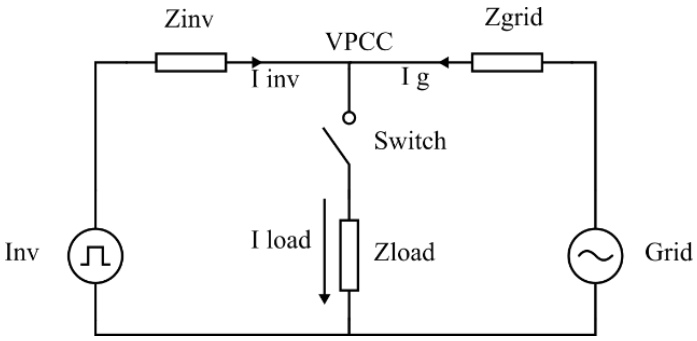


Figure. 53. Phase angles of grid voltage and PCC voltage vectors

6.2. Case 2: Volt-VAR Control (VVC) when 0.92 p.u. < V < 0.98 p.u.

The inductive load model is S = 1.49 MVA rating and p.f. 0.3 (L = 26.9 mH, R = 3.2 Ω) The waveforms captured on oscilloscope are scaled down in magnitude. The scaling factor for current and voltages are 0.01x and 0.001x respectively. In addition OPAL RT has an internal attenuation of 0.1 x.



6.2.1. Inverter currents and PCC voltages

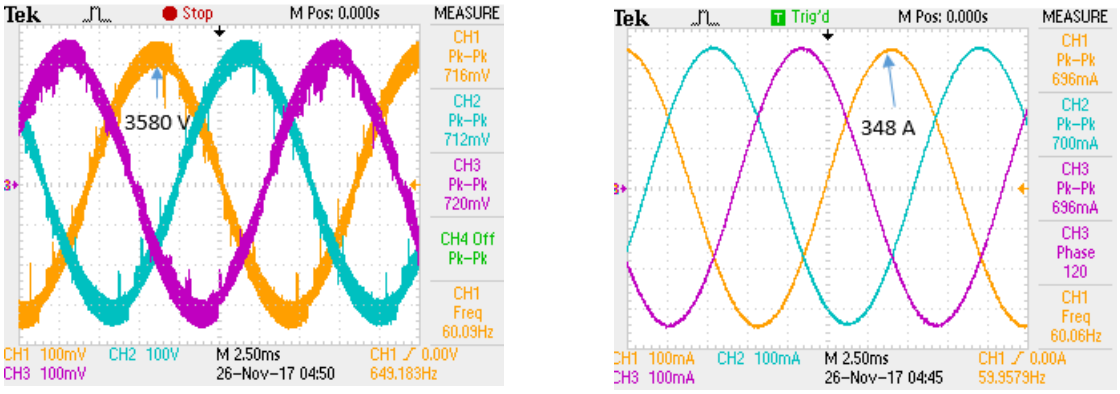


Figure. 54. Case 2: Inverter currents and PCC voltages

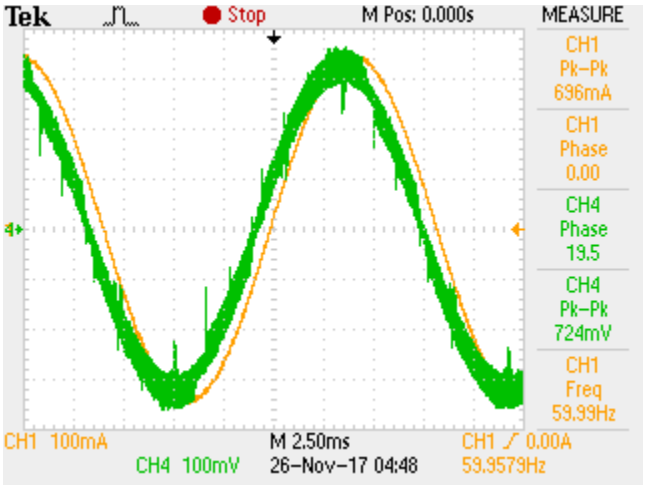


Figure. 55. Case 2: Phase Difference between 3 phase voltage & currents ~ 20 °

6.2.2. Results from eHS Scope:

In this case, the under voltage is detected by the PLL to be 0.94 p.u. Thus, based on the calculation, controller logic would update the set points for Q.

6.2.2.1. Magnitude of voltage vector

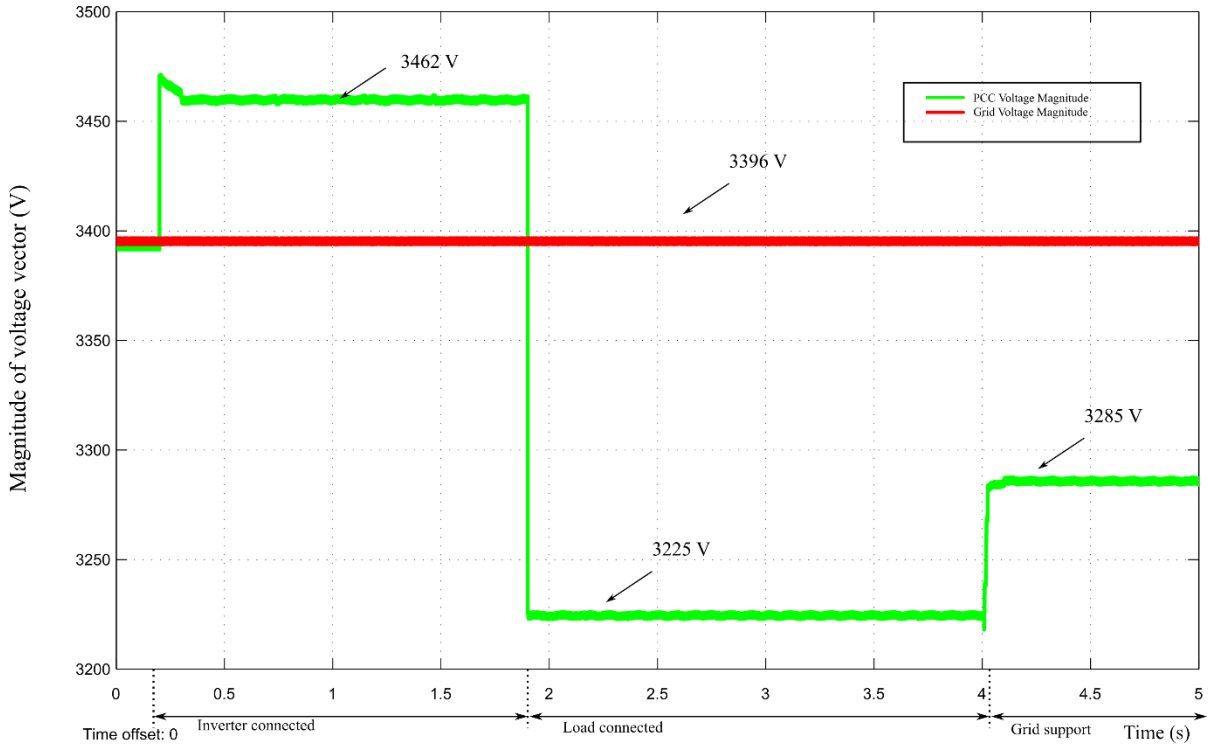


Figure. 56. PCC Voltage Dip

6.2.2.2. Magnitude of current vector

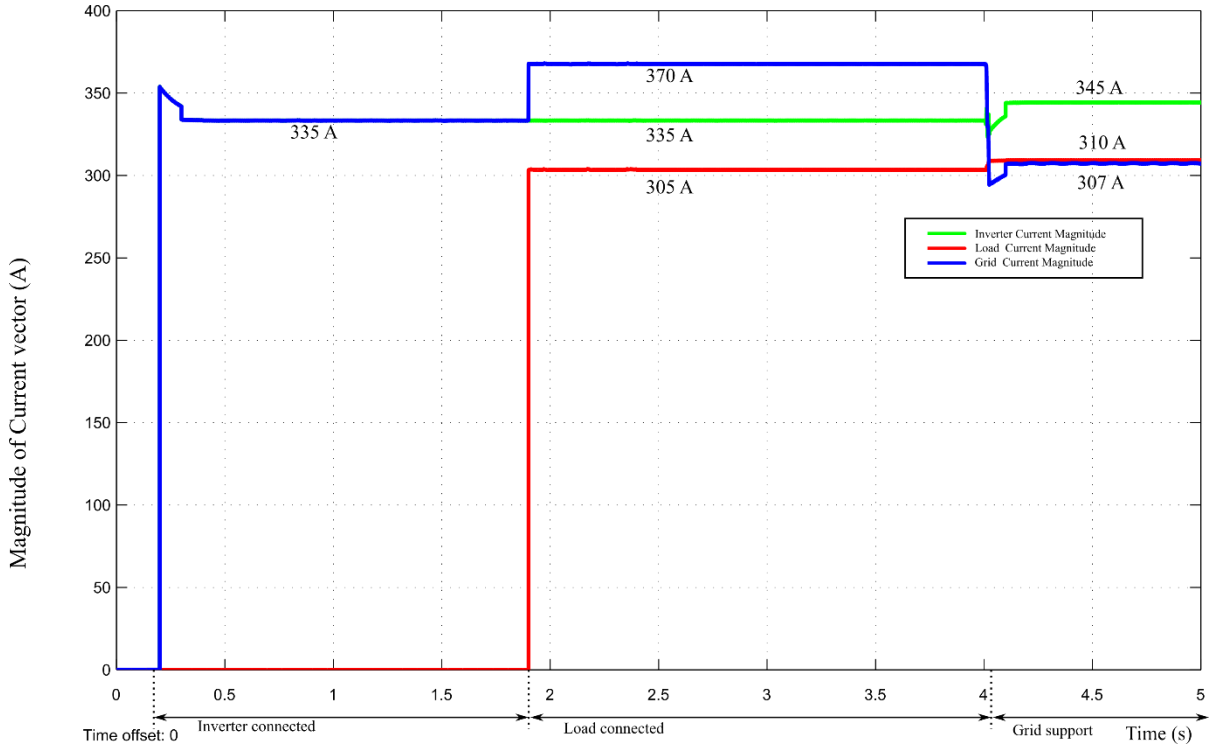


Figure. 57. Current vector magnitude

6.2.2.3. PLL output Vd, Vq

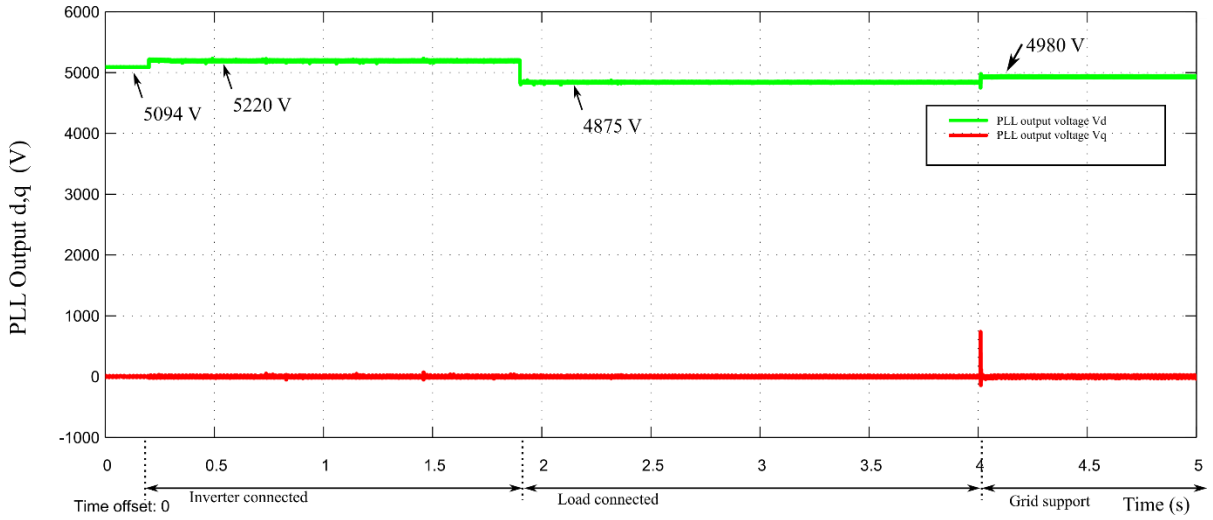


Figure. 58. Detection of Sag from PLL Output

From PLL output, we can measure the sag and take necessary action. So, after load gets connected the voltage at PCC is 0.94 p.u. (4875/5220). So, from the sag-swell table, we infer that this operating point is in zone B (0.92 p.u. < V < 0.98 p.u.).

Hence, the controller detects the operating point and calculates the set point of reference. So, Q injection is given by the following relation:

$$\mathrm{Q} = \frac{0.44}{0.06} x\ (0.98 - V)$$

$$\mathrm{Q} = \frac{0.44}{0.06} x\ (0.98 - 0.94)$$

$$\mathrm{Q} = 29.33\ \%$$

6.2.2.4. Inverter current in d axis

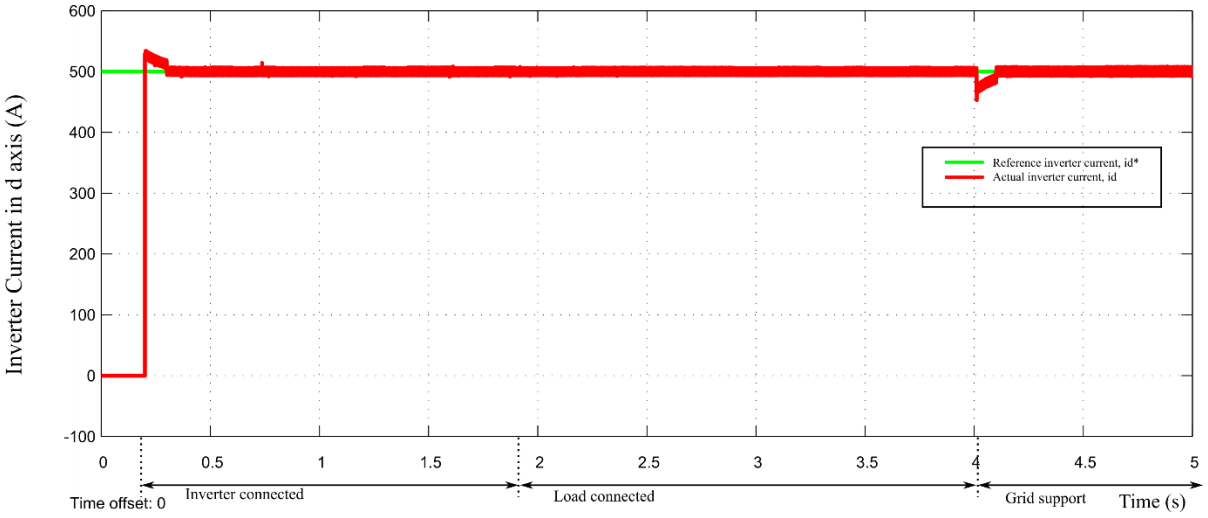


Figure. 59. Inverter Current in d axis

6.2.2.5. Inverter current in q axis

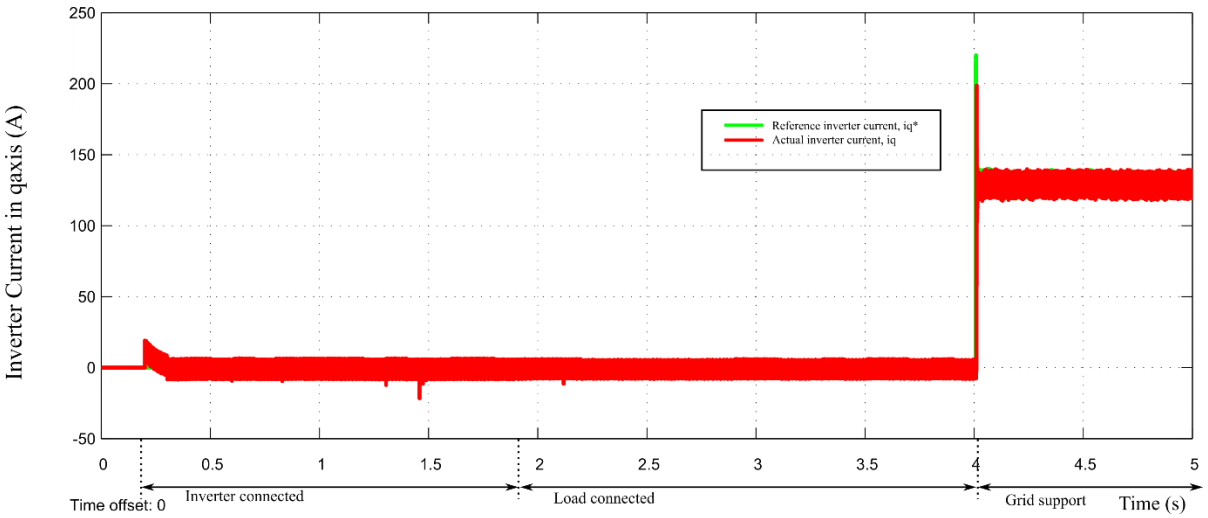


Figure. 60. Change in q component of inverter current to support grid

6.2.2.6. Active Power P

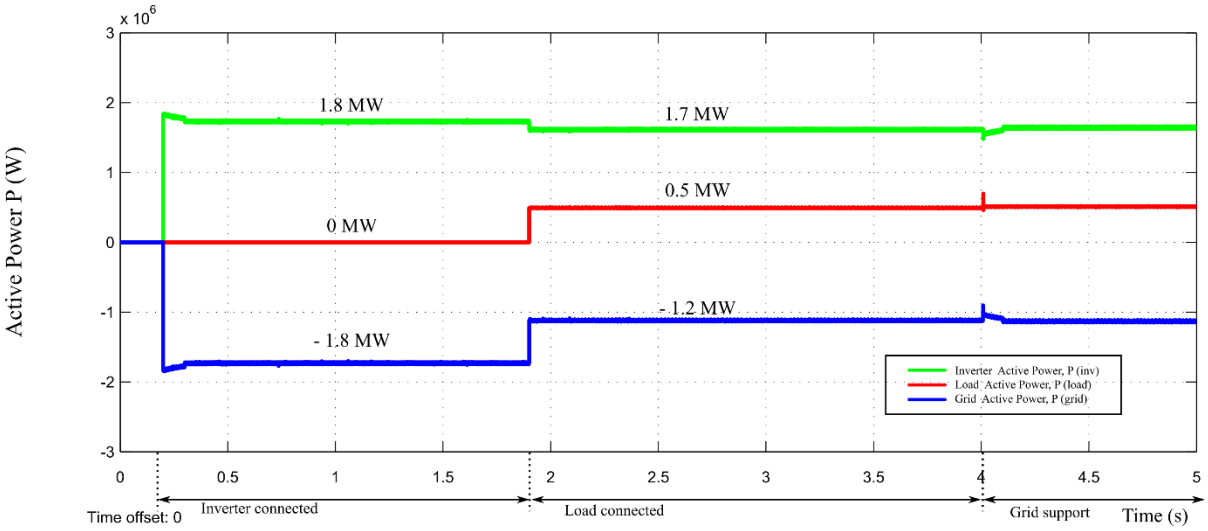


Figure. 61. Active power transitions

6.2.2.7. Reactive Power Q

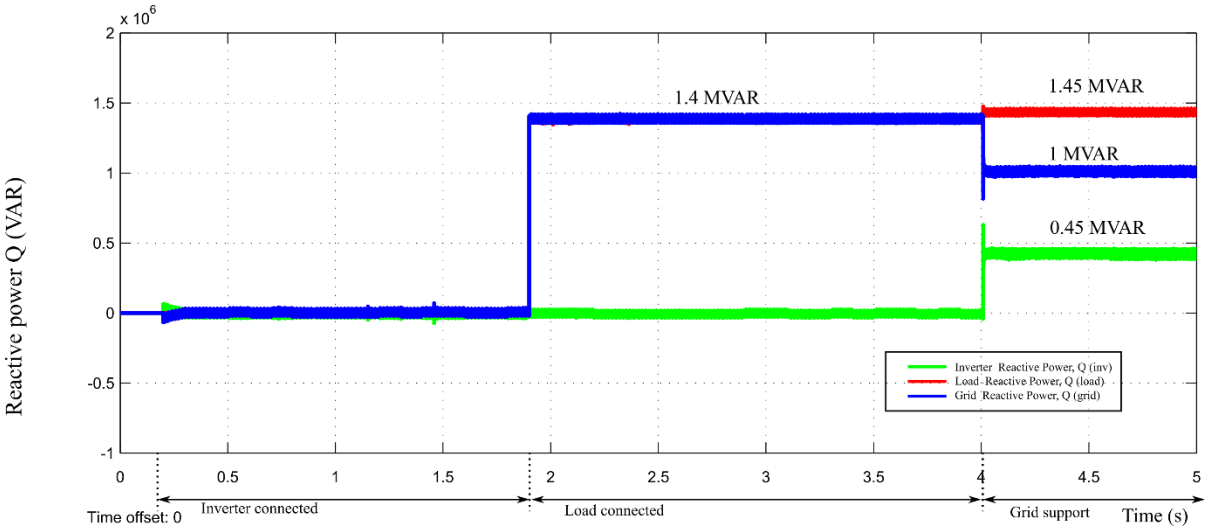


Figure. 62. Reactive power transitions

6.2.2.8. Apparent Power S

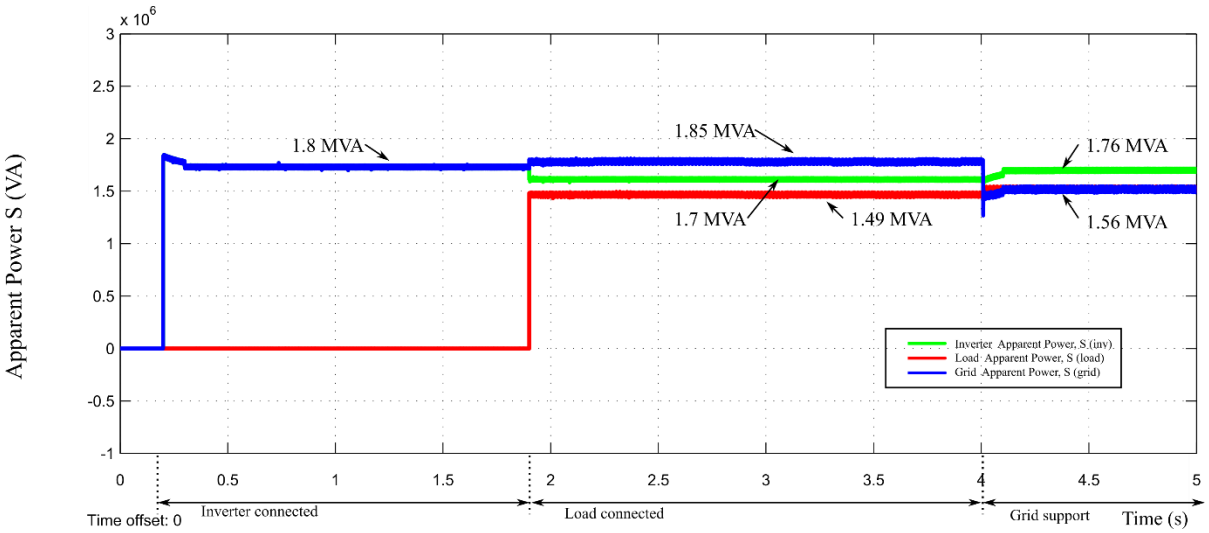


Figure. 63. Apparent power transitions

6.2.2.9. PCC currents

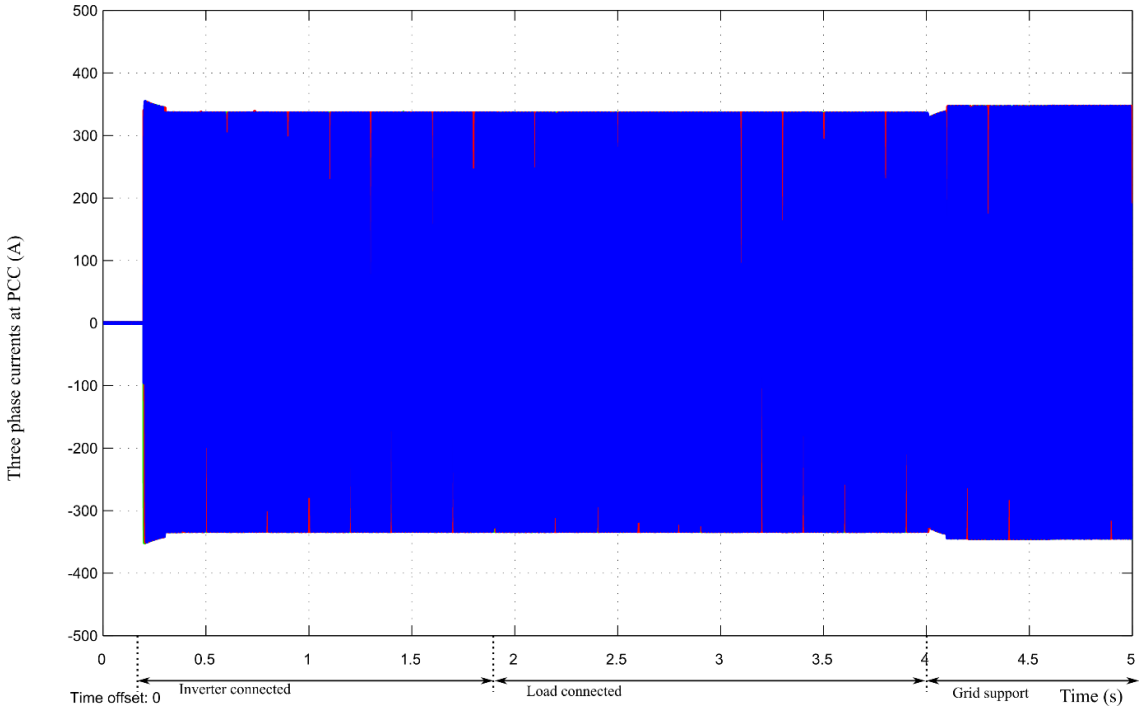


Figure. 64. Inverter currents transitions

6.2.2.10. PCC voltages

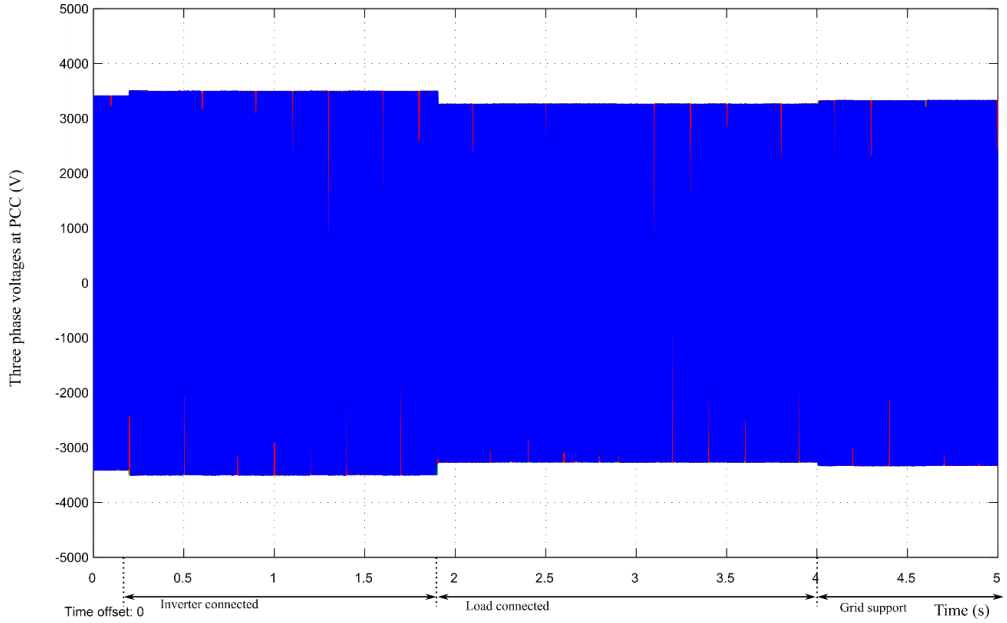


Figure. 65. PCC Voltage transitions

6.2.2.11. Phase Variation in Currents

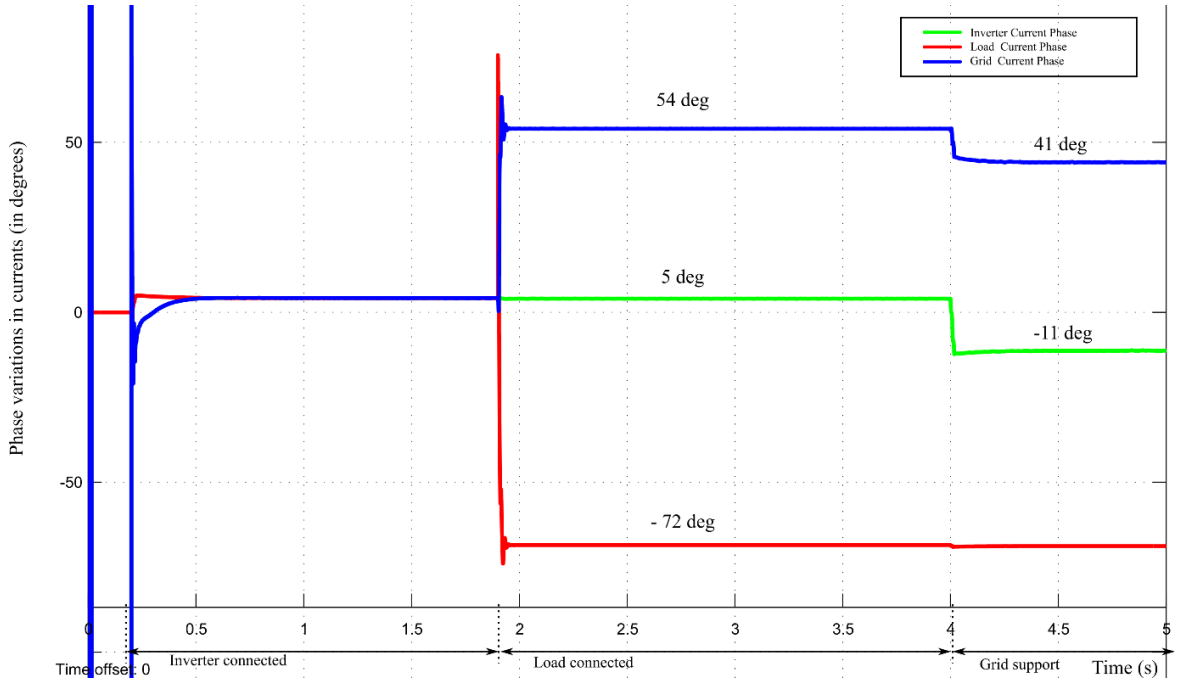


Figure. 66. Phase angles of different current vectors in inverter, load and grid branch

Based on the current vectors magnitude and phase analysis, the phasor representation is depicted in the figure below.

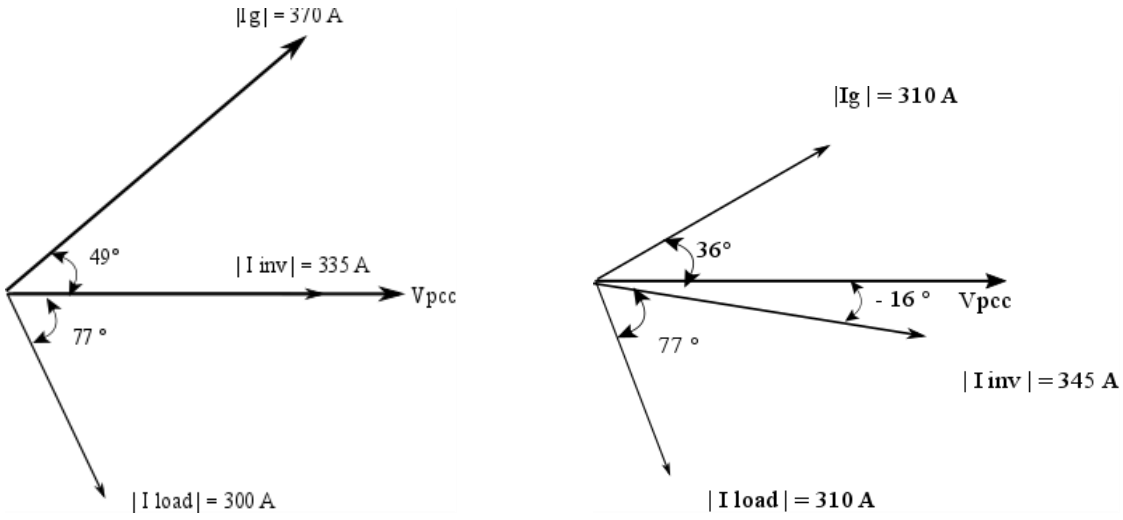


Figure. 67. Phasor representation of currents

6.2.2.12. Phase Variation in Voltages

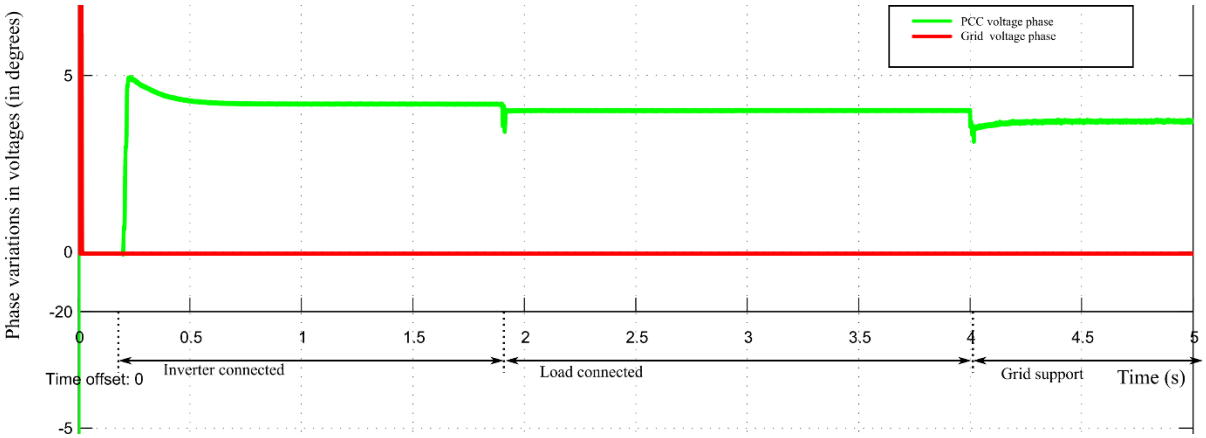


Figure. 68. Phase angles of grid voltage and PCC voltage vectors

6.3. Case 3: Volt-VAR Control (VVC) when 0.98 p.u. < V < 1.0 p.u.

The inductive load modelled is S = 0.36 MVA rating and p.f. 0.3 (L = 0.13 H, R = 16.15 Ω) The waveforms captured on oscilloscope are scaled down in magnitude. The scaling factor for current and voltages are 0.01x and 0.001x respectively. In addition OPAL RT has an internal attenuation of 0.1 x.

6.3.1. Inverter currents and PCC voltages

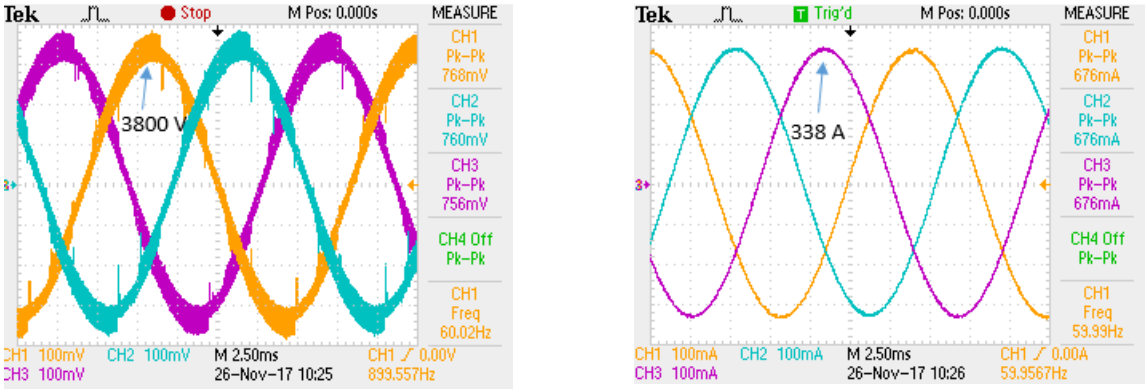


Figure. 69. Case 3: Inverter currents and PCC voltages

6.3.2. Results from eHS Scope:

6.3.2.1. Magnitude of voltage vector

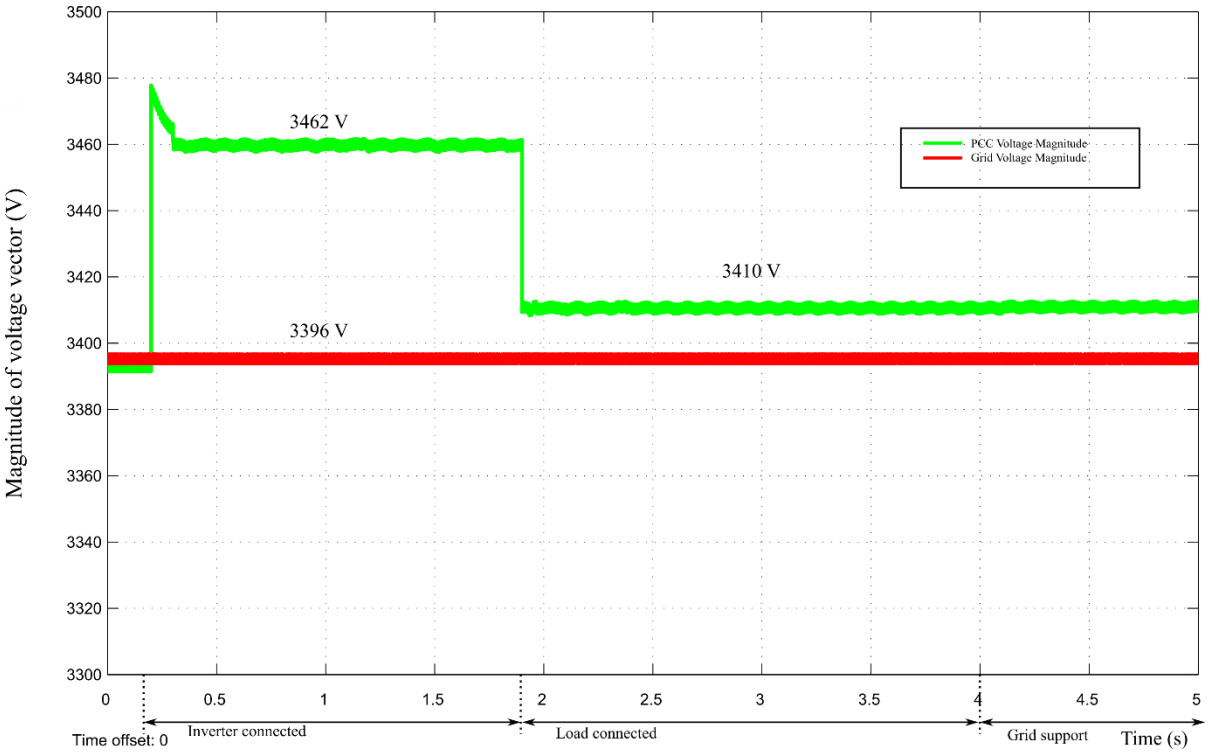


Figure. 70. PCC Voltage Dip

6.3.2.2. Magnitude of current vector

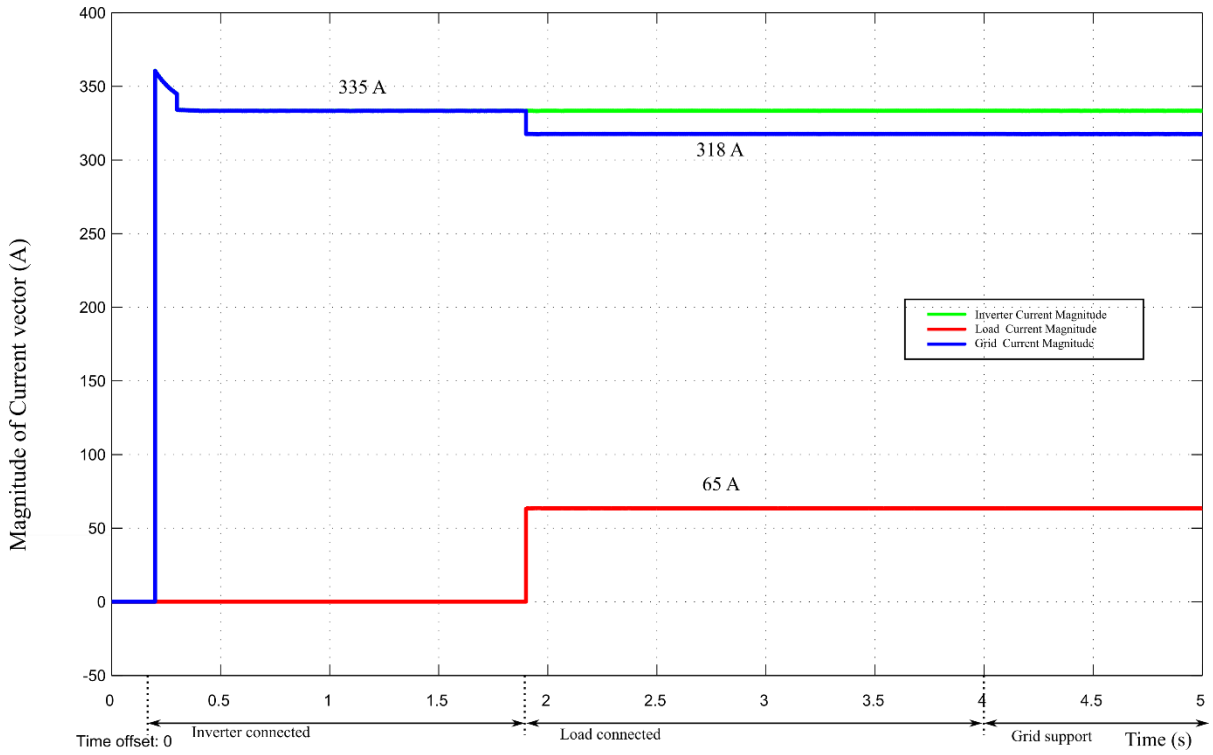


Figure. 71. Current vector magnitude

6.3.2.3. PLL output Vd, Vq

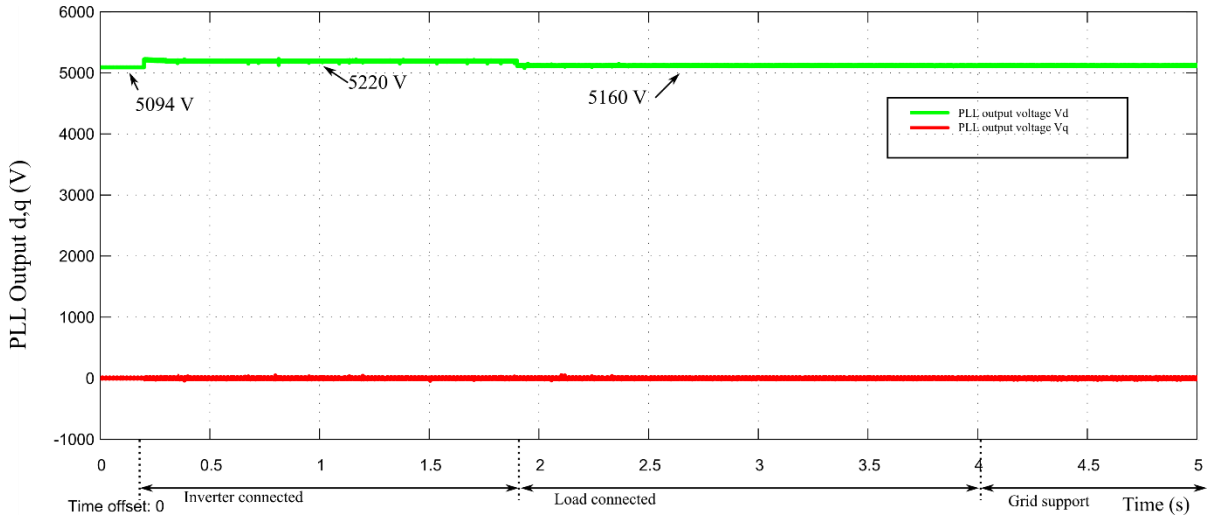


Figure. 72. Detection of Sag from PLL Output

6.3.2.4. Inverter current in d axis

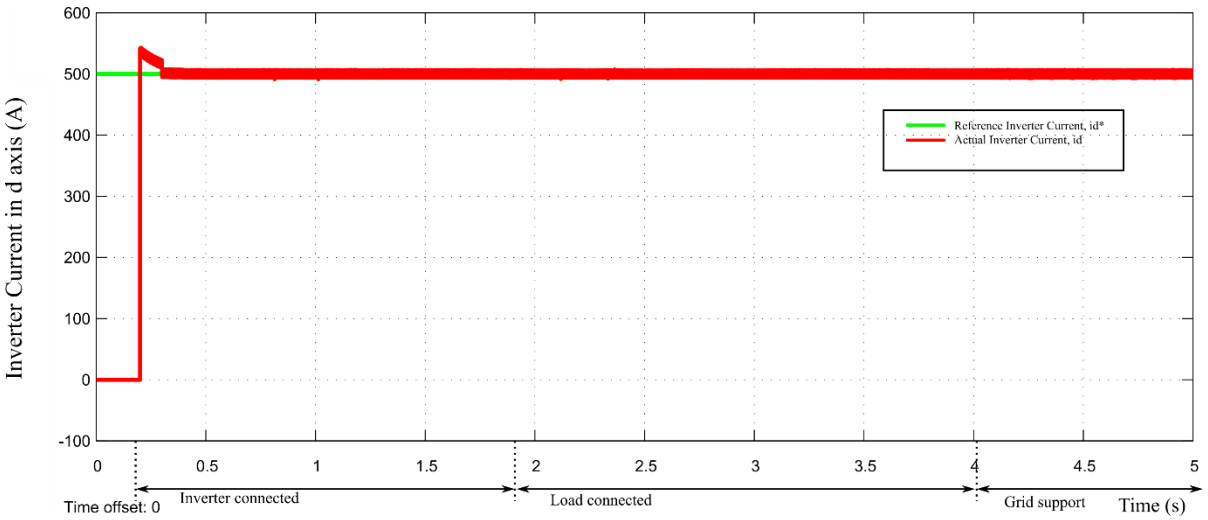


Figure. 73. Inverter Current in d axis

6.3.2.5. Inverter current in q axis

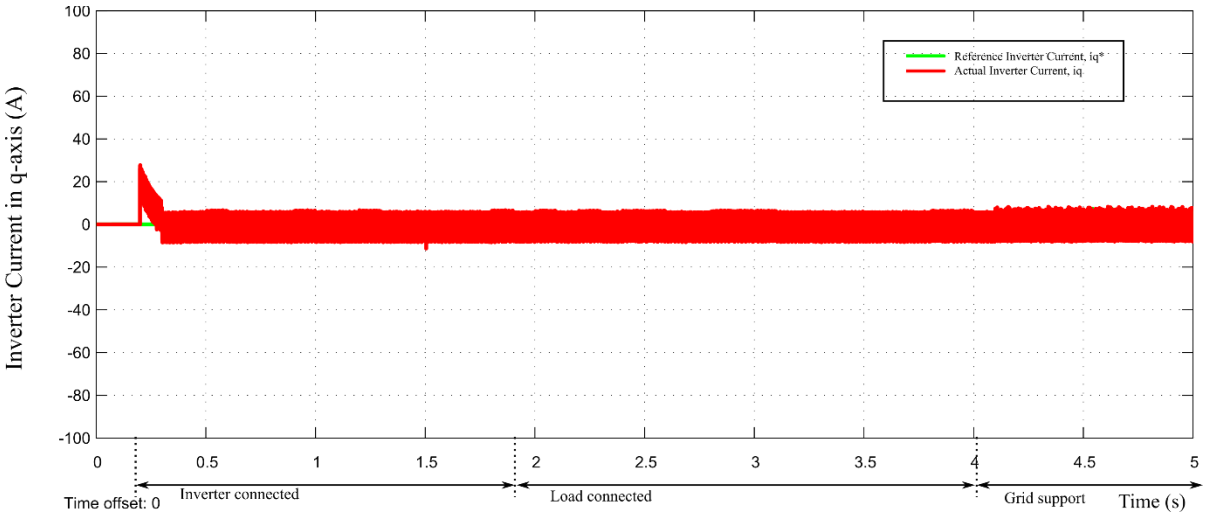


Figure. 74. No Change in q component of inverter current

6.3.2.6. Active Power P

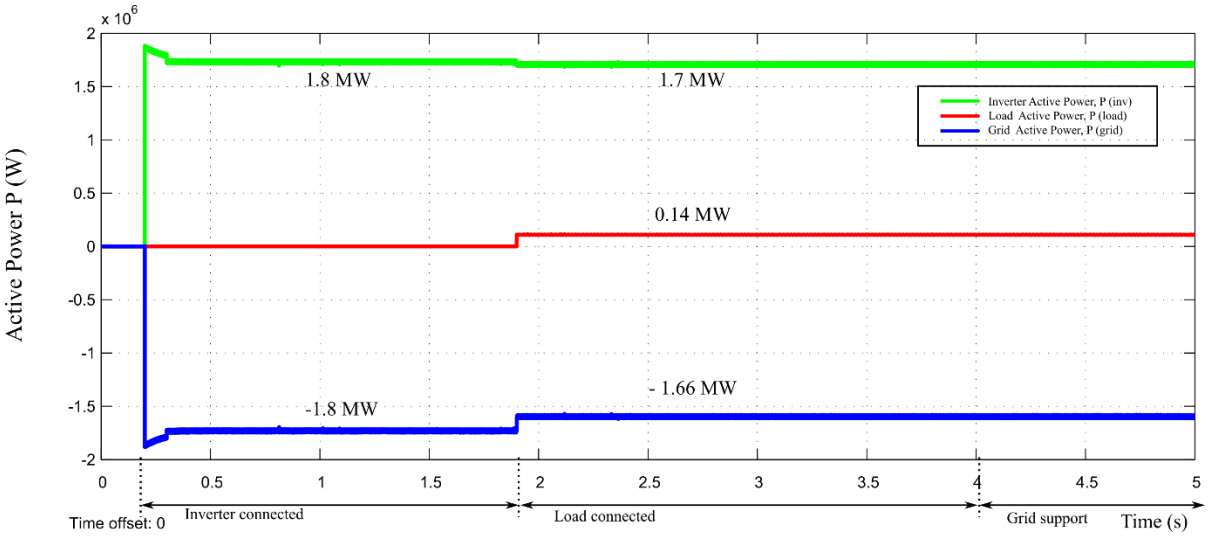


Figure. 75. Active power transitions

6.3.2.7. Reactive Power Q

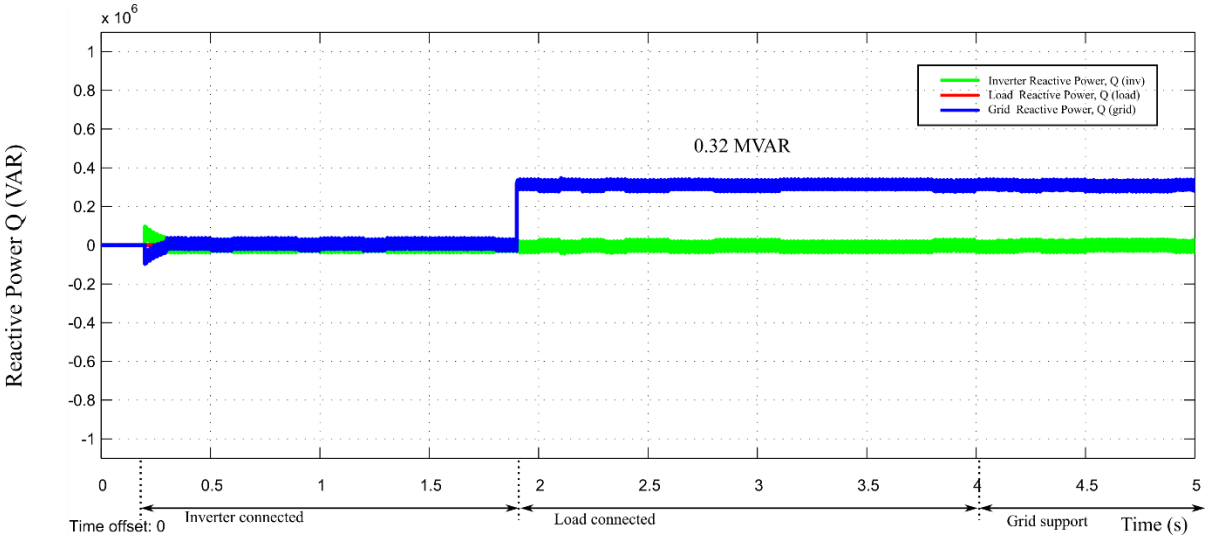


Figure. 76. Reactive power transitions

6.3.2.8. Apparent Power S

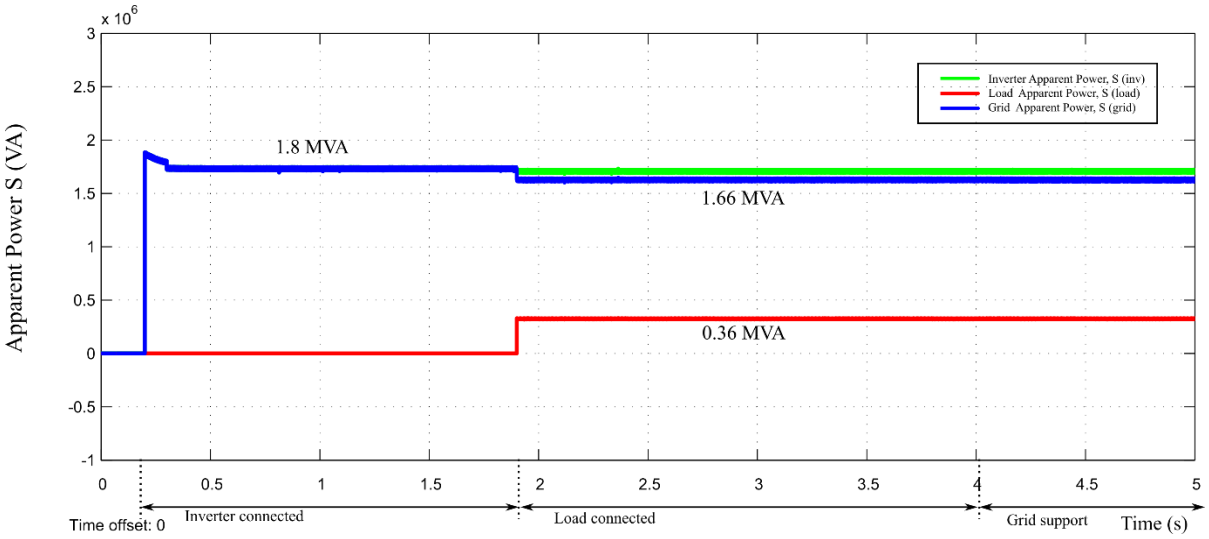


Figure. 77. Apparent power transitions

6.4. Case 4: Volt-VAR Control (VVC) when V > 1.08 p.u.

The inductive load modelled is of S = 0.36 MVA rating and p.f. 0.3 (C = 400 uF, R = 2.4 Ω) The waveforms captured on oscilloscope are scaled down in magnitude. The scaling factor for current and voltages are 0.01x and 0.001x respectively. In addition OPAL RT has an internal attenuation of 0.1 x.

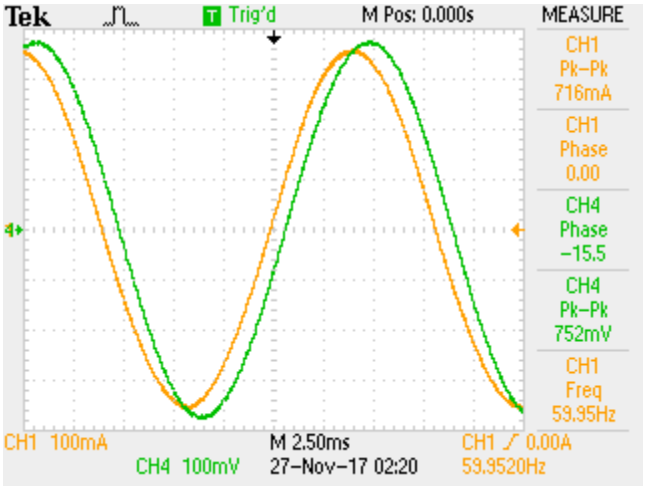


Figure. 78. Case 4: Phase Difference between 3 phase voltage & currents ~ (-15 °)

Negative phase represent that current is leading the voltage due to capacitive load

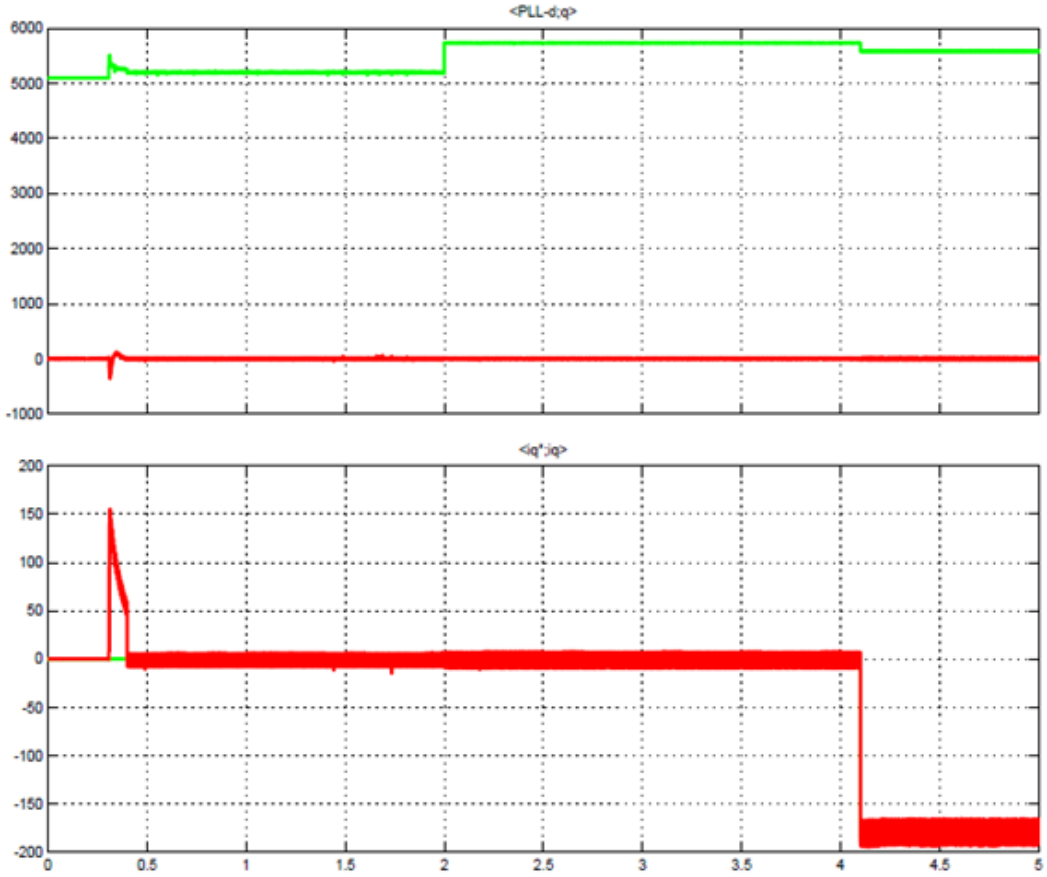


Figure. 79. PCC Voltage rise due to cap load and iq reference current is negative

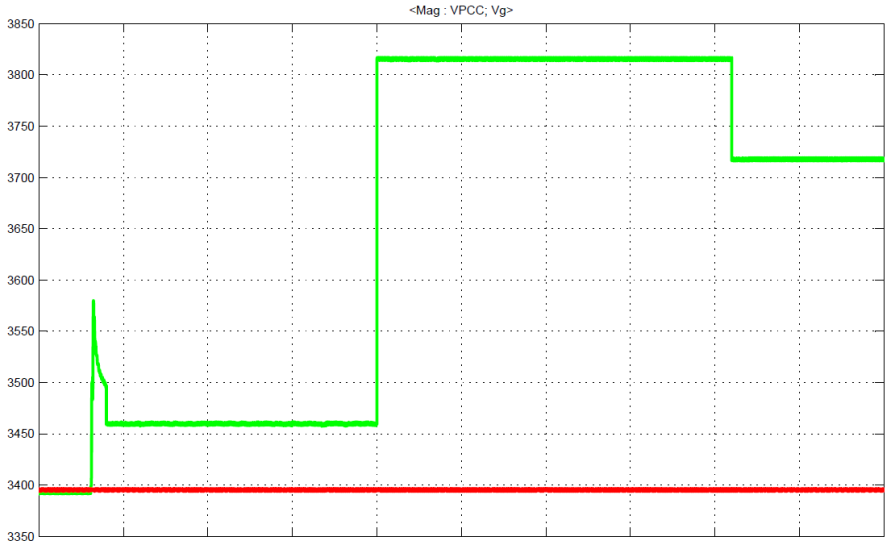


Figure. 80. Inverter absorbs reactive power during grid support, PCC voltage reduces

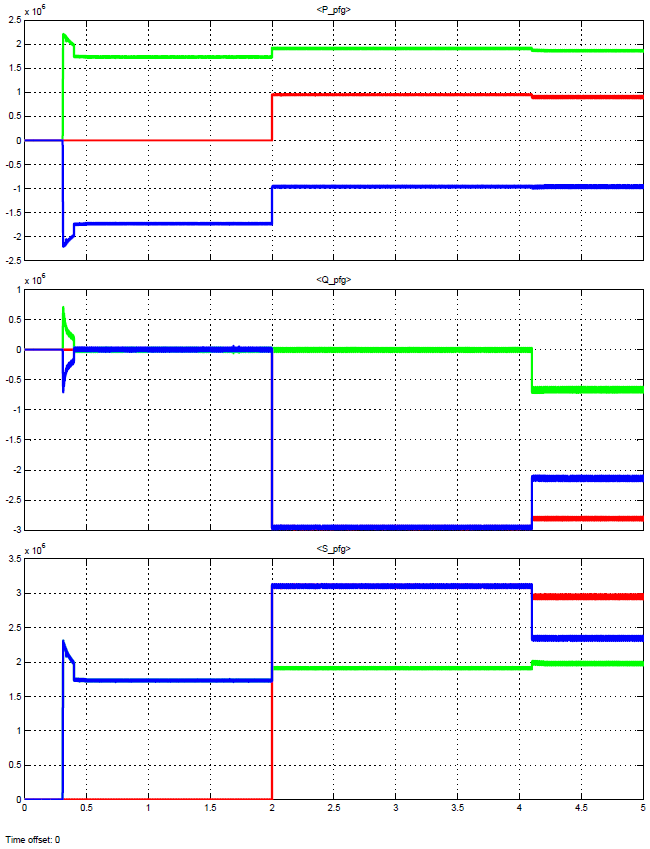


Figure. 81. Active, Reactive and Apparent power transitions

6.5. Case 5: Volt-Watt Control (VWC) when 1.07 < V < 1.10

Load parameters: (C = 400 uF, R = 2.4 Ω)

V1 =1.07 p.u.; V2 = 1.10 p.u.

P = P rated + Slope*(V- V1) = P = P rated + (-0.8/ 0.03)* (V- 1.07)

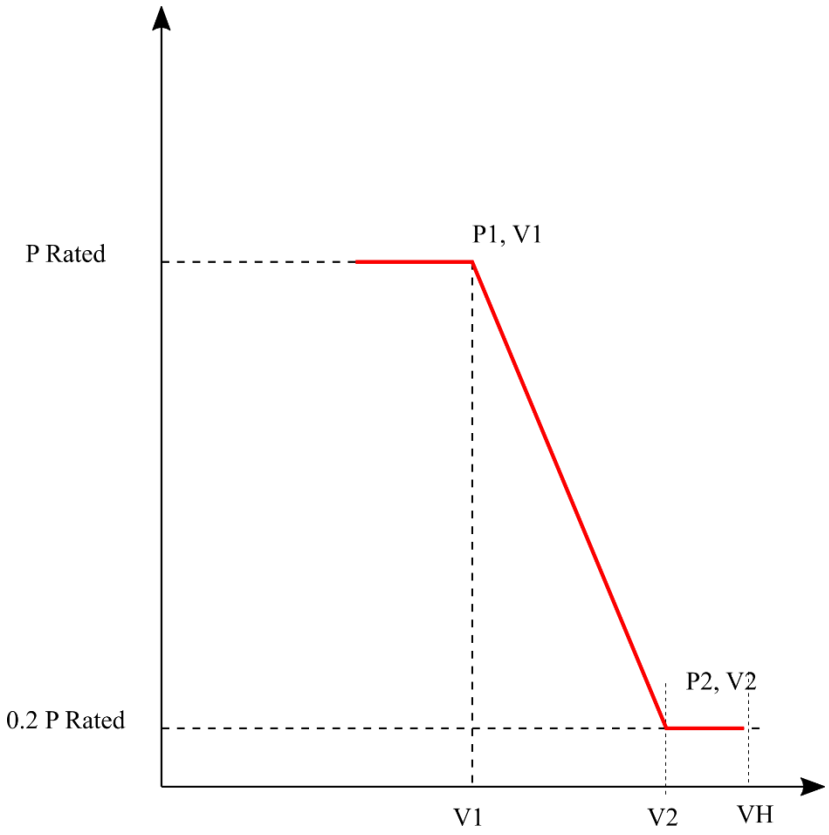


Figure. 82. Voltage-active power characteristics

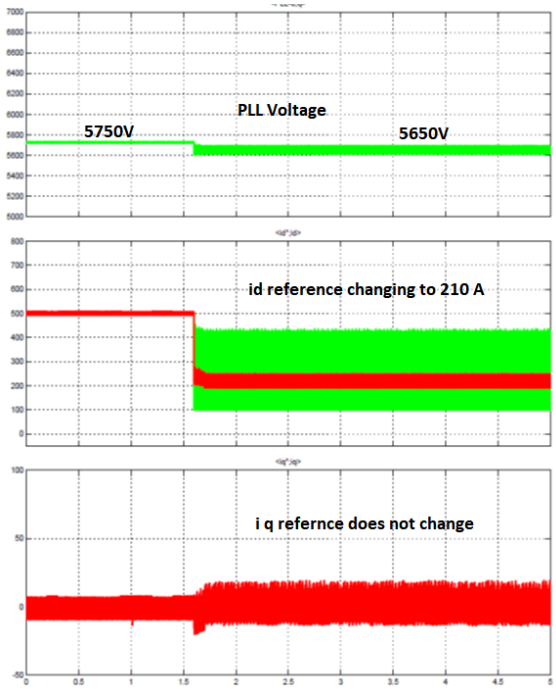


Figure. 83. Case 5: PLL Voltage change and id ref

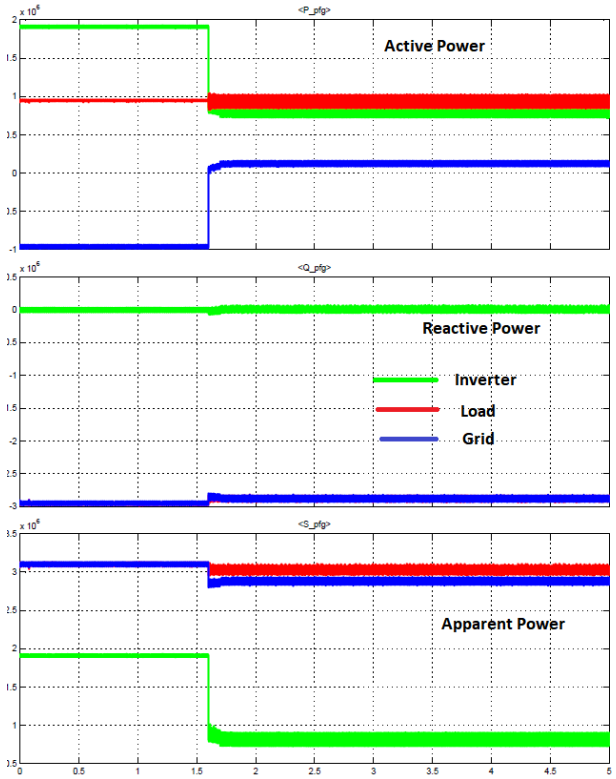


Figure. 84. Case 5: Active, Reactive and Apparent Power transitions

6.6. THD (Total harmonic distortion)

According to IEEE 519 standard requirements for THD, the harmonic current injection into the Area EPS at PCC must not exceed the percentages as specified in the table below.

6.6.1. Odd harmonics

Table 7: Odd harmonics.

Individual harmonic order h (odd)	$h < 11$	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 \leq h < 50$	Total rated current distortion
Required %	4.0	2.0	1.5	0.6	0.3	5.0
Resulted %	0.187	0.0635	0.0319	0.0326	0.00984	0.507

6.6.2. Even harmonics

Table 8: Even harmonics.

Individual harmonic order h (even)	$h = 2$	$h = 4$	$h = 6$
Required %	1.0	2.0	3.0
Resulted %	0.0012	0.0004	0.0027

We observe low order harmonics in the system due of the small variations in the DC bus voltage (ideally constant). These variations are propagated into the currents that is injected from the inverter and hence penetrate into the grid current. However, the percentage of these distortions observed as well within the allowable range provided by IEEE 519.

CHAPTER 7: Conclusion & Future Work

7.1. Performance Analysis:

7.1.1. Response to Disturbances

The response time is a critical parameters to decide the figure of merit of the controller action in events of any abnormal operation condition at the PCC. The detection is an instantaneous action, and only incorporates delays due to processor, followed by reference tracking by the current controller that responds within the range of its bandwidth. As seen in the results section, a typical reference tracking action takes about 2 ms to settle to the reference, which is almost two orders of magnitude less that the maximum response time requirement.
It must be noted that once more complex control function are added, both individual and as combination, the response time would get slower.

7.1.1.1. Detection Scheme

Slope method used for detection of the operating point with respect to the characteristics given in IEEE 1547 is observed to be a robust and accurate method to mathematically find the operating point with respect to nominal voltage at PCC. The robust nature comes from its ability to detect both under voltage and overvoltage based on a single detection logic, which uses a two stage validation in the logic for better performance and safety from unexpected mode change. This has also proven to work accurately when the control modes i.e. Volt-VAR and Volt-Watt are combined to take corrective action in both injecting/ absorbing reactive power and also controlling the active power flow at the same time.

7.1.2. Requirements Covered

The analysis covered major aspects discussed in latest advances in IEEE 1547 in terms of voltage –reactive power control, voltage – active power control, harmonic requirements, set points with adjustable range, combination of control modes as and when specified by the Area EPS and lays the fundamental test ground for evaluating performance in ride through functionality testing, fault detection and response time.

7.1.3. Support Features of Focus

7.1.3.1. Volt-VAR Control

The inverter connected to the grid is tested for a spectrum of major under- voltage and overvoltage points and the results were analyzed to be fairly accurate with the action specified in the IEEE 1547 section of voltage – reactive power control. Also, the seamless detection strategy makes possible a smooth detection over the piecewise linear Q-V characteristics to maintain accurate update of the set point reference. However, this is limited by the sensitivity of the detection logic.

7.1.3.2. Volt-Watt Control

For some specific cases highlighted in the standard, over voltage tests were conducted for both an independent mode operation and combinational mode operation. Here a similar approach to Volt-VAR is used with the only difference being that the logic updated only d component of the inverter current responsible for control the active power injected into the grid. The active power injection is not applicable for this system.

7.2.Conclusion

7.2.1. Effects of Grid Support

It is observed that the control modes have been tested and their performance in terms of providing grid support in occurrences of under voltage or overvoltage, has been demonstrated to be fairly accurate base on the capacity. One concern it that depending on the load, the DER may be insufficient in capacity to bring back the normal operation of the PCC voltage. However, this shows the capability of a DER for a minimum grid support according to requirements from IEE 1547. This can be scaled up to higher percentages to the extent to rated capacity of the DER, while taking other factors into consideration. Also, exploring other mutually exclusive modes of control such as constant power factor mode or the fixed reactive power mode could be a better option to extract full capability for reactive power compensation, however that will be limited in terms of range of operability.

7.2.1.1. Advantages:

Some issues in interconnection of DER with EPS are its capability to inject and absorb reactive power as required by the EPS at the PCC. The test cases have covered the entire range of voltage disturbances at the PCC and evaluated the function of grid support to be able to detect and take action as necessary. Also, this takes advantage of the de-coupled nature of active and reactive components of power, hence regulating voltage function becomes an independent function of active and reactive power as the modes are independently operated. The Volt-VAR and Volt-Watt modes are discussed and implemented using the digital controller. Another major advantage of this scheme is a seamless detection and corrective action as the control algorithm follows a well-defined hierarchy of steps before it changes the reference set points.

7.2.1.2. Challenges Faced

Implementation of FPGA based OPAL RT and generating binary code for eHS was difficult.

7.2.1.3. Limitations

This methodology comes with some limitation on scope for a more comprehensive architecture, there are other factors that could be incorporated using this template and building on top of this. Some of the issues not covered in this work include cases of unbalanced sag and swell conditions. The PLL design would require little modification for it to not only detect the magnitude of the voltage, but also accurately determine unbalanced condition that would introduce second order harmonics. Also, this scheme takes has indirect control on the power flow at the PCC node using the measurements of three phase quantities which is a critical region for mode errors. This could be improved by introducing a power loop that is slower but could provide more accurate calculations of the new set point of power references I the system. Another limitation is in regard to the range of PCC sag or swell cases. Currently, this work has been focused on cases where the sag or swell is a resultant of a comparable load getting connected. This idea can be extended for fault conditions. Also, detection of islanding and testing anti-islanding scenarios is not covered as part of this work.

7.3. Future Work

7.3.1. Fault testing and ride thorough cases

7.3.2. Islanding issues

Since grid support function are introduced to support the grid during voltage and frequency disturbances, these could also affect islanding detection. It is suggested that anti-islanding methods with grid support would have impacts on run – on times.

7.3.3. Frequency variations

Testing grid support functions for frequency variations under abnormal grid conditions

7.3.4. Expand network to multiple DER and load configuration

7.3.5. Unbalanced conditions at PCC

Advanced control algorithm for PLL detection and current control. Proposing characteristic curve and regulation scheme for single phase sag/ swell.

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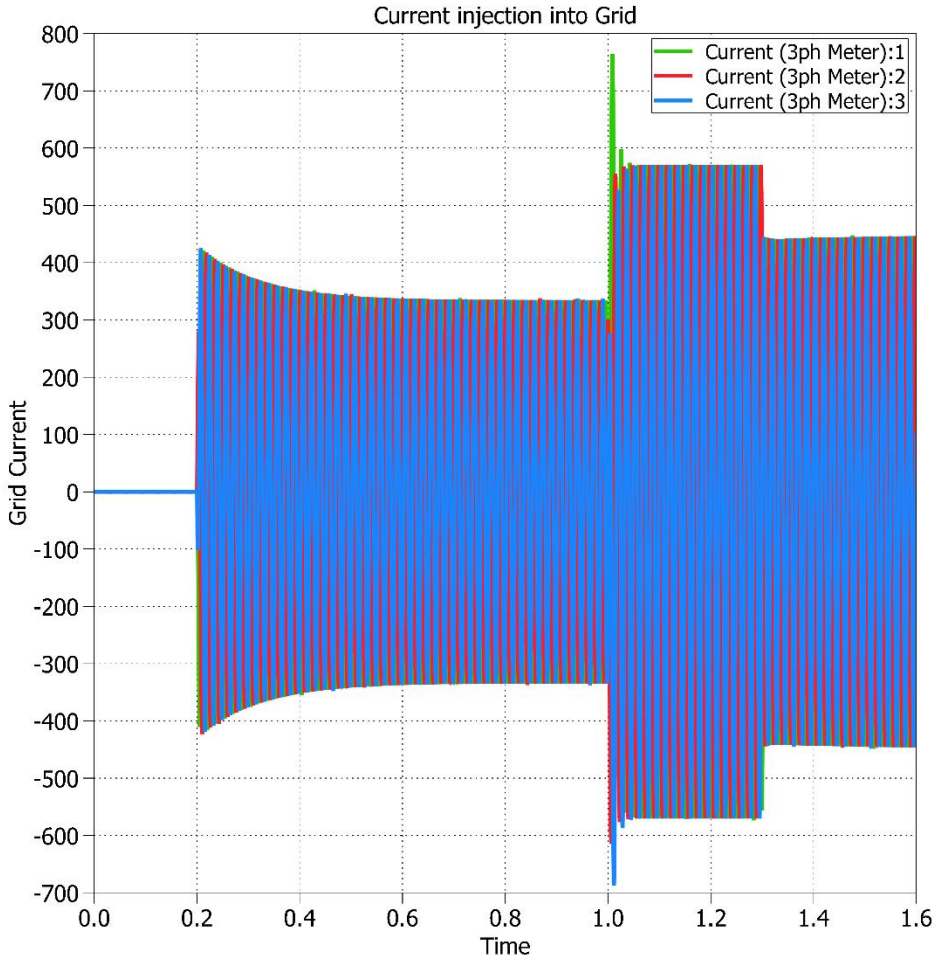
APPENDICES

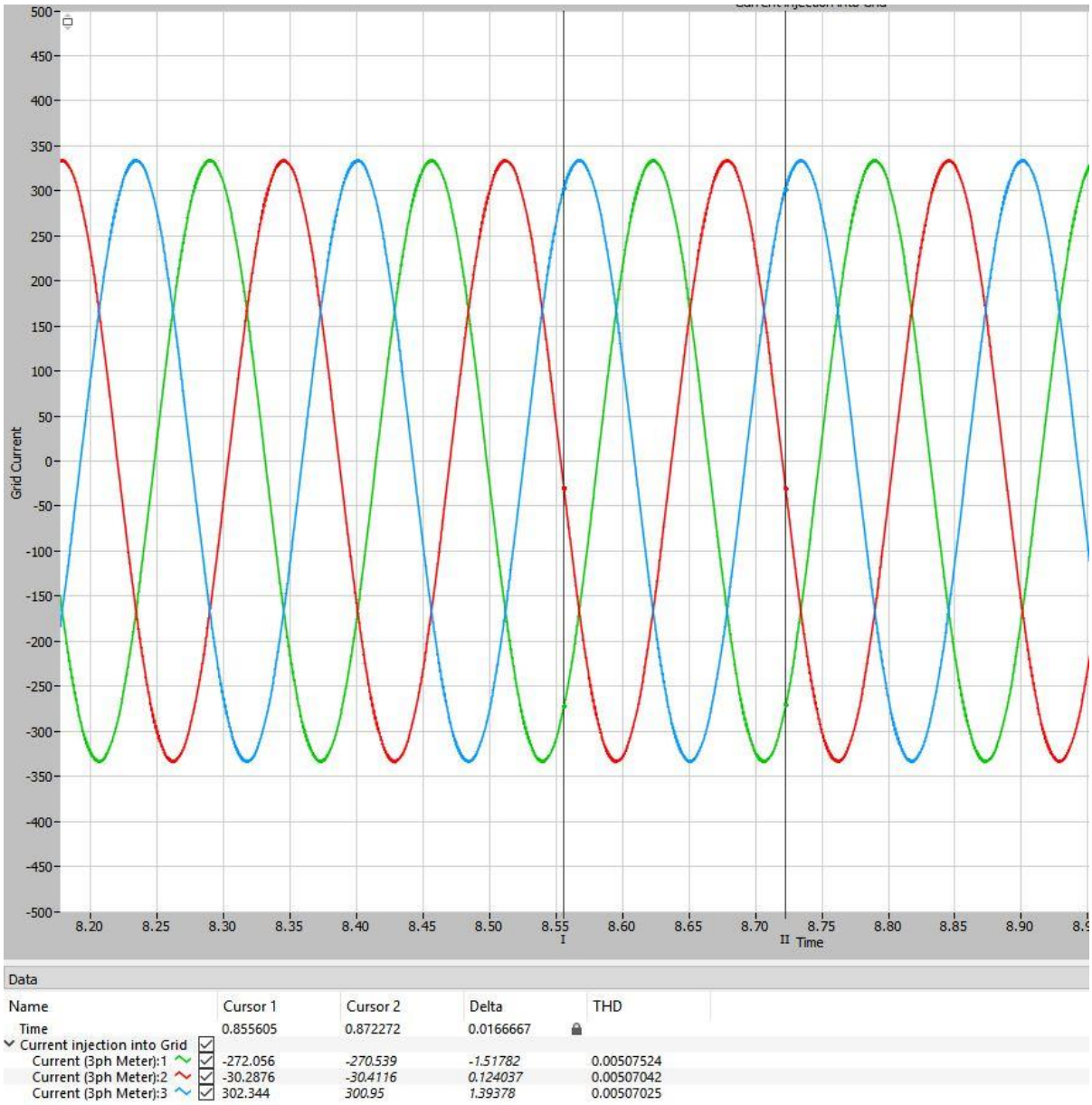
Appendix A

THD of 3 phase grid currents measured from PLECS

Grid Current

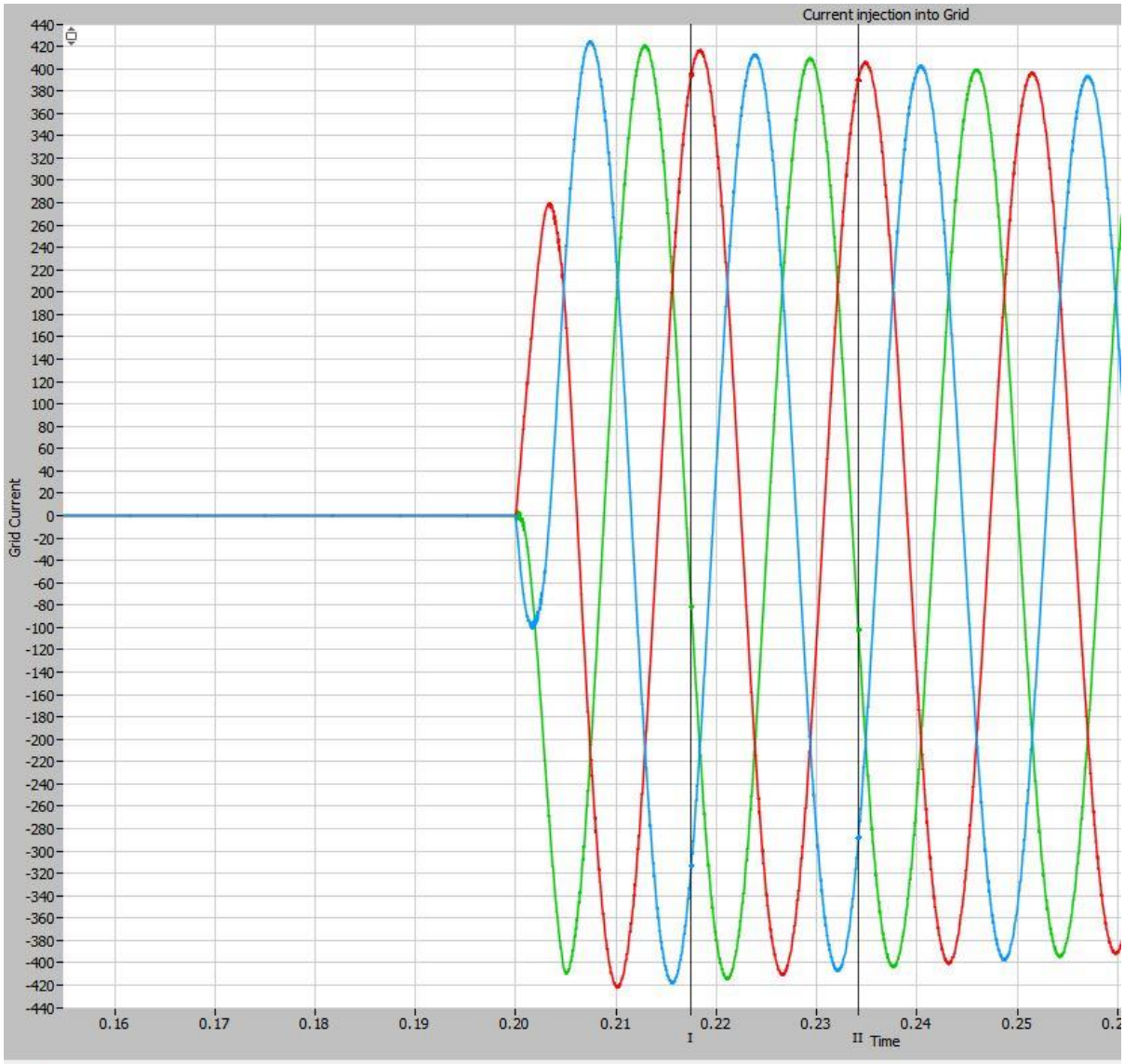


Inverter Mode:



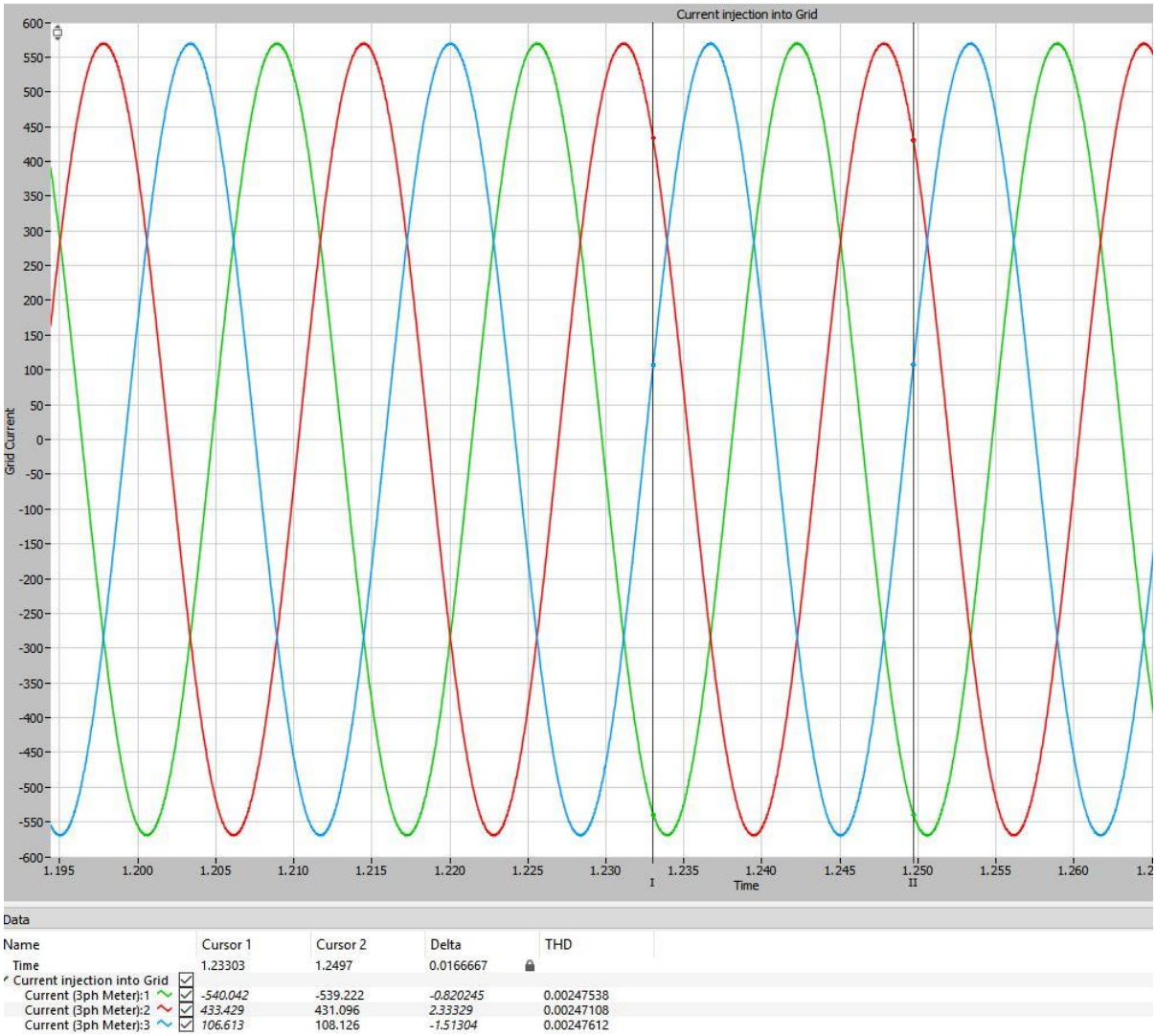
THD in grid current during steady state operation of the inverter is 0.5 % < 5%.

Inverter Start THD



THD in grid current during start-up operation of the inverter is 1.7 % < 5%.

Load connected – THD

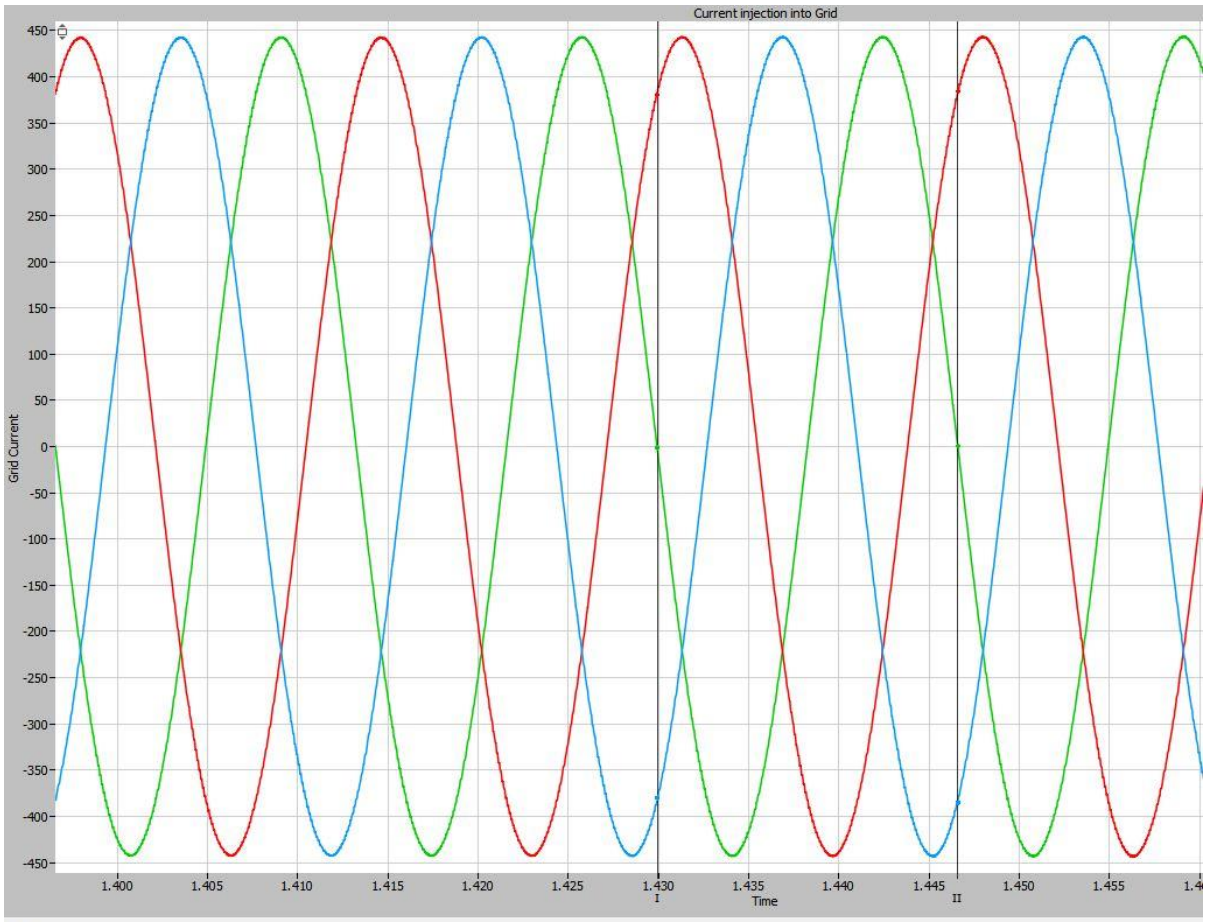


Data

Name	Cursor 1	Cursor 2	Delta	THD
Time	1.23303	1.2497	0.0166667	
Current injection into Grid				
Current (3ph Meter):1	*-540.042*	-539.222	*-0.820245*	0.00247538
Current (3ph Meter):2	*433.429*	431.096	*2.33329*	0.00247108
Current (3ph Meter):3	*106.613*	108.126	*-1.51304*	0.00247612

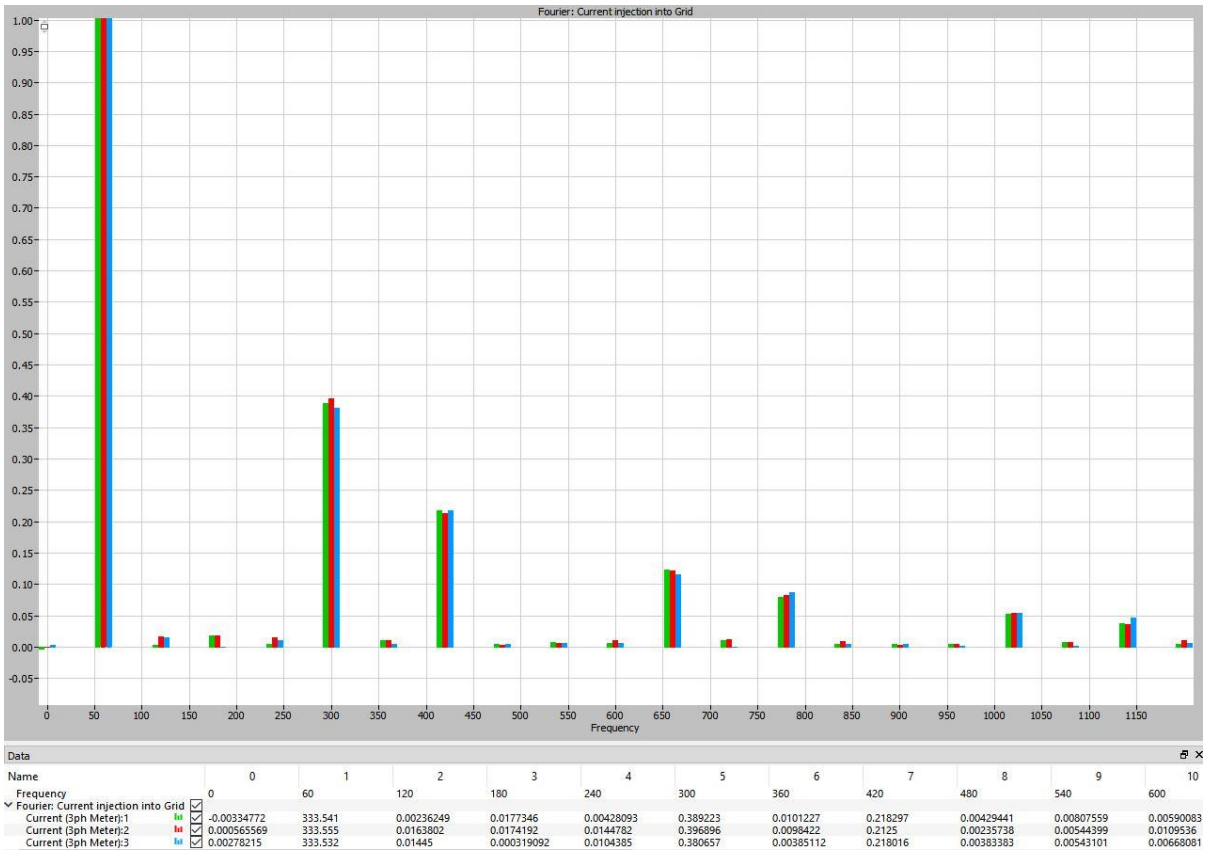
THD in grid current during load connection operation of the inverter is 0.24 % < 5%.

Grid Support – THD



THD in grid current during grid support operation of the inverter is 0.37 % < 5%.

Individual Harmonic content



Name	0	1	2	3	4	5	6	7	8	9	10
Frequency	0	60	120	180	240	300	360	420	480	540	600
Fourier: Current injection into Grid											
Current (3ph Meter):1	-0.00334772	333.541	0.00236249	0.0177346	0.00428093	0.389223	0.0101227	0.218297	0.00429441	0.00807559	0.00590083
Current (3ph Meter):2	0.000565569	333.555	0.0163802	0.0174192	0.0144782	0.396896	0.0098422	0.2125	0.00235738	0.00544399	0.0109536
Current (3ph Meter):3	0.00278215	333.532	0.01445	0.000319092	0.0104385	0.380657	0.00385112	0.218016	0.00383383	0.00543101	0.00668081

Individual harmonic components with % distortion and contribution to THD (well within limits)