ABSTRACT

NEGI, ABHAY. Two-stage Active Gate driver for SiC MOSFET. (Under the direction of Dr. Subhashish Bhattacharya).

Wide-band gap devices have rejuvenated the research in field of power electronics due to their superior properties over Silicon (Si) such as low on-resistance, high breakdown voltage, low switching losses and high temperature operation. However, SiC MOSFETs and GaN devices pose varied challenges due to high dv/dt and di/dt switching which creates issues related EMI, common mode current, high voltage overshoot, cross-talk, etc.

In phase-leg configuration, due to high turn-on dv/dt of SiC MOSFET, a positive spurious voltage is induced on the gate to source voltage (V_{gs}) of the complementary MOSFET. This reduces signal to noise margin on the V_{gs} of the complementary MOSFET making it susceptible to spurious turn-on in the phase-leg. This can be reduced by using higher turn-on gate resistance for lower dv/dt but it will lead to higher switching loss. This thesis explores the two-stage turn-on active gating for SiC MOSFETs to control turn-on dv/dt and di/dt independently. A two-stage active gate driver is designed which uses lower gate resistance in first stage to increase rate of current rise and higher gate resistance in second stage for lower turn-on dv/dt. A low-inductance DC bus PCB is designed to minimize voltage overshoots and ringing associated with high loop inductance. Switching losses are measured with and without active gating by double-pulse testing of 1200V/ 300A ROHM SiC half-bridge module BSM300D12P2E001 for comparison.

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Two-stage Active Gate Driver for SiC MOSFET

by
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DEDICATION

To Mummy, Papa & Amma.

BIOGRAPHY

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CHAPTER 1

1 Introduction

Silicon Carbide (SiC) MOSFETs allow power electronics engineers to achieve higher efficiency due to lower switching loss and conduction loss [1]. SiC devices have rejuvenated the research in power electronics with their superior properties over the industry workhorse Silicon (Si) devices [2] [3][4]. As compared to Si, SiC has three times the band gap, ten times the dielectric breakdown field strength and three times the thermal conductivity. This enables SiC device to have lower switching loss, higher temperature operation and lower on-resistance. Lower switching loss enables higher frequency operation which leads to smaller size of passives components such as magnetics and capacitor and effectively reduce the converter size. SiC MOSFETs are commercially available in 900V to 1700V range and are expected to replace Si devices completely in future for industrial application once protection and reliability related issues are addressed [5]. SiC MOSFETs pose a lot of challenges due to high dv/dt and di/dt switching such as EMI, common mode currents, high voltage overshoots, cross-talk, etc. These issues can be mitigated by proper design of gate drivers.

For MOSFETs, voltage source based gate drivers are used. For designing a gate drive for SiC MOSFET, the basic design steps remain the same as that for Si devices. However, the coupling capacitance associated with power supply should be of order of low pico-Farads to minimize common mode currents and optocouplers should have high common-mode transient immunity (CMTI). To drive SiC MOSFET at very low gate resistances for lower switching loss, the gate loop inductance should be optimized to ensure no ringing during switching transients.

1.1 Motivation

The switching losses of SiC MOSFET are a function of the gate resistance for a given switching voltage and current. For lower gate resistance, the switching losses are lower but the dv/dt is higher. In phase leg configuration shown in Fig 1-1, during turn-on of a SiC MOSFET, the rate of voltage fall across the device is equal to rate of voltage rise across the complementary

MOSFET. The dv/dt experienced by the complementary device results in current flow through miller-capacitor which induces a positive spurious voltage on the gate to source voltage of complementary device [6],[7], [8].

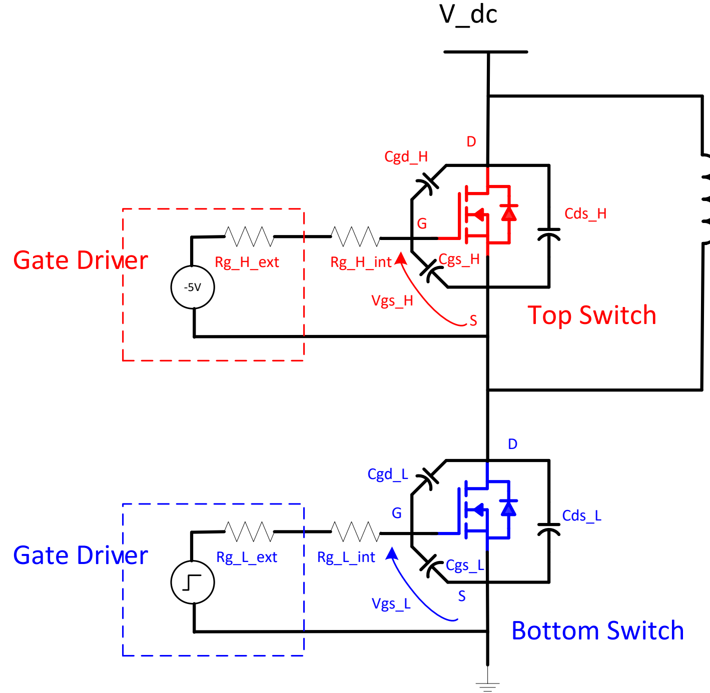

Figure 1-1 SiC MOSFET in phase leg configuration

In Fig 1-2, the cross-talk associated with high turn-on dv/dt of SiC MOSFET is shown using spice models for device ROHM SiC Module BSM300D12P2E001[10] . The peak value of the spurious gate voltage [6] can be written as

$$V_{gs_H(\max)} = \frac{dv}{dt} \times R_{g_H} \times C_{gd_H} \times \left(1 - e^{\frac{-V_dc}{\frac{dv}{dt} \times C_{iss_H} \times R_{g_H}}}\right) \quad (1.1)$$

where $$R_{g_H} = R_{g_H_int} + R_{g_H_ext} \quad (1.2)$$

and $$C_{iss_H} = C_{gs_H} + C_{gd_H} \quad (1.3)$$

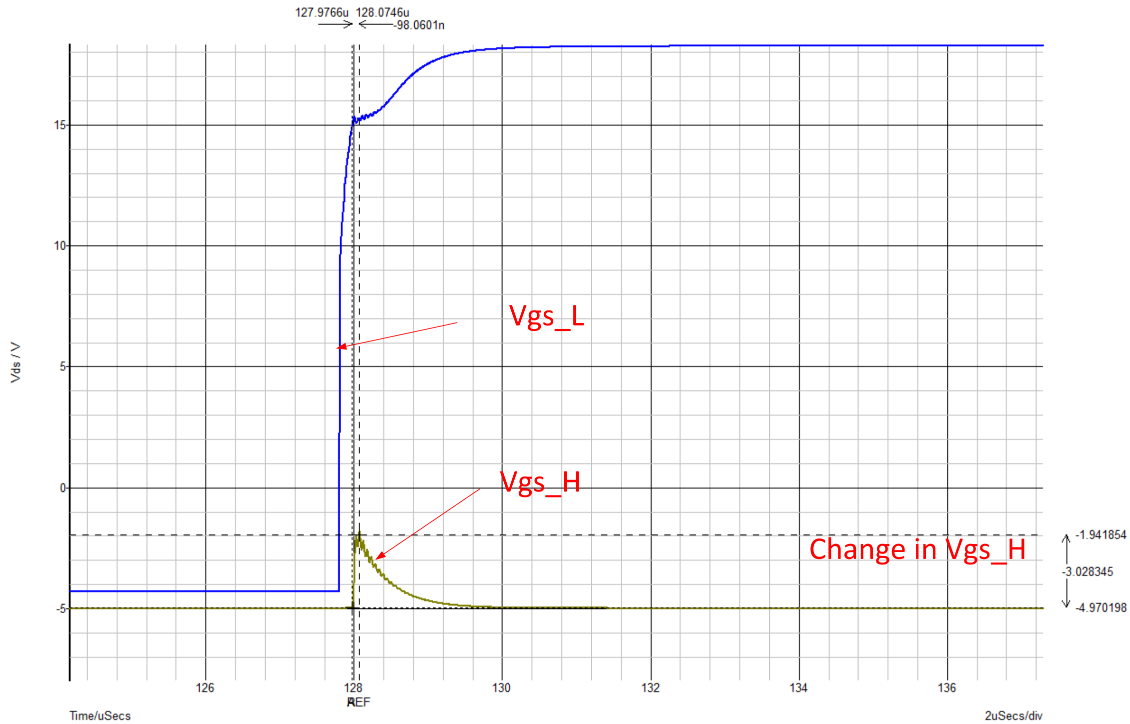

Figure 1-2 Cross-talk between SiC MOSFETs in phase-leg due to high turn-on dv/dt

The positive induced voltage reduces signal to noise margin on the V_{gs} of the complementary MOSFET making it susceptible to spurious turn-on in the phase-leg. In worst case scenario, the V_{gs} may cross the threshold voltage leading to shoot-through which can be detrimental to the device. This can be reduced by lowering dv/dt by using higher turn-on gate resistance but it will lead to higher switching loss. An active gate driver can be used to reduce turn-on losses and mitigate spurious induced voltage to improve reliability.

This thesis explores the turn-on active gating for SiC MOSFETs to independently control turn-on di/dt and dv/dt . A two-stage active gate driver is designed which uses lower gate resistance in first stage to increase rate of current rise and higher gate resistance in second stage for lower turn-on dv/dt.

1.2 Outline of Thesis

The thesis is organized in the following chapters:

Chapter 2: Design consideration for gate driver for SiC MOSFET are described. Details of opto-coupler along with protection feature used are explained.

Chapter 3: Cross-talk issue associated with SiC MOSFET in phase-leg is explained. Details of 2-stage active gate driver for independent control of dv/dt and di/dt to mitigate cross-talk are explained.

Chapter 4: Design of DC bus PCB for low loop inductance is discussed. Double pulse testing method used for device characterization is explained. Capacitor bank sizing details and Ansys Q3D simulation results are provided.

Chapter 5: A 1200V /300A ROHM SiC Module BSM300D12P2E001 [9] has been characterized for switching loss and results are provided. Comparison for results with and without active gating has been provided.

Chapter 6: Finally, conclusions are drawn and possible suggestions for future work are provided.

CHAPTER 2

2 Gate Driver Design

A gate driver is required to drive a MOSFET and driving voltage is decided based on recommended values provided by the device manufacturer. For SiC MOSFETs, the turn-on V_{gs} of 18-20V is generally applied while for turn off, negative V_{gs} of -5V is used.

2.1 Switching Characteristics of MOSFET

To understand the switching characteristics of MOSFET, consider a diode-clamped inductive load circuit as shown in Fig 2-1. When the MOSFET is turned on by applying positive gate-source voltage, inductor current increases linearly during on-time. On reaching a desired current value, the device is turned off by applying negative V_{gs}.

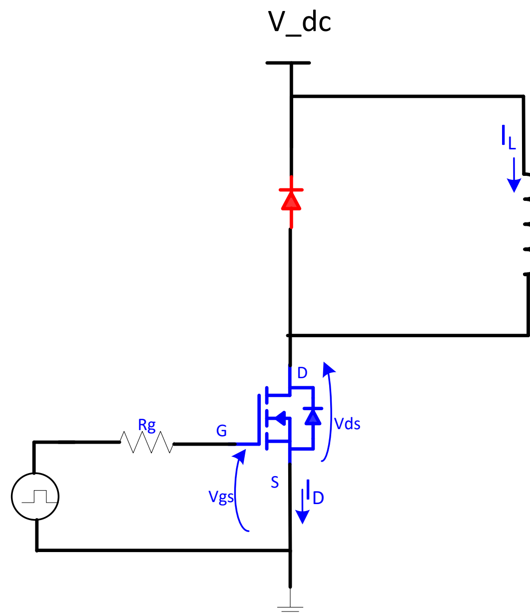

Figure 2-1 Diode- clamped inductive load circuit

Fig 2-2 shows the turn-on switching characteristics of MOSFET. Before the turn-on of MOSFET, it is assumed that the free-wheeling diode is carrying all the load current. From time 0 to t_1, both C_{gd} and C_{gs} are charged and the gate voltage reaches the threshold voltage. During this time the device is not switched on and the time period is known as turn-on delay time.

Once the threshold voltage is crossed, the channel starts conducting and the current starts rising and reaches maximum load current from time t_1 to t_2. During this time, the drain voltage remains high at the DC bus voltage since diode cannot block any voltage until all load current is transferred to the MOSFET [1].

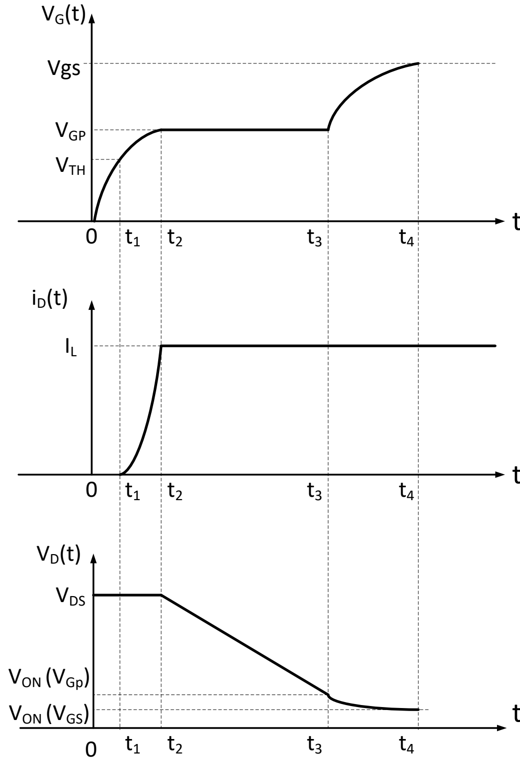

Figure 2-2 Turn-on Waveforms for MOSFET

After time interval t_2, the drain voltage starts to decrease while the drain current remains constant. The gate voltage remains constant at gate plateau voltage or Miller plateau voltage during time interval t_2 to t_3. The gate current charges the miller capacitance C_{gd} during this time leading to reduction in gate-drain voltage. At t_3, the drain voltage becomes equal to on-stage voltage corresponding to plateau gate bias voltage [1] .

C_{gd} changes with V_{ds} i.e. at lower V_{ds}, C_{gd} is high and at higher V_{ds}, C_{gd} is low. After t_3, C_{gd} is high due to small on-state voltage and hence, gate voltage rises with lower rate as compared to that during 0-t_2 and reaches the gate supply voltage. Ideal case has been considered here. In

practical circuits, there is current overshoot due to reverse recovery of the diode and di/dt. Also, the voltage drops by 'L * di/dt' during current rise time where L is the loop inductance.

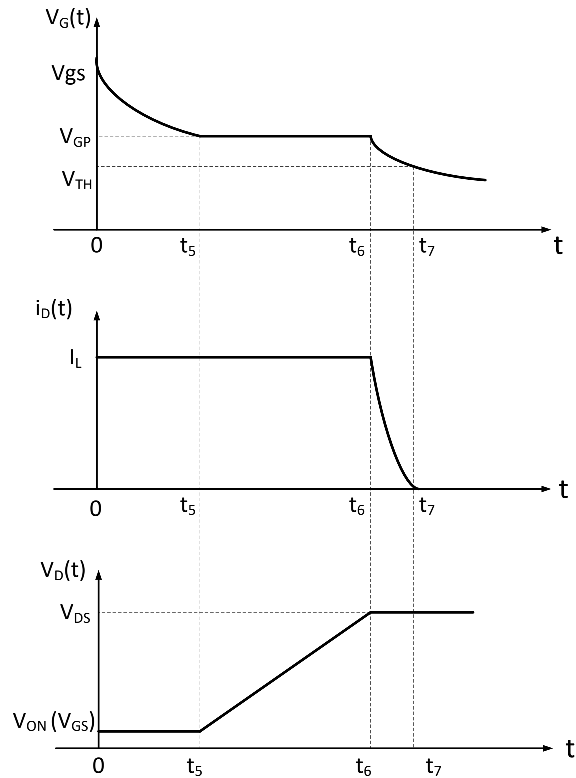

Figure 2-3 Turn-off Waveforms for MOSFET

Fig 2-3 shows the turn-off switching characteristics of a MOSFET. Before turn-off, the MOSFET is carrying all the load current and switching it off transfers all current back to the free-wheeling diode. When the MOSFET is turned off by applying zero or negative gate voltage, Vgs gradually reduces to the gate plateau voltage. However, there is no change in drain current or drain voltage during time interval 0-t5 which is known as turn-off delay time. [1]

After time t_5, the drain voltage increases gradually while current remains constant. During time interval t_5-t_6, gate current is discharging the miller capacitance and the gate to source voltage remains constant. The voltage reaches a peak voltage V_{ds} at time t_6. At this instant, the drain voltage becomes equal to dc supply voltage plus one diode drop which forward biases the freewheeling diode.

After t_6, the current starts decreasing gradually and both C_{gd} and C_{gs} are discharged leading to exponentially fall in V_{gs}. At time t_7, V_{gs} drops below threshold voltage and keeps decreasing till it reaches zero or negative gate voltage (if applied).[1] In practical circuits, there is voltage overshoot equal to 'L*di/dt' at time t_6. Since, SiC MOSFETs can switch at very high di/dt, so loop inductance should be very low to avoid voltage overshoot. Higher loop inductance will lead to high voltage overshoot which will reduce the safety margin and shall require voltage derating of the devices.

The switching loss of a device are a function of gate resistance used and the gate-source voltage applied for a given switching voltage and current. For higher V_{gs}, higher gate current will be available which shall create channel faster and turn-on the device faster and will have lower turn-on loss. Similarly for turn-off, using negative voltage removes the majority carries faster leading to faster turn-off.

The gate resistance can be used to control the time spans t_1-t_2 and t_2-t_3, A lower turn-on gate resistance will reduce the RC time constants corresponding to time span t_1-t_2 resulting in faster rise of current and will also reduce time span t_2-t_3 leading to higher dv/dt. This will effectively reduce the area under product of V-I curves leading to lower turn-on losses. On the contrary, a higher turn-on gate resistance will lead to lower di/dt, dv/dt and higher switching losses. Similarly for turn-off, the time spans t_5-t_6 and t_6-t_7 can be controlled using gate resistance for desired dv/dt , di/dt and switching loss. Lower turn-off resistance will lead to higher dv/dt and di/dt and lower turn-off losses while higher turn-off gate resistance will result in lower dv/dt, di/dt and higher switching loss. It should be noted that there is no effect of C_{ds} on the V_{gs}.

2.2 Gate Driver Design Consideration

For designing a gate driver, first the device for which gate driver is being designed should be known to know the gate charge and voltage limits for V_{gs}. For this work, ROHM SiC Module 1200V 300A device BSM300D12P2E001 [9] has been used. Based on the device datasheet, the absolute maximum gate to source voltage is +22V/ -6V. The device can withstand surge voltages of +26V/ -10V for 300 ns.

The SiC MOSFETs have very fast rise times and fall times which leads to very high dv/dt and di/dt. Therefore, for selecting an optocoupler, the following parameters need to be considered:

a. Common-mode Transient Immunity (CMTI) – The CMTI of the optocoupler is an important parameter to ensure it can withstand high dv/dt switching. It should be higher than 50kV/µs and preferably 100kV/µs.
b. Peak output current - The peak source and sink currents are dependent upon the voltage swing of V_{gs} and the gate resistance used. If output current of the optocoupler is less than the calculated peak current, then current buffers need to be used.
c. Propagation delay – Low propagation delay is desired preferably less than 100 ns. In case, there is a fault which sends signal to pulse generator/ microcontroller to block the PWM, the output will change after the propagation delay of optocoupler (plus propagation delay of current buffer, if used).

The other design consideration for designing gate driver are:

2.2.1 Drive Power

The gate charge characteristics of the device is used to calculate the driving power for gate driver. Ideally gate charge should be calculated by integration of gate current but that requires access for measurement of gate current.

The drive power is calculated using gate charge, switching frequency and gate driver output voltage swing:

$$P_{drive} = Q_{Gate} \times f_{IN} \times \Delta V_{Gate} \tag{2.1}$$

As per datasheet, Q_{gate} = 1700 nC for 20V. If a Vgs of +20 V is considered for turn-on and -5 V for turn-off is considered, then ΔV_{gate} = 25V. For frequency of 20 kHz, ΔV_{gate} = 25 V and Q_{gate} of ~2000 nC, the drive power should be 1W. A power supply of 2W has been used for the gate driver.

2.2.2 Peak Output Current

The peak current is calculated based on the sum of external and internal gate resistance. In case Rg= 0.5 Ω is used with internal resistance of 1.6 Ω and ΔV_{gate} = 25 V, the peak current can be calculated using following relation:

$$I_{out_cal} = \frac{\Delta V_{gate}}{R_{gate_\min}} \tag{2.2}$$

I_{out_cal} is equal to 11.9 A.

However, due to presence of parasitic inductance, the peak current observed in the working circuit is 70% of $I_{out_cal.}$ [11]

$$I_{out_\max} \geq 0.7 \times I_{out_cal} \tag{2.3}$$

The gate driver should be selected taking into account reduction factor of 0.7. For above mentioned parameters, I_{out_max} is greater than to 8.33 A is required.

2.2.3 Minimum Gate resistance

The minimum gate resistance should be selected to ensure voltage overshoots on gate-source voltage is critically damped. For critically damped system or quality factor, Q< 0.5, the following relation can be used to calculate minimum gate resistance R_{gate_min}:

$$R_{gate_\min} \geq 2\sqrt{\frac{L_{gate}}{C_{iss}}} \tag{2.4}$$

where C_{iss} is the input capacitance of the SiC MOSFET and L_{gate} is the gate loop inductance. In case, ringing on gate is experienced at a given gate resistance, then it may be due to high gate loop inductance. Using higher gate resistance or reducing the length of gate-source connection twisted wire should damp out the oscillation.

2.2.4 Gate loop inductance

Gate loop inductance should be minimized with good layout. It can be cancelled by overlapping of forward path and return path of gate loop inductance over two layers. The effective loop inductance path starts from output of current buffer (or opto-coupler, if current buffer is not used). Most half-bridge modules provide Kelvin source connection which helps in minimizing the gate loop inductance as well as coupling of high di/dt currents into gate loop [12].

2.2.5 Signal Isolation Using Optical Transmitter & Receiver

An optical transmitter and receiver can be used to provide signal isolation. The long optical fiber can be used to ensure the function generator/ DSP board can be placed far off from the device under test(DUT) which will minimize EMI experienced due to fast switching transients.

2.2.6 Isolated power supply with low coupling capacitance

The power supply (DC/DC converter) should have with very low coupling capacitance (<= 10 pF) to minimize flow of C*dv/dt common mode currents into power supply. For 1200V and 1700V SiC MOSFETs, power supply with isolation of order of 5 kV DC/minute are commercially available. In case, customized isolated power supply is designed in-house, then the coupling capacitance for the isolation transformer should be verified using impedance analyzer. Suitable clearances and insulation should be provided to achieve desired galvanic isolation.

2.3 Optocoupler

Optocoupler IC TI ISO5852S [13] has been used for the gate driver. It has capacitive isolation of 5.7kV RMS and can withstand common mode transients upto 100 kV/us. Since SiC MOSFETs are associated with high dv/dt, CMTI is an important parameter for choosing an optocoupler. The IC also has propagation delay of 76-110 ns. Care should be taken so that ground for primary(input) and secondary (output) side are isolated.

Fig 2-4 shows a snapshot of circuit connection for Optocoupler IC TI ISO 5852S with bipolar output and Fig 2-5 shows the gate loop connections after current buffer. The bipolar output on secondary has been provided using bipolar output supply. For higher output current requirement, pnp / npn based totem pole or external current buffer IC can be used.

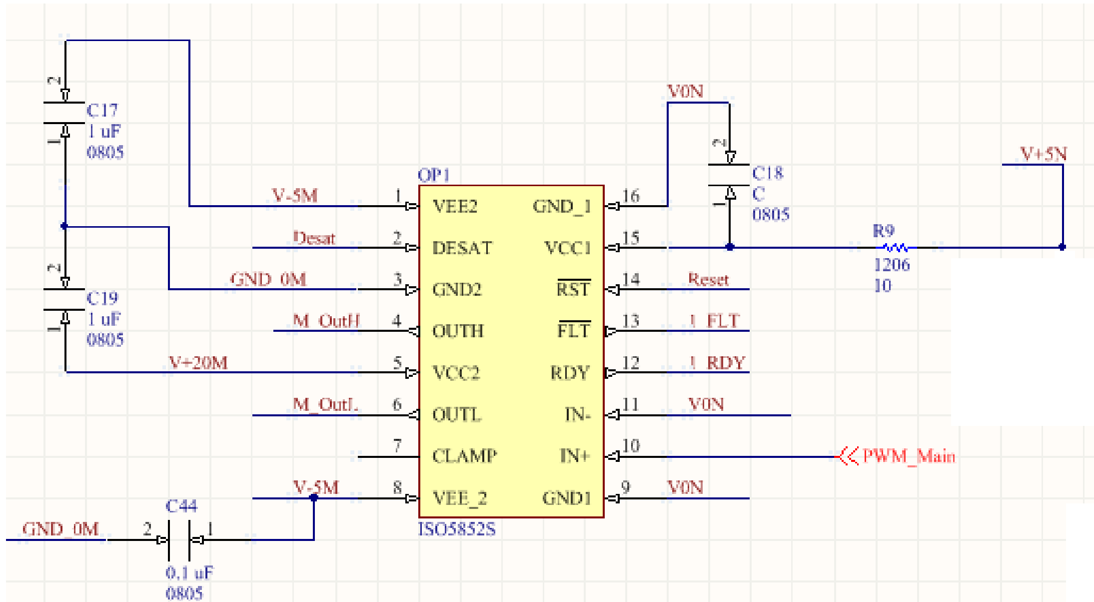

Figure 2-4 Schematic showing Optocoupler TI IC ISO5852S connections

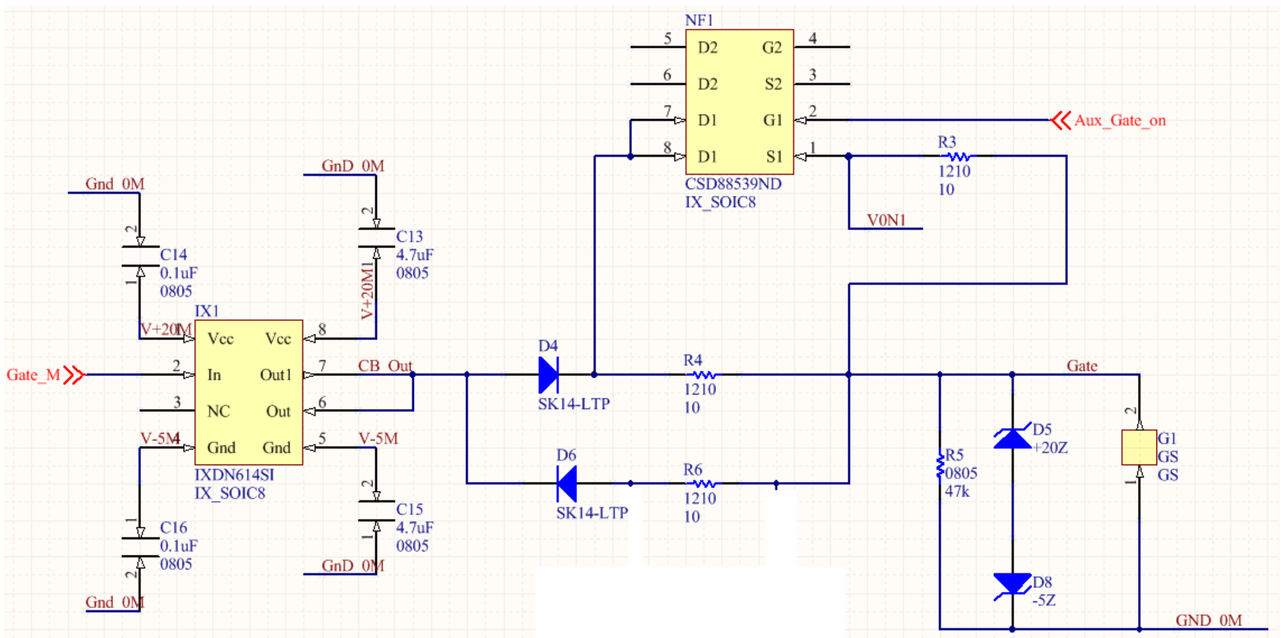

Figure 2-5 Schematic showing gate-loop connections after current buffer

As the output current of IC is 2.5 peak source and 5A peak sink, a current buffer IC IXDN 614 [17] has been used which can provide sink and source current of up to 14 A. Generally non-inverting current buffer ICs are used as Desat protection feature is not compatible with inverting current buffers. In the Fig 2-5, the effective gate resistance is defined after the current buffer and has been represented with Rg. The inductance path from current-buffer to gate-source terminals should be optimized to minimize gate loop inductance.

2.4 Short Circuit Protection (DESAT)

The DESAT protection feature of the optocoupler is used for short circuit protection. Desat feature is designed primarily for IGBTs for detection of transition from saturation region to active region. In MOSFETs, there is no clear transition between linear and saturation region. However, the VI curves provided in the datasheet for the SiC MOSFET can be used to define the V_{ds} at which protection gets triggered.

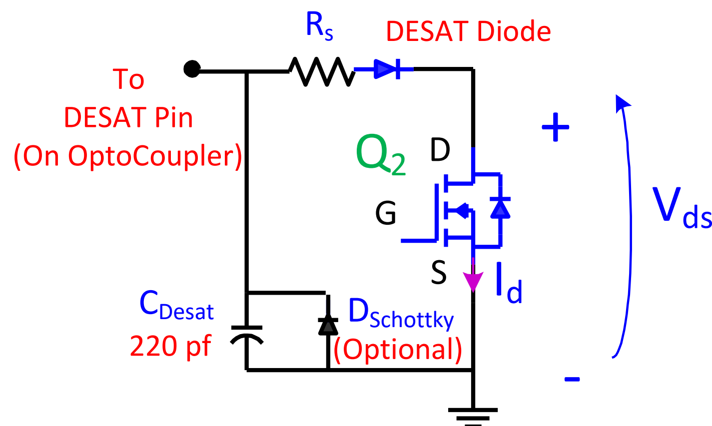

Figure 2-6 DESAT circuit

In Fig 2-6, the Desat circuit used has been shown. The Desat protection pin on the optocoupler senses the on-voltage drop across the device. This is done by connecting Desat diode from DESAT pin of optocoupler to the drain of the MOSFET. A resistance R_s of 100 Ω to 1 k Ω is connected in series to limit the current during transients. An optional Schottky diode can also be used, whose low-forward voltage assures clamping of the DESAT input to ground potential at low-voltage levels. Under turn-on condition, the Desat diode will conduct forward current

for sensing the V_{ds} across the MOSFET and shall block the high voltage when it is turn off [13] . Multiple Desat diodes are generally used to meet the desired forward voltage V_f . For TI ISO5852S optocoupler, the sum of voltage across the device, V_{ds} and the forward voltage drop of the diodes should be less than to 9V under normal operation. If the sum of these voltages exceed 9V, then the desat fault protection is triggered [13].

$$V_{DS-Fault} = (9 - n \times V_f)V \tag{2.5}$$

where n is the number of diodes and V_F is the forward voltage of the diodes.

This abnormal condition occurs during overcurrent or shoot-through conditions.
Since, during turn-on, the current first rises and the voltage subsequently fall afterwards, the desat protection should not operate during this initial period. Hence, a blanking period is provided to avoid spurious turn-off. The blanking time is of order of 310 ns to 480 ns for the optocoupler used. Blanking capacitor, C_{Desat} of 220 pF has been recommended by the manufacturer. The Desat diodes used should have a net blocking voltage of 1200V i.e the rating of the SiC MOSFETs used.

CHAPTER 3

3 Active Gate Driver

3.1 Cross-talk issues with SiC MOSFET phase leg

In phase leg configuration shown in Fig 3-1, during turn-on of a SiC MOSFET, the rate of voltage fall across the device is equal to rate of voltage rise across the complementary MOSFET. The dv/dt experienced by the complementary device results in current flow through miller-capacitor which induces a positive spurious voltage on the gate to source voltage of complementary device [6].

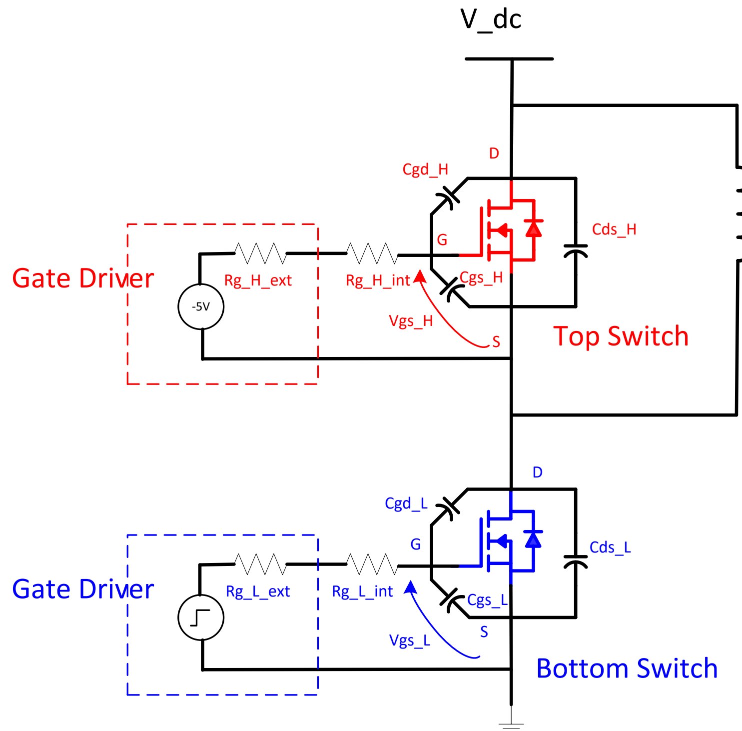

Figure 3-1 Phase-leg configuration for SiC MOSFET

The peak value of the spurious gate voltage [6] can be written as

$$V_{gs_H(\max)} = \frac{dv}{dt} \times R_{g_H} \times C_{gd_H} \times \left(1 - e^{\frac{-V_dc}{\frac{dv}{dt} \times C_{iss_H} \times R_{g_H}}}\right) \quad (3.1)$$

where $$R_{g_H} = R_{g_H_int} + R_{g_H_ext} \tag{1.2}$$

and $$C_{iss_H} = C_{gs_H} + C_{gd_H} \tag{1.3}$$

Due to high turn-on dv/dt of bottom MOSFET, the complementary device experiences current flow through miller capacitor C_{gd} which induces positive spurious gate voltage as shown in Fig 3-2.

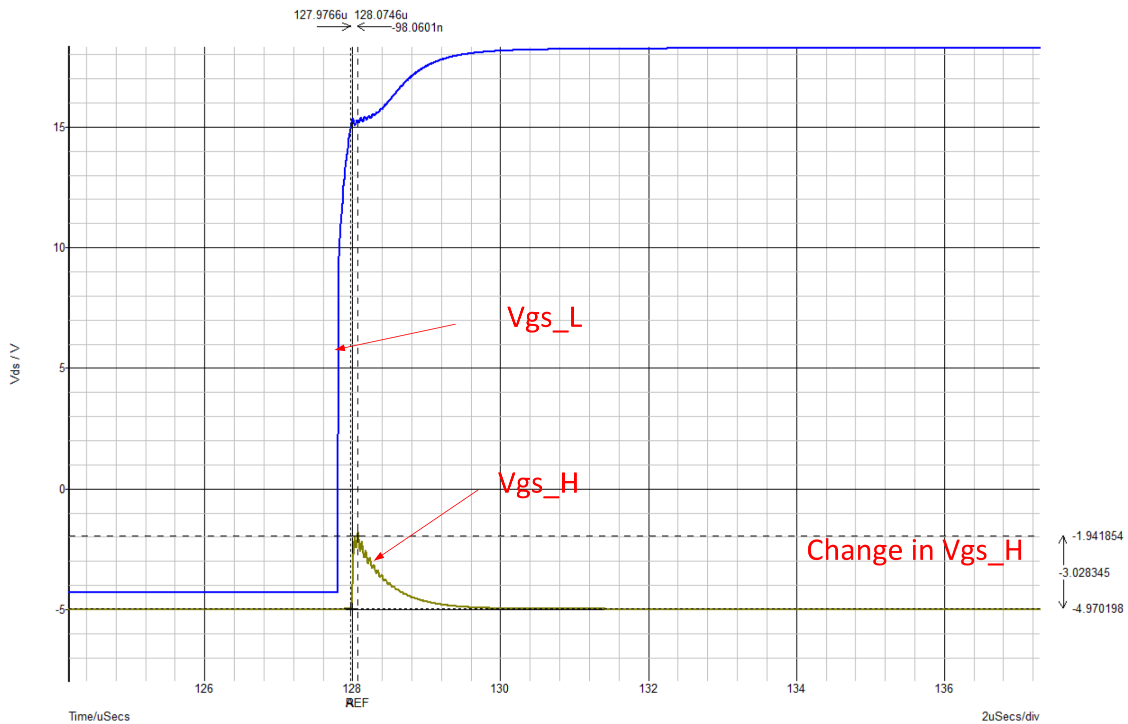

Figure 3-2 Cross talk waveform in phase leg configuration for SiC MOSFETs

The positive induced voltage reduces signal to noise margin on the V_{gs} of the complementary MOSFET making it susceptible to spurious turn-on in the phase-leg. In cases of extreme fast switching, the gate voltage may even cross the threshold voltage which may lead to partial turn-on resulting in additional switching loss and may even lead to shoot through failure. It may be noted that the dv/dt associated with SiC devices varies from one manufacturer to other.

For a device with smaller C_{gs} and C_{ds}, the dv/dt shall be higher for the same gate resistance as the RC time constants shall be lower during gate charging and discharging. Active gate driver circuit has been proposed in [14] in which two gate assist circuits have been proposed to reduce gate loop impedance and controlling the gate voltage respectively for crosstalk elimination. A gate assist circuit reported in [15] provides a bypass path for miller capacitor current.

A low turn-off resistance R_{g_H} for the device under test (DUT) will minimize the positive spurious voltage induced; however, it will increase the turn-off dv/dt of the complementary device. A higher turn-off dv/dt of the DUT shall induce negative spurious voltage on the complementary device. This will not create shoot-through problem but it may degrade the reliability of the complementary device if the magnitude exceeds the maximum allowable negative biased gate voltage [6]. In order to reduce turn-off dv/dt of complementary device, a higher turn-off resistance may be used for it. In that case, only a low turn-on dv/dt of bottom device can help to reduce the magnitude of positive spurious voltage. The dv/dt for a higher resistance is lower but the main disadvantage of using a higher resistance is increased switching losses. An active gate driver can be used to reduce turn-on losses and mitigating spurious induced voltage to improve reliability. A two-stage active gate driver is designed which uses lower gate resistance in first stage to reduce di/dt and higher gate resistance in second stage for minimizing dv/dt. The two-stage active gate driver can independently control turn-on di/dt and dv/dt to mitigate cross-talk.

3.2 Active Gating Circuit

An active gate driver can be used to maintain turn-on di/dt as per lower gate resistance in 1st stage and turn-on dv/dt in second stage as per higher resistance in 2nd stage. Variable resistance based active gate driver has been used for IGBT in [16]. The basic concept of active gating can be explained using Fig 3-3. If $R_{on_1}<R_{on_2}$, during turn-on of a main MOSFET, the auxiliary MOSFET M1 is turned on to provide gate resistance of R_{on_1} in first stage. In second stage, auxiliary MOSFET M1 is switched off and M2 is turned-on to get gate resistance R_{on_2} during second stage. The two stage gate driver allows to decouple turn-on di/dt and dv/dt. This can be implemented by providing suitable signals to MOSFETs M1 and M2.

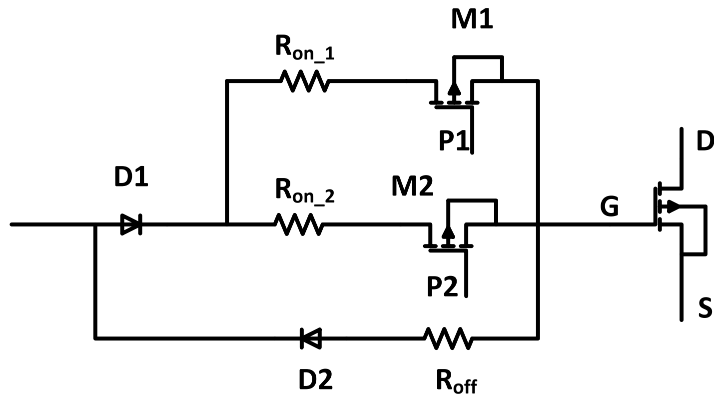

Figure 3-3 Active gate driving concept circuit

The main challenge in the logic circuit shown in Fig 3-3 is to get timing correct as one of the two resistance should be in gate path during the transition. However with SiC MOSFETs, it becomes more challenging as transition times for changing from one resistance to the other are of order of tens of nano-seconds.

An alternative approach is to use circuit shown in Fig 3-4 with only one MOSFET M1. If MOSFET M1 is turned-on during first stage, then effective resistance is $R_{on_1} \parallel R_{on_2}$. When MOSFET M1 is turned off during second stage, the gate resistance shall be R_{on_2}.

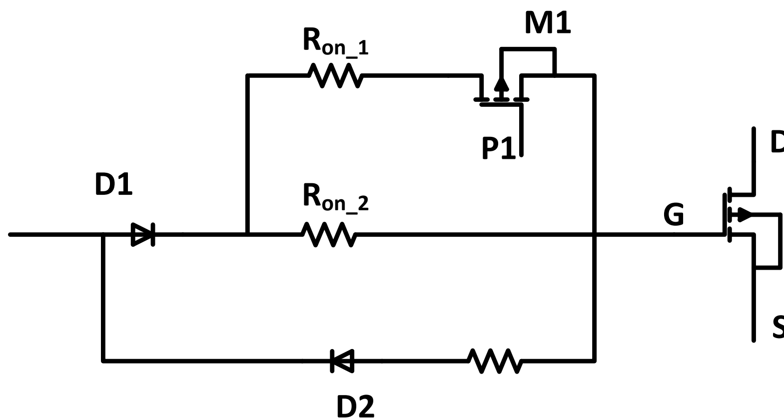

Figure 3-4 Active gate driver Circuit Used

The lower resistance during stage 1 needs to be configured using the parallel combination of the two resistances which should be less than R_{on_2}. Placement of diode D1 in forward path is

required to ensure body diode of auxiliary MOSFET doesn't conduct during turn-off. Otherwise, it will affect the turn-off gate resistance.

3.3 Delay Circuit and Timing Diagram

A delay circuit has been used for generating delay PWMs of order of 10-20 ns. An all-pass network as shown in Fig 3-5 is used to generate the delayed PWM using op-amps OP2 and OP3 with bandwidth of 300MHz. A wide bandwidth buffer OP1 is used at the input for high input impedance. The delay time is defined by the R and C shown in the Fig 3-5. The effective delay is given by the following equation

$$T_{delay} \geq 2(2RC + T_d) \tag{3.2}$$

Where Td is the delay of op-amp and has typical value of 2.8 ns for op-amp used in circuit.

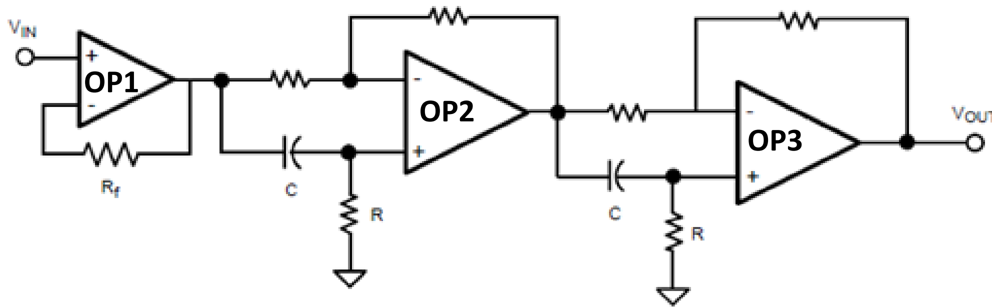

Figure 3-5 All-pass network to generate delayed PWM

Trimmer (variable resistor) is used for resistance variation to generate different delay signals by keeping the same capacitor. Capacitive loading of op-amps mentioned in the datasheet should be considered as well the effect on slew rate with capacitor variation. An inverter is placed at the output of the all-pass network to generate a complementary PWM P1 with timing sequence shown in the Fig 3-6. The delayed pulse D1 is generated from PWM from the receiver and the complementary pulse P1 is generated using an inverter.

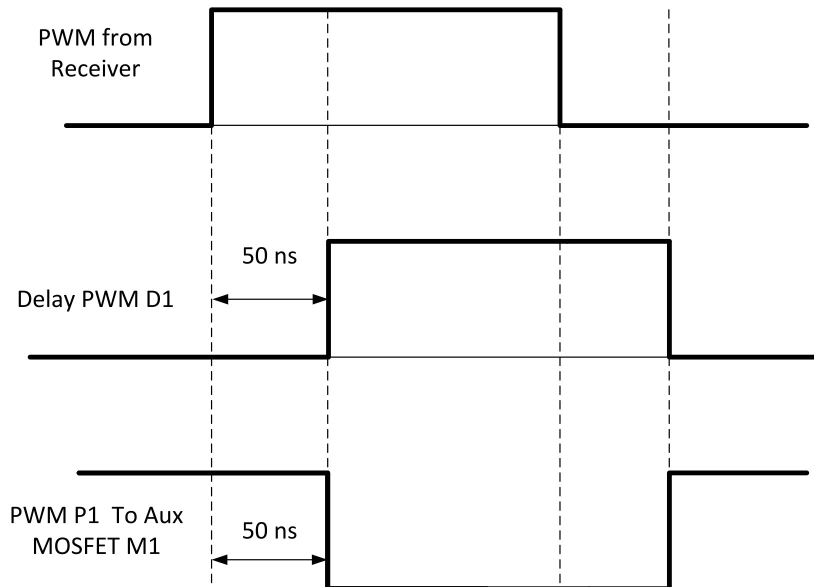

Figure 3-6 Timing diagram for Main MOSFET and Auxiliary MOSFET

In the active gate driver designed, it is possible to achieve delay PWM of order of 1ns if very precise trimmer is used. This can be explained with the help of Fig 3-7

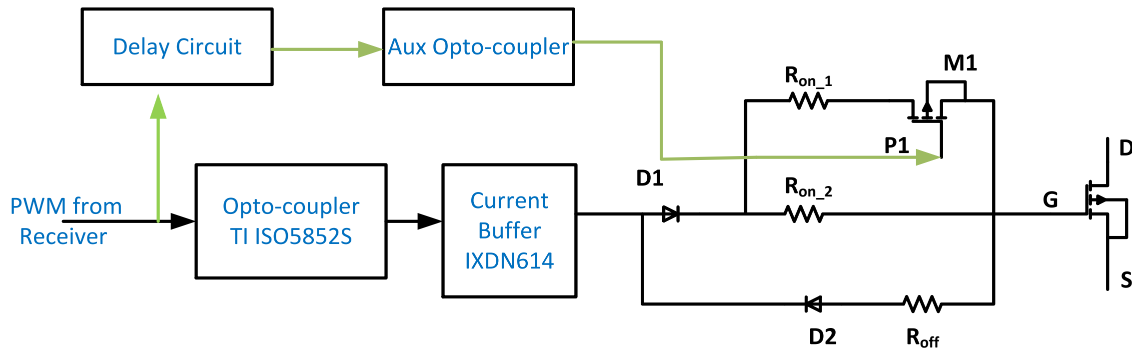

Figure 3-7 Block Diagram for 2-stage Active gate Driver

To closely match the timings of the PWM for SiC MOSFET and the delayed PWM for Aux MOSFET, same opto-coupler IC has been used for driving auxiliary MOSFET. Since current buffer is also present in the path of the PWM for SiC MOSFET, it should also be taken into account. As the propagation delay of current buffer IC IXDN614 [17] is 50-70 ns, the delay circuit should generate extra delay (in ns) to compensate. In fact, it is possible to turn-off

MOSFET M1 even before the PWM for the main SiC MOSFET by taking advantage of current buffer propagation delay.

3.4 Active gating for di/dt and dv/dt control with loss optimization

As explained in section 3.1, a two stage active gate driver is considered to control turn-on di/dt as per lower gate resistance in first stage and control turn-on dv/dt as per higher gate resistance in second stage. In Fig 3-8, a turn-on switching transient of a SiC MOSFET has been shown. It can be observed that the initial rate of current rise is slower, Once the current reaches 50-70% of the maximum load current,the di/dt is higher. If the rate of current rise can be increased in di/dt region marked in Fig 3-8 by using a lower resistance, then the area under product of V-I curve should reduce leading to lower turn-on loss.

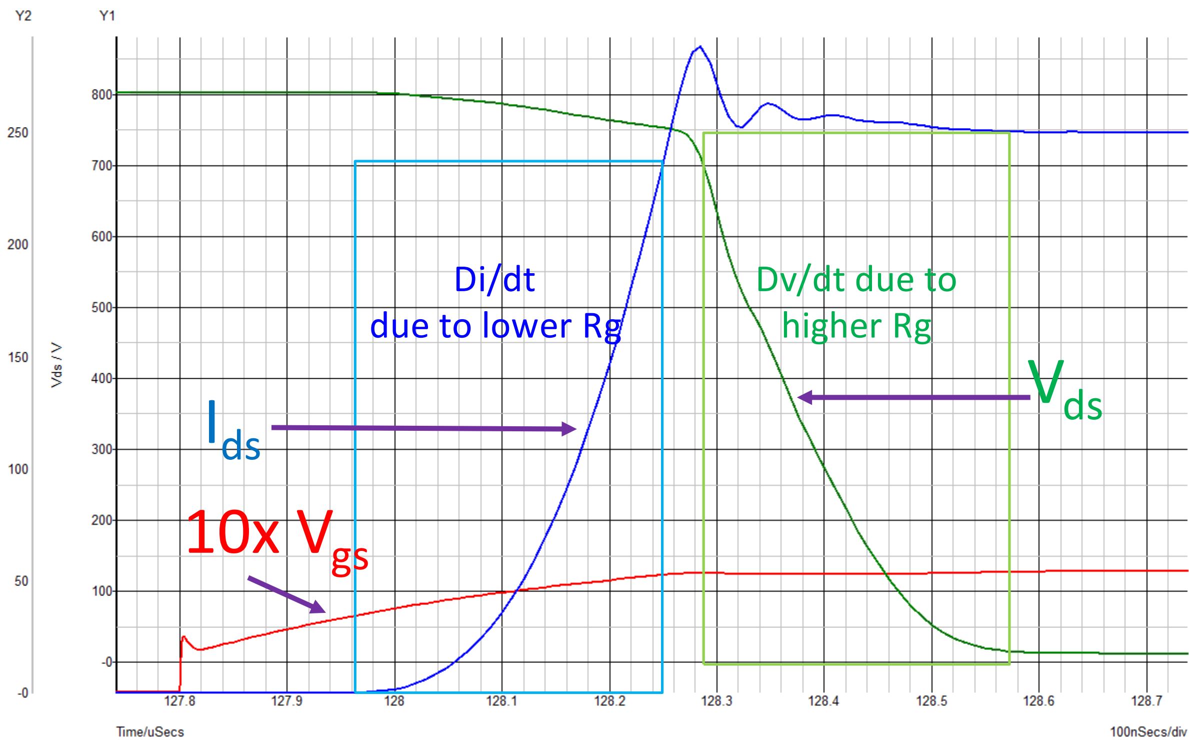

Figure 3-8 Scope for Loss Reduction with lower dv/dt

Also, due to higher di/dt, the voltage drop due to L*(di/dt) shall also be higher which will also contribute in reducing the turn-on switching loss. However, if the loop inductance is low, then

the voltage drop may not be appreciable. The turn-on gate resistance should be switched to a higher resistance near 50-70% of the load current value. Otherwise, a higher current overshoot may occur due to lower resistance which in turn increase the switching loss. By using optimum timing for transition of gate resistance from lower gate resistance to higher gate resistance, the switching losses can be optimized. This switching loss shall be lower as compared to the case when non-active gate driving is used with the higher gate resistance (which is used in 2nd stage of active gating).

3.5 Active Gate Driver PCB

A 4-layer PCB with dimensions of 95.6 mm x 110.5 mm has been designed in Altium Designer. Fig 3-9 shows the PCB designed for 2- stage active gate driver. The current buffer IC has been placed close to the gate-source terminals to reduce the gate loop inductance.

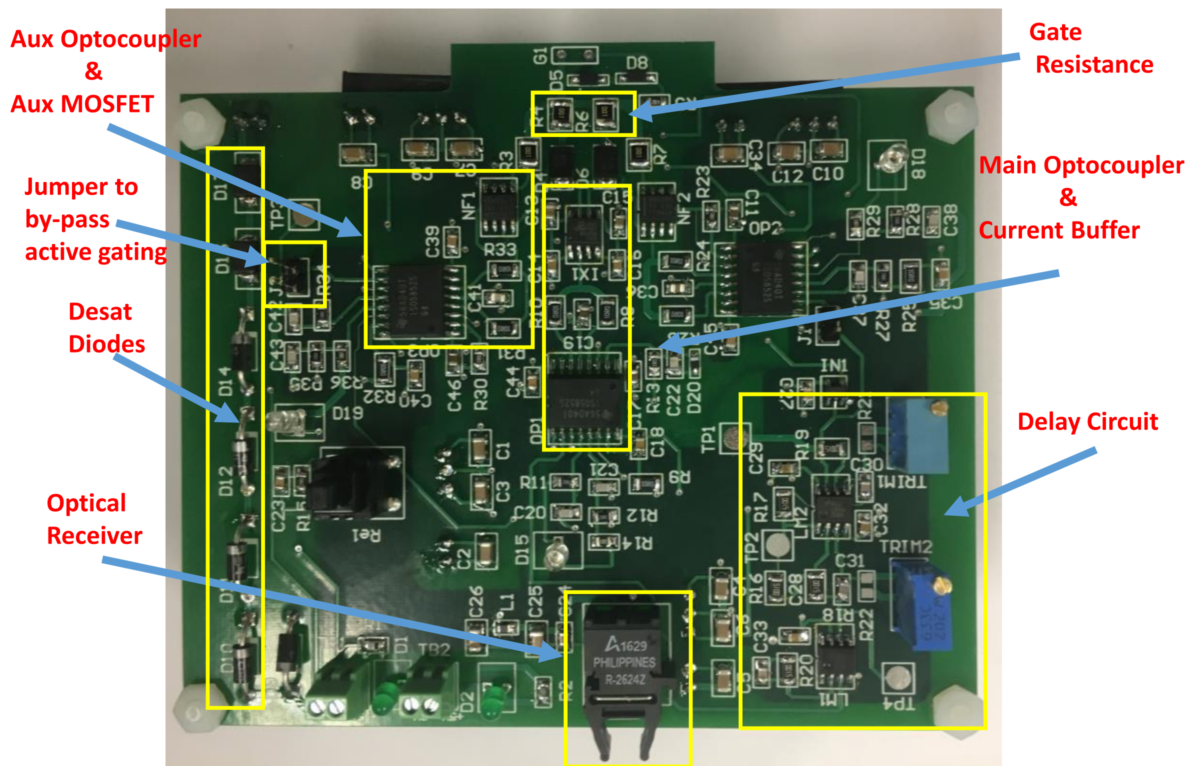

Figure 3-9 Two-stage Active gate Driver PCB

The top layer has been used for routing of signals. Second layer has been used as ground plane while third layer has been used as power plane. Power connections are done by placing de-coupling capacitors very near to the power pins. Vias have been used for direct connection to power plane. The bottom layer has been used for signal routings at some places.

Position of various components has been marked for easy identification. A jumper has been provided for flexibility of including or excluding active gating circuitry. This gate driver shall be used for testing and results are provided in Chapter 5.

CHAPTER 4

4 Double Pulse Testing and DC Bus Design

4.1 Double Pulse Test

For validating the effectiveness of active gate driver, switching losses for SiC MOSFET are measured first without using active gating feature. Switching loss are then compared when driving the device with active gate driver. A double pulse test (DPT) set up as shown in Fig. 4-1 is used for characterization of SiC MOSFET.

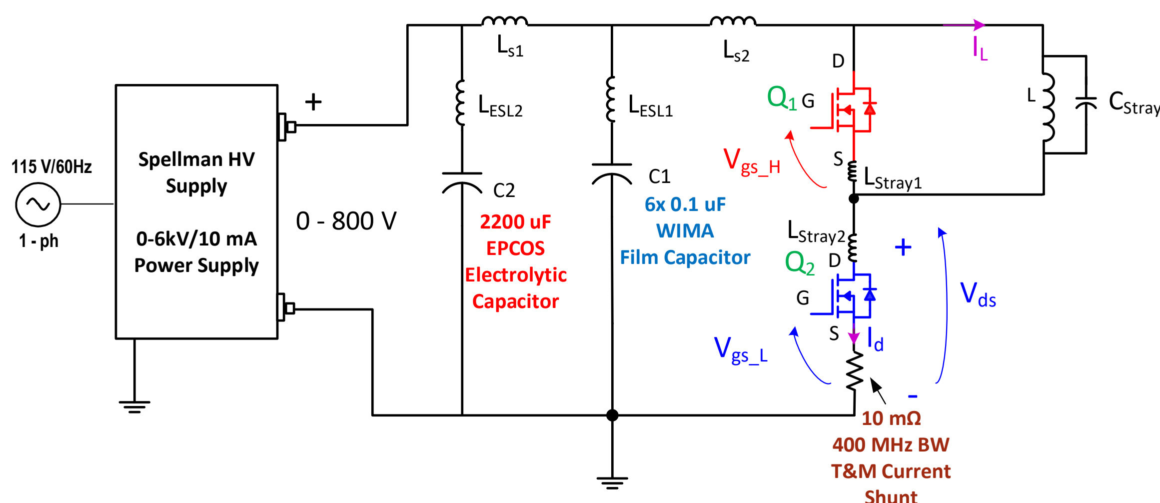

Figure 4-1 Double Pulse Test Set up for characterization of SiC MOSFET

A 1200 V/ 300 A ROHM SiC half bridge power module BSM300D12P2E001 has been used for DPT. An air core inductor of 113.7 uH is connected across the top MOSFET Q1. An air core inductor has been used to avoid saturation issues. However, current limit must still be kept in limit to ensure that the devices doesn't get heated up if current exceeds its maximum rating.

Double pulse is applied to the bottom MOSFET Q2 which is the device under test (DUT). The top switch Q2 is always switched off by applying negative Vgs to ensure that only diode of the top MOSFET Q1 conducts. When MOSFET Q2 is turned on, the inductor current rises linearly and the current starts to flow though Q2. On turning off Q1, the current starts to freewheel

through body diode of Q2. Since during first turn-on of MOSFET Q2, the device current is zero, so the turn-on switching losses are not measured at first turn-on transition. The turn-on switching losses are measured at the turn-on instant of second pulse. The turn-off losses are measured at the turn-off instant of first pulse.

For DPT, only two pulses are used. This is due to the fact that no extra information is gained by increasing the number of pulses. Secondly, the inductor current will keep on increasing and can lead to inductor saturation (if air core inductor is not used). This should be avoided as it will lead to short circuit. Thirdly, with continuous switching, the device gets heated up and the junction temperature may increase and the losses reported for a particular temperature may not be accurate.

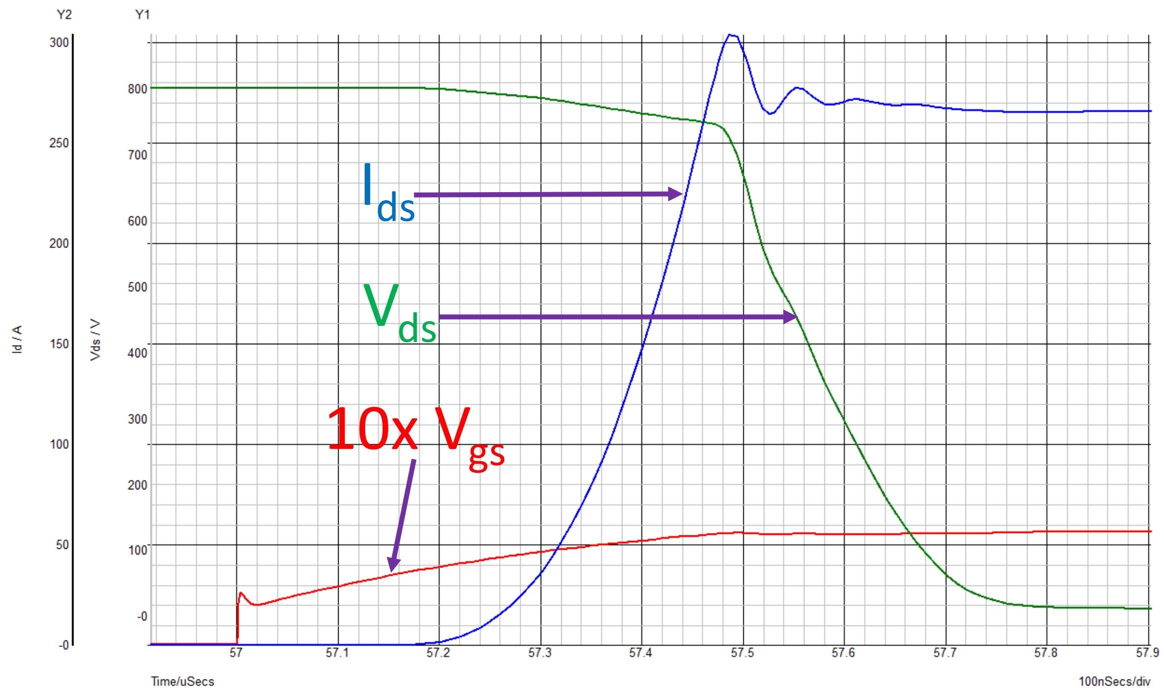

Figure 4-2 Turn-on transient of SiC MOSFET

Fig 4-2 shows the turn-on transition for DPT. At turn-on, there is current overshoot which may depend on reverse recovery current of the diode of the top switch and switching di/dt. Fig 4-3 shows the turn-off transients for SiC MOSFET. During turn-off, voltage overshoot occurs and

the magnitude of overshoot is equal to L*di/dt. To minimize the voltage overshoot at high di/dt switching, the loop inductance ‘L’ needs to be minimized.

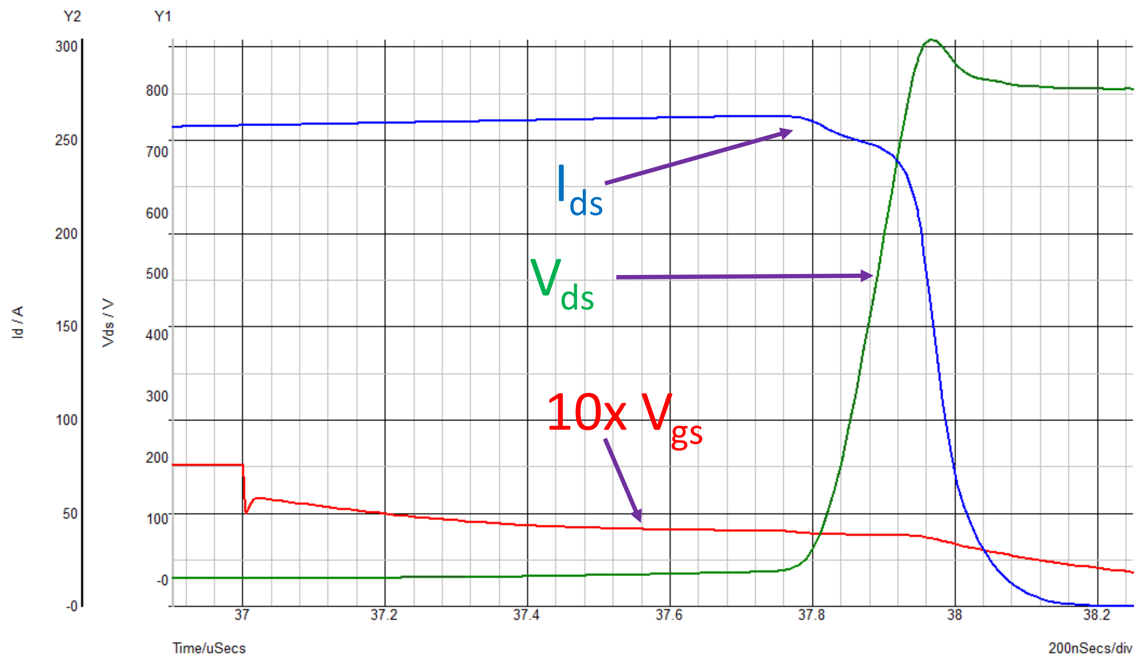

Figure 4-3 Turn-off transient of SiC MOSFET

4.2 DC Bus Design

4.2.1 Capacitor Bank Sizing

For SiC MOSFET switching at high di/dt, low loop inductance is required to minimize voltage overshoots and ringing. This is achieved by placing film capacitors very near to the device which supply the pulse current at switching transients. The film capacitors are selected based on peak current carrying capacity, voltage rating and equivalent series inductance (ESL). Multiple film capacitors are generally placed in parallel to reduce the effective inductance. For film capacitors, 6 numbers of 0.1 uF WIMA capacitors FKP1T031007E00JSSd [20] are connected in parallel.

A combination of electrolytic and film capacitors is used for the capacitor bank. The electrolytic capacitors ensure that DC bus voltage is maintained with little or negligible voltage

drop and also supply the steady state current after the switching transients. These capacitors are comparatively placed far off from the device as compared to the film capacitors. For sizing the electrolytic capacitors, the following relation is used [18]:

$$C_{EL} = \frac{L * I_L^2}{V_i^2 - V_f^2} \tag{4.1}$$

Where L is the inductance of load inductor

V_i = Initial Input voltage

V_f = Final Input voltage (with voltage drop)

I_L = Peak Inductor current drawn

For V_i = 800V and V_f = 795V, I_L= 375 A and L = 113.7 uH, the size of capacitor bank comes out to be 2004.9 uF. TDK/ EPCOS screw capacitors B43456A9338M [19] of 3300 uF / 400V rating have been used for DC bus. Three capacitors are placed in series and three more such capacitor are connected in parallel to achieve DC bus capacitance of 2200 uF. Balancing resistor of 1MΩ is connected in parallel with the capacitors for equal voltage sharing.

4.2.2 Current Sensing

The device current measurement method can also introduce additional power loop inductance. The following three options can be used:

a. Rogowski coil
b. Pearson Current Monitor
c. Current Shunts

Rogowski coils are small and compact and contribute negligible or no inductance for a good layout. However, for 250 A current, the maximum bandwidth of commercially available coils is 30MHz [21].

Pearson current [22] monitor for high band width are available. However, since the current has to flow though the current monitor, the busbar connection used introduces extra loop inductance. To reduce this inductance, multiple parallel connection may be used.

T&M Research Shunt SSDN-414-01 shunt [23] with 10 mΩ resistance and 400 MHz bandwidth has been used for DC bus PCB. The shunt not only reduces the loop inductance, it can also track high di/dt current very accurately.

According to control theory [24],

$$BW = \frac{0.35}{\min(t_r, t_f)} \tag{4.2}$$

Where t_r is the rise time and t_f is fall-time of the signal.

A 400 MHz bandwidth (BW) shunt should be able to track a 80Mhz signal well (i.e. 1/5 th of BW). For 80 MHz, rise/fall- time is order of 4.375 ns. For 250A peak current, the rise/fall-time encountered are of order of 100-200 ns, so 400 MHz bandwidth shunt can very accurately track the current.

4.2.3 PCB Design

For low loop inductance, PCB design can help to achieve low loop inductance as compared to copper bus bar connections. Although PCB is required to be designed for testing for 1200V/ 300 A device, it can be designed on PCB as only pulse testing is envisaged. For continuous current, heat removal shall be an issue and PCB design is not recommended.

A 4-layer DC bus PCB is designed using Altium Designer as shown in Fig 4.-4. It has 4-oz copper on the outer layers and 2 oz copper on the inner layers. Clearance between layers is of utmost importance. The film capacitors are arranged in zig-zag manner to avoid current crowding. It also ensures that the current path is equal for top layer and bottom layer.

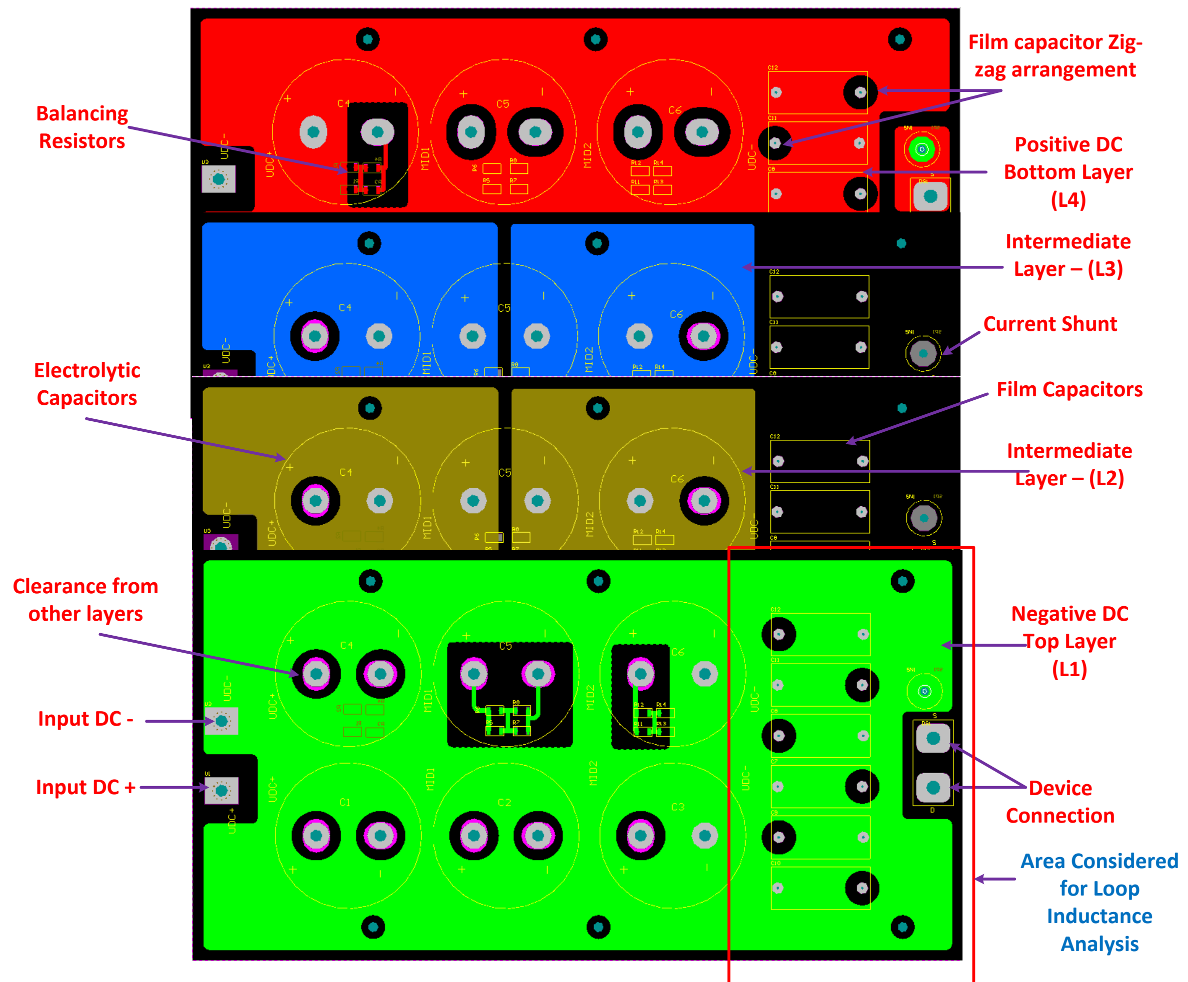

Figure 4-4 Layer Stack-up for DC Bus PCB

A layer stack up is provided in Fig 4-4. All copper corners should have smooth curvature.

4.3 Ansys Q3D Simulation

After designing the PCB in Altium Designer, its loop inductance is analyzed using Ansys Q3D. As the low loop inductance of PCB is defined by the film capacitors, so only small portion of PCB is analyzed which has film capacitors. The area is also marked in Figure 4-4 on layer 1. Altium gives the option of exporting the PCB layers to AutoCAD. It is advised to export the files layer by layer. The AutoCAD files can then be imported to Ansys Q3D for analysis.

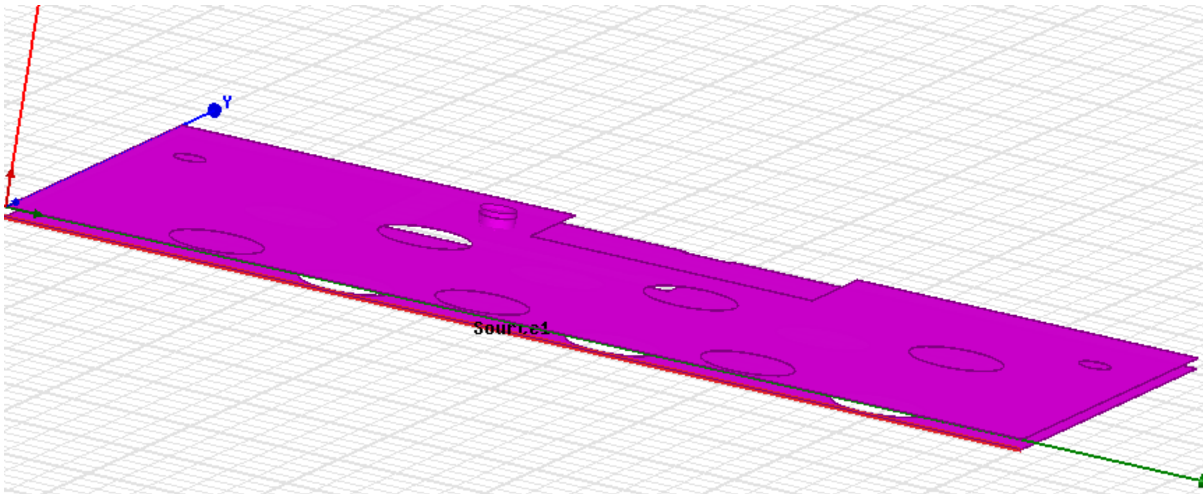

Figure 4-5 Inductance Analysis of PCB using Anys Q3D

For inductance analysis, a continuous path is required. For shunt connection, the top and bottom layers should be shorted together. Also the loop is still not closed as the device is not connected. The drain-source is shorted through copper connection. After that, a sink and source is defined for flow of current. The bottom layer is marked as source in Fig 4-5. Using Ansys Q3D, inductance has been calculated as 16.371 nH at 100 kHz as shown in Fig 4-6..

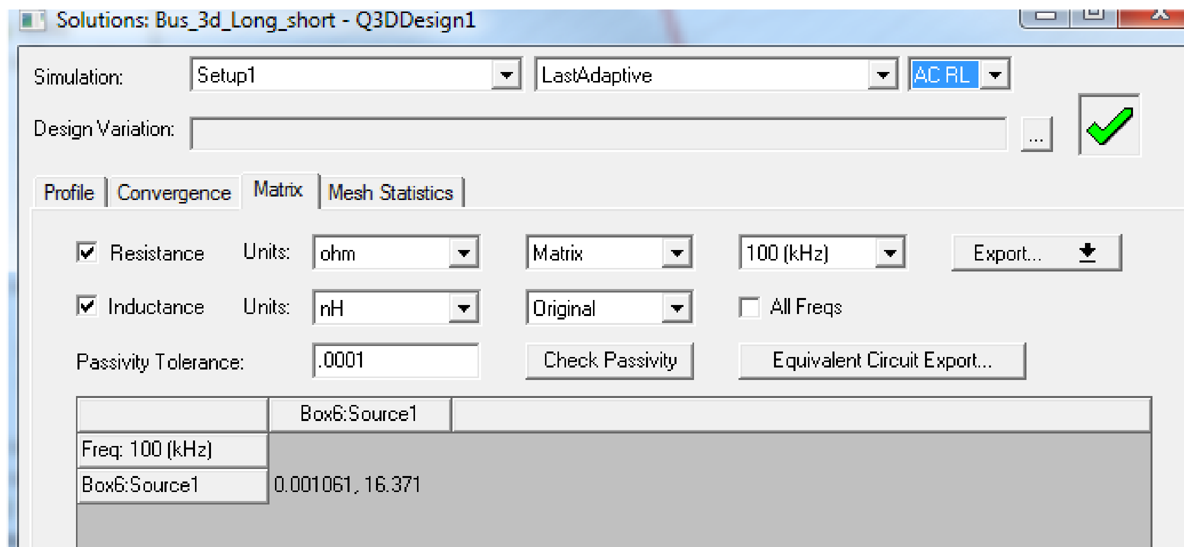

Figure 4-6 Inductance using Ansys Q3D simulation

However, this inductance doesn't include the module stray inductance. The stray inductance of the ROHM SiC power module BSM300D12P2E001 [9] is 13nH as per the datasheet.

Figure 4-7 ROHM SiC power module BSM300D12P2E001

So, net inductance of the PCB is expected to be ~30 nH. In addition, there will be extra inductance due to connection of nuts and screws. The spice models were then used in SIMPLIS/ SIMETRIX to simulate the effect of around 30 nH inductance. The overshoot for 2Ω gate resistance was found out to be of 167 V at 800V using Spice Models [10] which is less than 1200V rating of SiC MOSFET as shown in Fig 4-8.

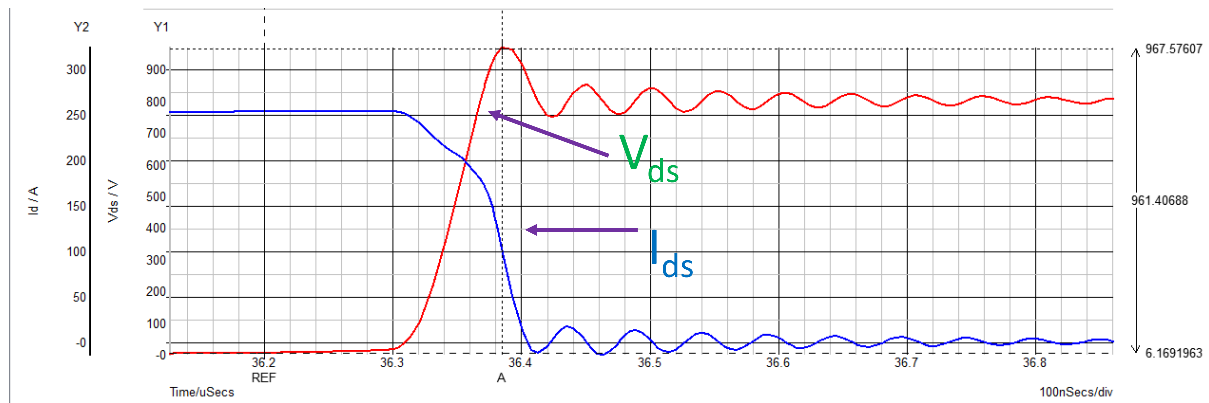

Figure 4-8 Peak Voltage overshoot for 800V input, 250A current for R_g= 2Ω

4.4 Loop Inductance of PCB

After analysis in Q3D, PCB was manufactured. Fig 4-9 shows the DC bus pcb designed for the thesis work.

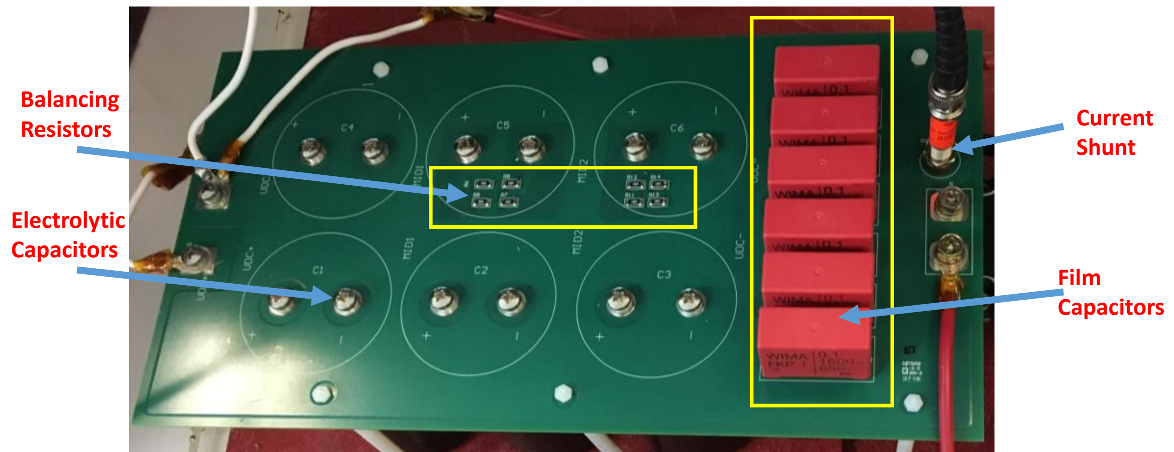

Figure 4-9 DC Bus PCB

The loop inductance of the PCB can be calculated by observing the overshoot voltage at turn-off and measuring the turn-off di/dt.

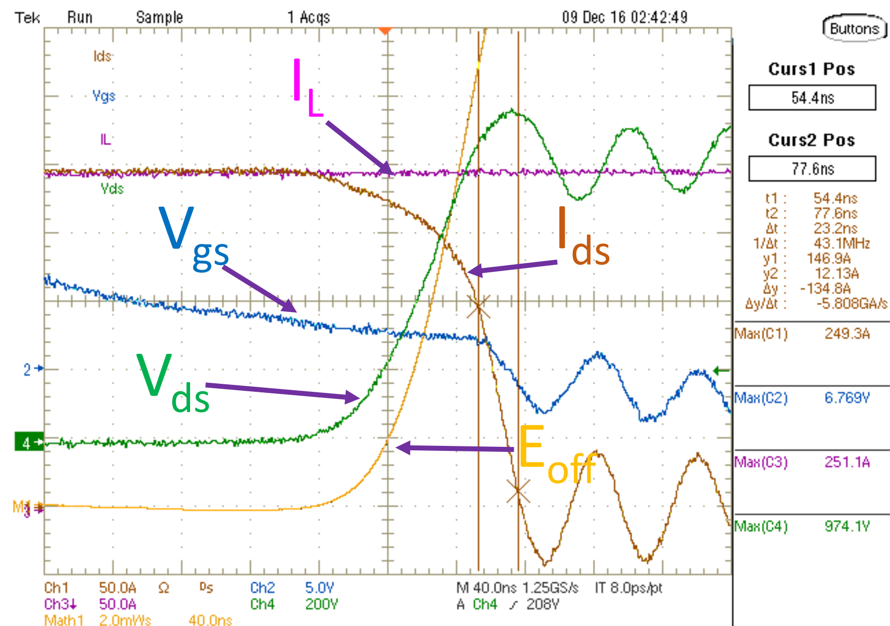

Figure 4-10 Turn-off switching transients at 800V for $R_{goff} = 2\Omega$

The following relation can be used

$$V_{Over-shoot} = L \times \frac{di}{dt} \tag{4.3}$$

In Fig 4-10, the voltage overshoot is 174.1V at DC bus of 800V and di/dt is 5.808 kA/us. So, the loop inductance for the DC is 174.1/5.808 ~ 30 nH which involves loop inductance of module. The module stary inductance is 13nH as per datasheet. The effective loop inductance of PCB is approximately equal to 23.5 nH (= 30 – (13/2)). The designed DC bus PCB with low loop inductance is used for characterizing SiC power module and results are reported in Chapter 5.

CHAPTER 5

5 Hardware Results

5.1 Switching Loss Measurement Consideration

For validating the improvement in loss reduction using active gating, it is required to characterize a SiC MOSFET using DPT under same conditions with and without active gating. A SiC ROHM power module BSM300D12P2E001 of 1200V/ 300A rating has been used.

For measuring switching loss, it is very important to ensure that the bandwidth of voltage probes and current sensors is sufficient to track voltage and current transients of a fast SiC MOSFET. The relation between bandwidth and rise time is given in equation 4.2.The following instrumentation has been used for experiments

Table 5-1 Details of Measurement Instrumentation Used

S.No	Instrumentation Used	Details
1	Tektronix P5205A Differential Probe	100 MHz BW
2	T&M Research Current Shunt SSDN-414-01	10 mΩ, 400 MHz BW
3	Tektronix TDS5054B Oscilloscope	500 MHz 5GS/s
4	Pearson Current Monitor Model 3972	20 MHz BW

The probes must be de-skewed [24] to ensure accurate measurement of switching losses which is defined by area under product of Voltage-current graph. For de-skewing the probes, the load inductor is replaced with a resistor in the DPT setup. If a voltage pulse is applied to the system, then voltage and current should be in phase since the load is resistive. As the current shunt is of higher bandwidth, the voltage measurement lags the current measurement. By using the de-skew feature of the oscilloscope, the voltage is de-skewed to synchronize voltage and current transitions through the resistor. The switching loss measurement can now be done after de-skewing.

5.2 Test Setup

Fig 5-1 shows the double pulse test set up for the characterization of ROHM SiC Module BSM300D12P2E001. It is an E-type module in H-bridge configuration. An air core inductor of 113.7 uH is used for the testing to avoid saturation of inductor. A pearson current Monitor 3972 has been used for inductor current measurement.

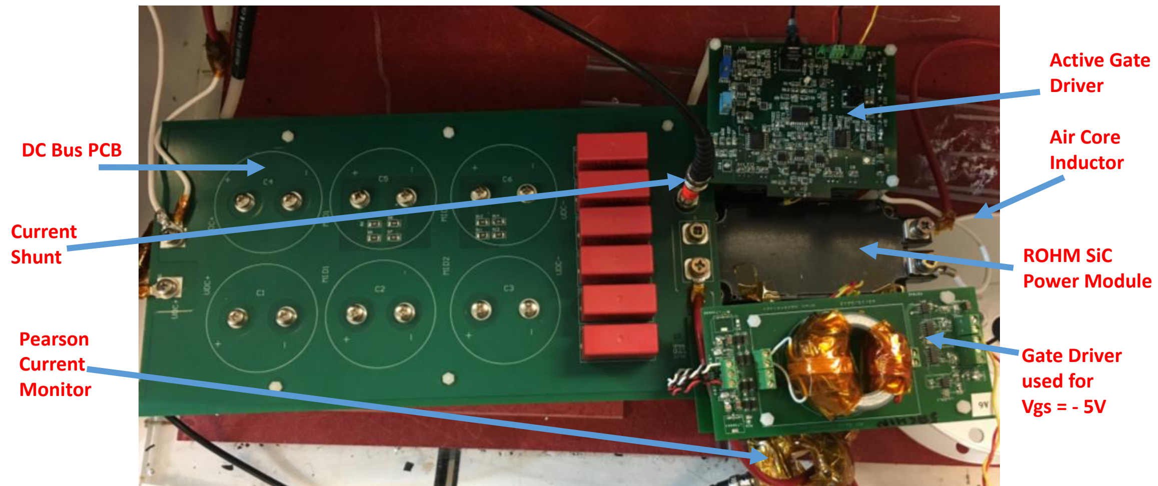

Figure 5-1 Double Pulse Test Setup

V_{gs} of -5V is applied to the high side MOSFET to ensure that only body diode is used. This provides higher safety margin against spurious turn-on associated with high turn-on dv/dt as shown in Fig 3-2. The bottom side MOSFET is provided double pulse through the gate driver. The inductor current can be calculated by using the relation

$$I_L = \frac{V}{L} \times DT_s \tag{5.1}$$

The on-duration of first pulse is set accordingly to reach 250A for different voltages. The second pulse is kept very short as compared to first pulse to limit current rise as the turn-on transients are of main interest for the second pulse.

5.3 Results without Active Gating

The gate driver has a jumper which allows to by-pass active gate driving feature. First, DPT is done without using active gating feature. For all results, Vgs of +20V / -5V has been used. The testing is done for a current of 150A, 200A and 250 A. Fig 5-2 shows the turn-on loss measurement for 600V, 250A for 3.9Ω turn-on gate resistance. Oscilloscope is suitably triggered to capture the turn-on transients. The gate resistor are of 0.25 W rating for all tests. Please note that all gate resistances mentioned are external gate resistances.

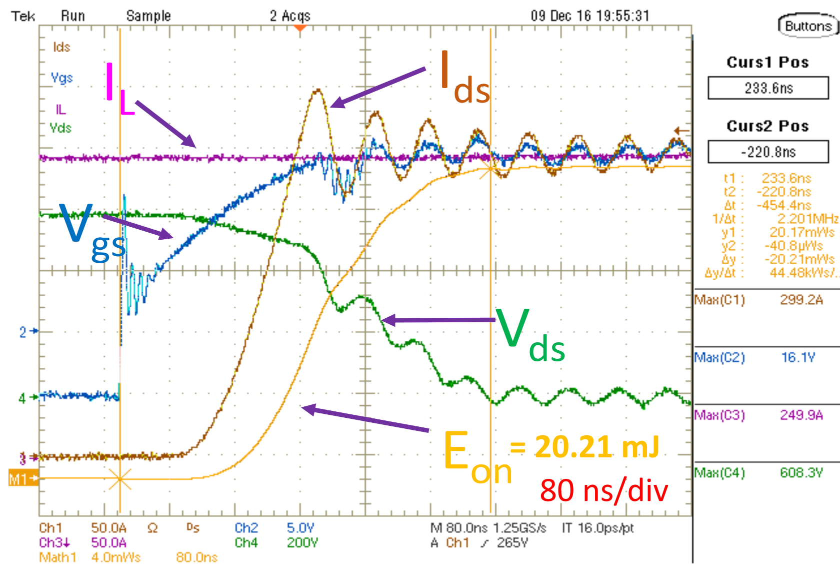

Figure 5-2 Turn-on Loss measurement for 600V, 250A at gate resistance of 3.9Ω

As per IEC 60747-9, the turn-on switching losses are calculated using following equation

$$E_{on} = \int_{t1}^{t2} v_{ds}(t) * i_{ds}(t) dt \tag{5.2}$$

where t_1 is 10% of V_{gs} (on) and t_2 is 2% of V_{ds}. Math function of the oscilloscope has been used to calculate turn-on losses in Fig 5-2 which gives E_{on} of 20.21 mJ for 600V, 250A at gate resistance of 3.9 Ω.

Similarly, as per IEC 60747-9 the turn-off loss is calculated using following equation

$$E_{off} = \int_{t3}^{t4} v_{ds}(t) * i_{ds}(t)dt \quad (5.2)$$

where t_3 is 90% of V_{gs} (on) and t_4 is 2% of I_{ds}. Fig 5-3 shows the turn-off transients of ROHM SiC MOSFET at 600V, 250A at turn-off gate resistance of 3.9 Ω. A voltage overshoot of 125.3V is observed due to presence of loop inductance.

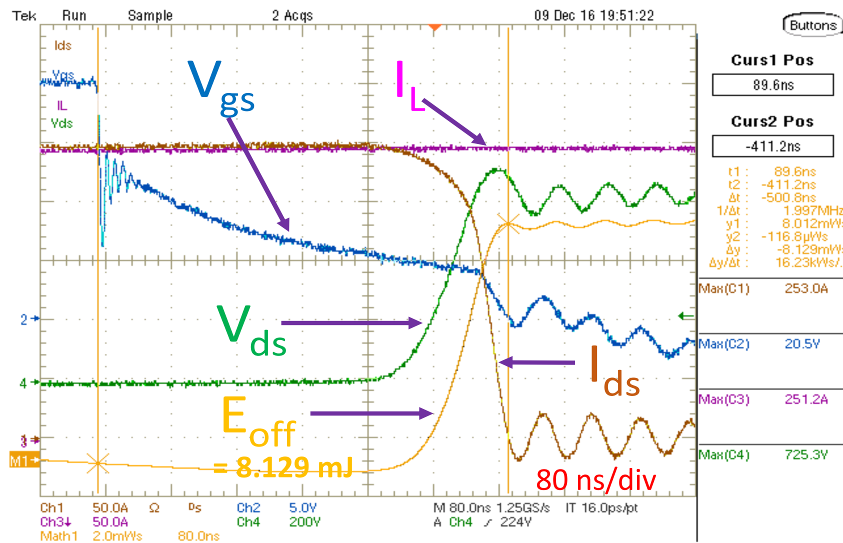

Figure 5-3 Turn-off Loss measurement for 600V, 250A at gate resistance of 3.9Ω

5.3.1 Turn-on Results at 800V without active gating

The ROHM module used has been characterized at 800V by repeating DPT at 150A, 200A and 250A for 2Ω and 3.9Ω. All the testing is done by disabling the active feature of the gate driver. The results without active gating have been plotted in Fig 5-4 to Fig 5-7.

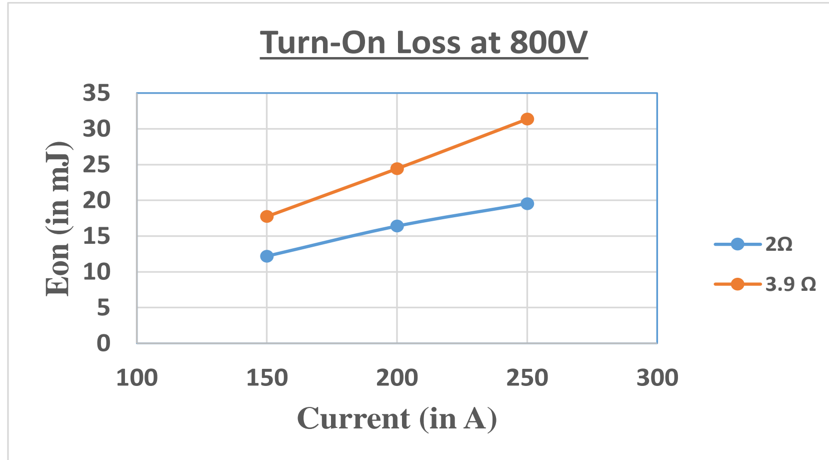

Figure 5-4 Turn-on losses at 800V switching for gate resistance of 2Ω and 3.9Ω

As expected, the turn-on switching loss for gate resistance of 3.9 Ω is higher than that for 2Ω which can be seen in Fig 5-4. The turn-on peak current, di/dt and dv/dt are higher for gate resistance of 2Ω which can be seen in Fig 5-4, Fig 5-5 and Fig 5-6 respectively.

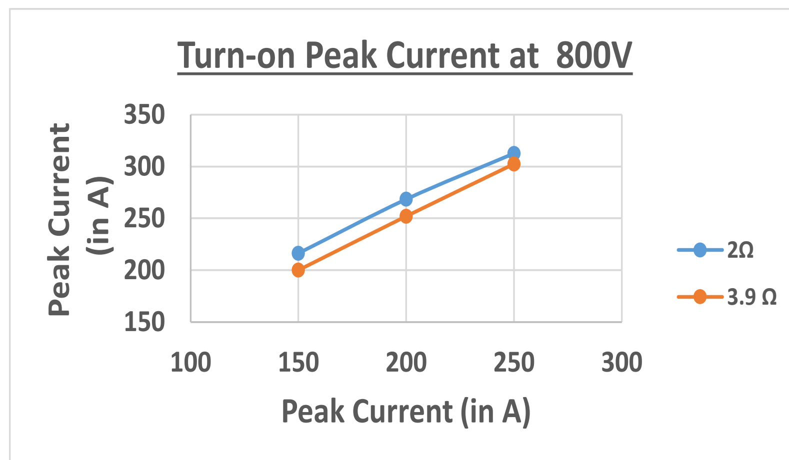

Figure 5-5 Turn-on Peak current at 800V for gate resistance of 2Ω and 3.9Ω

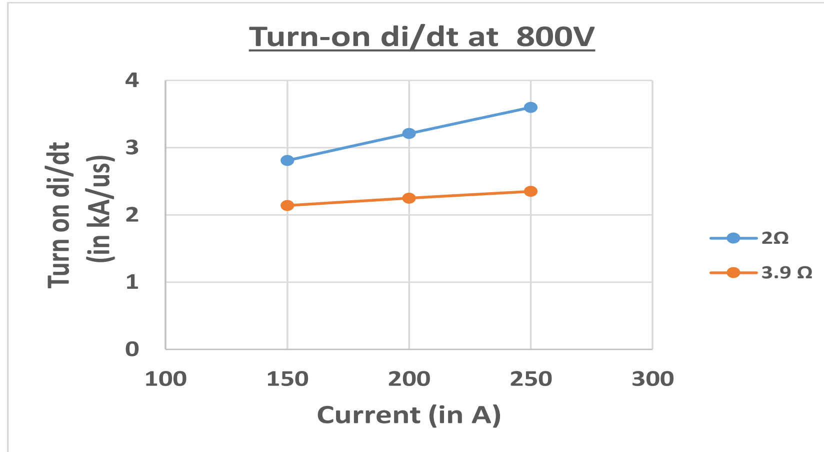

Figure 5-6 Turn-on di/dt at 800V for gate resistance of 2Ω and 3.9Ω

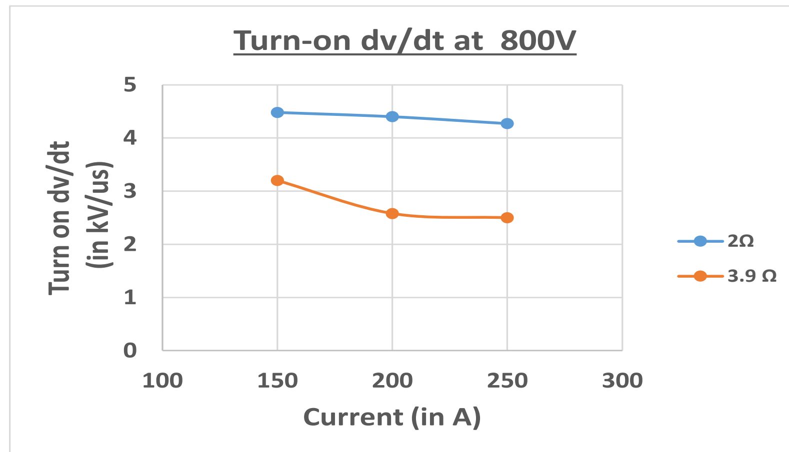

Figure 5-7 Turn-on dvdt at 800V for gate resistance of 2Ω and 3.9Ω

5.4 Results with Active Gating

5.4.1 Delayed Pulse Generation

To change the turn-on resistance at the correct instant, the turn-on delays and rise times of currents for different resistances needs to be observed. The delay circuit needs to be tuned for turning off the auxiliary MOSFET accordingly. The triggering time for delay circuit should be tuned according to following timing:

$$t_{trigger} = t_{on-delay} + t_{i-slow-rise} + t_{ibuffer_prop_delay} - t_{Aux-MOS-turn-off} \tag{5.3}$$

which depends on the turn-on delay for the gate resistance, the time period for slow-current rise, propagation delay of current buffer and the time required to turn-off the Aux MOSFET. As the timing instants depend on number of variable times, the triggering time is changed using a variable resistor in the delay circuit to find operating points for optimum turn-on losses.

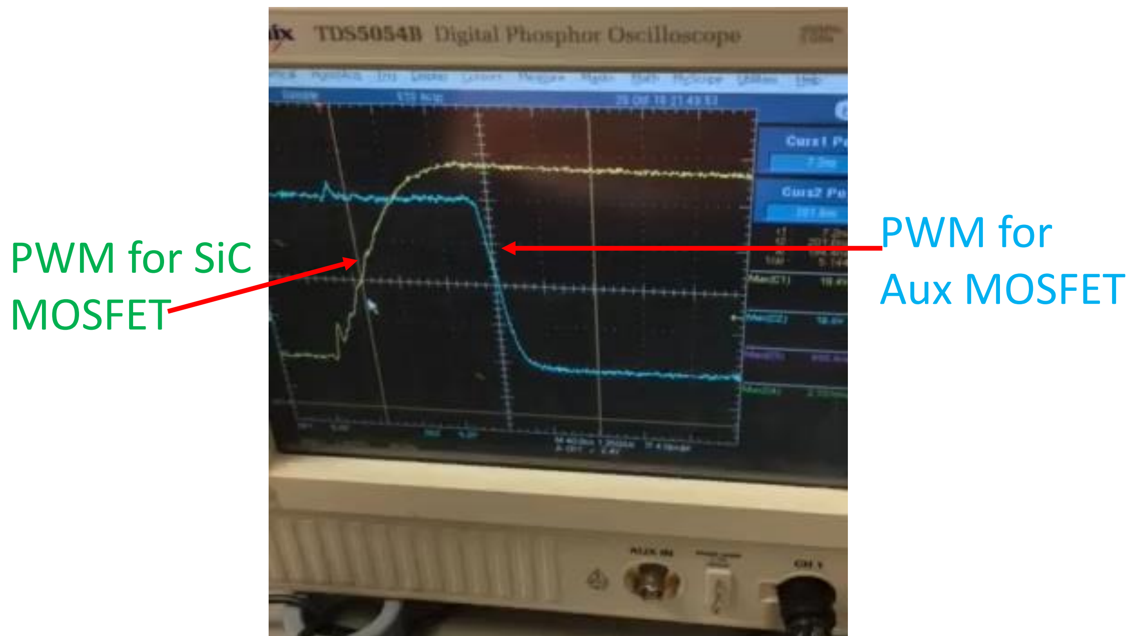

Figure 5-8 PWM generated for Aux MOSFET for Active gating

Fig. 5-8 shows the PWM for driving SiC MOSFET (in yellow) and the trigger pulse for Aux MOSFET (in blue). By using trimmer, the delay timing for the delayed pulse can be varied. Fig 5-9 shows the gate to source voltage (V_{gs}) waveform for non-active gate driver while Fig 5-9 shows the V_{gs} waveform for active gate driver.

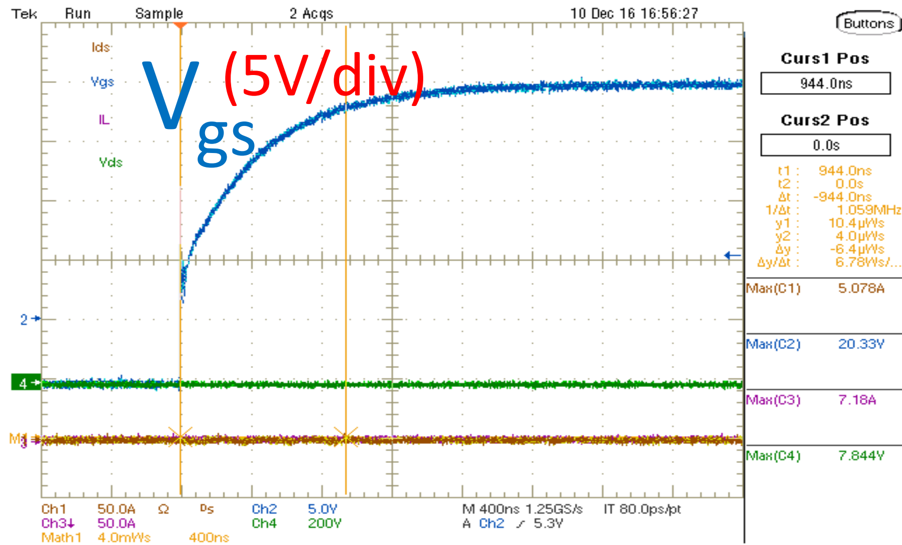

Figure 5-9 V_{gs} waveform without active gating

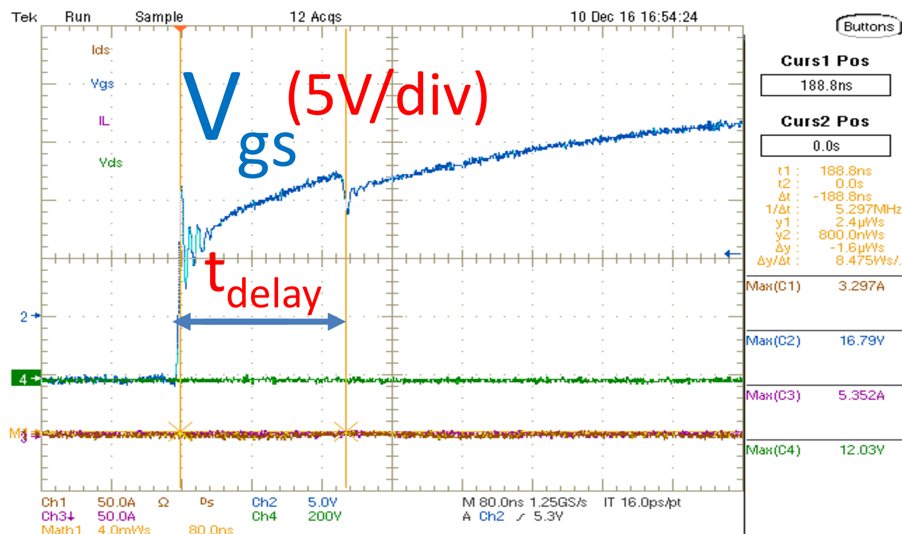

Figure 5-10 V_{gs} waveform for active gate driver

It can be clearly seen that on applying active gating the V_{gs} curve has two slopes. When the active gate driving is actuated at time delay 't_{delay} ', the rate of V_{gs} rise decreases due to switching from lower gate resistance to higher gate resistance. This time delay 't_{delay}' has been used for reporting the switching loss and dv/dt parameters in further sections.

5.4.2 Turn-on Active Gating results

The active gate driver has been used for characterization of 1200V, 300A ROHM SiC MOSFET. For all results, V_{gs} of +20V / -5V has been used. In the two-stage active gate driving, a lower resistance has been used for first stage and a higher resistance has been used for second stage. For first stage, gate resistance is obtained by parallel combination of R_{on1} = 3.9 Ω and R_{on2} = 3.9 Ω which is 1.95 Ω. For second stage, the gate resistance of 3.9 Ω is used.

For active gating, the delay pulse is varied by using trimmer to get different operating points. Using different time deays 't_{delay}' of 131 ns, 142 ns, 152 ns and 163 ns, turn-on loss, peak current, di/dt and dv/dt have been measured for 800V switching.

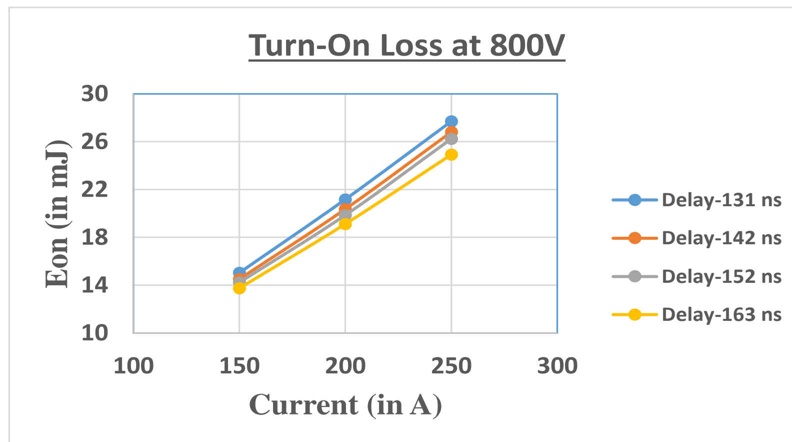

Figure 5-11 Turn-on losses at 800V switching for active gating with different 't_{delay}'

Fig 5-11 shows the turn-on switching loss for different time delays at 800 V switching. While repeating experiments for different time delays, it must be ensured that all the external conditions must remain identical for every test. The turn-on peak current, di/dt and dv/dt have been plotted in Fig 5-12, Fig 5-13 and Fig 5-14 respectively.

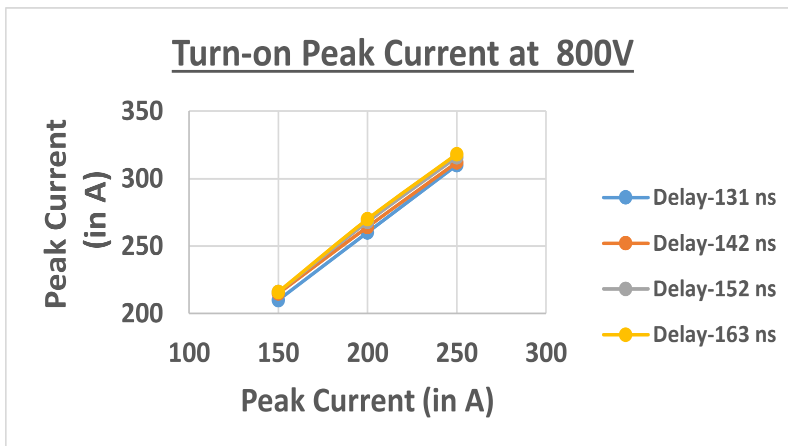

Figure 5-12 Turn-on peak current at 800V switching for active gating with different t_{delay}

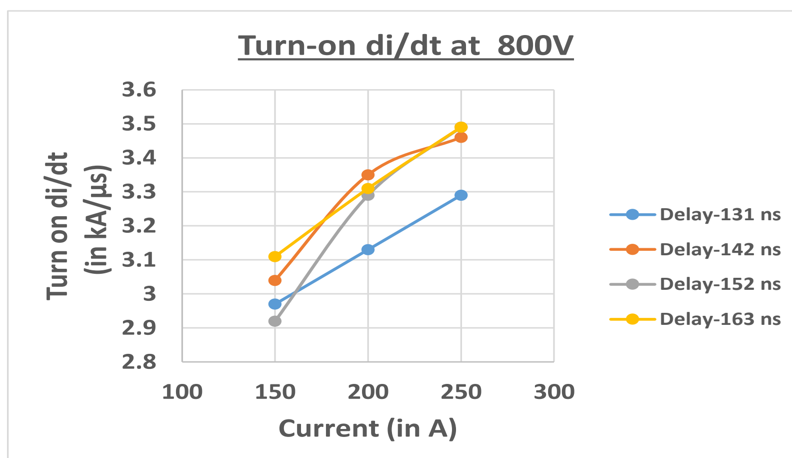

Figure 5-13 Turn-on di/dt at 800V switching for active gating with different t_{delay}

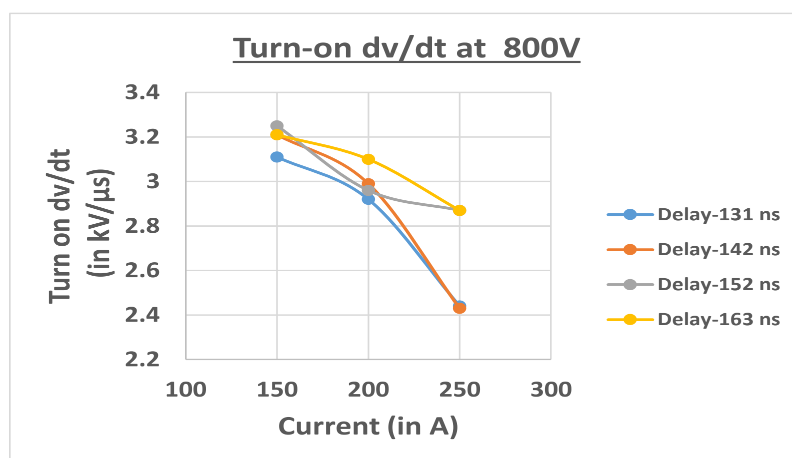

Figure 5-14 Turn-on dv/dt at 800V switching for active gating with different t_{delay}

The optimum time delay for active gating is decided based on following considerations :

i. Switching loss should be lower compared to when R_g of 3.9 Ω is used but higher than that for R_g of 2 Ω.
ii. Turn-on peak current should be comparable or higher than when R_g of 2 Ω is used as gate resistance of 1.95 Ω has been used in first stage of active gating.
iii. Turn-on di/dt should be comparable or higher than when Rg of 2 Ω is used as gate resistance of 1.95 Ω has been used in first stage of active gating. It should be higher than that for R_g of 3.9 Ω.
iv. Turn-on dv/dt should be comparable to when R_g of 3.9 Ω is used and lower than that for R_g of 2 Ω.

It may be observed that the switching losses are lower for higher time delays but it will have higher dv/dt. This is due to fact that with higher time delay, the lower gate resistance operates during current rise time as well as a major chunk of voltage fall time, leading to higher dv/dt. So, careful analysis of results is necessary ensuring they meet the above mentioned considerations for optimum delay time. Based on the analysis, time delay of 163 ns is optimum for turn-on active gating at 800V switching.

Table 5-2 Turn-on Loss (in mJ) Comparison at 800V

Current (in A)	**Eon (in mJ)**				
	At R_g=2 Ω	**At R_g=3.9 Ω**	**With Active Delay-163 ns**	**% Increase from 2 Ω**	**% Reduction from 3.9 Ω**
150	12.2	17.74	13.75	12.70	22.49
200	16.4	24.43	19.12	16.59	21.74
250	19.55	31.36	24.92	27.47	20.54

Table 5-2 tabulates the turn-on switching losses for without active gate driving for 2Ω and 3.9Ω along with that for active gate driving at time delay of 163 ns. It can be seen that turn-on switching losses decrease by ~ 20-22% with active gate driving as compared to that with non-active gate driving for gate resistance of 3.9 Ω.

Table 5-3 tabulates the turn-on peak current for without active gate driving for 2 Ω and 3.9 Ω along with that for active gate driving at time delay of 163 ns. The turn-on peak current for active gate driving is comparable to that for non-active gate driving for gate resistance of 2 Ω as gate resistance of 1.95 Ω has been used for first stage of active gate driving.

Table 5-3 Turn-on Peak Current (in A) Comparison at 800V turn-on

Current (in A)	Peak Current (in A)				
	At R_g=2 Ω	At R_g=3.9 Ω	With Active Delay-163 ns	% Increase from 2 Ω	% Increase from 3.9 Ω
150	216.3	200	216	-0.14	8.00
200	268.4	252	270	0.60	7.14
250	312.6	302.4	318.2	1.79	5.22

Table 5-4 tabulates the turn-on di/dt for without active gate driving for 2Ω and 3.9Ω along with that for active gate driving at time delay of 163 ns. It can be seen that turn-on di/dt with active gating is higher or comparable than that with non-active gate driving for 2Ω since gate resistance of 1.95 Ω is used for first stage of active gating.

Table 5-4 Turn-on di/dt (in kA/us) Comparison at 800V switching

Current (in A)	di/dt (in kA/µs)				
	At R_g=2 Ω	At R_g=3.9 Ω	With Active Delay-163 ns	% Increase from 2 Ω	% Increase from 3.9 Ω
150	2.81	2.14	3.11	10.68	45.33
200	3.21	2.25	3.31	3.12	47.11
250	3.6	2.35	3.49	-3.05	48.51

Table 5-5 Turn-on dv/dt (in kV/us) Comparison at 800V switching

Current (in A)	dv/dt (in kV/µs)				
	At R_g=2 Ω	At R_g=3.9 Ω	With Active Delay-163 ns	% Reduction from 2 Ω	% Increase from 3.9 Ω
150	4.48	3.2	3.21	28.35	0.31
200	4.4	2.58	3.1	29.55	20.16
250	4.27	2.5	2.87	32.79	14.80

Similarly, table 5-5 tabulates the turn-on dv/dt for without active gate driving for 2Ω and 3.9Ω along with that for active gate driving at time delay of 163 ns. As desired, the dv/dt for active

gating is ~28-32% lower than that for non-active gating with gate resistance of 2Ω. Hence, with two-stage gate driving, reduced dv/dt has been achieved with lower switching loss.

The data for switching loss and dv/dt in Table 5-2 and Table 5-5 respectively can be plotted for easier understanding. Fig 5-15 shows the turn-on switching loss for gate resistance of 2Ω (blue) and 3.9 Ω (orange) without active gating and with active gating for a delay of 163 ns. It can be clearly seen that switching losses for active gating are less than that for gate resistance of 3.9 Ω without active gating.

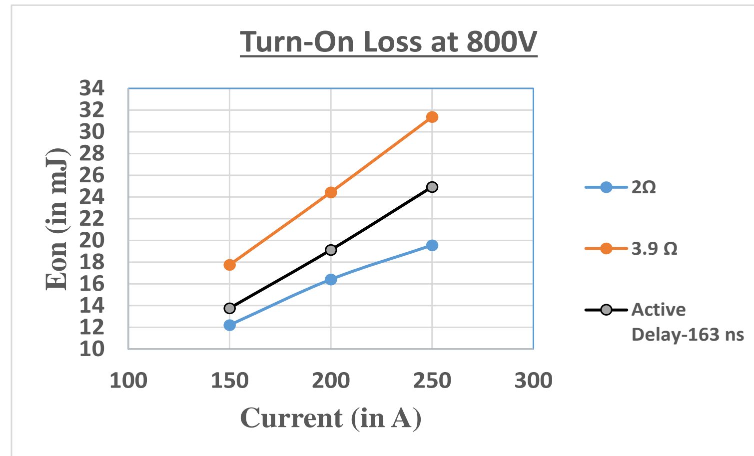

Figure 5-15 Turn-on losses comparison at 800V for active and non-active gate driving

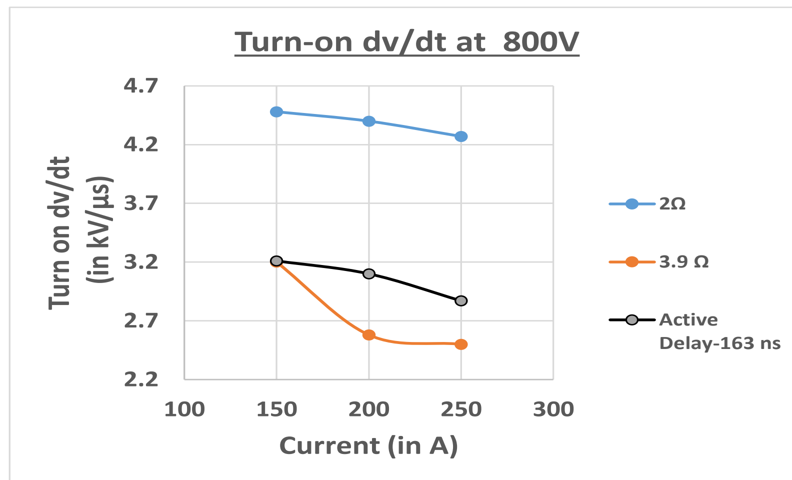

Figure 5-16 Turn-on dv/dt comparison at 800V for active and non-active gate driving

Similarly, Fig 5-16 shows the switching dv/dt at turn-on for gate resistance of 2Ω (blue) and 3.9 Ω (orange) without active gating and with active gating for a delay of 163 ns. It can be clearly seen that dv/dt for active gating is comparable to that for gate resistance of 3.9 Ω without active gating and is less than compared to dv/dt for gate resistance of 2 Ω without active gating.

5.5 Discussion

Two-stage active gating has been implemented to control di/dt in first stage and dv/dt in second stage at turn-on switching transition. Experimental data is obtained for non-active gate driving for gate resistance of 2 Ω and 3.9 Ω. Timing delays are suitably tuned using equation 5.3 for active gating. Experiments are repeated for active gate driving for different delays to find optimum delay operating point. A gate resistance of 1.95 Ω has been used for 1st stage and 3.9 Ω for 2nd stage for active gate driving. Comparison has been tabulated in Table 5-2 to Table 5-5 for switching loss, peak current, di/dt and dv/dt for active gating and without active gating. Using active gating, the turn-on switching loss has been reduced by ~20% for 800V, 250A switching as compared to the non-active gate driving using gate resistance of 3.9 Ω. Similarly, dv/dt has been reduced by ~32% for active gating for 800V, 250 A switching as compared to the non-active gate driving using gate resistance of 2 Ω. This can be used to suppress cross-talk due to high dv/dt associated with SiC devices.

CHAPTER 6

6 Conclusion and Future Work

6.1 Conclusion

Two stage active gate driving has been successfully implemented for controlling turn-on di/dt in first stage and dv/dt in second stage which can be used to suppress cross talk associated with high dv/dt of SiC devices. Analog circuitry consisting of high bandwidth op-amps has been used to achieve turn-on delays of order of 10-200 ns. The propagation delays of opto-couplers, current buffer and auxiliary MOSFET has been taken in account to achieve triggering pulses. However, the complexity of the circuit has greatly increased as delay circuit, auxiliary MOSFET and auxiliary opto-coupler have been used. This also increases the cost of the gate driver at the same time.

6.2 Future Work

Active gating at turn-off can also be explored to achieve the following:

i. Reduce dv/dt to mitigate cross talk due to turn-off dv/dt

ii. Reduce di/dt to minimize turn-off voltage overshoot.

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APPENDIX

Appendix A

Abbreviations

C	: Capacitor
C_{ds}	: Drain to source capacitance
C_{gd}	: Gate to drain capacitance
C_{gs}	: Gate to source capacitance
Di/dt	: Rate of change of current
DPT	: Double Pulse Test
Dv/dt	: Rate of change of voltage
E_{on}	: Turn-on switching loss
E_{off}	: Turn-off switching loss
IGBT	: Insulated Gate Bipolar Transistor
L	: Inductance
MOSFET	: Metal Oxide Semiconductor field-effect transistor
PWM	: Pulse Width Modulation
V_{gs}	: Gate to source Voltage