ABSTRACT

KADAVELUGU, ARUN KUMAR. Medium Voltage Power Conversion Enabled by 15 kV SiC IGBTs. (Under the direction of Dr. Subhashish Bhattacharya).

This work is aimed at experimental evaluation of the state-of-the-art 15 kV SiC IGBTs with the ultimate objective of demonstrating them on medium voltage, high frequency power conversion systems, and investigating techniques for their optimal utilization. As the experimental switching characteristics of the 15 kV SiC N-IGBTs have never been reported, the foremost step to understand the SiC IGBTs was to build a high voltage inductive switching test setup to characterize the 15 kV SiC IGBTs up to 11 kV. The 5 μm field-stop buffer layer N-IGBTs have been found to be more suitable than 2 μm buffer layer N-IGBTs for high frequency power conversion, due to their lower turn-off energy loss and turn-on dv/dt. However, both variants of the N-IGBT have exhibited two-slope switching voltage transitions with steeper transitions over punch-through voltage.

This led to in-house development of high dv/dt immunity, high isolation gate driver for the SiC IGBTs, as the commercially available gate drivers are not capable of handling such high stress. The gate driver has been tested on pulse tests up to 11 kV and over 100 kV/μs. This was followed by evaluation on continuous switching tests by developing different converter circuits to expose the gate driver to 8 kV and 85 kV/μs.

Subsequently, the 15 kV, 5 μm buffer layer SiC N-IGBTs have been evaluated on 10 kV hard-switched boost converter heat-run tests with power dissipation density of 550 W/cm^2 (active area) at the junction temperature of 146^{o}C. This boost converter has been used as a 10 kV dc power source for the subsequent tests. A method to accurately measure the online IGBT junction temperature based on turn-off voltage waveform is provided. The hard-switching frequency limits have been analytically evaluated based on the switching data and thermal resistance of the IGBT module package.

Following the gate driver evaluation and IGBT heat-run tests, a three-level neutral point clamped converter has been developed, and tested up to 10 kV dc input at 10 kHz and 9 kW resistive loading. After this, the IGBTs have been demonstrated on 10 kV, two-level, H-bridge inverter at 5 kHz and 6 kW. This was followed by evaluating 15 kV, multi-chip IGBT

modules and comparing their performance with single-chip IGBT modules. Using the multi-chip IGBT co-pack modules, six three-level poles have been built and validated up to 10 kV dc input, for a three-phase solid state transformer application.

The latter part of the work is focused on extracting optimal performance of the SiC IGBTs for converter applications. The dv/dt of the IGBTs has been investigated with respect to current, temperature and buffer layer thickness. Analytical results of the dv/dt and their comparison with the experimental data are presented for the turn-off dv/dt over punch-through. The passive gate current control technique has been used to reduce the turn-on dv/dt. However, this led to drastic increase in turn-on energy loss, which was addressed by implementing a two-stage active gate driver at 11 kV.

Subsequently, the discrete SiC IGBTs have been evaluated under zero voltage switching (ZVS) conditions using a capacitive snubber. The influence of the voltage spike during ZVS turn-on and the turn-off current bump have been provided. The 5 μm buffer layer IGBTs are found to be better from the perspective of percentage turn-off energy loss reduction, in comparison to the 2 μm buffer layer IGBTs. Lastly, complementary inverter topology using 15 kV P-IGBT and N-IGBT has been investigated for zero dv/dt stressed gate drivers.

Medium Voltage Power Conversion Enabled by 15 kV SiC IGBTs

by
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DEDICATION

To my Parents and Brothers

BIOGRAPHY

Arun Kumar Kadavelugu was born in Korapally, Karimnagar district, of the state of Andhra Pradesh in India. He received his Bachelor of Engineering in Electrical Engineering from Osmania University campus, in 2005. He completed his Master of Technology in Electrical Engineering from Indian Institute of Technology in 2007, with specialization in Power Electronics. From 2008 to 2009, he worked on a standalone renewable system implementation project sponsored by the government of India. In 2009, he joined the Future Renewable Electric Energy Development and Management (FREEDM) systems center, Department of Electrical and Computer Engineering, North Carolina State University to pursue his PhD. His research interests are power conversion using wide band-gap devices, which include 1200 V SiC MOSFETs, 10 kV SiC MOSFETs and 15 kV SiC IGBTs. He worked as an R&D Intern at GE Global Research, Niskayuna, during fall 2011.

ACKNOWLEDGMENTS

Several people have helped me directly or indirectly during the course of my PhD. I am very thankful to each and every one of them. Pardon me, if I have forgot to mention someone explicitly.

Firstly, I take this opportunity to thank my supervisor Prof. Subhashish Bhattacharya for giving me enormous freedom in choosing my work, for his kind support and encouragement, and most importantly for entrusting challenging and exciting responsibilities on me.

I am very grateful to Prof. Jayant Baliga for taking his valuable time to explain the fundamentals of device physics, for the several discussions on the SiC IGBT characteristics, and for the critical comments on my work. I am very thankful to Prof. Iqbal Husain and Prof. Xiangwu Zhang for their kindness in accepting my request to be on my PhD committee, and for the enormous support they provided.

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I need to specially mention my colleagues Gangyao, Arvind, Kamalesh, Sachin, Awneesh, Xu, Fei, Seunghun, Dhaval, Krishna, Ankan, Ritwik, Hesam, Sayan, Edward, Meng-Chia and Woongje for several insightful discussions. I am grateful to Harekrishna, Krishnan Subramanian and Sameer Khan for their help in mechanical design of the high voltage converter prototypes. I am thankful to our lab manager Hulgize for his valuable help in

mechanical design of the converters and for guidance on high voltage safety. I thank our receptionist Karen Autry for her prompt help in component orders.

The invaluable support and encouragement provided my roommates and their spouses is highly appreciated. My special thanks to Prasenjit, Ajay-Sandhya, Boopathy-Vijji, Samir-Swastika, Kasu-Jayashree, Kiran and Hemanth. I thank all my friends from Osmania University, IIT Kanpur and FREEDM center for their encouragement.

Finally, the immense support and guidance from my family has been a very great help. Their critique of my career choices and their toleration have an important role. It needs a special mention that my father and younger brother have motivated me to work hard.

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Chapter 1
Introduction

1.1 Background

The silicon (Si) MOSFETs and IGBTs are most widely used power semiconductor devices today. MOSFETs are suitable for high switching frequency but are typically limited to a kilo-volt in practical applications due to increase in on-resistance resulting from the unipolar physics. On the other hand, IGBTs are attractive over a wide range of voltages, beginning from about 600 V to 6.5 kV (device blocking voltage) owing to their bipolar physics of operation with simple MOS gate control. The development of further higher voltage Si IGBTs is limited by increased energy losses resulting from the fundamental material properties of Si.

At this juncture, 4H-SiC has been found to be a viable alternative due to its much wider band-gap. The several fold increase in critical electric field in comparison to Si makes it feasible to build high voltage unipolar devices with extremely low resistance as predicted by Baliga's figure of merit [1]. The better thermal conductivity properties of SiC is another factor of considerable importance which is critical in heat removal process [2]-[3]. The high temperature capability of SiC, due to its wider band-gap, is another attractive feature.

These unique advantages of SiC led to development of MOSFETs beyond 10 kV [4]-[5]. The 10 kV SiC MOSFETs have been demonstrated on a single-phase 1 MVA soft-switched Solid State Power Substation (SSPS) by GE in the year 2010 – 2011 [5]. The 13 kV SiC MOSFETs have been demonstrated on a 20 kVA single-phase Solid State Transformer (SST) by FREEDM Center at North Carolina State University [6]-[7].

However, similar to the case of silicon, as the voltage is scaled-up, IGBT is more efficient due to its bipolar physics with MOS gate structure. Therefore, significant research effort has been spent in the recent years to develop high voltage 4H-SiC IGBTs. Due to difficulty in producing low resistivity P+ substrate, the initial SiC IGBTs have been developed with P-channel (using

N+ substrate) [8]. However, with advances in SiC technology, low resistivity P+ substrates have been developed leading to the development of SiC N-IGBTs [9]. The characteristics of 12.5 kV N-IGBTs and 15 kV P-IGBT have already been reported up to switching voltage of 8 kV [10]. However, there has been no literature on converter design and demonstration using these ultrahigh voltage SiC IGBTs.

The objective of this thesis is to understand the state-of-the-art 15 kV SiC N-IGBTs with emphasis on the design considerations for optimal and reliable application to high power conversion. As SiC N-IGBTs over 20 kV are being developed [11], understanding behavior of the 15 kV devices is crucial in paving way for scaling up the design techniques for their application in power conversion systems.

1.2 Outline of this Dissertation

This thesis is organized as follows.

Chapter-1 provides the prior art of the research on high voltage SiC power semiconductor devices and their demonstration, followed by motivation of the work presented in this thesis.

Chapter-2 begins with the switching characterization of the 15 kV SiC N-IGBTs up to 10 kV and 175^{o}C under inductive, partly inductive and resistive loads. A comparison of 2 μm and 5 μm field-stop buffer layer N-IGBTs is provided. This is followed by a short discussion on understanding the design considerations of power conversion system using these devices.

Chapter-3 presents the gate driver design and its evaluation as per the requirements determined in switching tests presented in Chapter-2. Different test circuits are built to validate the gate driver in continuous switching tests and the robustness evaluation results of the gate driver are provided.

Chapter-4 is devoted to demonstrating the 5 μm buffer layer 15 SiC N-IGBTs. The SiC IGBT is first demonstrated on 10 kV boost converter heat-run tests. This was followed by three-level

NPC converter demonstration with 10 kV dc-input in inverter mode with sine-PWM and square-PWM modulation. The performance of multi-chip IGBT module is also provided.

Chapter-5 presents analysis of the dv/dt generated by the SiC IGBTs, with varying collector current, temperature and buffer layer thickness, based on the experimental evaluation. The latter part of the chapter is devoted to development of two-stage active gate driver to minimize turn-on dv/dt without increasing energy loss.

Chapter 6 is continuation of the investigation on optimal performance of the SiC IGBTs. The behavior of the IGBTs under zero voltage switching conditions is evaluated under different conditions. This is followed by understanding its impact on soft-switched converter applications.

Chapter 7 provides investigation on the 15 kV SiC P-IGBT and N-IGBT based complementary inverter to have zero dv/dt stress on the gate drivers.

Chapter 8 summarizes the contributions of the work and future research direction on this subject.

Chapter 2
Hard Switching Characterization of 15 kV SiC N-IGBTs

2.1 Introduction

In [10], switching characteristics of 12.5 kV SiC N-IGBTs and 15 kV SiC P-IGBTs have been reported up to 8 kV. The 15 kV SiC N-IGBTs are the state-of-the-art devices whose switching characteristics have never been reported previously. Moreover, it is important to experimentally validate the switching behavior of the 15 kV SiC N-IGBTs at least up to 10 kV considering their operation in a power converter system due to voltage surges and overhead incorporated for the protection circuitry. Also, the turn-on switching characteristics of the SiC IGBTs and their influence on power converter design have never been reported. Therefore, a high voltage switching test setup has been built with nominal rating of 12 kV (with peak voltage of 14 kV) to characterize the 15 kV SiC IGBTs for both turn-on and turn-off at different temperature. The 15 kV SiC N-IGBTs are designed and built by Cree, and the packaging and static (forward conduction and leakage) characteristics are provided by Powerex.

2.2 The 15 kV SiC N-IGBT

The simplified cross-sectional view of the 15 kV SiC N-IGBT is shown in Fig. 2.1. The drift layer is 140 μm thick with doping concentration of $2x10^{14}$ cm^{-3}. The IGBT used for the characterization has a buffer layer thickness of 5 μm, and its chip area is 0.84cmx0.84cm, with an active area of 0.32 cm^2. Fig 2.2 shows the co-pack module with the 15 kV SiC IGBT with 20 kV (2x10 kV) SiC JBS diodes. The current-sense resistors and the thermistor integrated in the module for over current and temperature protection are seen in the figure. The forward

conduction and leakage characteristics of the IGBT are provided by powerex, and are shown in Appendix.

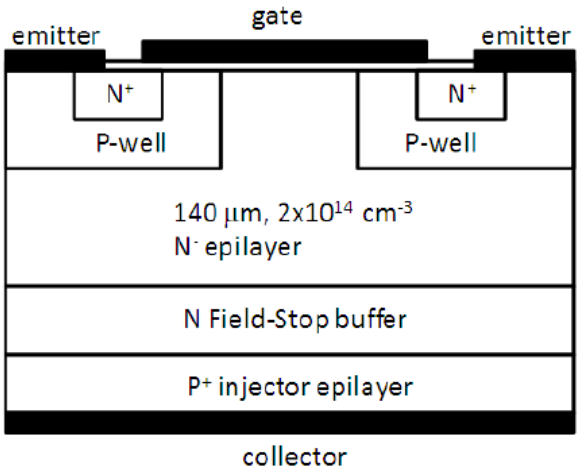


Fig. 2.1: Simplified cross-sectional view of 15 kV SiC N-IGBT

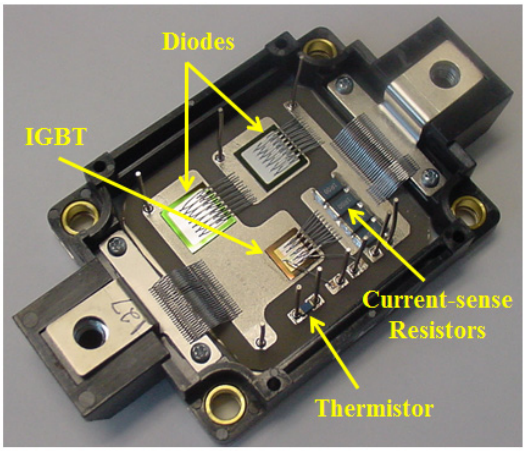


Fig. 2.2: 15 kV SiC N-IGBT co-pack module

2.3 Hard-switching Characteristics

In this section, fully hard-switching characteristics of the 15 kV, 5 μm buffer layer IGBT are presented for purely inductive, partly inductive and fully resistive load conditions up to 10 kV. The turn-on gate resistance, $R_{G(ON)}$, used is 20 Ω, and the turn-off gate resistance, $R_{G(OFF)}$, used is 10 Ω. The IGBT voltage is measured using Tektronix 20 kV, 75 MHz single-ended probe, and the IGBT current is measured using a pearson coil of 20 MHz bandwidth. The 500 MHz oscilloscope is set to 150 MHz for the voltage measurement and 20 MHz for the current measurement.

2.3.1 Clamped-Inductive Load Switching Conditions

The clamped inductive (or fully hard-switched) characteristics are most widely provided data for power semiconductor devices to cover majority of applications. The circuit schematic of the double-pulse test circuit is shown in Fig. 2.3. The freewheeling diode used in the switching tests is 20 kV SiC JBS diode module (2x10 kV, 10 A diodes in series). The load is a single-layer, 8 mH inductor (two 4 mH inductors in series) with saturation current of 30 A (shown in Fig. 2.4) and with ultralow inter-winding capacitance (estimated to be < 10 pF). Experiments have been performed at 10 kV with varying current and temperature.

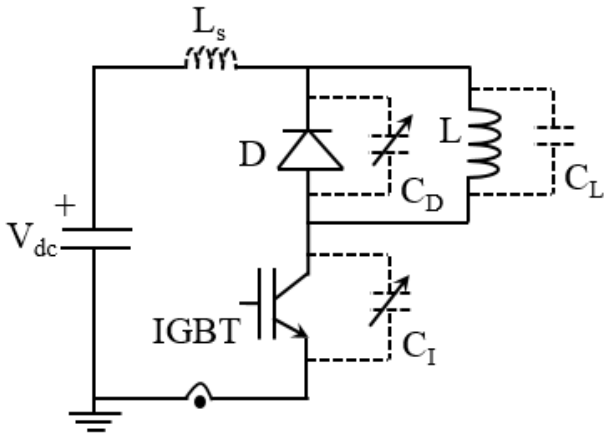


Fig. 2.3. The double-pulse test circuit schematic with different parasitic components

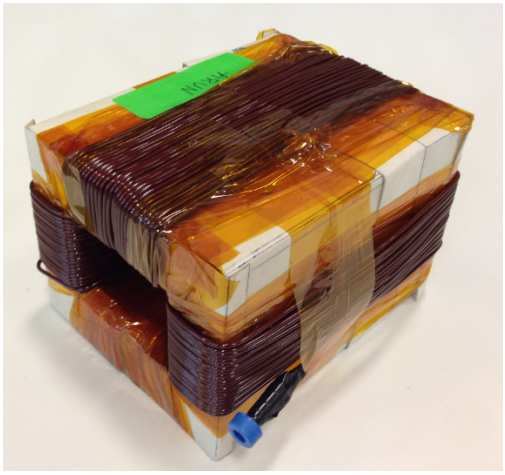


Fig. 2.4: The high voltage, low capacitance, HV load inductor (4 mH, 30 A). Two of them have been used in series for the switching characterization tests.

Fig. 2.5 shows turn-on switching loss (E_{ON}) and turn-off switching loss (E_{OFF}) at 25°C, at 10 kV, 2 A to 10 A. Unlike the turn-on loss, the turn-off loss is weakly dependent on the current. Fig. 2.6 shows the turn-off transitions at 10 kV, 5 A, and 10 A at 25°C. The duration of the 10 A transition is about 60 % of that of the 5 A transition, resulting in very slight variation of energy loss from 5 A to 10 A. The temperature dependency of the turn-off loss is shown in Fig. 2.7. The energy loss is increased to a factor of three from 25°C to 175°C, due to increased injection at higher temperature resulting in significantly larger amounts of charge in the drift region. As shown in Fig. 2.8, the larger amount of charge to be removed at higher temperature is slowing down the voltage rise (before punch through) which in consequence is resulting in higher energy loss. The switching energy losses reported in the entire thesis are calculated online using the oscilloscope math function, $\int v.i.dt$ on IGBT voltage and current.

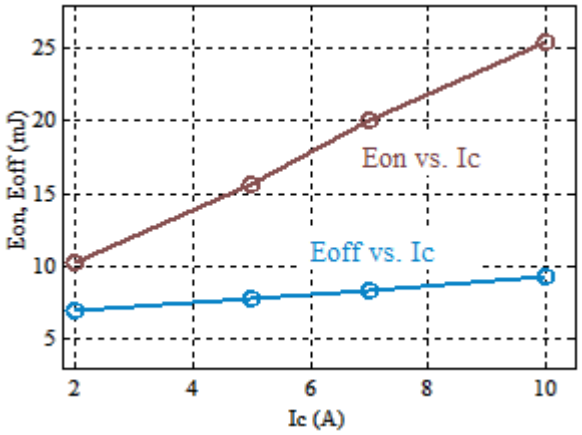


Fig. 2.5: Turn-on and turn-off energy loss values with current variation at 10 kV and 25ºC, under clamped inductive load.

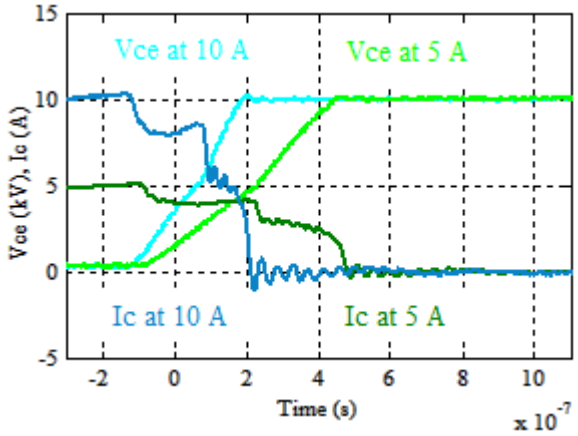


Fig. 2.6: Turn-off switching transitions at 10 kV, 25ºC, 5 A and 10 A, under clamped inductive load conditions.

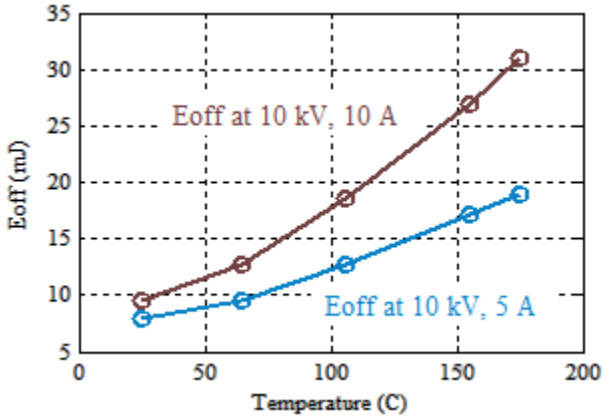


Fig. 2.7: Turn-off switching loss variation with temperature at 5 A and 10 A at 10 kV, under clamped inductive load conditions.

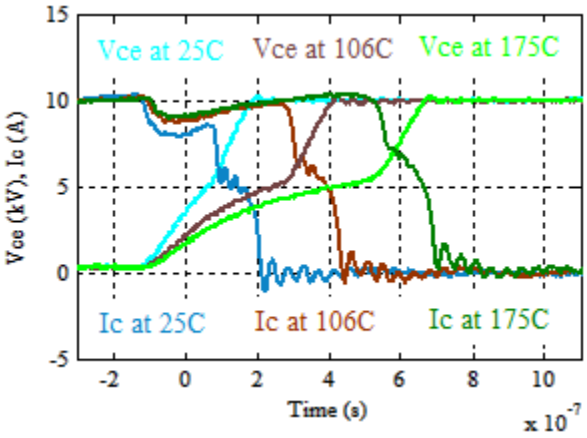


Fig. 2.8: Turn-off switching transitions with temperature at 10 kV and 10 A, under clamped inductive load conditions.

The turn-off loss at different temperature values is summarized in Table 2.1. The hot plate was allowed to reach steady state for an hour before characterizing the switching transient at a particular temperature. The difference in reading between the hot plate display and the thermistor mounted in the IGBT module (shown in Fig. 2.2) are provided in the table. The thermistor (rated for 150^{o}C) temperature values are taken as reference for the entire study. The turn-on energy loss is not as strongly dependent on temperature as shown in Fig. 2.9. The

$R_{G(ON)}$ used is 33 Ω for the temperature dependency turn-on loss characterization, unlike the rest of the experiments which were conducted with $R_{G(ON)}$ of 20 Ω . The use of 20 Ω $R_{G(ON)}$ has damaged the hot-plate used for the characterization, most probably due to the EMI. Therefore, the turn-on loss behavior at high temperature is evaluated with higher gate resistance of 33 Ω. Based on the results shown in Fig. 2.9 and Table 2.2, the turn-on energy loss is not drastically varying with temperature, unlike the turn-off energy loss.

Table 2.1: Inductive turn-off energy loss values at 10 kV, 5 A and 10 A.

Hot-plate Setting	**Thermistor Reading**	**E_{OFF} at 10 kV, 5 A**	**E_{OFF} at 10 kV, 10 A**
25ºC	26ºC (Measured)	8.0 mJ	9.6 mJ
75ºC	65ºC (Measured)	9.6 mJ	12.7 mJ
125ºC	106ºC (Measured)	12.7 mJ	18.6 mJ
175ºC	155ºC (Measured)	17.2 mJ	27.0 mJ
195ºC	175ºC (Estimated)	19.0 mJ	31.0 mJ

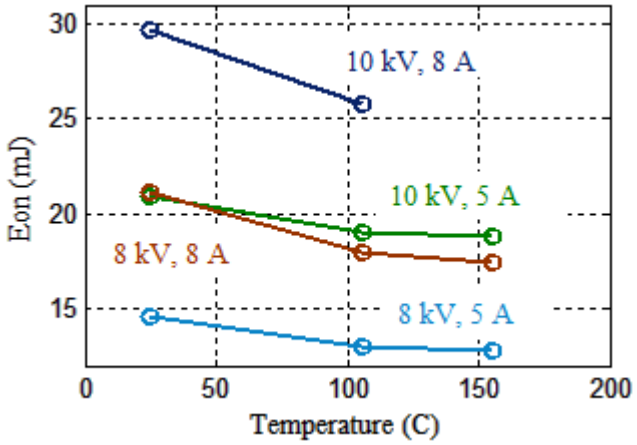


Fig. 2.9: The turn-on energy loss variation of 15 kV N-IGBT with temperature with $R_{G(ON)}$ = 33 Ω.

Table 2.2: Turn-on energy loss variation of 15 kV N-IGBT with temperature

Voltage and Current	**E_{ON} at 25°C**	**E_{ON} at 106°C**	**E_{ON} at 155°C**
8 kV, 5 A	14.6 mJ	13.0 mJ	12.8 mJ
8 kV, 8 A	21.1 mJ	18.0 mJ	17.4 mJ
10 kV, 5 A	20.9 mJ	19.0 mJ	18.8 mJ
10 kV, 8 A	29.7 mJ	25.8 mJ	N/A

2.3.2 Partly Inductive Load Switching Conditions

The majority of the power converter applications fall into the fully hard-switching category due to the high L/R time constants of the RL loads. The hard-switching characteristics provided in the previous subsection address this category. For very high L/R loads, as the time constant is very large in comparison to the switching duration, the behavior corresponds to the fully inductive load conditions. However, some applications like dual active bridge converters with high frequency transformers have low L/R time constant loads, where the assumption of fully

inductive load is not valid particularly under light load conditions. To understand the behavior of the IGBT under those conditions, a 1 kΩ resistance in series with the 8 mH inductor (8μs time constant) is used as the load in this subsection.

Based on the 25ºC turn-on and turn-off transitions shown in Fig. 2.10 and Fig. 2.11 respectively, at 10 kV and 5 A, the RL load is behaving almost as the purely inductive load at 25ºC, except for slightly lower peak during turn-on and slower transition during turn-off. The reason for this behavior is the longer time constant of the RL load in comparison to the switching transition duration. The slower turn-off transition is due to the inductive energy dissipation during the switching transition causing reduced load current. It must be noted that the effects of RL nature of the load would have been dominant during the turn-off transition if the measurements were made at higher temperature due to longer switching transition duration.

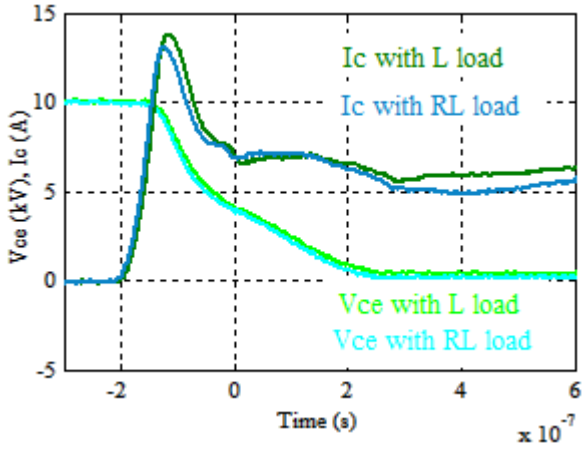


Fig. 2.10: Comparison of turn-on transitions with L and RL loads at 10 kV and 5 A, at 25ºC.

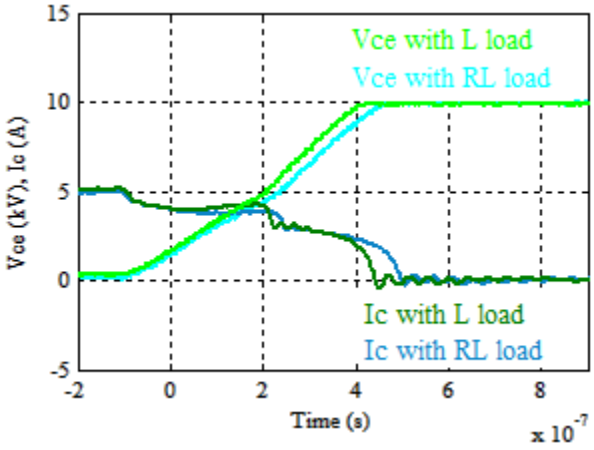


Fig. 2.11: Comparison of turn-off transitions with L and RL loads at 10 kV and 5 A, at 25ºC.

2.3.3 Resistive Load Switching Conditions

This switching characterization is done with 2 kΩ wire-wound resistor (with stray inductance of 0.3 mH) at 10 kV and 5 A. The tests at other load currents are conducted by appropriately scaling the load resistance values for the desired current value. Unlike the case for RL load, the R load presents significantly different turn-on and turn-off characteristics in comparison to the purely L load characteristics. The current spike is significantly reduced due to zero current turn-on, and also probably due to absence of load capacitance. The resistive turn-on and turn-off transitions at 10 kV, 5 A and 25ºC are compared with corresponding inductive characteristics in Fig. 2.12 and Fig. 2.13 respectively. The turn-on and turn-off energy loss comparison with the different loads is provided in Fig. 2.14 and Fig. 2.15 respectively. The L and RL loads have almost same amount of energy loss during turn-on and turn-off transitions. The zero current turn-on is resulting in same energy loss at different currents with the R load. The energy dissipation (load current reduction in the R load) during turn-off transition reduces IGBT current and consequently the turn-off loss, in comparison to that with L or RL load.

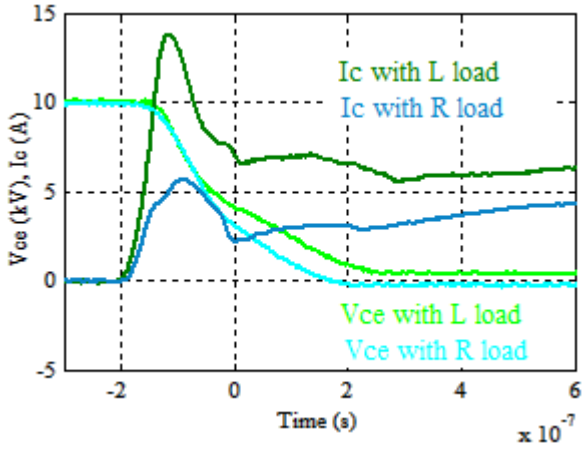


Fig. 2.12: Comparison of turn-on transitions with L and R loads at 10 kV and 5 A, at 25ºC.

The resistive load does not find wide real-time application. However, the characteristics are provided to show behavior of the IGBT under all possible loads. The heating applications where pure R load conditions are seen, are realized by using a series capacitor (for resonance) to cancel the impedance offered by the stray inductance of the coils.

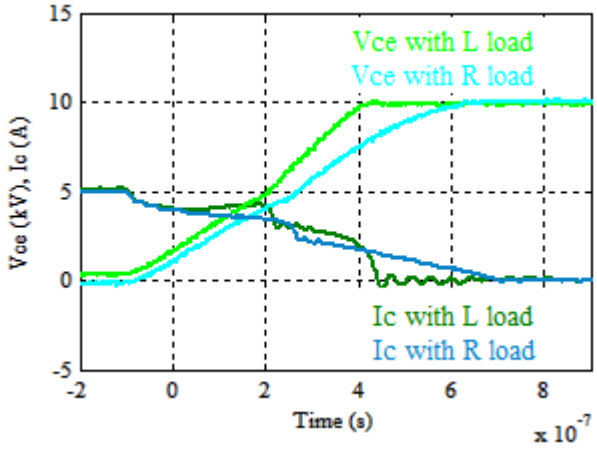


Fig. 2.13: Comparison of turn-off transitions with L and R loads at 10 kV and 5 A, at 25ºC.

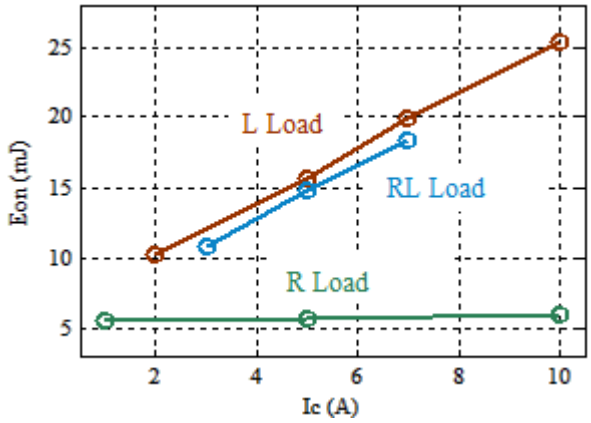


Fig. 2.14: Comparison of turn-on energy loss with L, RL and R loads at 10 kV and 25°C.

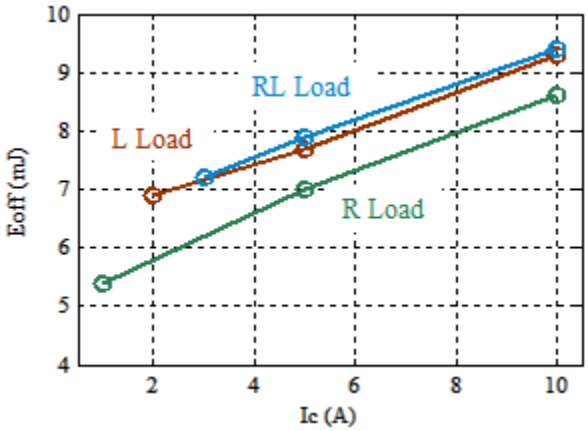


Fig. 2.15: Comparison of turn-off energy loss with L, RL and R loads at 10 kV and 25°C.

2.4 Comparison of 15 kV 5 µm and 2 µm buffer layer N-IGBTs

The 15 kV SiC N-IGBT characteristics reported in the earlier section has 5 µm thick field-stop buffer layer (refer cross-sectional view of the IGBT shown in Fig. 2.1). This section is devoted to understanding the characteristics of the SiC IGBT, from an application perspective, if the field-stop buffer layer thickness is varied.

The forward conduction characteristics of both the 15 kV SiC IGBT are provided in Appendix. The reduction in buffer layer thickness from 5 µm to 2 µm has reduced the conduction drop from 7.2 V to 6.0 V at 20 A. Both the IGBTs have been designed with same drift layer parameters and same buffer layer doping, except for its thickness. Fig. 2.16 shows turn-off transition of 2 µm and 5 µm buffer layer IGBTs at 10 kV and 10 A. The turn-off transition of the 5 µm buffer layer IGBT is much faster than that of the 2 µm buffer layer IGBT, due to reduced injection, explained in Chapter-5.

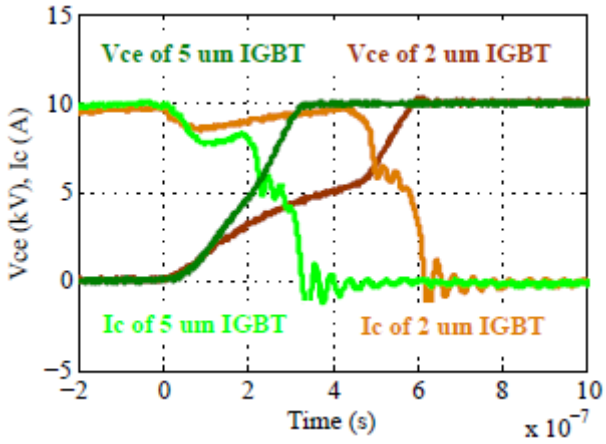


Fig. 2.16: Turn-off transitions of 15 kV, 2 µm and 5 µm thick buffer layer, SiC IGBT at 10 kV, 10 A, 25°C with $R_{G(OFF)}$ of 10 Ω.

The turn-on transitions of both the IGBTs at 10 kV, 8 A are shown in Fig. 2.17. The 2 µm IGBT has significantly larger dv/dt above the punch-through voltage resulting in a large current spike due to discharge of the capacitance of the free-wheeling diode of the clamped inductive test circuit. It should be noted that the current waveform of the 2 µm buffer layer IGBT is scaled to 0.33x in Fig. 2.17. The ringing in the gate voltage is due to the high di/dt probe pickup resulting from the discharge of the capacitance of the free-wheeling diode. Table 2.3 summarizes dv/dt values of both the devices at 25°C with $R_{G(ON)}$ = 50 Ω and $R_{G(OFF)}$ = 10 Ω. Table 2.4 summarizes energy loss values of both the IGBTs. Based on the data shown in these two tables, the thicker buffer layer IGBT has significantly lower turn-off loss and turn-on dv/dt

(over punch-through voltage). However, the conduction drop is moderately increased due to the thicker buffer layer. Thus, the 5 µm devices are more suitable for high frequency, high voltage power conversion. Fig 2.18 shows the high voltage double-pulse switching test setup used for characterizing the SiC IGBTs.

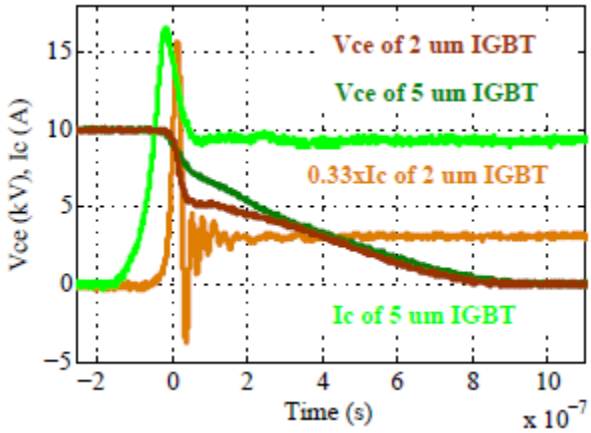


Fig 2.17: Turn-on transitions of 15 kV, 2 µm and 5 µm thick buffer layer, SiC IGBT at 10 kV, 8 A, 25°C with $R_{G(ON)}$ of 50 Ω (The 2 µm IGBT current is scaled down to 0.33x to accommodate the current spike).

Table 2.3: dv/dt of 2 µm and 5 µm IGBTs at 10 kV, 8 A (turn-on) and 10 A (turn-off)

Parameter	**2 µm IGBT (kV/µs)**	**5 µm IGBT (kV/µs)**
Turn-on dv/dt (above PT)	135	39
Turn-on dv/dt (under PT)	7.3	9.0
Turn-off dv/dt (before PT)	12	30
Turn-off dv/dt (after PT)	39	47

Table 2.4: Energy loss values of 15 kV, 2 µm and 5 µm SiC IGBTs

Parameter	2 µm IGBT (# 153)	5 µm IGBT (# 164)
Forward drop at 20 A, 25°C (V_{GE} = 20 V)	5.52 V	7.12 V
Turn-off energy loss at 10 kV, 10 A and 25°C ($R_{G(ON)}$ = 10 Ω)	20.4 mJ	7.2 mJ

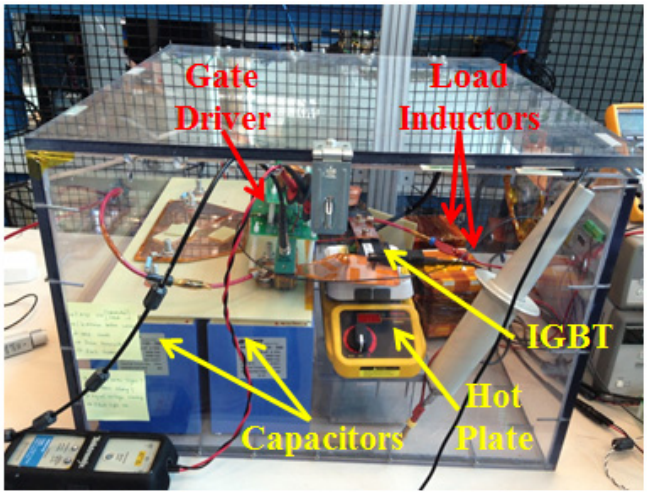


Fig. 2.18: Double pulse tester (14 kV peak) used for characterizing the IGBTs (High voltage capacitors, IGBT under test, gate driver, hot plate and HV load inductors are shown).

2.5 Power converter design considerations

The fundamental advantage of the 15 kV IGBT is simplification of the converters' topology, minimizing the converter system footprint, while considerably improving the efficiency and reliability. However the high dv/dt resulting from the deep punch-through design and the resulting turn-on current spike requires careful design of the converter system, particularly for the thinner field-stop buffer layer IGBT.

The high dv/dt (shown in Fig. 2.19) requires an ultralow coupling capacitance in the isolation power stage of the gate driver for common-mode noise immunity. The complete details of the gate driver design are provided in Chapter-3.

The turn-on di/dt (shown in Fig. 2.20) is in the order of 1 kA/µs, which can induce 1 V/nH (volt per nano Henry) in a nearby inductive loop in the control signal carriers or the printed circuit boards. The spurious tripping of the power converters system due to this di/dt noise needs to be minimized by using very low ESL decoupling capacitors. Similarly, the dv/dt of 100 kV/µs would generate 100 mA/pF (milli-ampere per pico-farad) ground current spikes due to the common mode capacitances of the converter system. The dv/dt induced common mode current should be minimized by reducing the coupling capacitances, or by constraining a path for these currents as discussed in the Chapter-4.

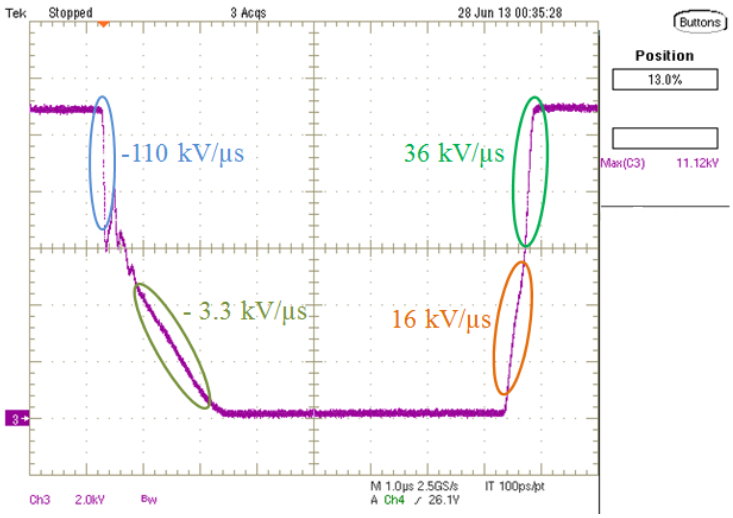


Fig. 2.19: Turn-on and turn-off switching voltage transitions with dv/dt values at 11 kV, for the 2 µm buffer layer thick 15 kV N-IGBT

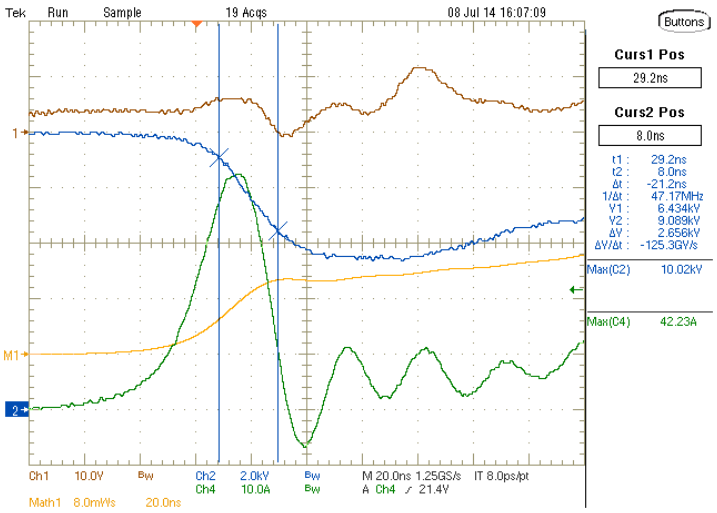


Fig. 2.20: The current turn-on spike of 15 kV, 20 A, 2 µm buffer layer IGBT at 10 kV, 8 A and 25°C [Ch4 (Green): 10 A/div; time: 20 ns/div]

2.6 Summary

A 14 kV double-pulse switching test setup has been built to characterize the 15 kV SiC N-IGBTs. The turn-on and turn-off switching tests are done up to 10 kV and 175°C with inductive, partly inductive and resistive load conditions. The 15 kV, 5 µm IGBT has negligible tail current with switching duration of about 800 ns at 10 kV, 10 A and 175°C. Based on the comparison of 5 µm buffer layer and 2 µm buffer layer IGBT, the 5 µm buffer layer IGBT is more suitable for high frequency power conversion due to lower turn-off loss and turn-on dv/dt, with almost equal dv/dt during turn-on and turn-off. The considerations for power converter design using these ultrahigh voltage devices, which exhibit two-slope voltage transitions during turn-on and turn-off, are provided. These results are basis for the gate driver development, IGBT heat-run tests and converter demonstrations presented in the next chapters.

Chapter 3
Gate Driver Design and Development for 15 kV SiC N-IGBT

3.1 Introduction

As outlined in Chapter-2, the 15 kV SiC IGBTs, particularly the 2 μm field-stop buffer layer IGBT generates dv/dt over 100 kV/μs at the beginning of the turn-on switching transition. The high voltage and the high dv/dt present unprecedented challenges for designing the gate driver for these ultrahigh voltage IGBTs. The commercially available gate driver isolation power supplies have a maximum dielectric test voltage (50 Hz, 1 minute) of 18 kV rms [12]. These power supplies are meant for application to high voltage (4.5 kV or 6.5 kV) Si IGBTs based multilevel converters, where the dv/dt values and switching frequencies are expected to be considerably lower than that with the 15 kV SiC IGBTs. In [13], the high isolation gate driver design has been presented for 10 kV SiC MOSFETs. The ferrite-core isolation transformer is tested up to 26.8 kV dc while superposing 6.5 kV high frequency (non-square wave, low dv/dt) pulses. This gate driver is expected to withstand dv/dt of 50 kV/μs, which is generated by the 10 kV SiC MOSFETs. The gate driver was demonstrated on a solid state transformer (SSPS) [5], where the dv/dt values are lower than 50 kV/μs, due to soft-switched circuit. On the other hand, gate driver with 240 kV/μs dv/dt capability has been demonstrated at 400 V using PCB integrated capacitive coupling method [14]. However, the 15 kV SiC IGBTs present a different scenario with dv/dt greater than 100 kV/μs, and operating voltage up to 11 kV. Therefore, it is important to understand the available techniques to build a gate driver for these operating conditions including proper selection of logic ICs and voltage levels for good noise immunity. Also, the validation of the gate driver in high voltage, hard-switched, high frequency, high dv/dt test circuits is another critical element which is being addressed in this chapter.

3.2 Gate Driver Development

3.2.1 Design Criteria

The clamped inductive turn-on and turn-off switching voltage transitions of the 15 kV, 20 A, 2 µm field-stop buffer layer IGBT at 11 kV are shown in Fig. 3.1 (this figure is provided in chapter-2, but given again here due to its relevance to the topic). The turn-on device current is 5 A with gate resistance of 200 Ω (used to limit the dv/dt) and turn-off current is 10 A with gate resistance of 10 Ω. The turn-on dv/dt is high at the beginning of the transition, followed by a very slow fall in the voltage. The initial high dv/dt is due to extremely low depletion capacitance of the IGBT. About 6 kV, as the IGBT enters into diffusion mode (where the capacitance is significantly higher) the dv/dt is much lower. The high turn-on gate resistance, $R_{G(ON)}$ used for limiting the initial dv/dt has significant influence in slowing down the dv/dt in the diffusion mode. The turn-off transition also has two different slopes with higher dv/dt over the punch through voltage. Limiting the turn-on dv/dt using a higher $R_{G(ON)}$ would drastically increase energy loss. Therefore, the isolation stage of the high-side gate driver should be designed to handle this high dv/dt and high voltage.

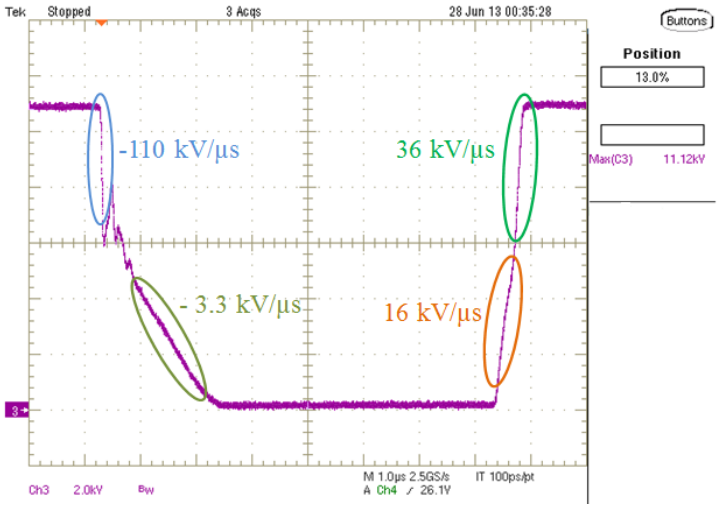


Fig. 3.1: Turn-on and turn-off switching voltage transitions with dv/dt values at 11 kV, for the 2 µm buffer layer thick 15 kV N-IGBT (same as Fig. 2.19 shown in Chapter-2)

It has been determined to employ dc-dc isolation power supply for power isolation, and an optical transfer for signal isolation for designing the gate driver. This method has no duty cycle limitation to provide the bipolar gate voltages (typically +20V and -5V) and transformer saturation issues like in realizing the gate driver using the pulse transformers. There have been techniques proposed to address the transformer saturation [15]-[16], but they would increase the complexity of the gate driver design. Also, the need for high isolation with low coupling capacitance, to handle high dv/dt, increases leakage inductance which distorts the signal in the case of pulse transformers. However, using separate power isolation and signal isolation increases cost, which is of minor concern for these high voltage SiC IGBTs, which are suitable for over 100 kW applications, and the reliable operation of the gate driver is the foremost consideration. The design details of the isolation stage are discussed in the next subsections.

3.2.2 High Isolation Power Supply Design

The high isolation dc-dc power supply is designed with the circuit schematic shown in Fig. 3.2. The primary side H-Bridge provides a 50 kHz square wave to the isolation transformer. The two secondary windings have individual diode rectifier stages to generate +20 V supply for turn-on and -5 V supply for turn-off. There is absolutely no galvanic connection between the primary and secondary windings of the isolation stage, as the diode rectifier stages do not need any control supply (unlike the H-Bridge on the primary side).

The isolation transformer for this application has been studied using several off-the-shelf core materials and sizes with toroid shape. The cores that have been used for the study are shown in Fig. 3.3 and their properties are listed in Table. 3.1. The powder cores (high flux and kool mu) have been chosen to build the initial version of the isolation transformer due to their high $B_{max,}$ which minimizes the core size as given by equation (3.1). However, the transformer was drawing relatively large magnetizing current, due to very low relative permeability as shown by equation (3.2), which was thermally loading the logic ICs used for generating the high frequency square wave. Therefore, the transformer was redesigned with a nano-crystalline core, which reduced the magnetizing current to a low value due to its very high permeability.

However, in the later iteration, ferrite core has been chosen due to its high permeability and lower cost, which is the most optimal material for this application.

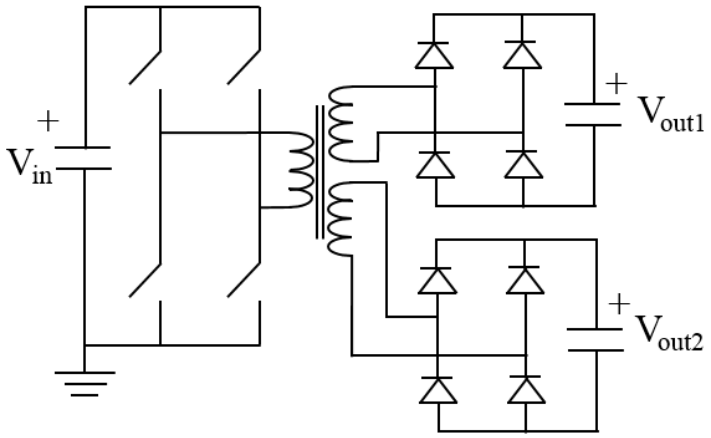


Fig. 3.2: Circuit schematic of the isolation stage of the gate driver.

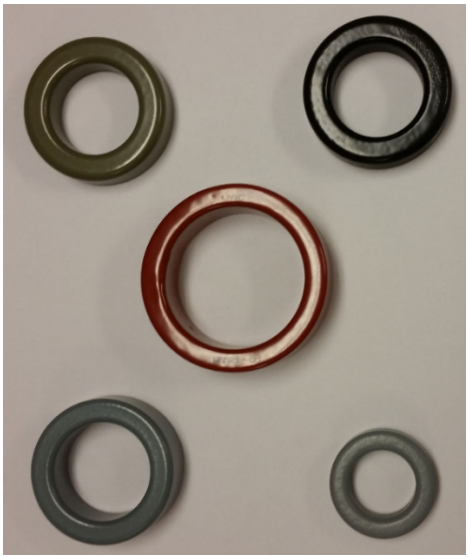


Fig. 3.3: The cores evaluated for the isolation stage design of the high voltage gate driver. High flux (top left), Kool Mu (top right), Nano crystalline (center), Ferrite (bottom both).

Table 3.1: Specification of the different cores evaluated for the high isolation transformer.

Core	μ_r	B_{max}	Outer diameter /Inner diameter	Height
High Flux	60	1.50 T	51.7mm/ 30.9mm	14.4 mm
Kool Mu	60	1.05 T	51.7mm/ 30.9mm	14.4 mm
Nanocrystalline	40,000	1.20 T	65.6mm/ 46.6mm	22.8 mm
Ferrite (normal)	10,000	0.43 T	49.1mm/ 33.8mm	15.9 mm
Ferrite (small)	10,000	0.43 T	36 mm/ 23 mm	10 mm

The size of the core is a very critical parameter in determining the inter-winding coupling capacitance. This was the reason why different sizes of ferrite have been investigated. But the larger size ferrite (bottom left in Fig. 3.3) was chosen to have higher safety margin from the perspective of isolation (corona discharge) between primary and secondary windings. Initially, high isolation has been achieved using high voltage wire, as shown in Fig. 3.4. However, the thicker insulation of the wire made it difficult to put large number of turns on the core, which is critical to reduce the magnetizing current. Therefore, the next version of transformer has been built by placing the insulation on the core with kapton polymide tape and using low voltage (thin) wire with increased number of windings. This helped in achieving flexibility in the transformer design, with reduced magnetizing current while achieving sufficient clearance between the windings. The low voltage wire is sufficient as the voltage per turn is low, and the high inter-winding voltage is possible due to high insulation provided by the kapton tape. The final version of the isolation transformer is designed by the ferrite core (shown in bottom left of Fig. 3.3). Fig. 3.5 shows the inter-winding coupling capacitance measured by an Agilent precision impedance analyzer. The capacitance is 3.4 pF and 13 pF at 50 MHz and 100 MHz respectively. Such low capacitance is critical to maintain signal integrity under the high dv/dt conditions.

$$B_{max}NA > LI_p \qquad (3.1)$$

$$L = \mu N^2 A/l \qquad (3.2)$$

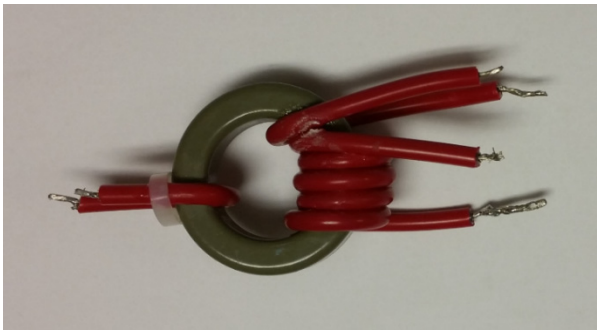


Fig. 3.4: High isolation transformer designed using high voltage wire.

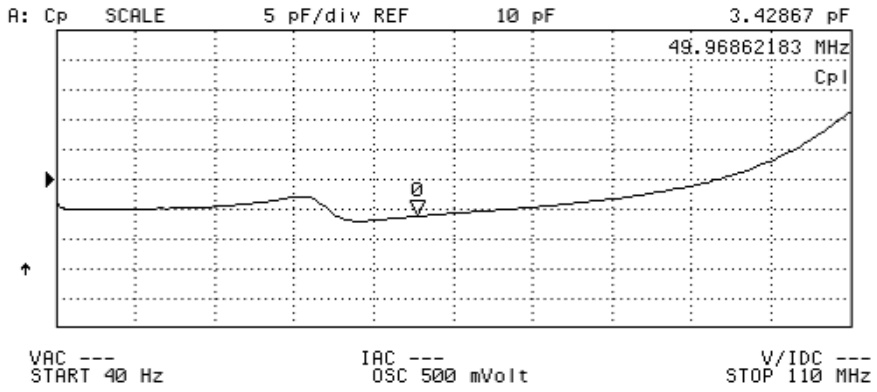


Fig. 3.5: The coupling capacitance curve with respect to frequency up to 110 MHz.

The dc-dc high isolation power supply is built using the transformer described above with two separate secondary windings, as shown in Fig. 3.2. The input voltage is chosen as 10 V dc to obtain better noise margin as explained in the next subsection. The output voltages are about +20 V and -5 V. This is obtained by connecting the negative terminal of the V_{out1} (20 V) to the positive terminal of V_{out2} (5 V).

3.2.3 The Driver Stage Development

The selection of components that have high immunity to noise is very critical for operation of the gate driver circuit. As the MOS gate of the IGBT does not consume considerable amount of power (about a watt is sufficient), the off-the-shelf ICs, meant for low voltage, low power applications, have been sufficient to build the isolation power conversion stage for the gate driver. To maintain good signal fidelity, V_{cc} of 10 V has been chosen for most of the ICs. The high V_{cc} in combination with good noise margins of the CMOS logic levels (in contrast to lower noise margin TTL logic at 5 V) are pivotal in maintaining integrity of the signals. The de-coupling capacitors used in the circuit (for both isolation and driver stages) have extremely low ESL of < 400 pH, which are placed close to the V_{cc}/ground pins of the ICs.

The PWM input to the driver stage is transferred from the DSP controller using fiber optic cable and optical transmitter/receiver. This method of signal transfer is extremely reliable as there is no limit on either isolation voltage or dv/dt (when the receiver and transmitter are provided with power supplies having necessary isolation). However, as the V_{cc} of the optical receiver and transmitter of the off-the-shelf components is typically limited to 5 V, the driver stage (in contrast to the isolation stage) is provided with V_{cc} of 5 V. Therefore, PCB design was done with ground planes for low inductance to ensure reliability of the signals due to the lower noise margins presented by V_{cc} of 5 V.

As mentioned earlier, the gate voltage (V_{GE}) requirement for the SiC IGBT is +20 V and –5 V for turn-on and turn-off respectively. Unlike the case of Si device, the SiC devices require V_{GE} of about +20 V during turn-on to minimize the conduction loss [17]. Fig. 3.6 shows the prototype gate driver built with all these considerations. The top PCB in the picture is the dc to dc isolated power supply stage; whereas the bottom PCB is the driving stage with optical receiver for the PWM.

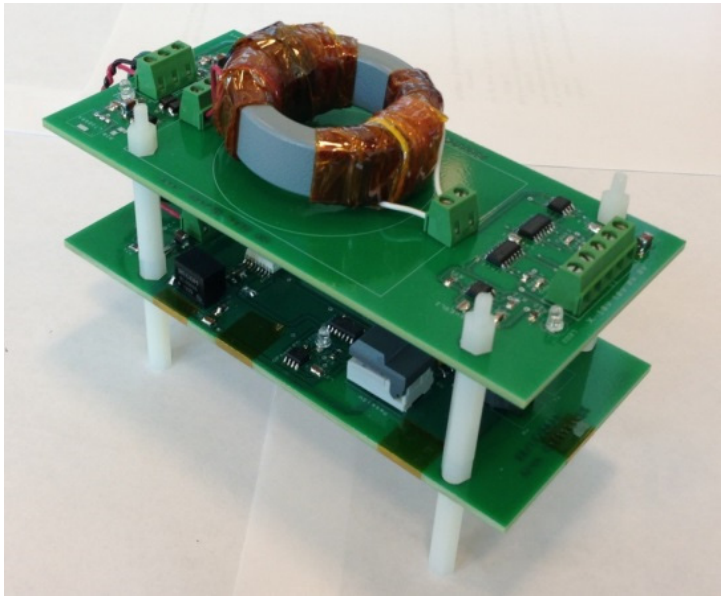


Fig. 3.6: The high voltage gate driver prototype for the 15 kV SiC IGBT.

3.3 Experimental Validation

The fundamental challenge in validating the gate driver prototype is availability of high voltage (> 10 kV) high power dc source. Therefore, initial tests on the driver were performed on a clamped inductive double-pulse test setup intended for characterizing the switching performance of the IGBT. The tests were carried out by a high voltage and low current (10 mA) dc source storing the required amount of energy for two switching pulses in a string of high voltage film capacitors. The test circuit is a simple half-bridge converter with purely inductive load, with the 2 μm field-stop buffer layer IGBT on high-side so that the gate driver is exposed to high voltage and high dv/dt, as shown in Fig. 3.7. The switching voltage waveform of the IGBT at 11 kV on this test setup is shown in Fig. 3.8, which is identical to the waveform shown in Fig. 3.1. It should be noted that the gate voltage measurement is practically limited due to unavailability of a low voltage differential probe with very high isolation. The validation of the gate driver is confirmed from the operation of the circuit. Despite the confirmation from this test that the driver circuit can reliably transfer the gate

pulses with desired isolation and dv/dt capability, the robustness of the gate driver cannot be confirmed unless a continuous switching frequency test is performed.

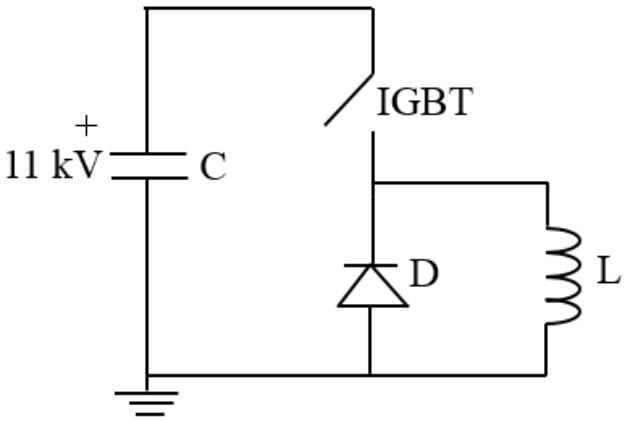


Fig. 3.7: The half-bridge test circuit schematic used for 11 kV double-pulse validation of the gate driver.

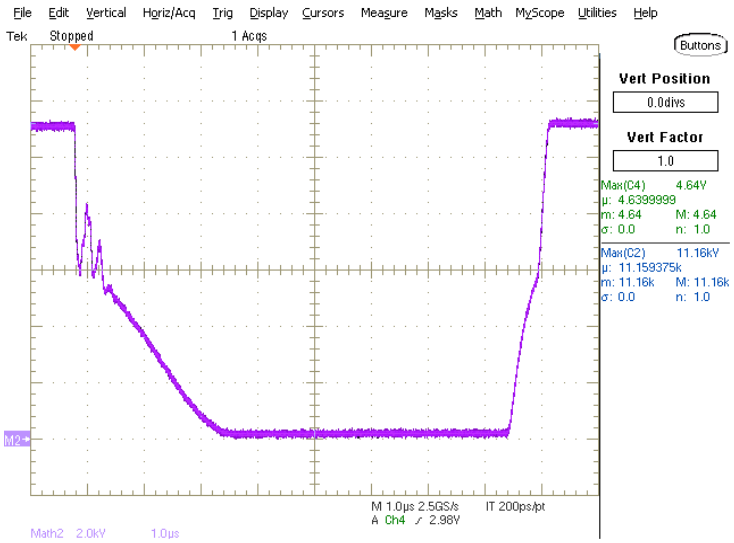


Fig. 3.8: The high-side IGBT (2 μm buffer layer) switching waveform at 11 kV validating the gate driver (waveform measured using single-ended probe and math function on the oscilloscope)

To perform continuous switching frequency tests on the gate driver, the high voltage, high current (not milli-ampere as in double pulse circuit) source is realized by a dc-dc boost converter with a 5 μm field-stop buffer layer IGBT. The input to the boost converter is a regulated laboratory high current, dc power supply of 3 kV, 50 A capability. A buck converter is realized on the same high voltage dc link, to avoid one more set of high voltage low ESL film capacitors, to test the gate driver, as shown in Fig. 3.9. The IGBT S2 and diode D2 form the boost topology for high voltage source realization; whereas, the IGBT S1 and diode D1 are used for buck topology for the gate driver tests. The inductance, L, has been designed with series connection of four individual high voltage inductors (each with a value of about 20 mH) to provide an effective inductance of about 80 mH. The duty cycle of the boost and buck converters are 80 % and 20 % respectively. The corresponding boost and buck converter waveforms at 6 kV dc link and at 5 kHz switching frequency on both boost and buck converters, validating the gate driver (on S1) are shown in Fig. 3.10.

The boost converter fed buck converter has drawback of using two 15 kV SiC IGBTs and two HV diode modules. Also, an over voltage protection is needed on the high voltage dc bus to prevent damage of the boost converter switching devices in case of gate driver failure on the buck converter. In addition, it is critically important to save the SiC IGBTs, as they are research samples. Therefore, for higher voltage continuous frequency tests, buck-boost converter topology (shown in Fig. 3.11) has been used to evaluate the gate driver. This topology uses only one IGBT (5 μm field-stop buffer layer) and one diode. However, the IGBT will be stressed to the sum of input and output voltage; whereas, the gate driver sees maximum common mode voltage magnitude corresponding to the output voltage (for a step-up buck-boost converter). The buck-boost converter is operated at 5 kHz with an input of 2 kV and output of 8 kV (80 % duty cycle). The IGBT is exposed to a continuous voltage stress of 10 kV at 5 kHz under these conditions. The gate driver is exposed to common-mode voltage of 2 kV when the IGBT is on; and -8 kV when the IGBT is off. The corresponding experimental waveforms of the inductor voltage (common-mode voltage seen by the gate driver) and current are shown in Fig. 3.12. This test has been carried out for a duration of 3 hours to validate reliable operation of the gate driver. The maximum turn-on and turn-off dv/dt are 85 kV/μs

and 15 kV/μs respectively, as shown in Figs. 3.13 and 3.14, with $R_{G(ON)}$ of 20 Ω and $R_{G(OFF)}$ of 10 Ω. Table 3.2 summarizes all the above test conditions under which the gate driver is evaluated.

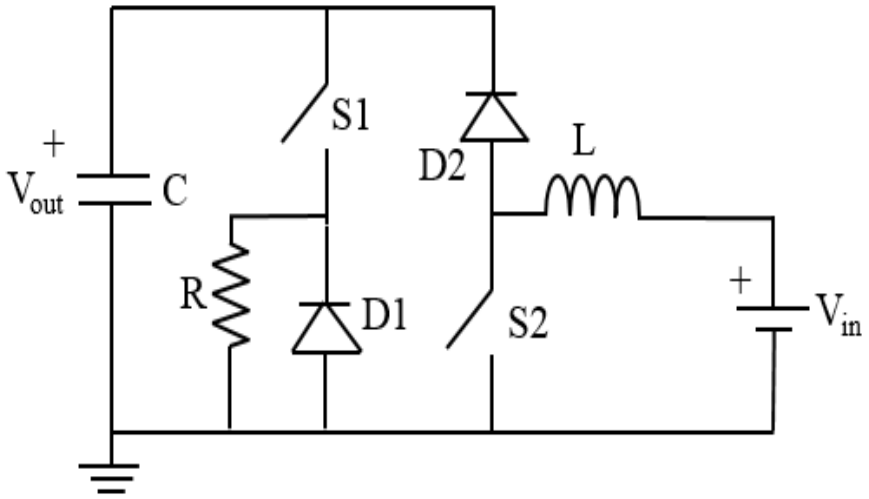


Fig. 3.9: The boost converter fed buck converter test circuit schematic used for 6 kV, 5 kHz validation of the gate driver.

The test setup of the buck-boost converter is shown in Fig. 3.15, and of the double-pulse tests is shown in Chapter-2 (Fig. 2.18). The high voltage probes used are Tektronix 6015A 20 kV single-ended probes with 75 MHz bandwidth. The oscilloscope bandwidth is set to 150 MHz on the corresponding channels. It can be noticed from Fig. 3.10 that the HV single-ended probes are undercompensated during the boost converter fed buck converter tests. The probe compensation is adjusted for the buck-boost converter tests, and it is evident from the voltage waveform in Fig. 3.12.

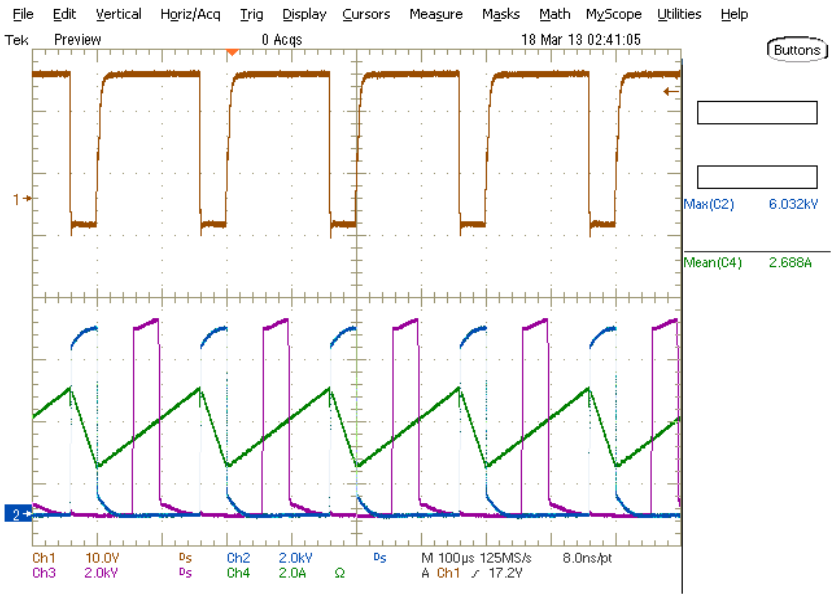


Fig. 3.10: Waveforms showing 6 kV, 5 kHz evaluation of the gate driver. (Ch1: V_{GE} of 15 kV IGBT S2; Ch2: V_{CE} of S2; Ch3: V_{CE} of D1; Ch4: I_L).

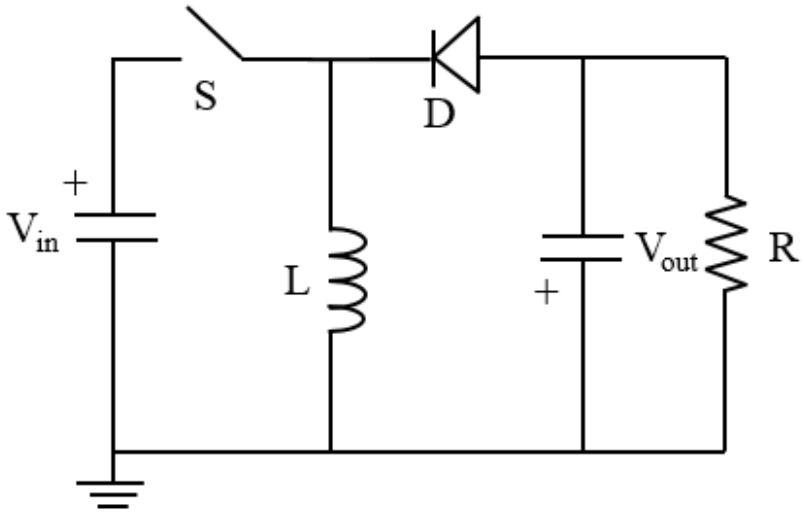


Fig. 3.11: The buck-boost converter schematic used for 8 kV, 5 kHz validation of the gate driver.

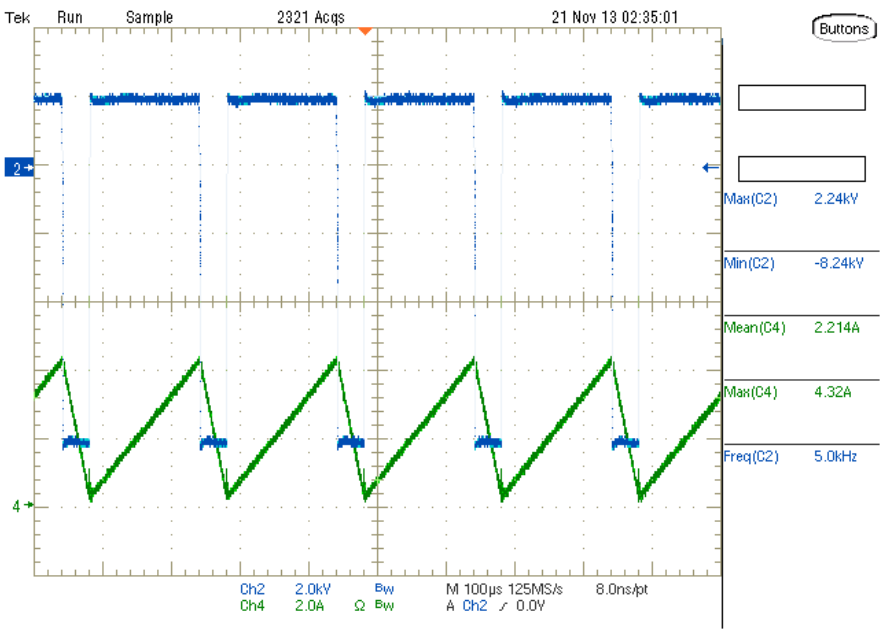


Fig. 3.12: Waveforms showing 8 kV, 5 kHz evaluation of the gate driver. (Ch2: Isolation supply common mode voltage; Ch4: I_L)

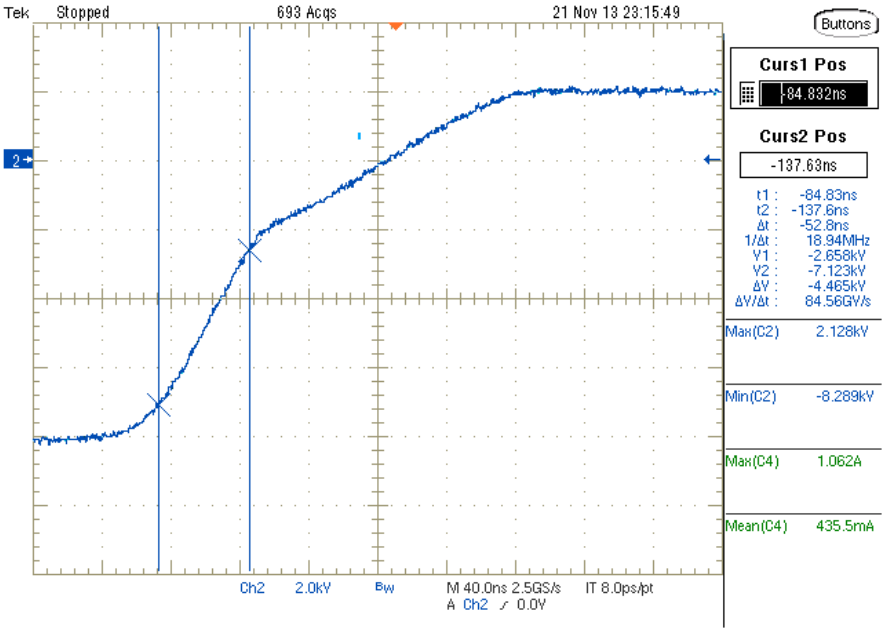


Fig. 3.13: Turn-on dv/dt during 8 kV, 5 kHz evaluation of the gate driver with $R_{G(ON)}$ = 20 Ω. (Ch2: Isolation supply common mode voltage)

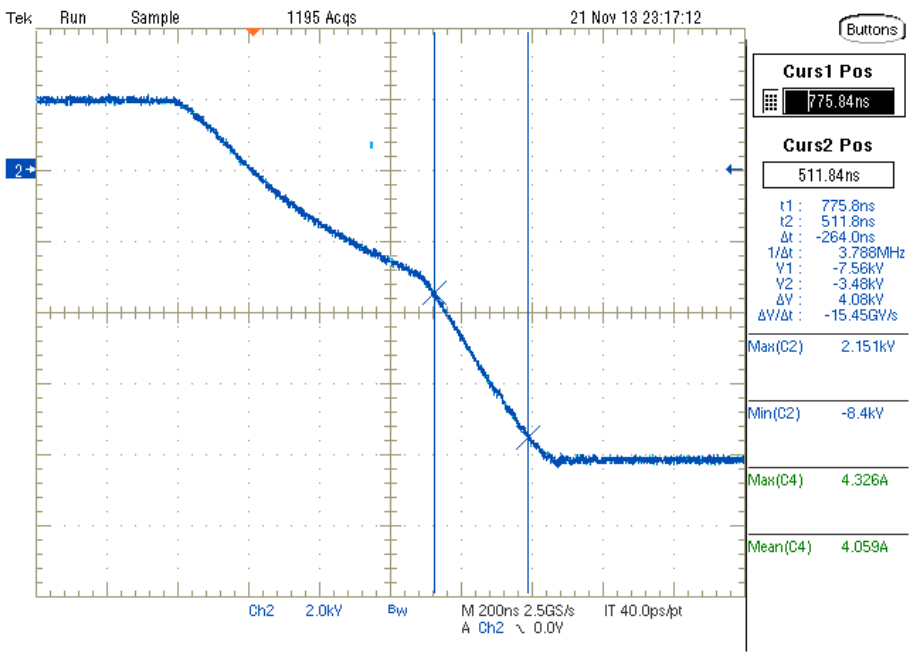


Fig. 3.14: Turn-off dv/dt during 8 kV, 5 kHz evaluation of the gate driver with $R_{G(OFF)}$ = 10 Ω. (Ch2: Isolation supply common mode voltage)

Table 3.2: Summary of gate driver evaluation

Test Procedure	**Max common-mode voltage**	**Max punch-thru dv/dt**	**$R_{G(ON)}$/ $R_{G(OFF)}$**	**Duration of Test**
Double-Pulse	11 kV	110 kV/µs	200 Ω/ 10 Ω	< 20 µs
Boost converter fed Buck converter	6 kV	<30 kV/µs	200 Ω/ 10 Ω	5 minutes
Buck-boost converter	8 kV	85 kV/ µs	20 Ω/ 10 Ω	3 hours

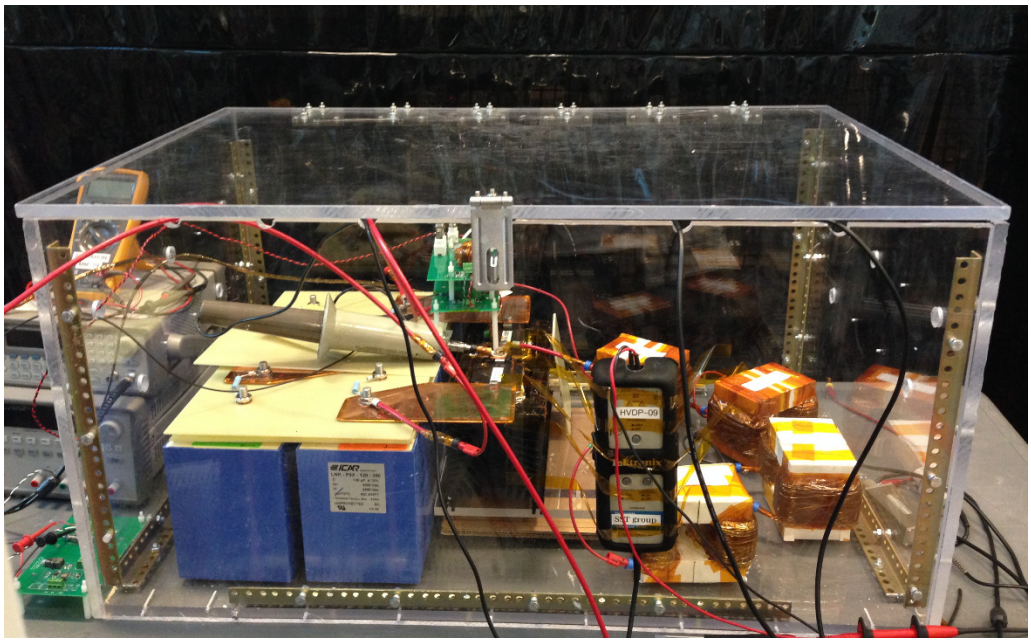


Fig. 3.15: Experimental setup of buck-boost converter used for 8 kV, 5 kHz validation of the gate driver.

3.4 Robustness Evaluation of the Gate Driver

To understand influence of the high dv/dt on signal fidelity of the gate driver, the PCB layout of the isolation stage is redesigned by incorporating BNC connectors to probe different signals on the primary (control-supply ground) side of the isolation stage as shown in Fig. 3.16 (bottom). It can be seen that this layout is similar to the one that has been used for all the previous evaluation (top layout in Fig. 3.16), except for incorporation of the BNC connectors. The BNCs have been used to probe the signals accurately under high di/dt environment without any significant ground-loop noise pickup. This method has been chosen for analysis as the floating ground (secondary of the isolation supply or the emitter of the IGBT) side signals cannot be measured due to unavailability of commercial low voltage probe with such high isolation.

Fig. 3.17 shows output of the two BNC connectors along with the common-mode voltage across the isolation stage of the buck-boost converter at 8 kV output at 5 kHz. One of the two BNC connectors correspond to the 50 % square wave PWM of the H-bridge IC used for high frequency square-wave generation to feed the primary of the isolation transformer of the dc-dc isolation stage of the gate driver. The other BNC connector corresponds to V_{cc} of the H-bridge IC. The schematic of the isolation stage of the driver with these ICs is shown in Fig. 3.18. From the waveforms shown in Fig. 3.17, the PWM signal has negligible influence due to the dv/dt generated by the IGBT (85 kV/μs during turn-on; 15 kV/μs during turn-off). But, ringing of 3 V peak-peak is observed in the V_{cc} of the H-bridge IC, during turn-on transition of the IGBT. However, it is not detrimental to the operation of gate driver as this induced noise is well below the threshold of the CMOS logic levels used in the circuit.

This validates robustness of the design at 8 kV and maximum dv/dt of 85 kV/μs. Several other signals have also been monitored using the other BNC connectors shown in Fig. 3.13, but found to have negligible influence from the common-mode dv/dt. The negligible influence on the fidelity of the signals can be attributed to the design of the isolation stage with insulation dielectric strength over 100 kV dc (based on the number of layers of kapton insulating tape), which resulted in very low interwinding coupling capacitance. It is to be noted that the bench-top control supply (supply input to the gate driver) ground is solidly earthed to bypass its isolation so as to expose the gate driver to the complete common-mode voltage of 8 kV with 85 kV/μs.

To understand the influence of increased inter-winding coupling capacitance of the isolation stage, a transformer with considerable overlap between primary and secondary windings has been designed. The capacitance values of this transformer are compared with the original transformer in Table 3.2. Fig. 3.19 shows the original transformer (top) and the redesigned one with higher capacitance (bottom). The influence of the dv/dt on the PWM input to the H-bridge can be seen in Fig. 3.20. A dip of about 1 V in the PWM at both the turn-on and turn-off transitions of the IGBT can be seen. This dip in the (50 % duty cycle) PWM signal is not significant considering the 10 V CMOS logic voltage levels used in the design. But, it is an

indication that the increased capacitance could distort the PWM to an extent where the duty varies from its original value of 50 %, thus saturating the core and influencing the reliability of the gate driver operation.

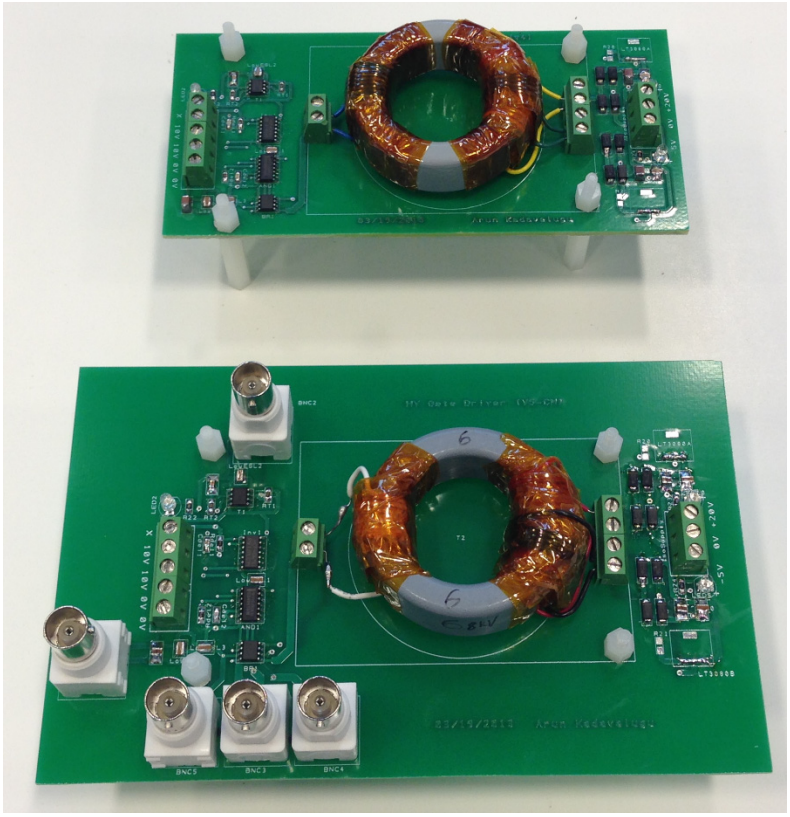


Fig. 3.16: Isolation power supply stage of the gate driver prototype with BNC connectors (bottom board).

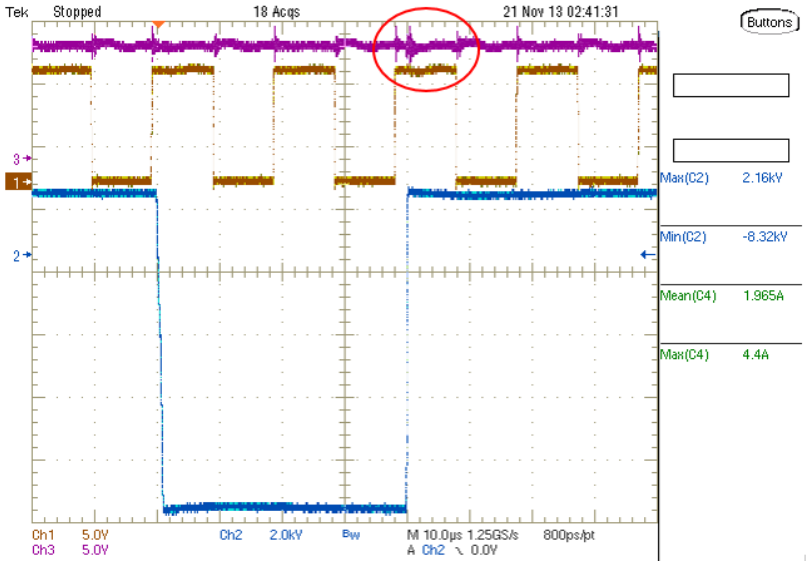


Fig. 3.17: Waveforms of the common-mode voltage and its influence on the signals on the primary side of the isolation stage. (Ch1: A PWM input of the H-bridge IC on primary side of the isolation stage; Ch2: Common-mode voltage; Ch3: V_{cc} of the H-bridge IC).

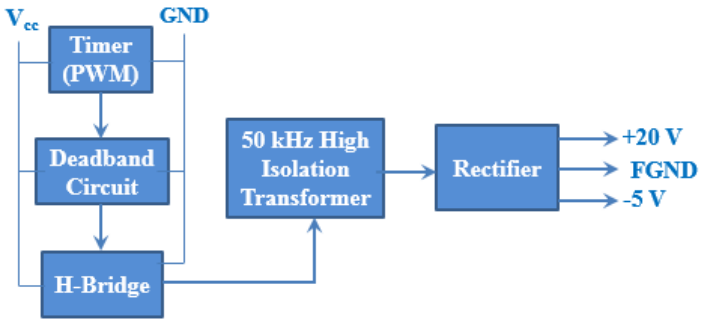


Fig. 3.18: Schematic of the isolation power supply of the gate driver showing primary side ground (GND) and output floating ground (FGND).

Table 3.3: Comparison of the isolation stage transformers used for dv/dt performance evaluation

Isolation supply transformer	**Coupling capacitance w.r.t Frequency**			
	1 kHz	10 kHz	50 kHz	100 kHz
Original design	11.5 pF	5.9 pF	4.5 pF	4.3 pF
Higher capacitance design	35.0 pF	28.5 pF	26.4 pF	25.8 pF

The detailed investigation on the life time reduction (aging) of the insulation due to such high dv/dt is beyond the scope of this work. Also, the results shown on the performance of the dv/dt are only to validate feasibility of the design techniques employed for the gate driver and its testing on the state-of-the-art 15 kV IGBT. A comprehensive investigation needs to be done to clearly understand the influence of the dv/dt on the gate driver operation and to develop methods to mitigate these influences. The possibility of corona formation due to air trapped in the kapton tape layers needs to be evaluated. Using epoxy based potting could be a possible solution to prevent insulation deterioration with time.

Fig. 3.19: The original isolation transformer (top) and the redesigned version for higher coupling capacitance (bottom).

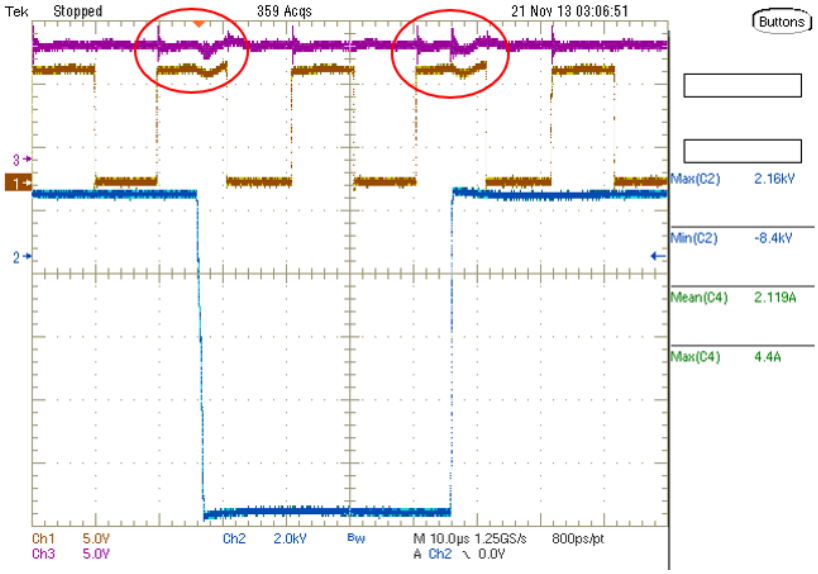


Fig. 3.20: Waveforms of the common-mode voltage and its influence on the signals on the primary side of the isolation stage. (Ch1: A PWM input of the H-bridge IC on primary side of the isolation stage; Ch2: Common-mode voltage; Ch3: V_{cc} of the H-bridge IC).

3.5 Summary

The high voltage and high dv/dt gate driver is designed with dc-dc isolation power supply and optical PWM signal transfer for high reliability, flexibility to extend for higher voltages, and without any limits on the duty cycle of the PWM input. After investigating several commercially available toroidal cores, the ferrite core has been chosen due to its high permeability and low cost. The different circuit design techniques used to have better noise immunity are provided. The isolation stage is designed with a 50 kHz, 50 % duty cycle square wave generator on the primary and two separate diode rectifier stages on the secondary to provide +20 V and -5 V supplies, with no galvanic connection between both sides of the transformer. The high isolation is realized by placing insulation on the core and using low voltage wire for windings placed on opposite sides of the toroid. This gave the inter-winding coupling capacitance of 3.4 pF at 50 MHz. The gate driver is then evaluated on a high-side SiC IGBT at 11 kV on a double pulse test setup exposing it to over 100 kV/μs. This was followed by implementation of several test circuits to continuously expose the gate driver up to 8 kV, 5 kHz, 85 kV/us (maximum dv/dt) for three hours at a stretch, for robust validation, while considering the protection of the SiC IGBTs which are research samples. The influence of increased coupling capacitance is also investigated by redesigning the high isolation transformer. Subsequently, the gate driver immunity to high dv/dt was validated by redesigning the PCB with several BNC connectors for signal probing to observe distortion at the IGBT voltage transient instants.

Chapter 4
Demonstration of 15 kV SiC N-IGBT based Power Converters

4.1 Introduction

The earlier chapters have dealt with characterizing 15 kV IGBTs, understanding their influence on power converter design and development of gate driver. The objective of that work is to provide a clear understanding for design and development of high power converters using these novel high voltage devices. In a converter level demonstration (unlike the double-pulse tests) understanding the thermal loading of the IGBT is very critical factor for reliable operation. A major portion of this chapter is devoted to understand the factors that limit the thermal performance of the SiC IGBT. As a part of that evaluation, Powerex has provided the thermal information of the IGBT custom module package based on the finite element analysis. The subsequent sections of this chapter explain the factors that limit the thermal performance of the IGBT, the actual experimental switching frequency limits for air cooled and liquid cooling heat sink systems, followed by 10 kV demonstration of dc-dc boost converter, three-level poles and H-bridge inverter.

4.2 Thermal resistance of the SiC IGBT Module

In practical power converter applications, the IGBT power dissipation (determined by the operating current and switching frequency) is limited by the ability to transfer the generated heat from the device junction to the ambient. A low thermal resistance would not increase device junction temperature considerably because of low thermal drop from the power dissipation. The thermal resistance from the junction to the ambient is contributed by the module package, the thermal interface compound and the external heat sinking (cooling)

mechanism. As the overall thermal resistance is pivotal in determining the switching frequency (thermal) limits, understanding the different components contributing to the effective thermal resistance of the state-of-the-art 15 kV SiC IGBT Module is very crucial.

The base plate of the 15 kV IGBT has AlN isolation layer rated for 20 kV dc. The AlN isolation and several other packaging layers contributing to the thermal resistance from the IGBT junction to the ambient are shown in Fig. 4.1. Thermal simulations have been performed by Powerex by incorporating thermal conductivity values of the different layers to determine the temperature drop across the entire thermal path for a power dissipation of 125 W by the IGBT. The IGBT junction temperature is found to be 67.2^{o}C for 125 W power dissipation (the heat sink is constrained to 0^{o}C), indicating thermal resistance of 0.54^{o}C/W from the IGBT junction to the bottom of the heat-sink. The corresponding temperature distribution profile of the IGBT module is shown in Fig. 4.2, along with the temperature drop across each layer in Table 4.1. The thermal conductivity of the AlN layer is taken as 135 W/mK, corresponding to 175^{o}C. It should be noted that the thermal resistance of the heat sink taken in this analysis corresponds to the liquid cooling mechanism. These thermal resistance values are the basis for determining the IGBT safe operating frequency limits presented in the next section.

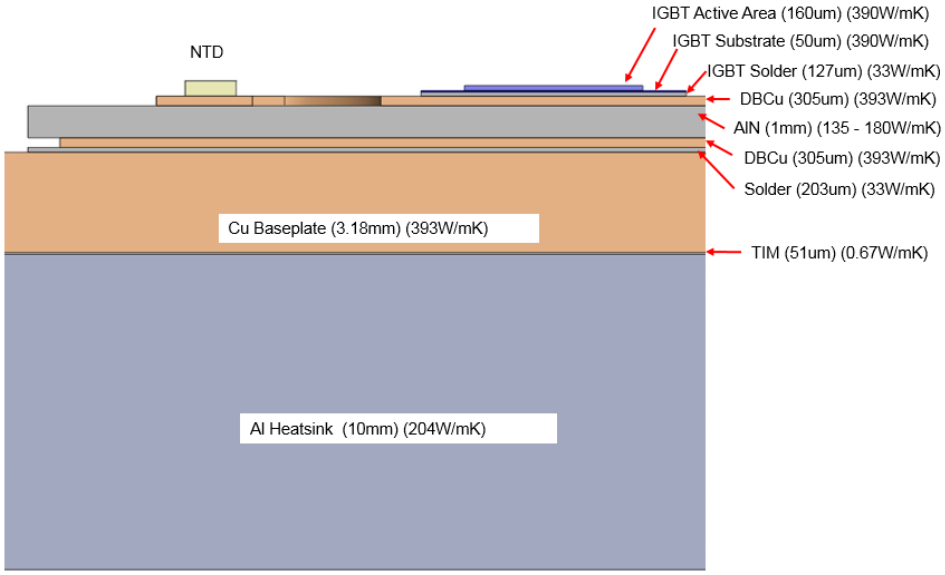


Fig. 4.1: The different layers in the IGBT module package contributing to the thermal resistance (figure provided by Powerex)

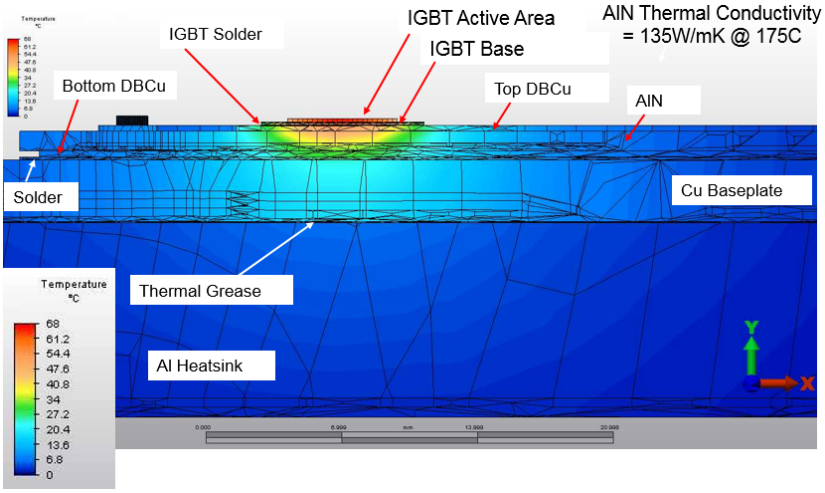


Fig. 4.2: Simulation result showing the temperature profile across the cross-section of the IGBT module for 125 W power dissipation (result provided by Powerex)

Table 4.1: Temperature drop across each layer in the thermal path of the 15 kV SiC IGBT module package (data provided by Powerex)

Layer	Temperature at Top of Layer (°C)	Temperature drop across Layer (°C)	% Temp drop
IGBT Active	67.2	0.8	1.2 %
IGBT Base	66.4	0.2	0.3 %
IGBT Solder	66.2	13.1	19.5 %
Top DBCu	53.1	1.8	2.7 %
AlN	51.3	19.8	29.5 %
Bottom DBCu	31.5	1.0	1.5 %
Substrate Solder	30.5	5.3	7.9 %
Baseplate	25.2	7.0	10.4 %
Thermal Grease	18.2	12.0	17.8 %
Heat sink	6.25	6.3	9.3 %
Bottom of Heat sink	0	-	-

4.3 Analytical evaluation of IGBT freqeuncy limits based on the experimental data

Based on the recommendation from Cree, 150^{o}C is taken as the maximum operating temperature for the 15 kV SiC N-IGBT during its operation in a power converter system. The junction power dissipation (or W/cm^2) is limited by this maximum operating temperature and the thermal resistance from the junction to the ambient. Table 4.2 shows the IGBT parameters for which the thermal limits are evaluated. The nominal operating voltage in a power converter system is chosen as 10 kV (with 1.5 factor of safety; as per the practical converter applications) of the maximum blocking voltage of 15 kV. Also, the hard-switching frequency limits are being evaluated for two different current densities as shown in the table. The thermal resistance information for the liquid cooling case is taken from the analysis presented in the earlier section. For the case of air cooling, the heat sink thermal resistance is scaled up appropriately based on the heat sink datasheet used in the boost converter demonstration presented in the next section.

Fig. 4.3 shows 6.2 kHz as the frequency limit for the case of 10 kV, 5 A with liquid cooling mechanism. It is can be seen that at 6.2 kHz, the junction temperature reaches stable operating point of 150^{o}C, where the power loss curve intersects the thermal resistance line. The power loss curves are obtained from MATLAB curve fitting the turn-off energy loss versus temperature (T) data at 10 kV and 5 A, given by equation (4.1). The conduction duty cycle is taken as 50 % and the clamped inductive load switching loss data at 10 kV presented in chapter-2 for 5 μm field-stop buffer layer are used. The reduction of turn-on loss with temperature is ignored, as it is not considerable in comparison to the turn-off loss, and the conduction loss data used corresponds to 150^{o}C. It should be noted that the conduction loss variation with temperature is negligible. The thermal resistance line, showing the steady state junction temperature with respect to power dissipation, given in equation (4.2) is shown in Fig. 4.3 (red line). At a particular switching frequency, the IGBT power dissipation increases with the junction temperature. The junction temperature rise increases the power dissipation further, which in turn, increases the junction temperature. This process is repeated till the IGBT

junction finally settles down to the steady temperature determined by the intersection of temperature dependent power dissipation curve with the thermal resistance line.

$$E_{OFF}(T) = -2x10^{-9}T^3 + 8.2x10^{-7}T^2 - 2.1x10^{-5}T + 0.008 \quad (4.1)$$

$$T_J = (P_D \times R_{TH}) + T_A \quad (4.2)$$

Where, T_J is the IGBT junction temperature, P_D is the power dissipation, R_{TH} is the total thermal resistance and T_A is the ambient temperature.

Table 4.2: Parameters of 15 kV SiC N-IGBT used for evaluating hard-switching limits

Parameter	Value
IGBT rated blocking voltage	15 kV
Nominal operating voltage	10 kV
Nominal operating current	5 A (15 A/cm^2) 10 A (30 A/cm^2)
Active area	0.32 cm^2
Maximum operating junction temperature	150^{o}C
Thermal resistance from junction to the ambient (liquid cooling)	0.54^{o}C/W
Thermal resistance from junction to the ambient (air cooling)	0.65^{o}C/W
Ambient Temperature, R_A	35^{o}C

The hard switching frequency limit is 6.2 kHz for 10 kV, 5 A operation with liquid cooling, as shown in Fig. 4.3. The intersection of the power dissipation curve at 6.2 kHz and the thermal line at 150^{o}C (taken as the maximum operating junction temperature) is seen in the figure. The

frequency limit for 10 kV, 10 A is 3.9 kHz, with liquid cooling, as shown in Fig. 4.4. The 10 kV, 10 A turn-off energy loss versus temperature (T) obtained from the MATLAB curve fitting is given in (4.3). The frequency limits with air cooling at 10 kV, 5 A and 10 A are shown in Fig. 4.5 and Fig. 4.6 respectively. The thermal resistance line is derived by using the R_{TH} value corresponding to the air cooling, shown in Table 4.2. The summary of frequency limits for all these cases is provided in Table 4.3. In moving from liquid cooling to air cooling, the power dissipation density is marginally reduced from 660 W/cm^2 to 550 W/cm^2. This emphasizes the role of the package thermal resistances (rather than the cooling mechanism) in exploiting the SiC material for efficient and high power density power conversion.

$$E_{OFF}(T) = -2.2\text{x}10^{-9}T^3 + 1.1\text{x}10^{-6}T^2 - 8.2\text{x}10^{-6}T + 0.0091 \qquad (4.3)$$

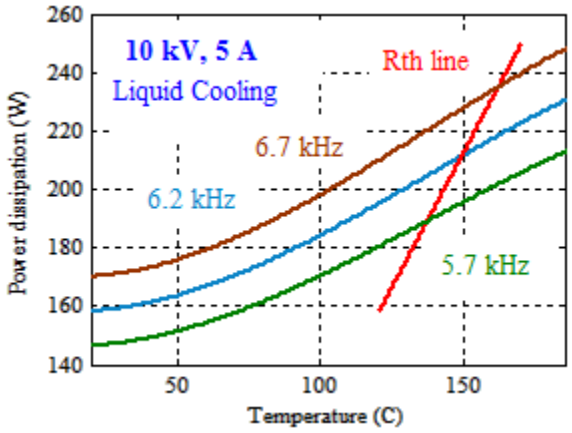


Fig. 4.3: Frequency limit curves at 10 kV, 5 A (50 % conduction duty cycle) with liquid cooling.

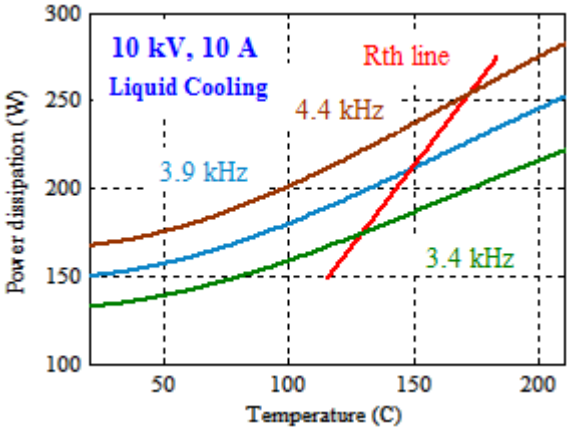


Fig. 4.4: Frequency limit curves at 10 kV, 10 A (50 % conduction duty cycle) with liquid cooling.

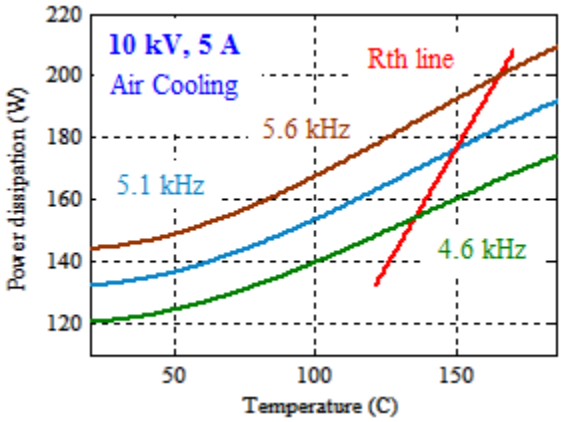


Fig. 4.5: Frequency limit curves at 10 kV, 5 A (50 % conduction duty cycle) with air cooling.

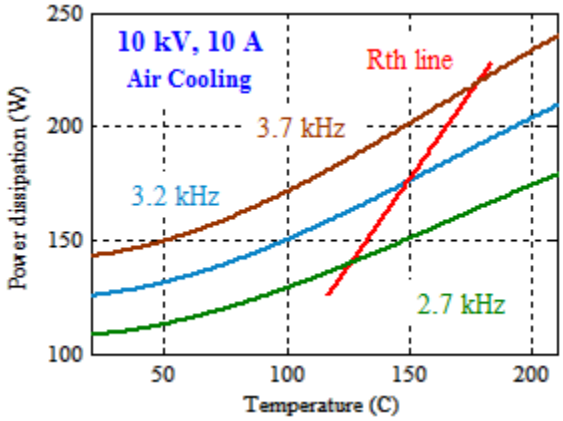


Fig. 4.6: Frequency limit curves at 10 kV, 10 A (50 % conduction duty cycle) with air cooling.

Table 4.3: Summary of hard switching frequency limits of the 15 kV SiC N-IGBT

Parameter	Value
Frequency limits at 10 kV, 5 A	6.2 kHz (liquid cooling) 5.1 kHz (air cooling)
Frequency limits at 10 kV, 10 A	3.9 kHz (liquid cooling) 3.2 kHz (air cooling)
Power dissipation density (active area)	660 W/cm2 (liquid cooling) 550 W/cm2 (air cooling)
Maximum operating junction Temperature	150°C
Ambient Temperature (Assumed)	35°C

4.4 Experimental Demonstration of the IGBT Frequency Capability on a 10 kV Boost Converter

This section presents experimental demonstration of the analytically derived frequency limits provided in the previous section. A dc-dc boost converter topology has been chosen for demonstration, to emulate the hard-switching frequency limits. The converter is operated at 10 kV output, satisfying the IGBT operating voltage outlined in the previous section. The input voltage is chosen as 2 kV. Therefore, the conduction losses are scaled to 80 % to exactly determine the power dissipation under these conditions. Also, only air cooled condition is validated, due to ease of building and implementing the converter system.

The boost converter is operated at 6.7 kHz at 10 kV output voltage as shown in Fig. 4.7, to obtain the 550 W/cm^2 power dissipation density. The IGBT turn-on current is 1.6 A, and the turn-off current is 5 A, with filter inductor of 78 mH in the converter. The turn-off and turn-on transitions measured at the end of one hour duration of the boost converter operation are shown in Fig. 4.8 and Fig. 4.9 respectively. The conduction loss is calculated for 80 % duty with the ramp rise. The online junction temperature is determined from the instant at which IGBT enters punch-through (the point at which the slope of voltage changes) during turn-off transition. In Fig. 2.8, it is shown that the duration it takes to reach punch-through is increasing with junction temperature. This fact is used to estimate the junction temperature accurately, by matching the voltage transitions with the hot-plate based double-pulse switching tests. This method of determining temperature provides accuracy data and measurement safety at high voltage. Also, the double-pulse tests have been re-conducted with 78 mH (in place of the originally used 8 mH) at 10 kV and 5 A to match the waveforms for better accuracy, for the temperature estimation.

Based on this method, the junction temperature is found to be 146^{o}C at the end of one hour of the boost converter operation. The corresponding voltage rise curves, from the converter startup instant to one hour operation, are shown in Fig. 4.10. It is seen that the junction temperature increased negligibly from 30 minute to one hour instants. The details of the heat

sink used are given in [18]. It should be noted that the IGBT and diode modules are mounted on the same heat sink. The IGBT power dissipation is 176 W at 6.7 kHz, as summarized in Table 4.4, which corresponds to 550 W/cm^2 (active area). The equation (4.2) is used to extract the exact thermal resistance of the heatsink, provided in Table 4.4. It should be noted that the ambient and the corresponding junction temperature are slightly lower in the demonstration.

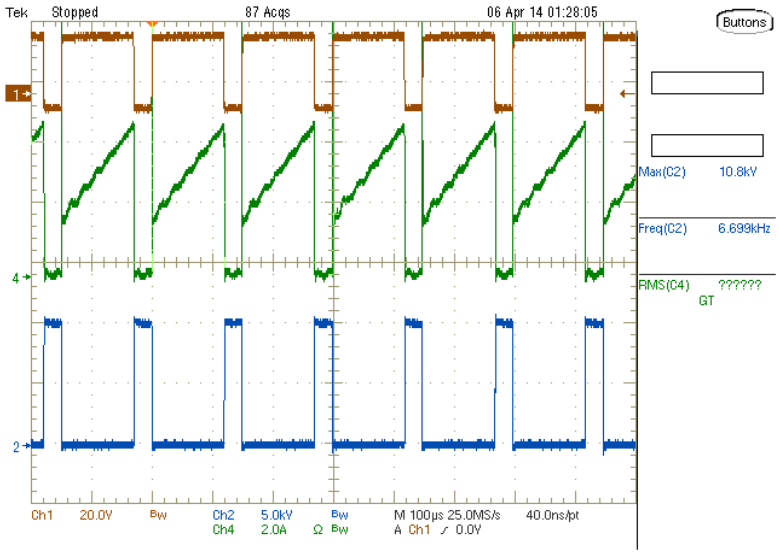


Fig. 4.7: The boost converter operation at 6.7 kHz, with 2 kV input and 10 kV output, at 6.4 kW. (Ch1: V_{GE}, Ch2: V_{CE}, Ch4: Inductor current)

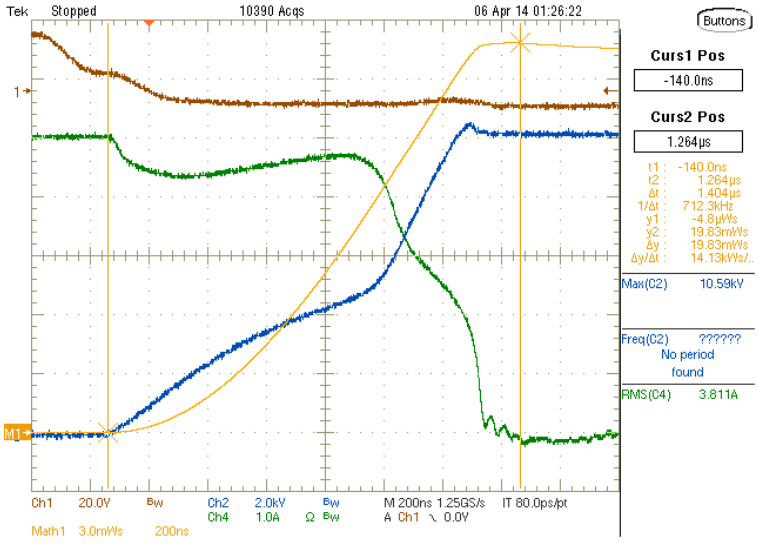


Fig. 4.8: The turn-off transient during the 6.7 kHz operation of the boost converter at 10 kV, 6.4 kW output (taken after 60 minutes).

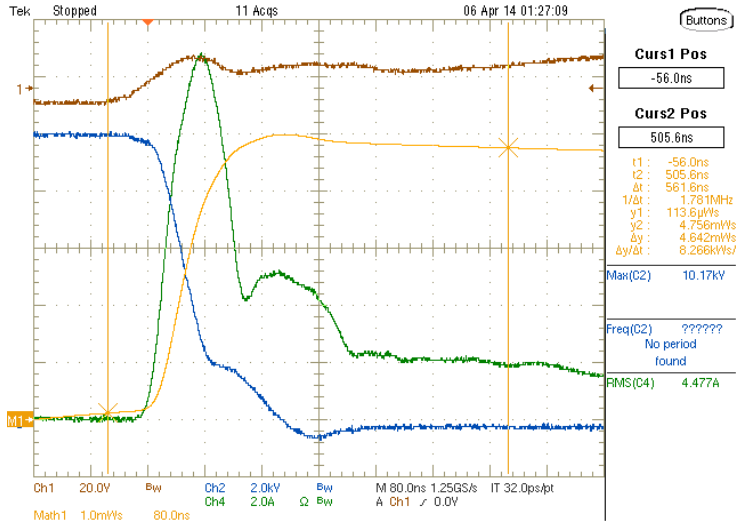


Fig. 4.9: The turn-on transient during the 6.7 kHz operation of the boost converter at 10 kV, 6.4 kW output (taken after 60 minutes).

Table 4.4: Summary of boost converter demonstration

Parameter	Value
Input Voltage, Output Voltage	2 kV, 10 kV
Switching Frequency	6.7 kHz
Filter Inductor	78 mH (Q = 308 at 5 kHz)
Input Power	6.4 kW
Cooling Mechanism	Forced air convection
Conduction Loss (80 % duty)	12 W
Turn-on Loss (10 kV, 1.6 A)	31 W (at 6.7 kHz)
Turn-off Loss (10 kV, 5 A)	133 W (at 6.7 kHz)
Total Power Loss (active area)	176 W
IGBT Power Dissipation Density	550 W/cm^2
Thermal Resistance (Junction to Ambient)	0.65 $^oC/W$
IGBT Junction Temperature (After operating for one hour)	146^oC
Ambient Temperature (Measured)	32^oC

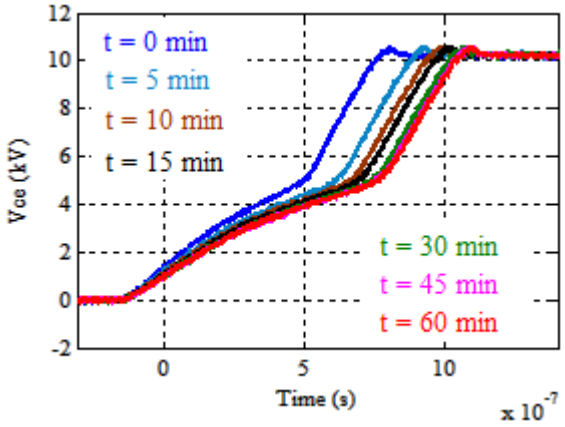


Fig. 4.10: The turn-off voltage curves (indicating temperature settling) during the 10 kV, 6.7 kHz boost converter demonstration.

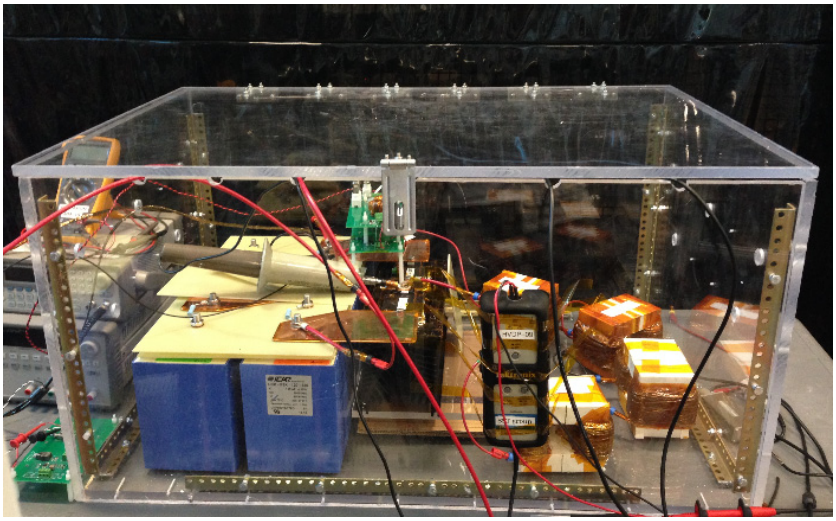


Fig. 4.11: The test setup of the 10 kV output dc-dc boost converter, demonstrating 15 kV SiC IGBT at 550 W/cm^2 with air cooling.

4.5 Three-level NPC Converter Demonstration

The objective of characterizing the IGBT, building a high voltage gate driver and conducting heat-run tests are the necessary steps to demonstrate the SiC IGBT in any practical power conversion system. It has been chosen to demonstrate the SiC IGBT on a three-phase 13.8 kV, 60 Hz to 480 V, 60 Hz, grid interfaced Solid State Transformer (SST), referred as the Transformerless Intelligent Power Substation (TIPS) [19]. This section presents the IGBT converter development and its evaluation for the TIPS system. As shown in Fig. 4.12, the TIPS system has six 3-level neutral point clamped (NPC) converter poles based on the 15 kV SiC N-IGBTs for the rectifier and dc-dc Dual Active Bridge (DAB) HV stage.

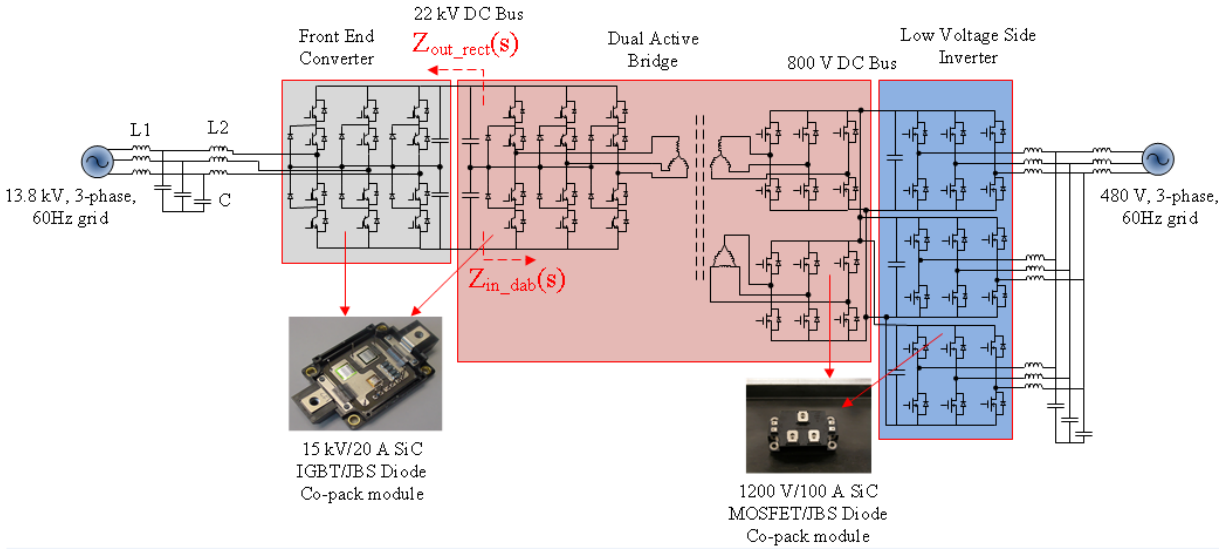


Fig. 4.12: The schematic of the transformerless intelligent power substation (TIPS) interfaced between 13.8 kV and 480 V three-phase grids [19].

The prototype of 3-level pole with four 15 kV IGBT co-pack modules and two diode modules with the bus-bar structure is shown in Fig. 4.13. As the current is in the order of 5 A to 10 A, the di/dt induced voltage spikes are negligible on the IGBTs. Therefore, a simple bus-bar was employed in place of a complex cascaded structure, without impacting the converter performance. However, providing sufficient clearance for handling high voltage is very critical.

The edges of the bus-bar are covered with kapton tape including rounding the corners to minimize surface charge densities, which could be potential points for corona discharge.

As seen from Fig. 4.13, all the IGBT and diode modules of the 3-level pole are mounted on a single heatsink, which was floated, in the initial tests. However, this resulted in spurious tripping of the gate drivers about 6 kV dc-link, which was not resolved even after minimizing the switching dv/dt by increasing the gate resistances. This issue was eventually addressed by connecting the heatsink to mid-point of the dc-link, which led to successful operation up to 10 kV without any spurious tripping. Fig. 4.14 shows operation of the 3-level pole in inverter mode with dc input of 10 kV at 10 kHz square wave switching and 9 kW. The 10 kHz switching was chosen in accordance with the requirements of the dc-dc stage of the TIPS system. The 10 kV single-ended DC source is derived from a built-up DC-DC boost converter using the 15 kV SiC IGBT (presented in the previous section), with a maximum power of 10 kW.

Fig. 4.15 shows common mode currents flowing in the loop from heat sink to dc-link mid-point at both rising and falling edges of the IGBT voltage, which has over 9 A peak. By using a 3 mH choke in between the heatsink and the dc-link mid-point, the common-mode currents were limited to about 1 A as shown in Fig. 4.16. This choke was used a precautionary measure to limit high frequency circulating currents.

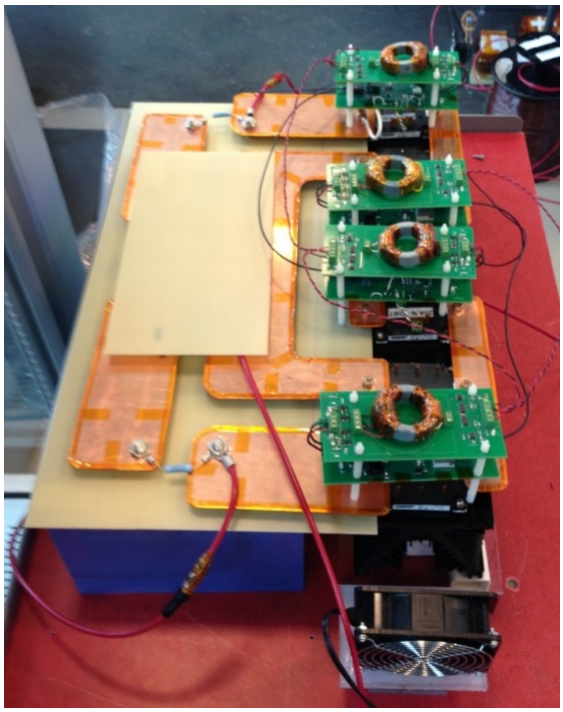


Fig. 4.13: The bus-bar structure of the 3-level NPC pole.

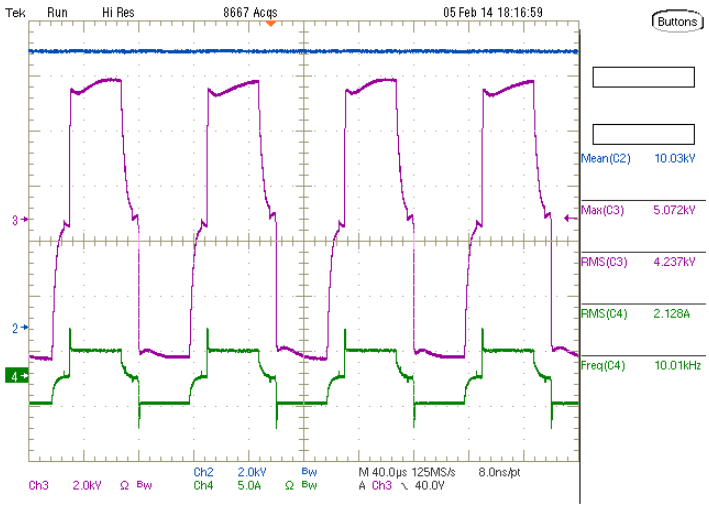


Fig. 4.14: The three-level converter pole waveforms at 10 kV, 10 kHz and 9 kW resistive load. [Ch2: Input dc voltage (2 kV/div); Ch3: Three-level pole output voltage (2 kV/div); Ch4: Pole output current (5 A/div)]

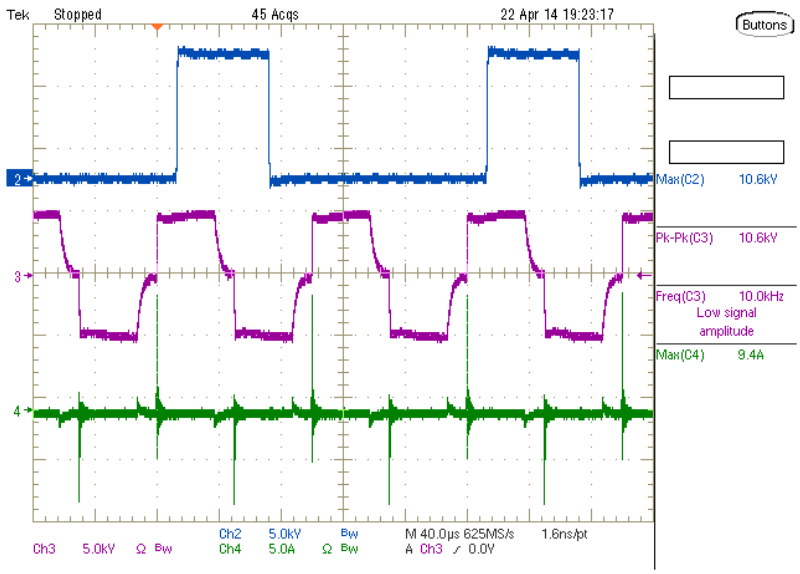


Fig. 4.15: The common currents from the heat sink to the dc-link midpoint with direct shorting. [Ch2: Boost converter switch voltage (5 kV/div), Ch3: Three-level pole output voltage (5 kV/div); Ch4: Common-mode current flowing through the heat sink (5 A/div)

Fig. 4.16: The common currents from the heat sink to the dc-link midpoint with 3 mH choke. [Ch2: Boost converter switch voltage (5 kV/div), Ch3: Three-level pole output voltage (5 kV/div); Ch4: Common-mode current flowing through the heat sink (1 A/div)

The base plate isolation is rated for 20 kV dc, as noted in the earlier section. However it is important to reduce the voltage stress on the baseplate isolation considering 10 kHz switching and high dv/dt. The heatsink connection to the mid-point of the dc-link has the advantage of limiting baseplate isolation of all the IGBT and diode modules to 5 kV, for converter operation at 10 kV dc input. Fig. 4.17 shows the electrical schematic connecting base plates of all the IGBTs and diode modules to the dc-bus midpoint with a 3 mH common-mode choke. The base isolation of each IGBT is between its collector terminal and the common heat-sink of the three-level pole, as represented by the red squares in Fig. 4.17. The voltage stress across each base plate is listed in Table 4.5. The heatsink to dc-bus midpoint connection is ensuring that none of the baseplate isolation layers are stressed beyond 5 kV.

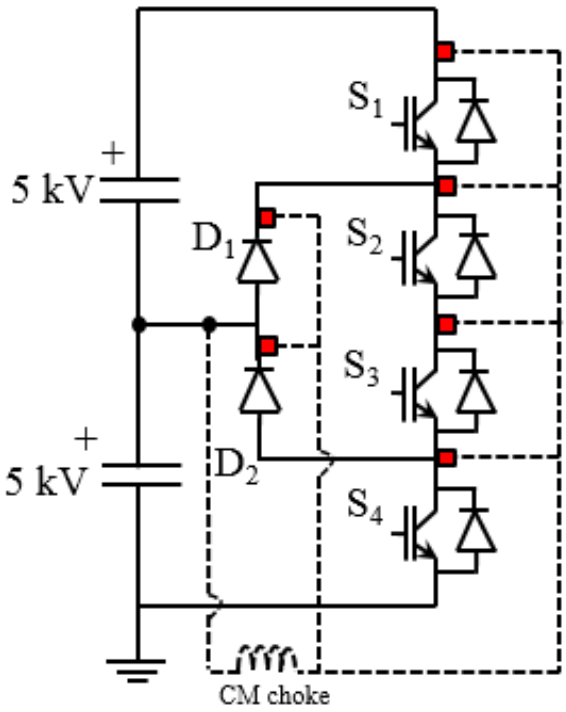


Fig. 4.17: The 3-level pole schematic showing the connection of base plate to the dc-bus midpoint through a common-mode choke (the red squares signify baseplate isolation of each IGBT module).

Table 4.5: Voltage stress across baseplate isolation of each device in the 3-level NPC pole with reference to ground

Device name	Device-side voltage	Heat-sink side voltage	Effective voltage stress across base plate of IGBTs
S_1	10 kV	5 kV	5 kV
S_2	5 kV to 10 kV	5 kV	0 to 5 kV
S_3	0 to 10 kV	5 kV	0 to 5kV
S_4	0 to 5 kV	5 kV	0 to 5kV
D_1	5 kV to 10 kV	5 kV	0 to 5 kV
D_2	5 kV	5 kV	0 kV

4.6 Two-level H-bridge Converter Demonstration

The three-level converter tests are conducted up to a maximum voltage of 10 kV dc input due to the limitation of the dc power supply. Under these conditions, the 15 kV SiC IGBTs are exposed to 5 kV stress in steady state, which is 33% of their maximum voltage blocking capability. A two-level H-bridge topology is attempted to demonstrate, as the 15 kV SiC IGBT is exposed to 10 kV in steady state, which is the practical device operating voltage (considering 1.5 factor of safety).

Each phase leg of the H-Bridge is mounted on a separate heat sink. Similar to the case of 3-level converter, the heatsinks are connected to the mid-point of the dc source to limit the stress on the base plate isolation of all the IGBT modules to 5 kV. The circuit schematic of the H-bridge with common mode choke connection is shown in Fig. 4.18, where the red squares indicate baseplate isolation of the IGBTs. Fig. 4.19 shows the H-Bridge converter results with 10 kV dc input in inverter mode of operation. The converter is operated at 5 kHz switching

frequency, 6 kW power level, with unipolar sine-triangular modulation. The output PWM voltage has a +10 kV, 0 V and -10 kV states resulting from the modulation scheme. The modulation index used is 0.5 to limit the load inductor current to prevent its saturation. The output filter inductance is 240 mH, with resistive load of 2 kΩ. As shown by the PWM output ac voltage with 10 kV peak, the objective of demonstrating the SiC IGBTs to their full voltage capacity (considering 1.5 factor of safety) has been achieved. The gate resistances used are 33 Ω for turn-on and 10 Ω for turn-off. The 10 kV supply is realized by a 1:4 dc-dc boost converter built using a 15 kV SiC IGBT, operated from a regulated commercial dc power supply with input of 2.5 kV.

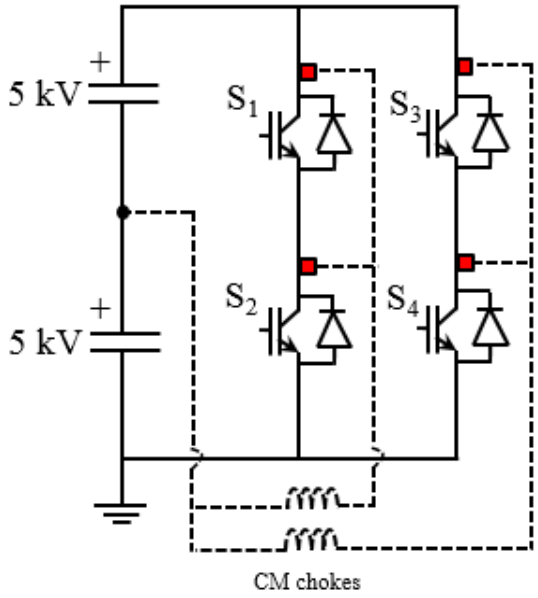


Fig. 4.18: The schematic of H-bridge showing the connection of each heatsink (effectively the baseplates mounted on that pole) to the midpoint using separate common-mode chokes. (The red squares signify baseplate isolation of each IGBT module).

Fig. 4.20 shows thermal image of the converter at the end of 15 minute operation. The maximum temperature on the heat sink is found to be 37.5ºC. The three set points sp1, sp2 and sp3 of the thermal camera are pointing the heat sink under base plates of S1, S2 and S4 respectively. The

slight difference in temperature from device to device is due to cooling fan on only one side of each phase leg. The heat sinks used for each phase-leg have thermal resistance of 0.08ºC/W at 100 CFM air flow [18]. Fig. 4.21 shows the 10 kV H-bridge converter test setup and the dc-dc boost converter providing the 10 kV dc input.

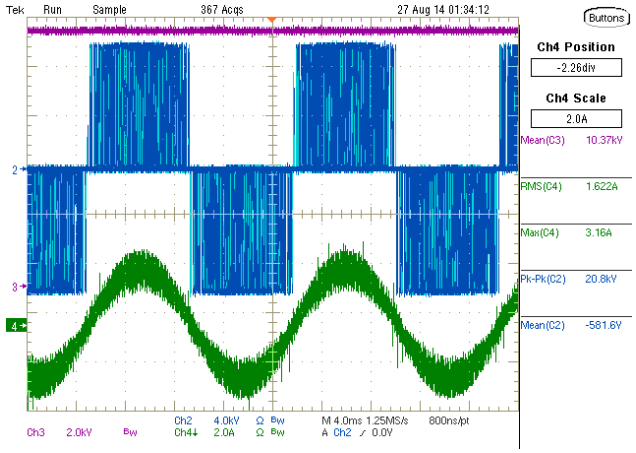


Fig. 4.19: The waveforms of the H-Bridge with 10 kV dc input at 5 kHz and 6 kW operation; $R_{G(ON)}$ = 33 Ω and $R_{G(OFF)}$ = 10 Ω. [Ch2: V_{DC}, 2 kV/div; Ch3: $V_{AC,}$ 4 kV/div; Ch4: $I_{AC,}$ 2 A/div].

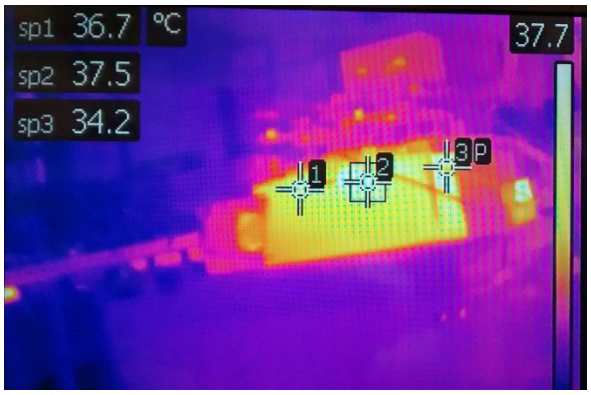


Fig. 4.20: The thermal image of the converter system at the end of 15 minute operation. (sp1, sp2 and sp3 are pointing the heat sink under base plates of S1, S2 and S4 respectively)

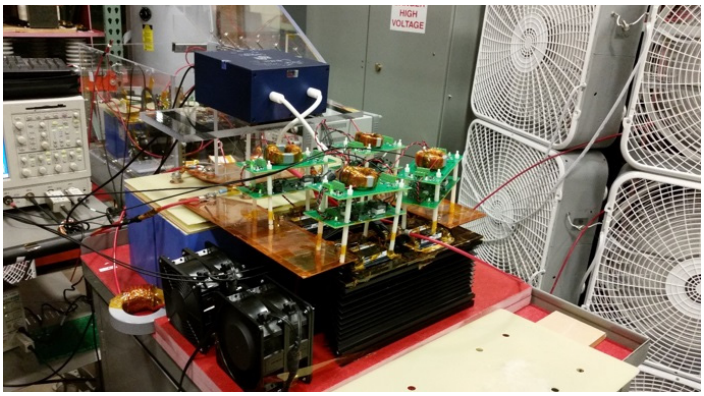


Fig. 4.21: The lab experimental test setup of the H-Bridge converter. The 10 kV dc-dc boost converter inside the plexi glass is in the background.

4.7 Evaluation and Demonstration of multi-chip 15 kV N-IGBT Modules

The results reported in the previous sections and chapters are based on single IGBT chip per module, with size of 0.84cmx0.84cm and active area of 0.32 cm^2. To demonstrate increased current handling capability, two-chip IGBT modules have been designed, whose experimental results are presented in this section. The chip size for the case of two-chip module is increased to 0.84cmx1cm (about 20% more chip size in comparison to the single-chip case) to have reduced thermal resistance. Fig. 4.22 shows the two-chip module design where both the IGBT chips share common gate and current sense terminals. The multi-chip modules have been built using 5 μm field-stop buffer layer as they have found to be more suitable for the TIPS demonstration, as noted earlier.

The 10 kV results presented for the single-chip case in Chapter-2, have shown that the turn-off energy loss is not as strongly dependent on the collector current as the turn-on energy loss. The impact of this on the multi-chip IGBT performance is demonstrated in this section. Fig. 4.23 shows comparison of turn-on and turn-off energy loss of both single-chip and two-chip IGBT modules at 5 kV. The gate resistances used for the two-chip IGBT module are 33 Ω and 10 Ω for turn-on and turn-off respectively, to maintain consistency with the converter

demonstrations results presented in the previous section. The gate resistances used for the single-chip IGBT module are 66 Ω and 20 Ω, for turn-on and turn-off respectively, to have same per-chip gate resistances for both the IGBT modules. From Fig. 4.23, the turn-on loss for both the cases is almost identical. However, there is a significant increase in turn-off loss for the two-chip case. This is due to weak dependency of turn-off loss on the collector current, which is now divided into two chips. Also, the 20% increase in chip area contributed to further increased loss due to increased number of carriers (stored charge). Fig. 4.24 shows variation of the turn-on and the turn-off energy loss with temperature for single-chip IGBT module. With temperature, the turn-off loss at 5 kV, 5 A has increased by a factor of over 3x, whereas, the turn-on loss has slightly decreased. Based on the results shown, it is apparent that decreasing the gate resistance would further reduce the turn-on loss, whereas, the turn-off loss would have negligible impact.

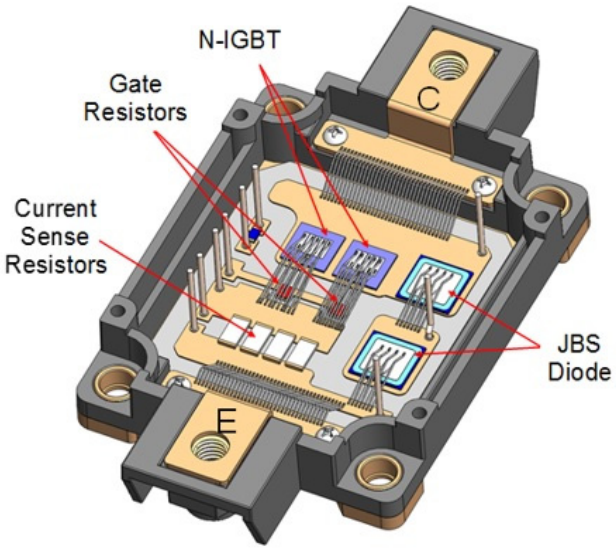


Fig. 4.22: The pictorial view of the two-chip 15 kV IGBT co-pack (Provided by Powerex)

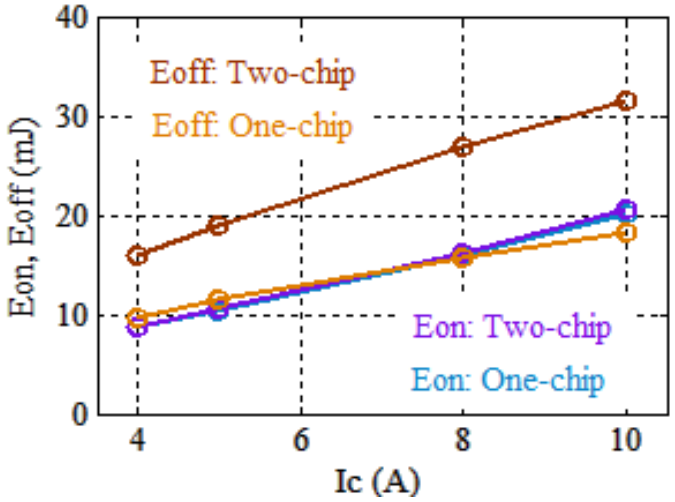


Fig. 4.23: The turn-on energy loss (at 25°C) and turn-off energy loss (at 155°C) comparison of the single-chip and two-chip 15 kV IGBT modules at 5 kV and varying current, with per-chip $R_{G(ON)}$ of 33 Ω and $R_{G(OFF)}$ of 10 Ω.

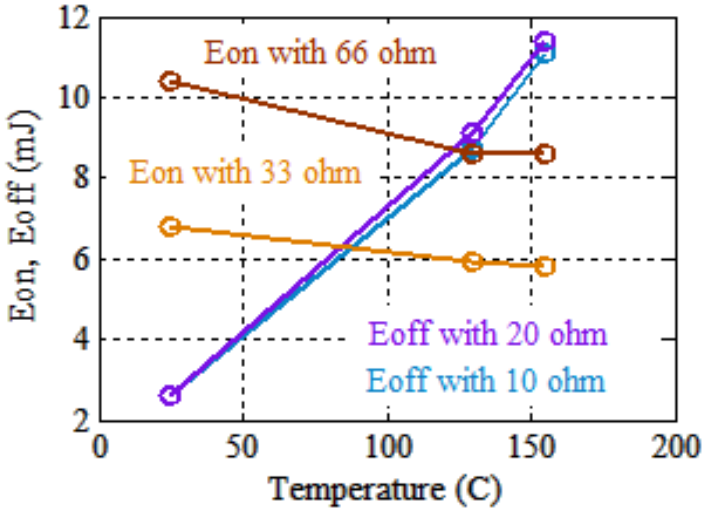


Fig. 4.24: The turn-on and turn-off energy loss comparison at 5 kV and 5 A at different temperature and gate resistances, for single-chip 15 kV IGBT module. $R_{G(ON)}$ values are 66 Ω and 33 Ω; $R_{G(OFF)}$ values are 20 Ω and 10 Ω.

Following the device switching evaluation, the three-level pole tests for the TIPS demonstration have been carried out at 10 kV dc-input (each IGBT stressed to 5 kV). Fig. 4.25 shows operation of a three-level pole with 10 kV dc-input with sine-PWM modulation at 5 kHz and 7.2 kW. Similarly, the results with square PWM are shown in Fig. 4.26 at 5 kHz and 7.2 kW. The reduced frequency in comparison to the results shown in section 5.5 is a precaution due to slight overheating (increased energy loss) from the multi-chip IGBT modules. It should be noted that the junction temperature will be lower in the multi-chip case due to splitting the power dissipation between two chips of larger size. Also, the 3-level voltage waveform in Fig. 4.26 has lower distortion (than that shown in Fig. 4.14) due to adjusted probe compensation. The sine-PWM results are validation for the front-end rectifier stage of the TIPS and square-PWM results for the dc-dc Dual Active Bridge (DAB) stage. Currently, three poles each for FEC and DAB stages have been tested up to 10 kV input for 30 minutes each, suitable for the three-phase TIPS demonstration up to 10 kV dc-link. Fig. 4.27 shows the three-phases of the FEC and the high frequency transformer isolated DAB using the multi-chip IGBT modules.

The objective of demonstrating the 3-level converters presented in this section and the previous section is to validate the complete hardware, thermal management and also its immunity to electromagnetic interference (EMI) without spurious tripping. The 3-level converter needs to be operated up to 22 kV dc-link (IGBT stress is 11 kV) to complete its validation for the TIPS system. However, the two-level H-bridge converter presented in section-III is tested almost to the IGBT limits from the perspective of the operating voltage. It needs further investigation to determine the efficiency of these converters. Unlike the boost converter case, the sinusoidal currents, and their transition from IGBTs to diodes and vice-versa in the H-bridge, are resulting in tedious and inaccurate estimation of efficiency.

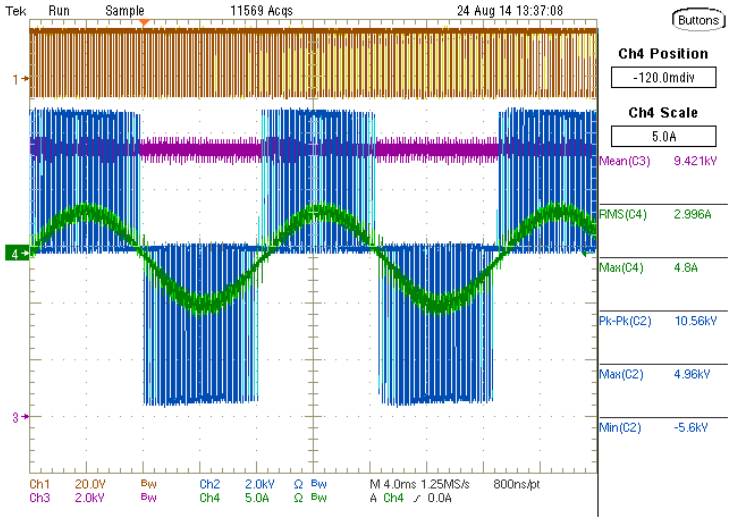


Fig. 4.25: The 3-level pole waveforms with 10 kV dc-input, sine-PWM modulation for rectifier stage at 5 kHz switching and 7.2 kW. [Ch1: V_{GE} of boost converter IGBT, 20 V/div; Ch2: $V_{AC\,(OUT)}$, 2 kV/div; Ch3: Boost converter output, 2 kV/div; Ch4: $I_{AC\,(OUT)}$, 5 A/div; Time: 4 ms/div]

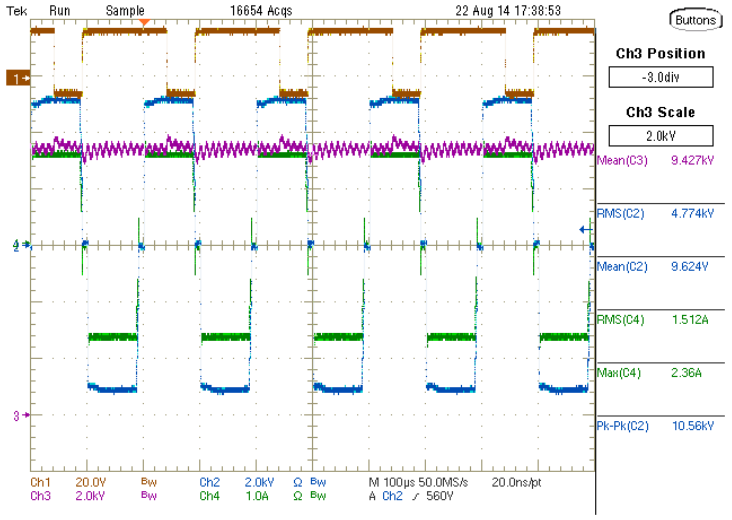


Fig. 4.26: The 3-level pole operation with 10 kV dc-input, square-PWM modulation for DAB stage at 5 kHz and 7.2 kW. [Ch1: V_{GE} of boost converter IGBT, 20 V/div; Ch2: $V_{AC\,(OUT)}$, 2 kV/div; Ch3: Boost converter output, 2 kV/div; Ch4: $I_{AC\,(OUT)}$, 1 A/div; Time: 100 µs/div]

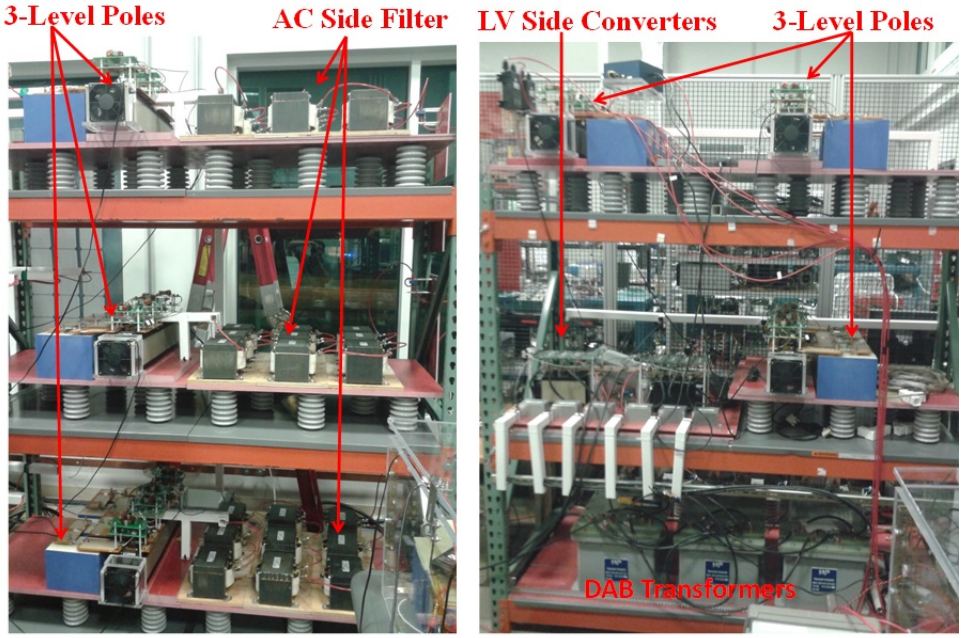


Fig. 4.27: The laboratory test setup of the TIPS system. (a) Front-end converter (rectifier) (b) dc-dc dual active bridge (DAB) with high frequency transformers.

4.8 Conclusions

This chapter is devoted to understanding the practical limits of operation of the 15 kV SiC N-IGBTs. Based on the experimental switching results and the Powerex's package thermal data, the switching frequency limits have been analytically evaluated at 10 kV, 15 A/cm^2 and 30 A/cm^2, based on experimental switching data under both liquid and air cooling conditions for a maximum operating junction temperature of 150^{o}C. These limits are experimentally validated on 10 kV boost converter heat-run demonstration with 550 W/cm^2 (active area) with junction temperature of 146^{o}C at the end of one hour, where the junction temperature has reached a steady value. An easy and reliable method of online estimation of IGBT junction temperature, based on the turn-off voltage punch-through transition point, has been provided. The experimental total energy loss in the IGBT is evaluated at that particular junction temperature. Following this, the SiC IGBT is demonstrated on 10 kV dc-input three-level NPC

converter at 10 kHz, 9 kW with resistive loading. The IGBT is exposed to a steady state voltage stress of 5 kV in this converter. The heatsink has been referenced to dc-bus mid-point to limit the stress on baseplates of all IGBT and diode modules to 5 kV. Subsequently, the IGBT is demonstrated on a single-phase H-Bridge converter with 10 kV dc-input to exploit their full potential from the perspective of practical operating voltage.

The evaluation of energy losses for two-chip SiC IGBT module and the comparison with single-chip IGBT module is provided. At 5 kV, the turn-off energy losses in the multi-chip module are found to be significantly larger, corroborating the results presented in Chapter-2 on variation of the turn-off energy loss with current. Finally, the two-chip IGBT modules have been demonstrated on three-level converter poles with 10 kV dc-input, 5 kHz and 7.2 kW with sine-PWM and square-PWM modulation schemes. In total, six three-level NPC poles have been validated for 30 minutes each, with 10 kV dc-input for the TIPS system - three poles for the front-end rectifier stage with SPWM modulation, and the remaining three for the HV DAB side with square-PWM.

Chapter 5
Understanding dv/dt of 15 kV SiC N-IGBTs and Active Gate Control

5.1 Introduction

It has been reported for silicon (Si) IGBTs and MOSFETs that the high dv/dt generated during switching transitions is detrimental for the operation of power conversion system due to common-mode current flow through the heat-sinks [20], insulation and bearing failure of motors [21]-[23]. Also, the integration of high frequency magnetics into the power converter system is difficult due to parasitic capacitive currents resulting from high dv/dt [24]. As mentioned in earlier chapters, the gate driver isolation stage also need to be designed for high dv/dt signal immunity along with thicker insulation layer for reliable operation. These effects can be minimized by controlling the gate current, or by using snubber capacitors to reduce the dv/dt, which increase the switching energy loss. Also, it is proposed to use EMI filters [25] with the converters for limiting the dv/dt, but this adds to the size, weight and cost of the converter system.

The state-of-the-art ultrahigh voltage 15 kV SiC IGBTs have steep voltage transitions above the punch-through voltage, as shown in Chapter-2. So, it is of considerable interest for a power converter designer to understand the reason for this high dv/dt generation and the methods to mitigate it, which are addressed in this chapter.

5.2 Understanding dv/dt of 15 kV SiC N-IGBTs

The SiC IGBTs exhibit two distinct voltage transitions during turn-off and turn-on switching. The voltage transition above the punch-through voltage (about 5 kV) is much steeper than that

during the diffusion phase (under 5 kV), during both turn-on and turn-off conditions. This section is devoted to understanding this behavior with varying current, temperature and buffer layer thicknesses based on the experimental measurements. The explanation provided here is primarily for the turn-off transition, where the carriers in the drift and buffer layers are at a steady concentration before the initiation of the transition, making it easier to analyze. It is expected that the same reasoning is valid for the turn-on transition as well, however, the diffusion times, carrier mobility and conductivity modulation lag (forward recovery) may have additional impact on the turn-on switching dv/dt (which is beyond the scope of this thesis).

5.2.1 Turn-off Transition at 11 kV, 10A and 25°C

The turn-off transition at 11 kV, 10 A, 25°C with $R_{G(OFF)}$ of 10 Ω is shown in Fig. 5.1. The voltage is rising slowly until about 5 kV (before punch-through), followed by steep rise from 5 kV to 11 kV (after punch-through). This can be explained from the carrier concentration profile of the lightly doped ($2x10^{14}cm^{-3}$) drift and heavily doped buffer layer (of thickness 2 µm) of the SiC IGBT.

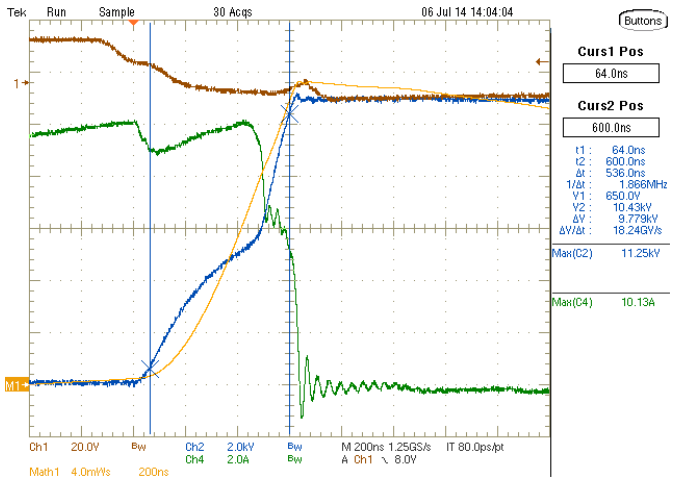


Fig. 5.1: Turn-off transition of 15 kV, 2 µm IGBT at 11 kV, 10 A, 25°C with $R_{G(OFF)}$ of 10 Ω. [Ch1: V_{GE} (20 V/div); Ch2: V_{CE} (2 kV/div); Ch4: I_C (2 A/div); Math1: Energy loss (4 mJ/div)]

Fig. 5.2 shows representation of the carrier concentration (on a log scale) along the drift and buffer layers. As the IGBT depletion layer expands (starting from 0 µm, the junction of N-drift and P-base) the number of excess carriers to be removed increases at an exponential rate which slows down the voltage rise as the voltage reaches punch-through point (about 5 kV in Fig. 5.1). The depletion expansion in the drift layer results in triangular electric field profile (lines a and b in Fig. 5.3) until the depletion reaches the junction of the drift and the buffer layers. Beyond this, the depletion region is expanded very little (solid vertical line in the buffer layer of Fig. 5.2) into the highly doped buffer layer. As a result, the electric field profile changes from triangular to trapezoidal (case c in Fig. 5.3), accommodating a significantly larger voltage blocking capability (the area under the curve), essentially at the same depletion thickness.

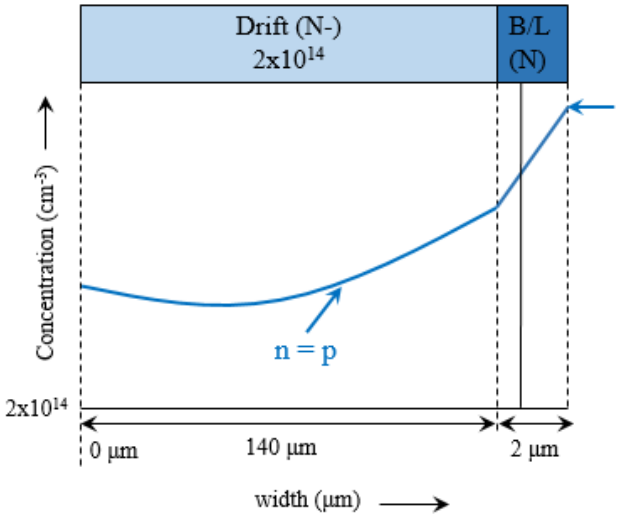


Fig. 5.2: Representation of carrier concentration in the drift and buffer layer (B/L) of the 15 kV SiC IGBT under high level injection conditions (y-axis on log scale).

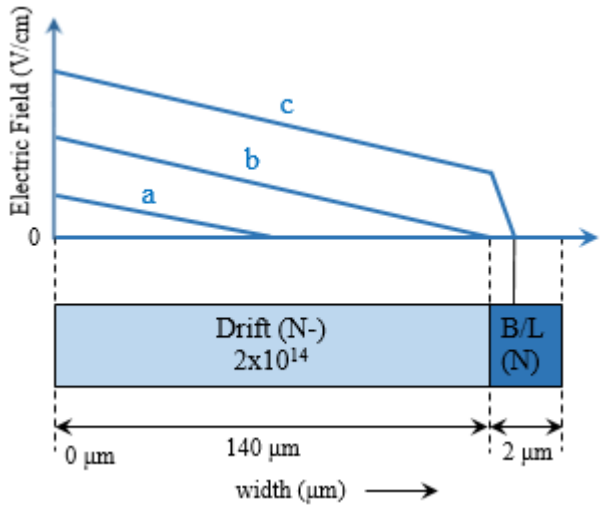


Fig. 5.3: A depiction of electric field profile as the drift and buffer layers are depleted during the turn-off process of the SiC IGBT.

It should be noted that charge (carriers) that needs to be removed from the punch-through point (5 kV) to 11 kV corresponds to that stored in the negligible width of the buffer layer that is depleted (shown with the solid vertical line in the buffer layer of Fig. 5.3) for attaining the trapezoidal field profile. The steep rise in voltage from 5 kV to 11 kV can be explained from this fact that the charge that needs to be extracted is negligible (for changing the electric field from triangular profile to trapezoidal profile). In other words, the IGBT capacitance (= $\Delta Q/\Delta V$) is very low beyond 5 kV due to very little charge (carriers) removal needed per unit voltage rise.

5.2.2 dv/dt with Current Variation at 11 kV and 25°C

The clamped inductive turn-off dv/dt with current variation at 11 kV, 25°C with $R_{G(OFF)}$ of 10 Ω is shown in Fig. 5.4. The voltage transitions before and after the punch-through are steeper with increase in current. The faster voltage rise at higher current can be explained by the fact that the stored charge needs to be removed at a faster rate to maintain the inductive load current. The turn-off dv/dt values at 11 kV with varying current are shown in Fig. 5.5.

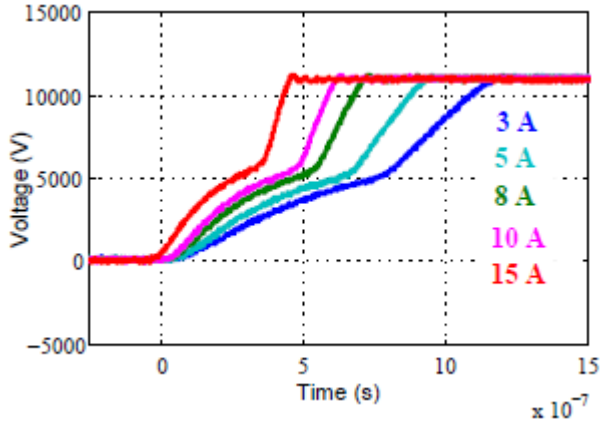


Fig. 5.4: Turn-off voltage transitions of 15 kV, 2 µm thick buffer layer, SiC IGBT at 11 kV, 25°C with $R_{G(OFF)}$ of 10 Ω, with varying load current.

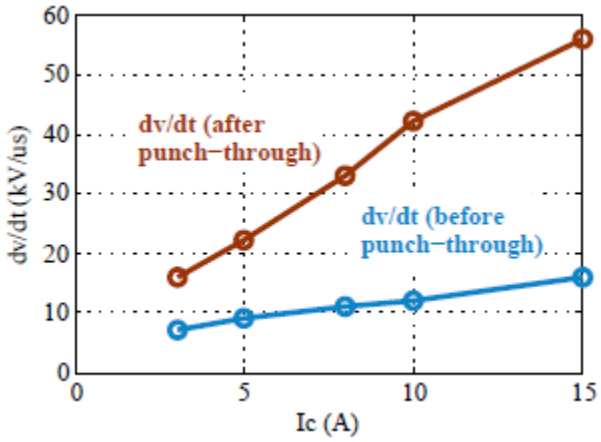


Fig. 5.5: Turn-off dv/dt values of 15 kV, 2 µm thick buffer layer, SiC IGBT at 11 kV, 25°C with $R_{G(OFF)}$ of 10 Ω, with varying load current.

Equation (5.1) [9] shows the analytical expression for the dv/dt (after the punch-through). The depletion capacitance C_{SCR}, shown in equation (5.2) [9], is 61.3 pF/cm^2 (or 19.6 pF, considering 0.32 cm^2 active area of the IGBT). The dv/dt calculated at 10 A is 17.6 kV/µs, which is significantly different from the measured value of 41.7 kV/µs. However, from the normalized dv/dt values shown in Fig. 5.6, with respect to 10 A, the measured and calculated dv/dt values are fitting to a good extent. Considering the equation (5.1), the L_{pNB} and C_{SCR} used for this IGBT

could have caused the variation between the absolute dv/dt values. The value L_{pNB} is dependent on hole mobility value [26] and carrier lifetime value [27] in the buffer layer. It was attempted to calculate normalized voltage rise time, t_{RT}, before punch-through, but the values are not consistent with the experimentally measured values shown in Fig. 5.4. It needs further investigation to understand the difference between the experimentally measured and calculated values. However, the measured voltage rise time, t_{RT} decreased with the collector current as predicted by the equation (5.3) [9].

$$\frac{dV_C}{dt} = \frac{J_{C,ON}}{C_{SCR}}\left[1 - \frac{1}{\cosh(W_{NBL}/L_{pNB})}\right] \qquad (5.1)$$

$$C_{SCR} = \frac{\varepsilon_S}{W_N} \qquad (5.2)$$

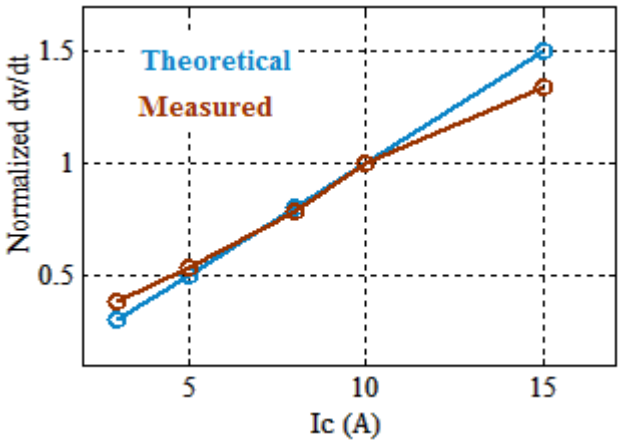


Fig. 5.6: The measured and calculated normalized dv/dt values after punch-through at 11 kV, 10 A, 25°C.

As shown in Fig 5.4, the punch-through voltage transition point (the depletion is at the edge of the drift and buffer layers) of the IGBT is slightly decreasing with increase in collector current.

This is in conformity with the analytical expression given by (5.4) [9]. Fig. 5.7 shows the consistency of the measured and calculated normalized punch-through transition points, measured with reference to the values at 11 kV, 10 A and 25°C.

$$t_{RT} = \frac{qL_a p(W_{NB+})}{J_{C,ON}} \left\{ \frac{\cosh[W_N/L_a] - \cosh[W_{SC}(0)/L_a]}{\sinh[(W_N + W_{NB})/L_a]} \right\} \tag{5.3}$$

$$V_{RT}(J_{C,ON}) = \frac{q(N_D + p_{SC})W_N^2}{2\varepsilon_S} \tag{5.4}$$

$$p_{SC} = \frac{J_{C,ON}}{qv_{sat,p}} \tag{5.5}$$

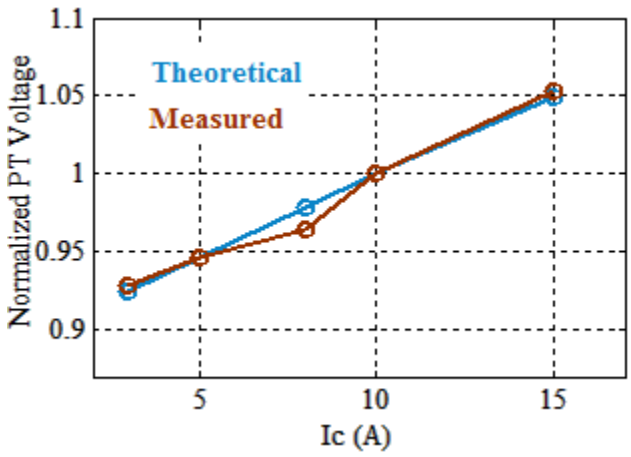


Fig. 5.7: The measured and calculated normalized punch-through transition voltage values with reference to the punch-through voltage at 11 kV, 10 A, 25°C.

5.2.3 dv/dt with Increased Buffer Layer Thickness

Fig. 5.8 shows turn-off transition of 2 µm and 5 µm buffer layer IGBTs at 10 kV and 10 A. Both the IGBTs have same drift layer parameters and same buffer layer doping, except for its thickness. The turn-off transition of the 5 µm buffer layer IGBT is much faster than that of the 2 µm buffer layer IGBT due to lower carrier concentration in the drift and buffer layers as depicted in Fig. 5.9. The lower charge in the 5 µm buffer layer IGBT is resulting from larger exponential decay of the injected carriers (in the thicker and highly doped buffer layer) before reaching the junction of the buffer layer and the drift layer. The solid vertical line in Fig. 5.9 indicates the depletion width penetrated into the field-stop buffer layer.

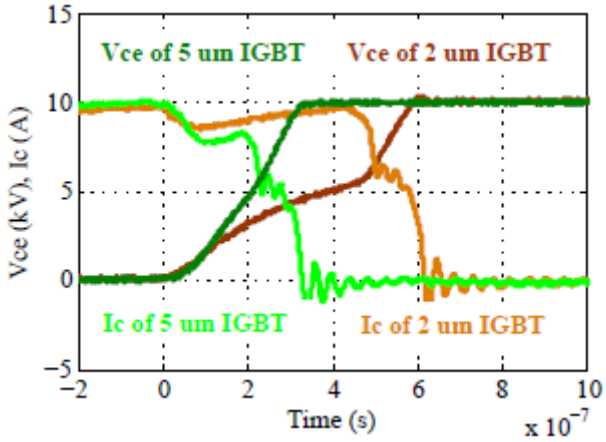


Fig. 5.8: Turn-off transitions of 15 kV, 2 µm and 5 µm thick buffer layer, SiC IGBT at 10 kV, 10 A, 25°C with $R_{G(OFF)}$ of 10 Ω.

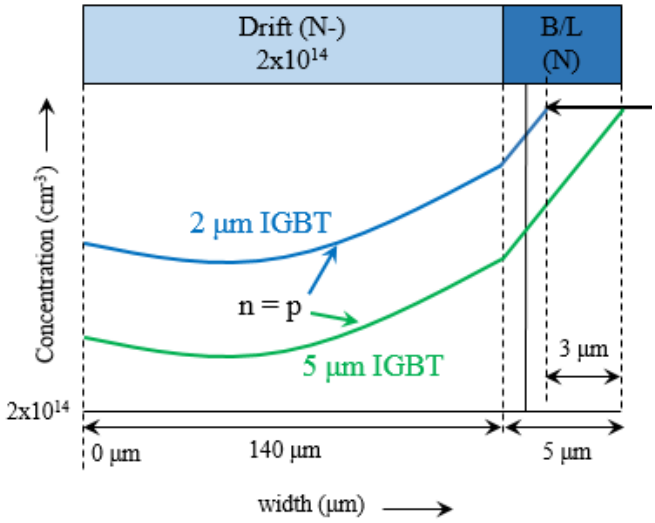


Fig. 5.9: Representation of carrier profile in the 2 µm and 5 µm buffer layer thick SiC IGBTs (y-axis on log scale).

The turn-on transitions of both the IGBTs at 10 kV, 8 A are shown in Fig. 5.10. The 2 µm IGBT has significantly higher dv/dt above the punch-through voltage resulting in a large current spike due to discharge of the capacitance of the free-wheeling diode of the clamped inductive circuit used for the tests. It should be noted that the current waveform of the 2 µm buffer layer IGBT is scaled to 0.33x in Fig. 5.10. The full scale waveform along with the gate signal is shown in Fig. 5.11. The ringing in the gate voltage is due to the high di/dt probe pickup resulting from the discharge of the capacitance of the free-wheeling diode. The reason for lower turn-on dv/dt (above punch-through voltage) of 5 µm IGBT is reduced injection as shown in Fig. 5.9. It needs further investigation to determine why the turn-on dv/dt for both the devices is almost same under the punch-through voltage, and why the punch-through transition voltage (during turn-on) is about 7 kV for 5 µm IGBT, whereas it is 5 kV for 2 µm IGBT. Table 5.1 summarizes the dv/dt values of both the devices at 25ºC with $R_{G(ON)}$ = 50 Ω and $R_{G(OFF)}$ = 10 Ω.

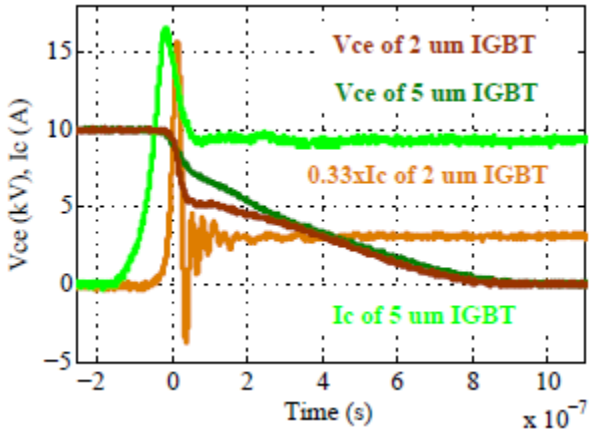


Fig. 5.10: Turn-on transitions of 15 kV, 2 µm and 5 µm thick buffer layer, SiC IGBT at 10 kV, 8 A, 25ºC with $R_{G(ON)}$ of 50 Ω. (The 2 µm IGBT current is scaled down to 0.33x to accommodate the current spike).

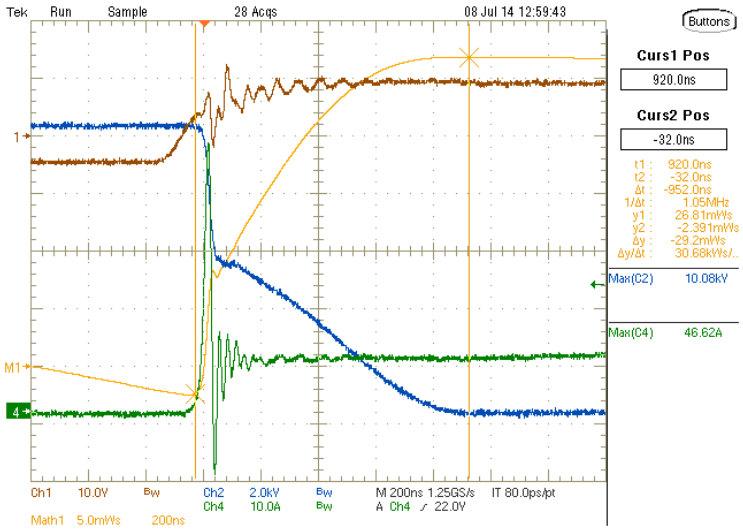


Fig. 5.11: Turn-on transitions of 15 kV, 2 µm thick buffer layer, SiC IGBT at 10 kV, 8 A, 25ºC with $R_{G(ON)}$ of 50 Ω (full scale waveform). [Ch1: V_{GE} (10 V/div); Ch2: V_{CE} (2 kV/div); Ch4: I_C (10 A/div); Math1: Energy loss (5 mJ/div)]

Table 5.1: dv/dt of 2 µm and 5 µm IGBTs at 10 kV, 8 A (turn-on) and 10 A (turn-off)

Parameter	2 µm IGBT (kV/µs)	5 µm IGBT (kV/µs)
Turn-on dv/dt (above PT)	135	39
Turn-on dv/dt (under PT)	7.3	9.0
Turn-off dv/dt (before PT)	12	30
Turn-off dv/dt (after PT)	39	47

5.2.4 dv/dt with Temperature

The dv/dt of the 5 µm IGBT is evaluated at 8 kV, 5 A from 25°C to 106°C, during both turn-on ($R_{G(ON)}$ = 50 Ω) and turn-off ($R_{G(OFF)}$ = 10 Ω) transitions, as shown in Fig. 5.12. The turn-off dv/dt below punch-through (PT) voltage is slowed down significantly due to excess carriers stored in the drift region because of increased injection from the backside p+ injector at higher temperature, depicted in Fig. 5.13. The higher injection during turn-on transition also has resulted in increased dv/dt above and below the PT voltage.

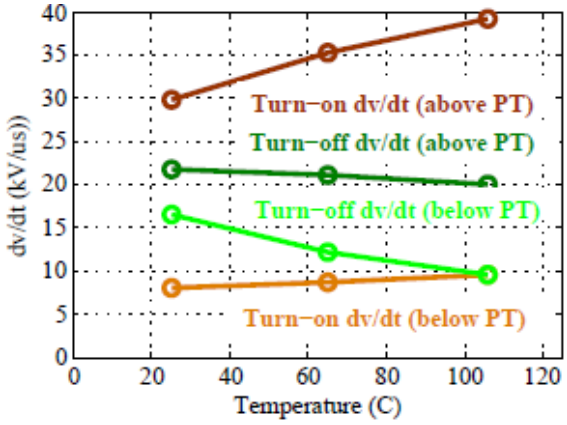


Fig. 5.12: Turn-on and turn-off dv/dt variation with temperature of 5 µm thick buffer layer SiC IGBT at 8 kV, 5 A with $R_{G(ON)}$ of 50 Ω and $R_{G(OFF)}$ of 10 Ω.

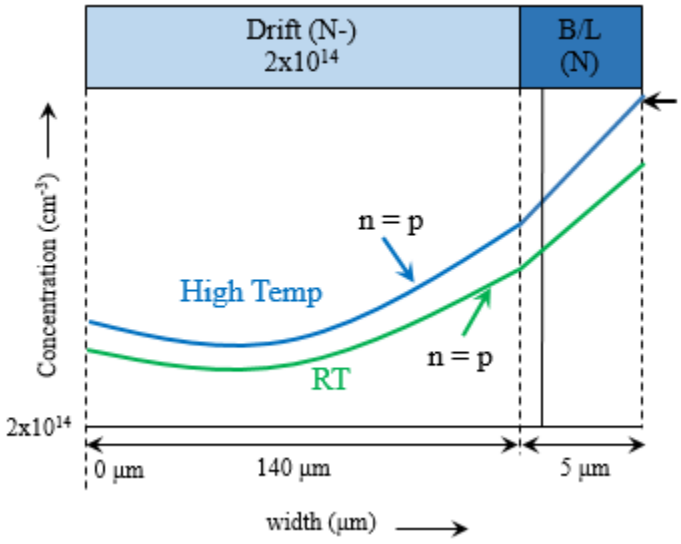


Fig. 5.13: Representation of carrier profile in the 15 kV SiC IGBTs with respect to temperature (y-axis on log scale).

The turn-off dv/dt (after PT) has been analytically evaluated based on the equation (5.1). The only temperature dependent component in the equation is L_{pNB} (diffusion length of holes in N-buffer layer) which is given by the equation (5.6) where hole mobility (μ_p) and carrier life-time (τ) are temperature dependent [26]. Based on the mobility equation (5.7) [$\alpha_p = 2.8$] and life-time equation (5.8) [$\beta = 3.2$], the temperature dependency of the L_{pNB} can be derived as shown in the equation (5.9). As the mobility reduces with temperature and the carrier life-time increases with temperature, these two opposite effects have been almost nullified each other as per this equation. Based on this equation, the turn-off dv/dt (above PT) reduction has been analytically calculated to be 7.5 % from 25°C to 106°C. This is in agreement with the experimentally measured values shown in Fig. 5.12 where the reduction is 7.3 %. The different parameters used for this analysis are shown in Table. 5.3. The different constants have been referenced from [26].

$$L_{pNB} = \sqrt{\frac{kT}{q}\mu_p \tau} \tag{5.6}$$

$$\mu_p = \frac{\mu_{max\_p}(T/300)^{-\alpha_p}}{1 + [(N_D + N_A)/N_{ref\_p}]^{\gamma_p}} \tag{5.7}$$

$$\tau_{n,p} = \frac{\tau_{max}(T/300)^{\beta}}{1 + [(N_D + N_A)/N_{ref\_\tau}]^{\sigma}} \tag{5.8}$$

$$L_{pNB} \propto \left(\frac{T}{300}\right)^{0.2} \tag{5.9}$$

Table 5.2: Parameters used in the analytical evaluation

Parameter	**Description**	**value**
N_D	Drift layer doping concentration	$2x10^{14}$ cm^{-3}
N_{BL}	Buffer layer doping concentration	$3x10^{17}$ cm^{-3} [27]
N_{P+}	P+ substrate doping concentration	$2x10^{19}$ cm^{-3} [assumed]
W_N	Drift layer width	140 µm
W_{NBL}	Buffer layer width	2 µm, 5 µm
μ_{max_n}	Electron mobility at 25ºC (low N_D)	950 cm^2/Vs [26], [27]
μ_{max_p}	Hole mobility at 25ºC (low N_D)	124 cm^2/Vs [26], [27]
τ_{HL}	High-level carrier life time	2.13 µs [27]
τ_{LL}	Low-level carrier life time	0.219 µs [27]

5.3 Active Gate Current Control of 15 kV SiC N-IGBT

The 2 µm field-stop buffer layer SiC IGBT has been chosen for this investigation, as it has higher turn-on dv/dt as shown in the previous section. Based on the results presented in section 5.2, the dv/dt over punch-through (PT) during the turn-on transition is much higher than that during the turn-off. Therefore, the turn-on dv/dt control is being investigated in this section with the fundamental technique of controlling gate current described by (5.10) to limit the rate of discharging the miller capacitance of the IGBT. The $R_{G(ON)}$ is increased to minimize the dv/dt by controlling the gate current. The gate resistance circuit of the gate driver is shown in Fig. 5.14. The Fig. 5.15 shows variation of the PT turn-on dv/dt and the energy loss with increase in $R_{G(ON)}$, at 11 kV, 8 A, 25°C. The turn-on dv/dt is reduced from 153 kV/µs to 119 kV/µs when the $R_{G(ON)}$ is increased from 50 Ω to 300 Ω. However, larger $R_{G(ON)}$ values have drastically increased the turn-on energy loss, as shown. The increase in the turn-on energy loss is attributed to the slow-down of voltage fall during the diffusion phase (below PT voltage) and thus increasing the switching transition duration, as shown in Fig. 5.16.

$$i_{G(ON)} = (+V_{GG} - V_M)/R_{G(ON)} \qquad (5.10)$$

where, $i_{G(ON)}$ is the on gate current, $+V_{GG}$ is the positive gate supply, V_M is the miller plateau voltage and $R_{G(ON)}$ is the turn-on gate resistance.

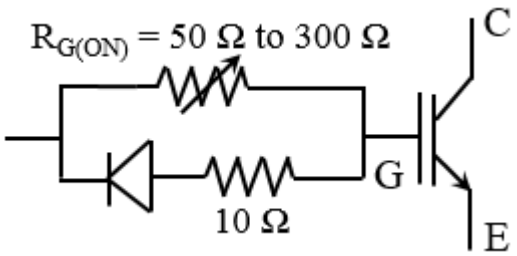


Fig. 5.14: The gate resistance configuration used for the non-active gating of the 15 kV SiC IGBT.

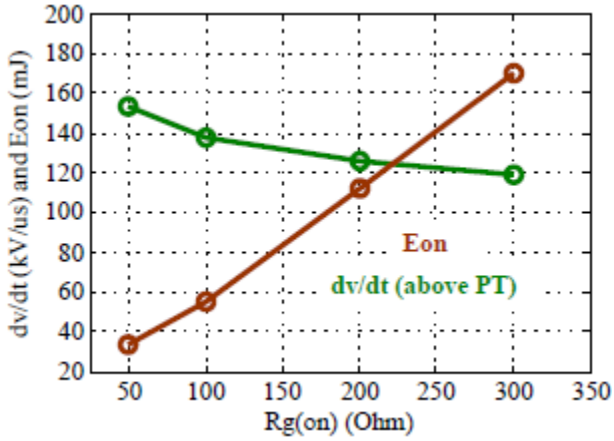


Fig. 5.15: The turn-on dv/dt and the energy loss with increase in $R_{G(ON)}$ from 50 Ω to 300 Ω, at 11 kV, 8 A and 25°C of 2 µm, 15 kVIGBT.

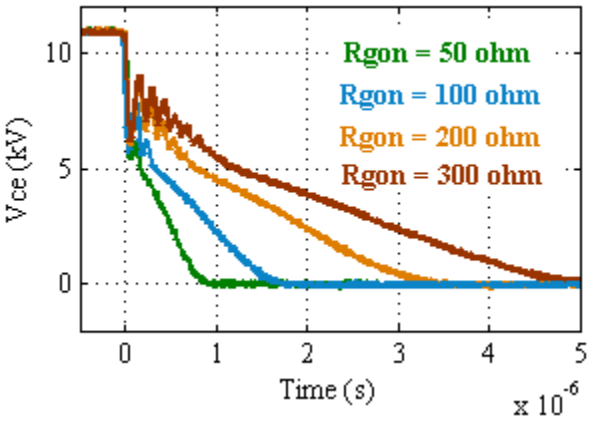


Fig. 5.16: The voltage transitions with increase in $R_{G(ON)}$ from 50 Ω to 300 Ω, at 11 kV, 8 A and 25°C of the 2 µm, 15 kV IGBT using non-active gate driver.

Thus, the punch-through (PT) turn-on dv/dt is found to be weakly dependent on $R_{G(ON)}$, while adding significant turn-on loss in the diffusion phase of the transition. This problem can be overcome by using active gate control techniques widely reported for commercial Si IGBTs [28]-[30]. A large $R_{G(ON)}$ can be used to limit the PT turn-on dv/dt, followed by a small $R_{G(ON)}$ in the diffusion phase to minimize the energy loss. So, the IGBT miller capacitance is

discharged in two different phases to achieve the twin objectives of reducing dv/dt without increasing the energy loss. The gate driver resistance configuration of the active gating is shown in Fig. 5.17, where the gate resistance is varied from 100 Ω to 300 Ω in the depletion phase (above PT), and a 10 Ω is used in the diffusion phase (below PT) of the turn-on transition.

The IGBT gate waveform under the two-stage active driving conditions is depicted in Fig. 5.18. The $R_{G(ON)}$ is switched from high value (100 Ω to 300 Ω) to 10 Ω at time instant, t_4. This instant should ideally correspond to the PT voltage transition point. An RC delay based circuit is used to switch from high $R_{G(ON)}$ to low $R_{G(ON)}$. The measured gate voltage waveform with and without acting gating at zero collector bias with $R_{G(ON)}$ of 200 Ω is shown in Fig. 5.19. The reduction of turn-on switching loss at 11 kV, 8 A, 25°C on the 2 μm buffer layer IGBT with the active gating is shown in Fig. 5.20. The corresponding voltage transition plots (all of them taking less than 1 μs) are shown in Fig. 5.21. In contrast, the voltage transitions shown for the non-active case in Fig. 5.16, have taken much longer duration causing considerably higher switching loss.

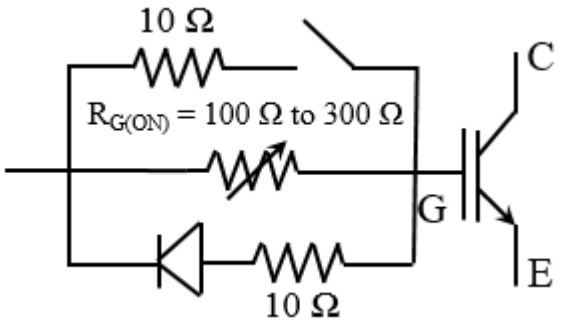


Fig. 5.17: The gate resistance configuration used for the active gating of the 15 kV SiC IGBT.

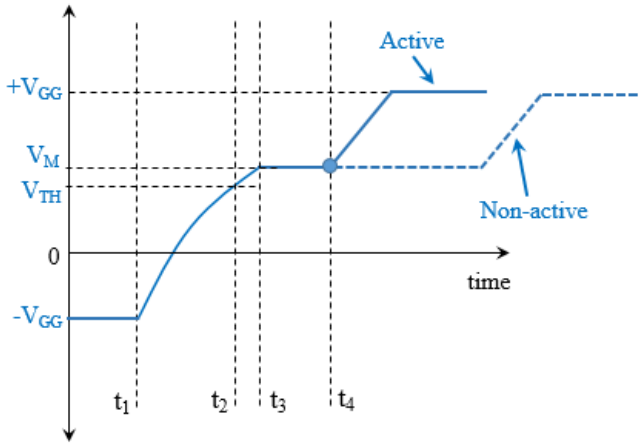


Fig. 5.18: The representation of two-stage active vs. non-active gate waveforms showing different instants during turn-on transition.

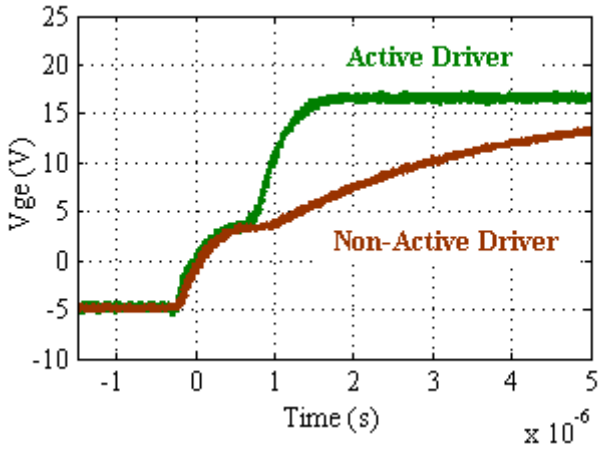


Fig. 5.19: The gate voltage of the IGBT with $R_{G(ON)}$ of 200 Ω, at zero collector bias for both non-active and active gate driving cases.

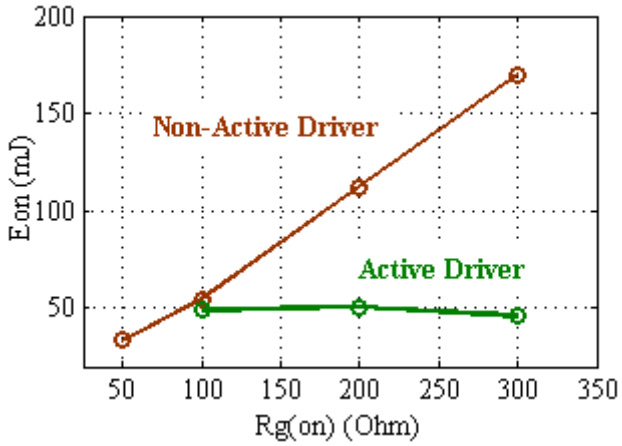


Fig. 5.20: The variation of the energy loss with $R_{G(ON)}$ from 50 Ω to 300 Ω, at 11 kV, 8 A and 25°C of the 2 μm, 15 kV IGBT with non-active and active gating.

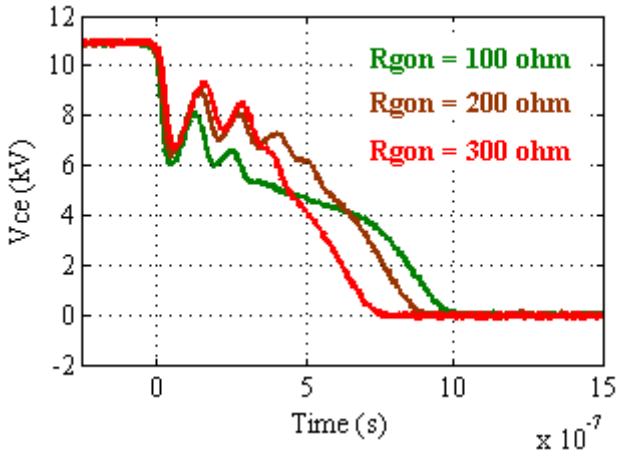


Fig. 5.21: The voltage transitions with increase in $R_{G(ON)}$ from 100 Ω to 300 Ω, at 11 kV, 8 A and 25°C of the 2 μm, 15 kV SiC IGBT using active gate driver.

As mentioned above, the RC delay used in the active driver for switching $R_{G(ON)}$ from high value to low value should exactly correspond to the PT voltage point to achieve optimal switching loss and the dv/dt values simultaneously. From Fig. 5.20, the turn-on loss

corresponding to $R_{G(ON)}$ of 300 Ω is lower than that for the $R_{G(ON)}$ of 100 Ω, indicating the delay is optimal for the 300 Ω case. This is verified from the IGBT voltage transitions corresponding to both the cases shown in Figs. 5.22 and 5.23 for $R_{G(ON)}$ of 300 Ω and 100 Ω respectively. The case with $R_{G(ON)}$ of 300 Ω has the gate resistance switched from high to low just after the PT voltage point. However, the transition point for the $R_{G(ON)}$ of 100 Ω is towards the end of the diffusion phase as shown in Fig. 5.23, resulting in larger switching loss. This is due to the same RC delay used for both the conditions, which is actually optimized for the higher $R_{G(ON)}$ case. This emphasizes the importance of appropriate timing to switch from high $R_{G(ON)}$ to low $R_{G(ON)}$. A larger delay would increase the turn-on loss like the case presented, and shorter delay would have eliminated the fundamental advantage of limiting the dv/dt.

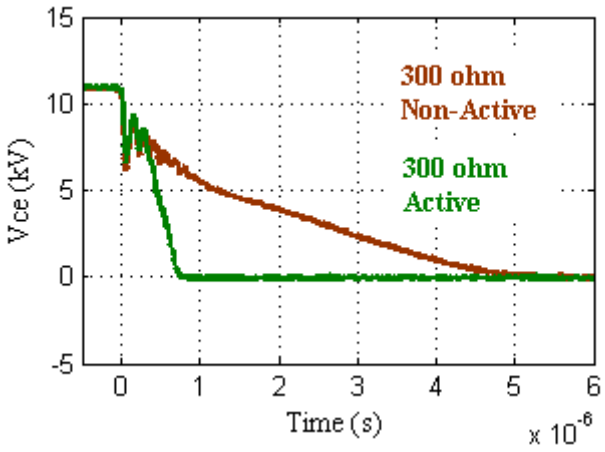


Fig. 5.22: The IGBT turn-on voltage transitions at 11 kV, 8 A and 25ºC of the 2 μm, 15 kV IGBT with $R_{G(ON)}$ of 300 Ω under non-active and active gating.

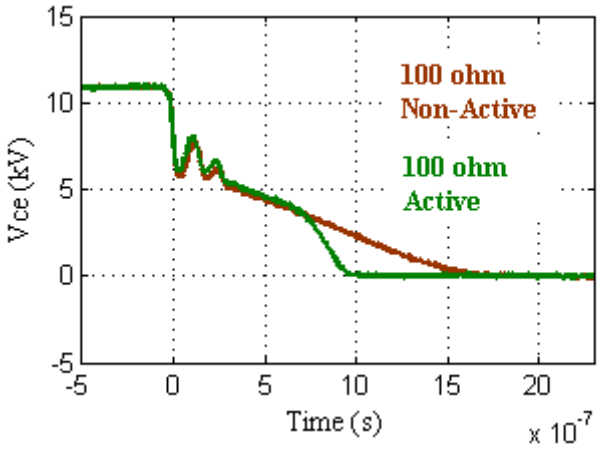


Fig. 5.23: The IGBT turn-on voltage transitions at 11 kV, 8 A and 25°C of the 2 μm, 15 kV IGBT with $R_{G(ON)}$ of 100 Ω under non-active and active gating.

This two-stage active gate driver (basically two different gate resistances during switching transient) would decrease the rate of rise of gate voltage until small $R_{G(ON)}$ is turned-on, which can cause increased delay times (consequently dead-times and harmonic voltage) in the power converters. This can be addressed by using another low gate resistance from the t_1 (initiation of the turn-on transient) to t_2 (threshold voltage point) instants shown in Fig. 5.18, resulting in three-stage active driving [30], represented by equation (5.11). A lookup table based control can be implemented for optimal delay generation to accommodate the IGBT parameter variation with temperature and current, which is a scope for future research.

Where, $R_{G(ON)1}$ and $R_{G(ON)3}$ are low resistance values, and $R_{G(ON)2}$ is very high gate resistance.

$$i_{G(ON)}(t) = \begin{cases} [[V_{GG} - V_G(t)]/R_{G(ON)1}], & \text{for } t_1 < t < t_2 \\ [[V_{GG} - V_G(t)]/R_{G(ON)2}], & \text{for } t_2 < t < t_4 \\ [[V_{GG} - V_G(t)]/R_{G(ON)3}], & \text{for } t > t_4 \end{cases} \quad (5.11)$$

5.4 Summary

This chapter outlines the possible impacts of the high dv/dt generated by the SiC N-IGBTs in power conversion systems, followed by a study on understanding the two-stage switching voltage transitions of the 15 kV SiC N-IGBTs with varying current, temperature and buffer layer thickness, taking the turn-off transient as the reference. A reasonably good match between the analytically evaluated and measured data is found between the normalized values of turn-off dv/dt over punch-through voltage. But, there is a considerable difference between them if the absolute values are considered. However, the objective of this chapter was to get a basic understanding of the physical quantities that are defining the dv/dt of the IGBT. A detailed investigation with exact mobility, and lifetime values needs to be done to completely match the analytical and measured values, which is scope for future study.

Considering that the turn-on dv/dt (above punch through voltage) is higher than any other dv/dt of the IGBT, a conventional gate current control technique is implemented at 11 kV, 25^{o}C for its control. It was shown that increasing the $R_{G(ON)}$ from 50 Ω to 300 Ω has reduced the dv/dt from 153 kV/µs to 119 kV/µs. But it has resulted in considerable increase in energy loss from 30 mJ to 170 mJ due to prolonged duration of the voltage transition in diffusion phase, for the 2 µm buffer layer at 11 kV, 8 A and 25^{o}C. The two-stage active gate current control technique demonstrated the twin objectives of reduced dv/dt without increasing energy loss at 11 kV. As a future research, a three-stage active gate driver can be investigated to achieve further optimized performance by reducing the gate voltage rise time until the threshold point.

Chapter 6

Design Considerations for 12 kV SiC IGBTs based ZVS Converters

6.1 Introduction

As noted in the previous chapters, the SiC IGBTs generate extremely high dv/dt due to the abrupt punch-through design. Also, the high isolation requirement in the base-plate of the module has resulted in 0.49^{o}C/W thermal resistance from the junction of the IGBT to the top of the heatsink. This coupled with the high power dissipation densities limit the switching frequency of the IGBTs as explained in Chapter-4. The high dv/dt also lead to reliability issues in the power conversion system due to common-mode current flow as outlined in Chapter-5. All these can be addressed if a soft-switching technique is employed that provides slower dv/dt while minimizing the power loss of the IGBT. Therefore, the zero voltage switching (ZVS) scheme [31]-[32] with an external capacitive snubber is evaluated for the 2 μm and 5 μm buffer layer IGBTs up to 5 kV turn-on and turn-off switching transitions. To understand the behavior of IGBT current, 12 kV discrete devices have been evaluated, in contrast to the 15 kV co-pack modules used in the earlier chapters.

6.2 ZVS Turn-on Characteristics

Under ZVS conditions, the turn-on gate bias is provided for the IGBT just before the circuit gets configured to conduct current through it. Despite formation of the MOS channel, the conductivity modulation lag (forward recovery) [1], [33] in the drift region results in higher forward drop (V_{CE}) across the IGBT, when the current starts to flow with reasonable di/dt. Once the drift layer is fully modulated, the V_{CE} of the IGBT settles down to steady state saturation

value. Consequently, higher di/dt results in higher voltage spike because of instant high current availability in the unmodulated drift region.

Fig. 6.1 and Fig. 6.2 show the turn-on voltage spike under different di/dt conditions for the 2 µm and 5 µm buffer layer IGBTs respectively. The voltage spike has increased from 6 V to over 15 V when the di/dt is increased from 1 A/µs to 10 A/ µs for both IGBTs. Also, it can be noticed that the 5 µm IGBT has about 1 V higher steady state voltage drop, as explained in Chapter-2. The reduced mobility at high temperature [1] also increases the resistance of unmodulated drift that result in higher voltage spike. Fig. 6.3 shows the effect of temperature on the voltage spike for the 5 µm buffer layer IGBT. Similar behavior is observed for the 2 µm buffer layer IGBT. The voltage spike is found to have negligible influence due to package inductance.

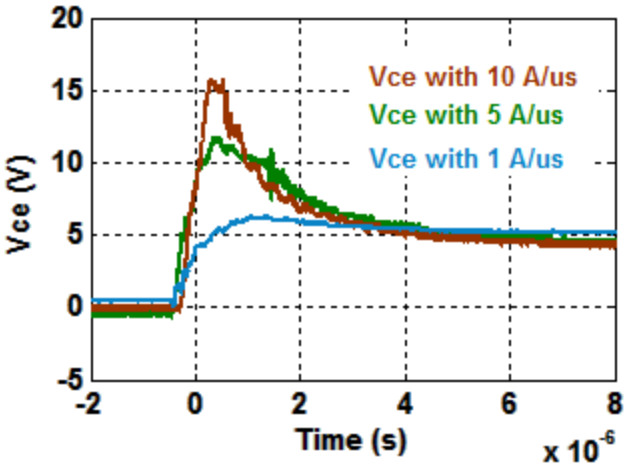


Fig. 6.1: Turn-on voltage spike of 12 kV, 2 µm buffer layer SiC IGBT under different di/dt conditions at 150ºC.

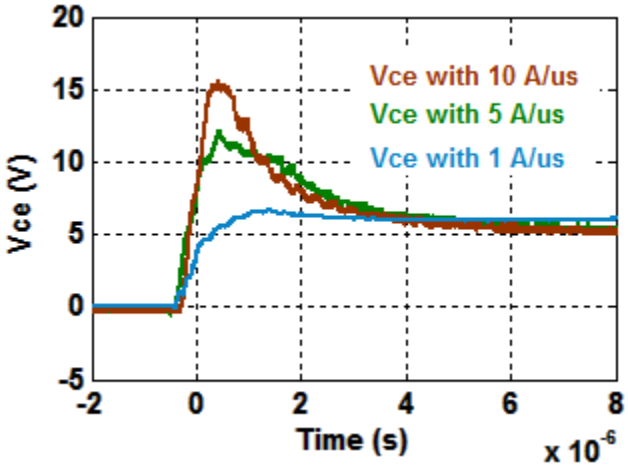


Fig. 6.2: Turn-on voltage spike of 12 kV, 5 µm buffer layer SiC IGBT under different di/dt conditions at 150ºC.

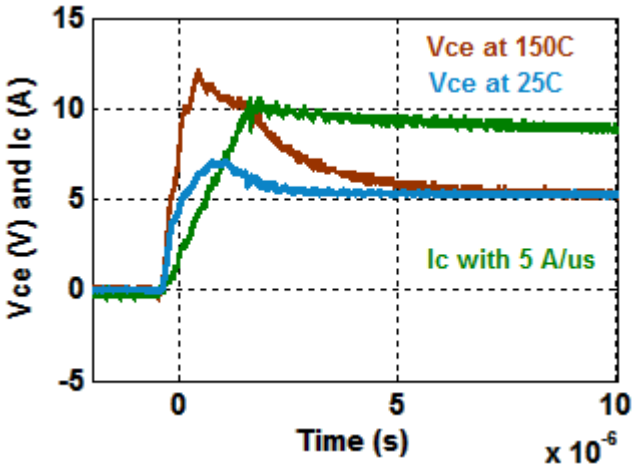


Fig. 6.3. Turn-on voltage spike of 12 kV, 5 µm buffer layer SiC IGBT under di/dt of 5 A/µs at 25ºC and 150ºC.

6.3 ZVS Turn-off Characteristics

The turn-off characteristics at different temperature, with and without a 1.1 nF external snubber capacitor are presented in this section. Fig. 6.4 shows turn-off transition at 7 kV, 10 A at 25ºC and 150ºC without external snubber capacitor. The turn-off current has five different stages

during the transition: a dip at the beginning of the transition resulting from transferring load inductor current into the IGBT capacitance (and capacitance of the free-wheeling diode); the bump existing until the punch-through voltage (4.3 kV); a slow drop in current from punch-through voltage until the voltage reaches dc-bus voltage of 7 kV; a sudden drop in current once the voltage reached dc-bus value of 7 kV; lastly, the current tail resulting from recombination of the stored charge. There is no current tail at 25ºC, but the increased stored charge at 150ºC is responsible for the small tail current. It is to be noted that the magnitude of collector-emitter capacitance, C_{CE}, of the IGBT is significantly different in the sweep-out phase (under 4.3 kV, removal of excess carriers), and punch-through phase (over 4.3 kV). Once the punch-through phase has been reached, the amount of minority carriers removed by the increase in V_{CE} becomes very small, resulting in much faster voltage rise, as explained in chapter-5.

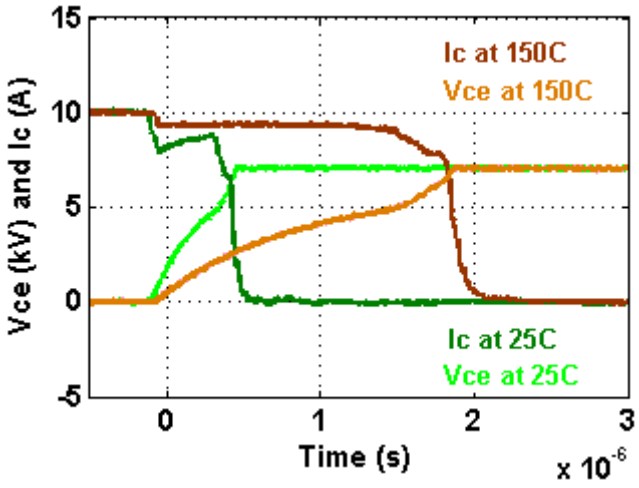


Fig. 6.4: Turn-off transitions of 12 kV, 2 µm buffer layer SiC IGBT at 25ºC and 150ºC without an external snubber capacitor.

Fig. 6.5 and Fig. 6.6 show turn-off transitions with a 1.1 nF external snubber capacitor, at 25ºC and 150ºC respectively. With the snubber capacitor, the magnitude of the current bump is smaller and exists for longer duration (basically, the time to reach punch-through voltage is increased with the addition of external capacitor).

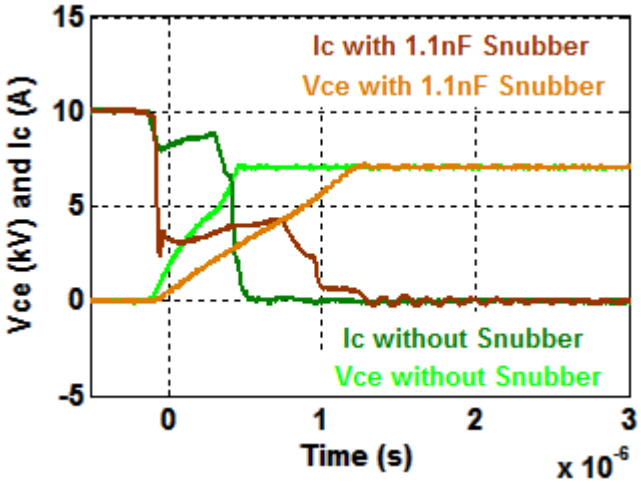


Fig. 6.5: Turn-off transitions of 12 kV, 2 µm buffer layer SiC IGBT at 25ºC with and without the 1.1 nF external snubber capacitor.

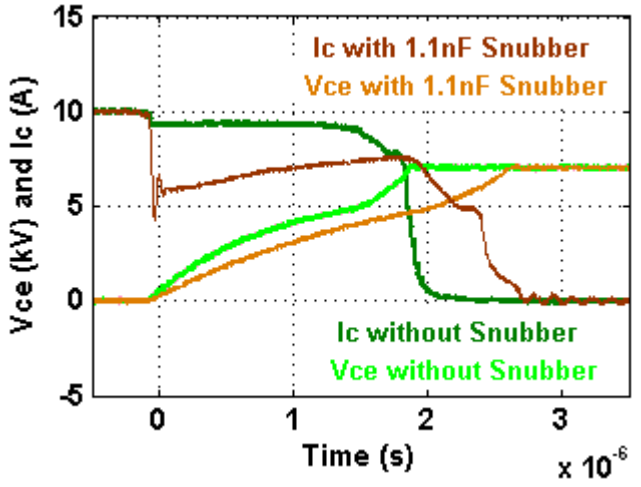


Fig. 6.6: Turn-off transitions of 12 kV, 2 µm buffer layer SiC IGBT at 150ºC with and without the 1.1 nF external snubber capacitor.

The turn-off characteristics of the 5 µm buffer layer IGBT without external snubber capacitor are shown in Fig. 6.7. By comparing with the similar results of the 2 µm buffer layer IGBT (shown in Fig. 6.4), the transitions of the 5 µm IGBT at 25ºC and 150ºC are significantly faster resulting in considerably lower switching loss. The 2 µm and 5 µm buffer layer IGBTs are

identical, except for thickness of the buffer layer. The transitions with 1.1 nF external snubber capacitor at 25ºC and 150ºC are shown in Fig. 6.8 and Fig. 6.9 respectively.

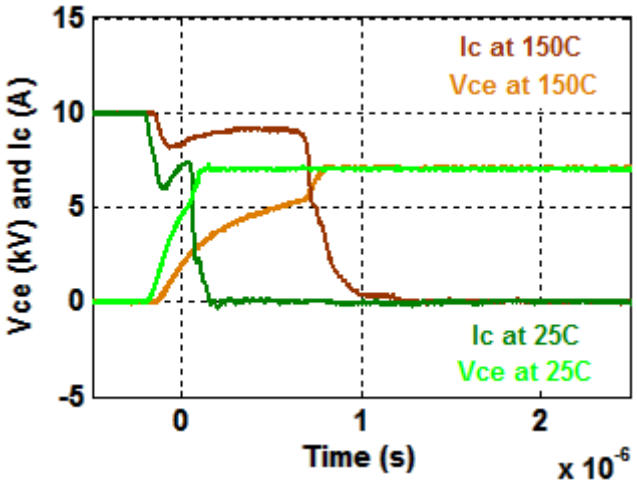


Fig. 6.7: Turn-off transitions of 12 kV, 5 µm buffer layer SiC IGBT at 25ºC and 150ºC without an external snubber capacitor.

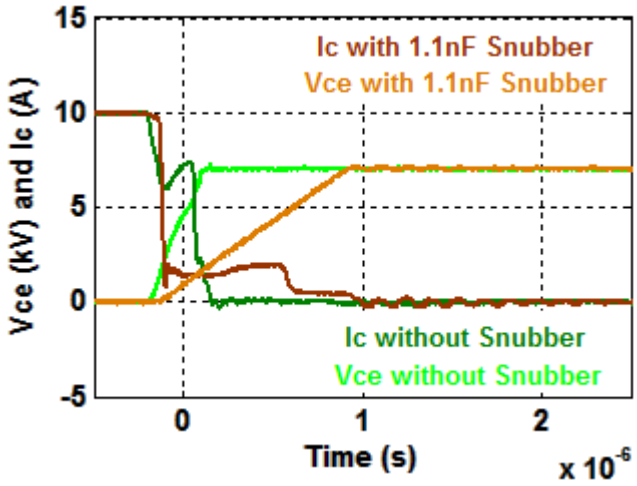


Fig. 6.8: Turn-off transitions of 12 kV, 5 µm buffer layer SiC IGBT at 25ºC with and without the 1.1 nF external snubber capacitor.

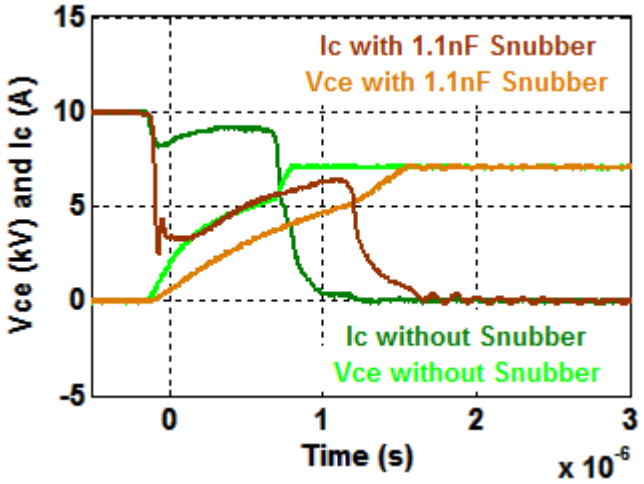


Fig. 6.9: Turn-off transitions of 12 kV, 5 µm buffer layer SiC IGBT at 150°C with and without the 1.1 nF external snubber capacitor.

The test circuit [34] used for evaluation of the ZVS characteristics is shown in Fig. 6.10. The turn-on characteristics are obtained by supply is + 20 V gate to the DUT before the current is passed through it (without the snubber capacitor in the circuit). The turn-off characteristics are obtained by charging the 8 mH load resonant inductor (L) to a desired current value and then turning off the switch S1. Then, the inductor current freewheels through DUT and Diode D1. Turning-off the DUT now provides the required ZVS transition, while the current is shifted from DUT to Diode D2. The 10 kV SiC MOSFET/ JBS diode co-packs are used in place of the switch S1 and also free-wheeling diodes, D1 and D2 with their gates shorted.

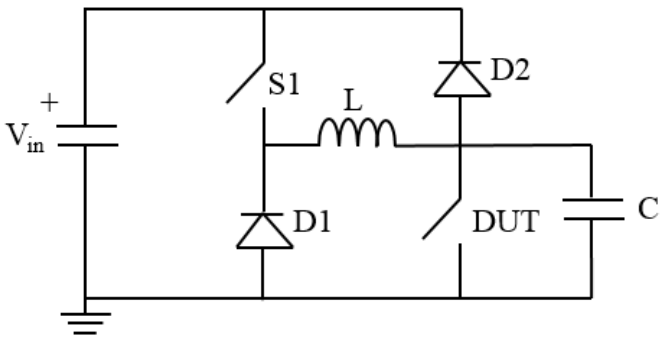


Fig. 6.10: Test circuit used for ZVS characterization of the IGBTs [34]

6.4 Considerations for Power Converter Design

The advantages of the ZVS based power converters are eliminating turn-on dv/dt and controlling turn-off dv/dt while achieving improved power conversion efficiency. This improves reliability of power converter system by minimizing common-mode currents, reducing dv/dt stress on gate drivers and motor loads, and minimizing parasitic ringing. However, the IGBTs have been shown to exhibit forward voltage spike during turn-on and current bump during turn-off.

The forward voltage spike can trigger spurious de-sat shoot-through fault. This can be addressed for moderate di/dt levels by increasing the blanking capacitor values of the gate driver. The current-sense based short-circuit detection can be used for low current converters to completely eliminate the spurious fault trigger issue. The turn-off energy loss of 2 μm and 5 μm buffer layer SiC IGBTs at 25^{o}C and 150^{o}C, with and without the 1.1 nF snubber capacitor, are given in Table 6.1. The IGBT energy loss values in the presence of snubber capacitor are a significant portion of hard-switched loss data, which requires careful design of the thermal management system even under ZVS conditions.

The 5 μm IGBT has only 40-50% of turn-off energy loss of that of the 2 μm IGBT. Also, the loss reduction resulting from using the external snubber is about 10 % more for the 5 μm IGBT. A larger snubber capacitor can be used for further loss reduction, after considering its impact on the ZVS load range of the power converters.

Table 6.1: Turn-off energy loss of the SiC IGBTs

Voltage, Current and Temperature Conditions	**E_{OFF} of 2 µm IGBT**		**E_{OFF} of 5 µm IGBT**	
	No Ext. Snubber	***1.1 nF Snubber***	***No Ext. Snubber***	***1.1 nF Snubber***
7 kV, 10 A, 25°C	15.6 mJ	11.5 mJ	6.2 mJ	4.0 mJ
7 kV, 10 A, 150°C	64.8 mJ	56.4 mJ	33.0 mJ	25.7 mJ

6.5 Summary

The zero voltage switching behavior of 2 µm and 5 µm buffer layer, discrete 12 kV SiC N-IGBTs has been investigated. The turn-on voltage spike of over 15 V is observed at 150°C at 10 A/µs. The turn-off current bump is causing significant energy loss even with capacitive snubber. Based on the comparison of turn-off energy loss of both IGBTs, the 5 µm IGBT has 10 % more loss reduction by incorporating the same snubber capacitor. An analytical investigation needs to be done to understand the causes of the current bump.

Chapter 7

Complementary Inverter Using 15 kV P-IGBT and N-IGBT

7.1 Introduction

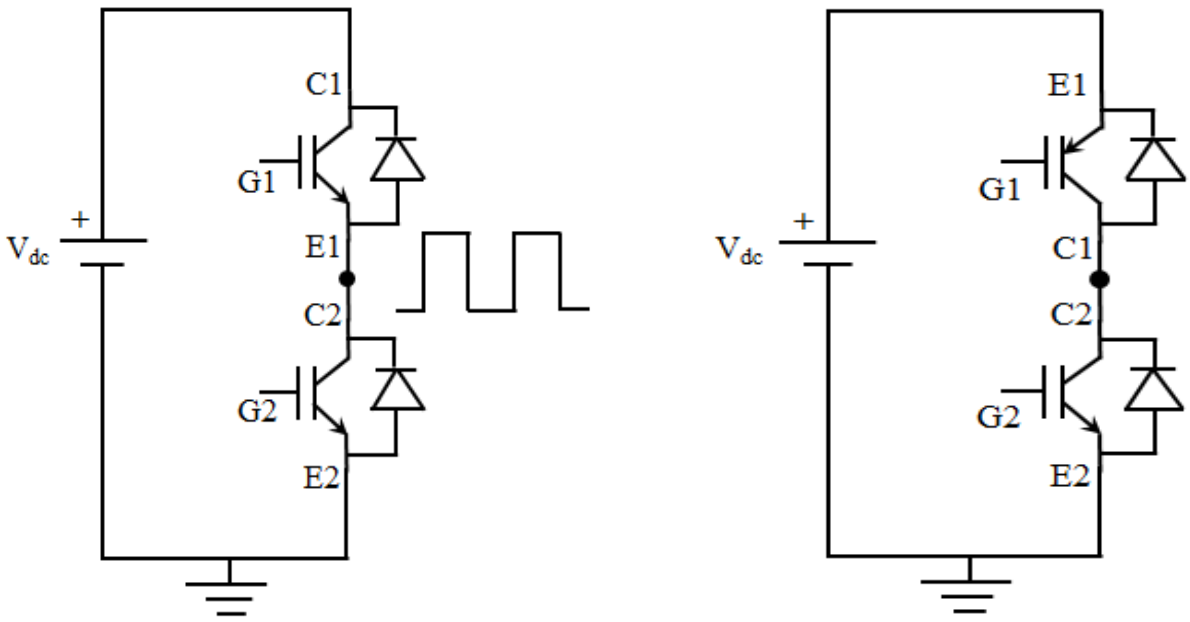
The earlier SiC IGBTs were developed with P-type drift due to practical limitation in preparing low resistivity P+ SiC substrates required for the N-IGBTs [8]. However, with advances in the SiC technology, N-IGBTs have also been built [9]-[10] and are found to be more efficient. However, the availability of complementary devices at such high voltage creates a unique option for simple and reliable high power converter design.

The use of complementary switching devices for power conversion has been explored with low voltage (up to 600 V) Si devices. The higher power loss of the P-channel devices has substantially narrowed their application. Also, the matured technology to design highly reliable gate drivers for Si IGBTs (up to 6.5 kV) has not favored use of complementary topology at that voltage and low dv/dt levels. On the other hand, the SiC IGBTs have created a new paradigm with ultrahigh voltage blocking and dv/dt stress handling requirements. At this point, the option of exploring the application of P-IGBT, despite the fact that it is not as efficient as N-IGBT, is worth consideration with the motivation to achieve zero dv/dt stress on the gate drivers.

Fig. 7.1(a) shows phase-leg of an inverter using N-channel switching devices on both high-side and low-side. The emitter of the low-side device (E2) is connected to the negative rail (fixed potential) permanently, and therefore zero dv/dt is seen between the converter control ground and the emitter of the bottom switch. It is shown in the figure that the mid-point (E1) voltage is floating with quick transitions from full dc-bus voltage to zero and vice-versa, in response to the PWM pulses for power conversion. The high frequency, high dv/dt square wave

requires a thorough gate driver design as described in Chapter-3, to minimize common-mode injection to have reliable converter operation. The dv/dt can be minimized by active gate current control demonstrated in Chapter-5, but it is complicated in comparison to a conventional gate driver. Moreover, the insulation strength of the gate driver isolation stage may deteriorate over the years due to constant exposure to high voltage, dv/dt and frequency. The complementary inverter is pursued as a simple and robust alternative where the gate drivers are exposed to zero dv/dt stress.

Fig. 7.1 (b) shows the phase-leg of a complementary inverter with P-IGBT on high-side and N-IGBT on low-side. As shown in the figure, the emitters of both the devices, E1 and E2 are connected to the steady potential terminals of $+V_{dc}$ and zero respectively, completely eliminating the possibility of dv/dt coupling currents through the gate drivers. However, as mentioned earlier, the use of P-channel device increases the power loss. The following sections evaluate this phenomenon based on the switching losses and dv/dt generated by both the devices, with advantages and disadvantages of application of the complimentary topology for high power conversion.



(a) (b)

Fig. 7.1: Schematic of (a) Inverter phase-leg with N-type devices; (b) Phase-leg of complementary inverter with P-type device on top and N-type device on bottom.

7.2 Characteristics of 15 kV, 5 A, P-IGBT

Fig. 7.2 shows cross-sectional view of the 15 kV P-IGBT. The forward characteristics of the IGBT are shown in Appendix. The forward drop is 5.5 V for a current of 5 A at room temperature. Fig. 7.3 shows turn-off waveforms of the IGBT under clamped inductive load test at 6 kV and 5 A. The transition duration is 2.2 µs with energy loss of 21 mJ. The corresponding turn-on transition is shown in Fig. 7.4. Unlike the turn-off transition, the turn-on transition has a spike of 66 A with a very short transition time of about 500 ns. The high current spike is due to discharge of the capacitance of the freewheeling diode across the load inductor due to high dv/dt generated by the IGBT. The polarities of the current and voltage have been reversed for convenience and for ease of comparison with the N-IGBT.

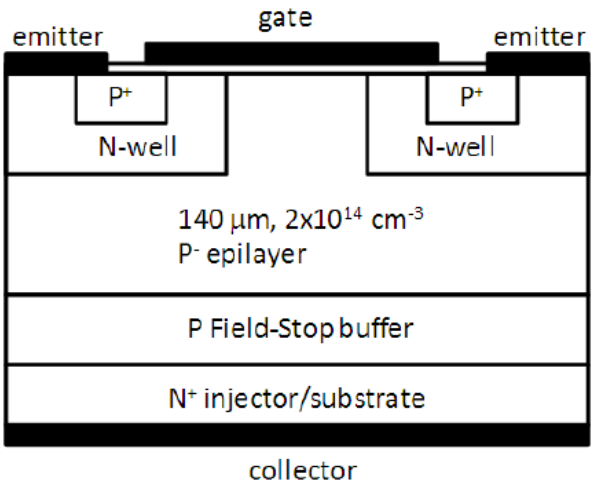


Fig. 7.2: Cross-sectional view of the 15 kV P-IGBT

The turn-off gate resistance, $R_{G(OFF)}$, used in the evaluation is 10 Ω, whereas the turn-on gate resistance, $R_{G(ON)}$, is 200 Ω. The gate voltage, V_{GE}, used is -20 V for turn-on, and + 4.5 V for turn-off. The high $R_{G(ON)}$ is used to suppress the current spike at the beginning of the transition by limiting the rate of discharge of the depletion capacitance of the IGBT. As the injection from the N+ emitter is very efficient, the current spike is not suppressed significantly. However, further increase of $R_{G(ON)}$ will reduce the spike and decrease the rate of voltage transition at the cost of increased power loss.

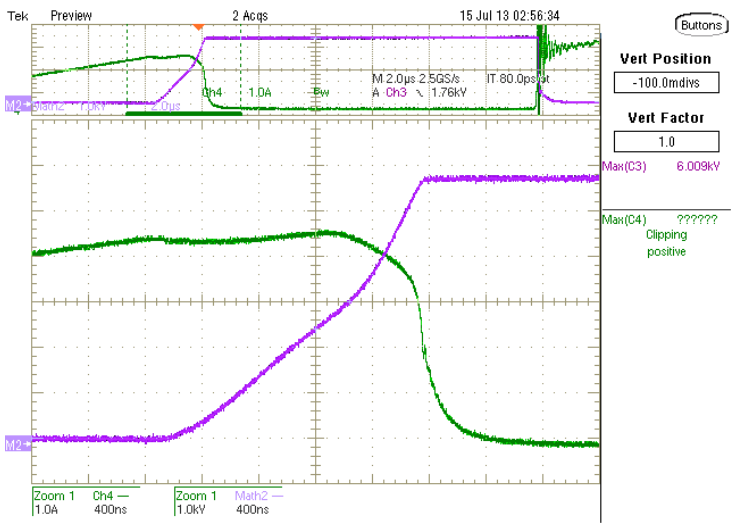


Fig. 7.3: Turn-off transition of the 15 kV, 5 A, P-IGBT with clamped inductive load at 6 kV, 5 A with $R_{G(OFF)}$ = 10 Ω. [Ch4: I_C (1 A/div); Math2: V_{CE} (1 kV/div); Time scale: 400 ns/div].

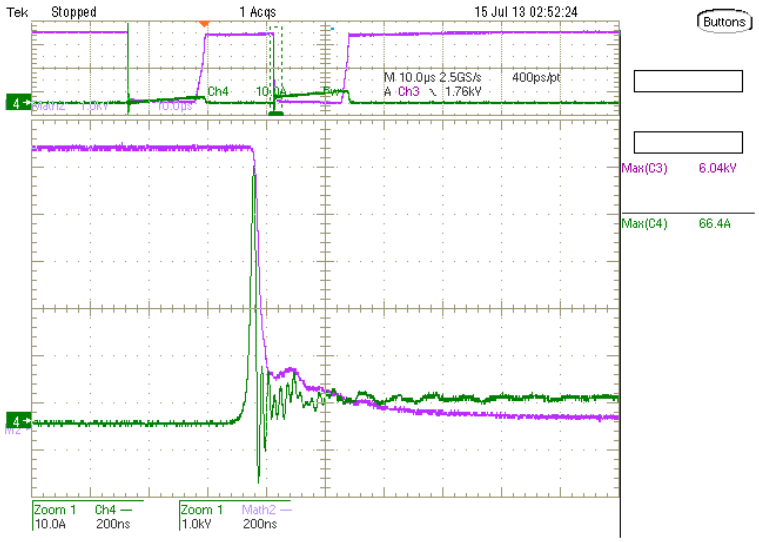


Fig. 7.4: Turn-on transition of the 15 kV, 5 A, P-IGBT with clamped inductive load at 6 kV and 5 A with $R_{G(ON)}$ = 200 Ω. [Ch4: I_C (10 A/div); Math2: V_{CE} (1 kV/div); Time scale: 200 ns/div].

7.3 Characteristics of 15 kV, 5 A, N-IGBT

The cross-sectional view of the N-IGBT is shown in Fig. 7.5. The N-IGBT has same drift layer thickness and doping as P-IGBT, but the thickness, doping and life time of the field-stop buffer layer are different (as per the information from Cree). The 15 kV, 5 A, N-IGBT has a forward drop of 4.9 V at 5 A, and room temperature. The forward characteristics of the IGBT are shown in Appendix.

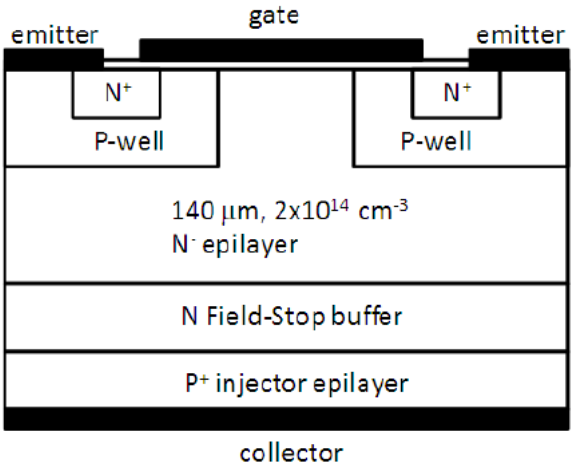


Fig. 7.5: Cross-sectional view of the 15 kV N-IGBT

The switching characteristics have been evaluated on a clamped inductive double pulse test setup with a discrete 20 kV SiC diode (two 10 kV didoes in series) for free-wheeling. The turn-off and turn-on characteristics of the N-IGBT are shown in Figs. 7.6 and 7.7 respectively. The gate resistances used are same as those used for the P-IGBT tests. It can be seen that the turn-off duration is much shorter for the N-IGBT. This is due to lower injection of the P+ emitter of the N-IGBT as compared to the higher injection of the N+ emitter of the P-IGBT. The lower injection is also the reason for much lower current spike or the dv/dt at the beginning of the turn-on transition.

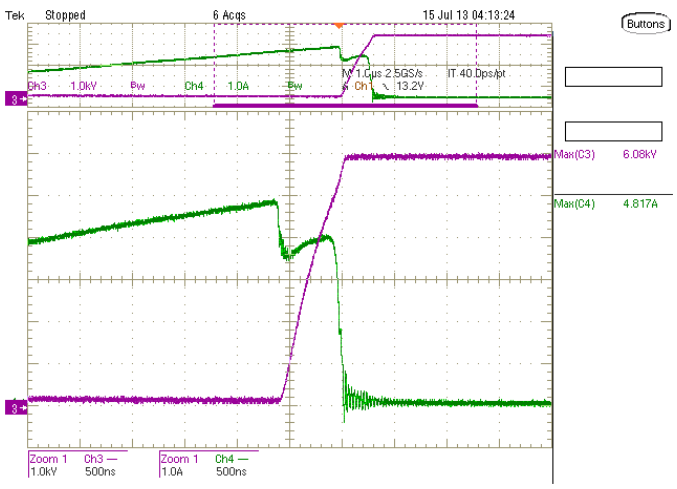


Fig. 7.6: Turn-off transition of the 15 kV, 5 A, N-IGBT under clamped inductive load test at 6 kV and 5 A with $R_{G(OFF)} = 10\ \Omega$. [Ch3: V_{CE} (1 kV/div); Ch4: I_C (1 A/div); Time scale: 500 ns/div].

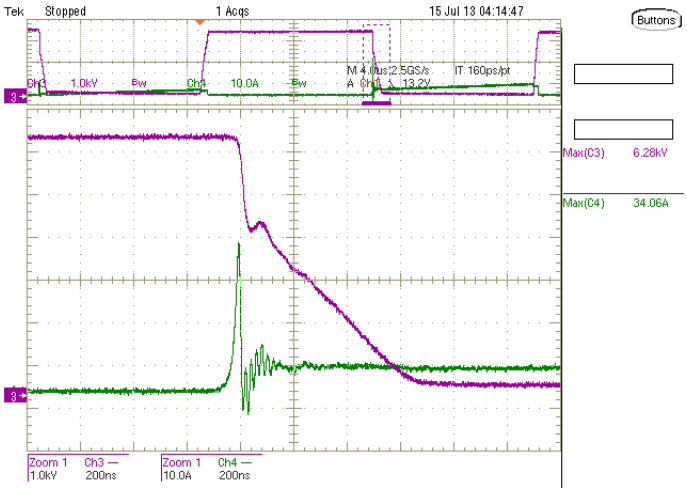


Fig. 7.7: Turn-on transition of the 15 kV, 5 A, N-IGBT under clamped inductive load test at 6 kV and 5 A with $R_{G(ON)} = 200\ \Omega$. [Ch3: V_{CE} (1 kV/div); Ch4: I_C (10 A/div); Time scale: 200 ns/div].

7.4 Discussion

The comparison of the characteristics of the 15 kV, 5 A, P-IGBT and N-IGBT is shown in Table 7.1. The higher conduction drop of the P-IGBT is due to lower MOS channel mobility in comparison to the N-IGBT. The turn-off loss of the P-IGBT at 6 kV, 5 A is 21 mJ, whereas, it is 6.7 mJ for the N-IGBT. As explained earlier, the higher injection efficiency of the N+ emitter in the P-IGBT is resulting in more storage charge to be removed during the turn-off process. This is consequently leading to longer turn-off duration and more energy loss in the P-IGBT. A representation of the stored charge in the P-IGBT and N-IGBT is shown in Fig. 7.8. The analytical expressions presented in Chapter-5 are valid for the comparison of voltage rise time (defined by the stored charged) of P-IGBT and N-IGBT also.

On the other hand, the turn-on loss of the N-IGBT is higher. It can be seen from Fig. 7.7 that the voltage of the N-IGBT has a sudden change in slope during the turn-on transition. The sharper region is due to discharge of its low depletion capacitance, whereas, the slower region is dictated by the high diffusion capacitance and the high $R_{G(ON)}$ of 200 Ω, used to slow down the rate of discharge of the depletion capacitance at the beginning of the transition. From Fig. 7.4, it can be seen that the P-IGBT has a steep slope in voltage till it reaches about 1 kV. Thus, the turn-on dv/dt of the P-IGBT is much higher (about twice) than that of the N-IGBT. The higher dv/dt of the P-IGBT is also responsible for higher current spike due to discharge of the capacitance across the diode (this includes the inter-winding capacitance of the inductive load used for the double pulse switching tests).

Table 7.1: Comparison of the 15 kV P-IGBT and N-IGBT at 6 kV, 5 A

Parameter	P- IGBT	N- IGBT
Forward drop at 5 A	5.5 V	4.9 V
Turn-off loss at 6 kV, 5 A	21 mJ	6.7 mJ
Turn-on loss at 6 kV, 5 A	6.3 mJ	12.7 mJ
Turn-off dv/dt (in the steeper region)	6 kV/µs	11 kV/µs
Turn-on dv/dt (in the steeper region)	119 kV/µs	62 kV/µs
Turn-off duration	2.2 µs	650 ns
Turn-on duration	500 ns	700 ns
Turn-on current spike	66 A	34 A
$R_{G(ON)}$ /$R_{G(OFF)}$	200 Ω/ 10 Ω	200 Ω/ 10 Ω

So, the conduction, turn-off and turn-on losses information shown in Table 7.1 has validated that the N-IGBT is more efficient. Also, it is to be noted that the turn-on loss of the N-IGBT can be reduced by using a lower gate resistance that produces the same dv/dt (or current spike) seen with the P-IGBT, for a fair comparison from the perspective of a power converter.

Also, in [1], it is explained that a trade-off of forward-drop and switching loss (and dv/dt) is possible by adjusting the thickness, doping concentration and life-time parameters of the field-stop buffer layer of the IGBTs. This opens the possibility of reducing the switching loss of the P-IGBTs to about the same level as the N-IGBTs, with a moderate increase in conduction loss and thus making them ideal to use as a complementary pair for high switching frequency applications. In the cases where the heat sinks of the power converters are grounded, an investigation on the influence of high dv/dt produced by these fast switching IGBTs on the power circuit common mode currents needs to be performed.

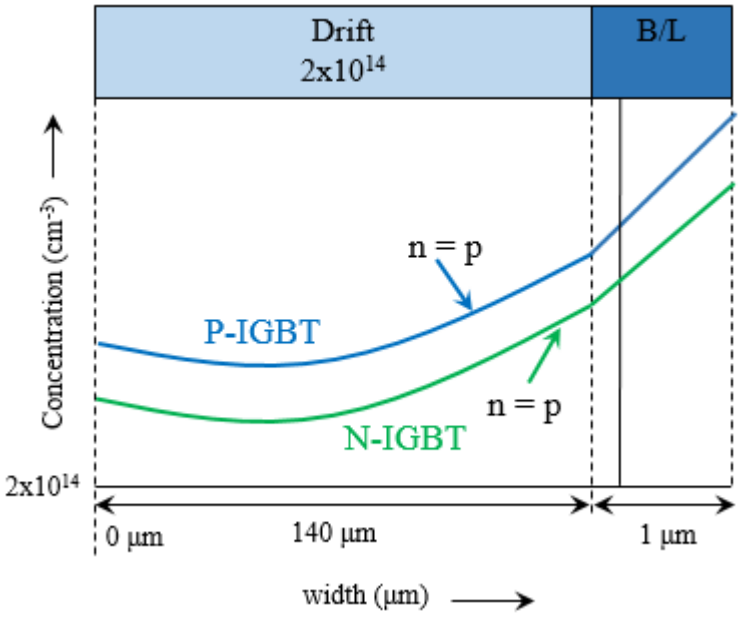


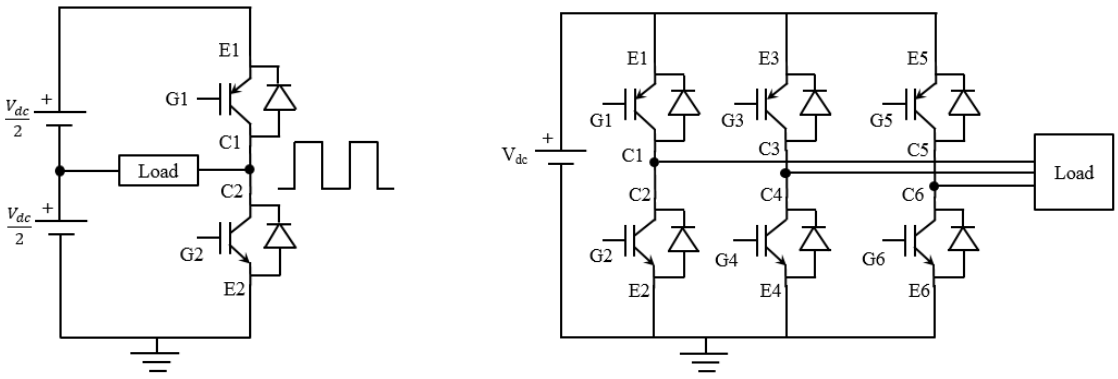
Fig. 7.8: Representation of stored charge in P-IGBT and N-IGBT.

7.5 Experimental Results

A complementary half-bridge inverter (schematic shown in Fig. 7.9(a)) prototype is built using the 15 kV, 5 A, SiC, P-IGBT and N-IGBT. The results of the inverter prototype with 3 kV dc input at 5 kHz and 10 kHz switching frequencies are shown in Figs. 7.10 and 7.11 respectively, where the IGBTs are exposed to a peak stress of 3 kV. At 5 kHz switching, the ac output voltage and current of the converter are 819 V rms and 2.1 A rms respectively. The corresponding values at 10 kHz are 731 Vrms and 1.9 A.

The reduction of switching ripple with 10 kHz switching is evident from the figures. Also, the magnitude of the output voltage is reduced with 10 kHz switching, due to increased voltage drop across the filter inductance. The noticeable distortion in ac current (or voltage) at 10 kHz is due to amplified effect of the same dead-band. The modulation index of the converter is 0.8, and the resistive load and filter inductor values are 380 Ω and 75 mH respectively. The results on the three-phase prototype (schematic shown in Fig 7.9 (b)) are shown in Fig. 7.12, for input

voltage of 3 kV and 5 kHz switching frequency. The output line voltage and line current are 1.8 kV (rms) and 0.35 A (rms) respectively. The half-bridge and three-phase complementary inverter prototypes are shown in Fig. 7.13 and Fig. 7.14 respectively.



(a) (b)

Fig. 7.9: Schematic of (a) half-bridge; (b) three-phase complementary inverters

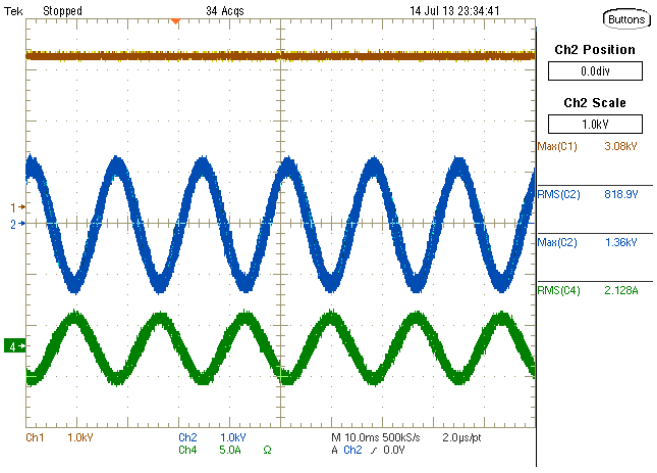


Fig. 7.10: Experimental waveforms of the half-bridge complementary inverter at 5 kHz switching frequency. [Ch1: Input voltage (1 kV/div); Ch2: Output voltage (1 kV/div); Ch4: Output current (polarity reversed) – 5 A/div; Time scale: 10 ms/div].

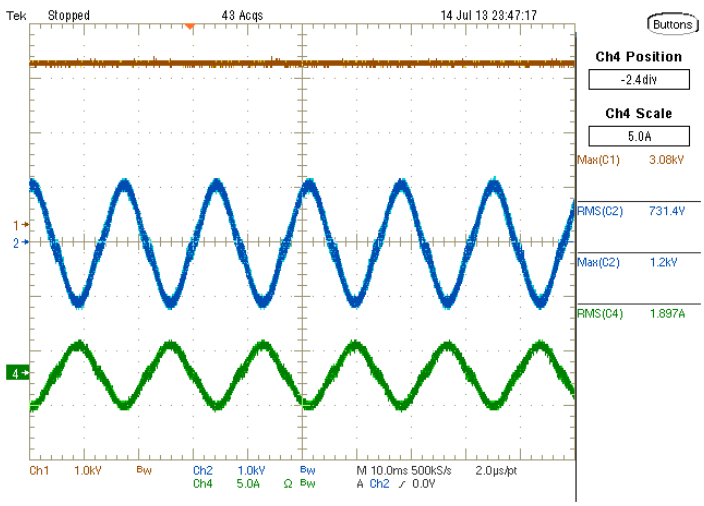


Fig. 7.11: Experimental waveforms of the half-bridge complementary inverter with 10 kHz switching frequency. [Ch1: Input voltage (1 kV/div); Ch2: Output voltage (1 kV/div); Ch4: Output current (polarity reversed) – 5 A/div; Time scale: 10 ms/div].

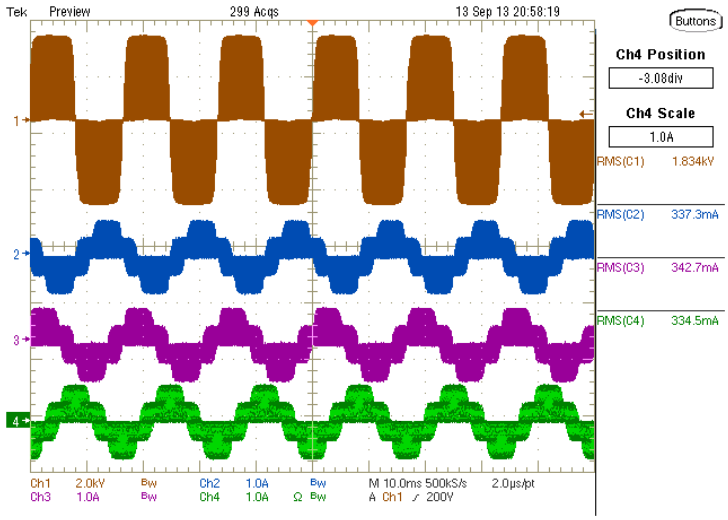


Fig. 7.12: Experimental waveforms of the three phase complementary inverter at 5 kHz switching frequency. [Ch1(Brown): Output line voltage – 2 kV/div; Ch2(Blue), Ch3(Magenta) and Ch4(Green): Load currents – 1 A/div; Time scale: 10 ms/div].

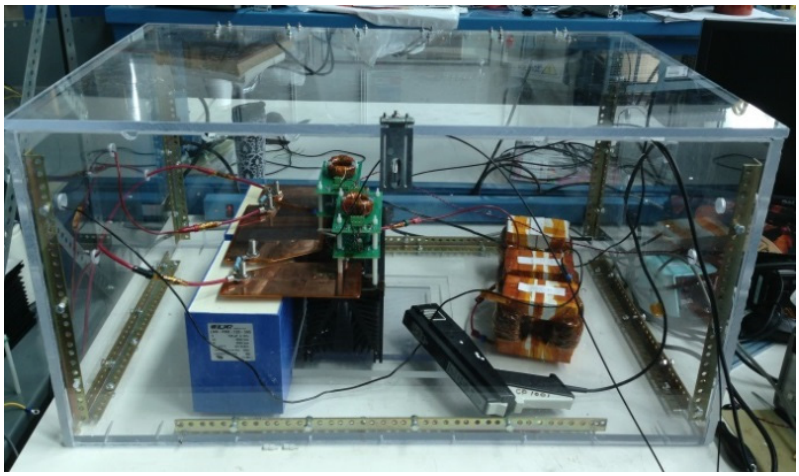


Fig. 7.13: The prototype of the complementary half-bridge inverter with 15 kV SiC IGBTs

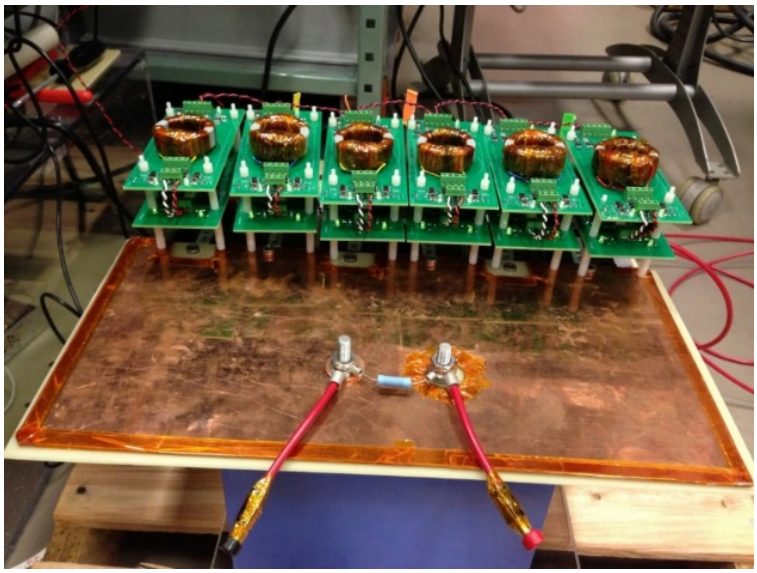


Fig. 7.14: The prototype of the complementary three phase inverter with 15 kV SiC IGBTs.

7.6 Summary

The simple two-level complementary voltage source converter topology represents a new paradigm and new possibilities in medium voltage power conversion. Based on the experimental switching results at 6 kV and 5 A, the N-IGBTs are found to be more efficient than the P-IGBT. However, as both these devices generate high dv/dt, the use of complementary topology has the benefit of improving gate driver reliability by eliminating injection of the common-mode currents. The experimental results on a 3 kV complementary inverter prototype have been presented as a validation of the proposed concept for the high voltage SiC devices. The optimization of the field-stop buffer layer parameters of the IGBTs for better switching performance presents a promising option of high efficiency, ultrahigh voltage power conversion. The high voltage 15 kV SiC optimized N-IGBT and P-IGBT based simple two-level complementary inverter topology can provide the desired converter reliability required for any ground referenced dc source medium voltage applications.

Chapter 8
Conclusions

8.1 Summary of the Work

The work presented in this thesis is the first attempt at detailed understanding of the high voltage SiC IGBTs from the perspective of their performance in power conversion systems. A high switching characterization test set-up has been built to characterize different 15 kV SiC IGBTs with an equivalent rating JBS diode for freewheeling the inductive load. The SiC IGBTs have been characterized up to 11 kV, 10 A and 175^{o}C (maximum values) and design consideration for power converters have been identified. An 11 kV, over 100 kV/μs dv/dt immunity gate driver has been developed with dc-dc high isolation stage based on ferrite-core transformer. The gate driver has been demonstrated on different hard-switched converters to evaluate its performance under high dv/dt, high voltage conditions. The SiC IGBT power dissipation limits have been evaluated experimentally on a 10 kV hard-switched boost converter to be 550 W/cm^2 (active area) while maintaining the junction temperature at 150^{o}C. The analytical evaluation of the frequency limits for two different current densities and cooling mechanisms has been provided. A thorough investigation on the factors that limit switching frequency limits – the thermal resistance of the module package, the thermal resistance of the heatsink and the turn-off energy loss increase with temperature – has been presented. A method to estimate the online IGBT junction temperature based on collector turn-off switching voltage measurement is provided.

The SiC IGBT has been demonstrated on 3-level NPC inverter with 10 kV dc-input, 10 kHz switching frequency and 9 kW resistive loading. Also, the IGBTs are demonstrated on 2-level H-Bridge inverter where they are exposed to steady-state switching voltage stress of 10 kV at 5 kHz and 6 kW. To have optimal stress on the base-plate isolation of all the IGBT modules, the common heatsinks have been connected to the dc-link mid-point. Following this, the performance of multi-chip IGBT modules has been investigated. The multi-chip IGBT is

effectively generating more loss due to weak dependency of turn-off loss with collector current. Six 3-level poles have been demonstrated, each for 30 minutes duration, using the multi-chip IGBT modules – three with sine-PWM and the remaining three with square-PWM – suitable for a three-phase solid state transformer demonstration.

The subsequent work is focused on evaluation of methods to extract optimal performance of the SiC IGBT in converter applications. The turn-off dv/dt of the SiC IGBT during the two-slope switching transitions has been studied with variation of current, temperature and buffer layer thickness. Analytical evaluation of the dv/dt has been presented using the normalized results for the turn-off dv/dt. The latter part of the work is on two-stage active gate driver demonstration at 11 kV for reducing the turn-on dv/dt without increasing the energy loss. This was followed by evaluating the IGBT characteristics for soft-switched power converter application up to 7 kV, 150^{o}C and capacitive snubber. Finally, the option of complementary inverter topology with 15 kV P-IGBT and N-IGBT with zero dv/dt stress on gate drivers is investigated. The comparison of energy losses and dv/dt of both the IGBTs is presented at 6 kV along with the demonstration of single-phase and three-phase complementary inverter prototypes with 3 kV dc input.

8.2 Scope for Future Research

Implementation of three-stage closed-loop active gate driver for the 15 kV SiC IGBT to obtain further reduction of dv/dt without adding any delay time. Also, the impact of high dv/dt on deteriorating the insulation of the isolation transformer in the long-run needs to be studied.

Investigation of methods to determine efficiency of the medium voltage 3-level NPC and 2-level H-bridge converters. A back-to-back connection of two identical converters could be pursued to determine converter losses with good accuracy. Also, the root cause of converter tripping when the heat-sinks were floated needs to be investigated.

Based on the availability of experimental data on carrier life-time and mobility, detailed models of the IGBT can be developed to explain and quantify the dv/dt, turn-off current bump,

ZVS characteristics, and to provide optimal device design parameters (doping profile, thickness and life time in drift and buffer layers) for soft-switching, hard-switching and complementary inverter applications.

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APPENDIX

Static Characterization Data Provided by Powerex

The different chapters of the thesis have shown switching behavior of the 15 kV SiC IGBTs. As mentioned earlier, the static characterization (forward conduction and leakage) data is provided by Powerex. Fig. A.1 shows the conduction characteristics of 15 kV, 2 µm buffer layer SiC IGBT with temperature (V_{GE} = 20 V). The voltage drop is increased from 6 V to 7 V for the temperature rise from 25°C to 150°C. The corresponding leakage data is shown in Fig. A.2. The power loss at 12 kV and 150°C is less than 2 W due to the leakage current.

The forward conduction drop of 15 kV, 5 µm buffer layer IGBT with temperature is shown in Fig. A.3. On comparing with the data for 2 µm buffer layer IGBT, shown in Fig. A.1, the conduction drop is about 1.2 V higher for 5 µm buffer layer IGBT at 25°C.

The devices used for complementary inverter evaluation are rated for 15 kV and 5 A. Fig. A.4 shows the conduction drop with temperature for the 15 kV P-IGBT, at V_{GE} of -20 V. The corresponding data for 15 kV N-IGBT, at V_{GE} of 20 V is shown in Fig. A.5.

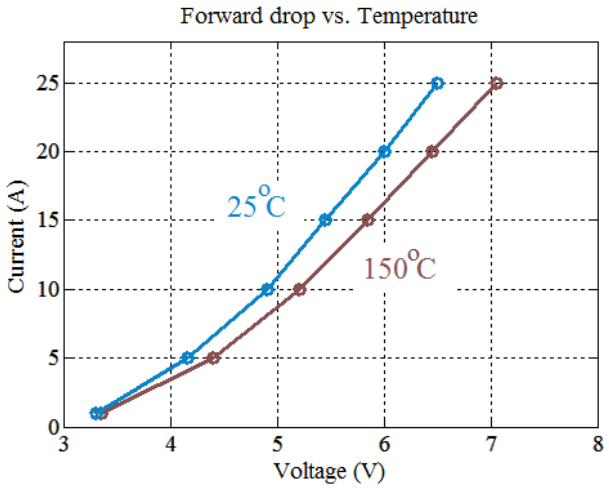

Fig. A.1: Forward conduction characteristics of 15 kV, 2 µm SiC IGBT with temperature (V_{GE} = 20 V). [Data provided by Powerex]

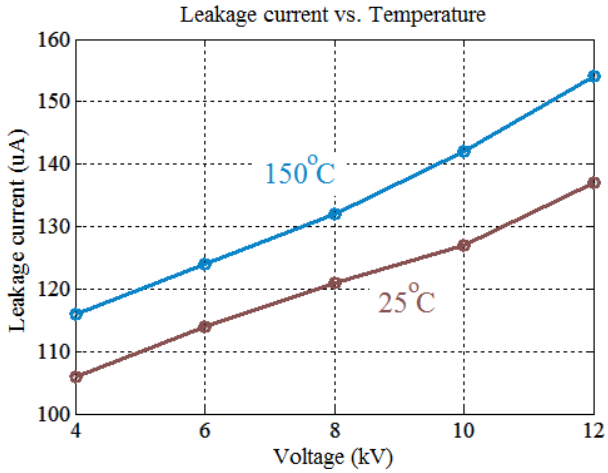

Fig. A.2: Forward blocking characteristics of 15 kV, 2 µm SiC IGBT with temperature (V_{GE} = 0 V). [Data provided by Powerex]

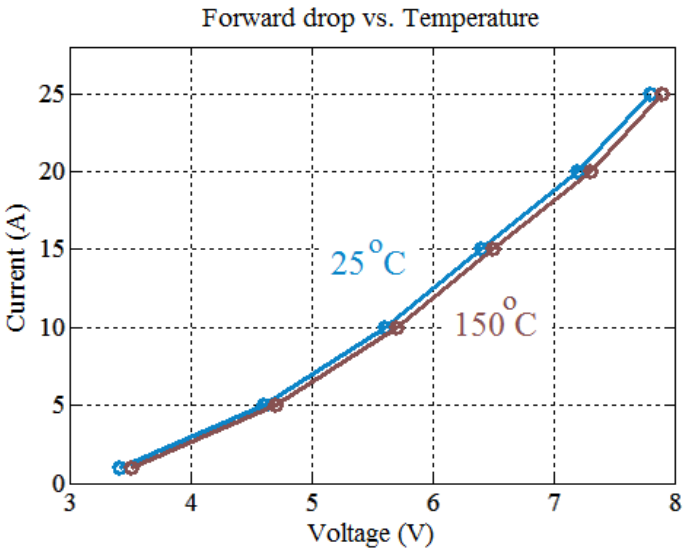

Fig. A.3: Forward conduction characteristics of 15 kV, 5 µm IGBT with temperature (V_{GE} = 20 V). [Data provided by Powerex]

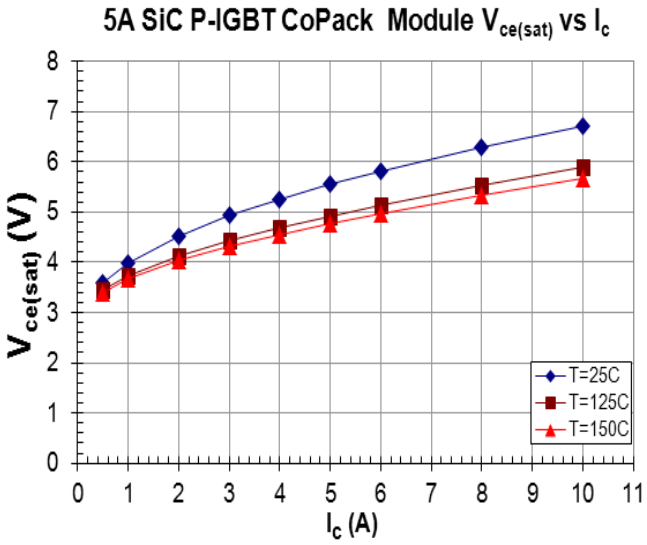

Fig. A.4: Forward characteristics of the 15 kV, 5 A, P-IGBT at different temperature. (V_{GE} = -20 V) [Data provided by Powerex]

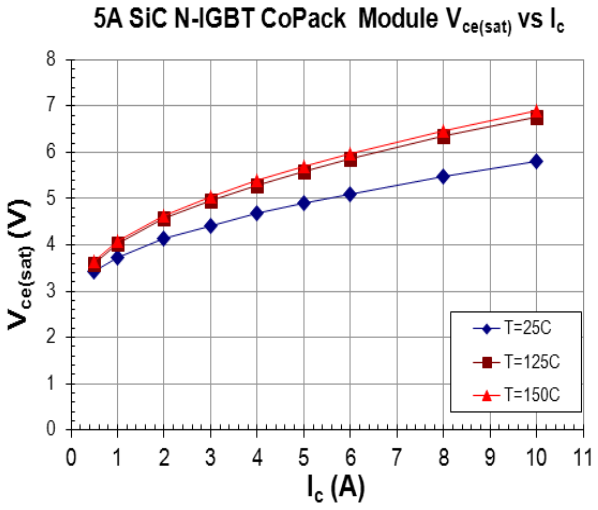

Fig. A.5: Forward characteristics of the 15 kV, 5 A, N-IGBT at different temperature. (V_{GE} = +20 V). [Data provided by Powerex]