ABSTRACT

MAHAJAN ANIURUDHA ATUL. Characterization of Wide Band Gap Power Semiconductor Devices. (Under the direction of Dr. Subhashish Bhattacharya).

Power semiconductor devices are the main building blocks for power conversion systems. Wide band gap power devices offer advantages like improved efficiency and low system cost.

This work includes the static and switching characterization of Gallium Nitride and Silicon Carbide wide band gap transistors. The characterization procedures are explained. The characterization results are compared for various transistors and advantages of these transistors over Silicon based transistors are discussed.

The results are obtained by building a hardware characterization setup in the lab.

Characterization of Wide Band Gap Power Semiconductor Devices

by
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DEDICATION

To my parents, Anagha and Atul Mahajan. I couldn't have done this without you.

Thank you for all your support along the way.

BIOGRAPHY

Anirudha Mahajan, was born in Aurangabad, India. He completed his schooling from Maharashtra Public School in Aurangabad, India. He completed his bachelor's degree in Electrical Engineering from Indian Institute of Technology, Indore in June 2013. He is currently pursuing Master of Science in Electrical Engineering from North Carolina State University. He is working at FREEDM Systems Center as Graduate Research Assistant. His research is focused on characterization of wide band gap power semiconductor devices.

Anirudha interned at Siemens, India working on HV SF_6 circuit breakers testing. He also interned at TDK-EPCOS, India working on design and simulation for triggering circuit of thyristor for capacitor applications. He worked with Cree, Inc. on characterization of Silicon Carbide power modules.

ACKNOWLEDGMENTS

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I am thankful to all my close friends who have stuck with me through thick and thin. I am thankful for the support of my family without whom this would not be possible.

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1. Introduction

Power semiconductor devices are used to control the energy transfer of electrical and electronic systems. For last 5 decades Silicon (Si) was a dominant power semiconductor material. It had several advantages over Germanium and Selenium. Si opened new applications which were not physically possible with previous materials. It was more reliable than previous materials. It was easy to use and is a low cost material. Now that the energy requirement is growing continuously, we need to develop high power, high efficiency, and high power density applications for power transfer. Si based devices are approaching their limits for high voltage and high frequency applications. Currently, Si IGBTs (Insulated gate bipolar transistor) can handle voltage of 5 kV and current of 1000 A but the operating frequency is limited to maximum of 100 kHz [1]. It reduces the efficiency and makes integration of system more difficult. Also, because of low frequency operation, a bulky filter circuit is required which increases system size and cost. Also, bulky cooling system is required to dissipate the heat generated because of high energy losses. On the other hand, Si MOSFETs have high on resistance which causes high conduction loss at high voltages limiting the use of these MOSFETs for low and medium voltages (< 600 V). The junction temperature of 150°C limits the use of Si devices in high temperature and high power density applications [2].

The Silicon is approaching its theoretical limits and there is a need to develop other materials suited for current power market requirements. For Power devices, there are many characteristics that matter in variety of power conversion systems today. Most important of them are cost, efficiency, size, and breakdown voltage. The research is going on currently on wideband gap device technology to address all the problems present with Si based devices. The wideband gap power semiconductor materials are Gallium Nitride (GaN) and Silicon Carbide (SiC) with bandgap of 3.4 eV and 3.2 eV respectively. The critical field of GaN and SiC is 10 times higher than that of Si. Because of high critical field, GaN and SiC can block the same voltage as Si devices and reduce the size by 10 times. This reduces ON resistance which also reduces the energy losses in converters which reduces converter size small and increase power density [3-7].

1.1 Motivation

The material properties of GaN, SiC and Si are discussed in the following table [7].

Parameter	Unit	Silicon	GaN	SiC
Band gap	eV	1.12	3.39	3.26
Critical Field	MV/cm	0.23	3.3	2.2
Electron mobility	$Cm^2/V.s$	1400	1500	950
Permittivity		11.8	9	9.7
Thermal Conductivity	W/cm.K	1.5	1.3	3.8

Table 1.1: Properties of Power Semiconductor Materials

Since GaN and SiC, both have superior material properties than Silicon, the new power electronics systems can be designed with these semiconductor materials which were not possible because of limitations of Silicon. With GaN, high frequency, low voltage applications are made possible with very high efficiency. With SiC, high power applications are made more efficient and power density is increased.

The main objective of this thesis is to characterize wide band gap devices to evaluate their static, switching and thermal parameters to gain knowledge about the device capabilities and use this knowledge to design and build highly efficient and compact power conversion systems. In this thesis, GaN HEMTs and SiC MOSFETs are characterized for static and switching parameters. This data will be used to design converters for high frequency, high efficiency and high temperature applications.

1.2 Organization of Thesis

In chapter 2, the static and switching characterization procedures for power semiconductor devices are discussed. The characterization setup used and precautions taken to obtain accurate results are also discussed in this chapter.

In chapter 3, material properties of GaN, basic GaN structure and characterization results are discussed. GaN HEMTs from three different manufacturers are characterized and they are compared against their characterization data. The results are also plotted in this chapter.

In chapter 4, material properties of SiC and characterization results are discussed. The half bridge SiC module is characterized and the results and test setup modifications needed for half bridge module are discussed.

In chapter 5, GaN and SiC results are compared with Silicon transistors and their potential applications are discussed. Also, advantages of converters using wide band gap devices over Silicon based converters is discussed.

In chapter 6, thesis is concluded and future work based on this thesis is discussed.

2. Power Devices Characterization Procedures

This chapter introduces general static and switching characterization processes, terminologies, device behavior for SiC MOSFETs and GaN HEMTs. The specific issues for these devices will be discussed in following chapters.

2.1 Static Characterization Approaches

Static characterization of a power semiconductor device is a most basic evaluation of performance. Static characterization includes DC characteristics (I-V, current voltage relationship) and AC characteristics (Impedances) [9-11]. The DC characteristics for SiC MOSFETs and GaN HEMTs are mainly represented by I-V curves, blocking capability, transfer characteristics, threshold voltage and, diode and third quadrant characteristics. AC characteristics include internal gate resistance, nonlinear junction capacitances, and package parasitic inductances. DC characteristics are measured using Tektronix 371A curve tracer [8] and IWATSU curve tracer. AC characteristics are measured using Agilent E4980A LCR meter.

Characteristics of power semiconductor devices are also dependent on operating temperature. External temperature source is required to heat the device to analyze temperature dependence of statics characteristics of device under test (called DUT hereafter). A hotplate is used to control GaN HEMT junction temperature and Thermostream is used to control junction temperature of SiC MOSFETs. Both the setups are shown in figures 2.1 and 2.2 respectively.

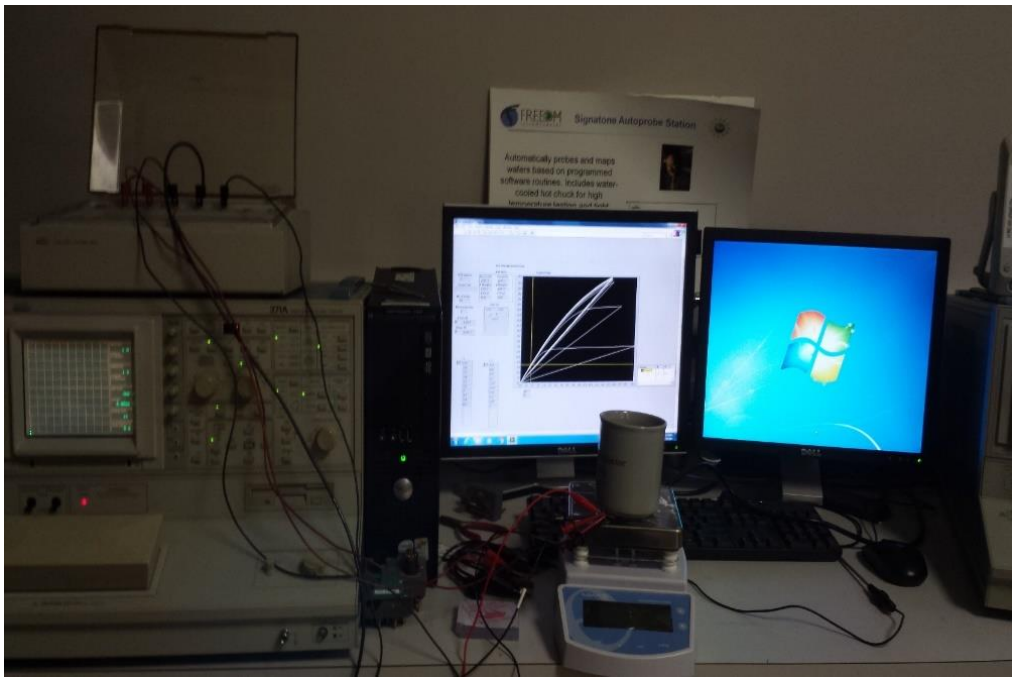

Figure 2.1: Static Characterization Setup with Hot Plate

Figure 2.2: Static Characterization Setup with Thermostream

2.1.1 Blocking Capability

The blocking capability of DUT is determined using following parameters [9].

1. BV_{DSS} – Drain to source breakdown voltage
2. I_{DSS} – Drain leakage current at rated voltage

BV_{DSS} of MOSFET is usually defined as the voltage which produces 250 µA drain leakage current. For GaN HEMTs the number is very small. The measured BV_{DSS} under this criterion is higher than rated voltage but at higher temperatures, device may produce 250 µA current at lower drain to source voltage than rated voltage. Also, for certain prototype DUTs, some single cells are weaker than the others, which will break under high voltage stress causing permanent damage to the DUT and incapability to block voltage [12].

To avoid the DUT damages, I_{DSS} is better option to evaluate blocking capability of the device. It is measured using curve tracer in high voltage mode.

2.1.2 Output and Transfer Characteristics

The output characteristics of the DUT is drain current I_D vs. Drain to source voltage V_{DS} at various gate voltages V_{GS}. The transfer characteristics of a DUT are drain current I_D vs. gate to source voltage V_{GS} for a given Drain to source voltage V_{DS}. These characteristics are measured using curve tracer. Positive gate bias is given to calculate I-V curves and transfer characteristics [9].

2.1.3 ON State Resistance (R_{DSON})

On state resistance can be calculated directly using the output characteristics of the DUT [9-10]. Some papers define R_{DSON} as maximum slope for given turn ON voltage while other papers define it as slope at specific drain current. We get minimum R_{DSON} value using first definition but it does not give the real gate resistance when DUT is ON i.e. when drain current is non zero. The second definition of R_{DSON} is used since it gives real gate resistance which can be used as design parameter for converters. The difference between the R_{DSON} at different drain currents is shown in figure 2.3.

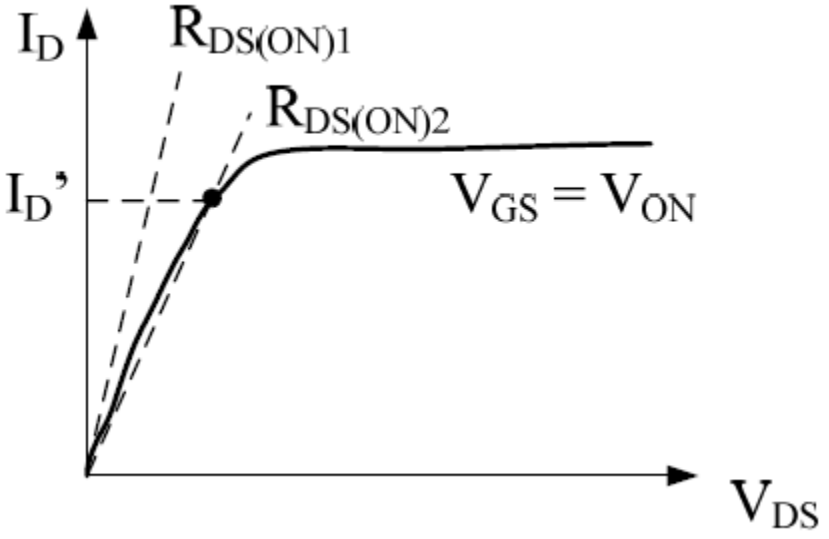

Figure 2.3: ON Resistance

2.1.4 Body Diode and Third Quadrant Characteristics

SiC MOSFETs have intrinsic body diode because of its device structure. GaN HEMT does not have a body diode because of lateral structure. Measuring body diode characteristics is similar to output characteristics except device channel needs to be pinched off during measurement. It is achieved by shorting gate and source terminals of applying negative bias to gate and source. For third quadrant characteristics, device channel is turned on and I-V characteristics are measured for body diode. It is achieved by giving positive bias between gate and source of the DUT.

2.1.5 Pre Characterization Precautions:

There are several precautions that need to be taken to ensure accurate measurements of device parameters.

1. Kelvin Sensing: Kelvin sensing is required to accurately measure static characteristics. Long wire and contact resistances may cause error in measurement in high current mode in the curve tracer. Conventional TO-247 and TO 220 packages usually fit into adapter panel of the curve tracer. For the surface mount devices (called SMD hereafter)

and other packaging, wires are needed to be connected to ensure kelvin sensing. Contact and wire resistance needs to be calculated and subtracted from measured readings to ensure accurate characteristics values. The Kelvin contacts setup for SiC power module is shown in the figure 2.4.

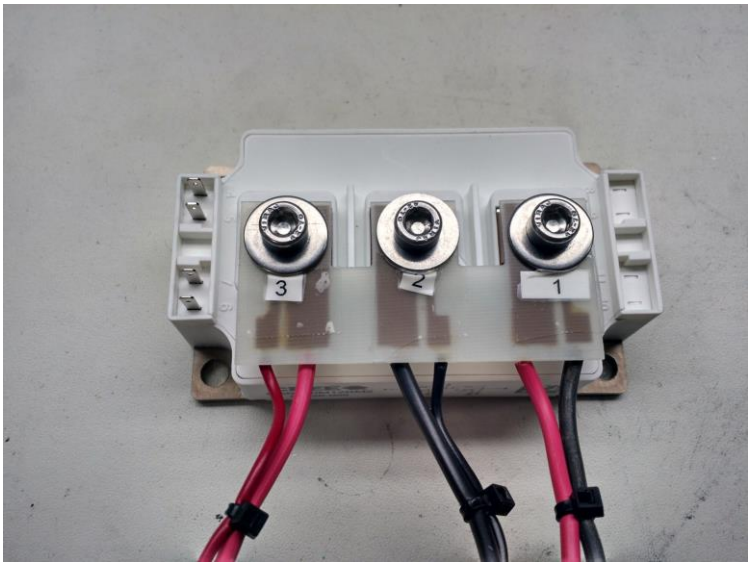

Figure 2.4: Kelvin Contacts for SiC Power Module

2. Temperature Control: The statics characteristics of power semiconductor devices are dependent on junction temperature. It is necessary to pay attention to junction temperature of the DUT. The static data needs to be collected as quickly as possible to avoid self-heating of the DUT which causes junction temperature change.
3. Electrostatic Discharge (ESD): If not handled properly, ESD can destroy gate-source oxide layer permanently. Some precautions need to be taken when storing power semiconductor devices [13].
    a. Shorting Gate-source terminals
    b. Using anti-ESD boxes
    c. Handling DUT by packaging and not the metal contacts

2.2 Switching Characterization Approaches

2.2.1 Double Pulse Tester

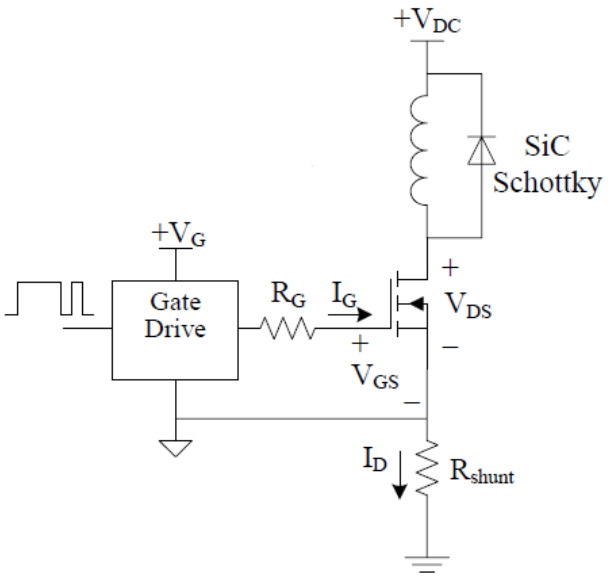

Figure 2.5: Double Pulse Test Schematic

The switching characteristics of DUT are evaluated using inductive load double pulse tester [14-16]. The double pulse tester schematic is shown in figure 2.5. The DUT is driven by high speed, high current gate driver CRD001 by Cree which supplies -5V to +20V for a MOSFET. Figure 2.6 shows typical V_{GS}, V_{DS} and I_D test waveforms. At the end of first cycle and at the start of second cycle, the DUT's switching transients can be captured for a desired V_{DS} and I_D values. The DUT can be switched under any V_{DS} and I_D stress. DUT is switched only twice to minimize the losses and therefore self-heating of the junction. The junction temperature is controlled externally to calculate switching characteristics at different temperatures.

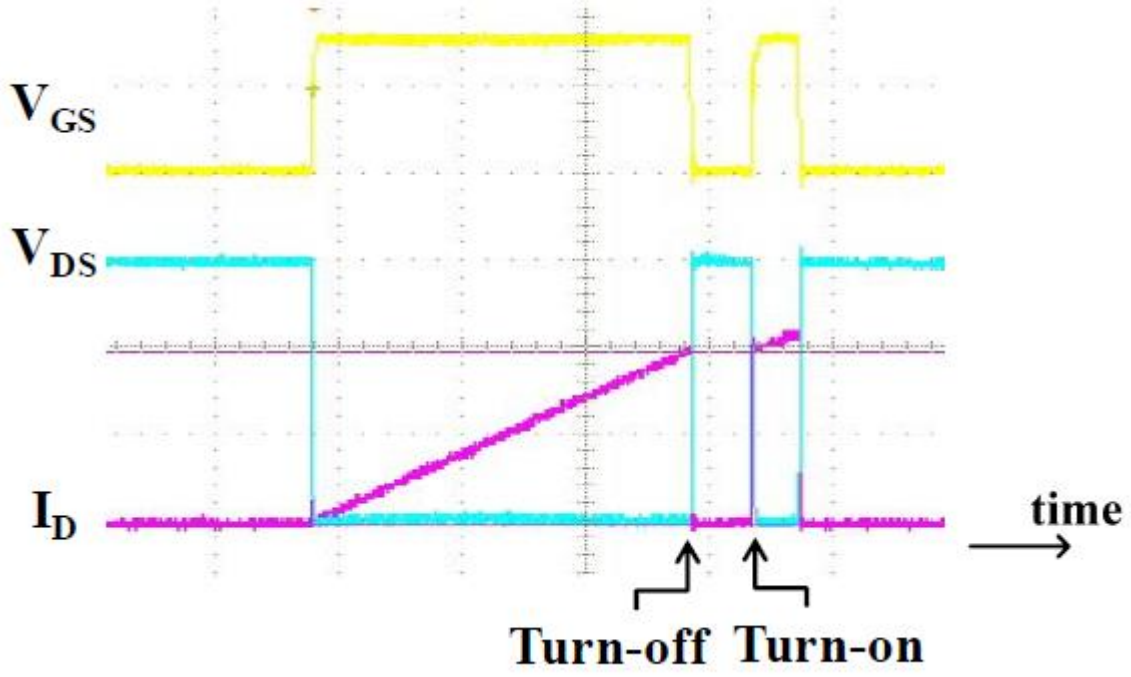

Figure 2.6: Ideal Switching Waveforms for Double Pulse Test

For SiC MOSFETs, high side MOSFET was switched OFF using gate driver providing V_{GS} = -5V and anti-parallel Schottky diode was used to conduct current at the high side. For GaN HEMTs, Infineon 1200V 15A, SiC Schottky diode is used on the high side. SiC diode can eliminate reverse recovery effect and therefore limit the current spike in the DUT during turn ON.

The inductor if 380 µH is used as load. The load inductor can be changed to obtain a desired drain current at the end of first pulse.

$$Vds = L\,\frac{\Delta I}{\Delta t}$$

For a given V_{DS} value, inductance and time period is chosen to obtain desired I_D value at the end of first switching cycle.

The drain current of the DUT is measured using 0.01 Ω shunt resistance for SiC MOSFETs and using Pearson current transformer for GaN HEMTs. The PCB is designed to achieve minimum parasitic inductance to minimize the switching ringing in the DUT.

2.2.2 High Speed Measurement Considerations

As seen in figure 2.6, the switching characterization of the device contains three waveforms, Gate-source voltage V_{GS}, drain-source voltage V_{DS} and drain current I_D.

The shunt resistor and Pearson transformer is used to measure I_D of the DUT because of its high bandwidth which does not cause aberrations during switching transients. All three waveforms share common source which is DUT source terminal. The drain current therefore needs to be inverted in the scope because original waveform measures negative current. All three probes used are single ended probes because the DUT is on the low side [17].

For high speed measurements, the probes need to have enough bandwidths to capture rise and fall edges of the switching transient. Rise time of the GaN is in order of 5 ns. Drain current rise time is also in the same order.

$$f_{bw} = \frac{0.35}{t_r}$$

Therefore, to ensure enough bandwidths, Tektronix P5100A, 2500 V, 500 MHz, 100x probe is used to measure V_{DS}, shunt resistor of 0.01 Ω, 2000 MHz is used to measure I_D and Tektronix P6139 300 V, 500 MHZ, 10x probe is used to measure V_{GS}.

The different types of probes have different propagation delays. Even though the delay time is several nanoseconds, in high speed measurements it matters a great deal as it can affect energy losses and turn ON and OFF times by a significant factor giving too high or too low energy losses and turn ON and OFF times. The shunt resistor consists of least propagation delay and Tektronix P5100A the most.

To compensate the different propagation delays, probes need to be de-skewed. The steps to de-skew the probes is explained below.

1. Choose one probe as the baseline probe.
2. Connect the first (baseline) and second probe to measure the same square waveform.
3. Carefully observe the rising edge and adjust the second waveform using de-skew option on the scope to ensure the same rising edge for both the probes.
4. Repeat the procedure for the third probe.

2.2.3 Switching Characterization Setup

The switching characterization is shown in figure 2.7. The double pulse (0-5 V) is generated using Agilent signal generator. Time period and amplitude of this signal can be adjusted on the signal generator. This signal is given to the double pulse tester (called DPT hereafter). The three waveforms (V_{DS}, V_{GS}, I_D) are captured on the oscilloscope and csv file is recorded on the USB drive. This data is then processed using MATLAB script to obtain switching energy losses (E_{SW}) values and, rise and fall timings.

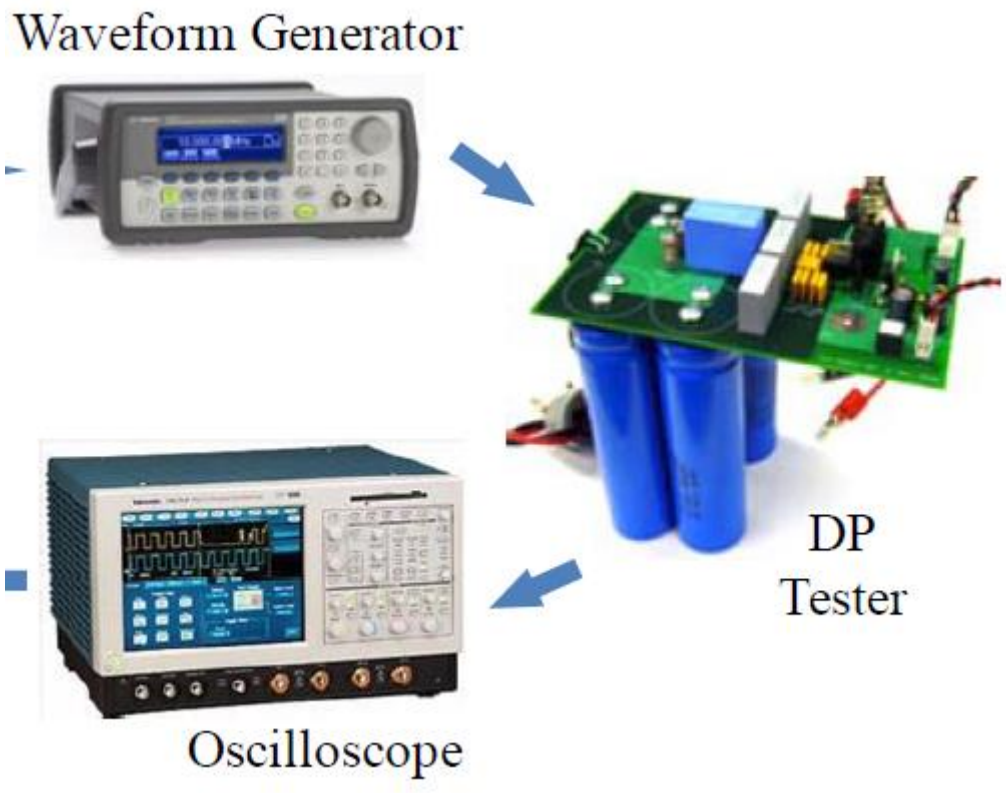

Figure 2.7: Switching Characterization Setup

2.2.4 Definitions of Switching Characteristics

Turn ON time T_{ON} is defined as time from I_D reaching 10% of the steady state current to V_{DS} falling to 10% of the DC bus voltage.

Turn ON delay time is defined as time from V_{GS} rising to 10% of the final V_{GS} voltage to I_D reaching 10% of the steady state current.

The turn OFF time T_{OFF} is defined as time from V_{DS} rising to 10% of the bus voltage to I_D falling to 10% of the load current.

The turn OFF delay time is defined as time from V_{GS} falling to 90% of the V_{GS} voltage to V_{DS} rising to 10% of the bus voltage.

Turn ON switching energy and turn OFF switching energy are integrals of products of V_{DS} and I_D over T_{ON} and T_{OFF} respectively [18].

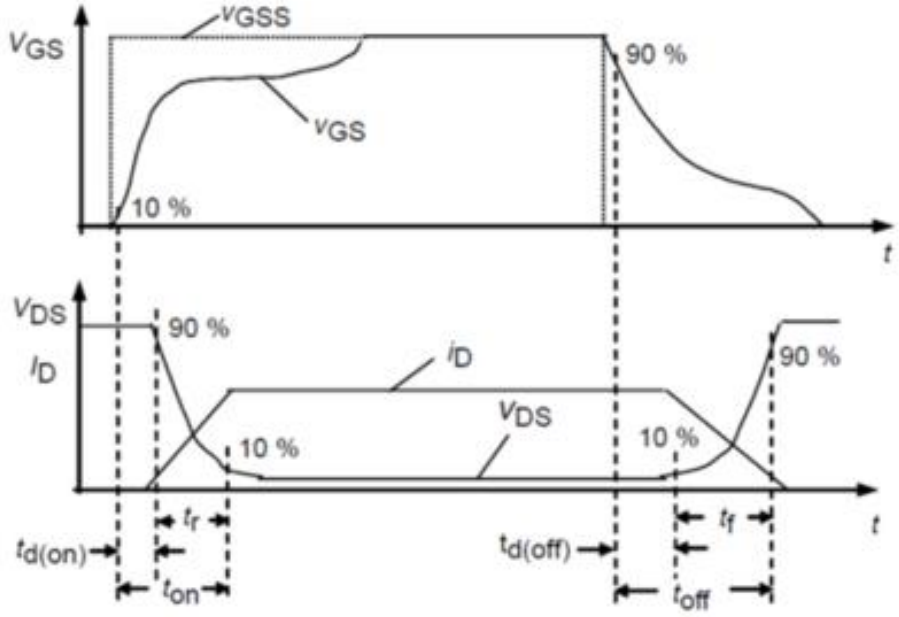

Figure 2.8: Switching Time Definitions

2.2.5 MOSFET Switching Behavior under Clamped Inductive Load

Under inductive load, load inductor current remains unchanged while current flows through high side diode during MOSFET turn OFF and flows through MOSFET during MOSFET turn ON. Switching under these conditions is most common commutation mode for power semiconductor devices in hard switching converters.

Ideal MOSFET Switching Behavior

The double pulse switching setup shown in figure 2.9 is used to explain ideal MOSFET behavior. Following assumptions are made to ensure ideal operation [2] [19].

1. Inductor load current is constant during switching.
2. Freewheeling diode is ideal.
3. Gate driver is ideal step voltage source.
4. No parasitic inductance from device packaging or circuit.

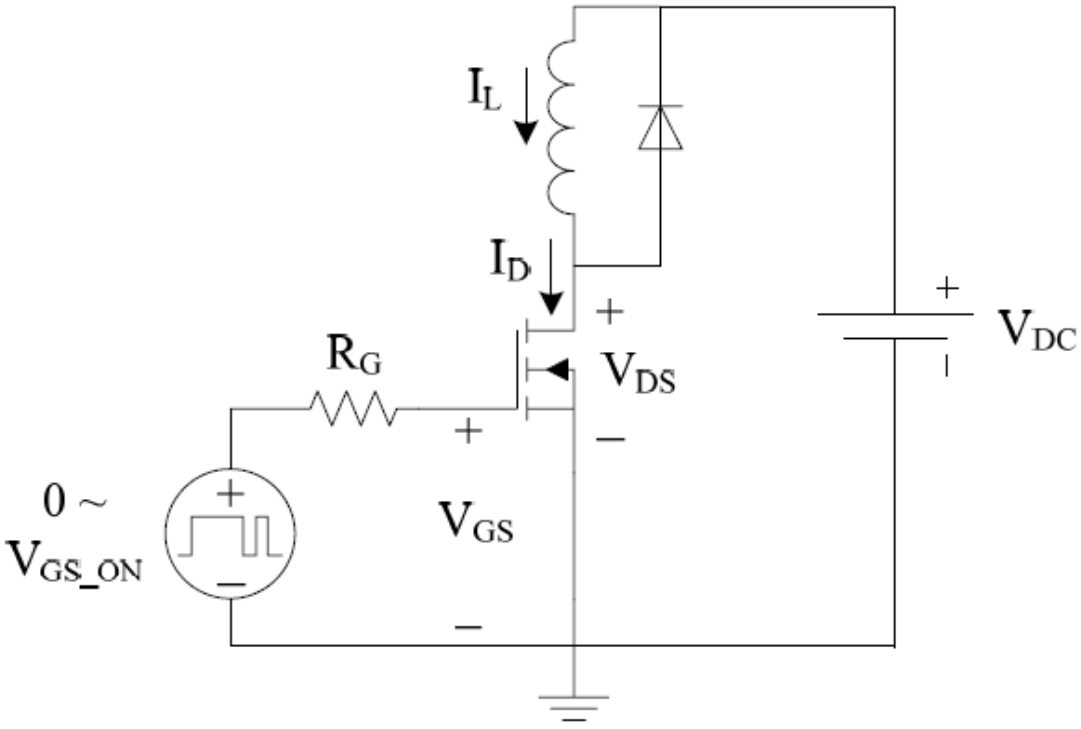

Figure 2.9: Ideal Double Pulse Test Schematic

Turn ON Process

The turn ON of a MOSFET is divided in 4 steps as shown in figure 2.10.

Step 1: Turn ON Delay

When the gate voltage steps from 0 V to V_{GSON}, DUT input capacitance starts to be charged. MOSFET will not switch until gate voltage is reached threshold voltage V_{GSTH}. This time represents turn ON delay.

During turn ON delay,

$$V_{DS} = V_{DC}$$

$$I_D = 0$$

$$V_{GS} = V_{GSON}\left[1 - \exp\frac{-t}{R_G C_{ISS}}\right]$$

R_G is gate resistance and C_{ISS} is DUT input capacitance.

Step 2: Current Rise

At the end of step 1, V_{GS} has risen to V_{GSTH} and MOSFET starts to turn ON. MOSFET starts to conduct current and therefore current from freewheeling diode is transferred to MOSFET. During this period, MOSFET still blocks DC bus voltage because diode is still conducting. When all the load current starts flowing through MOSFET, this step completes.

During current rise,

$$V_{DS} = V_{DC}$$

$$I_D = g_{fs}(V_{GS}, V_{DS})V_{GS}$$

$$V_{GS} = V_{GSON}\left[1 - \exp\frac{-t}{R_G C_{ISS}}\right]$$

g_{fs} is transconductance of MOSFET dependent on both V_{GS} and V_{DS}. MOSFET is still in saturation region because V_{DS} is still high. Therefore current is only dependent on gate voltage.

Step 3: Voltage Fall

At the end of second step, all the load current is flowing through MOSFET. In step 3, diode starts to block the voltage, therefore V_{DS} for MOSFET starts decreasing but since MOSFET is still in saturation region, V_{GS} value remains unchanged. The gate current deviates from C_{GS} to discharge miller capacitance C_{GD}. At the end of step 3, V_{DS} drops from V_{DC} to ON state voltage drop.

During voltage drop,

$$\frac{dV_{DS}}{dt} = -\frac{V_{GSON} - V_{plateau}}{R_G C_{GD}}$$

$$I_D = I_L$$

$$V_{GS} = {g_{fs}}^{-1} I_L$$

V_{DS} is hard to express because C_{GD} is nonlinear function of V_{DS}.

Step 4: V_{GS} Rise

At the end of step 3, MOSFET is completely turned ON. In this step, V_{GS} is increased to a value higher than $V_{PLATEAU}$ to observe low channel resistance. As gate voltage is increased, R_{DSON} is decreased. Therefore with increase in V_{GS}, low R_{DSON} is observed.

$$V_{DS} = R_{DSON} I_L$$

$$I_D = I_L$$

Turn OFF Process

Similar to turn ON, the turn OFF of a MOSFET is divided in 4 steps as shown in figure 2.11.

Step 1: Turn OFF Delay

When the gate drive voltage is stepped to zero, V_{GS} starts to fall. Therefore increase in R_{DSON} is seen. Because of increase in R_{DSON}, V_{DS} is also increased. When V_{GS} drops to miller plateau voltage this step ends.

$$V_{DS} = R_{DSON} I_L$$

$$I_D = I_L$$

$$V_{GS} = V_{GSON} \left[\exp \frac{-t}{R_G C_{ISS}} \right]$$

Step 2: Voltage Rise

When V_{GS} is reduced to $V_{PLATEAU}$, MOSFET enters saturation region. MOSFET starts blocking voltage and V_{GS} remains constant at $V_{PLATEAU}$. At the end of step 2, V_{DS} = V_{DC} = DC bus voltage and diode starts conducting current.

$$\frac{dV_{DS}}{dt} = -\frac{V_{plateau}}{R_G C_{GD}}$$

$$I_D = I_L$$

$$V_{GS} = {g_{fs}}^{-1} I_L$$

Step 3: Current Fall

At this step, load current is transferred to diode from MOSFET. The input capacitance of DUT continues to discharge until V_{GS} drops to V_{GSTH}. This step ends when total load current is transferred to diode.

$$V_{DS} = V_{DC}$$

$$I_D = g_{fs}(V_{GS}, V_{DS}) V_{GS}$$

$$V_{GS} = V_{GSON} \left[\exp \frac{-t}{R_G C_{ISS}} \right]$$

Step 4: V_{GS} Fall

The turn OFF process is completed by the end of third step. However, DUT input capacitance continues to discharge until V_{GS} reaches zero.

$$V_{DS} = V_{DC}$$
$$I_D = 0$$

The above turn ON and turn OFF processes conclude that

1. Smaller junction capacitances are essential for faster switching time.
2. Higher turn ON voltage and lower gate resistance lead to faster switching transients
3. For high load current, turn ON takes more time lengthening all the steps.

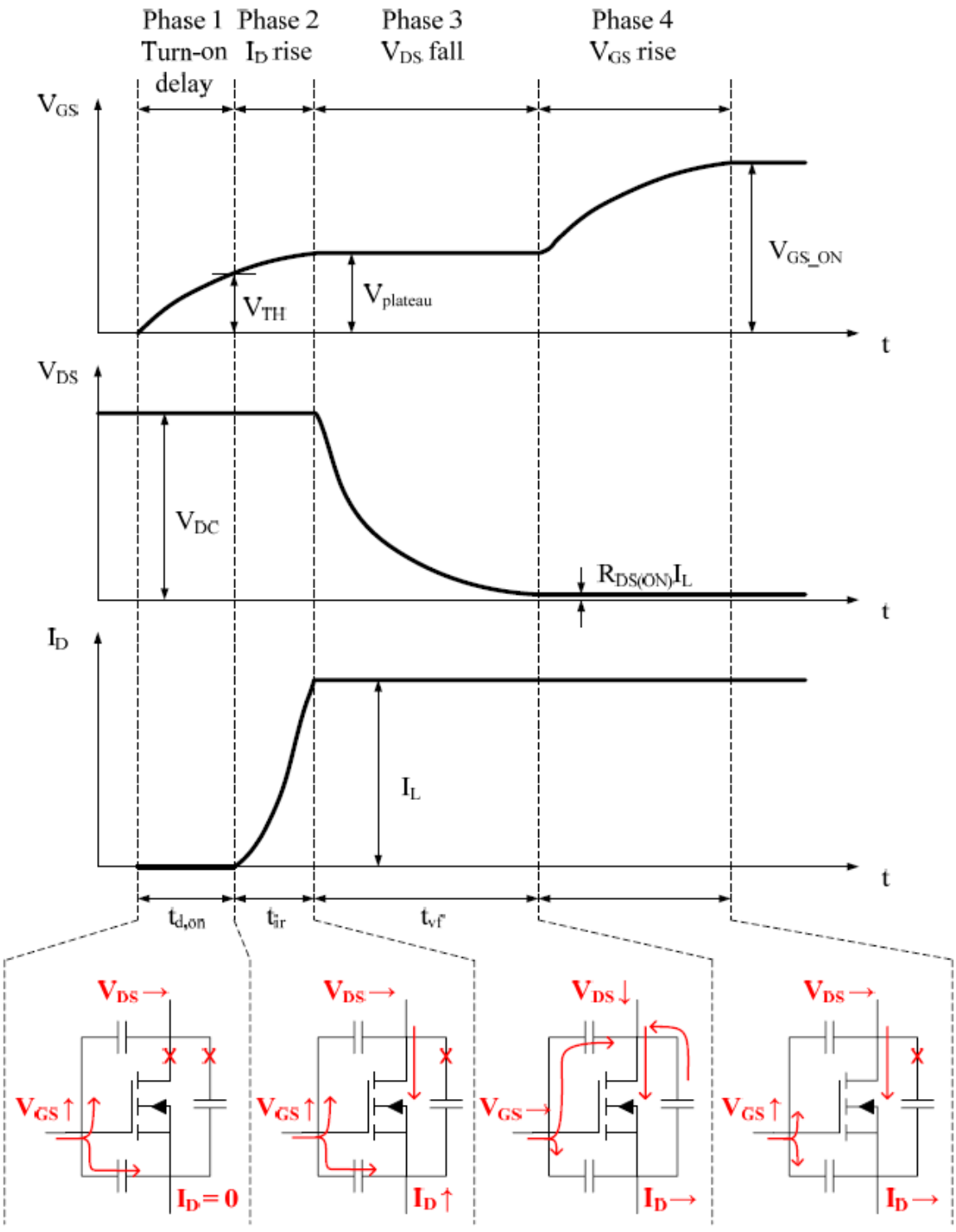

Figure 2.10: MOSFET Turn ON Steps

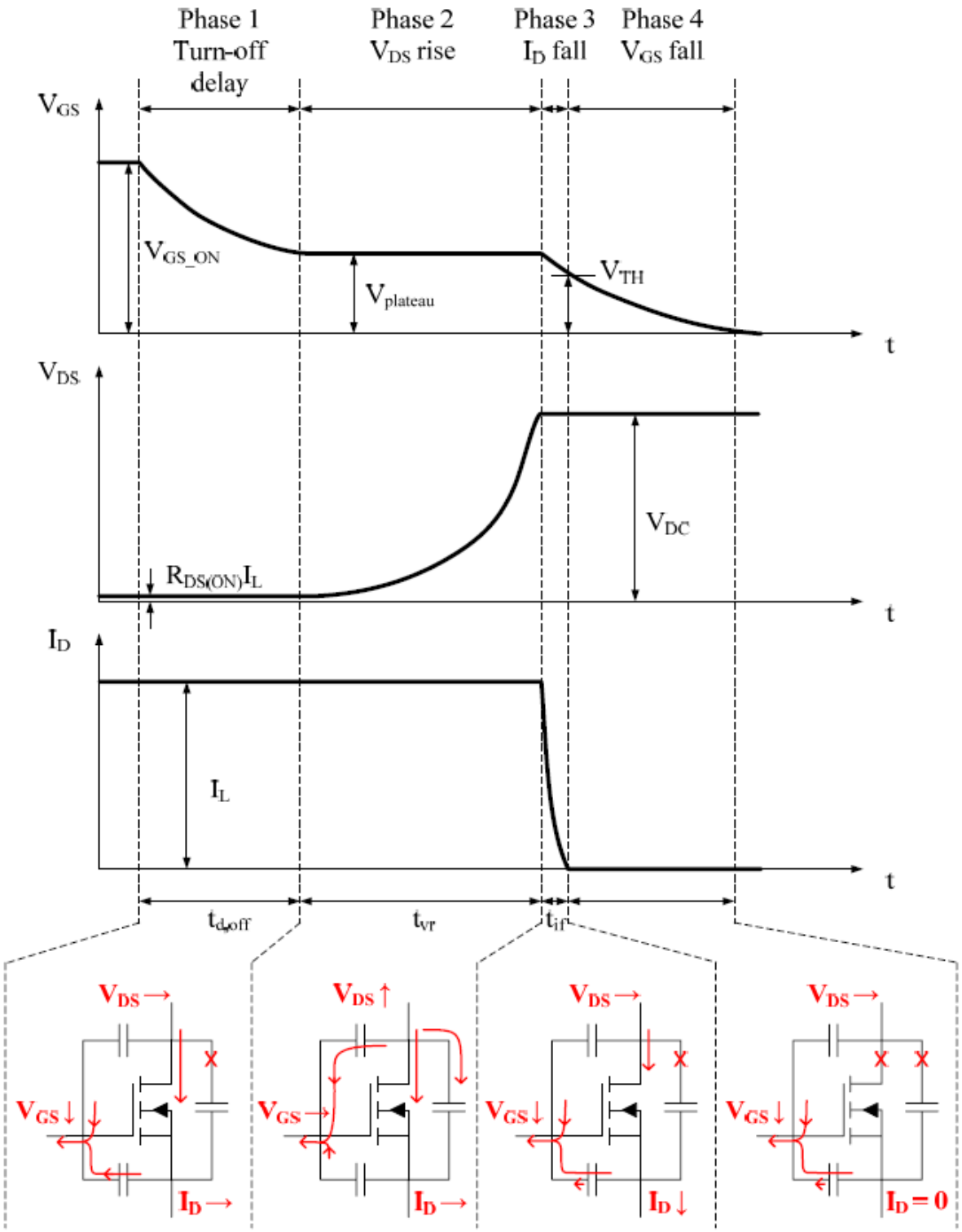

Figure 2.11: MOSFET Turn OFF Steps

Non Idealities

In this section, diode junction capacitance C_J and switching loop inductance L_{DS} a re-introduced in the ideal circuit.

The diode junction capacitance C_J will change the measured drain current waveform. During MOSFET turn ON, C_J is charged and that charging current will add to load current giving current spike during turn ON. During MOSFET turn OFF, C_J is discharged by drawing load current dropping drain current before diode starts conducting. The inductor EPC is in parallel with the C_J causing same effect.

L_{DS} comes from parasitic inductance along drain current paths. When drain current goes from I_L to zero, voltage drop across L_{DS} changes V_{DS} waveform. It forms a notch during turn ON and peak during turn OFF.

L_{DS} and C_J tend to resonate causing high frequency ringing in the waveforms.

Switching Trajectories

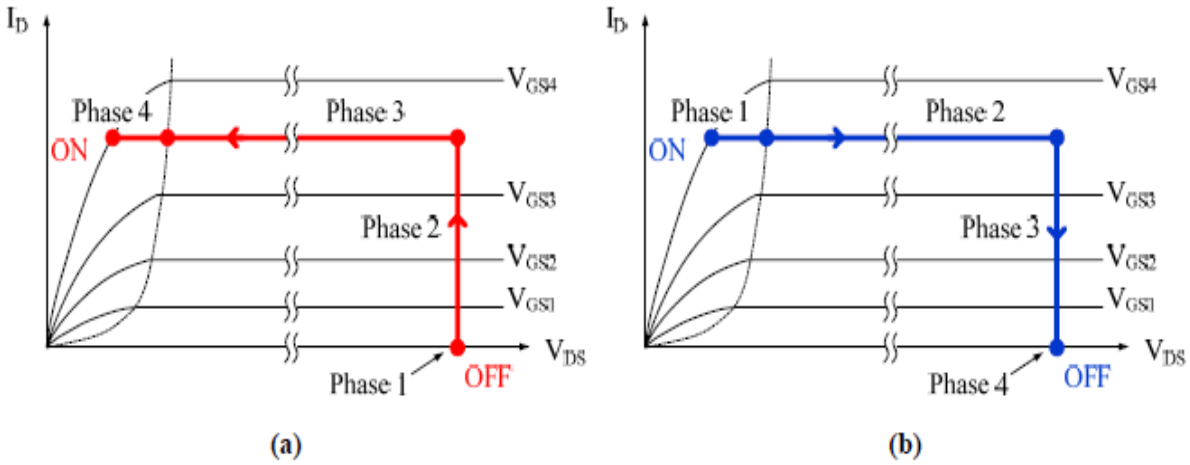

Figure 2.12: MOSFET Switching Trajectories

2.2.6 Gate Charge Measurement

If a certain charge is injected in the gate for a given V_{DD}, the gate voltage will rise to the certain level. According to datasheet characteristics, three gate charge parameters are discussed.

- Q_G is the total gate charge. It is calculated from the origin to the peak value of gate voltage.
- Q_{GS} is the gate to source charge. It is the charge from t_0 to t_2.
- Q_{GD} is gate to drain or miller charge. It is the charge from t_2 to t_3.

The setup for gate charge measurement is the similar to double pulse test. A constant current gate driver is used instead of regular gate driver. For a given V_{DS} and I_D, gate waveform is measured using oscilloscope. The time for gate voltage to rise from origin to its peak value is measured. Since we are injecting constant current from a gate driver, a simple product of gate current and time gives the gate charge. And gate charge curve may be plotted using this data [19-21].

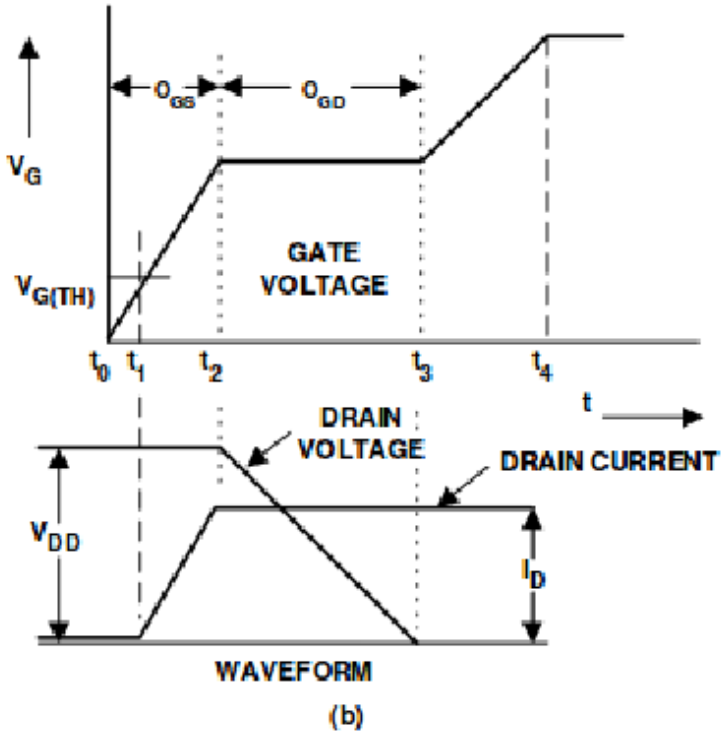

Figure 2.13: Gate Charge

3. Gallium Nitride (GaN) HEMTs Characterization

The basic structure of GaN HEMT is shown in the figure below. The source and drain electrodes are pierced through the AlGaN layer to form ohmic contact with the underlying 2DEG (two dimensional electron gas) layer so it creates the short circuit between source and drain terminals until this layer of 2DEG is depleted [7]. Gate electrode is placed on AlGaN layer to deplete this 2DEG layer. When negative potential is applied to the gate with respect to source, 2DEG layer will be depleted and flow of current between drain and source will be blocked.

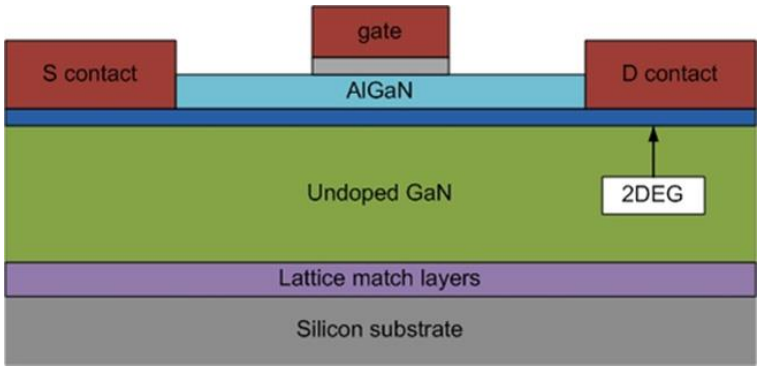

Figure 3.1: GaN HEMT Structure

Since electrons are derived from wideband gap material, there is no impurity scattering of electrons which results in high electron mobility and at low temperatures, the lattice scattering is also low.

GaN is composed of Ga with a large ionic radius and N with a small ionic radius and thus forms a slightly distorted tetrahedral arrangement, it exhibits spontaneous polarization [22]. When AlGaN is grown on GaN, piezoelectric polarization is further added due to the tensile stress generated in the AlGaN layer. With these two polarization effects, a fixed positive charge is generated near the AlGaN/GaN Heterojunction in the AlGaN layer and correspondingly a two-dimensional electron gas is induced in the GaN layer. The density of free electrons in GaN increases with increasing Al content of AlGaN. It is a unique characteristic of the AlGaN/GaN

Heterojunction that a high density of two-dimensional electrons is achieved without the addition of any donor impurities to the AlGaN layer.

Gallium Nitride transistors have R_{DSON} vs. V_{GS} curves similar to Si MOSFETs. The value of R_{DSON} is significantly less than that of Si MOSETs. GaN transistors have positive temperature coefficient which is slightly less than Si.

The threshold voltage of GaN is lower than that of Si MOSFETs. In addition to lower R_{DSON}, GaN transistors have lower device capacitance as well. Since the device capacitances are very small, it takes less time to charge and discharge the device during each switching making it preferred device for very high frequency operations.

GaN transistors are lateral devices. There is no parasitic bipolar junction like Si based MOSFETs. The device has different mechanism for body diode operation but similar function. At zero bias between gate and source, all the electrons are depleted. As the drain voltage is decreased, a positive bias on the gate is created relative to drift region. Once gate is reached to threshold voltage, there are enough electrons to conduct current in reverse direction. There are no minority carriers involved in conduction therefore there are no reverse recovery losses. Since it takes threshold voltage to turn on the transistor in reverse direction, forward voltage drop for body diode is higher than Si MOSFETs [23].

The Following table shows the GaN HEMTs that were characterized.

Device manufacturer	Blocking Voltage (V)	Current (A)	ON Resistance (mΩ)	Gate Voltage	Type	Packaging
RFMD	650	30	45	+20V / -20V	Cascode	TO-247
GaN Systems	650	30	52	+10V / -10V	e-GaN	GaNpx
Transphorm	600	17	150	+18V / -18V	Cascode	QFN

Table 3.1: GaN HEMTs Parameters

3.1 Static Characteristics

Using Tektronix 371A curve tracer, the output characteristics of a RFMD GaN transistor were measured. The pin geometry for this transistor is different than the standard pin geometry. Therefore connecting wires were used to connect this transistor with the curve tracer. Since the kelvin connection was not used, the wire resistance and contact resistance was also added in the transistor ON resistance, giving false I-V characteristics. The data observed was different than the preliminary datasheet data provided by the manufacturer.

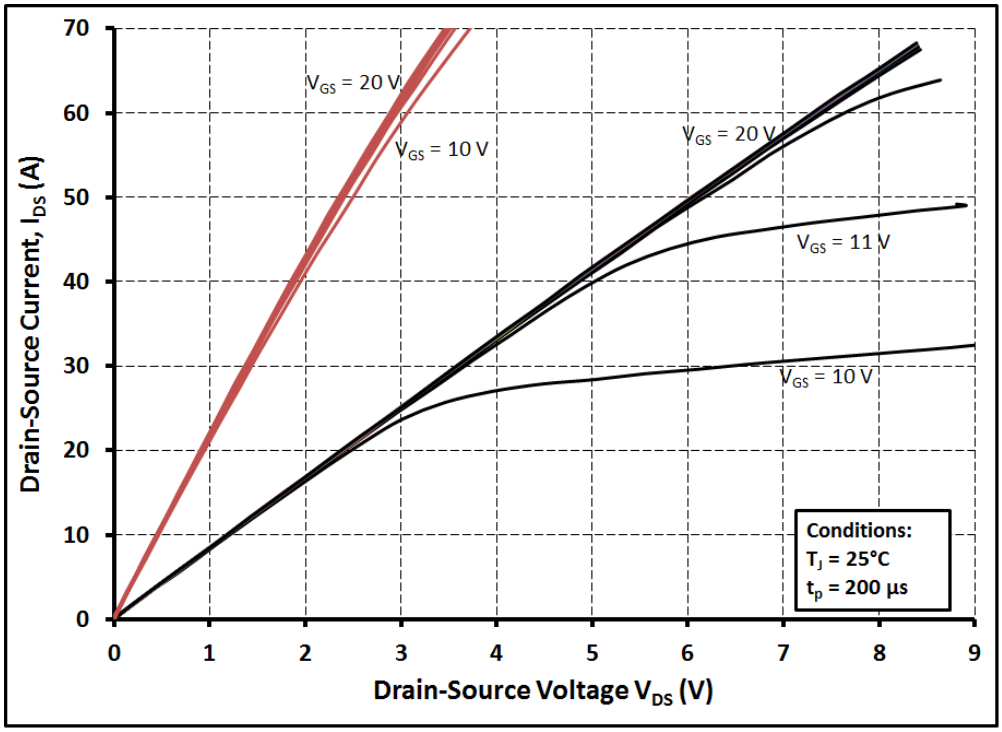

Figure 3.2: RFMD GaN I-V Characteristics (Kelvin vs. no Kelvin)

To debug the test setup, the other transistor sample was used to ensure transistor functionality. To calibrate the curve tracer, Infineon Si CoolMOS was used to measure output characteristics. The data acquired from the curve tracer was consistent with the datasheet parameters. When the curve tracer calibration was complete, kelvin contacts were used for RFMD transistor. The data acquired was consistent with the datasheet parameters in this case.

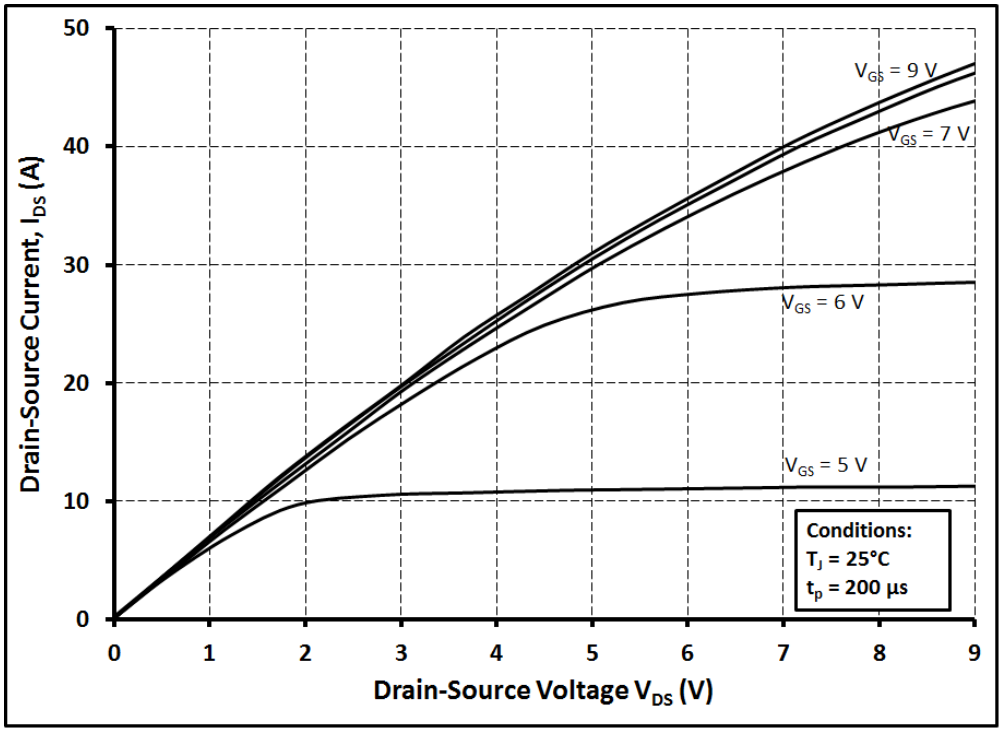

Figure 3.3: Silicon CoolMOS I-V Characteristics

Rated gate voltage for transistor is +10 V. The output characteristics are measured for gate voltages from 5 V to 10V in the interval of every 1 V. The change in the ON resistance with respect to gate voltage can be seen in the figures.

3.1.1 Static Characteristics of RFMD GaN Transistors

Total 3 samples from same batch were characterized to establish part to part variation and estimate absolute minimum, typical and maximum values for ON resistance. The temperature dependence of the ON resistance is also characterized to estimate the thermal coefficient of these transistors.

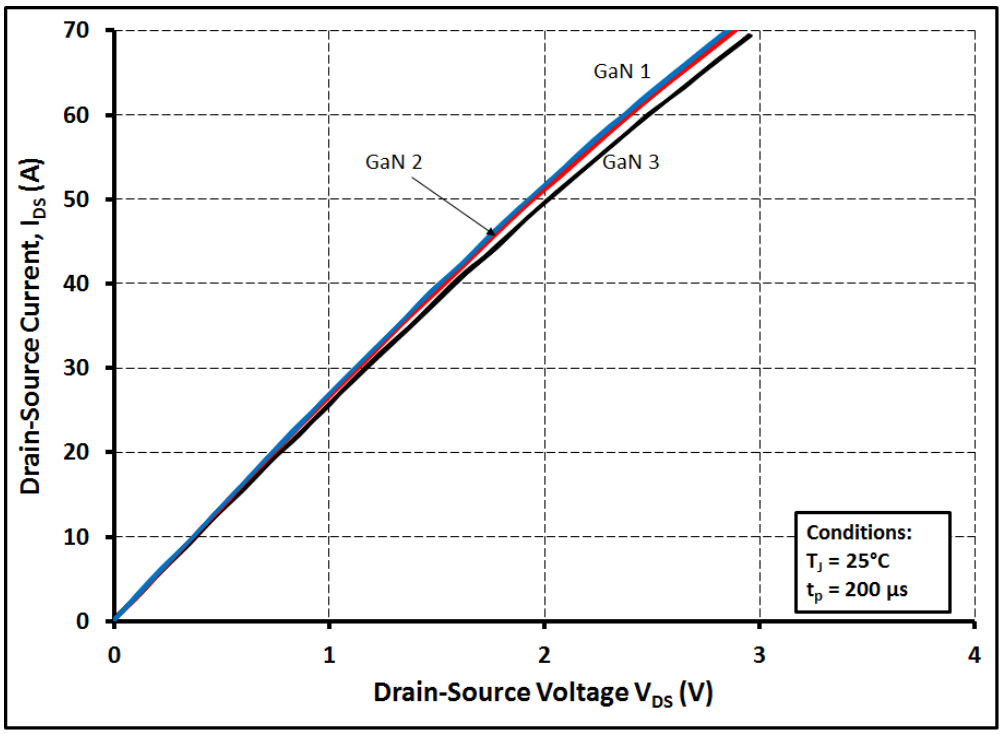

Figure 3.4: Part to part Variation for RFMD GaN HEMTs

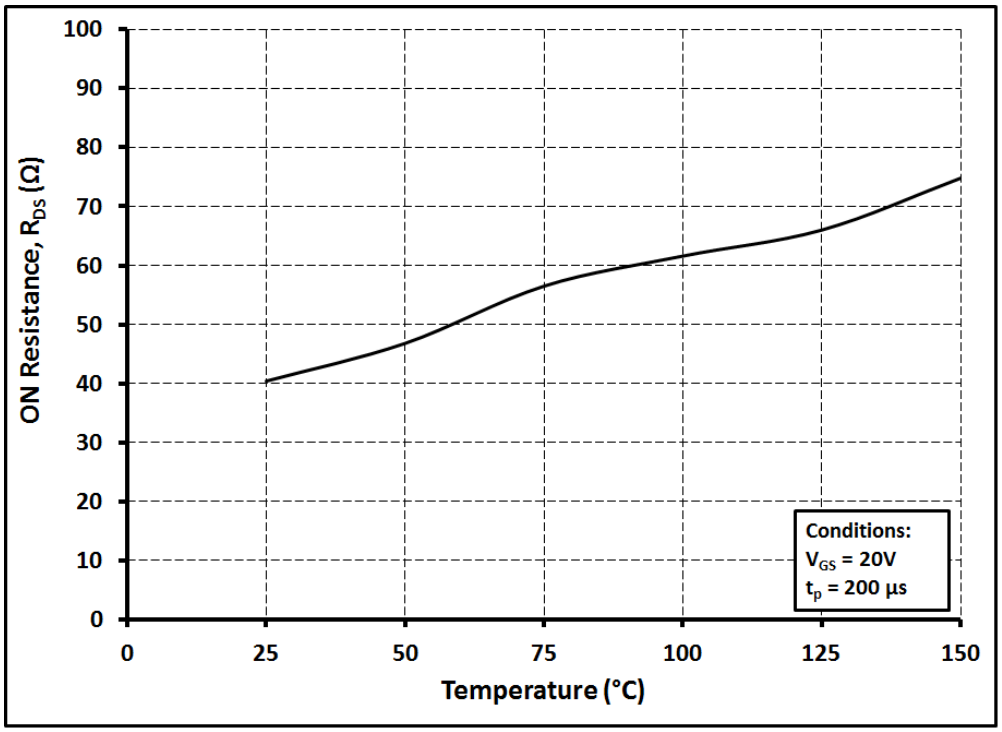

Figure 3.5: Temperature Dependance of ON resistance for RFMD GaN HEMTs

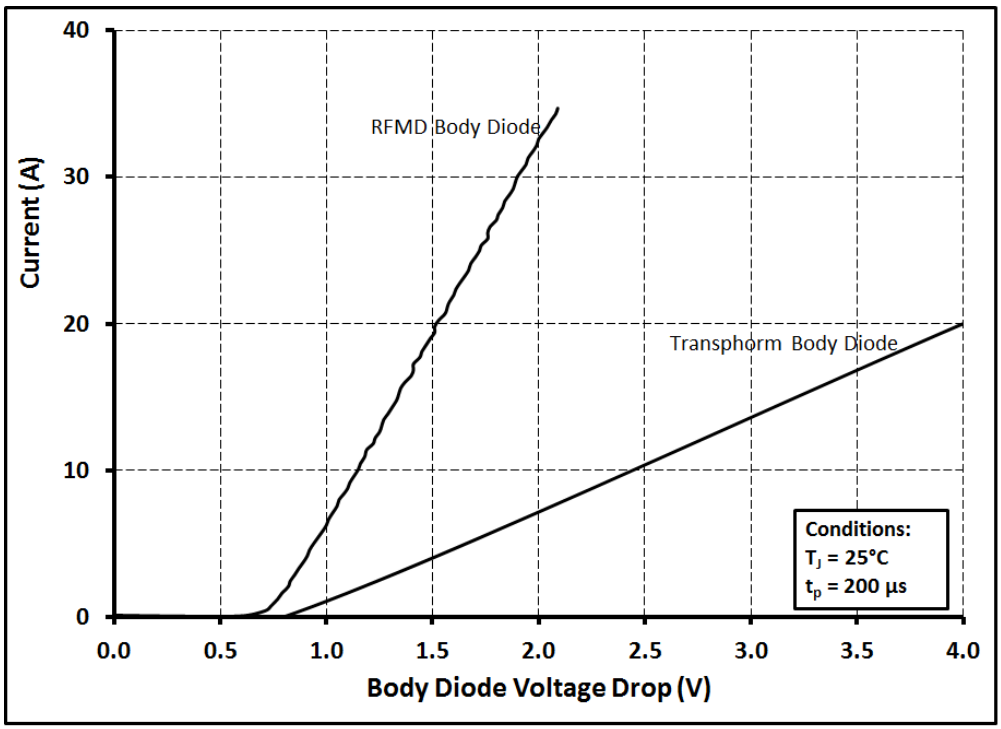

Figure 3.6: Body Diode Characteristics for RFMD and Transphorm GaN HEMTs

3.1.2 Static Characteristics of GaN Systems and Transphorm Transistors

The GaN systems and Transphorm transistors are also characterized for the output characteristics at various gate voltages going up to their respective gate voltages. For the GaN systems transistor, as seen in the figure, after saturation, drain current is decreasing with increase in forward voltage drop. One reason for this can be the self-heating of the transistor. For the Transphorm device, the transistor acted like resistor around the rated current. There was no separation in I-V curves for different gate voltages. The ON resistance was the same irrespective of the gate voltage.

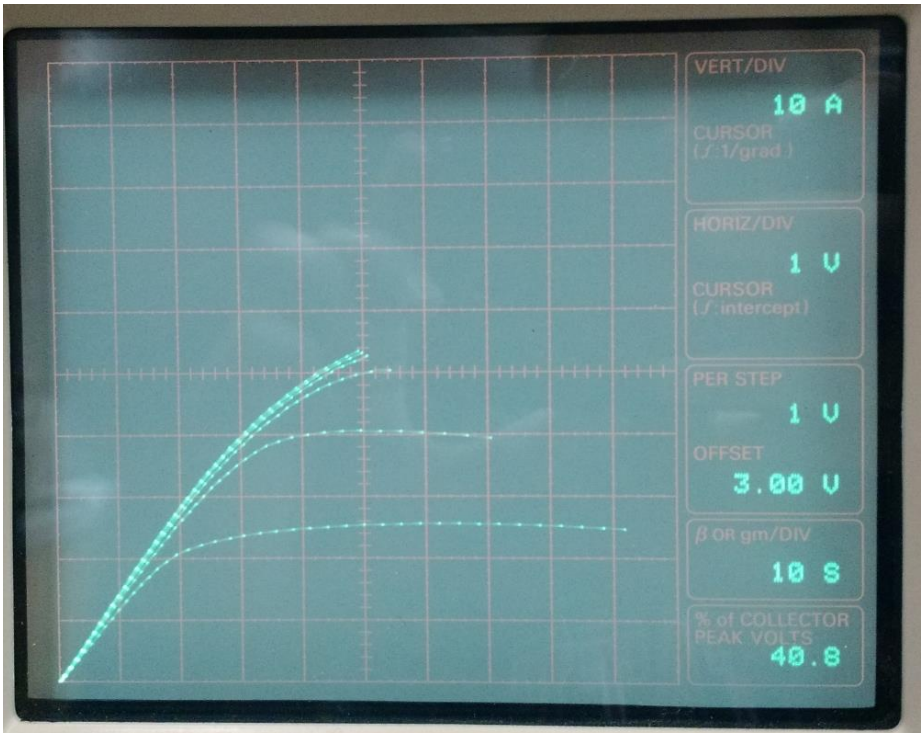

Figure 3.7: I-V Characteristics GaN Systems HEMT

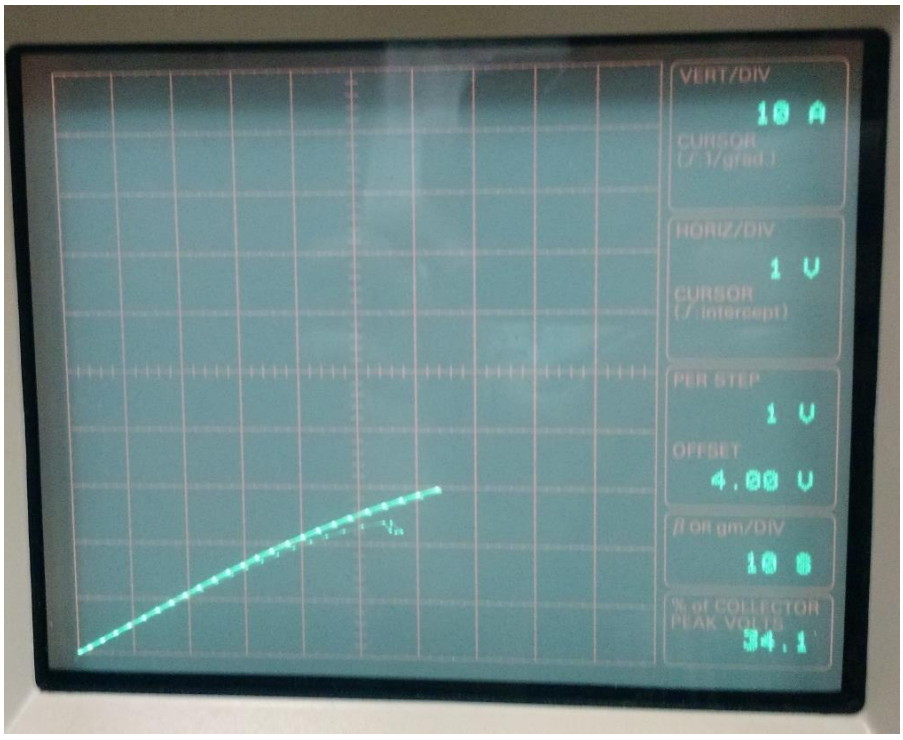

Figure 3.8 I-V Characteristics Transphorm HEMT

3.2 Switching Characteristics

The switching characteristics were also measured using the double pulse tester circuit explained in chapter 2. For the RFMD cascade transistor, Silicon Labs Si-8233 half bridge gate driver was used to provide gate pulse of +10 V / -5 V. Because of the parasitic inductance on the PCB and overlapping of the ground traces and high dV/dt traces, lot of ringing was observed and caused to transistor to fail. Since all the probe grounds were not connected to the source of the transistor, there was a ground loop which caused heavy current and voltage ringing. The rated gate voltage is +20 V, but to prevent the device, only +10 V gate voltage was given. The switching results for various gate resistances are measure to confirm that the ringing goes down with the increase in gate resistance. The dV/dt and dI/dt are measured at various DC bus voltages. Inductor value was chosen for a given drain current and DC bus value using a formula:

$$V = L\frac{\Delta I_L}{\Delta t}$$

V = DC bus voltage, I_L = inductor current = drain current.

Also, DC capacitor value decided to keep the voltage drop minimum at the end of last switching cycle. It is recommended that voltage drop be less than 10% of the DC bus voltage value. It is decided using the following formula:

$$I = C\frac{\Delta V}{\Delta t}$$

I = drain current, delta V = voltage drop, C = capacitance

After switching off the power supply, to capacitor voltage must drain to ensure the safety. It must drop to at least 10% of the DC bus voltage within 1 minute. The bleeder resistor value may be calculated using the following formula:

$$v_{final} = V_{DS} * \exp(\frac{-t}{RC})$$

3.2.1 RFMD Switching Results

The switching results for RFMD GaN HEMT are discussed in this section. The double pulse test PCB is designed using cadence Allegro [24-26]. Gate driver is soldered on board. The gate voltage pulse waveform is shown in figure 3.9. When DC bus voltage of 200V is applied to the DPT circuit, huge ringing in current waveform is observed. The capacitor bank is not soldered on board. Therefore there is a lot of inductance because of wires connecting DC capacitor bank to the PCB. Therefore low frequency ringing is observed in drain current waveform. The waveforms are captured for 0Ω, 20Ω and 20Ω with 80Ω ferrite bead external resistance for DC bus voltage of 200V and 400V. Theoretically, ringing should reduce with increase in external gate resistance. Because of the noise, it is hard to say if ringing is going down. In all the waveforms shown below, channel 1 is V_{DS}, Channel 2 is I_D and channel 3 is V_{GS}.

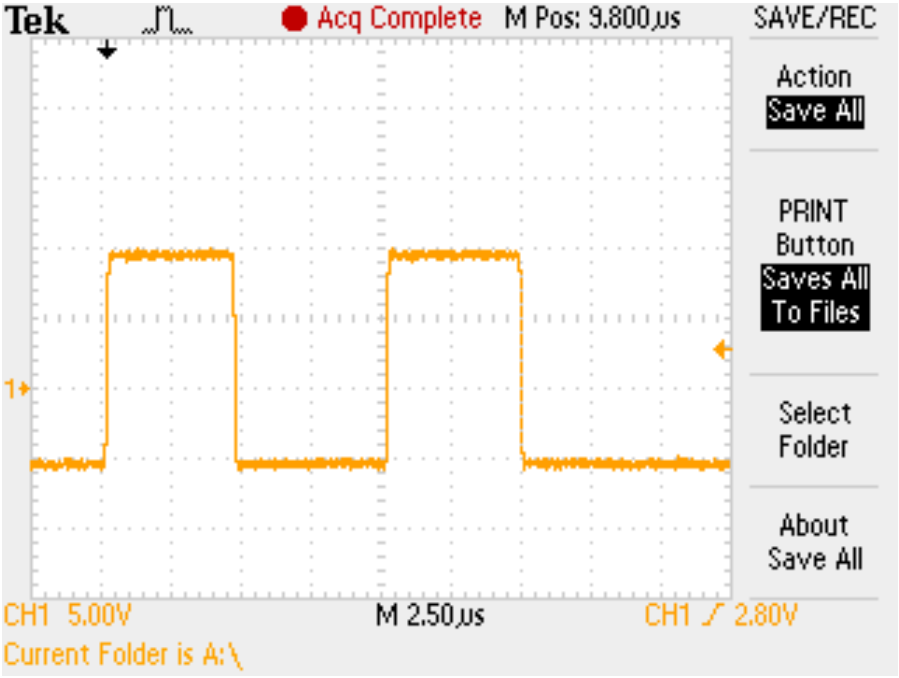

Figure 3.9: Gate to Source Voltage for Double Pulse Test

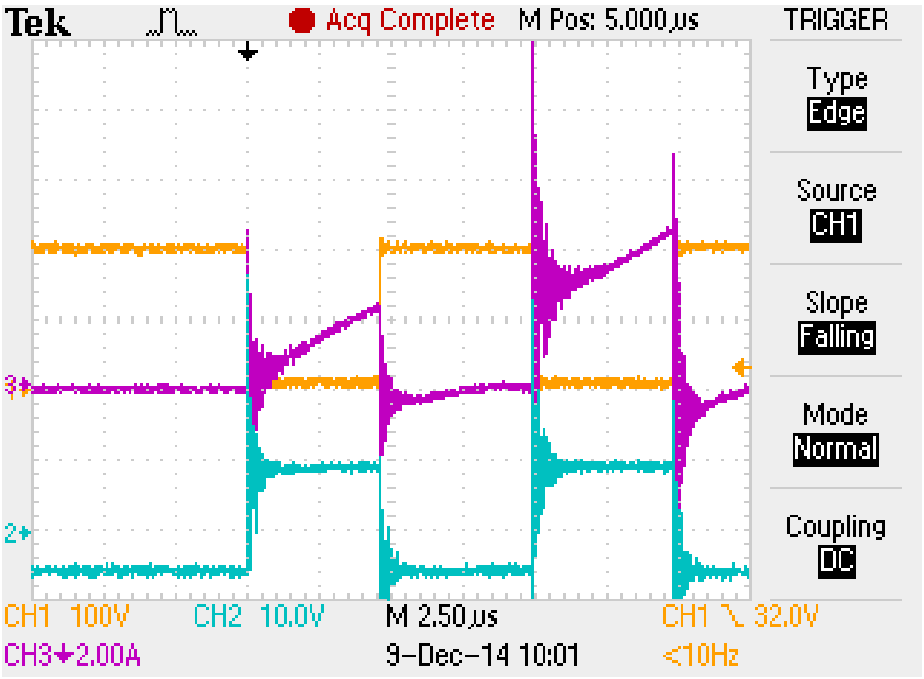

Figure 3.10: Switching Results at V_{DS} = 200V, I_D = 5A and R_G = 0Ω

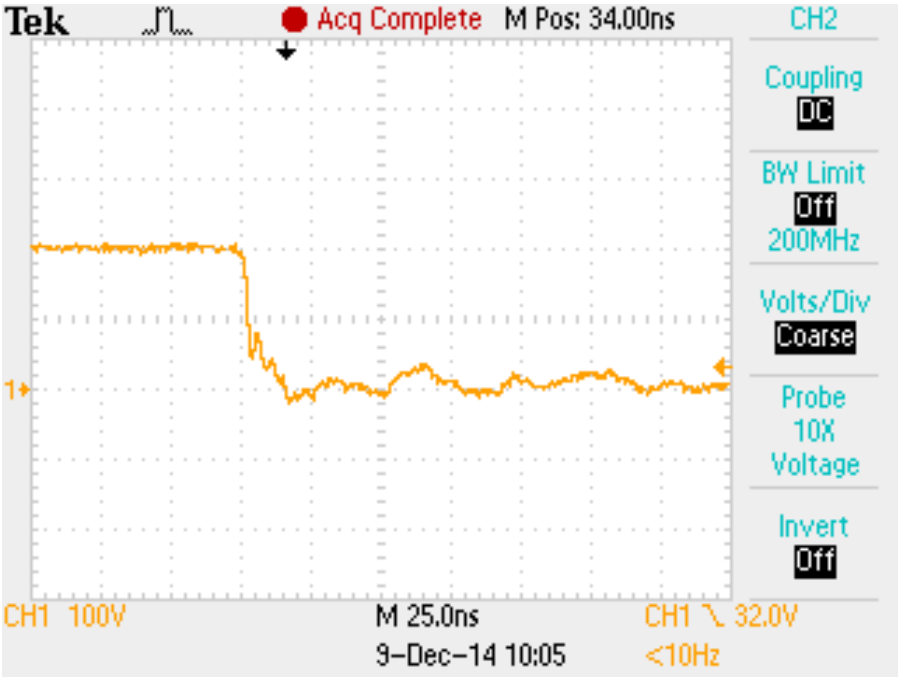

Figure 3.11: Turn ON dV/dt

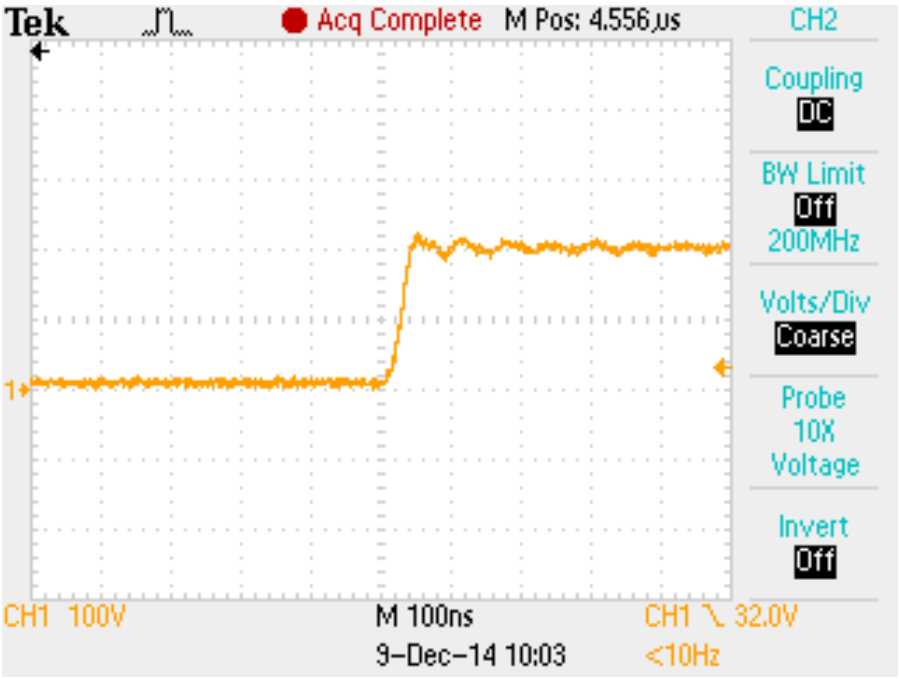

Figure 3.12: Turn OFF dV/dt

The turn ON and turn OFF dV/dt waveforms are shown in the figures 3.11 and 3.12 respectively. The device rated gate voltage is +20 V. To prevent the device from damage, only +10 V gate voltage is given in the DPT. Therefore, dV/dt is measured to be 10 V/ns. Theoretically GaN HEMTs can have a very high dV/dt up to 300V/ns. The switching waveforms at V_{DS} = 200V and external R_G = 20Ω are shown in figure 3.13. This waveform data is acquired in csv file format and then it is processed using MATLAB script to calculate switching energy losses. At V_{DS} = 400V and V_{GS} = 10V and I_D = 10A, the turn ON energy loss is 30 µJ and turn OFF energy loss is 20 µJ. The energy loss will reduce with the increase in gat voltage because the dV/dt will increase which will have very low current and voltage overlap reducing energy losses.

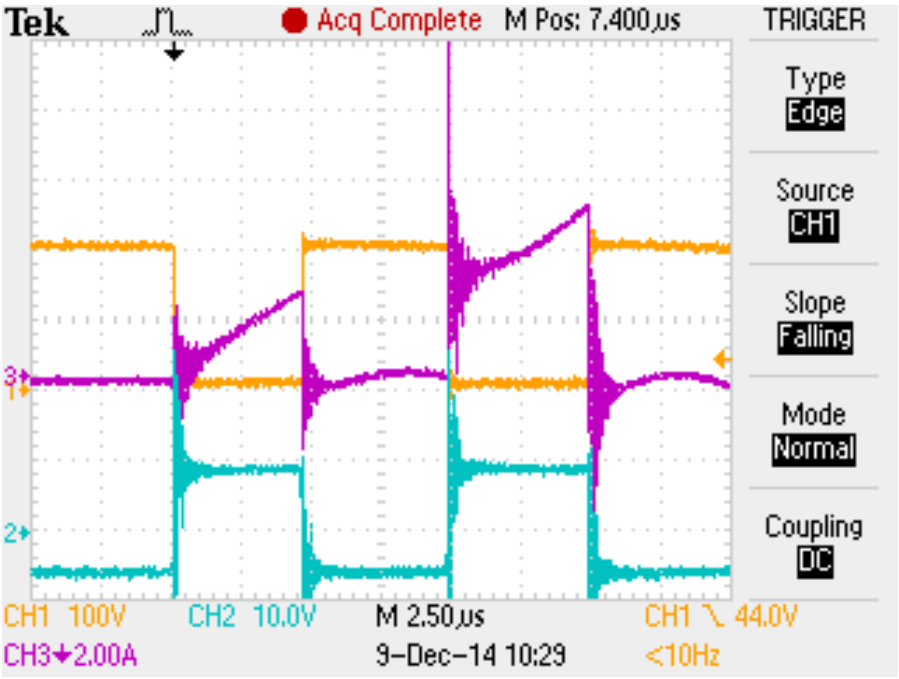

Figure 3.13: Switching Results at V_{DS} = 200V, I_D = 5A and R_G = 20Ω

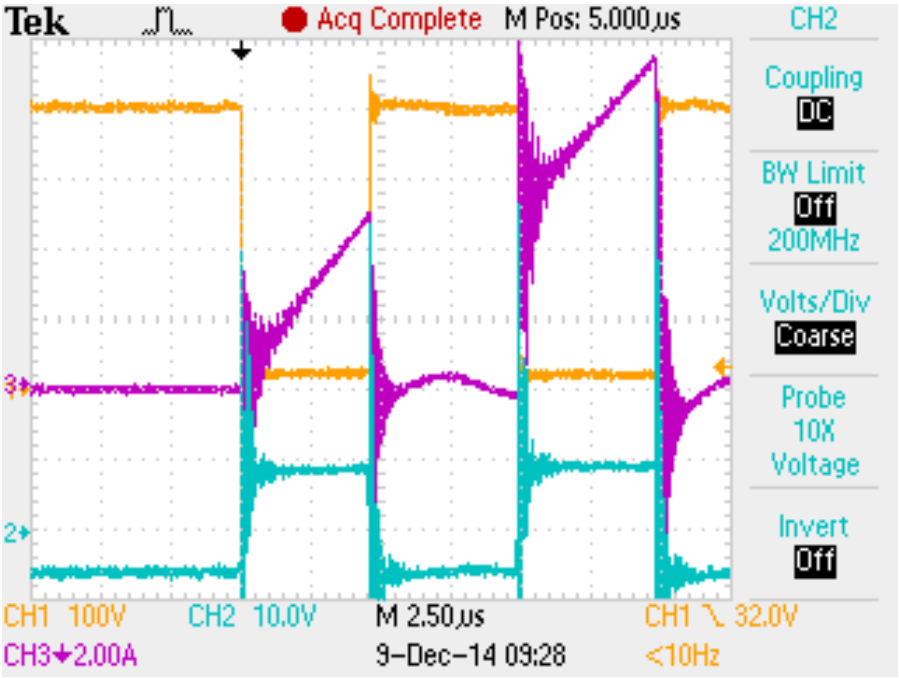

Figure 3.14: Switching Results at V_{DS} = 400V, I_D = 10A, R_G = 20Ω and Ferrite Bead 80Ω

3.2.2 Transphorm Switching Results

The Transphorm GaN HEMT is characterized for switching time measurements and switching losses. The DC bus voltage of 300V is applied to the circuit. Rated current of this device is 17A. 5 pulses were given instead of 2 pulses to current to rise to 15A which is close to rated current. The switching waveforms are observed at V_{DS} = 300V and I_D = 15A. The zoomed in turn OFF and turn ON waveforms are shown in figure 3.16 and 3.17 respectively.

The CREE CRD-001 gate driver is used to drive this device at +15V and -5V. Gate driver is causing lot of ringing because it can only withstand 40 V/ns dV/dt and dV/dt of approximately 100 V/ns is observed while switching this device from the zoomed in turn ON and turn OFF figures. The new gate driver needs to be designed which can withstand high dV/dt.

Because of high ringing caused by gate driver, ringing in drain current and drain to source is observed.

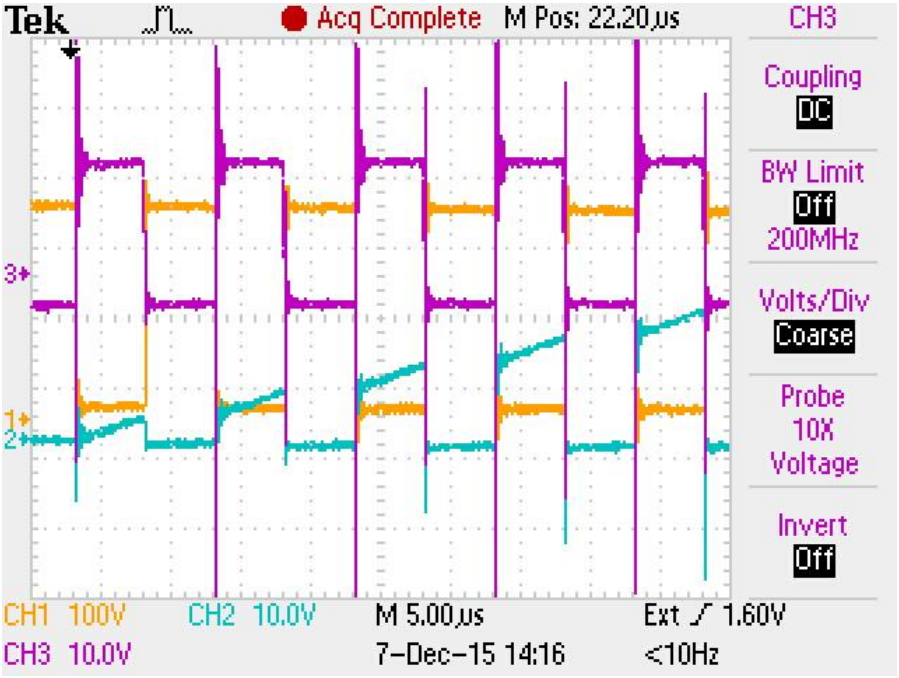

Figure 3.15: Switching Results at V_{DS} = 300V, I_D = 15A and R_G = 5Ω

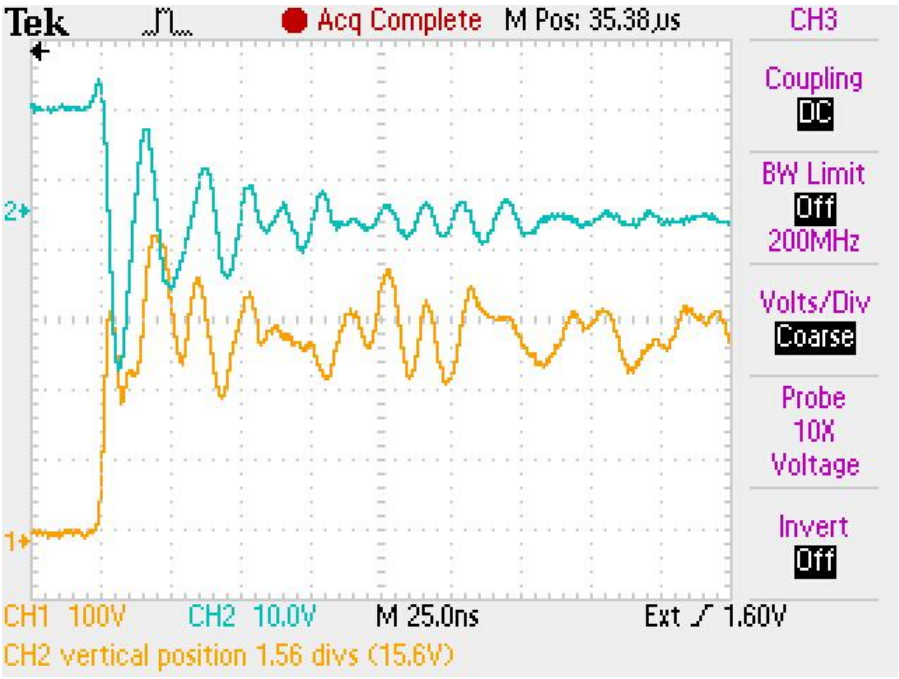

Figure 3.16: Turn OFF Switching Waveforms

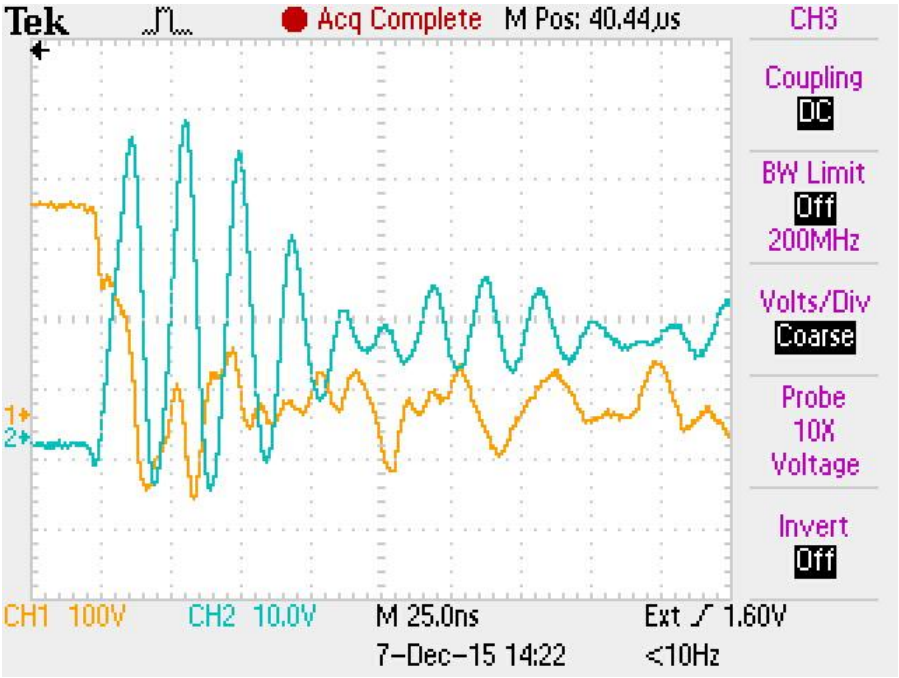

Figure 3.17: Turn ON Switching Waveforms

4. Silicon Carbide (SiC) MOSFETs Characterization

Silicon Carbide (SiC) is a compound semiconductor material which consists silicon (Si) and carbon (C). SiC semiconductors have dielectric breakdown field strength of 10x, thermal conductivity of 3x and bandgap of 3x compared to Si. SiC devices can operate at higher temperatures, have higher breakdown voltage and have low resistivity as compared to Si counterparts [7]. SiC exists in variety of polymorphic crystalline structures e.g. 6H-SiC and 4H-SiC. Currently 4H-SiC is used widely in practical power device manufacturing.
Since the dielectric breakdown field of SiC is 10 time higher than Si, the devices can be made with much thinner drift layer or high doping concentration. Therefore they have high breakdown voltage and low on resistance.

The SiC MOSFETs have low on resistance as compared to Si IGBTs. Also MOSFETs have no tail current as opposed to IGBTs. Therefore SiC MOSFETs reduce switching loss significantly at higher operating voltages enabling high frequency operation. Since these devices are operating at higher switching frequency, the filter circuit requirements are reduced making overall system less bulky. Also since it has low switching losses and SiC devices can operate at higher temperatures, the cooling system requirement is also reduced. Both of these parameters help reduce the overall system size increasing power density of the system.

The Following table shows the SiC MOSFET that was characterized.

Device manufacturer	Blocking Voltage (V)	Current (A)	ON Resistance (mΩ)	Type
Cree	1200	300	4.6	Half Bridge

Table 4.1: SiC MOSFET Parameters

4.1 Static Characterization

The On resistance of 1200V 300A SiC half bridge power module is measured using Iwatsu curve tracer. I-V characteristics are measured at -40°C, 25°C and 150°C for gate voltages from 10 V to 20 V at every 2 V. ON resistance increases with the increase in temperature. The normalized ON resistance graph is also shown below. For a given temperature, ON resistance decreases with the increase in Gate to source voltage.

Setup with kelvin contacts was used to characterize this half bridge module. One switch position in the bridge is characterized at once. The other switch was held in OFF state by shorting gate and source terminals (V_{GS} = 0).

4.1.1 Output Characteristics

Figure 4.1, 4.2 and 4.3 show I-V characteristics at 25°C, 150°C and -40°C respectively.

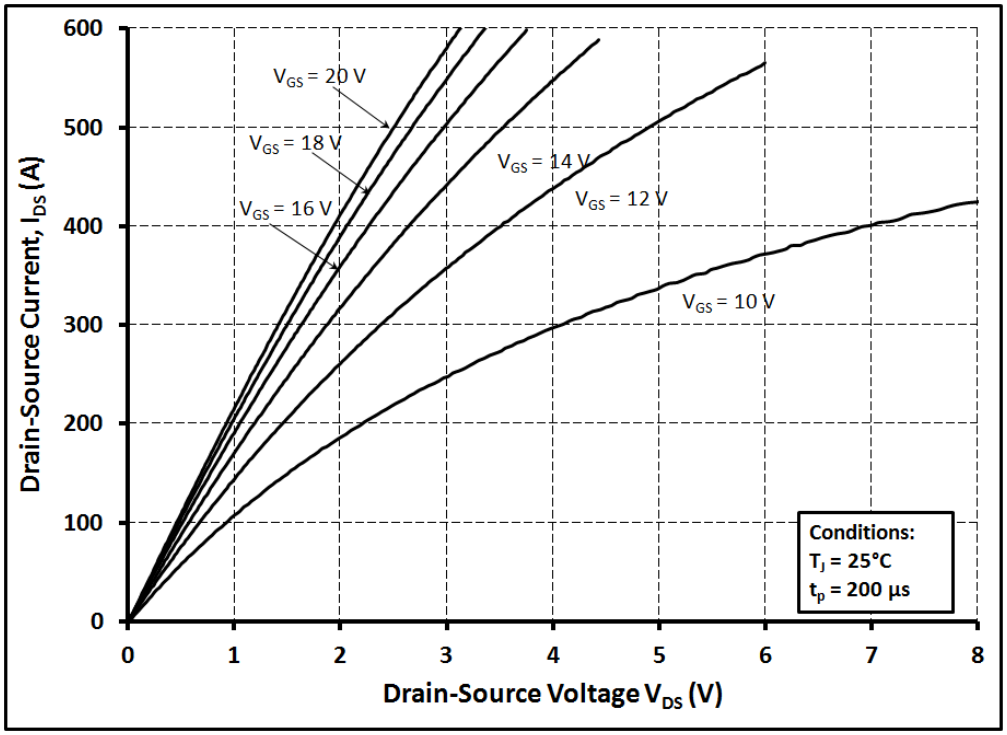

Figure 4.1: I-V Characteristics at 25°C

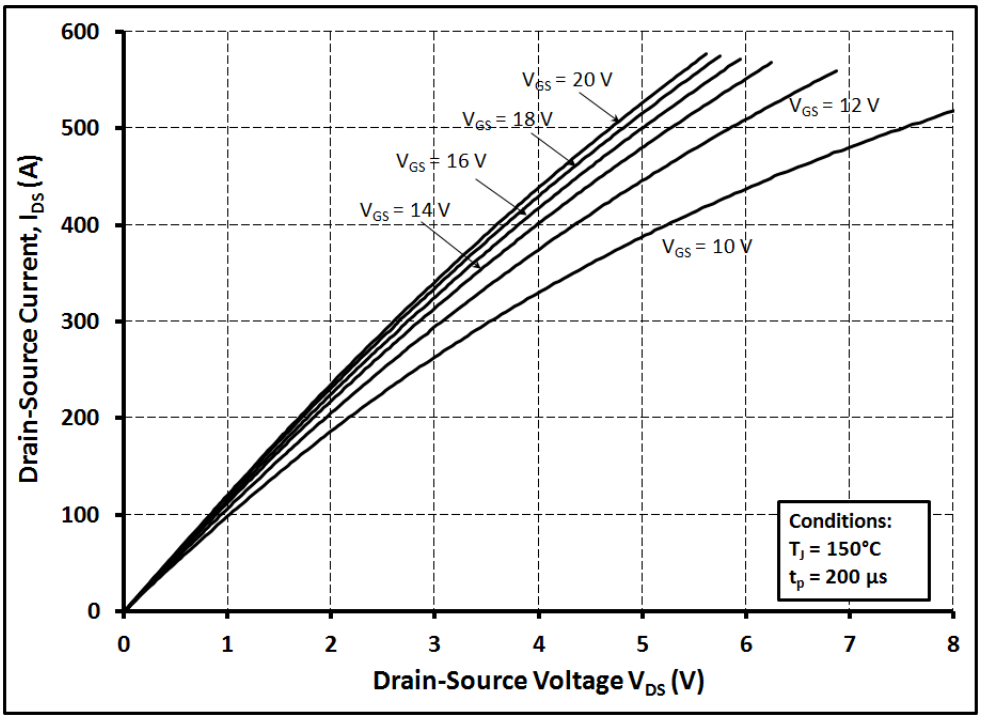

Figure 4.2: I-V Characteristics at 150°C

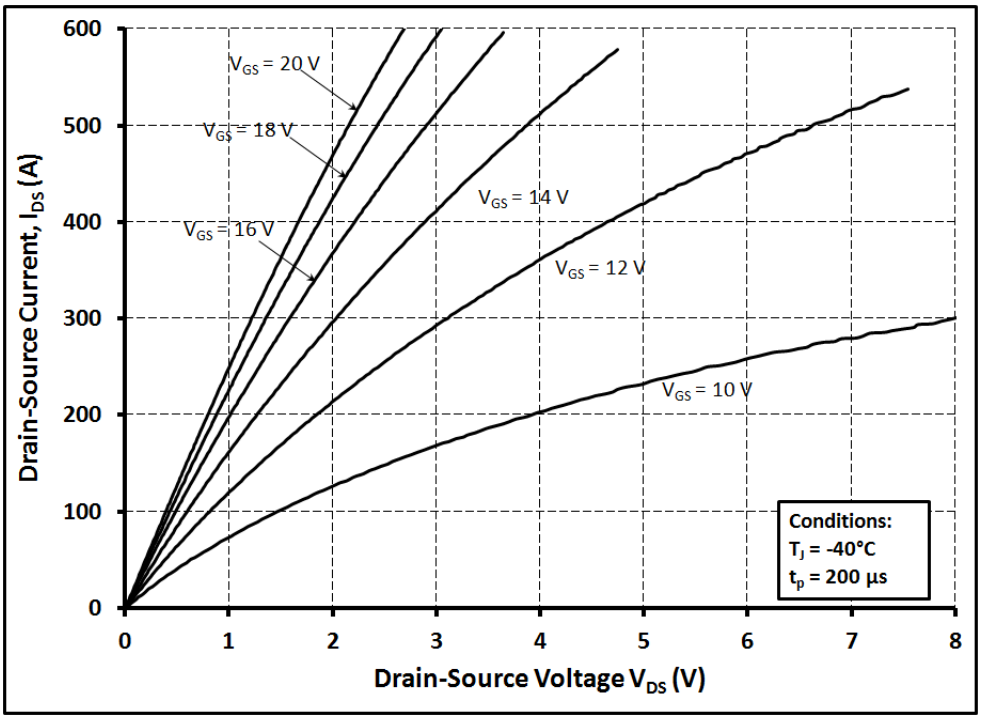

Figure 4.3: I-V Characteristics at -40°C

4.1.2 ON Resistance

The following figures show the ON resistance dependence on temperature and gate voltage.

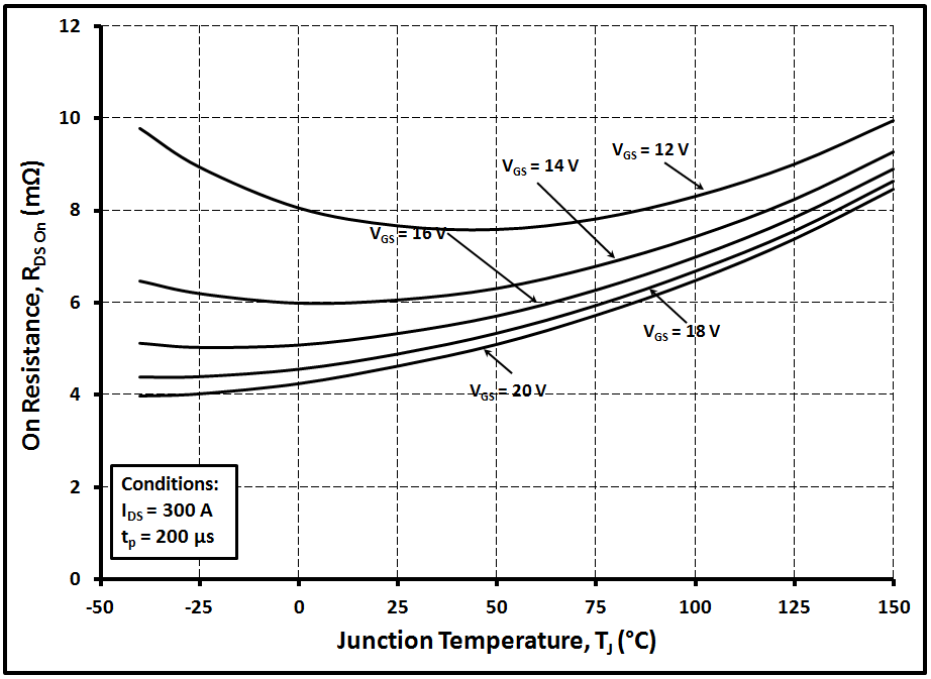

Figure 4.4: ON resistance vs. Temperature

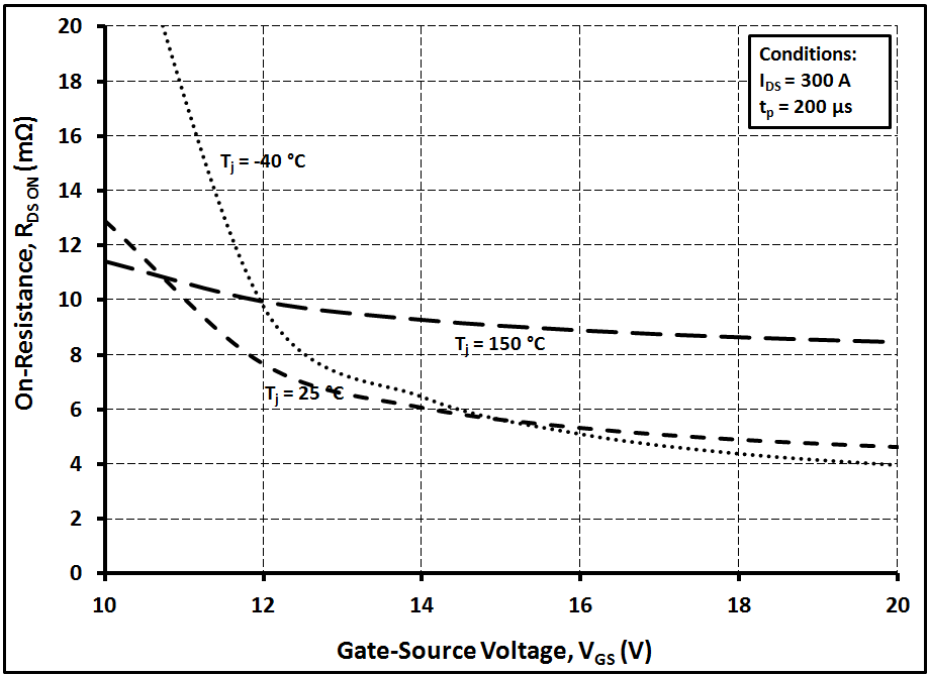

Figure 4.5: ON resistance vs. Gate to Source Voltage

4.1.3 Third Quadrant Characteristics

The following figures show the diode and third quadrant characteristics of MOSFETs.

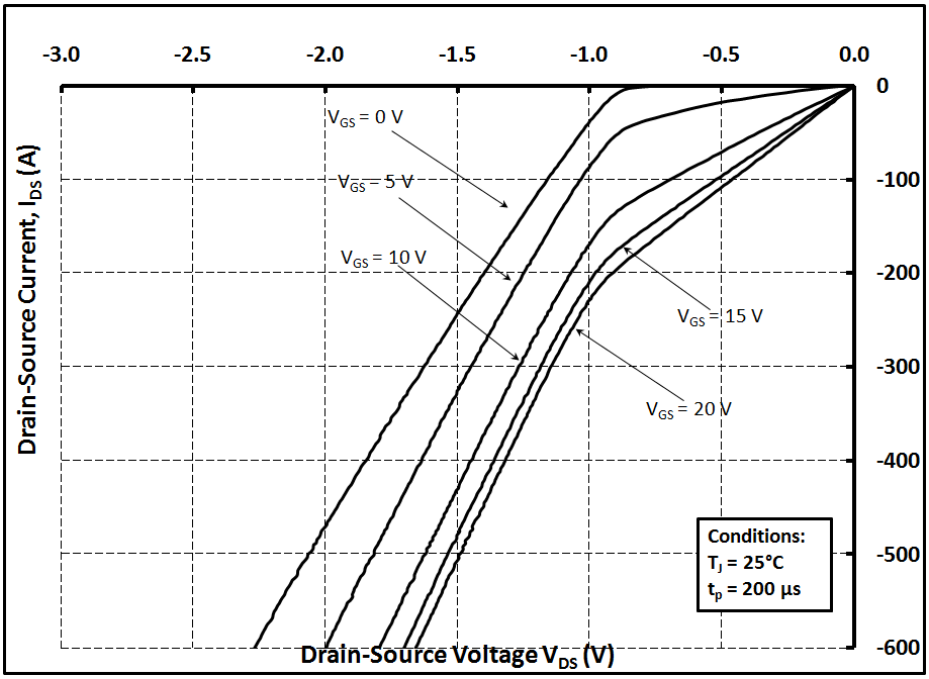

Figure 4.6: Third Quadrant Characteristics at 25°C

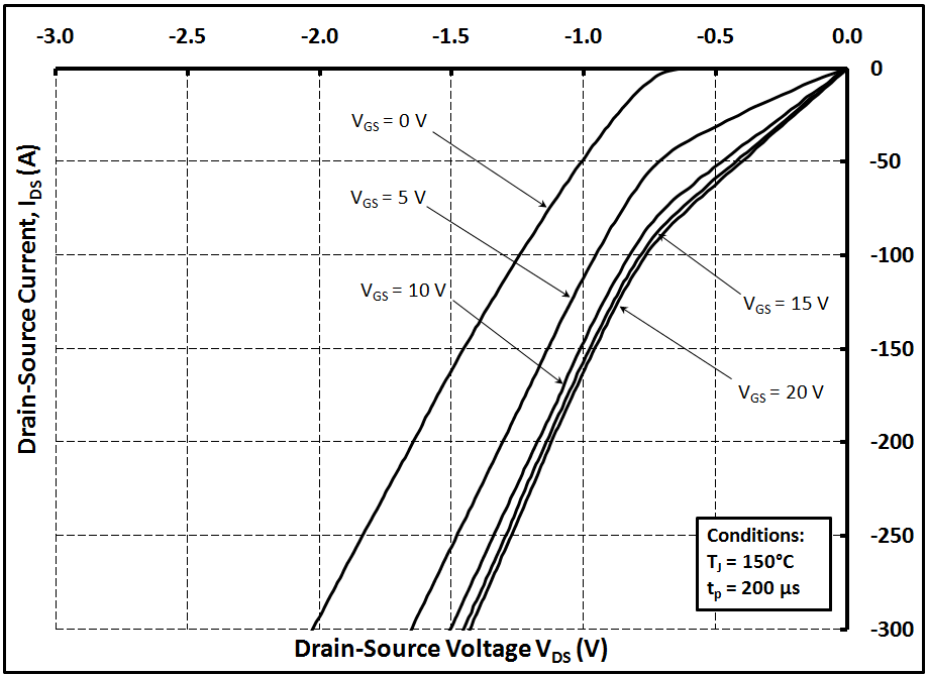

Figure 4.7: Third Quadrant Characteristics at 150°C

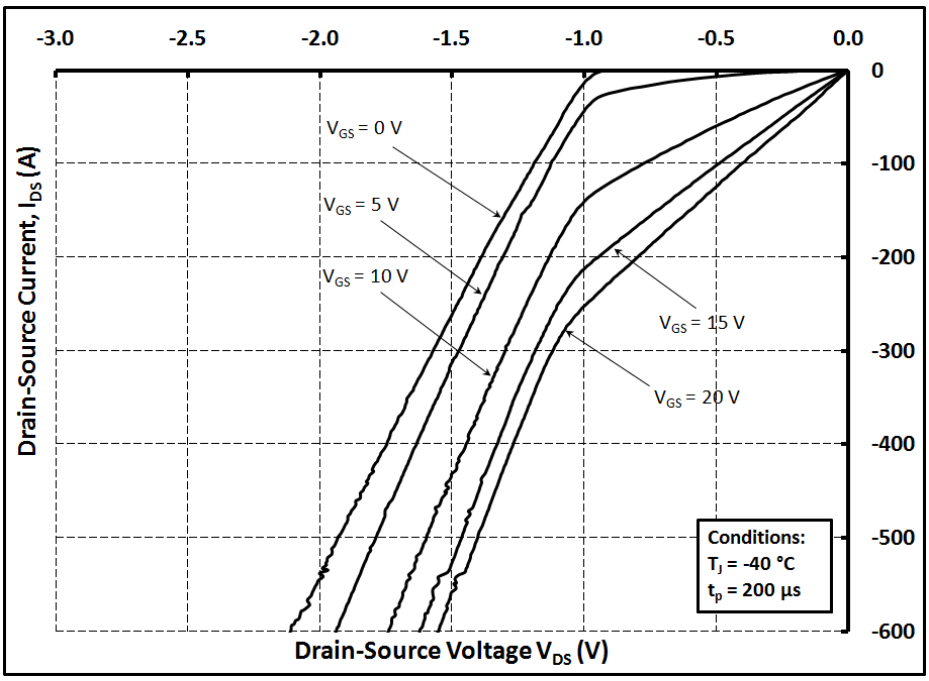

Figure 4.8: Third Quadrant Characteristics at -40°C

4.1.4 Threshold Voltage

The following figure shows the temperature dependence of the threshold voltage.

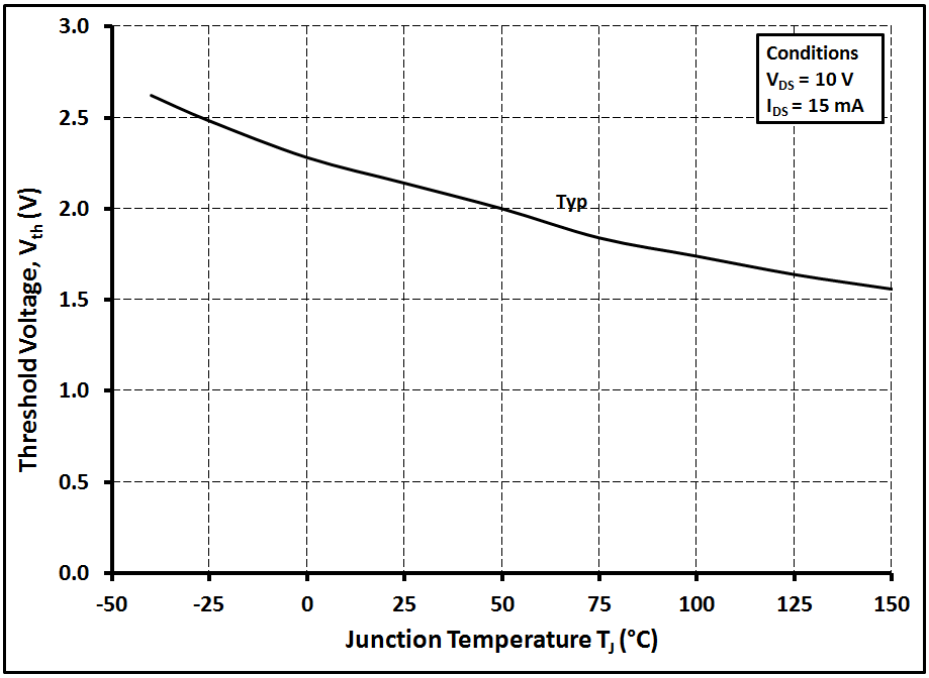

Figure 4.9: Threshold Voltage vs. Temperature

4.1.5 Transfer Characteristics

The drain voltage is kept constant at V_{DS} = 20 V by controlling the curve tracer remotely using LabView script. The drain current is measured manually at gate voltages from 0 V at every 0.5 V until the drain current reaches twice the rated value. The drain current vs. V_{GS} graph is plotted for junction temperature of -40°C, 25°C and 150°C. The nominal transconductance value is calculated at rated current.

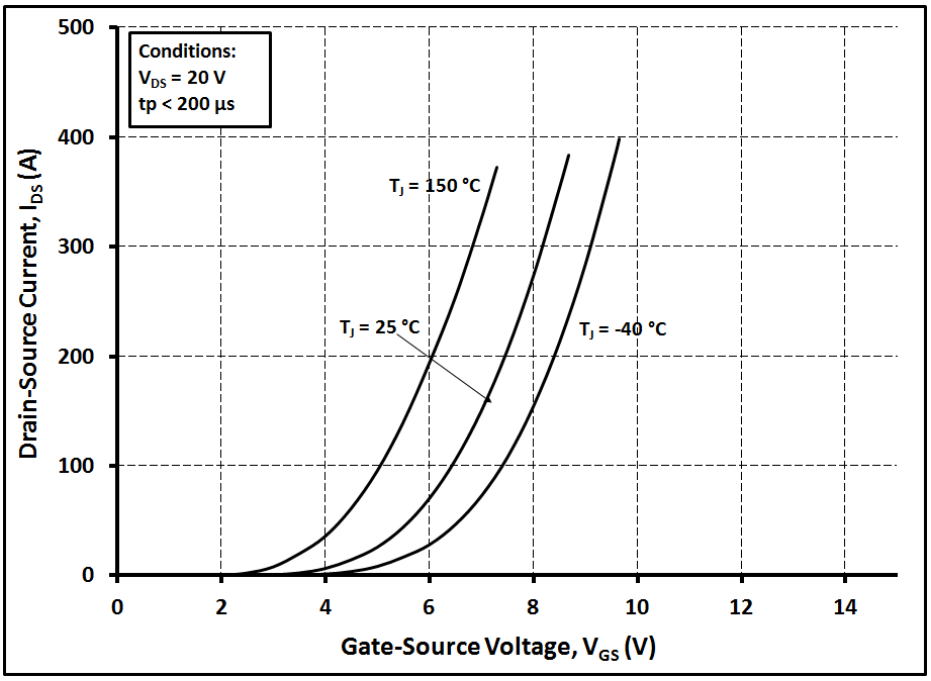

Figure 4.10: Transfer Characteristics

4.1.6 Device Capacitance Measurement

Input capacitance (C_{ISS}), output capacitance (C_{OSS}) and reverse transfer capacitance (C_{RSS}) are measured [27-28] using Agilent E4980A LCR meter. DC bias was provided using a power source. LabView script was run which controlled LCR meter and DC bias remotely and C-V curve measurement was recorded in a csv file format.

$C_{ISS} = C_{GS} + C_{GD}$, $C_{OSS} = C_{DS} + C_{GD}$, $C_{RSS} = C_{GD}$

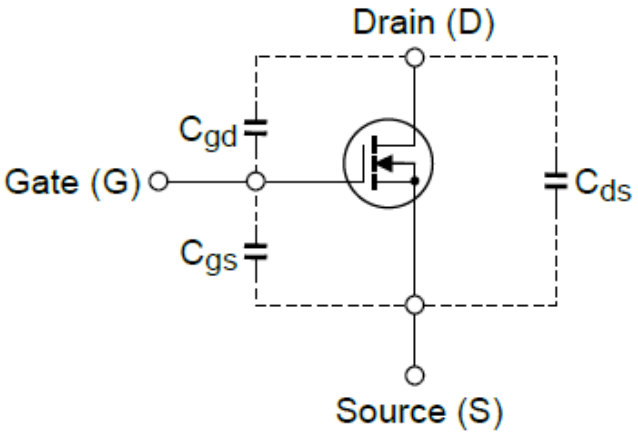

Figure 4.11: Device Capacitance Schematic

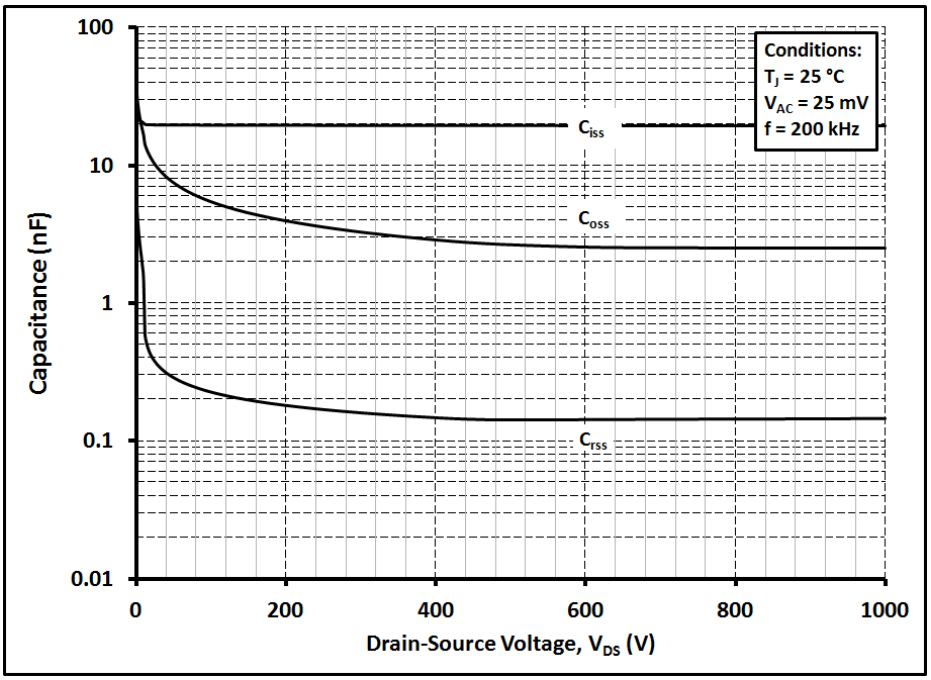

Figure 4.12: Device Capacitance Waveforms

4.2 Switching Characteristics

4.2.1 Clamped Inductive Test

The double pulse test setup was used for switching characterization of Cree half bridge module. 9 Pulses were given instead of two to go up to 1.5 times the rated current. Because of the 9 pulses, the energy losses were calculated at 8 different current levels providing switching loss dependence on the load current. The csv file was extracted from the oscilloscope which was post processed using MATLAB script to calculate ON and OFF switching energy losses and switching time. Also de-skewing of probes is very important to obtain correct energy losses. During the testing, it was observed that the overall switching losses remain almost constant but ON switching loss and OFF switching loss change drastically with the change in probe de-skewing. The switching characterization at half of the rated voltage (600V) and at 2/3rd of the rated voltage (800V). Channel 1 represents is V_{DS}, channel 2 represents I_D and channel 3 represents V_{GS}. Gate to source voltage of +20 V/ -5 V was given to gate using Cree CRD-001 gate driver.

The effect of external gate resistance on the switching energy losses and switching time is also observed. Gate drivers with external gate resistance of 2.5Ω, 5Ω, 10Ω, 20Ω and 40Ω are used to drive this module.

Since it is a half bridge module, in the double pulse test, low side switch was device under test (called DUT hereafter) and high side switch and its antiparallel diode was used for freewheeling diode in DPT setup. The high side device was kept OFF using a gate driver which provides -5V output voltage. But during a turn ON transition, the high side switch encounters a false turn ON sometimes causing shoot-through for drain current. Therefore high current ringing is observed at the turn ON transition. The switching energy losses are increased because of high current ringing.

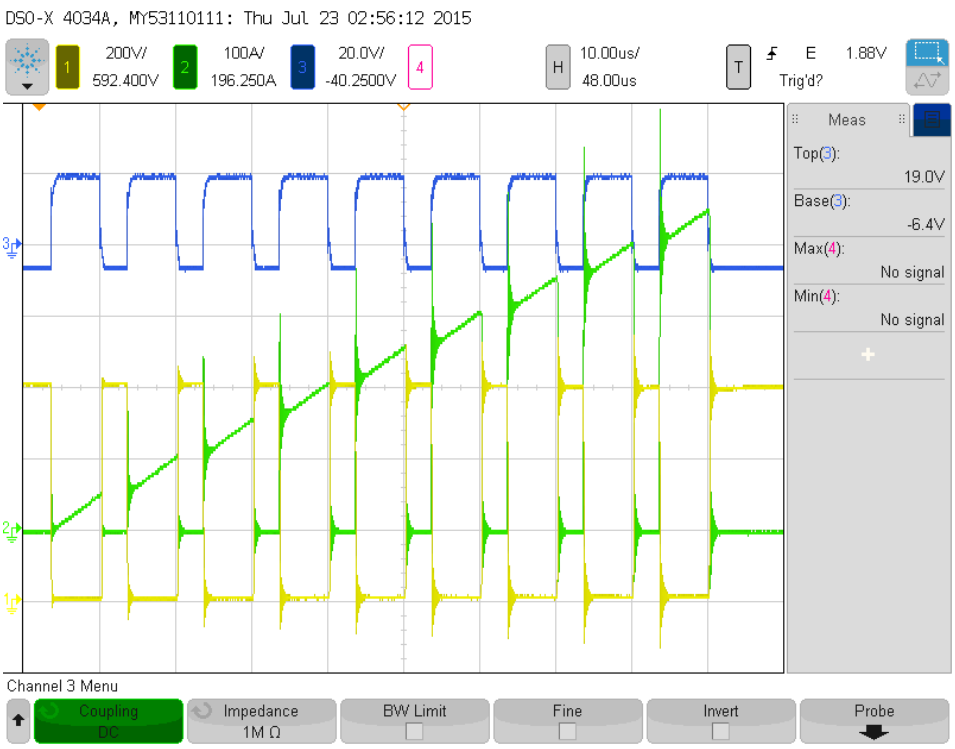

Figure 4.13: Switching Waveforms at V_{DS} = 600V

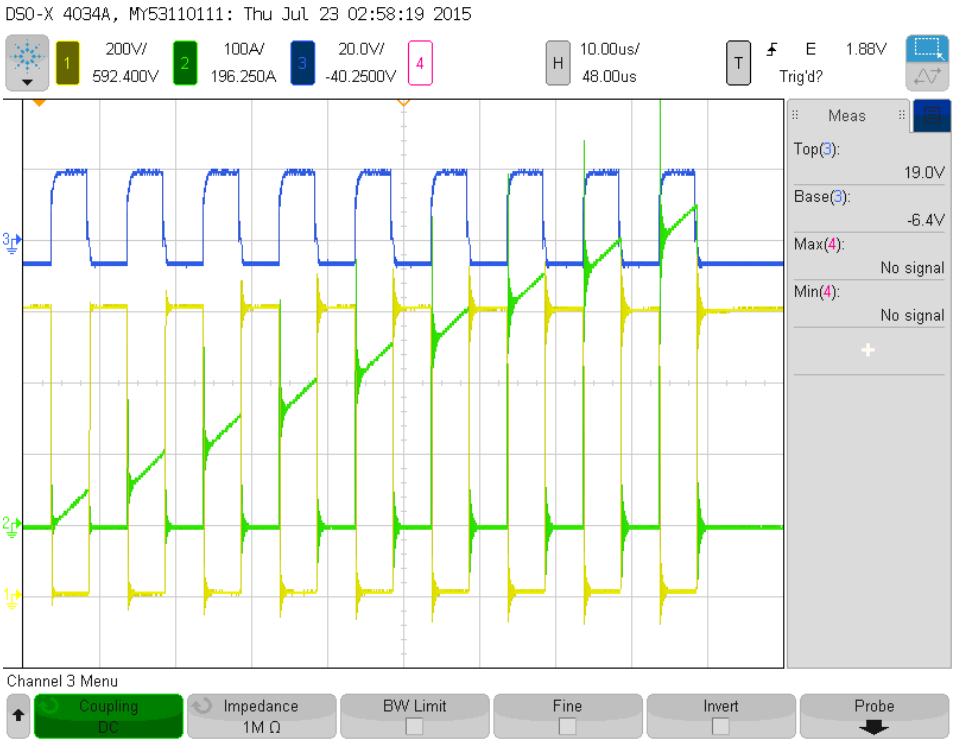

Figure 4.14: Switching Waveforms at V_{DS} = 800V

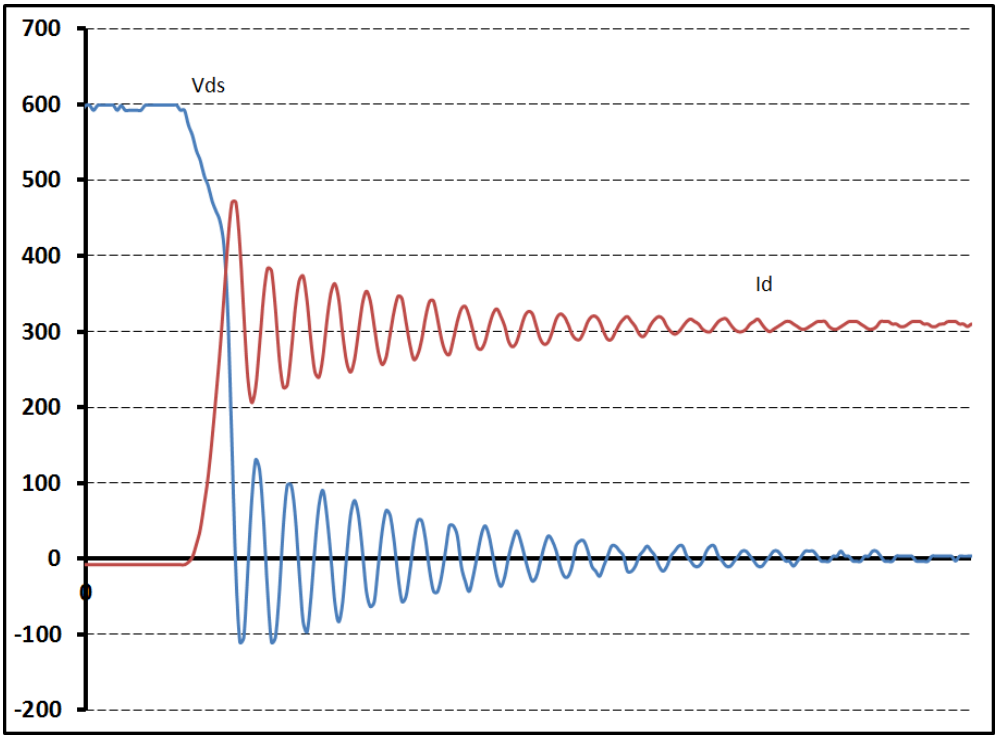

Figure 4.15: Turn ON at V_{DS} = 600V and I_D = 300A

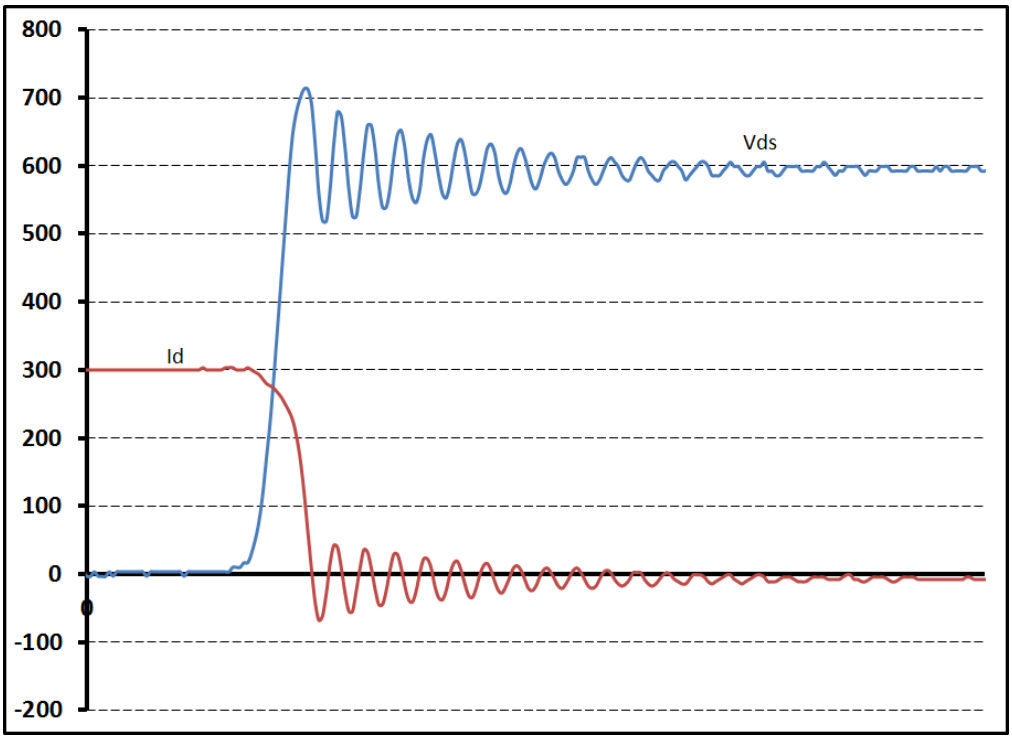

Figure 4.16: Turn OFF at V_{DS} = 600V and I_D = 300A

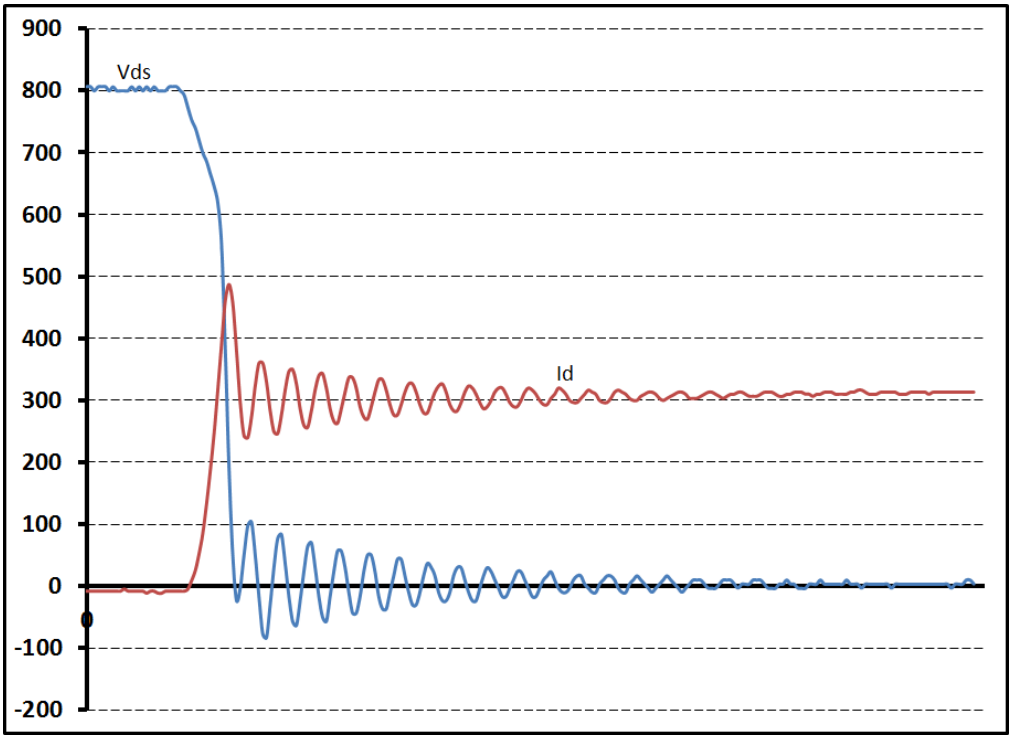

Figure 4.17: Turn ON at V_{DS} = 800V and I_D = 300A

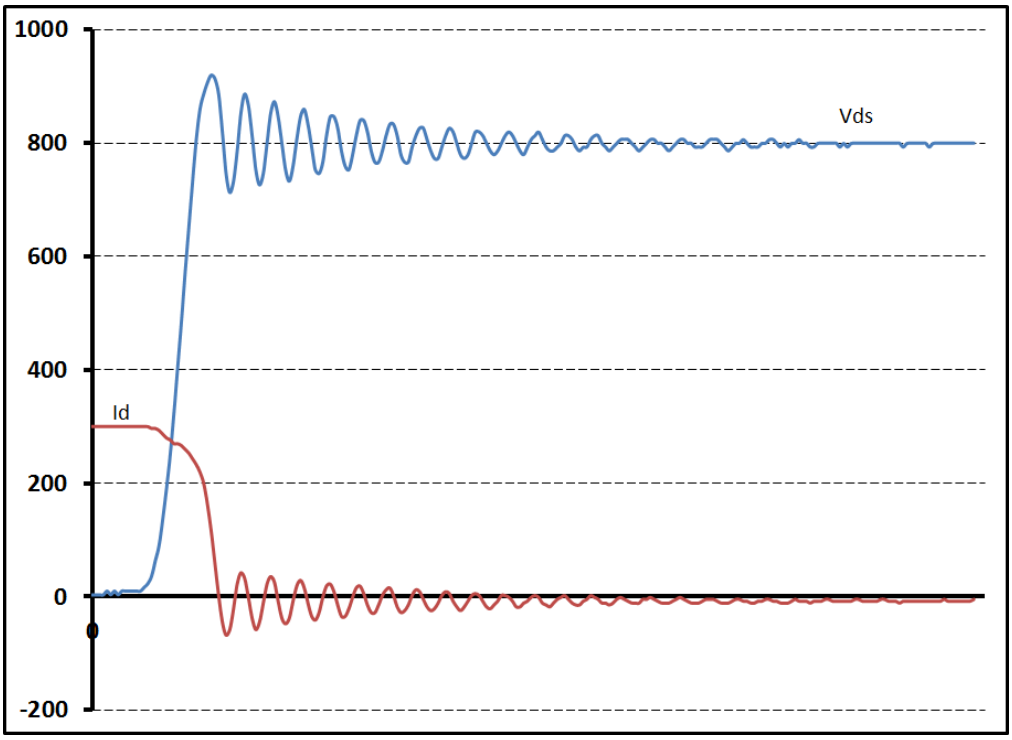

Figure 4.18: Turn OFF at V_{DS} = 800V and I_D = 300A

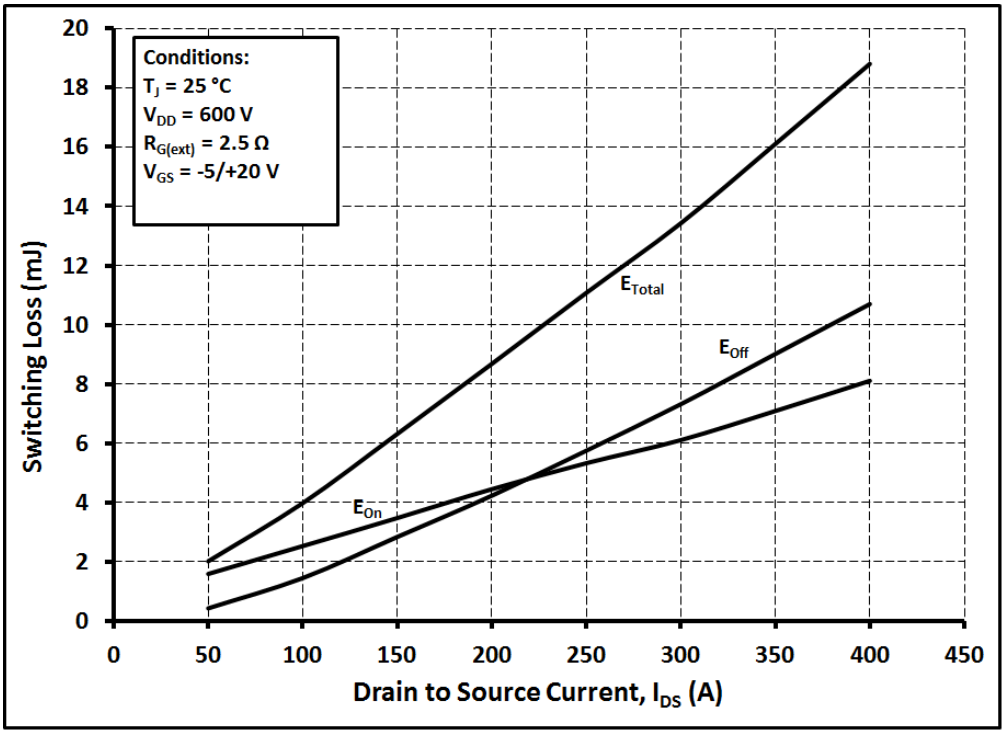

Figure 4.19: Switching Loss vs. I_D at V_{DS} = 600V

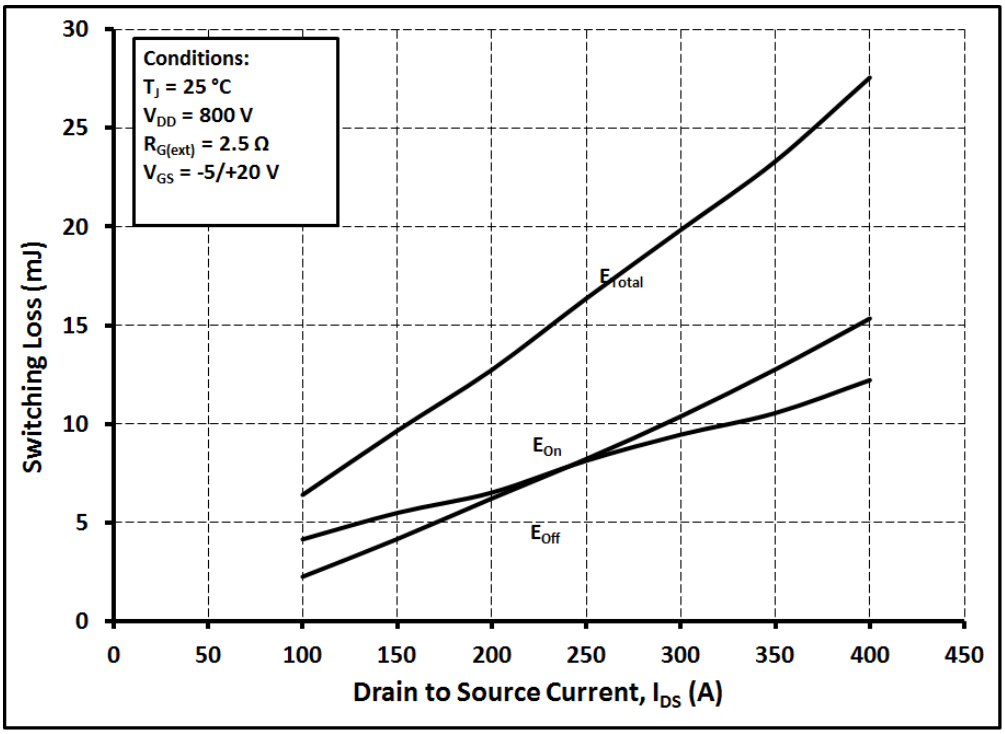

Figure 4.20: Switching Loss vs. I_D at V_{DS} = 800V

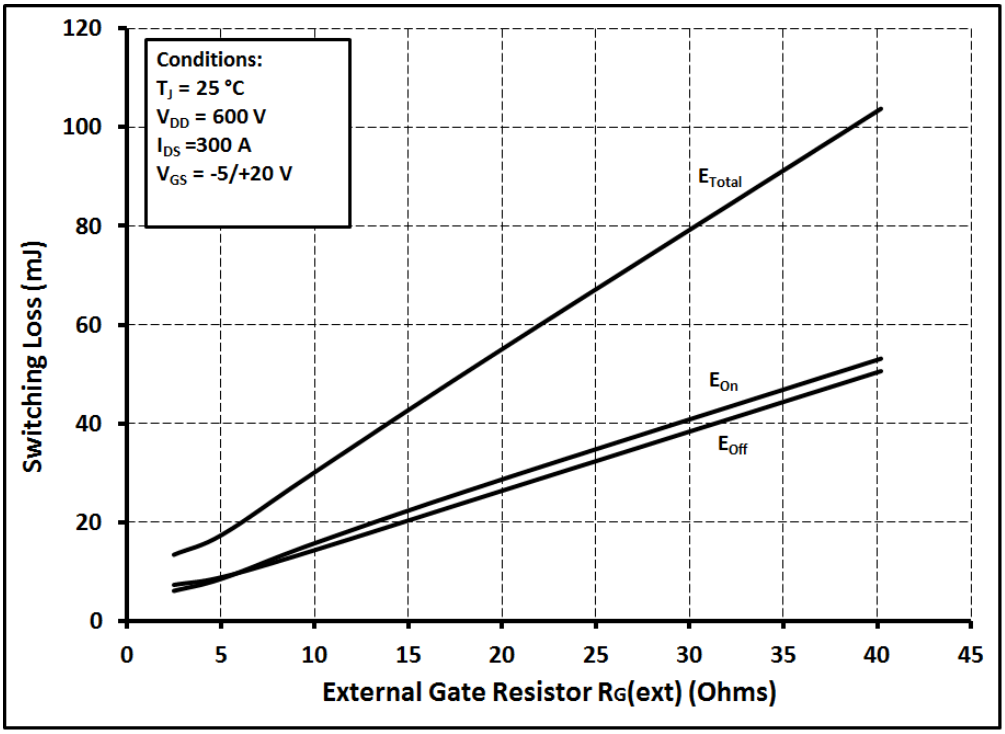

Figure 4.21: Switching Loss vs. Gate Resistance

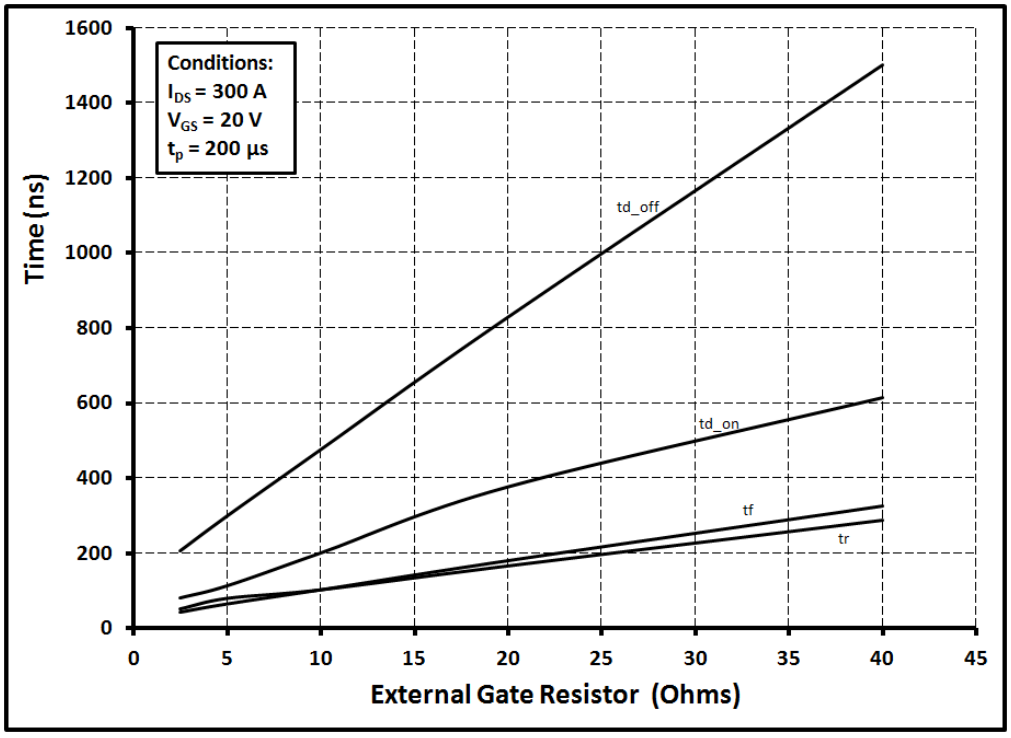

Figure 4.22: Switching Time vs. Gate Resistance

4.2.2 Gate Charge Measurement

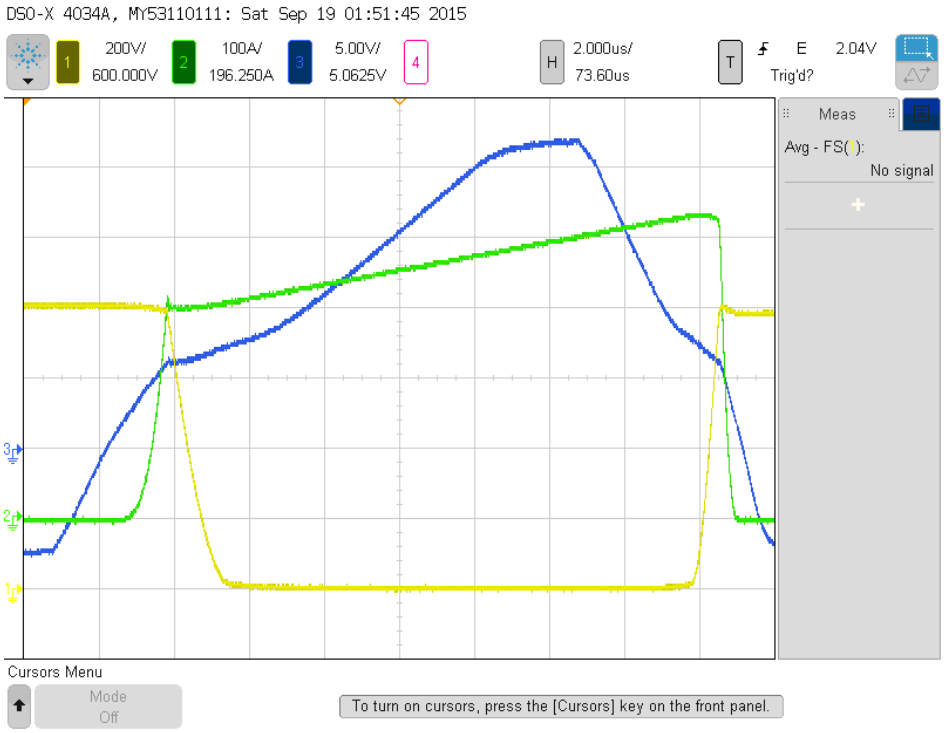

Figure 4.23: Gate Charge Waveforms at V_{DS} = 800V and I_D = 300A

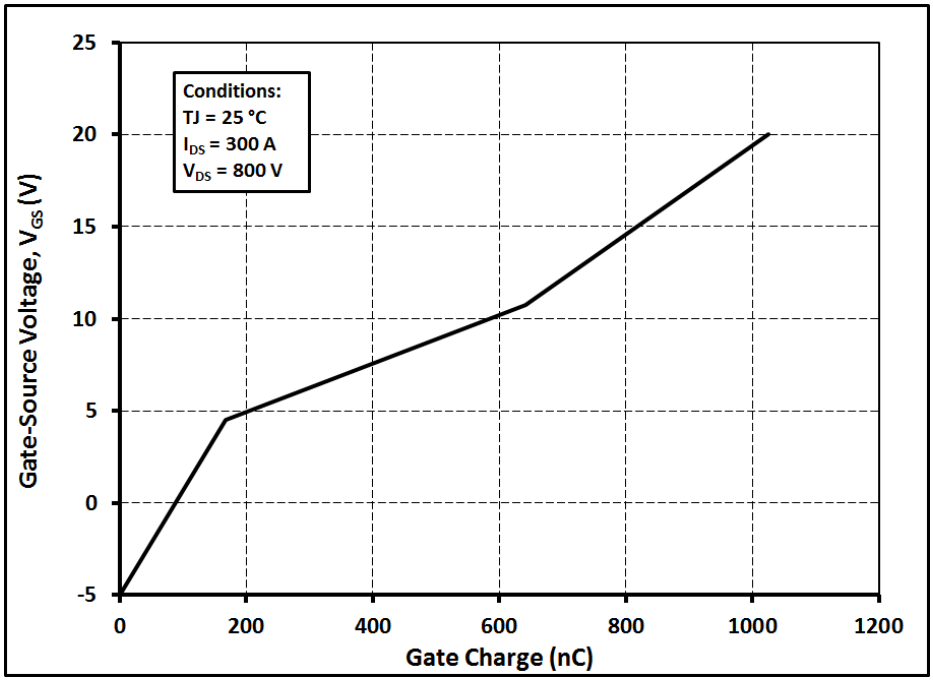

Figure 4.24: Gate Charge at V_{DS} = 800V and I_D = 300A

5. GaN vs. Si vs. SiC

In the previous chapters, the GaN HEMTs and SiC MOSFETs were characterized and their results are discussed separately. These characterization results are compared with Infineon 600V CoolMOS MOSFET.

Parameter	Unit	GaN (650V, 30A)	Si (650V. 30A)	SiC (1200V, 300A)
ON resistance	mΩ	50	120	5
Input capacitance	nF	0.18	2.1	18
Output capacitance	nF	0.07	0.125	2.5
Gate charge	nC	6.5	96	1025
Reverse recovery charge	µC	0	10	3.2

Table 5.1: GaN vs. Si vs. SiC Parameters

For the similar specifications, GaN has lower ON resistance than Si CoolMOS. The low on resistance reduces the conduction losses. The ON resistance of CoolMOS can be reduced by using several transistors in parallel. But paralleling the transistors also increase the overall device capacitance. The increase in capacitance causes increase in frequency dependent switching losses and limits the high frequency operation. The device capacitance of GaN is very low, enabling GaN to operate at higher frequencies at a reduced switching loss. For given R_{DSON}, GaN has a very low output charge, gate charge and reverse recovery charge as compared to Si CoolMOS as shown in above table. The low output charge enables fast turn ON and high dV/dt. It also plays an important role in reducing the dead-time. Negligible reverse recovery charge provides with the higher frequency limits.

SiC MOSFETs are designed for high power applications. For the high power applications, the switching frequency is lower than that for low power applications. The switching frequency for high power applications is 100-200 kHz. The low ON resistance reduces conduction losses significantly and SiC MOSFET does not have tail current as observed in Si IGBTs which

reduces turn OFF switching loss in MOSFETs. Also low reverse recovery charge in SiC MOSFETs allows operation at higher frequency than Si IGBTs.

For low power applications, GaN HEMTs are preferred over Si CoolMOS because of high frequency operation, low ON resistance, low capacitance and low gate charge. The high switching frequency allows reduction of filtering circuit. Low gate charge and capacitance allows high switching frequency operations and simplification of gate driver design since a low current is needed to charge the gate to turn ON the device. Low capacitance also gives high dV/dt which reduces switching losses. The cooling system requirements are reduced because of the low switching and conduction losses. The GaN HEMTs are around 10 times smaller than their Si counterparts which reduces the overall system size and increases the power density.

The converter topologies, magnetics, control and operating frequency need to be considered when using GaN transistors over Si CoolMOS. GaN benefits may not be completely realized if it is replaced for Si CoolMOS in the existing converter topologies.

The bridgeless totem-pole PFC converter with GaN is preferred over traditional PFC converter. In the traditional PFC converter, if Si is replaced with GaN, only advantage is reduction in conduction loss. The effect on the efficiency is negligible because of the significantly large diode drops in the bridge rectifier. Therefore, in the new totem-pole topology, there is no ridge rectifier which takes more advantage of GaN transistors' benefits and offer higher efficiency [4].

SiC MOSFETs are designed for high power operation. It has low conduction losses and low switching losses as discussed in chapter 4. SiC MOSFETs are also small in size as compared to their Si counterparts. The SiC MOSFETs can operate at higher frequencies than Si IGBTs and reduce switching and conduction losses increasing the efficiency of the system. SiC devices fit very well in the existing high power applications. Because of these advantages of SiC, it is preferred over Si IGBTs for high power applications.

6. Conclusion and Future Work

6.1 Conclusion

This thesis proposes, the characterization procedures for power semiconductor devices and precautions that need to be taken to obtain accurate results for wide band gap semiconductor devices. The static and switching characterization procedures are discussed in depth and several GaN HEMTs and SiC MOSFET are characterized. The data acquired is compared with the existing commercial power devices to discuss the superiority of wide band gap devices over existing transistors.

The ON resistance, device capacitances, gate charge and, switching energy losses and switching time are characterized. All of these parameters are superior for GaN and SiC when compared it with Si transistors which makes GaN and SiC superior than Si transistors. The potential applications are also discussed for both GaN and SiC transistors.

6.2 Future Work

The future work includes the characterization of wide band gap devices from various manufacturers to compare the static and switching parameters. The thermal characterization of GaN and SiC transistors to evaluate safe operation area and, current and power derating.
It also includes design of DC-DC converter systems which can take the most advantage of these transistors based on the characterized parameters.

References

[1] Bernet, Steffen. "Recent developments of high power converters for industry and traction applications." *Power Electronics, IEEE Transactions on* 15.6 (2000): 1102-1117.

[2] Chen, Zheng. "Characterization and modeling of high-switching-speed behavior of SiC active devices." (2009).

[3] Efficient Power Conversion, “Technical characteristics of GaN and SiC.”

[4] International Rectifier. “How 600 V GaN Transistors Improve Power Supply Efficiency and Density.”

[5] Digikey, “Gallium Nitride (GaN) versus Silicon Carbide (SiC) In the High Frequency (RF) and Power Switching Applications.”

[6] Semi-Engineering, “what happened to GaN and SiC.”

[7] Lidow, Alex, et al. *GaN transistors for efficient power conversion*. John Wiley & Sons, 2014.

[8] Tektronix, *371A Programmable High Power Curve Tracer User Manual*.

[9] International Rectifier, “Power MOSFET Basics.”

[10] Cui, Yutian, et al. "Characterization and modeling of silicon carbide power devices and paralleling operation." *Industrial Electronics (ISIE), 2012 IEEE International Symposium on*. IEEE, 2012.

[11] Chen, Zheng, et al. "Characterization and modeling of 1.2 kv, 20 A SiC MOSFETs." *Energy Conversion Congress and Exposition, 2009. ECCE 2009. IEEE*. IEEE, 2009.

[12] Fairchild Semiconductor, “Power MOSFET avalanche guideline”, *Application Note AN-9034*.

[13] International Rectifier, “Protecting IGBTs and MOSFETs from ESD”, *Application Note AN-955*.

[14] Cree, “SiC MOSFET Double Pulse Fixture.”

[15] Baliga, Vinod, et al. "Device characterization and performance of 1200V/45A SiC JFET module." *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*. IEEE, 2013.

[16] Hazra, Swarnali, et al. "High switching performance of 1.7 kV, 50A SiC power MOSFET over Si IGBT for advanced power conversion applications." *Power Electronics Conference (IPEC-Hiroshima 2014-ECCE-ASIA), 2014 International*. IEEE, 2014.

[17] Tektronix, “ABCs of probes - primer”, *Application Note*.

[18] Cree, “CCS050M12CM2 Datasheet.”

[19] Vishay Siliconix, “Power MOSFET Basics: Understanding Gate Charge and Using it to Assess Switching Performance”, *Application Note 608.*

[20] Microsemi, “Making Use of Gate Charge Information in MOSFET and IGBT Data Sheets”, *Application Note APT-0103*.

[21] International Rectifier, “Use Gate Charge to Design the Gate Drive Circuit for Power MOSFETs and IGBTs”, *Application Note AN-944.*

[22] Kuzuhara, Masaaki, et al. "AlGaN/GaN heterojunction FETs for high-power applications." *Electronics and Communications in Japan (Part II: Electronics)* 86.12 (2003): 52-60.

[23] Efficient Power Conversion, “Gallium Nitride (GaN) Technology Overview”, *White Paper WP001*.

[24] GaN Systems, “PCB thermal design guide for GaN enhancement mode power transistors.”

[25] Cree, “Design Considerations for Designing with Cree SiC Modules Part 1. Understanding the Effects of Parasitic Inductance.”

[26] Cree, “Design Considerations for Designing with Cree SiC Modules Part 2. Techniques for Minimizing Parasitic Inductance”

[27] Funaki, Tsuyoshi, et al. "Measuring terminal capacitance and its voltage dependency for high-voltage power devices." *Power Electronics, IEEE Transactions on* 24.6 (2009): 1486-1493.

[28] Li, Ke, Arnaud Videt, and Nadir Idir. "Multiprobe measurement method for voltage-dependent capacitances of power semiconductor devices in high voltage." *Power Electronics, IEEE Transactions on* 28.11 (2013): 5414-5422.