ABSTRACT

KUVAR, ABHIJIT. A Novel PWM Technique for Improved Total Harmonic Distortion of Cascaded H-bridge Converters. (Under the direction of Dr. Subhashish Bhattacharya).

Cascaded H-bridge topology is used as a multilevel inverter popularly in AC drives. Pulse Width Modulation control is typically used to control output AC voltage. This thesis aims to modify the conventionally used Pulse Width Modulation techniques in order to reduce the Total Harmonic Distortion at the output of the cascaded H-bridge. Conventional methods were interpreted through Space Vector Modulation and they were modified accordingly.

The results were obtained using MATLAB/Simulink and PLECS Blockset and tested for different values of indices and scenarios.

A Novel PWM Technique for Improved Total Harmonic Distortion of Cascaded H-bridge Converters

by
Abhijit Kuvar

A thesis submitted to the Graduate Faculty of
North Carolina State University
in partial fulfillment of the
requirements for the Degree of
Master of Science

Electrical Engineering

Raleigh, North Carolina

2015

APPROVED BY:

_____	_____
Dr. Subhashish Bhattacharya Committee Chair	Dr. Mesut Baran

_____
Dr. David Lubkeman

DEDICATION

To my parents, Murlidhar Kuvar and Shaila Kuvar and my brother, Abhishek for their unwavering support throughout my career.

BIOGRAPHY

Abhijit Kuvar, was born in Pune, India. He completed his schooling from G.E.I's High School and Birla College from Kalyan, India where he was brought up. He received his Bachelor's Degree in Electrical Engineering from Veermata Jijabai Technological Institute, Mumbai in 2012. He is currently pursuing Master of Science in Electrical Engineering from North Carolina State University. He has been working at FREEDM Systems Center as a Graduate Research Assistant. His research is focused on Control of Power Converters, Solid State Transformers and Analog Electronics.

Abhijit interned at Crompton Greaves, Mumbai working on HV transformer testing. He worked with Joby Motors, LLC in Santa Cruz, CA on PMSM motor control hardware. He also interned with Analog Devices Inc. in Greensboro, NC for designing power supply with cascaded H-bridge topology. He plans to continue working with Analog Devices Inc. in future as a Product Engineer in their Energy Metering Integrated Circuit team located at Wilmington, MA.

ACKNOWLEDGMENTS

I express my deepest gratitude towards Dr. Subhashish Bhattacharya for helping me in my academic career and for providing opportunities to develop my engineering skills in my field of interest. I would like to thank Dr. Mesut Baran and Dr. David Lubkeman for being effective instructors in the classroom and for providing insights in my research. Special acknowledgement to Jim Camp, my mentor at Analog Devices for proving me opportunity to work on cascaded H-bridge module. I am thankful to researchers with whom I have worked at FREEDM Systems Center; Vivek, Urvir, Samir and all others.

I am particularly thankful to my friends at NC State; Sandesh, Priyanka, Aniket, Omkar, Ankit, Revant and others for being wonderful companions. I owe a lot of gratitude to my close friends who have stuck with me through thick and thin; Chetan, Anil, Srikrishnan, Juili, Shruti and many others for always being there for me.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

1. Introduction

Multi-level inverters are used to synthesize a desired single-phase or three-phase voltage waveform. The required multi-staircase resembling output voltage is obtained by combination of several DC sources. Multi-level inverters have specific arrangement of switches and capacitor voltage sources. Multiple topologies exist for multi-level inverter – following of which are one of the important topologies [1]:

(a) Diode Clamped (Neutral Point Clamped having DC-link capacitors)

(b) Capacitor-clamped (DC-link capacitors)

(c) Cascaded H-bridge (Isolated DC supplies with individual DC-link capacitor)

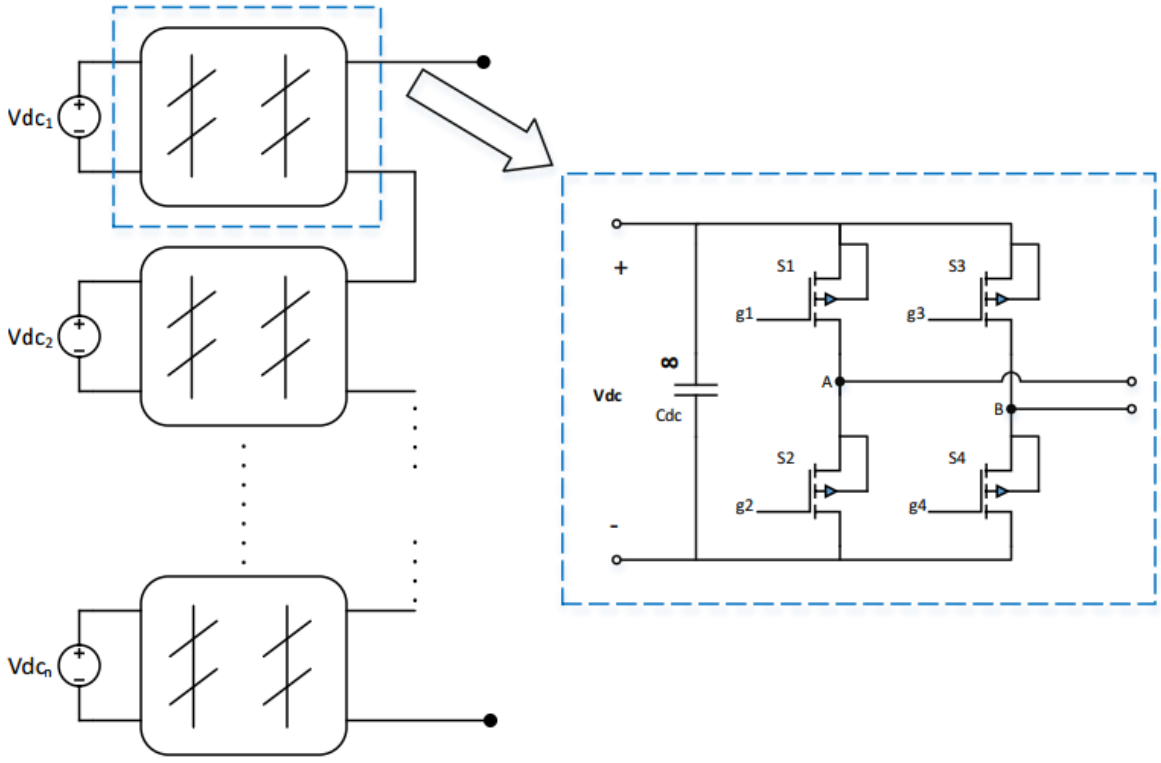

Figure 1.1 General Schematic of Cascaded H-bridge Multilevel Inverter

This thesis focuses on the Cascaded H-bridge topology of the multi-level inverter which is one of the popular converter topologies used in high-power medium-voltage (MV) drives [2]. It is constructed of multiple units of single-phase H-bridge powered by single DC-source as shown in figure 1.1. Cascaded H-bridge structure is a modular structure of DC-AC power conversion because of usability of sophisticated PWM strategies, reduced energy consumption and elimination of lower order voltage harmonics from the output. Most of the applications of cascaded H-bridge topology involve reactive power compensation application, photovoltaic power conversion (PV panels used as individual DC sources), uninterruptible power supplies and for magnetic resonance imaging [3].

The topological structure of an ideal cascaded H-bridge multi-level inverter, as shown in figure 1.1 above, requires a number of isolated dc supplies viz. Vdc_1, Vdc_2 ,…, Vdc_n for n number of H-bridges connected. Single module of H-bridge has 4 switches each with each two switches forming one leg. The switching action of S1-S4 produces different voltage levels at the output about which there is detailed discussion in chapter 2. Cascaded structure of topology makes a series connection of the individual voltage outputs of single H-bridges thus synthesizing the required AC output.

Increasing the number of H-bridge modules in cascaded H-bridge makes the AC output increase in smaller increments, naturally reducing the Total Harmonic Distortion (THD) at the output. For increasing the number of H-bridge modules, more number of switches are required which constitutes to increase in voltage stresses and increase in switching losses. Gating pulses for cascaded H-bridge topology are generated by variety of Pulse

Width Modulation (PWM) techniques. Chapter 3 describes the process of generation of gating pulses for the single H-bridge at its implementation using MATLAB function. Thereafter, chapter 4 draws focus on basics of Fast Fourier Transform (FFT) of sample harmonic spectrum of the voltage output and highlights the components of the output spectrum that affect the THD of the output.

For the purpose of analysis, 4-cell and 6-cell cascaded H-bridges are taken into consideration. Chapter 4 discusses about the common PWM techniques and their comparisons in terms of change in THD at the output. Generation of PWM requires a modulating wave and carrier wave. Instantaneous value of each of the aforementioned waves are compared in order to generate PWM. This thesis focuses on modification of the carrier waves so that the output voltage has lower amount of THD, thus improving the output quality. Chapter 5 discusses the basis for modification of carrier waves and their expected impact on the THD of output.

Chapter 5 also compares the voltage output quality for conventional carrier PWM techniques against the modified carrier PWM technique for different scenarios and different indices of modulation. MATLAB and PLECS simulation tools are used for the analysis of THD, generation of harmonic spectra and corresponding graphs.

2. Switching of H-Bridge and Cascaded H-Bridge

2.1 Mathematical formulation for H-bridge equations:

Essentially, H-bridge is a circuit that enables a voltage to be applied across a load in either direction. Therefore, H-bridge topology can be employed for DC-AC conversion at higher voltage and power levels. Figure 2.1 shows structure of an ideal single H-bridge.

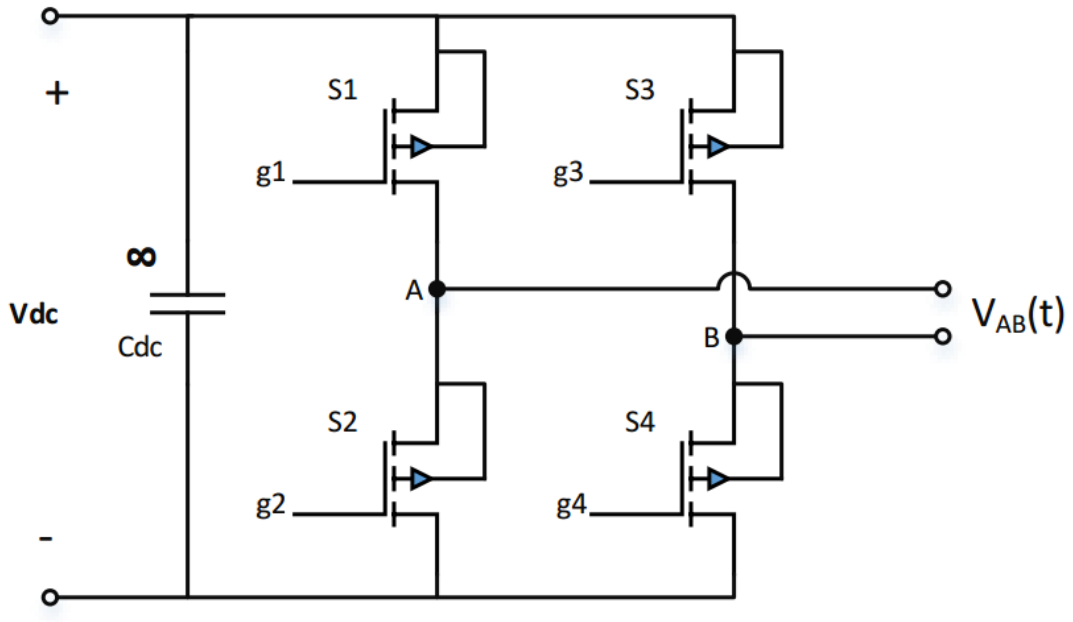

Figure 2.1 H-Bridge Circuit

H-bridge circuit is fed by a single DC source with value Vdc. For an ideal H-bridge circuit, an assumption is made that input capacitor Cdc is infinite and thus capable of holding voltage for infinite time and providing as much current as required by load. Switches S1 and S2 form one leg of H-bridge and switches S3 and S4 form the other and each of them are complementary of each other i.e. they cannot be ON simultaneously. Gating signals

to switches S1, S2, S3, S4 are g1, g2, g3, g4 respectively. Switch turns ON when corresponding gate signal is '1' or 'high'. Single H-bridge circuit is capable of providing three voltage levels: +Vdc, 0 and –Vdc as shown in figure 2.2.

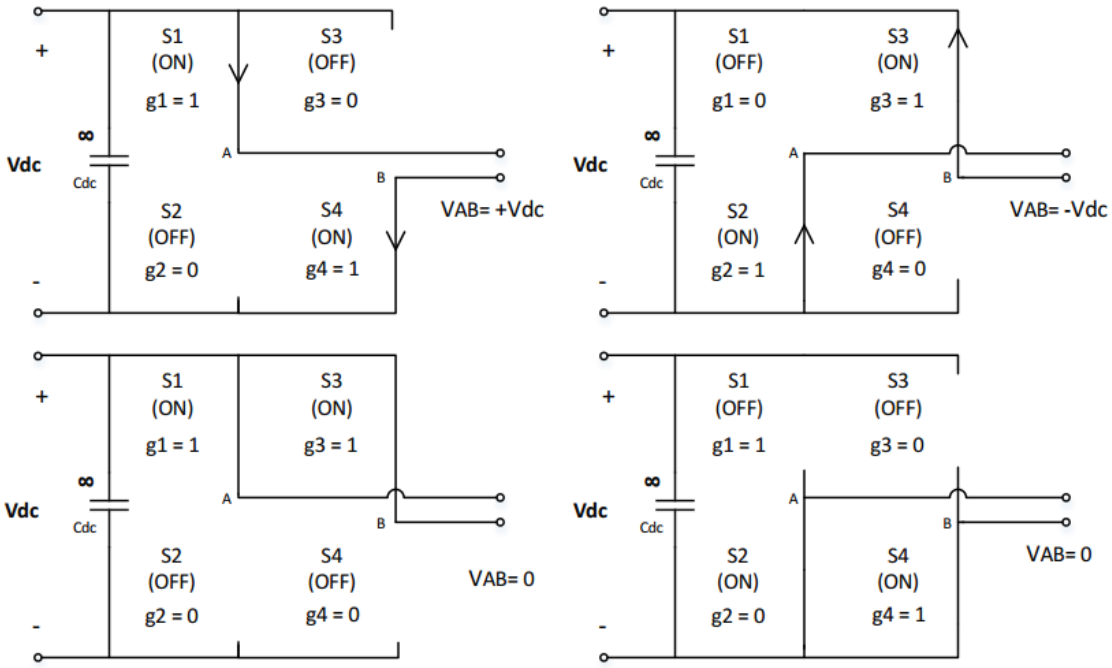

Figure 2.2 Switching states of single H-bridge

Table 2.1 Switching table for H-bridge

g1	g3	$V_{AB}(t)$
1	0	+Vdc
1	1	0
0	1	-Vdc
0	0	0

The output voltage equation for the single H-bridge can be established as from Table 2.1 above,

$$V_{AB}(t) = (g1 - g3)\, Vdc \quad (1)$$

Single cell of H-bridge is thus, capable of producing three voltage levels – Vdc, 0 and +Vdc. When cascaded H-bridges are used as shown in figure 1.1, more number of voltage levels can thus be obtained. Figure 2.3 shows the n number of H-bridge modules forming the cascaded H-bridge.

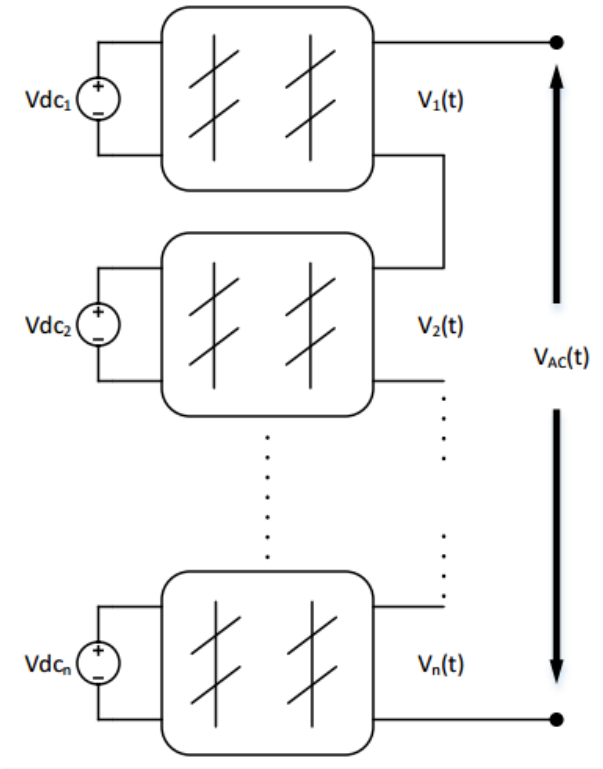

Figure 2.3 Cascaded H-bridge

$V_{AC}(t)$ is the output AC voltage resulting from series connection of individual voltage outputs of each cell of H-bridge and it can be expressed as,

$$V_{AC}(t) = V_1(t) + V_2(t) + \cdots + V_n(t) \quad (2)$$

When *n* number of H-bridge cells are connected to form a cascaded H-bridge, the voltage levels that be obtained from this are +nVdc, +(n-1)Vdc, … 0, … -(n-1)Vdc, -nVdc. Thus, if *m* indicates the number of voltage levels that can be obtained from *n* number of H-bridge modules, *m* can be expressed as

$$m = 2n + 1 \quad (3)$$

In case of cascaded H-bridge topology, *m* is always an odd number. Generalizing the statement, *n* number of H-bridge cells form m-level inverter. For all the further discussions, it is assumed that all H-bridge cells are fed by equal dc link voltage i.e. in figure 2.3,

$$Vdc_1 = Vdc_2 = \cdots = Vdc_n = Vdc \quad (4)$$

2.2 Introduction to Switching Techniques for Cascaded H-Bridge inverter:

As established, cascaded H-bridge can be switched to more number of DC voltage levels as we go on adding the individual H-bridge cells in the topology. The methods by which the output AC voltage is obtained by attaining the available DC voltage levels are various and this variation is fundamentally obtained by using different PWM techniques for generating gate pulses. The harmonic distortion in the output voltage depends on use of particular PWM technique used. All the PWM techniques discussed henceforth are sine wave modulated with triangular carriers.

PWM techniques used for cascaded H-bridge are most likely multi-carrier based because of the requirement of identifying and generating gating pulses for individual H-bridge cells. These multicarrier modulation PWM techniques differ from each other from the factors such as phase displacement of carriers and spatial arrangement of multiple carriers. Following are the common multicarrier level-shifted modulation PWM schemes that are used for cascaded H-bridge multi-level inverters [4]:

(a) In-phase disposition (IPD)

All the triangular carriers are of equal width and same modulation frequency. They are in phase with each other. Refer figure 2.4

(b) Alternative phase opposition disposition (APOD)

All the triangular carriers are of equal width and same modulation frequency. They are alternatively in phase with each other. Refer figure 2.5

(c) Phase opposition disposition (POD)

All the triangular carriers are of equal width and same modulation frequency. Half of the carriers are in phase with each other while the rest of them are in opposite phase. Refer figure 2.6

In each of the above topologies, if there are *n* number of H-bridge cells forming a cascaded H-bridge, the number of carriers required for PWM would be *2n*.

Following figures indicate the difference between level-shifted multicarrier PWM schemes indicated above. Figures assume that the cascaded H-bridge in consideration is a 5-level (from (3), 2 H-bridge cells) cascaded H-bridge.

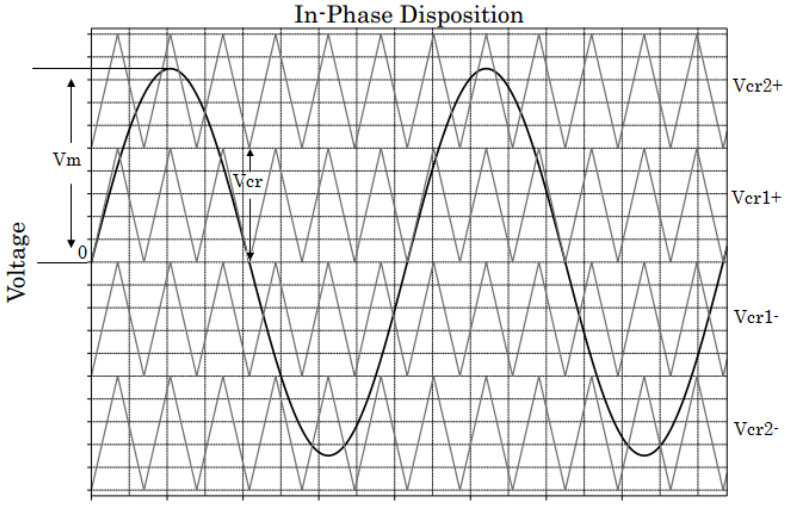

Figure 2.4 In-Phase Disposition

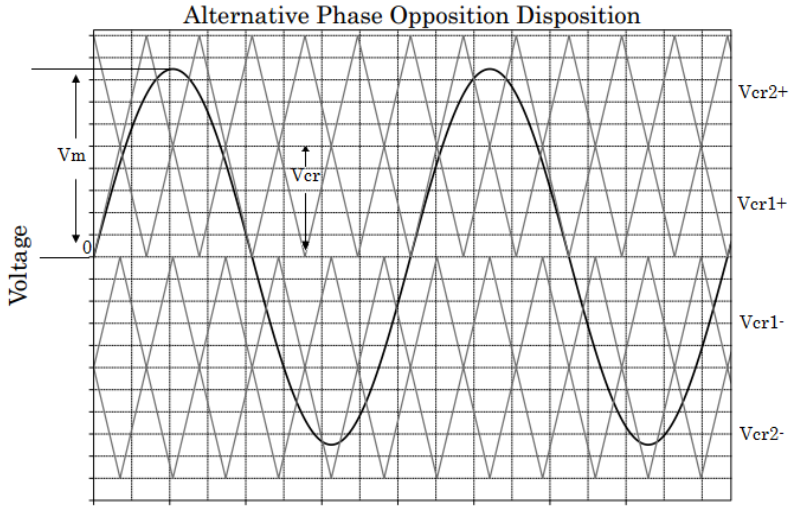

Figure 2.5 Alternative Phase Opposition Disposition

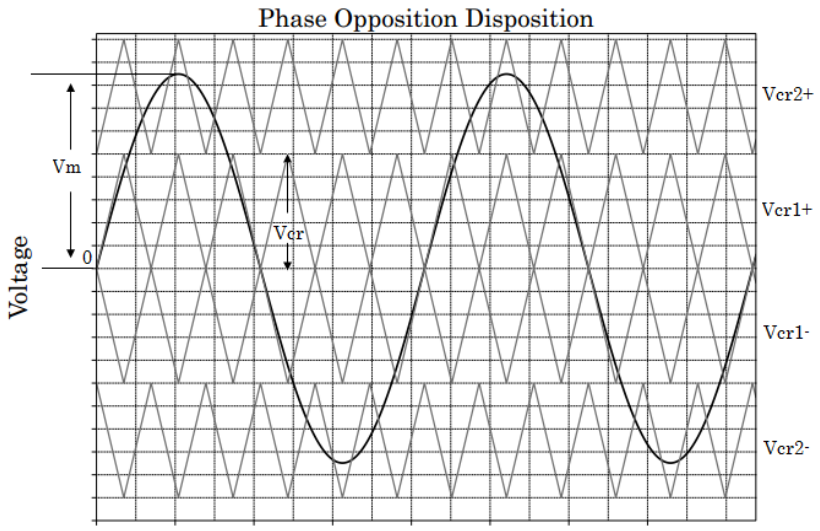

Figure 2.6 Phase Opposition Disposition

In figures 2.4-2.6, there are 4 carrier waves viz. Vcr2+, Vcr1+, Vcr1-, Vcr2- of equal peak-to-peak amplitude V_{cr} and equal frequency f_{cr}. Modulating sine wave has peak amplitude of V_m and frequency f_m. For the analysis of PWM techniques, mainly variation in M_a – Amplitude modulation index and variation in M_f – frequency modulation index is taken into consideration. These indices are defined as,

$$M_a = \frac{V_m}{nV_{cr}} \; for \; 0 \leq M_a \leq 1 \tag{5}$$

n is as defined in (3)

$$M_f = \frac{f_{cr}}{f_m} \tag{6}$$

From device performance point of view, the switching frequency is not the same for different devices in different H-bridge cells. In general, the switching frequency of the inverter using level-shifted multicarrier modulation is equal to carrier frequency i.e.

$$f_{sw,inv} = f_{cr} \tag{7}$$

From which, the average device frequency is,

$$f_{sw,dev} = \frac{f_{cr}}{(m-1)} \tag{8}$$

In addition to unequal device switching frequencies, the conduction time of the devices is not evenly distributed. For practical implementation, the switching pattern in the cells of cascaded H-bridge is rotated in order to evenly distribute the conduction times among devices. For cascaded H-bridge, devices in topmost cells conduct for lesser time than that of those at the bottom. Next chapter illustrates more about gating pulses generation logic for cascaded H-bridge.

3. Switching Logic Generation

3.1 Generalized Mathematical Formulation for n-cell Cascaded H-bridge:

For generating switching logic for cascaded H-bridge it is needed to understand how output voltage is generated from the inverter. Figure 3.1 shows generalized n-cell cascaded H-bridge with each cell fed by equal DC voltage source *Vdc*. Single H-bridge cell shown in the figure represents i^{th} cell in the hierarchy assuming the cells are numbered from top to bottom.

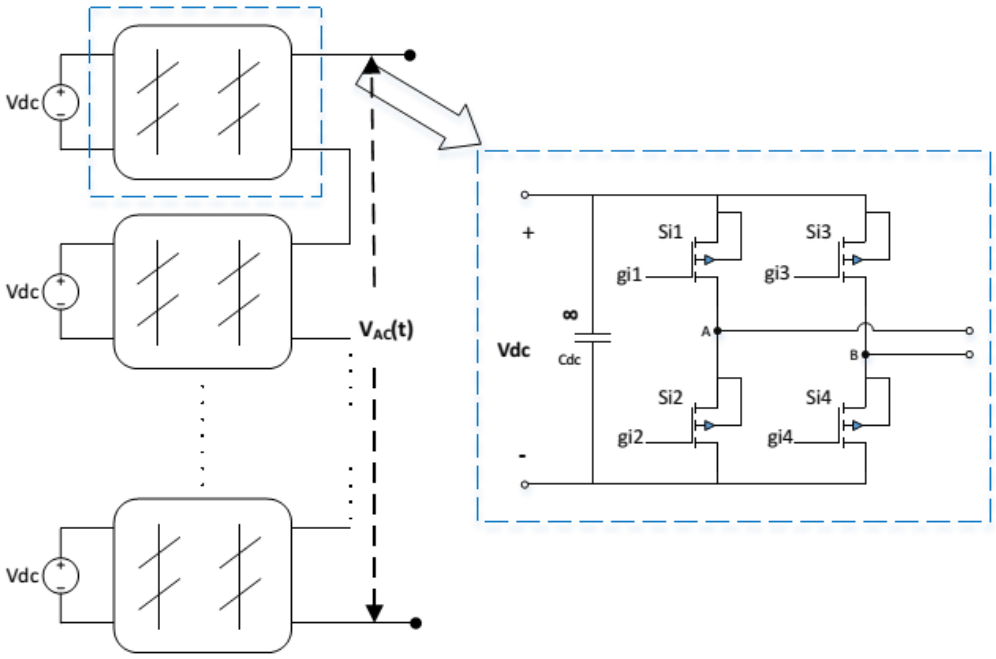

Figure 3.1 n-cell Cascaded H-bridge

Si1, Si2, Si3, Si4 represent the corresponding switches in the i^{th} H-bridge which are provided with gating signals gi1, gi2, gi3 gi4 respectively. From (1) and (2),

$$V_{AC}(t) = (g11 - g13)V_{dc} + (g21 - g23)V_{dc} + \cdots + (gn1 - gn3)V_{dc}$$

$$V_{AC}(t) = \sum_{i=1}^{n} (gi1 - gi3)\, V_{dc} \tag{9}$$

In the following discussions, considerable amount of analysis is done on 4-cell cascaded H-bridge multilevel inverter. The output voltage for 4-cell inverter can be given from (9) as,

$$V_{AC}(t) = [(g11 - g13) + (g21 - g23) + (g31 - g33) + (g41 - g43)\,]\, V_{dc} \tag{10}$$

3.2 Switching Logic Generation for 4-cell Cascaded H-bridge:

4-cell cascaded H-bridge uses 8 triangular carriers for level-shifted multicarrier modulation. Switching logic essentially remains the same for all types of level-shifted modulation schemes mentioned in 2.2. For explaining the switching logic, in-phase disposition scheme is considered. PLECS simulation is used for generating carrier signals and modulating signal. Figure 3.2 shows the PLECS simulation platform used for analysis.

Modulating sine wave Vm(t) has peak amplitude of V_m = 169.71 V (120 Vrms) with modulating frequency, f_m = 60 Hz. All carrier signals have equal peak-to-peak amplitude V_{cr} = 50 and carrier frequency, f_{cr} = 1800 Hz. From (5) and (6), amplitude modulation index, M_a = 0.848 and frequency modulation index, M_f = 30. Figure 3.3 shows the spatial distribution of the carrier and modulating signal.

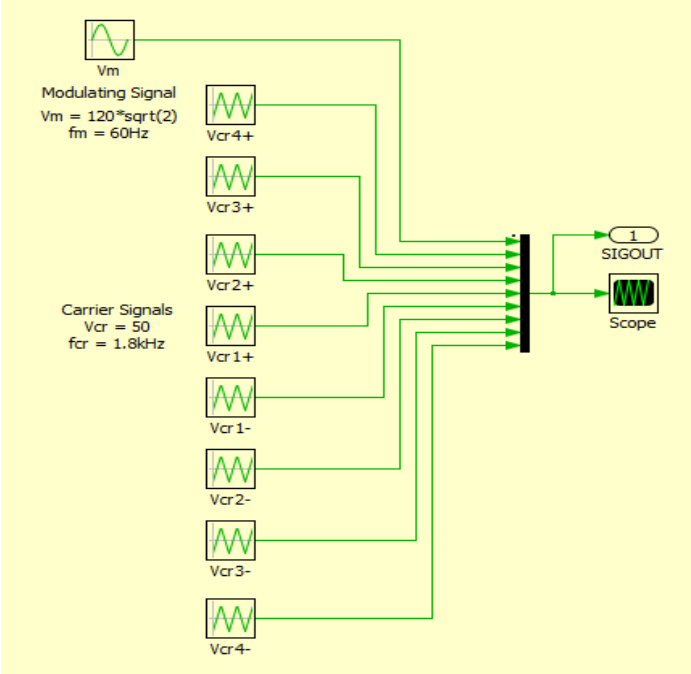

Figure 3.2 PLECS Simulation Platform for Carrier and Modulating Signal Generation

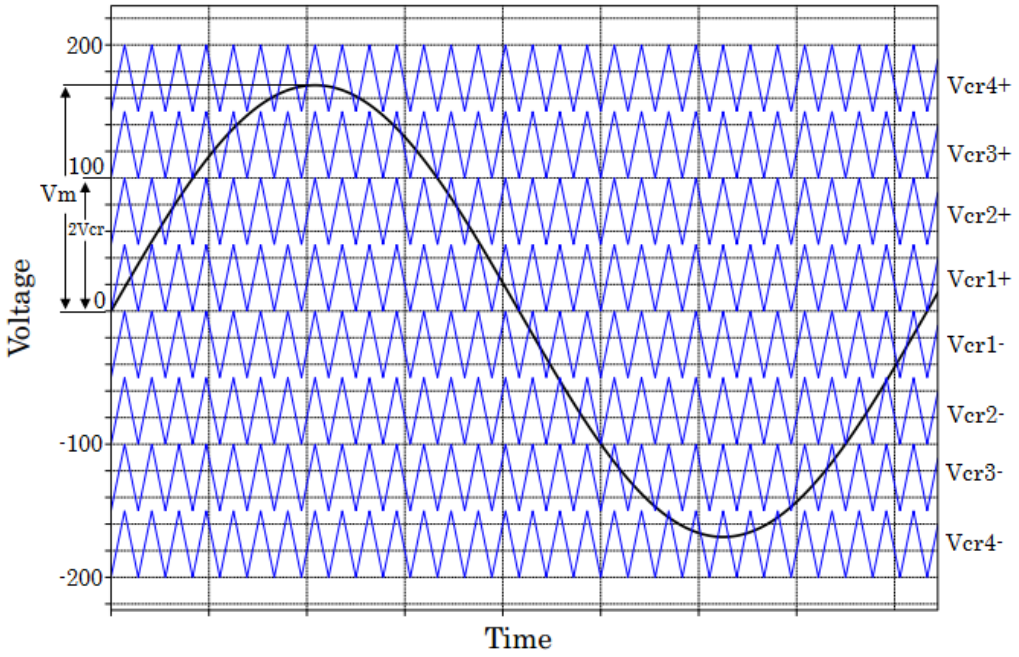

Figure 3.3 In-Phase Disposition with $M_a = 0.848$ and $M_f = 30$

As mentioned earlier, there are 8 carriers viz. Vcr4+, Vcr3+, Vcr2+, Vcr1+, Vcr1-, Vcr2-, Vcr3- and Vcr4-. The carriers with positive affix indicate that those triangular carriers lie in the positive region and same is applicable for explaining negative affix. Modulating signal Vm is simultaneously compared with carrier signals. In this scenario, carrier signals form 9 spatial regions that correspond to 9 voltage levels obtained by 4-cell cascaded H-bridge. Figure 3.4 indicates those 9 regions:

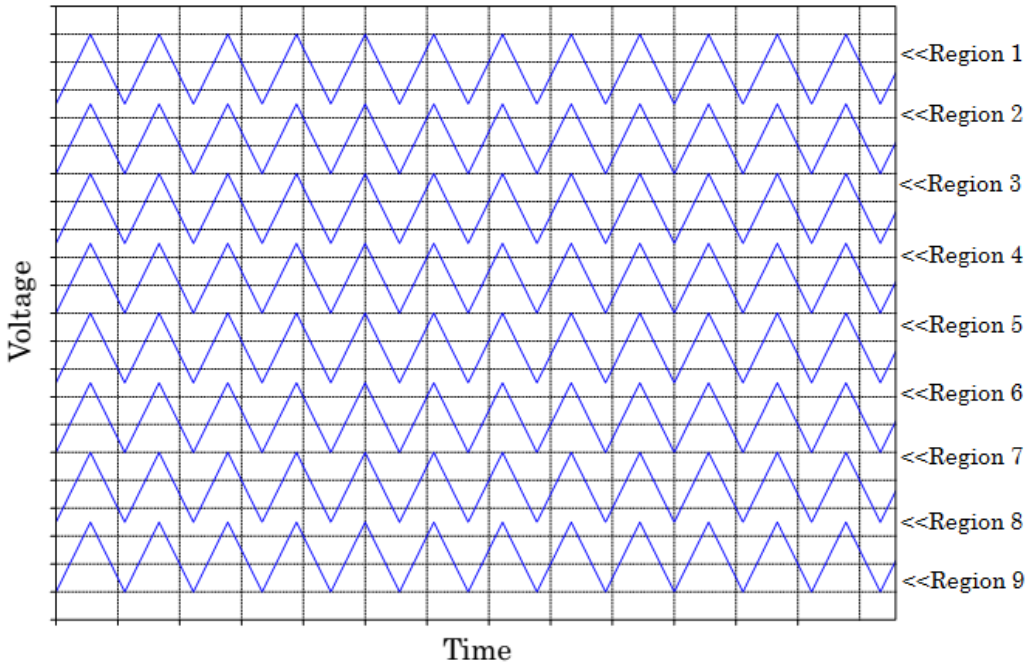

Figure 3.4 In-Phase Disposition Spatial Regions

Region 1 corresponds to maximum voltage level of +4Vdc that can be obtained by this multilevel inverter. The regions below that drop by Vdc each till it reaches region 9 which is the minimum voltage level of -4Vdc. The regions are basically the space between the carriers. When the modulating signal moves through particular region, corresponding

output voltage needs to be generated. For example, when modulating signal Vm lies in region 1, the corresponding output voltage of +4Vdc needs to be generated. Output voltage of +4Vdc would only be generated if all the cells are generating +Vdc at their output i.e. all switches S11, S21, S31 and S41 are all switched on and S13, S23, S33 and S43 are switched off. When Vm(t) moves from region 1 to region 2, +3Vdc is required at the output. In this case, top H-bridge cell is turned off i.e. net output from top H-bridge cell is 0 by making S11 off while keeping S21, S31 and S41 on and S13, S23, S33 and S43 are switched off again.

Table 3.1 on next page explains the sequence of switching for 4-cell cascaded H-bridge. The identification of regions occurs by comparing the instantaneous values of modulating signal with carrier signals. Output voltage $V_{AC}(t)$ is obtained from relationship between gating signals and output voltage as described in (10). Function block in Simulink is implemented in order to generate the corresponding switching logic.

Figure 3.5 shows on page 18 shows the switching pulses generated for the H-bridge using in-phase disposition. It can be observed that switches g11 and g13 conduct for short duration than those in 2nd cell. The conduction period of switches goes on increasing from 1st cell to 4th cell. From practical point of view, switches in top cells undergo lower conduction losses than those in bottom ones. Therefore the switching is rotated throughout every cell per cycle in switching frequency to evenly distribute these losses.

Table 3.1 Switching Table of 4-cell Cascaded H-Bridge

Region	Condition	g11	g13	g21	g23	g31	g33	g41	g43	$V_{AC}(t)$
1	Vm(t) > Vcr4+(t)	1	0	1	0	1	0	1	0	+4Vdc
2	Vcr3+(t) < Vm(t) < Vcr4+(t)	0	0	1	0	1	0	1	0	+3Vdc
3	Vcr2+(t) < Vm(t) < Vcr3+(t)	0	0	0	0	1	0	1	0	+2Vdc
4	Vcr1+(t) < Vm(t) < Vcr2+(t)	0	0	0	0	0	0	1	0	+Vdc
5	Vcr1-(t) < Vm(t) < Vcr1+(t)	0	0	0	0	0	0	0	0	0
6	Vcr2-(t) < Vm(t) < Vcr1-(t)	0	0	0	0	0	0	0	1	-Vdc
7	Vcr3-(t) < Vm(t) < Vcr2-(t)	0	0	0	0	0	1	0	1	-2Vdc
8	Vcr4-(t) < Vm(t) < Vcr3-(t)	0	0	0	1	0	1	0	1	-3Vdc
9	Vm(t) < Vcr4-(t)	0	1	0	1	0	1	0	1	-4Vdc

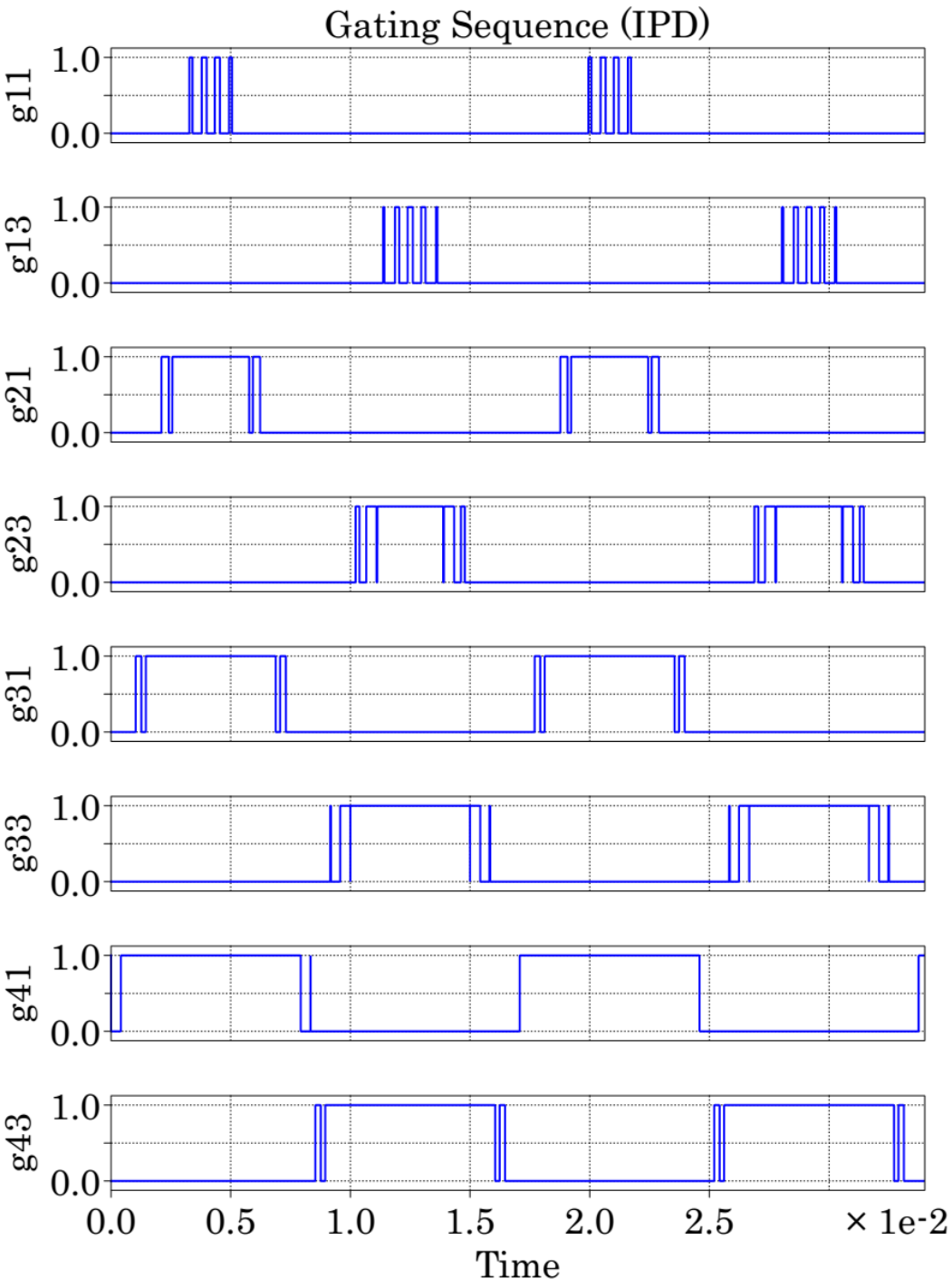

Figure 3.5 Switching Sequence of 4-cell Cascaded H-bridge

PLECS is used for designing cascaded H-bridge circuit with ideal MOSFET switches with integrated parallel diode. Figure 3.6 briefly shows the important details of implementation of the scheme in PLECS.

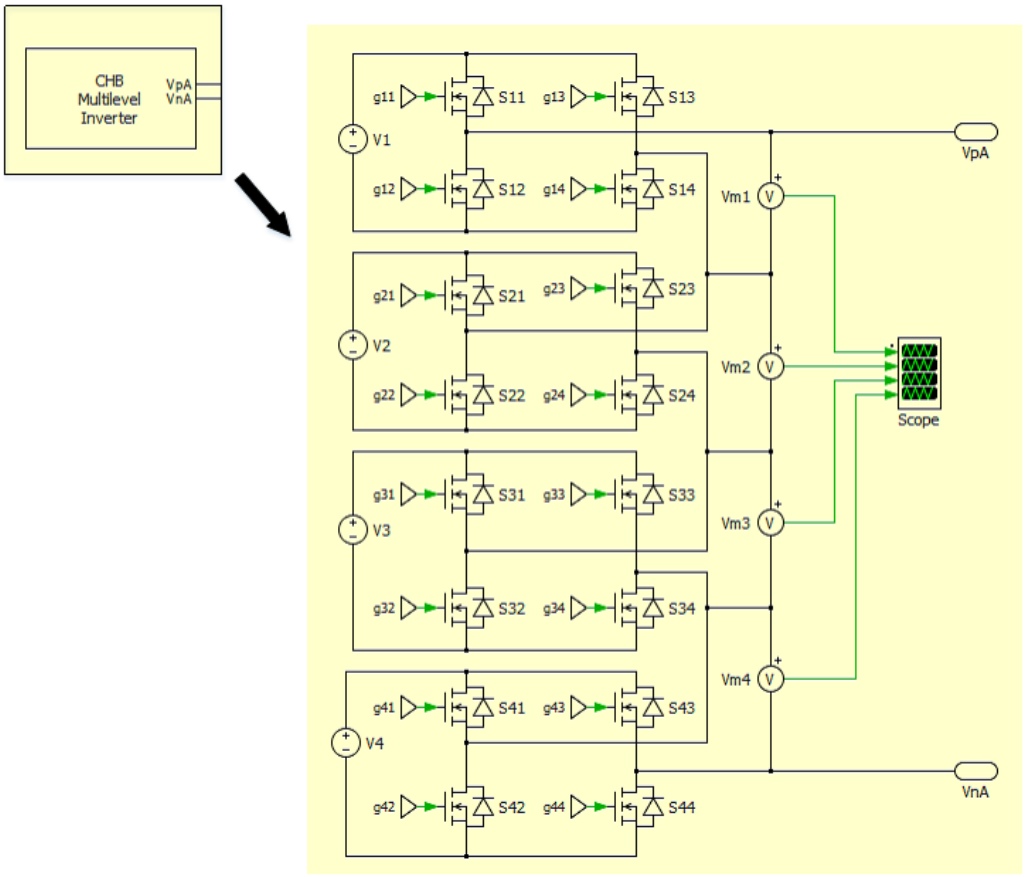

Figure 3.6 PLECS Implementation of 4-cell Cascaded H-bridge

In the figure above, the value of equal DC voltage sources is 50 V. Thus, the output voltage is obtained in steps of 50 V with 200 V and -200 V being the maximum and minimum DC voltage levels that can be obtained. Figure 3.7 and figure 3.8 show the single cycle of the output voltage that can be obtained with different values of M_a and M_f using IPD.

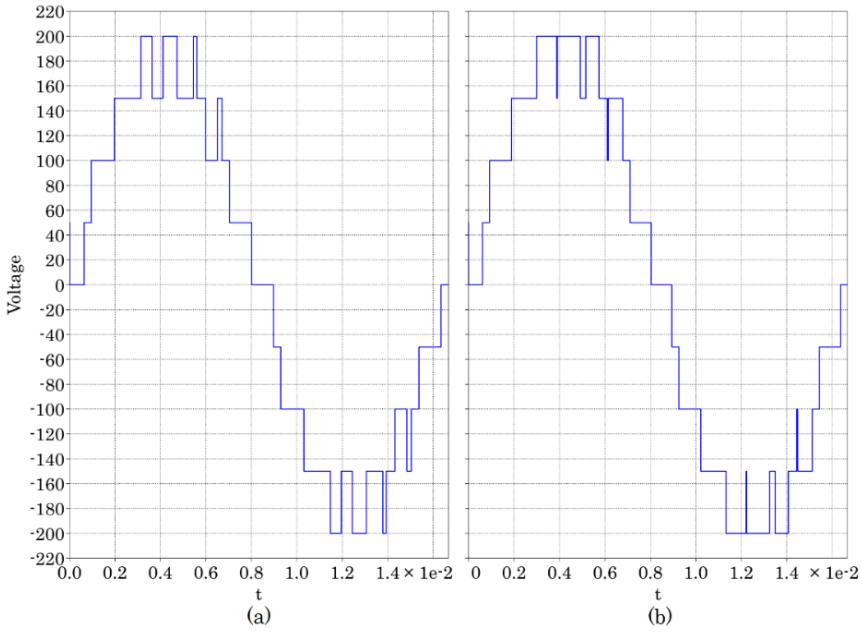

Figure 3.7 Output Voltage with (a) $M_a = 0.9$ and (b) $M_a = 1$ with $M_f = 15$ using IPD

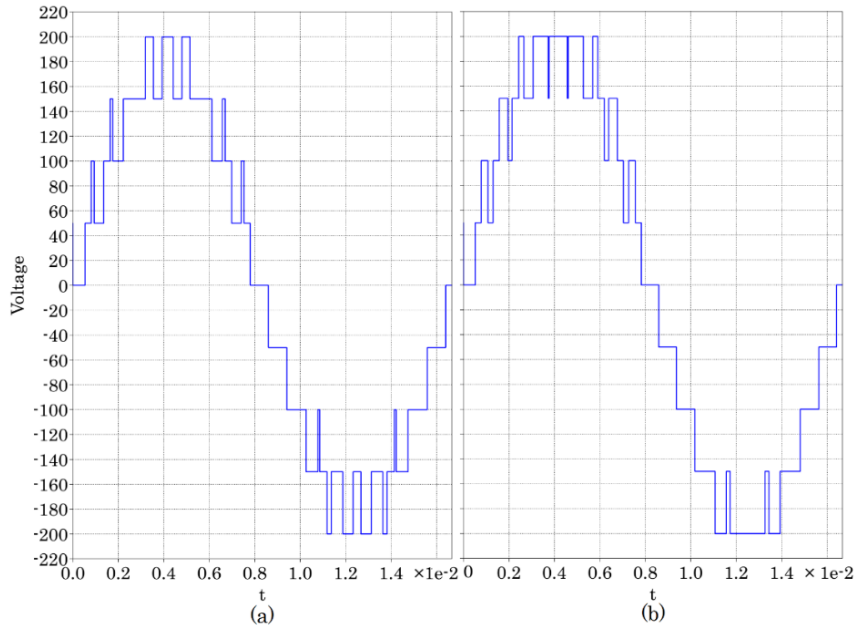

Figure 3.8 Output Voltage with (a) $M_a = 0.9$ and (b) $M_a = 1$ with $M_f = 20$ using IPD

From figure 3.7 and 3.8, it can be observed that with increase in value of M_a, the output voltage changes with in such a way that more amount of switching occurs at the top of the PWM sinusoidal wave. In figure 3.7, the PWM switched waveform is symmetrical on positive and negative part of the signal whereas in figure 3.8, it is asymmetrical. This occurs due to change in frequency modulation index. As per [8], the carrier frequency should be an odd triplen of the modulating frequency to have symmetrical output signal i.e. M_f should be 3,9,15,21,… Article 4.1 shows the effect on harmonic spectrum of the signal when M_f is neither a triplen nor an integer. Having symmetrical placement of switched pulses leads to lower harmonic content. Thus values of M_f are kept as odd triplens for further analyses.

4. Total Harmonic Distortion with PWM Techniques

The output voltage obtained from cascaded H-bridge by using PWM schemes is fundamentally a switched pattern of DC voltage levels that are fed to the H-bridge cells. Principally, all modulation schemes are designed to generate a train of switched pulses which have the same fundamental volt – second average i.e. integral of the voltage waveform over time as a target reference waveform at any instant [5]. In case of level-shifted multicarrier modulation, the target waveform is the modulating sine wave. One of the major problems with generation of the train of pulses is that they also contain unwanted harmonic components that need to be minimized.

For any PWM scheme, primary objective can be put forward as to calculate the converter switch ON times which helps in creating the desired low frequency target output voltage or current. Having reached this objective, the secondary objective is to determine the most efficient way of arranging the switching process to minimize unwanted harmonic distortion [6].

4.1 Theory of Fast Fourier Transform and Harmonic Spectrum:

The principle of Fourier decomposition theory is that any signal varying over time *f(t)* can be expressed as infinite series of sinusoidal harmonics viz.:

$$f(t) = \frac{a_0}{2} + \sum_{m=1}^{\infty} (a_m \cos m\omega t + b_m \sin m\omega t) \qquad (11)$$

Where,

$$a_m = \int_{-\pi}^{\pi} f(t) \cos m\omega t \, d(\omega t) \qquad m = 0, 1, \ldots, \infty$$

$$b_m = \int_{-\pi}^{\pi} f(t) \sin m\omega t \, d(\omega t) \qquad m = 1, 2, \ldots, \infty$$

The concept of level-shifted multicarrier converter system is that the low frequency modulating signal is compared against a high frequency carrier waveform. The output obtained from this comparison is used to control the state of switched phase leg. When the modulating waveform is higher than carrier signal, the phase leg is switched to upper DC rail. When the modulating waveform is lower than carrier signal, phase leg is switched to lower DC rail. Determination of harmonic frequency components of a PWM switched phase leg output is quite complex and thus done using Fast Fourier Transform (FFT) analysis of simulated time-varying signal.

In (11), time-varying signal *f(t)* is the voltage output obtained from modulating signal and carrier signal. The analysis of obtaining *f(t)* can be done by assuming two time variables $x(t) = f(\omega_c)$ and $y(t) = f(\omega_0)$ where ω_c is carrier angular frequency and ω_0 is the modulating wave angular frequency and thus formulating f(t) as, $f(t) = f[x(t), y(t)]$. Equation 3.10 in [6] formulates *f(t)* in terms of decomposing the waveform in four categories as shown in figure 4.1:

(a) DC Offset

(b) Fundamental components and baseband harmonics

(c) Carrier harmonics

(d) Sideband harmonics

$$f(t) = \underbrace{\frac{A_{00}}{2}}_{\text{DC Offset}} + \sum_{n=1}^{\infty} \underbrace{[A_{0n}\cos(n[\omega_o t + \theta_o]) + B_{0n}\sin(n[\omega_o t + \theta_o])]}_{\text{Fundamental Component \& Baseband Harmonics}}$$

$$+ \sum_{m=1}^{\infty} \underbrace{[A_{m0}\cos(m[\omega_c t + \theta_c]) + B_{m0}\sin(m[\omega_c t + \theta_c])]}_{\text{Carrier Harmonics}}$$

$$+ \sum_{m=1}^{\infty} \sum_{\substack{n=-\infty \\ (n \neq 0)}}^{\infty} \underbrace{\left[\begin{array}{l} A_{mn}\cos(m[\omega_c t + \theta_c] + n[\omega_o t + \theta_o]) \\ \quad + B_{mn}\sin(m[\omega_c t + \theta_c] + n[\omega_o t + \theta_o]) \end{array}\right]}_{\text{Sideband Harmonics}}$$

Figure 4.1 Decomposition of PWM waveform

The magnitudes of harmonic components can be obtained by $C_{mn} = \sqrt{A_{mn}^2 + B_{mn}^2}$ where m is carrier index variable and n is baseband index variable. This equation indicates that the harmonic components exist at fundamental frequency, integral multiples of fundamental frequency, carrier frequency, integer multiples of carrier frequency and in the groups of frequencies created which are because of interaction of fundamental and carrier frequencies which are called sideband frequencies given by $m\omega_c + n\omega_0$.

Figure 4.2 shows the harmonic spectrum of output voltage obtained from 4-cell cascaded H-bridge. Carrier frequency is 500 Hz and modulating frequency is 60 Hz with $M_a = 1$ using PLECS simulation block. Y-axis is the relative amplitude of the harmonic component with respect to fundamental component. Harmonics of fundamental frequencies (120 Hz, 180 Hz, 240 Hz,…) have relative amplitudes ranging from 2.5-4%. Carrier frequency has relative amplitude of 10% which is considerable.

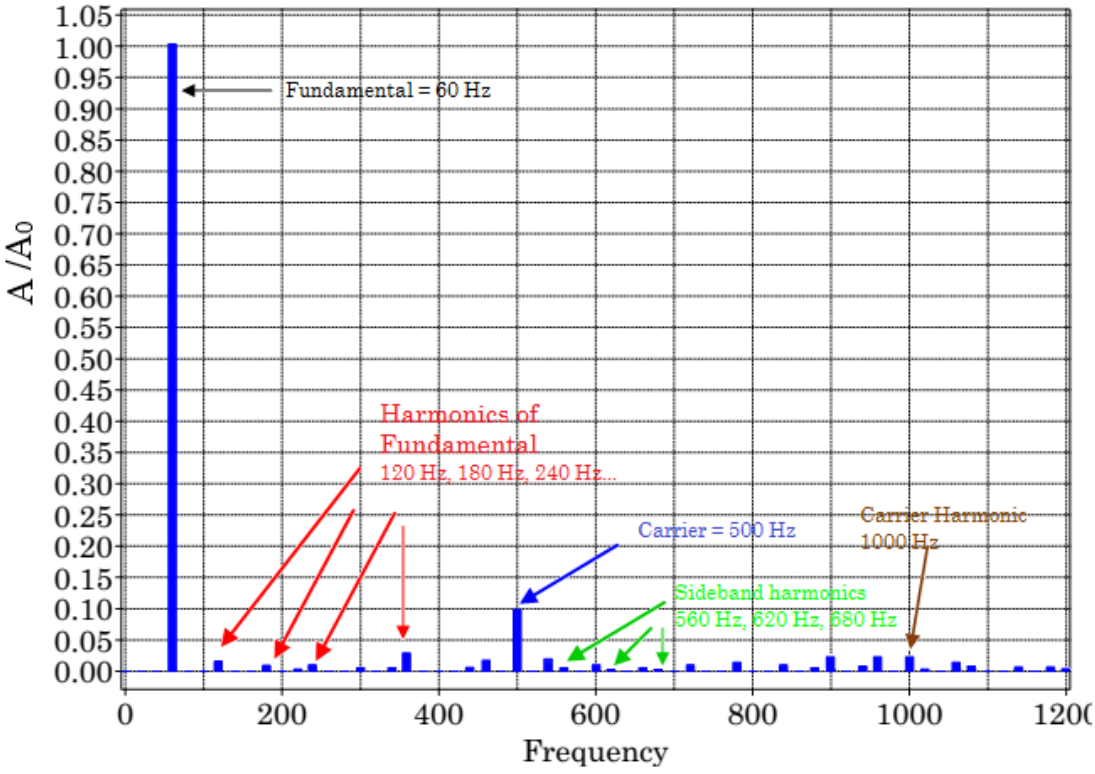

Figure 4.2 Harmonic Spectrum using IPD ($M_a = 1$; $f_{cr} = 500$; $f_m = 60$)

Also, the figure shows sideband harmonics (560 Hz, 620 Hz, 680 Hz) obtained using $m\omega_c + n\omega_0$ by substituting m=1 and n=1,2,3… which have less than 1% of relative amplitude.

4.2 Calculation of Total Harmonic Distortion (THD):

Total harmonic distortion is the measurement of harmonics present in the particular signal. It is defined as the ratio of sum of powers of all harmonic components to the power of the fundamental frequency.

$$THD = \sqrt{\frac{V_2^2 + V_3^2 + \cdots + V_n^2 + \cdots}{V_1^2}} \tag{12}$$

Figure 4.2 shows that harmonic spectrum of PWM also contains non-harmonic frequencies. This tends to occur because the carrier frequency 500 Hz is not an integral multiple of modulating signal of 60 Hz. Having non-harmonic frequencies gives rise to noise in PWM signal which does not have any effect on THD, but it affects another term called THD+N (Total Harmonic Distortion with Noise) which is defined as,

$$THD + N = \frac{\sqrt{\sum_{i=2}^{\infty} V_n} + noise}{V_1} \tag{13}$$

If the carrier frequency is integral multiple of modulating signal frequency (fundamental), harmonic spectrum of consists purely of harmonic components of fundamental frequency because in this case, even sideband harmonics are harmonic components. In order to have THD+N same as THD, M_f is kept as an integer and an odd triplen for including noise in the further analysis thus not having to develop separate consideration for noise factor.

Since power of a sinusoidal signal is directly proportional to the square of its amplitude, it is easier to find the THD in terms of amplitudes of its harmonic components. In (12), V_n represents the n^{th} harmonic component of the signal. In order to facilitate calculation of THD in Simulink, (11) can be modified as,

$$THD = \sqrt{\frac{V_{sig}^2 - V_1^2}{V_1^2}} \tag{14}$$

Simulink allows to calculate true signal power and also the power of the fundamental frequency, thus (12) can be implemented as shown in figure 4.3

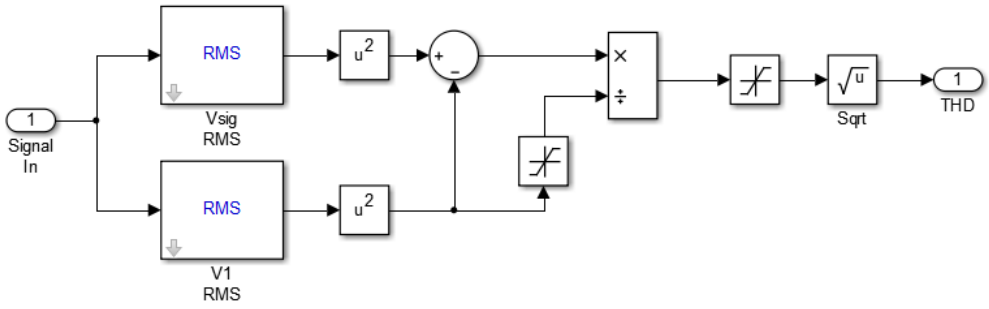

Figure 4.3 THD Calculator Implementation in Simulink

Vsig RMS block calculates the total root mean square value of the signal while V1 RMS block calculates the RMS value of the fundamental component of the signal as specified by the fundamental frequency in RMS block. Sample time of measurement is 1 μs and fundamental frequency is 60 Hz. Saturation blocks are provided to avoid the division by 0 and having error in simulation.

4.3 Total Harmonic Distortion of PWM Schemes:

In this section, THD for PWM methods mentioned in article 2.2 is plotted for different values of M_a and M_f. Frequency modulation index, M_f is kept as an odd triplen throughout the analysis. M_a is limited because of implementation of level-shifted modulation. In order to generate 9-level PWM from 4-cell cascaded H-bridge, modulating signal should pass through all regions in order to generate appropriate switching pulses. If M_a should be small enough so that it modulating signal can cross through all the regions, the output is

obtained is restricted to 7 levels rather than 9 levels because of switching signals are not produced for top H-bridge.

For example, if amplitude of carrier frequency i.e. $V_{cr} = 70$ and amplitude of modulating frequency i.e. $V_m = 120\sqrt{2}$, this gives us $M_a = 0.61$ for 9-level inverter from (5). The switching waveform for $M_f = 9$ appears as shown in figure 4.4

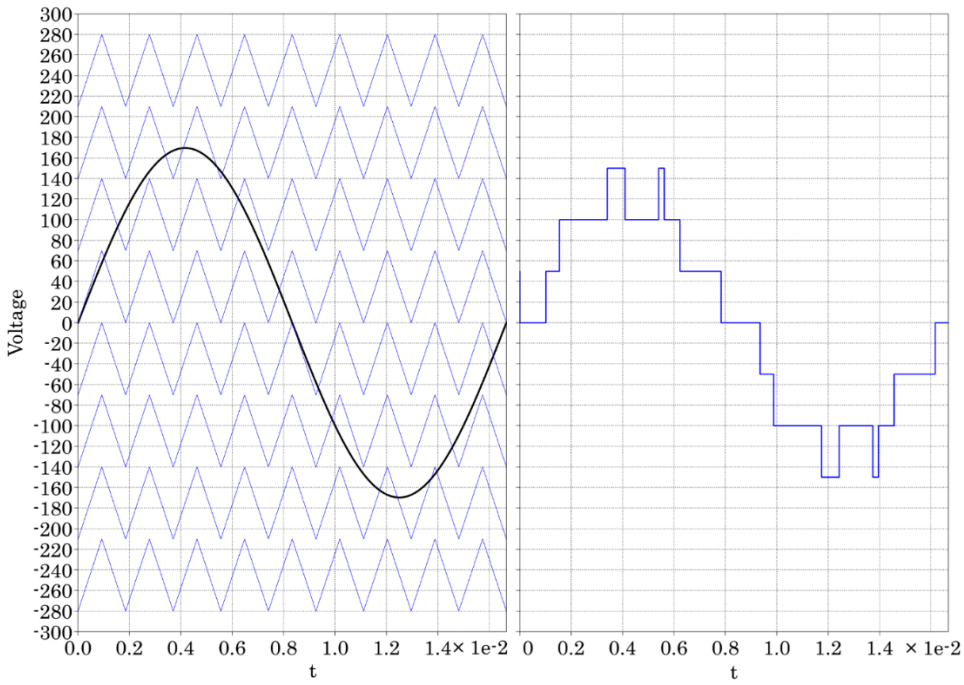

Figure 4.4 Limitation on Amplitude Modulation Index (M_a)

As seen from the simulation results, keeping M_a as low as 0.61 results in only 7 levels with maximum and minimum DC voltage levels being +150 and -150 respectively. Thus, carrier amplitude should have a maximum value for which modulating signal can

generate required number of voltage levels. This leads to formulation for maximum amplitude for carrier signal as for n-cell inverter,

$$V_{cr,max} = \frac{V_m}{(n-1)} \tag{15}$$

From (5), minimum M_a for a particular n-cell inverter can be given by,

$$M_{a,min} = \frac{V_m}{nV_{cr,max}}$$

$$M_{a,min} = \frac{n-1}{n} \tag{16}$$

From (15) and (16), 4-cell 9-level inverter has $V_{cr,max} = 56.568$ and $M_{a,min} = 0.75$.

THD (%) is plotted with variation for M_f = [3,9,15,…,57] and $0.75 < M_a < 1$ with in figures 4.5, 4.6 and 4.7 for different PWM methods.

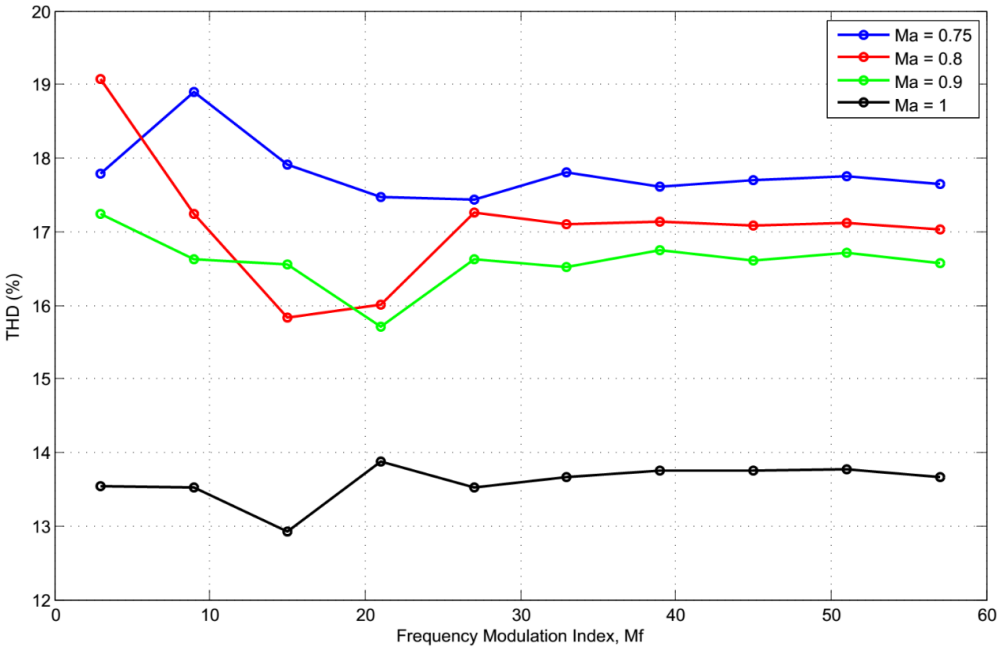

Figure 4.5 THD vs M_f for Variation in M_a (In-Phase Disposition)

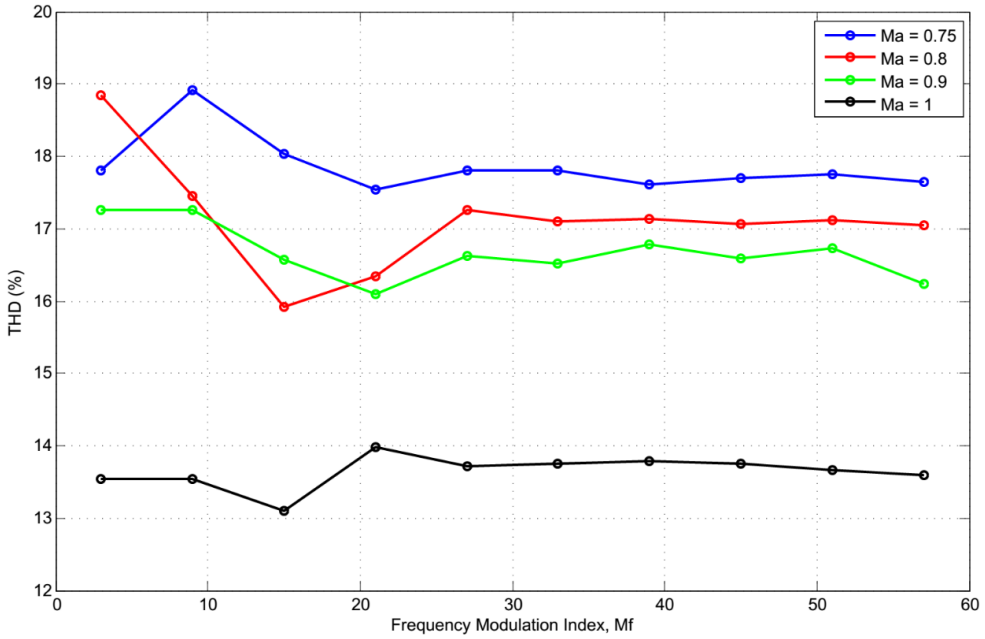

Figure 4.6 THD vs M_f for Variation in M_a (Phase Opposition Disposition)

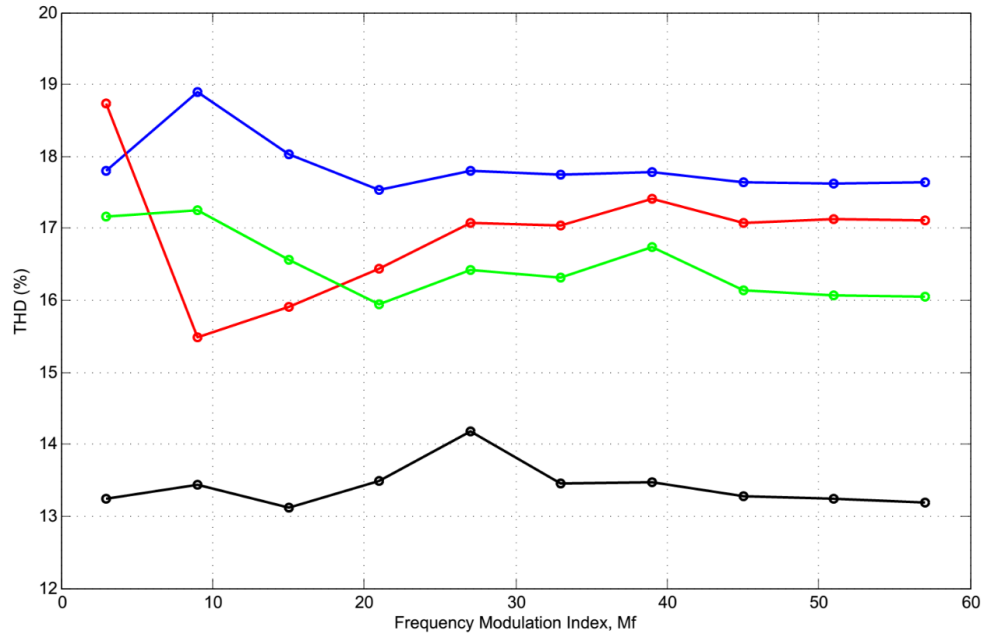

Figure 4.7 THD vs M_f for Variation in M_a (Alternative Phase Opposition Disposition)

From analytical point of view of figures 4.5-4.7, it can be concluded that,

(a) For all the PWM schemes, THD goes on decreasing as amplitude modulation index M_a is increased.

(b) At higher values of frequency modulation index M_f, THD more or less remains the same. This indicates that increase in carrier signal frequency does not affect THD significantly.

(c) In terms of decreasing THD, the effectiveness of PWM schemes is observed as APOD > POD > IPD. (Please refer Appendix A for graph data)

5. Proposed Modification of Carrier Signal for THD Reduction

5.1 Introduction to Space Vector Modulation (SVM):

Cascaded H-bridge multilevel inverters can be regarded as voltage-source inverters (VSIs). Single-phase and three-phase VSIs can be used to synthesize AC voltage waveforms using sinusoidal pulse width modulation (SPWM) technique which is extensively used, because it improves harmonic spectrum of the inverter by moving the voltage harmonic components to higher frequencies [6]. Level-shifted modulation technique is one of the conveniently adapted form of SPWM used substantially for operating cascaded H-bridge.

Space Vector Modulation (SVM) is the modified version of SPWM wherein the possible switching vectors are known in the given output voltage space. SPWM determines the width of pulses from the interactions between carrier signal and modulating signal. This width is often determinable but only with the help of complex mathematical analysis because of varying frequency modulation index and amplitude modulation index. SVM is simply an alternative method for determining switched pulse widths. Main benefit of SVM is the explicit identification of pulse placement as an additional degree of freedom which can be exploited to achieve harmonic performance gains.

Principle of SVM is typically used in voltage-source three-phase inverters. For three-phase inverter with 3 legs and two switches per leg, there typically eight possible switch combinations which result in output voltage vectors. These stationary vectors, at any point of time, can form an arbitrary target output voltage $\overline{V_0}$ by summing the volt-seconds

of these space vectors within one switching period. Two voltage vectors are typically available during one switching period which can be added mathematically to obtain target output voltage as,

$$\overline{V_0} = V_0 \angle \theta_0 = \frac{T_1}{T_{SW}} \overline{V_1} + \frac{T_2}{T_{SW}} \overline{V_2} \tag{17}$$

T_1 and T_2 are the times for which space vectors $\overline{V_1}$ and $\overline{V_2}$ are selected in switching period of T_{SW}.

5.2 Application of SVM to Cascaded H-bridge Multilevel Inverter:

This same principle in (17) can be made applicable to level-shifted PWM schemes where m number of voltage levels are available in order to synthesize the output voltage. Consider 4-cell multilevel inverter fed from unequal DC voltages $V_{dc1} - V_{dc4}$ from which 9 voltage levels can be obtained. As shown in figure 5.1, 4 voltage vectors each having amplitudes $V_{dc1} - V_{dc4}$ are arranged to obtain target output voltage $\overline{V_0}$.

T1, T2, T3 and *T4* are assumed to be the time intervals for which corresponding voltage vectors from each cell in H-bridge are selected. The output voltage obtained from these can be given as,

$$\overline{V_0} = \overline{V_1} + \overline{V_2} + \overline{V_3} + \overline{V_4}$$

$$\overline{V_0} = \frac{T_1}{T_{SW}} \overline{V_{dc1}} + \frac{T_2}{T_{SW}} \overline{V_{dc2}} + \frac{T_3}{T_{SW}} \overline{V_{dc3}} + \frac{T_4}{T_{SW}} \overline{V_{dc4}}$$

For equal DC voltage,

$$\overline{V_0} = \frac{(T_1 + T_2 + T_3 + T_4)}{T_{SW}} \overline{V_{dc}} \tag{18}$$

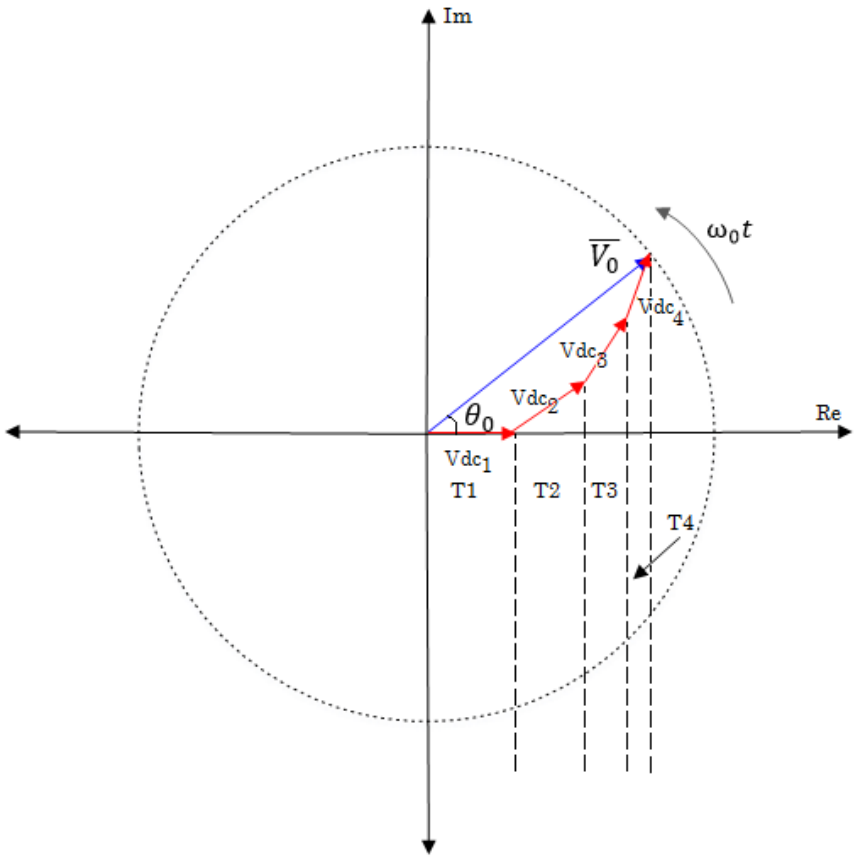

Figure 5.1 Space Vector Interpretation of Cascaded H-bridge Multilevel Inverter

Time intervals *T1-T4* are marked on the output of 4-cell H-bridge multilevel inverter fed with equal DC voltage V_{dc} in figure 5.2. The PWM scheme used is In-Phase Disposition. Individual times t_{1A}, t_{2A}... represent the amount of times one H-bridge cell generates V_{dc}.

THD of the output voltage waveform does not change with increase in carrier frequency as it was observed from THD calculation in Chapter 4. Unnecessarily increasing carrier frequency can also result in higher switching loss in the devices. Increasing M_a results in THD reduction, but it can only be limited to 1.

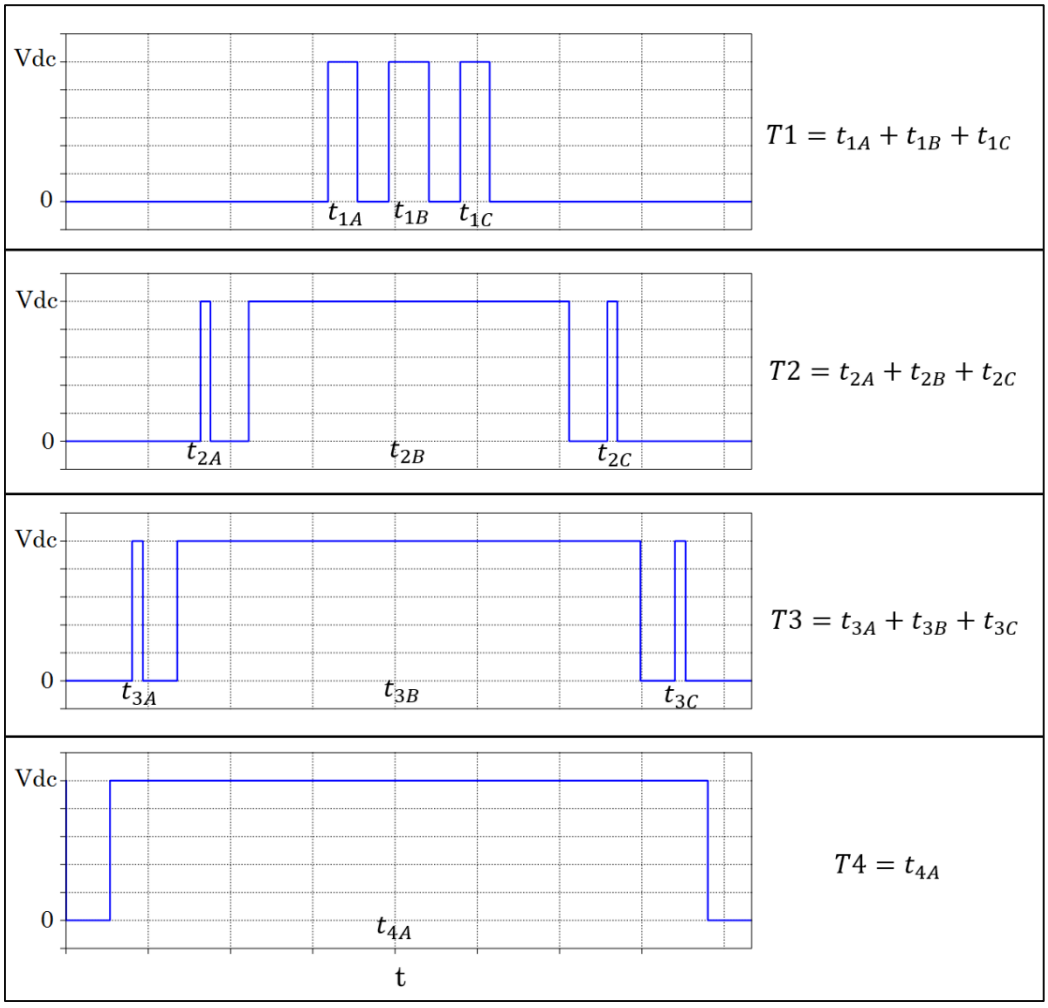

Figure 5.2 T1-T4 on Individual H-bridge Output Waveforms

5.3 Modification of Carrier Signals:

Space vector interpretation of the level-shifted multicarrier modulation showed that the output AC voltage vector $\overline{V_0}$ is obtained by number of individual voltage vectors obtained by individual H-bridge cells. These voltage vectors viz. $\overline{V_1}$, $\overline{V_2}$, $\overline{V_3}$ and $\overline{V_4}$ are actually the time-sampled instances of DC voltages. If these voltage vectors are subdivided in smaller

voltages themselves, there would be additional degree of freedom that could form the target output AC voltage.

An obvious way of achieving that is have as many number of DC voltage levels as possible. Although theoretically possible, having numerous H-bridge cells in multilevel inverters would result in additional amount of components and control of these individual cells working together becomes complex furthermore. Different way of achieving this is to divide the carrier frequency in equal voltage levels to get one DC voltage level by synthesis of new carrier. Having divided the carrier in equal voltage levels, each voltage vector, for example, $\overline{V_1}$ can be resolved as shown in figure 5.3

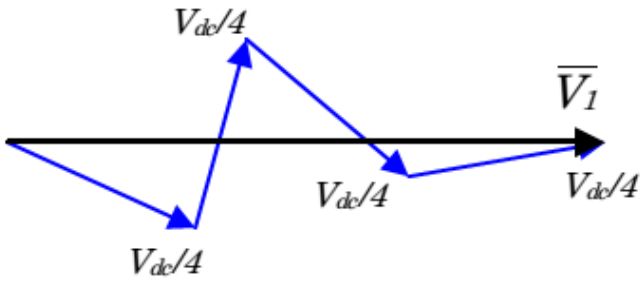

Figure 5.3 Vector Decomposition of Individual Voltages

In cascaded H-bridge, the voltage levels of $V_{dd}/4$ are not explicitly available. These virtual voltage levels can be created by generating smaller volt-seconds and dividing the time intervals *T1-T4* in figure 5.2 in more discrete amounts thereby dividing the times t_{1A}, t_{1B}, t_{2A},… as shown in figure 5.2 in smaller sections [6]. Dividing the carrier signal in equal parts results in obtaining the desired output voltage.

Synthesis of Modified Carrier Wave for n-cell Cascaded H-bridge:

(1) Original carrier signal of maximum amplitude V_{cr} is assumed to be divided in n equal parts for maintaining a consistent symmetry with original structure of carriers thus ensuring maximum harmonic performance [6].

(2) In given voltage space, n carrier signals with frequency of $(2n-1)f_{cr}$ are shown which lead to composing modified carrier, because of which these carrier signals are divided in $(2n-1)$ parts with respect to original carrier signal.

(3) $1^{st}$and $(2n-1)th$ part of 1^{st} carrier signal with maximum amplitude of Vcr/n, $2^{nd}$and $(2n-2)th$ part of 2^{nd} carrier signal with maximum amplitude of $2Vcr/n$, …, $i^{th}$and $[2n-i]th$ part of i^{th} carrier signal with maximum amplitude of $iVcr/n$ where $i < (\frac{n}{2})$ AND $\left(\frac{n}{2}\right)nd$ part of $\left(\frac{n}{2}\right)th$ carrier signal with maximum amplitude of Vcr are added together to synthesize the modified carrier signal.

In figure 5.4, black signal shows the modified carrier signal with respect to original carrier signal indicated by red signal for 4-cell cascaded H-bridge. The amplitude V_{cr} is divided in 4 equal parts of $0.25\,V_{cr}$. 4 signal carriers indicated by blue signals with frequency of $7f_{cr}$ leads to construction of the modified carrier signal. Same concept can be applied for 6-cell cascaded H-bridge, where V_{cr} is divided in 6 equal parts and 6 signal carriers with frequency of $11f_{cr}$ form the new carrier signal as shown in figure 5.5.

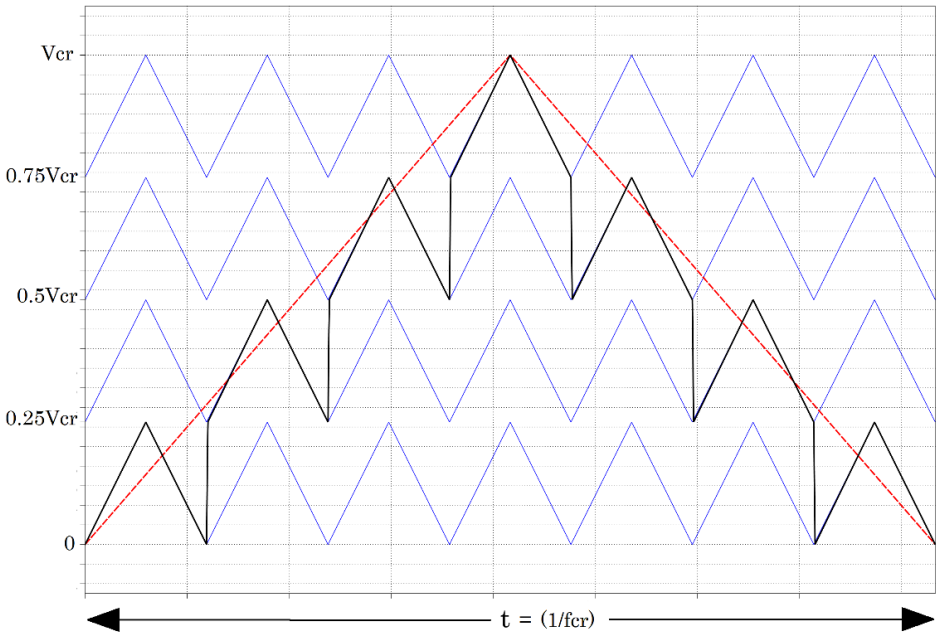

Figure 5.4 Modified Carrier Signal for 4-cell Cascaded H-bridge

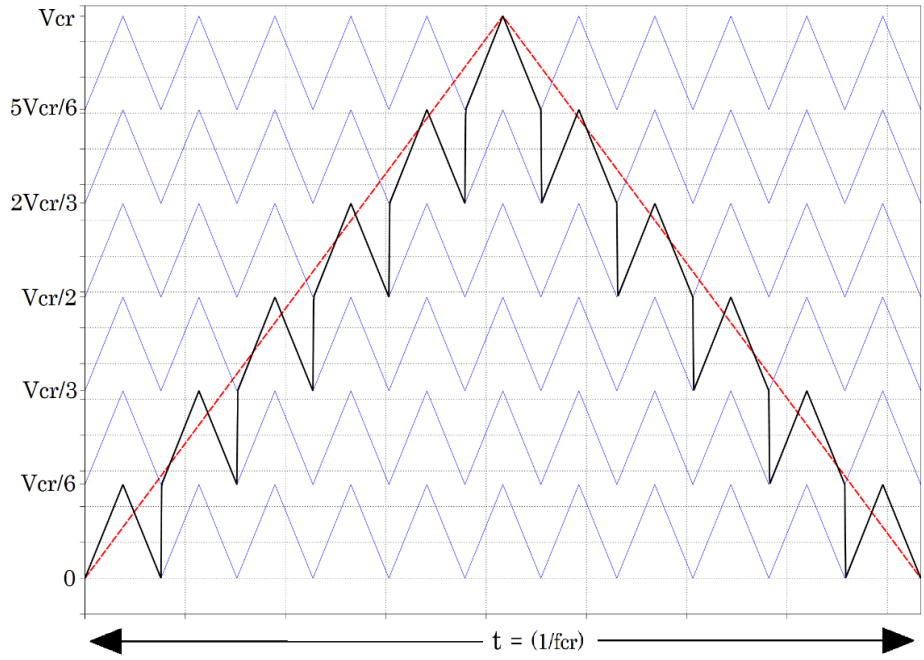

Figure 5.5 Modified Carrier Signal for 6-cell Cascaded H-bridge

5.4 Performance Comparison of Level-Shifted PWM Schemes with Modified Carrier:

Modified carrier scheme is implemented for level-shifted PWM schemes to verify the effectiveness in reduction of THD of output. Figure 5.6 shows the carrier signals and modulating signal for In-Phase Disposition (a), Phase-Opposition Disposition (b) and Alternate Phase-Opposition Disposition (c).

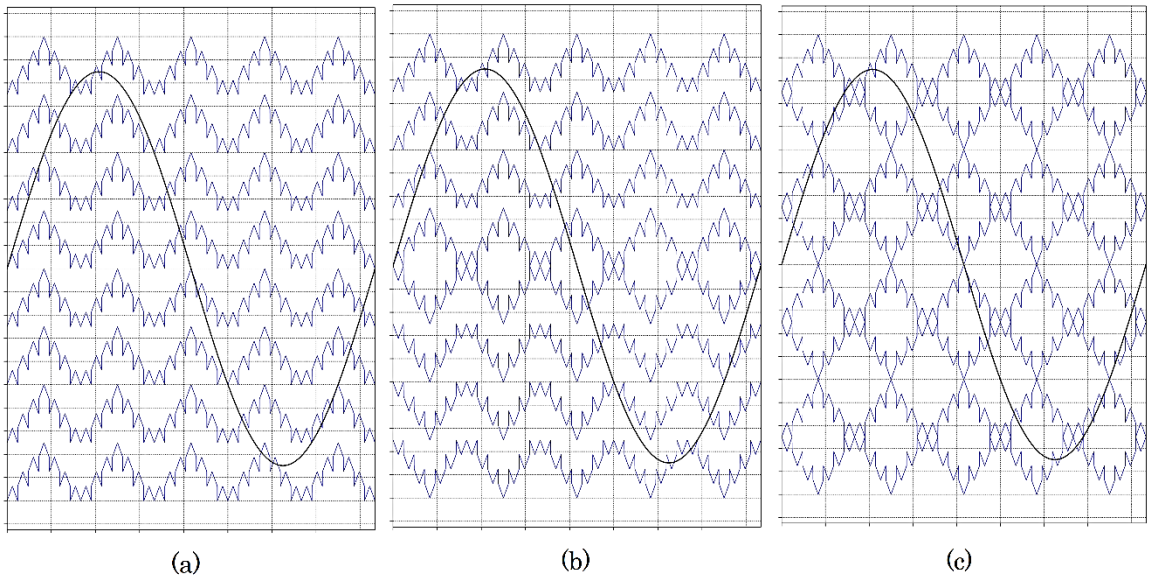

Figure 5.6 IPD – POD – APOD with Modified Carrier Signal

Effect of modifying the carrier wave are analyzed by comparing:

(a) Output voltage waveform

One cycle of output obtained with modified carrier is compared with conventional level-shifted carriers. The comparison is done with fixed M_f (= 21) and M_a (= 0.9) for visually distinguishing the output voltage.

(b) Harmonic spectrum of output voltage waveform

With fixed values of M_f(= 9) and M_a (= 0.9), the amplitude of harmonic frequencies is compared up to 30th harmonic of fundamental i.e. 1.8 kHz

(c) Comparison in THD for different values of M_a

THD values are plotted against variation in M_f from 3 to 57 with M_f being an odd triplen and different values of M_a (0.9 and 1) in comparison with conventional and modified carrier signals.

5.5 Comparative Analysis of PWM Schemes for 4-cell Cascaded H-bridge:

(i) Output Voltage:

(a) is the output voltage obtained from conventional carrier and (b) is the output voltage obtained from modified carrier.

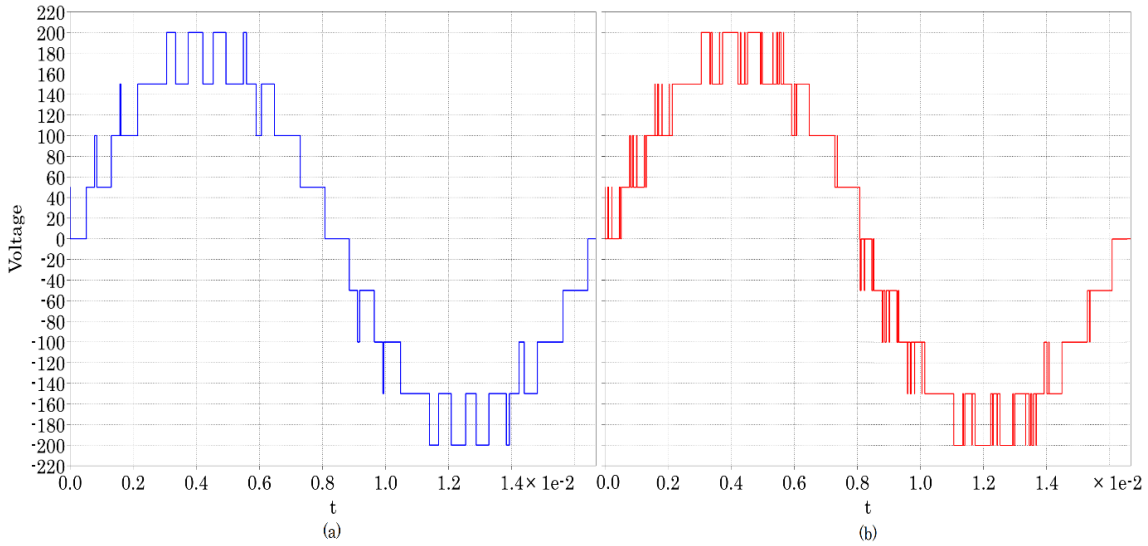

Figure 5.7 Output Voltage Comparison with IPD

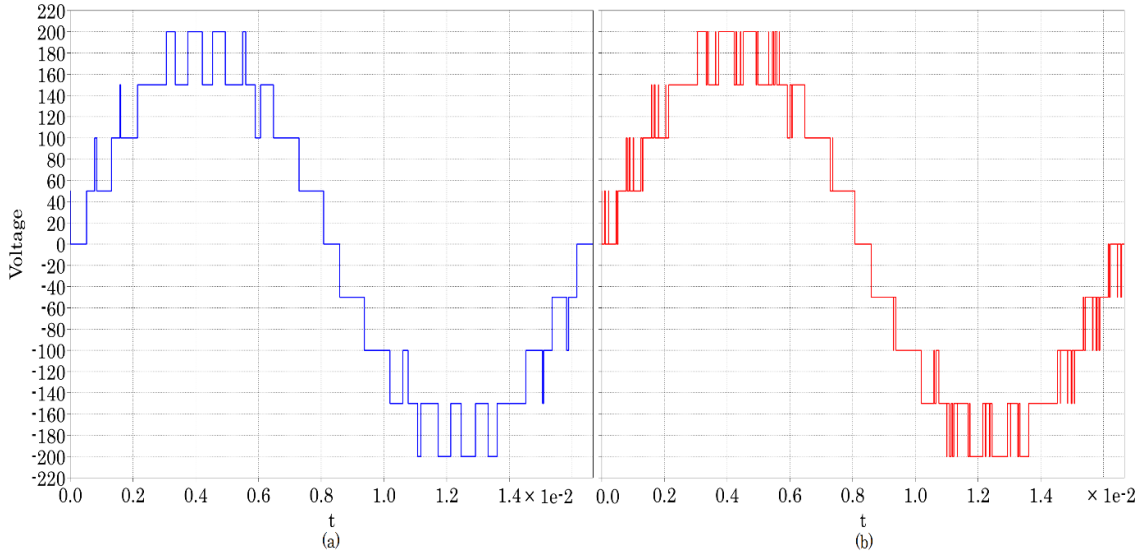

Figure 5.8 Output Voltage Comparison with POD

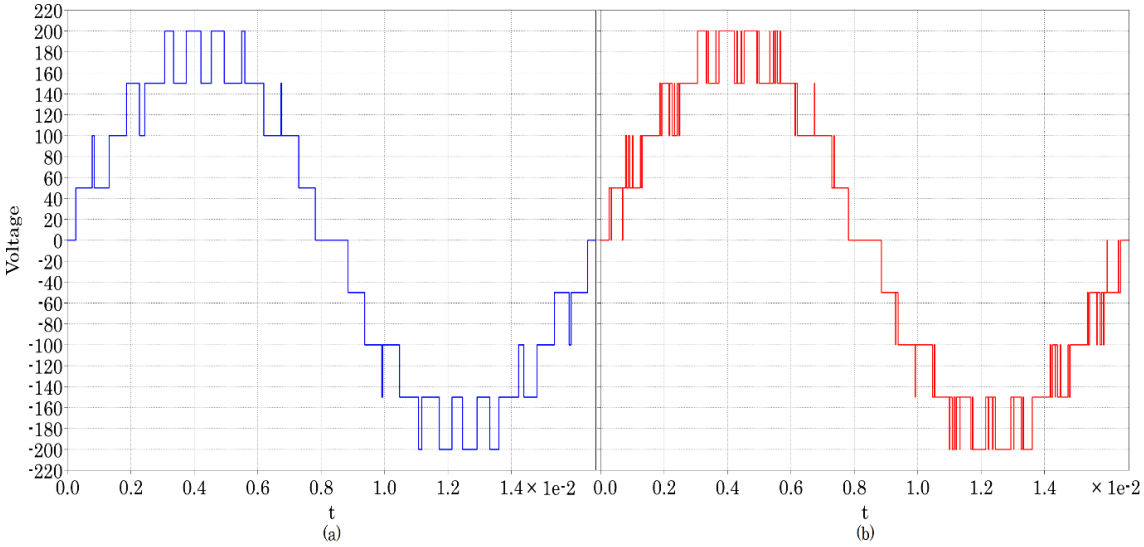

Figure 5.9 Output Voltage Comparison with APOD

As seen from the output waveforms from figures 5.7-5.9, time intervals *T1-T4* discussed in article 5.3 are divided smaller sections in (b) which is the desired outcome.

(b) Harmonic spectrum of output voltage waveform:

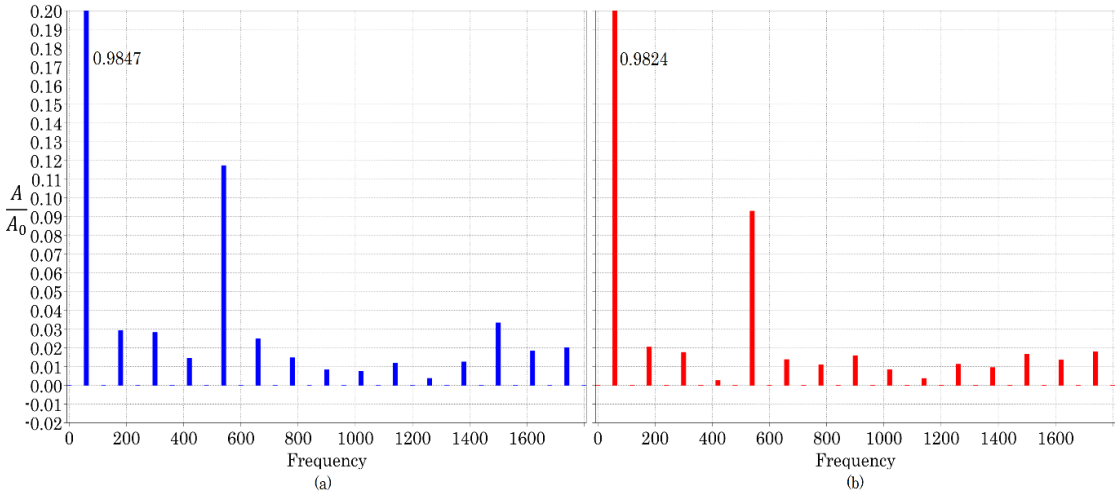

Figure 5.10 Harmonic Spectrum Comparison with IPD

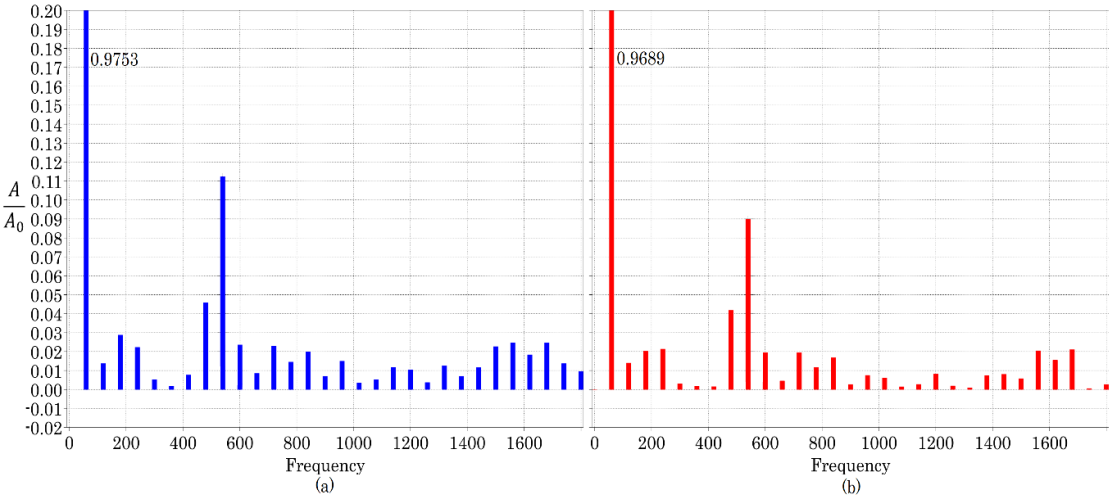

Figure 5.11 Harmonic Spectrum Comparison with POD

Relative magnitude of harmonic frequencies with respect to fundamental frequency, $\frac{A}{A_0}$ is plotted with frequency. As seen from the two spectra (a) and (b) in figures 5.9-5.11, magnitudes of majority of harmonic components are reduced considerably.

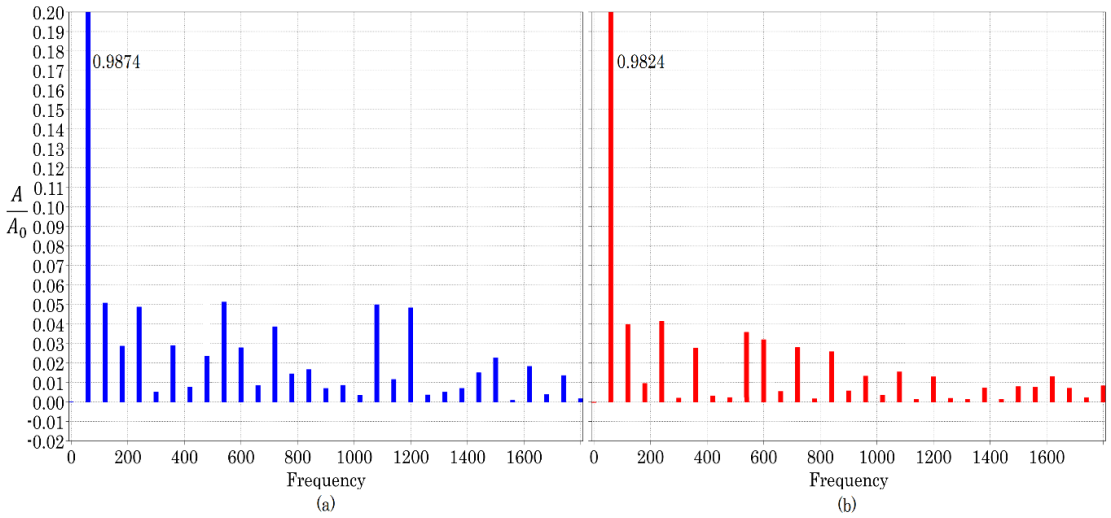

Figure 5.12 Harmonic Spectrum Comparison with APOD

Magnitude of fundamental frequency is shown in (a) and (b) which is close to 1. It is observed that the effect in reducing the harmonic content is more prominent in case of phase opposition disposition PWM technique than other two techniques. This also gets reflected in THD graphs in following section.

(c) Comparison of THD for different values of M_a:

Harmonic spectral comparison of PWM techniques gives an idea about harmonic distortion in the waveform. However the THD in each output waveform varies with change in frequency modulation index. This variation is plotted in figures 5.13, figure

5.14 and figure 5.15 for In-Phase Disposition, Phase Opposition Disposition and Alternate Phase Opposition Disposition respectively.

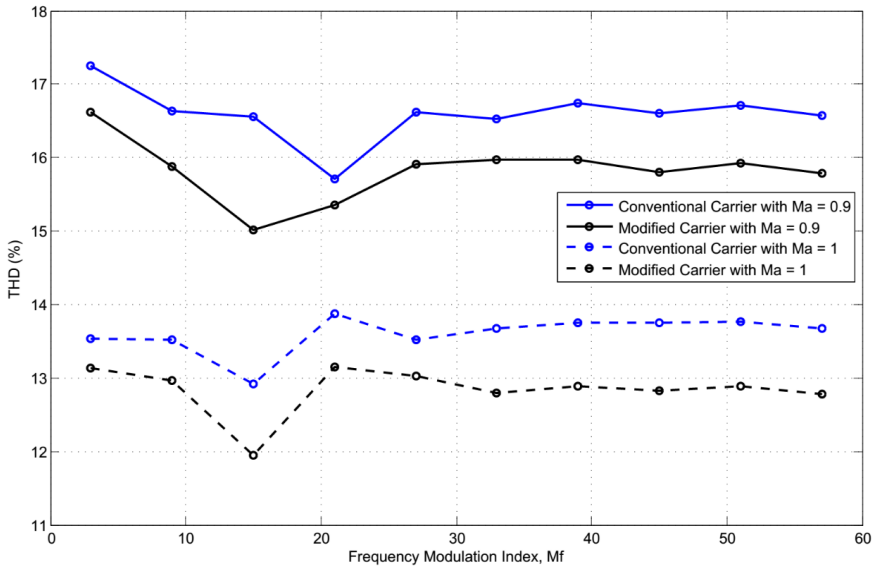

Figure 5.13 THD vs M_f for Conventional and Modified Carrier Signal (IPD 4-cell)

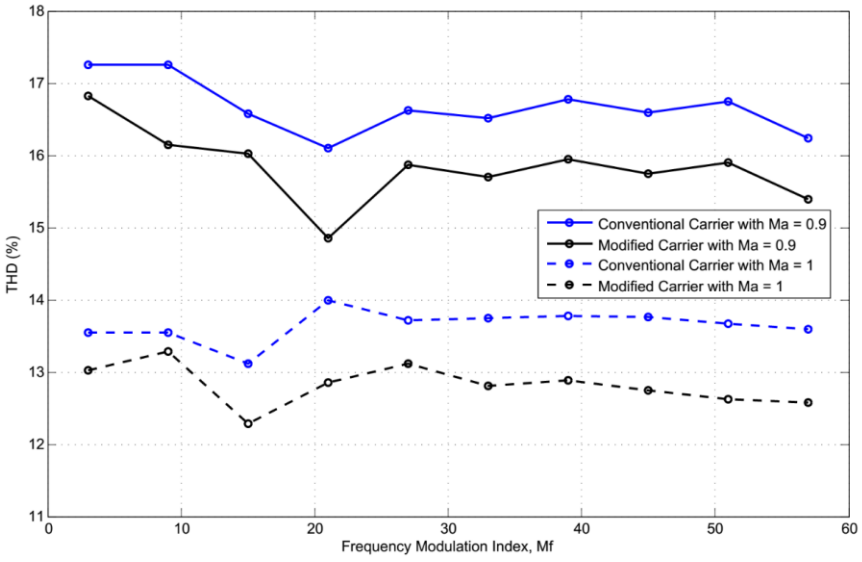

Figure 5.14 THD vs M_f for Conventional and Modified Carrier Signal (POD 4-cell)

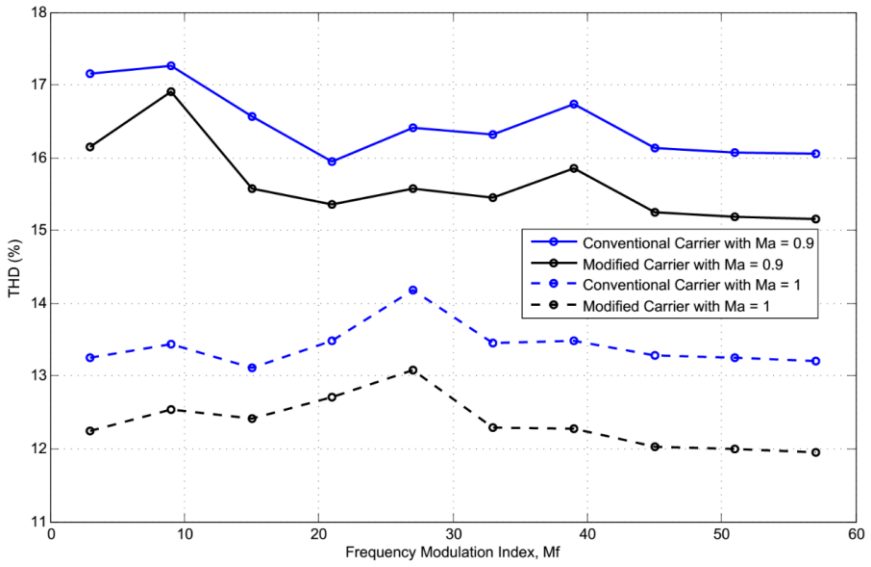

Figure 5.15 THD vs M_f for Conventional and Modified Carrier Signal (APOD 4-cell)

THD for both conventional carrier and modified carrier becomes constant at higher values of M_f, and thus a constant difference occurs in their respective measured THD. Reduction in THD is measured ranging from 0.35-1.54% using modified carrier PWM scheme. For In-Phase Disposition with $M_a = 0.9$, the difference in THD obtained is –0.79% and for $M_a = 1$, it is –0.89%. For Phase Opposition Disposition with $M_a = 0.9$, the difference in THD obtained is –0.85% while for $M_a = 1$, it is –1.02%. For Alternate Phase Opposition Disposition with $M_a = 0.9$, the difference in THD obtained is –0.89% while for $M_a = 1$, it is –1.25%. Numerical data in figures 5.13-5.15 is tabulated in Appendix B.

5.6 Comparative Analysis of PWM Schemes for 6-cell Cascaded H-bridge:

This section compares the performance of 6-cell cascaded H-bridge using conventional and modified carrier signal. For a 6-cell inverter, the limitation of amplitude modulation index is restricted to 0.83 according to (16). The final values for THD are compared with each other to verify effectiveness of modified carrier for 6-cell inverter. Comparison of one cycle of typical output voltage for In-Phase Disposition PWM scheme using (a) conventional carrier and (b) modified carrier appears as shown in figure 5.16

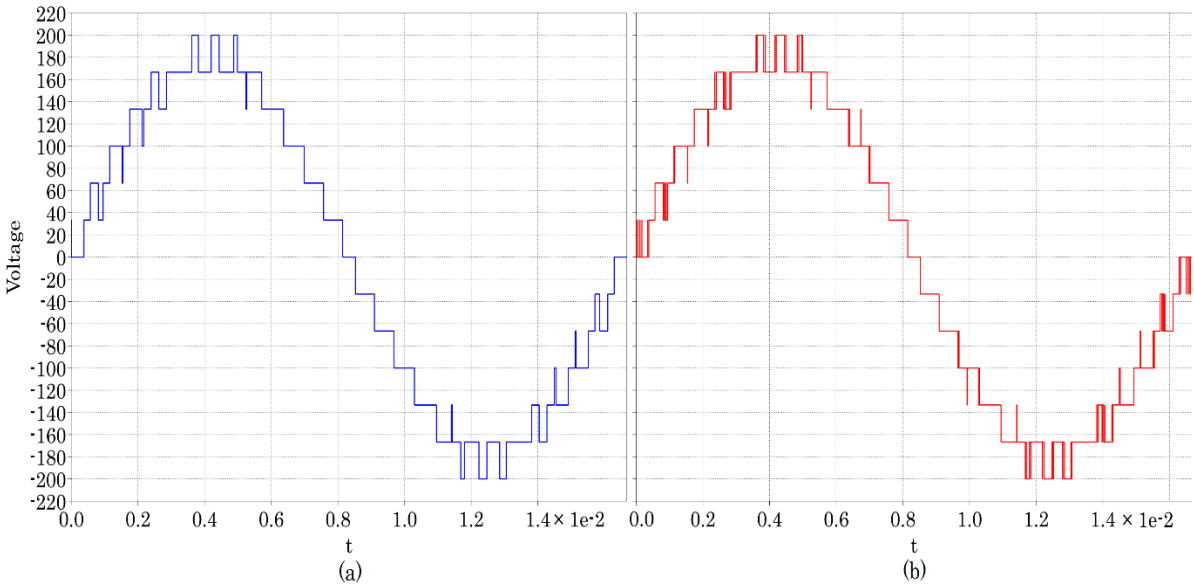

Figure 5.16 6-cell Output Comparison

THD obtained by 6-cell cascaded H-bridge is comparably lower by range of 4-5% than that of 4-cell cascaded H-bridge because of 2 additional voltage levels as seen from figures 5.17-5.19. In relation with SVM interpretation of output voltage, from (18) it can be formulated as,

$$\overline{V_0} = \frac{(T_1 + T_2 + T_3 + T_4 + T_5 + T_6)}{T_{SW}} \overline{V_{dc}} \tag{19}$$

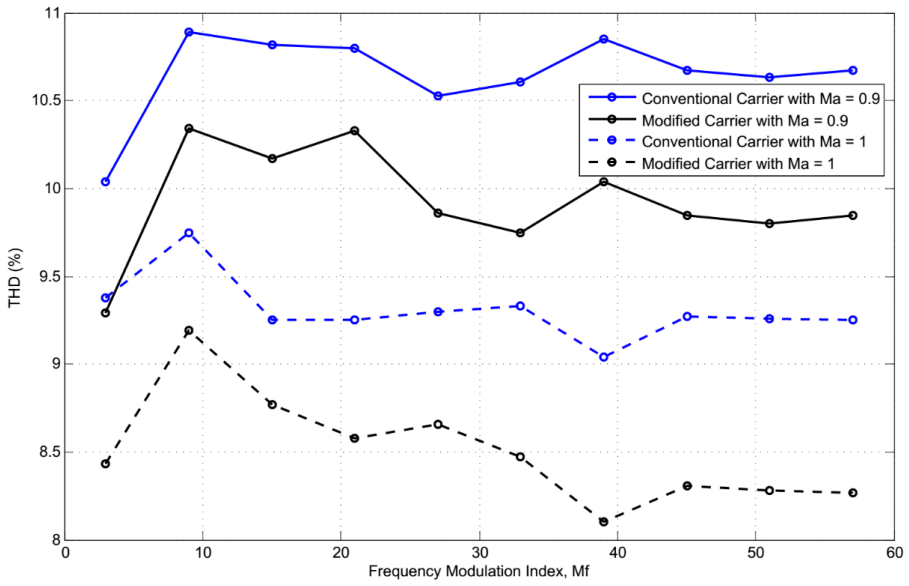

Figure 5.17 THD vs M_f for Conventional and Modified Carrier Signal (IPD 6-cell)

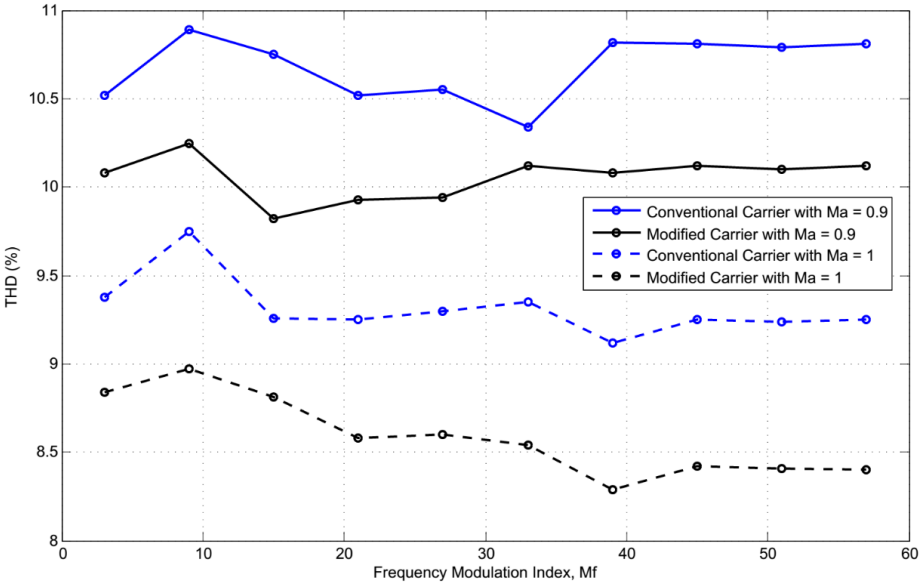

Figure 5.18 THD vs M_f for Conventional and Modified Carrier Signal (POD 6-cell)

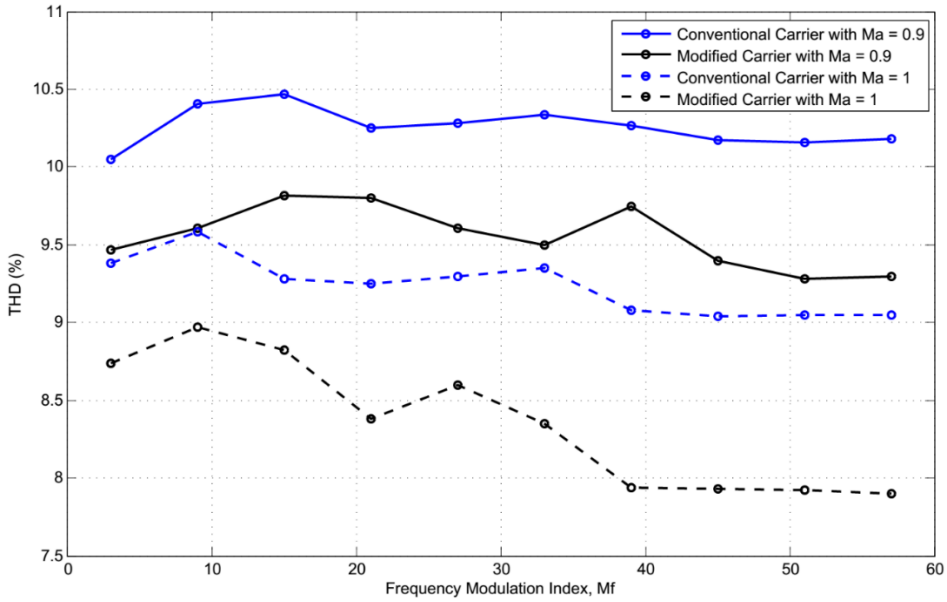

Figure 5.19 THD vs M_f for Conventional and Modified Carrier Signal (APOD 6-cell)

Identical to results for 4-cell cascaded H-bridge, using modified carrier signal for 6-cell also yields reduction in THD of output voltage. THD values are constant for higher frequencies and this higher values of M_f. Reduction in THD is measured ranging from 0.22-1.15% using modified carrier PWM scheme. For In-Phase Disposition with $M_a = 0.9$, the difference in THD obtained is –0.82% and for $M_a = 1$, it is –0.98%. For Phase Opposition Disposition with $M_a = 0.9$, the difference in THD obtained is –0.69% while for $M_a = 1$, it is –0.85%. For Alternate Phase Opposition Disposition with $M_a = 0.9$, the difference in THD obtained is –0.88% while for $M_a = 1$, it is –1.15%. Numerical data in figures above is tabulated in Appendix B.

6. Conclusion

This thesis proposes the modification in conventional carrier signals used to operating cascaded H-bridge with the basis of interpreting level-shifted modulation schemes in terms of Space Vector Modulation (SVM). The theory of proposed modification was successfully tested by running simulations with Simulink and PLECS blockset and measuring THD for variations in amplitude modulation index and frequency modulation index for 4-cell and 6-cell cascaded H-bridge. Harmonic spectrum comparison was done for 4-cell cascaded H-bridge to demonstrate reduction in magnitude of harmonic components. The THD is observed to be reduced in all the cases. One of the major contributions of this method is improvement in THD without increasing carrier frequency and without adding extra voltage levels.

Reduction in THD makes signal easier to filter at the output and also results in lower values of inductors and capacitors (lowered by 10%) to construct LCL power filters which are generally used to filter output from cascaded H-bridge [7]. Drawbacks of the proposed modified carrier signal would be increased frequency of switching of devices with the cost of reduction in THD of signal. Also, the increased frequency might lead to more switching losses in the system.

FUTURE WORK:

Construction of low-voltage prototype of the proposed system and implementing embedded hardware for generation of modified carrier waves.

REFERENCES

[1] Prasad, K.N.V.; Kumar, G.R.; Kiran, T.V.; Narayana, G.S., "Comparison of different topologies of cascaded H-Bridge multilevel inverter," *Computer Communication and Informatics (ICCCI), 2013 International Conference on* , vol., no., pp.1,6, 4-6 Jan. 2013

[2] Veeranna, S.B.; Beig, A.R.; Yaragatti, U.R., "Performance analysis of PWM strategies for cascaded H-bridge three-level inverter," *GCC Conference and Exhibition (GCC), 2011 IEEE* , vol., no., pp.81,84, 19-22 Feb. 2011

[3] Sunder P.G.; Shanthi B.; Nachiappan A.; Natarajan S.P., "Performance Analysis of Modified CHB Multilevel Inverter using Various Carrier Modulation Schemes," *International Journal of Engineering Research and Applications,* vol. 3, Issue 5, pp.310,316, Sep-Oct 2013

[4] Wu B. (2006). High-Power Converters and ac Drives. The Institute of Electrical and Electronics Engineers, Inc., pp.119-142

[5] Bailu Xiao; Filho, F.; Tolbert, L.M., "Single-phase cascaded H-bridge multilevel inverter with nonactive power compensation for grid-connected photovoltaic generators," *Energy Conversion Congress and Exposition (ECCE), 2011 IEEE* , vol., no., pp.2733,2737, 17-22 Sept. 2011

[6] Holmes D.G., Lipo T.A. (2003). *Pulse Width Modulation For Power Converters Principles and Practice.* IEEE Series on Power Engineering, John Wiley & Sons, Inc.

[7] Renzhong X.; Lie X.; Junjun Z.; Jie D., "Design and Research on the LCL Filter in Three-Phase PV Grid-Connected Inverters," *International Journal of Computer and Electrical Engineering*, vol. 5, No. 3, June 2013

[8] Barton T. H., "Pulse Width Modulation Waveforms – The Bessel Approximation," IAS78:40D, pp.1125-1130

[9] Kavitha M.; Arunkumar A.; Gokulnath N.; Arun S., "New Cascaded H-Bridge Multilevel Inverter Topology with Reduced Number of Switches and Sources," *IOSR Journal of Electrical and Electronics Engineering,* vol. 2, issue 6, pp.26-36

[10] Rodriguez, J.; Bernet, S.; Bin Wu; Pontt, J.O.; Kouro, S., "Multilevel Voltage-Source-Converter Topologies for Industrial Medium-Voltage Drives," *Industrial Electronics, IEEE Transactions on* , vol.54, no.6, pp.2930,2945, Dec. 2007.

[11] Villanueva, E.; Correa, P.; Rodriguez, J.; Pacas, M., "Control of a Single-Phase Cascaded H-Bridge Multilevel Inverter for Grid-Connected Photovoltaic Systems," *Industrial Electronics, IEEE Transactions on* , vol.56, no.11, pp.4399,4406, Nov. 2009

[12] P. W. Wheeler, L. Empringham, et al., Improved Output Waveform Quality for Multilevel H-Bridge Chain Converters Using Unequal Cell Voltages, *IEE Power Electronics and Variable Speed Drives Conference,* pp. 536–540, 2000.

[13] Zhong Du; Tolbert, L.M.; Ozpineci, B.; Chiasson, J.N., "Fundamental Frequency Switching Strategies of a Seven-Level Hybrid Cascaded H-Bridge Multilevel Inverter," *Power Electronics, IEEE Transactions on* , vol.24, no.1, pp.25,33, Jan. 2009

[14] Singaravelu T.; Balasubramani M.; Gowrishankar J., "Design and Implementation of Seven Level Cascaded H-Bridge Inverter Using Low Frequency transformer with Single DC Source," *International Journal of Engineering and Technology,* vol. 5, No. 3, pp.3068-3076, Jun-Jul 2013

[15] Jingsheng Liao; Kai Wan; Ferdowsi, M., "Cascaded H-bridge Multilevel Inverters - A Reexamination," *Vehicle Power and Propulsion Conference, 2007. VPPC 2007. IEEE* , vol., no., pp.203,207, 9-12 Sept. 2007

[16] Gobinath K.; Mahendran S.; Gnanambal I.; "New Cascaded H-Bridge Multilevel Inverter with Improved Efficiency," *International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering,* vol. 2, Issue 4, pp.1263-1271, April 2013

[17] G. Carrara; S. Gardella; et al., "A New Multilevel PWM Method: A Theoretical Analysis," *IEEE Transactions on Power Electronics,* Vol. 7, No. 3, pp. 497–505, 1992

[18] J. Chiasson; L Tolbert; et al., "Eliminating Harmonics in a Multilevel Converter Using Resultant Theory," *IEEE Power Electronics Specialists Conference (PESC),* pp. 503-508, 2002.

[19] N. Mohan, T. M. Undeland, et al., *Power Electronics—Converters, Applications and Design,* 3rd edition, John Wiley & Sons, New York, 2003.

APPENDICES

Appendix A

Table A.1 THD values (%) for figure 4.5

M_f	M_a			
	0.75	**0.85**	**0.9**	**1.0**
3	17.81	19.08	17.25	13.54
9	18.90	17.24	16.63	13.52
15	17.91	15.83	16.56	12.92
21	17.48	16.01	15.71	13.88
27	17.43	17.26	16.62	13.52
33	17.80	17.10	16.52	13.67
39	17.61	17.13	16.75	13.75
45	17.70	17.08	16.61	13.75
51	17.76	17.12	16.71	13.77
57	17.65	17.03	16.58	13.67

Table A.2 THD values (%) for figure 4.6

M_f	M_a			
	0.75	**0.85**	**0.9**	**1.0**
3	17.81	18.85	17.26	13.55
9	18.91	17.45	17.26	13.54
15	18.03	15.92	16.57	13.11
21	17.54	16.34	16.10	13.99
27	17.81	17.26	16.62	13.72
33	17.80	17.10	16.52	13.75
39	17.61	17.14	16.78	13.78
45	17.70	17.07	16.59	13.76
51	17.76	17.12	16.74	13.67
57	17.64	17.05	16.24	13.60

Table A.3 THD values (%) for figure 4.7

M_f	M_a			
	0.75	**0.85**	**0.9**	**1.0**
3	17.81	18.74	17.16	13.25
9	18.89	15.48	17.26	13.44
15	18.03	15.92	16.57	13.12
21	17.54	16.45	15.95	13.49
27	17.81	17.07	16.42	14.18
33	17.75	17.04	16.32	13.45
39	17.79	17.41	16.74	13.48
45	17.65	17.07	16.14	13.28
51	17.63	17.13	16.07	13.25
57	17.64	17.12	16.05	13.20

Appendix B

Table B.1 THD values (%) for figure 5.13

M_f	M_a		Change	M_a		Change
	0.9	0.9		1.0	1.0	
	Conventional Carrier	Modified Carrier		Conventional Carrier	Modified Carrier	
3	17.25	16.62	-0.63	13.54	13.14	-0.4
9	16.63	15.88	-0.75	13.52	12.97	-0.55
15	16.56	15.02	-1.54	12.92	11.95	-0.97
21	15.71	15.36	-0.35	13.88	13.15	-0.73
27	16.62	15.91	-0.71	13.52	13.02	-0.5
33	16.52	15.97	-0.55	13.67	12.80	-0.87
39	16.75	15.97	-0.78	13.75	12.89	-0.86
45	16.61	15.81	-0.8	13.75	12.83	-0.92
51	16.71	15.92	-0.79	13.77	12.89	-0.88
57	16.58	15.79	-0.79	13.67	12.78	-0.89

Table B.2 THD values (%) for figure 5.14

M_f	M_a		Change	M_a		Change
	0.9	0.9		1.0	1.0	
	Conventional Carrier	Modified Carrier		Conventional Carrier	Modified Carrier	
3	17.26	16.82	-0.44	13.55	13.02	-0.53
9	17.26	16.15	-1.11	13.54	13.29	-0.25
15	16.57	16.02	-0.55	13.11	12.29	-0.82
21	16.10	14.86	-1.24	13.99	12.85	-1.14
27	16.62	15.87	-0.75	13.72	13.12	-0.6
33	16.52	15.70	-0.82	13.75	12.80	-0.95
39	16.78	15.94	-0.84	13.78	12.89	-0.89
45	16.59	15.74	-0.85	13.76	12.74	-1.02
51	16.74	15.90	-0.84	13.67	12.62	-1.05
57	16.24	15.39	-0.85	13.60	12.58	-1.02

Table B.3 THD values (%) for figure 5.15

M_f	M_a		Change	M_a		Change
	0.9	0.9		1.0	1.0	
	Conventional Carrier	Modified Carrier		Conventional Carrier	Modified Carrier	
3	17.16	16.15	-1.01	13.25	12.25	-1
9	17.26	16.91	-0.35	13.44	12.54	-0.9
15	16.57	15.57	-1	13.12	12.42	-0.7
21	15.95	15.36	-0.59	13.49	12.71	-0.78
27	16.42	15.57	-0.85	14.18	13.08	-1.1
33	16.32	15.45	-0.87	13.45	12.30	-1.15
39	16.74	15.86	-0.88	13.48	12.28	-1.2
45	16.14	15.25	-0.89	13.28	12.03	-1.25
51	16.07	15.19	-0.88	13.25	12.00	-1.25
57	16.05	15.16	-0.89	13.20	11.95	-1.25

Table B.4 THD values (%) for figure 5.17

M_f	M_a		Change	M_a		Change
	0.9	0.9		1.0	1.0	
	Conventional Carrier	Modified Carrier		Conventional Carrier	Modified Carrier	
3	10.04	9.29	-0.75	9.38	8.43	-0.95
9	10.89	10.34	-0.55	9.75	9.19	-0.56
15	10.82	10.17	-0.65	9.25	8.77	-0.48
21	10.80	10.33	-0.47	9.25	8.58	-0.67
27	10.53	9.86	-0.67	9.30	8.66	-0.64
33	10.61	9.75	-0.86	9.33	8.47	-0.86
39	10.85	10.04	-0.81	9.04	8.10	-0.94
45	10.67	9.85	-0.82	9.27	8.31	-0.96
51	10.63	9.80	-0.83	9.26	8.28	-0.98
57	10.67	9.85	-0.82	9.25	8.27	-0.98

Table B.5 THD values (%) for figure 5.18

M_f	M_a		Change	M_a		Change
	0.9	0.9		1.0	1.0	
	Conventional Carrier	Modified Carrier		Conventional Carrier	Modified Carrier	
3	10.52	10.08	-0.44	9.38	8.84	-0.54
9	10.89	10.25	-0.64	9.75	8.97	-0.78
15	10.75	9.82	-0.93	9.26	8.81	-0.45
21	10.52	9.93	-0.59	9.25	8.58	-0.67
27	10.55	9.94	-0.61	9.30	8.60	-0.7
33	10.34	10.12	-0.22	9.35	8.54	-0.81
39	10.82	10.08	-0.74	9.12	8.29	-0.83
45	10.81	10.12	-0.69	9.25	8.42	-0.83
51	10.79	10.10	-0.69	9.24	8.41	-0.83
57	10.81	10.12	-0.69	9.25	8.40	-0.85

Table B.6 THD values (%) for figure 5.19

M_f	M_a		Change	M_a		Change
	0.9	0.9		1.0	1.0	
	Conventional Carrier	Modified Carrier		Conventional Carrier	Modified Carrier	
3	10.05	9.47	-0.58	9.38	8.74	-0.64
9	10.41	9.61	-0.8	9.58	8.97	-0.61
15	10.47	9.82	-0.65	9.28	8.82	-0.46
21	10.25	9.80	-0.45	9.25	8.38	-0.87
27	10.28	9.61	-0.67	9.30	8.60	-0.7
33	10.34	9.50	-0.84	9.35	8.35	-1
39	10.27	9.75	-0.52	9.08	7.94	-1.14
45	10.17	9.40	-0.77	9.04	7.93	-1.11
51	10.16	9.28	-0.88	9.05	7.92	-1.13
57	10.18	9.30	-0.88	9.05	7.90	-1.15