ABSTRACT

GUPTA, SHIVAM. Understanding the behavior of 1200 V SiC MOSFET under Short Circuit and Avalanche operation and Behavior of 1200 V SiC JBS Diode under Avalanche operation. (Under the direction of Dr. Subhashish Bhattacharya.)

SiC MOSFETs are now replacing Si based devices such as Si IGBTs for better efficiency and increased energy density. This work includes the short circuit analysis of 1200 V SiC MOSFET, and Avalanche energy analysis of 1200 V SiC MOSFET and 1200 V SiC JBS Diode. The short circuit results of SiC MOSFETs are compared with Si devices. The test results are also compared with the simulation results. The Short circuit protection scheme for 1200V SiC MOSFET is demonstrated. Switching characterization of 1200V SiC MOSFET has been done to evaluate the switching losses and compare it with a 1200V Si IGBT.

The Single Pulse Avalanche Energy capability of various commercially available 1200V SiC JBS Diodes are compared. The test procedures are explained. The results were obtained by building a hardware setup in the lab.

Understanding the behavior of 1200 V SiC MOSFET under Short Circuit and Avalanche operation and Behavior of 1200 V SiC JBS Diode under Avalanche operation

by
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DEDICATION

To my parents.

BIOGRAPHY

The author was born in Delhi, India. He completed his schooling from Lovely Public Sr. Sec. School, East Delhi, India. He completed his Bachelors degree in Electrical and Electronics Engineering from National Institute of technology, Hamirpur in May 2013. He is currently pursuing Master of Science in Electrical Engineering from North Carolina State University. He is working at FREEDM Systems Center as Graduate Research Assistant. His research is focused on characterization of wide band gap power semiconductor devices.

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Chapter 1

Introduction

1.1 SiC material properties

Silicon was a dominant power semiconductor material for about last five decades. In [1], trends in Semiconductor Power Devices is discused. However, Si-based power devices are approaching their material limits leading to researches in new Power Semiconductor material. Compared to Si, SiC has ten times the dielectric breakdown field strength, three times the bandgap, and three times the thermal conductivity [2] [3]. Both p-type and n-type regions can be formed in SiC which are necessary to fabricate device structures in a semiconductor materials. SiC devices can withstand higher breakdown voltage, have lower resistivity, and can operate at higher temperature. These properties of SiC can be utilized to manufacture high performance power devices. Different polymorphic crystalline structures of SiC exists (more than 170) which are called polytypes e.g., 3C-SiC, 6H-SiC, 4H-SiC. 4H-SiC is the preferred polytype in practical power device manufacturing since large wafers can be made using this material as compared to other polytypes. Table 1.1 summarizes the characteristics of 4H-SiC and 6H-SiC devices in comparison with Si devices [4].

The specific on-resistance of the drift region in a Power Device is related to the critical electric field by the Baliga Figure Of Merit [5] given by the denominator in the right hand side of eqation 1.1. Fig 1.1 shows the variation of Ideal Specific ON resistance with Parallel Plane Breakdown Voltage for Si and SiC. The relation is defined by equations 1.2 and 1.3 [6]. As can be seen from the graph SiC's Ideal Specific ON resistance is about 2000 times less than Si for the same Parallel Plane Breakdown Voltage.

$$R_{on,sp} = \frac{4BV^2}{\varepsilon_s \mu_n E_C^3} \tag{1.1}$$

$$R_{on,sp}(Si - nCh) = 5.93 * 10^{-9} BV_{PP}^{2.5} \tag{1.2}$$

$$R_{on,sp}(SiC - nCh) = 2.97 * 10^{-12} BV_{PP}^{2.5} \tag{1.3}$$

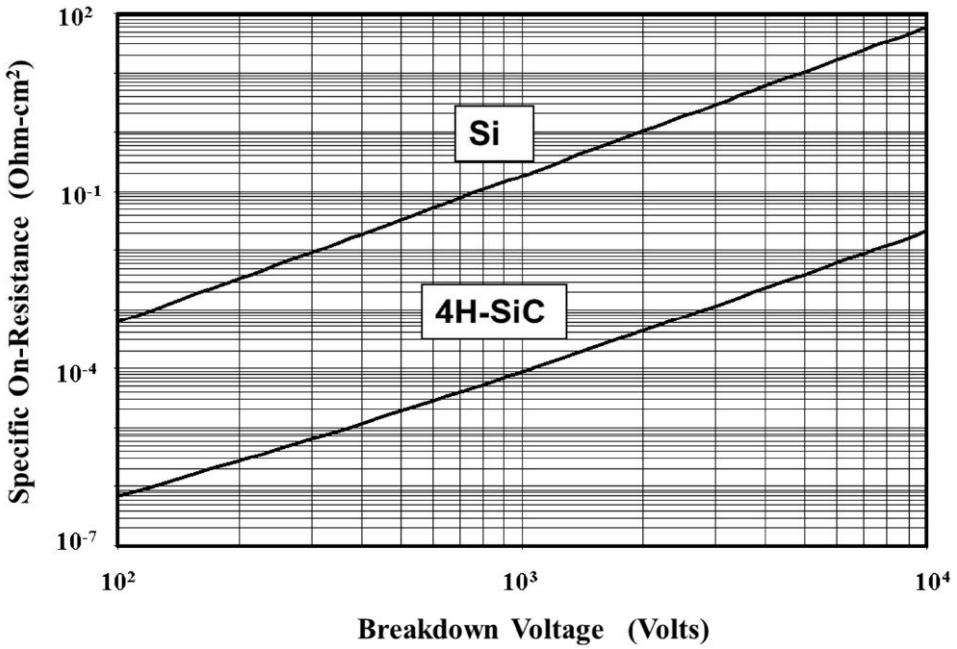


Figure 1.1: Specific ON resistance Comparison between Si and SiC

As the E_C (Critical Electric Field) for SiC is about 10 times greater than Si, the SiC devices can have much lower on-resistances. Also the drift region required is much thinner than the Si devices to support same level of Voltages. The Si IGBT is the most popular Si power device for high voltage and high current applications. Though in the Si IGBTs the on-resistance is very small even at very high voltages (due to minority carriers injection into the drift region during forward conduction), the minority carriers removal (by recombination) during turn off increases the switching losses and limits the switching frequency in Si IGBT. On the other hand SiC MOSFET is a majority carrier device. Thus SiC MOSFET can combine four most desirable characteristics of a power switch, i.e., high voltage, low on-resistance, low switching losses and fast switching speed. Also due to a larger Bandgap it can work at higher operating temperatures (150°C - 175°C), which is mainly limited by the thermal packaging constraints.

Table 1.1: Electrical And Physical Properties of Si and SiC

Property	Si	4H-SiC	6H-SiC
Bandgap, E_g(eV)	1.1	3.3	3
Critical field, E_C(MV/cm)	0.25	2.20	2.50
Electron Saturation velocity, $V_{sat}(10^7$ V/cm)	1.00	2.00	2.00
Electron mobility, $\mu_n(cm^2/\text{Vs})$	1350	947	380
Hole mobility, $\mu_p(cm^2/\text{Vs})$	480	120	80
Dielectric constant, ε_r	11.80	9.70	9.70
Thermal Conductivity, κ(W/cmK)	1.50	5.00	5.00
Melting point(°C)	1420	2830	2830

1.2 SiC Devices structures and working principle

1.2.1 SiC VD-MOSFET

Fig. 1.2 shows the cross section of an NPN SiC MOSFET structure. An n-channel is formed in the p-body when a positive bias is applied to the Gate (G). Electrons then flow from n^+ Source (S) to n^+ Drain (D) through the drift region (consisting regions A, B and C). The MOSFET blocks voltage by forming a depletion layer between p-body and n-drift region when a Zero or negative bias is applied to the Gate (G).

The Vertical D-MOSFET's ON resistance is mainly the sum of Channel resistance, Accumulation region resistance, JFET region resistance, Drift region resistance and Substrate resistance. As compared to Si VD-MOSFET (where the Drift region resistance is the main component), the channel resistance in SiC MOSFET is higher and can be dominating term in long channel devices.

Due to the larger Band Gap of SiC material, higher Gate bias (Gate voltage) is required to produce inversion layer and therefore the threshold voltage is very high for SiC MOSFET, defined by eq. 1.4. Lower Doping of p-base can decrease the threshold voltage but the depletion layer will extend in the p-base and can cause a reach-through breakdown. In Chapter-3, concept of Shielded Planar SiC MOSFET is explained in which a P^+ shielding layer is introduced just below the p-base to suppress reach-through. Also an Accumulation Channel device (ACCUFET) can be made by using an N-base region to improve the channel mobility.

$$V_{TH} = \frac{\sqrt{4\varepsilon_S kTN_A ln(N_A/n_i)}}{C_{ox}} + \frac{2kT}{q} ln\left(\frac{N_A}{n_i}\right) \tag{1.4}$$

The SiC VD-MOSFET structure also consists of an integral P-i-N body Diode. This diode operates in the third quadrant (of Operation) and is useful in certain applications. For fast switching, the parasitic Capacitances has to be charged and discharged quickly. This can be accomplished by a Gate Driver with higher output current rating and a negative Gate bias during turn off.

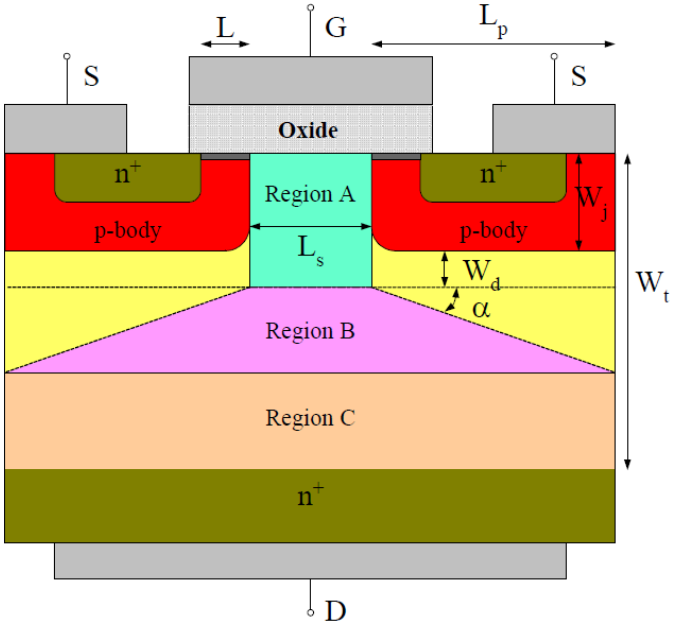


Figure 1.2: SiC MOSFET structure

1.2.2 SiC Junction Barrier Schottky Rectifier (JBS)

The conduction power loss in Schottky Junction Rectifiers is optimized against the leakage power loss by adjusting the schottky barrier height [5]. When Schottky Barrier height is reduced, forward voltage drop decreases leading to smaller conduction loss. At the same time, reverse leakage current increases more rapidly with the increase of blocking voltage. Apart from that the leakage current in SiC Schottky Rectifiers increases by a factor of 10^6 times due to Schottky Barrier lowering and Tunneling due to high electric fields in SiC. This makes SiC Junction Barrier Schottky Rectifier (JBS) more viable, as compared to both SiC P-i-N and SiC Schottky Rectifiers, due to their lower forward drop during conduction mode (compared to P-i-N) and

lower leakage current during blocking mode (compared to Schottky Rectifier). Leakage current in SiC JBS rectifier during blocking mode is given by eq. 1.5

$$J_L = \left(\frac{p-s}{p}\right) AT^2 * exp\left(\frac{-q\phi_b}{kT}\right) * exp\left(\frac{q\Delta\phi_{bJBS}}{kT}\right) * exp\left(C_T E_{JBS}^2\right) \tag{1.5}$$

$$\Delta\phi_{bJBS} = \sqrt{\frac{qE_{JBS}}{4\pi\varepsilon_s}} \tag{1.6}$$

Fig. 1.3 [6] shows the cross section of SiC JBS rectifier structure. The JBS Rectifier is designed such that the on-state current flows between the undepleted $P^+ - N^-$ junction with unipolar current transport mechanism. In the blocking mode the depletion region extends from the P-N junction to the region under the Schottky contact producing a potential barrier under Schottky contact which reduces electric field at the Schottky contact, reducing the leakage current at high voltages.

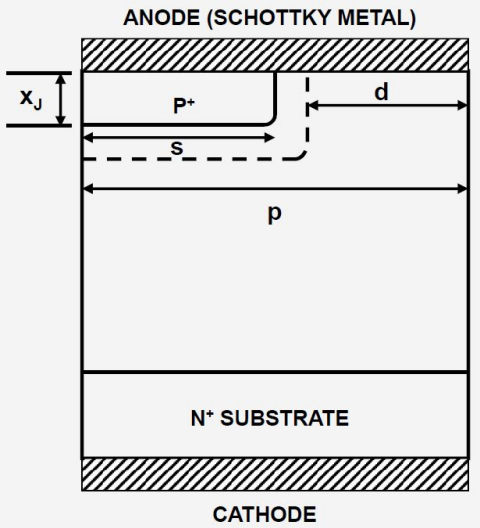


Figure 1.3: Junction Barrier Schottky Rectifier structure

1.3 Motivation

SiC Power devices are getting more practical and sufficiently available after years of research on device physics and manufacturing technology. Though there are some research on the SiC devices reliability issues but still much more attention is needed in regards of behavioral analysis of these devices (especially 1200V SiC MOSFET and 1200V SiC JBS Rectifiers) under Avalanche conditions. Also as the SiC devices make their way to market, applications such as Automotive and Energy distribution networks, more efforts are required to be put into application related issues such as Short-Circuit faults. The protection against these faults is a key issue for designers. The SiC devices are needed to be thoroughly characterized for abnormal operations such as Short Circuit and Avalanche operation.

The work presented in this thesis will help researchers and designers in assessing the Short Circuit design limits of commercially available 1200V SiC devices and will highlight technology improvement requirements for improving the Short Circuit withstand capability of SiC MOSFET. Based on results obtained a short Circuit protection scheme will also be described and demonstrated for 1200V SiC MOSFET.

The analysis of 1200V SiC MOSFETs and 1200V SiC JBS Rectifiers under Avalanche operation is crucial for certain Automotive and high speed applications. A highly rugged characteristics of SiC Devices will open a door for many novel applications.

1.4 Organization of Thesis

In chapter 2, the Gate Driver design for the 1200V SiC MOSFET is described. This Gate Driver with fault protection capability is used throughout the work. The test procedures for the Switching losses characterization is discussed and the experimental results obtained is quantified.

In chapter 3, Power devices Short Circuit behavior is analyzed. In this chapter the Short Circuit results for different Si and SiC devices are compared and short circuit results for 1200V SiC MOSFET is analyzed in detail. Also the Short Circuit protection scheme for the 1200V SiC MOSFETs is described.

In chapter 4, SiC MOSFET Avalanche Energy behavior is analyzed, 1200V and 900V SiC MOSFETs are characterized for Avalanche Energy ratings. The Avalanche Energy test setup and procedures are described and the obtained test results are explained.

In chapter 5, SiC JBS Avalanche Energy behavior is analyzed. The test setup for the 1200V SiC JBS Diode Avalanche Energy characterization is described and various commercially available 1200V JBS Diodes are characterized and compared. Potential applications for a rugged SiC JBS Rectifiers are also discussed.

Chapter 6 concludes the research work, summarizing and discussing all the obtained results and future scope for research based on this work is discussed.

Chapter 2

Gate Driver Design and Switching Losses Characterization

2.1 Gate Driver Design

A Gate driver is designed in CADENCE ALLEGRO PCB Editor for the 1200V SiC MOSFET using Opto-coupler IC HCPL-316J. The designed Gate driver has high peak current output, over-current fault protection and wide Gate output voltage range [7]. Following are the key Gate Driver specs:

1. Minimum differential supply voltage swing is 20-29 V. SiC MOSFETs require a higher positive gate drive voltage (+20 V) and, depending on the application, a negative OFF gate voltage in the -2 V to -6 V range. The maximum supply voltage rating of the driver is 30 V.
2. High peak output current upto 15 A maximum (using a current buffer circuit)
3. Wide operation temperature range
4. 1 MHz maximum switching speed
5. dV/dt transient immunity of 15 kV/us
6. Fault Protection (UVLO and Over-Load)

This Gate Driver is used in the tests described in the proceeding sections.

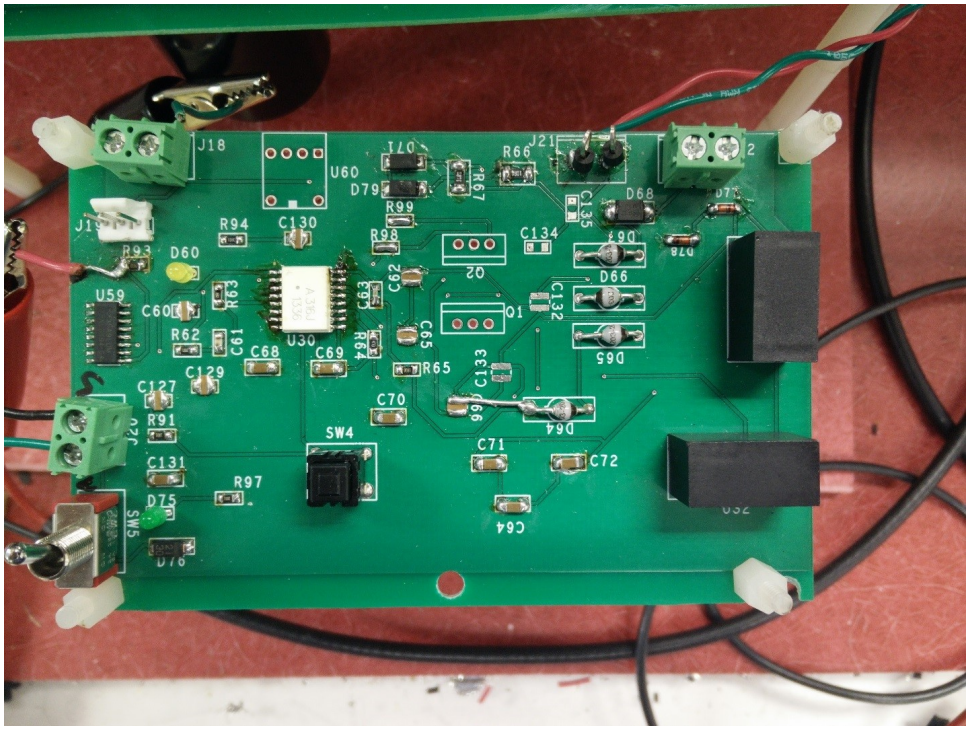


Figure 2.1: SiC MOSFET Gate Driver PCB

2.1.1 Short-Circuit fault detection and Protection

The most important feature of the Gate Driver is its capability of Short-Circuit fault detection and protection. The Principle of fault detection and protection is as follows:

When the DESAT pin sees a Voltage greater than 7 V while the MOSFET is ON, Vout is slowly brought low for the Soft-turn off of the MOSFET and prevent large di/dt induced voltage in the circuit. The $\overline{FAULT}$ output also turns low as the fault notification. The reset circuit is implemented to bring the $\overline{FAULT}$ output to normal again.

The DESAT blanking time is given following the turn-on of MOSFET to allow Drain to source voltage to fall below DESAT threshold i.e. 7 V and avoid spurious triggering of fault protection. This time period is calculated as:

$$\begin{aligned} T_{blank} &= C_{blank} * V_{DESAT}/I_{Charging} \\ V_{DESAT} &= 7V \\ I_{Charging} &= 250uA \end{aligned} \tag{2.1}$$

The value of blanking Capacitor can be selected for the optimum blanking time. The design value chosen for the Gate Driver is 50 pF to give the $T_{blank} = 1.4us$.

The fig. 2.2 illustrates input and output waveforms under the conditions of normal operation, a DESAT fault condition, and normal RESET behavior. During normal operation, Vout is controlled by either Vin+ or Vin-. When the voltage on the DESAT pin exceeds 7V while the MOSFET is ON, Vout is slowly brought low in order to softly turn-off the MOSFET and prevent large di/dt induced voltages. Also an internal feedback channel is activated which brings the $\overline{FAULT}$ output low, which lights up the $\overline{FAULT}$ LED. The $\overline{RESET}$ is then brought low by either a control signal from micro-controller or by a $\overline{RESET}$ switch, to reset the $\overline{FAULT}$ and bring it back to normal state.

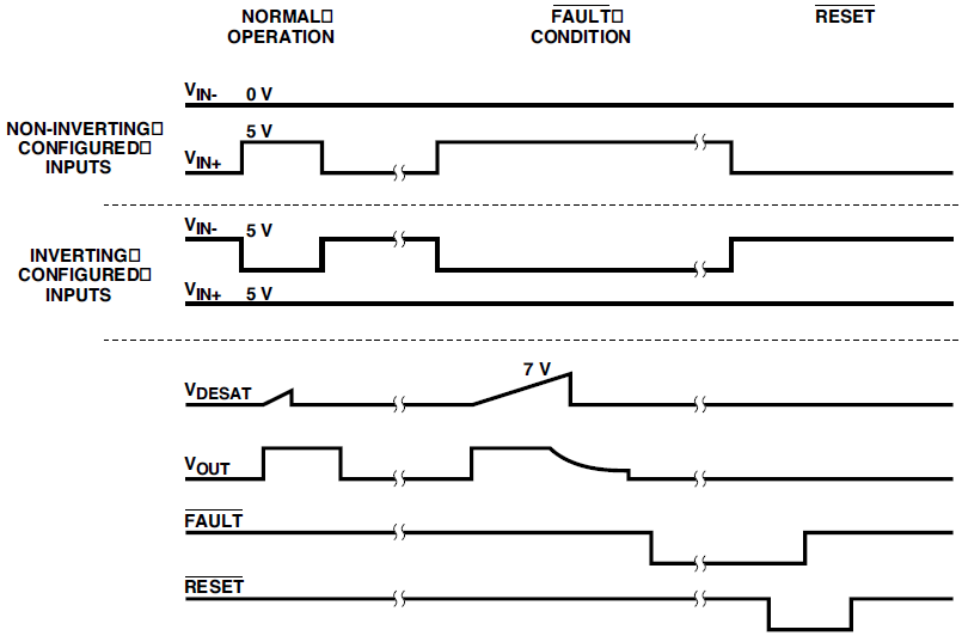
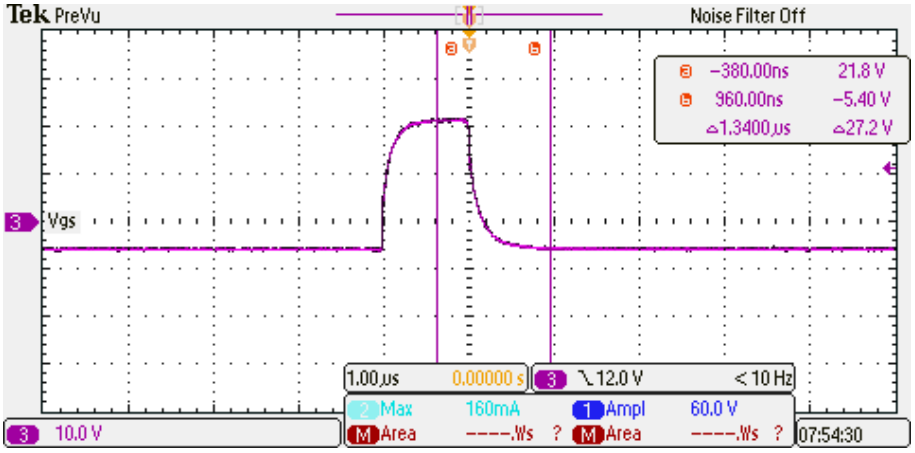


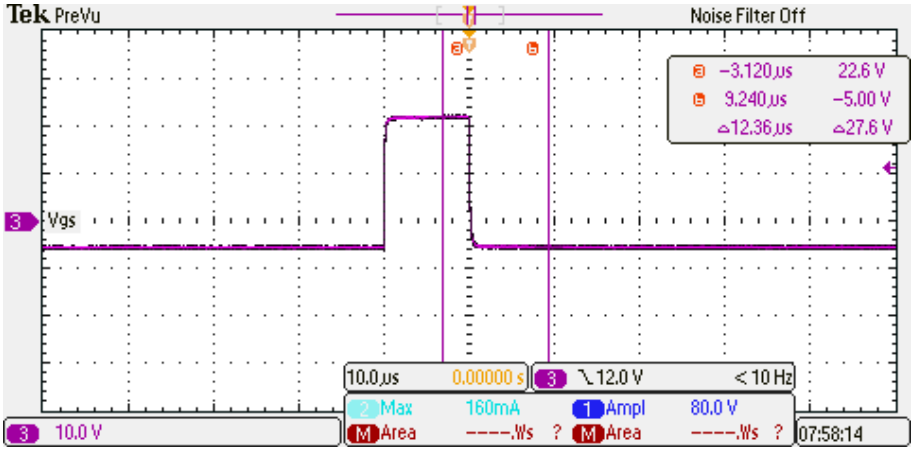
Figure 2.2: DESAT fault protection typical waveforms

2.1.2 Gate Driver Output waveforms

Some typical Gate driver output voltage waveforms are shown in fig. 2.3. Due to propagation delay and the rise time of the Gate Driver output voltage, the Gate driver ouput voltage waveforms are slightly distorted at very high frequency 2.3(a). The Gate driver output at 100kHz frequency has very small distortion. The Switching frequency used in this work is in the range of 100Hz to 1MHz.



(a) Gate Driver Output at 1MHz



(b) Gate Driver Output at 100kHz

Figure 2.3: Gate Driver Output Waveforms

2.2 Switching Losses Characterization

2.2.1 Double Pulse Test setup

Switching losses are evaluated using the inductive load Double pulse test setup [8]. A double pulse is given to the DUT and the V_{DS} and I_D transients at the end of first pulse and at the beginning of the second pulse are recorded. This gives the Turn-OFF and Turn-ON losses respectively. As only two pluses are given during a test, the device junction temperature rise due to the switching losses is minimized. The rise and fall time of V_{GS} is controlled by the gate resistance which in turn controls the di/dt of the switch.

The Keysight 33522A 30 MHz signal generator is used to generate the Gate pulses. The Gate driver used is described in section 2.1. The Double pulse test setup is fabricated on a PCB and an air-core inductor of value 380 uH is used. A 1200V SiC JBS diode is used as a freewheeling diode which have negligible reverse recovery effect, thus limiting the current spike of the DUT during turn-on process. Switching energy losses are evaluated by capturing V_{GS}, V_{DS} and I_D waveforms. Fig. 2.4 shows the overall setup.

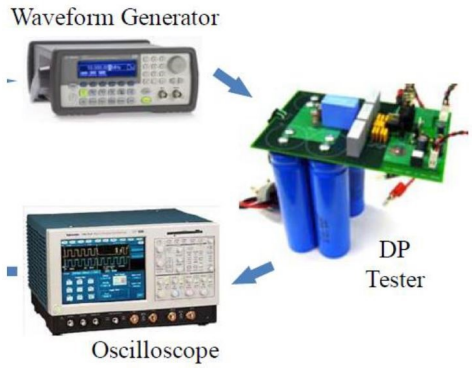


Figure 2.4: Double Pulse Test Setup

The rise and fall time of Vds and Id as in seen the fig. 2.8 and fig. 2.9 is around 20 ns. So, according to the signal theory, the effective bandwidth of a slope signal with a rise time tr can be expressed as $f_{BW} = 0.35/t_r$ [9] thus the bandwidth for the voltage probe and current probe should be above 90MHz (keeping a five times margin). The TEKTRONIX THDP0100 2500 V 100 MHz Differential Voltage Probe is used for measuring V_{DS} and a high bandwidth $PEARSON^{TM}$ current monitor is used for measuring I_D.

2.2.2 Switching Waveforms

Fig. 2.5 shows the basic circuit of double pulse test. The current in the inductor is ramped up by switching ON the DUT. The eq. 2.2 gives the relation of the Inductor current with time and voltage. When the desired load current value is reached, the DUT is turned OFF giving the TURN OFF losses in the DUT as shown in fig. 2.6. Then the DUT is turned ON after a very short duration which gives TURN ON losses at the required load current.

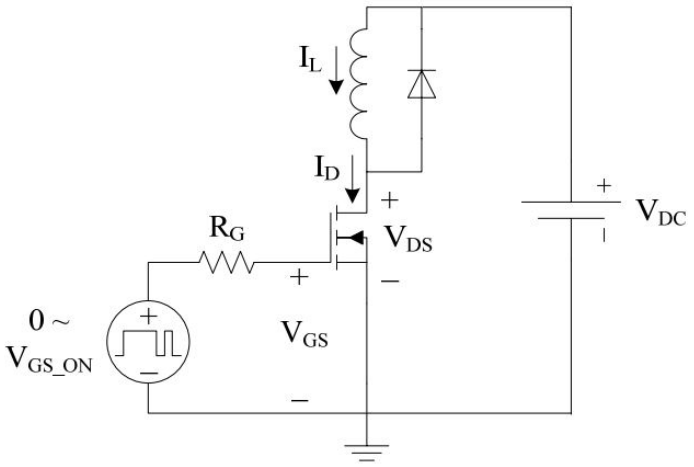


Figure 2.5: Ideal Clamped inductive load Switching circuit

$$V_{DS} = L * \frac{di}{dt} \tag{2.2}$$

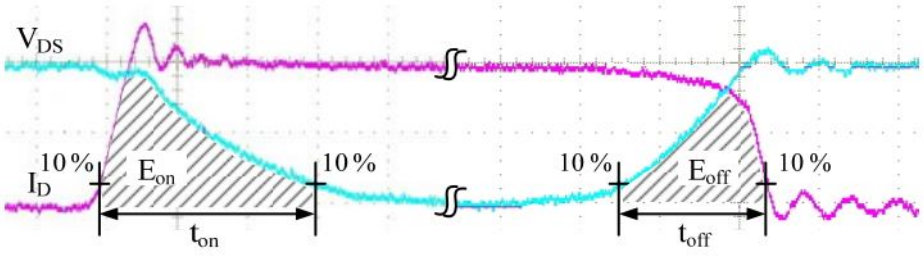
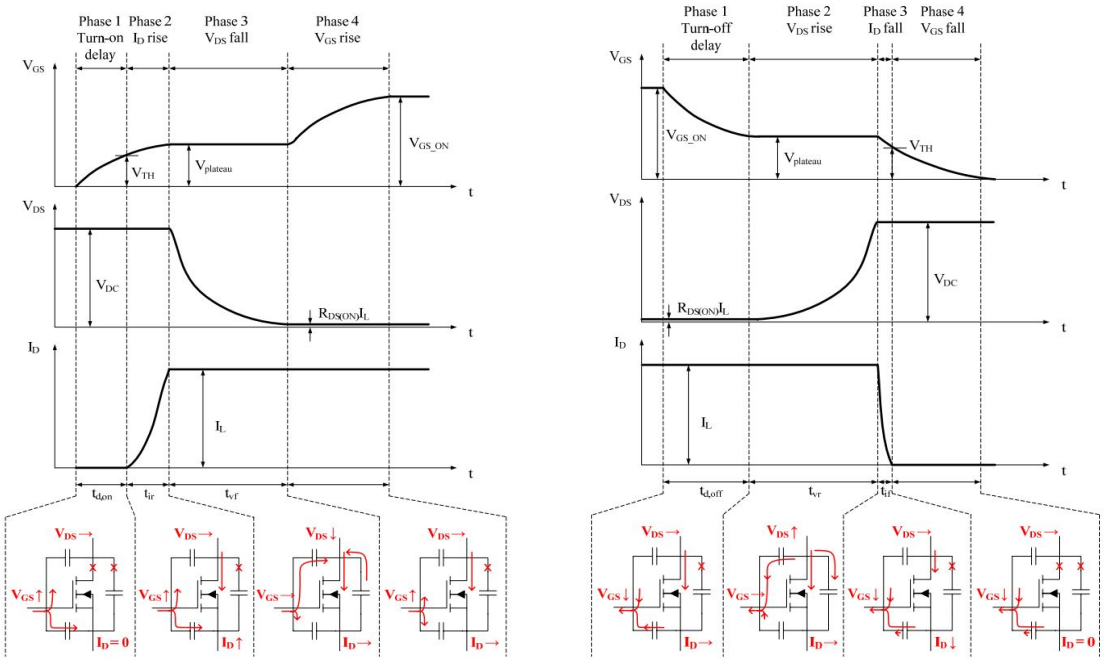


Figure 2.6: Definitions of switching times and energies

Following Ideal conditions are assumed while explaining the MOSFET Switching behavior:

1. The freewheeling diode is ideal, without junction capacitance and forward voltage drop
2. The load inductor current remains constant during the switching process
3. There is no parasitic inductance from either device packages or the circuit
4. The gate driver is an ideal step voltage source. The on-state level is V_{GSon} and the off-state level is zero

The general operation of MOSFET under clamped inductive load is described in [10] [11] [12] [8] and can be sketched into different phases as shown in fig. 2.7.



(a) Turn ON Switching Waveforms

(b) Turn OFF Switching Waveforms

Figure 2.7: General Switching Operation of a MOSFET

2.2.3 Test Results

Fig. 2.8 and fig. 2.9 show a typical switching waveforms at $V_{DS} = 600V$ obtained during testing in the LAB. The PINK waveform is the V_{GS}, the NAVY BLUE Waveform is the V_{DS} and the LIGHT BLUE Waveform is the I_D. The RED waveform gives the Power loss waveform during switching and the area under the RED waveform gives the approximate Switching energy loss.

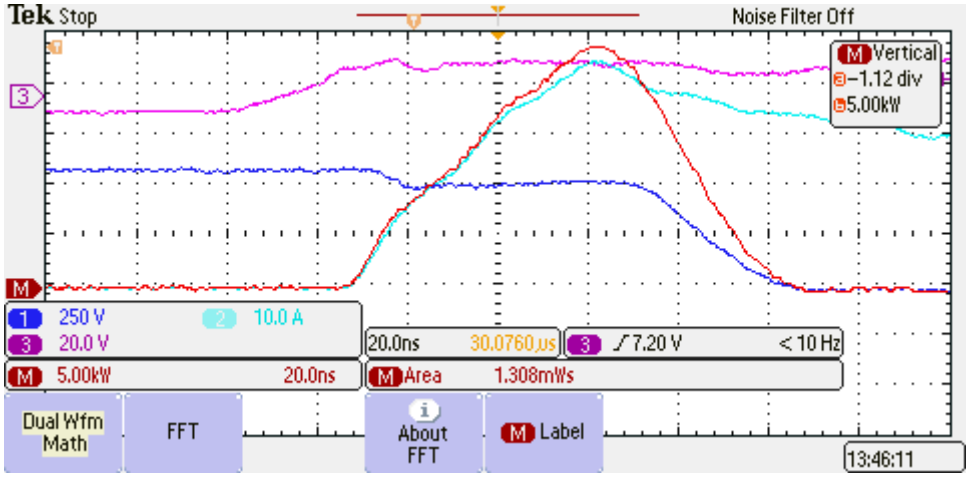


Figure 2.8: Turn ON Switching Waveforms at $V_{DD} = 600V$ and $I_D = 30A$

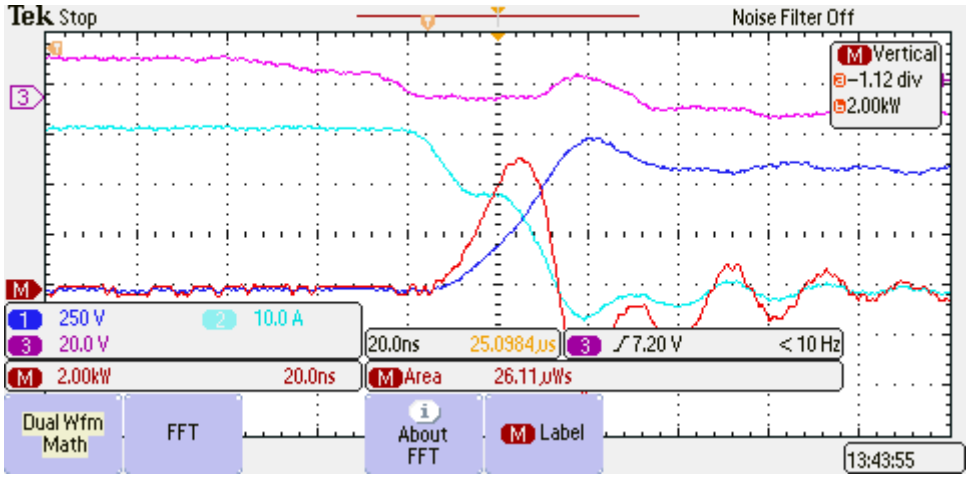


Figure 2.9: Turn OFF Switching Waveforms at $V_{DD} = 600V$ and $I_D = 30A$

The Double Pulse tests are carried out on a 1200V SiC MOSFET, at different V_{DS} for various load currents I_D and the results are plotted as shown in fig. 2.10 and fig. 2.11. Clearly Switching losses increases with I_D as well as V_{DS}. It should be noted that the external Gate resistance used in these tests is limited to $R_G = 10\Omega$. Though lowering the Gate resistance would have improved the switching time and decreased the switching losses but the high di/dt imposes high voltage strain on the DUT due to parasitic Inductance.

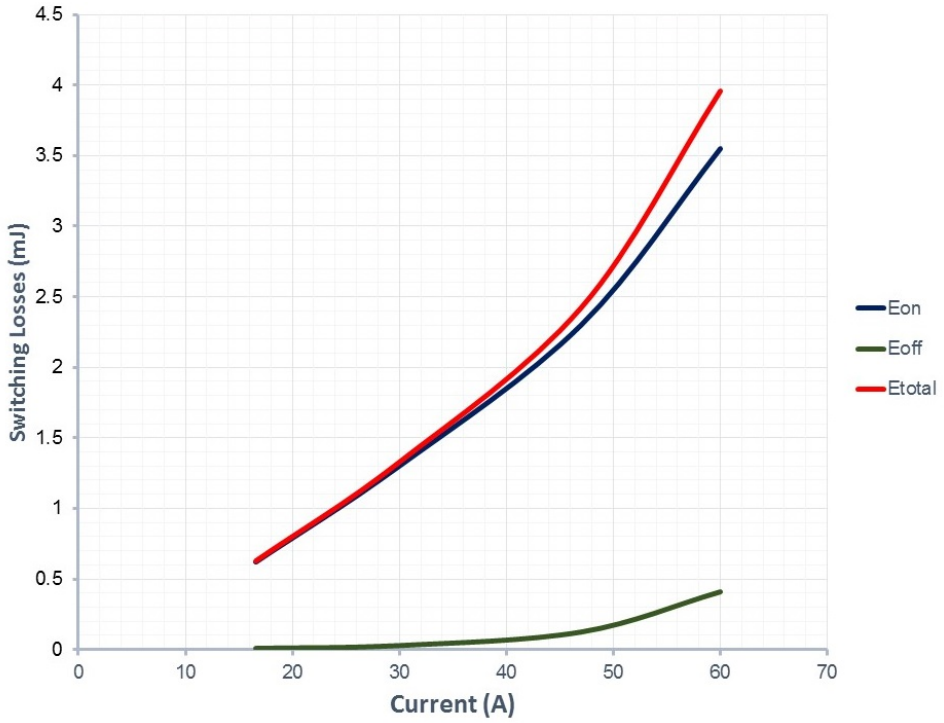


Figure 2.10: Inductive Switching Losses of 1200V SiC MOSFET at $V_{DD} = 600V$

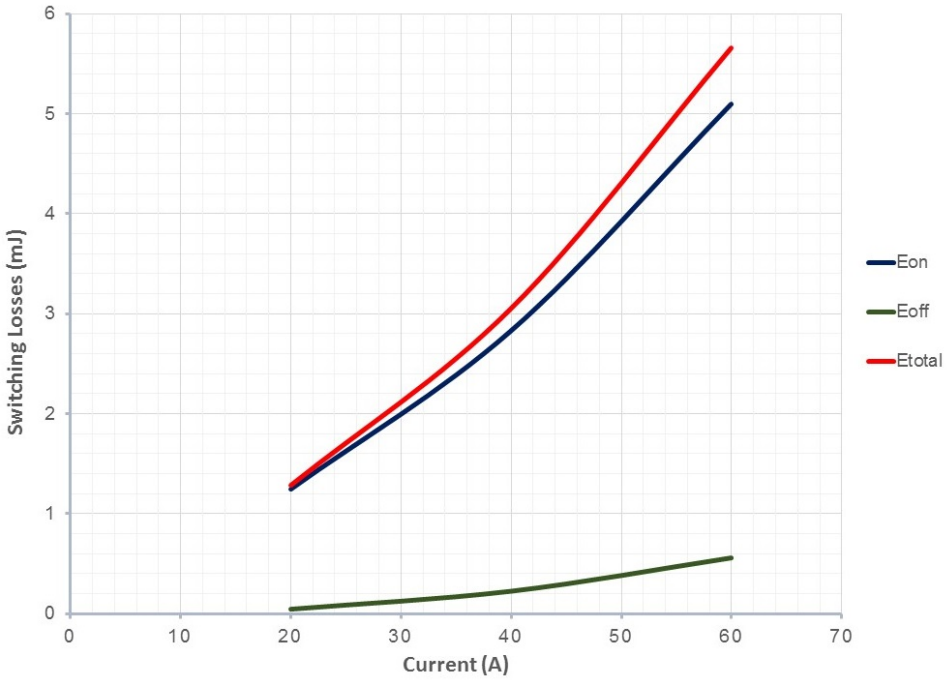


Figure 2.11: Inductive Switching Losses of 1200V SiC MOSFET at $V_{DD} = 800V$

2.2.4 Conclusion

The switching results obtained are in complaint to the theoretical analysis done in section 2.2.2. The Total switching losses of a FAIRCHILD SEMICONDUCTOR 1200V NPT IGBT [13] is around 3.5mJ at Collector current of 40 A, $V_{DS} = 600V$ and $R_G = 5\Omega$ whereas the 1200V SiC MOSFET's total switching Losses is about 2 mJ for the same collector current and V_{DS}. Thus the switching losses are about half of conventional Si IGBT. Using lower R_G value will decrease the switching losses further for the SiC MOSFETs.

Chapter 3

Short Circuit Characterization

3.1 Theoretical Analysis

Short Circuit is a common fault that occurs in a Power system. The shorting of motor-drive windings due to winding insulation failure is an example [14]. During short circuit the Switches in the converter experience a very high current (limited by their saturation current I_{Dsat}) and a high Drain-Source voltage, thus a large amount of energy is being dissipated in the Device and depending on the device characteristics, it fails in certain amount of time.

The short circuit withstand capability of the Switching device plays an important role in detection and protection of the power circuit from fault. If the short circuit withstand capability is high enough then the switching device can be shut off before it fails protecting the switch and the circuit from failure. The fig. 3.1 depicts the circuit when the device is under short circuit. The Device Under Test (DUT) is supplied a voltage V_{DS} from a DC power source while the Gate is at a positive bias V_{GS}.

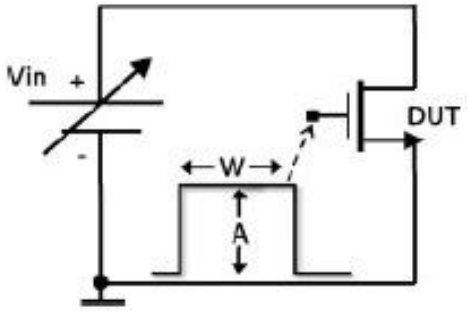


Figure 3.1: Short Circuit Equivalent Test Circuit

The Saturation current in the MOSFET is defined by eq. 3.1:

$$I_D = \frac{1}{2} * \mu * C_{ox} * \{\frac{W}{L}\} * (V_{GS} - V_{TH})^2 \tag{3.1}$$

In saturation region, the current I_D in the MOSFET is mainly dependent on channel resistance. The channel mobility (μ) increases with temperature but the V_{TH} decreases [5] [15] [16]. At lower temperatures the decrease in V_{TH} is determining factor in current increase and at higher temperature the channel mobility plays crucial role. The operating point of the device i.e the V_{DS}, temperature (T) and V_{GS} determine which term will dominate, such as shown below in fig. 3.2, the curve with the V_{DS} of 400V has negative current slope whereas with V_{DS} of 120V the current has only a positive slope. This is due to a critical temperature reached in the 400V case after which the channel mobility decreases and hence the current decreases. The critical temperature as reported in some text [15] [17] is around 600 K, upto which the mobility increases.

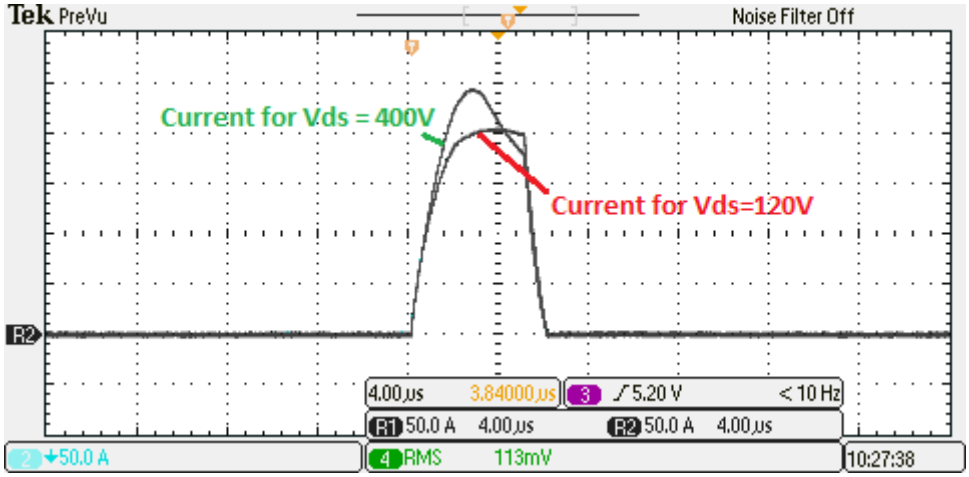


Figure 3.2: Saturation Current at $V_{DS} = 120V$ and $V_{DS} = 400V$

The negative slope is helpful in stabilizing the circuit as it breaks the positive feedback loop and decreases the current. Thus this is a desirable behavior which decreases the rate of increase in temperature during Short Circuit and extends the Short Circuit withstand period.

3.2 Factors resulting in Device failure during Short Circuit

3.2.1 Thermal Runaway

The thermal runaway temperature in Si and SiC has a large difference [18]. The intrinsic carrier concentration with Temperature in Si and SiC is shown in fig. 3.3.

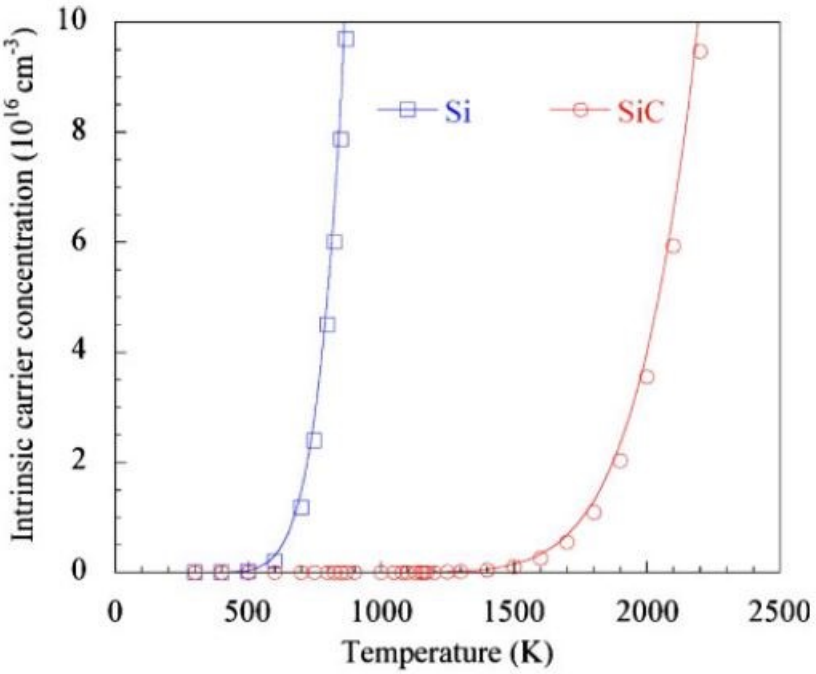


Figure 3.3: Intrinsic Carrier concentration variation with temperature

The intrinsic carrier concentration in Si starts increasing exponentially at 650K as compared to 1500K in SiC. Thus the aluminum contacts having melting point of 933K are expected to melt way before the thermal runaway in SiC thus making it the critical reason of failure of SiC MOSFETS under Short Circuit. The melted metal can diffuse into the device and result in a catastrophic failure. The bond wires (also made of aluminum) are also exposed to thermal stresses and will break in event of failure.

The Short Circuit analysis for IGBTs is done in [5]. The eq. 3.2 and eq 3.3 (accounting the non-uniform temperature distribution in the wafer K_T) gives the short circuit withstand time. These equations are based on the thermal runaway phenomenon (T_{CR}). As discussed above these equation can't be applied directly to SiC MOSFET's short circuit analysis.

$$t_{SCSOA} = \frac{(T_{CR} - T_{HS}) * W_{Si} * C_V}{J_{C,SAT} * V_{CS}} \tag{3.2}$$

$$t_{SCSOA} = \frac{(T_{CR} - T_{HS}) * W_{Si} * C_V}{K_T * J_{C,SAT} * V_{CS}} \tag{3.3}$$

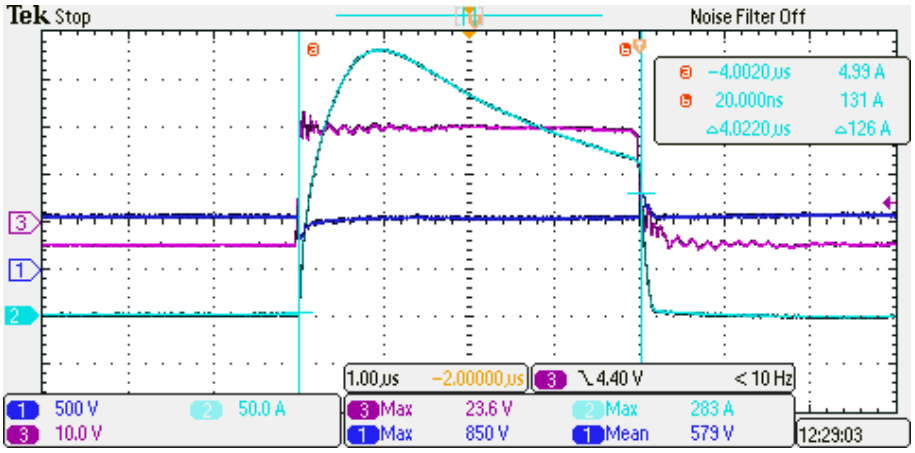
3.2.2 Gate Oxide failure

The Gate Oxide in SiC MOSFETs has been a key issue in device development [19]. As the SiC device's critical electric field is 10 times as that of Si, the electric field imposed on the Gate Oxide can be much higher than that in Si devices 3.4. The critical electric field in SiC is about 2.2 MV/cm which corresponds to 6.6 MV/cm Electric Field in Gate Oxide. This is very high for SiO_2 as the dielctric strength of SiO_2 is about 10 MV/cm [20].

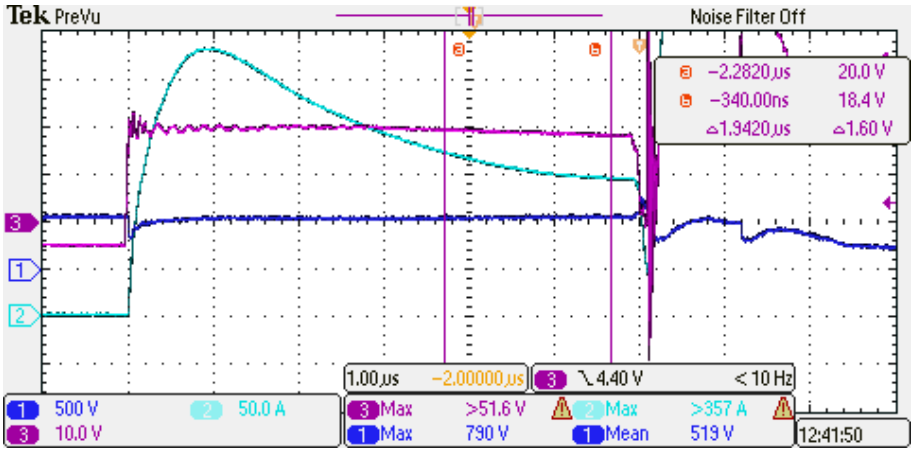
$$E_{oxide} = \frac{\varepsilon_{semi}}{\varepsilon_{oxide}} * E_{semi} \cong 3E_{semi} \tag{3.4}$$

The fig. 3.4 shows the V_{GS} (PINK) measured across the DUT under Short Circuit Test. As can be seen from the waveform (b) the V_{GS} decreases from 20V to 18.4V. This phenomenon is observed in all the short circuit failure waveforms. This can be explained by the degradation of the SiO_2 oxide layer due to high electric field prompting the leakage current through Gate Oxide. This phenomenon becomes more prominent due to the smaller gate thicknesses of SiC MOSFETs, and then triggered by the high-power dissipation from the short-circuit condition, which results in lower reliability of the gate oxide.

Increase in V_{DS} leads to a high electric field at the P-base/N-drift region which causes an increase in the depletion layer thickness in the P-base region. As a result, a reach-through breakdown occurs which causes a large leakage current to flow from the gate-to-source.



(a) DUT under 4us of short circuit stress



(b) DUT under 6us of short circuit stress

Figure 3.4: Gate Oxide Failure

Improving Gate Oxide Reliability

The Shielded Planar MOSFET Structure can be used for improving the gate Oxide Reliability [21] [22] [23]. It contains a sub-surface P^+ shielding region (fig. 3.5). The JFET region becomes depleted by the drain voltage applied and a potential barrier is formed at location A in the blocking mode. Thus the potential barrier formed prevents the electric field from becoming large at the gate oxide interface and at the P-base/N-drift junction.

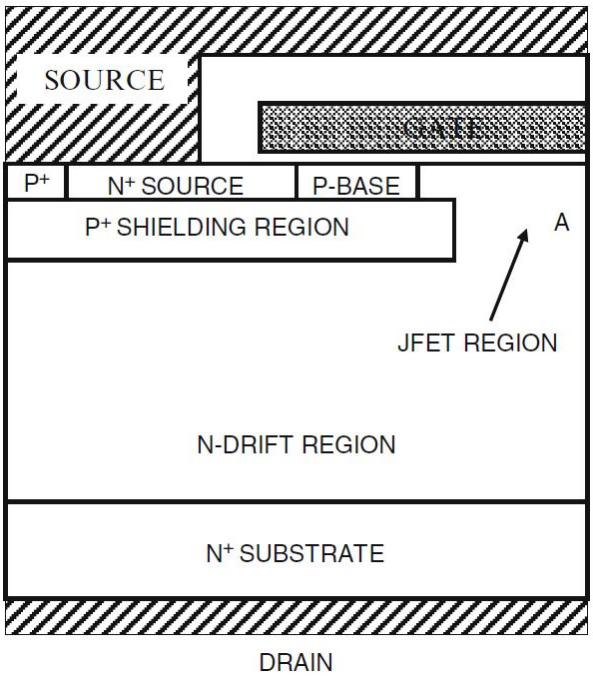


Figure 3.5: Shield Planar SiC MOSFET

3.2.3 Parasitic BJT latch-up

A current tail is observed during the turn off before the device fails as seen in the fig. 3.6. This tail gets longer with the Short Circuit time until the device fails fig. 3.7. This phenomenon can be attributed to the latching of parasitic BJT during turn off [24].

As shown in fig. 3.8 the displacement current caused by the formation of the depletion region (due to reverse biasing of drain-body) at the drain-body diode which is proportional to dv/dt flows in body of the MOSFET during turn off. This current flows in close proximity of Base of the parasitic n-p-n BJT. Thus if this current is large enough or the Base resistance is high, the BJT can become active.

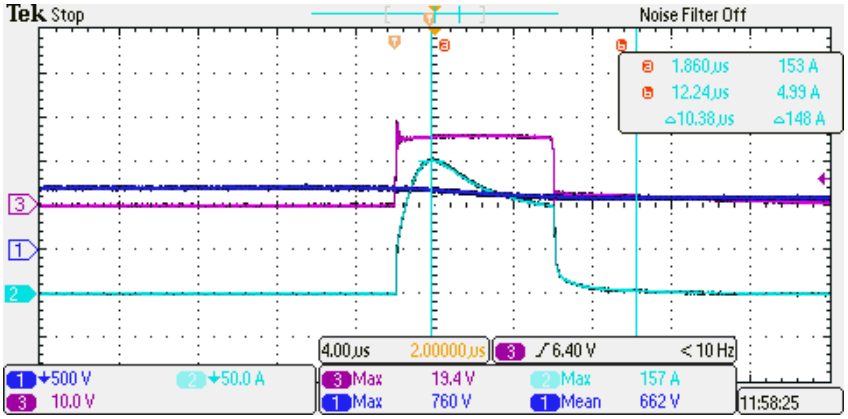


Figure 3.6: Short Circuit Waveform with a current tail

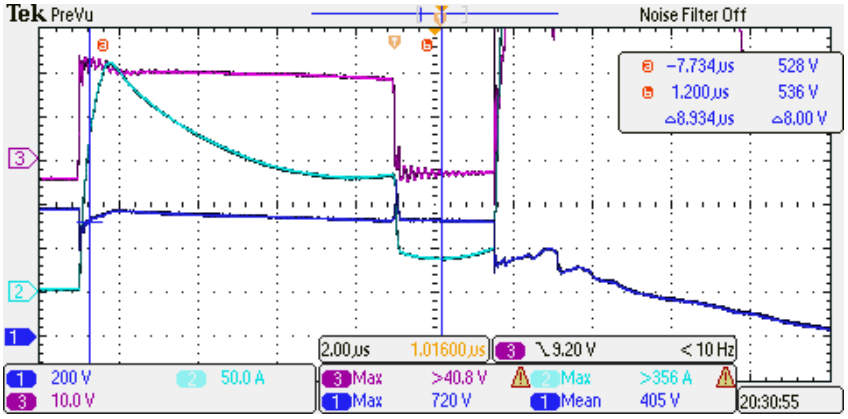


Figure 3.7: Short Circuit Failure Waveform due to a current tail

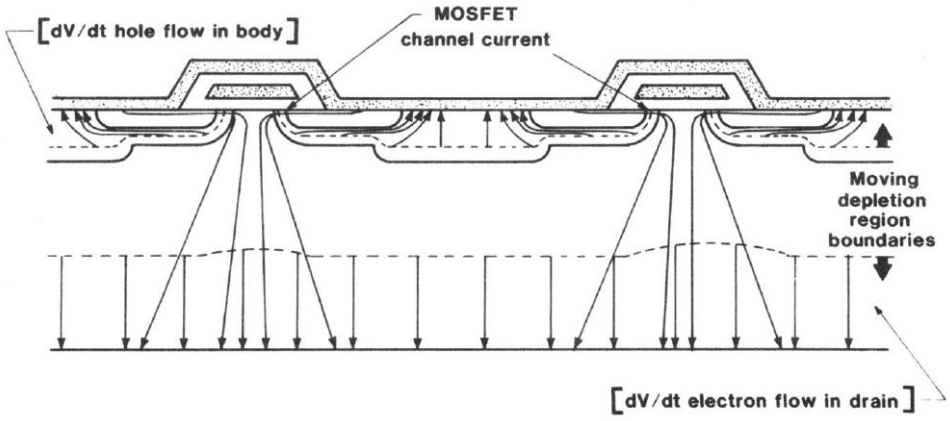


Figure 3.8: Parasitic BJT Latch-up

3.3 Simulation Results

A 1200 V 80$m\Omega$ SiC MOSFET LTspice model was used to simulate the short circuit test. The Simulations done are non Electro-thermal. The schematic used for the short circuit analysis is shown in fig. 3.9. Here CREE C2M0080120D LTspice model is used for the simulations.
Fig. 3.10 shows the short circuit waveforms for different Operating conditions. The peak saturation currents are marked in the figures and is tabulated in Table 3.1.

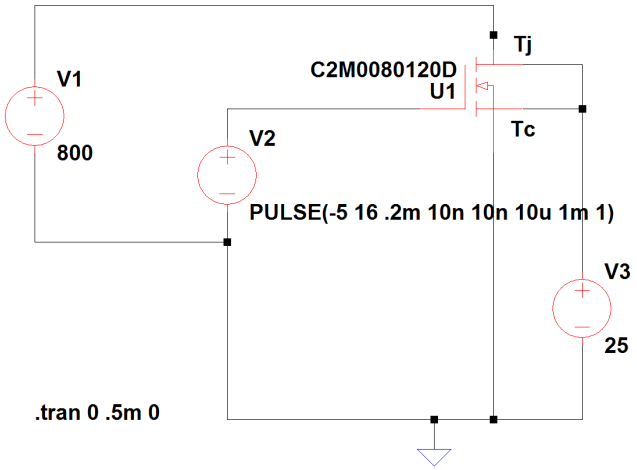


Figure 3.9: Test Schematic in LTspice using CREE C2M0080120D LTspice model

Table 3.1: Peak Saturation Currents of SiC MOSFET under Short Circuit at Different Operating Conditions

Drain to Source Voltage (V_{DS})	$V_{GS} = 16V$	$V_{GS} = 20V$
400V	155A	245A
600V	170A	270A
800V	185A	280A

The Peak Saturation Current values for $V_{GS} = 16V$ closely matches the experimental values obtained in the next section.

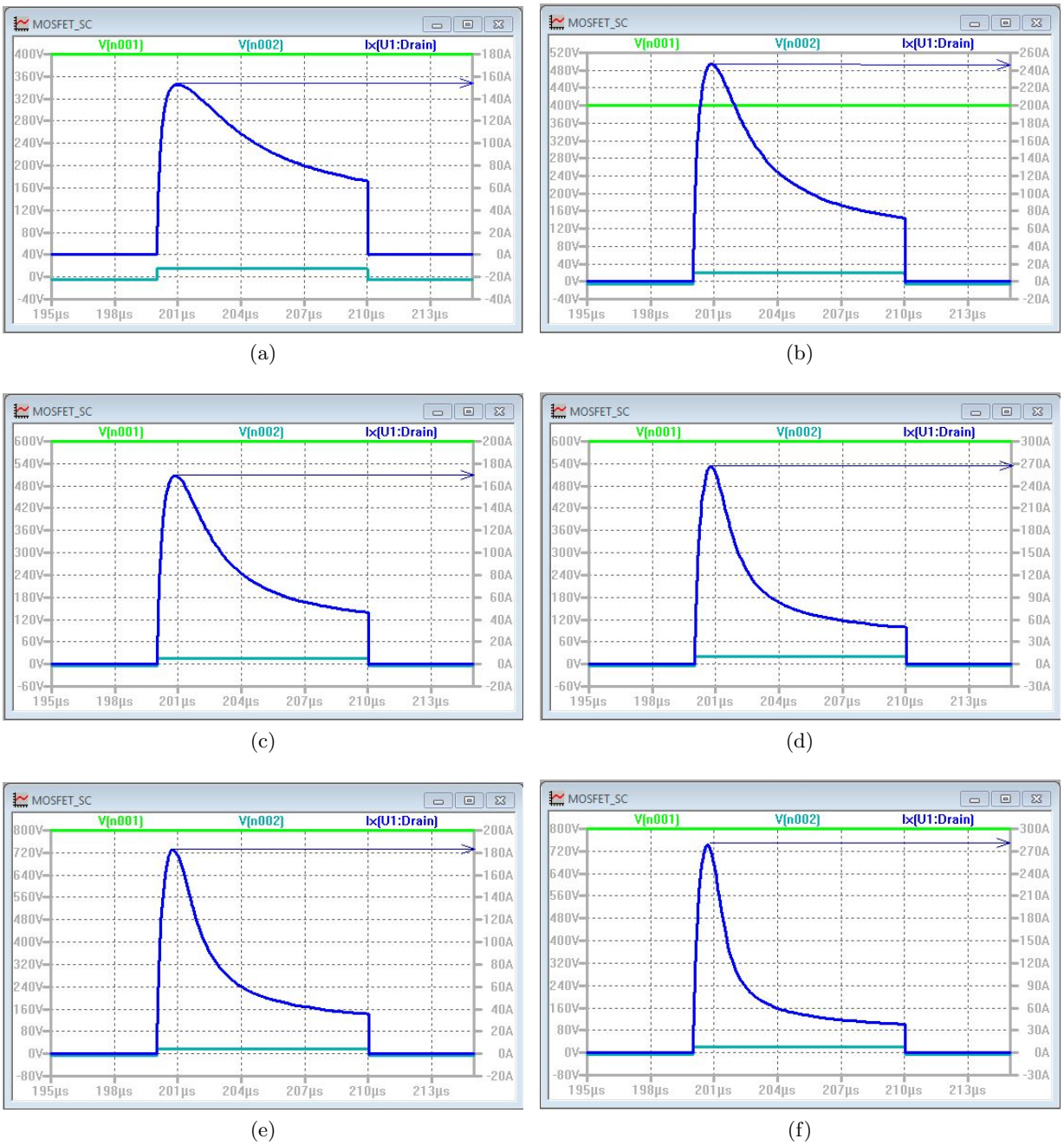


Figure 3.10: Short Circuit Simulations of 1200 V SiC MOSFET: (a) Vds=400 V Vgs=16 V (b) Vds=400 V Vgs=20 V (c) Vds=600 V Vgs=16 V (d) Vds=600 V Vgs=20 V (e) Vds=800 V Vgs=16 V (f) Vds=800 V Vgs=20 V

3.4 Test Results

Comprehensive testing was done to investigate the short circuit behavior of the SiC devices. The devices were tested at various drain-source voltages at different gate voltages to estimate their withstand capability.

Apart from SiC MOSFETs, Si devices are also tested to benchmark SiC MOSFETs against them. At least 3 samples of each devices are tested at Vg=20 V and an average failure rating of each device is presented in the Table 3.2. Fig. 3.11 shows the results of all the samples tested.

Table 3.2: Short Circuit Test Results for the Devices tested

Device Name	Average Failure rating (V_{DS}/Short Circuit time)
MSI Sample-B 1200 V	600 V/7.6 us
CREE C2DM0080120D 1200 V	600 V/6.3 us
IXYS Si IGBT IXYP20N120C3 1200 V	600 V/2 us

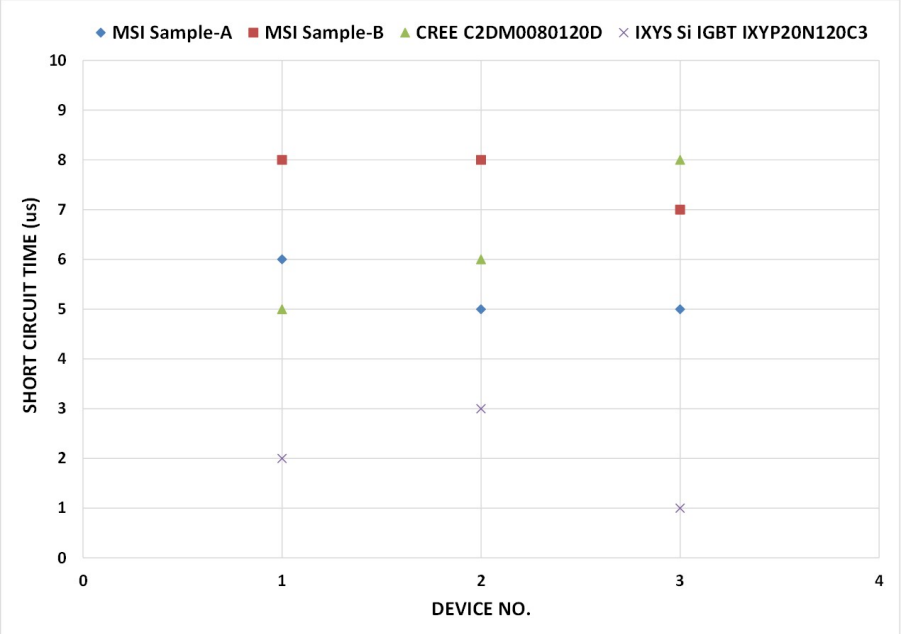


Figure 3.11: Short Circuit Data

3.4.1 Test Setup

Fig. 3.12 shows the test setup assembled in the Lab. Due to explosive nature of the tests, a box was built for protection. The PCB layout was done in CADENCE PCB Editor. The Lab equipments used for the supply and measurement are described below.

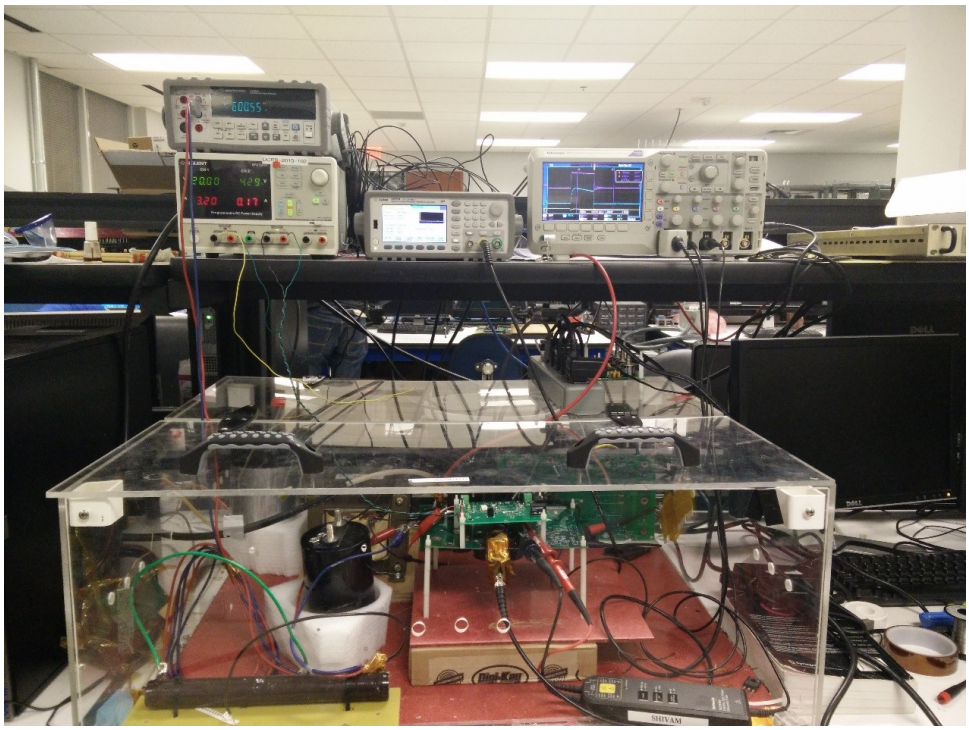


Figure 3.12: Short Circuit Lab Test Setup

Test equipment

1. Test BOX: Due to the explosive nature of the tests a Plexi Glass material is used to build an enclosure for a safety purpose.

2. DC power supplies: Two DC power supplies are used for the tests. A high voltage (6 kV) DC power Supply is used as input voltage source. A low voltage 35 V DC power supply is used for powering Gate Driver.

3. Waveform generator: The Agilent's 33522A 30 MHz Waveform generator is used for generating Gate Driver Pulse

4. Differential Probe: TEKTRONIX THDP0100 100 MHz high voltage differential probe is used for measuring V_{DS}

5. Pearson Cts: A high Bandwidth Pearson CT is used for measuring short circuit current.

6. Oscilloscope: Tektronix DPO 2024B Digital Oscilloscope is used for capturing the output waveforms.

3.4.2 1200V SiC MOSFET Short Circuit Analysis

In this section a detailed Short Circuit analysis of 1200V SiC MOSFET is done and results are plotted. The tests were done to understand the effects of the V_{GS} and V_{DS} variations on the Short Circuit time.

The Short Circuit analysis is done at a fixed $V_{GS} = 16V$ and $V_{GS} = 20V$ to show the variations in the SC withstand capability with drain voltage. Results obtained from the tests are plotted in the fig. 3.13 and fig. 3.14.

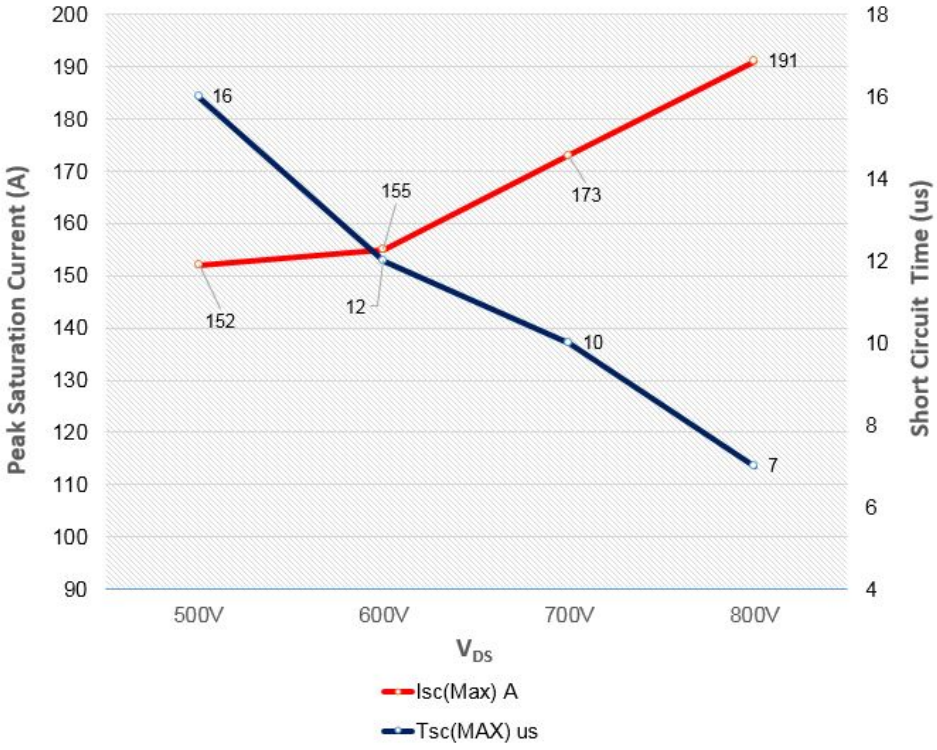


Figure 3.13: Short Circuit Analysis at $V_{GS} = 16V$

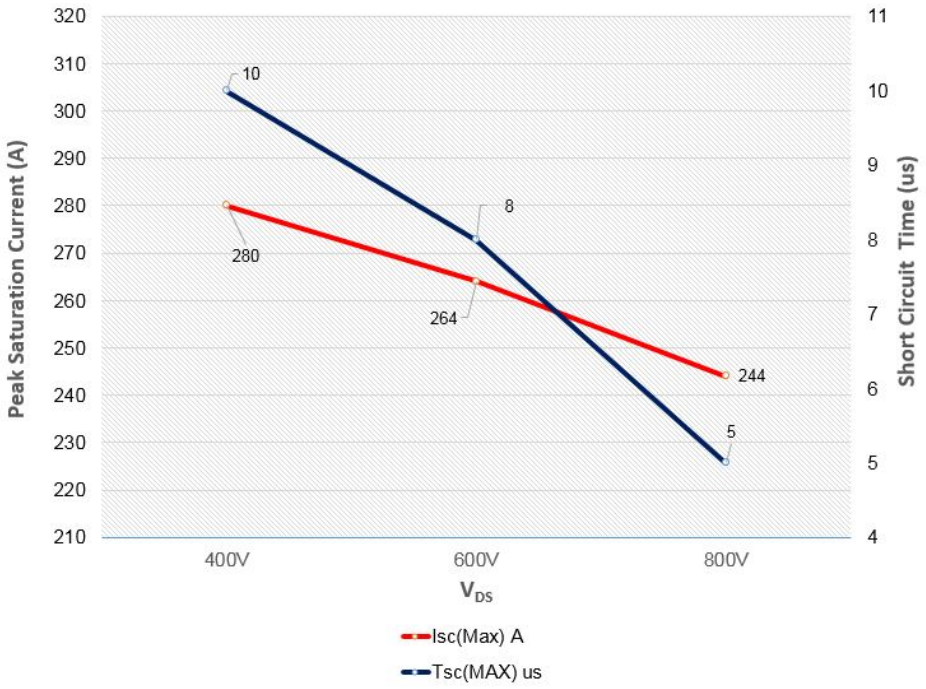


Figure 3.14: Short Circuit Analysis at $V_{GS} = 20V$

As expected the short circuit withstand time decreases with increasing V_{GS} as well as V_{DS}. The peak saturation current is higher for higher V_{GS}. One pattern difference in the fig. 3.13 and fig. 3.14 is the peak saturation current graph. The peak saturation current increases with the V_{DS} for $V_{GS} = 16V$ but it decreases with V_{DS} for $V_{GS} = 20V$. This is because for the higher V_{GS} case the current is mainly dependent on the channel mobility. The channel mobility decreases with increasing temperature (increasing V_{DS}). Thus the peak saturation current decreases.

3.5 Short Circuit Protection

As mentioned in section 2.1.1 an over-current protection circuitry was integrated within the Gate Driver for Short Circuit fault detection and protection. The fig. 3.15 curve shows the typical short circuit protection waveform obtained during the testing of the Gate Driver. The DUT was supplied with 250 V supply voltage and a Gate pulse of 10 us was given. As can be seen from the figure the device current rise upto 1.4 us and then starts falling. This is because of the blanking time of 1.4 us given in the Gate Driver. After the blanking period the Device is softly turned of with low di/dt. Also fig. 3.16 shows the short circuit protection waveform for the case when a blanking time of 2.8 us is given.

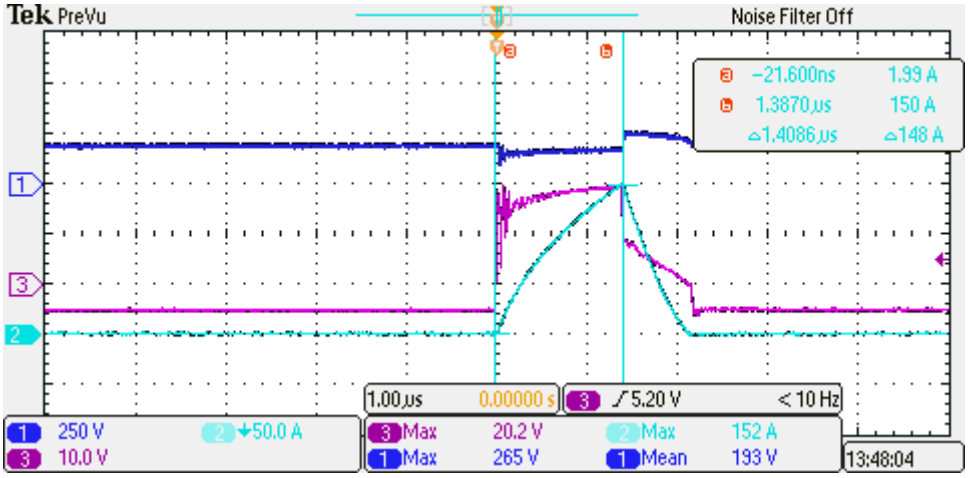


Figure 3.15: Short Circuit protection waveform

Thus the fault detection and protection circuitry works well for the SiC MOSFET under short circuit. Also as most of the devices tested have short circuit withstanding capability of above 4 us, this protection scheme can be applied to any of the devices tested. This scheme has much lower short circuit sensing delay time as compared to other fault detection schemes.

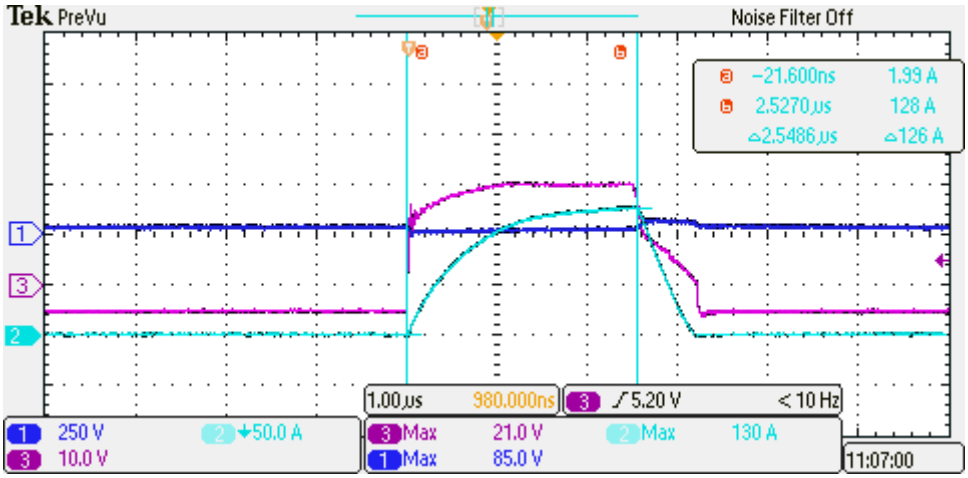


Figure 3.16: Short Circuit protection waveform

Chapter 4

MOSFET Avalanche Characterization

4.1 Avalanche Breakdown

The maximum voltage that can be supported by a power device before the onset of significant current flow is limited by the avalanche breakdown phenomenon [5]. Impact Ionization coefficient is the number of electron-hole pairs generated when a mobile carrier traverse one cm in the direction of the electric field through the depletion region. Impact ionization coefficient becomes infinity during avalanche breakdown. The total number of electron-hole pairs generated in the depletion region by single pair of electron-hole pair at a distance x from the junction is calculated by expression 4.1 where M(x) is multiplication coefficient.

$$M(x) = \frac{e^{\int_0^x (\alpha_n - \alpha_p) dx}}{1 - \int_0^W \alpha_p e^{(\alpha_n - \alpha_p)\, dx}\, dx} \tag{4.1}$$

The avalanche breakdown condition is defined to occur when the total number of electron-hole pairs generated within the depletion region approaches infinity, corresponding to M becoming infinity. Which gives expression 4.2 assuming ionization coefficients for electrons and holes to be equal.

$$\int_0^W \alpha\, dx = 1 \tag{4.2}$$

Thus the Avalanche breakdown is defined to occur when the ionization integral becomes one. The fig. 4.1 shows the impact ionization Coefficients curve for different Semiconductor material [6].

The avalanche energy capability is very important for high speed switching devices because

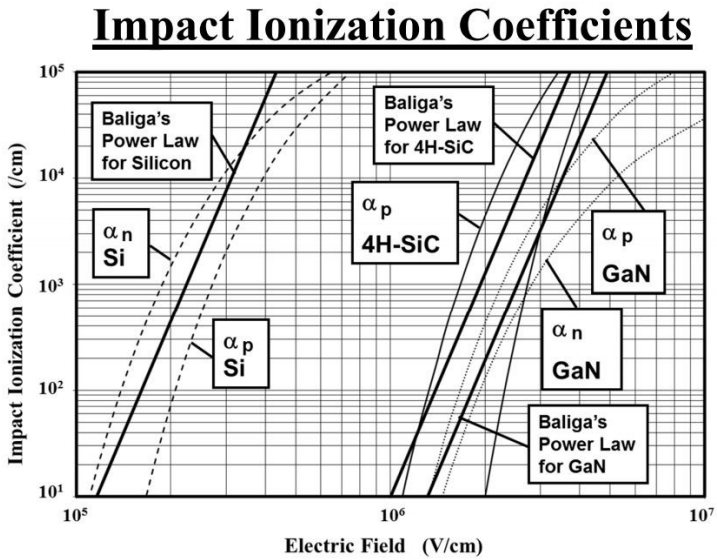


Figure 4.1: Impact Ionization Coefficients

at very high speed, the parasitic inductance can cause high inductive voltage spikes in the circuit. This voltage spike is suppressed by the avalanche breakdown of the switch, and the energy of this event is dissipated in the switching device.

4.2 MOSFET Failure Physics under Avalanche

A parasitic NPN BJT exists in all SiC Power MOSFETs. The p-n junction formed between the Drain and the p+ body no longer blocks voltage in Avalanche. The reverse leakage current increases exponentially with the applied electric field. With higher applied voltage impact ionization coefficient tends to infinity and a critical electric field is reached. The carrier concentration increases due to avalanche multiplication. As the electric field is stronger at bends, the maximum current flows near the base of the parasitic BJT as shown in 4.2 [25]. Also the power dissipation in the base of the NPN BJT increases temperature which increases the Base resistance Rb. Thus when the voltage drop across the base resistance is sufficiently high to forward bias the base-emitter junction the parasitic BJT turns on (latch up) and the MOSFET control is lost.

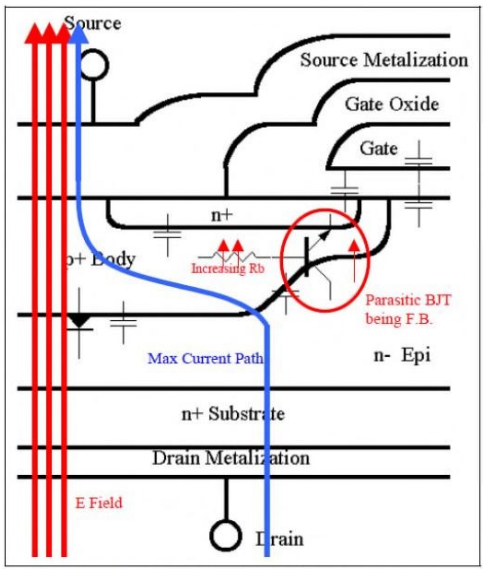


Figure 4.2: Cross-Section of MOSFET depicting current flow during Avalanche

4.3 Avalanche occurrences in Industrial application

4.3.1 Parasitic board inductance

Parasitic board inductance is very common in many applications. The objective is to minimize it but the parasitic inductance can not be fully omitted in the circuit. Thus if the di/dt is very high, a small parasitic inductance can put a high voltage across the MOSFET.

4.3.2 Flyback Converter

As seen in the fig. 4.3 energy is stored in the leakage Inductor when the MOSFET is ON in Flyback converter. The leakage inductance discharges through the MOSFET during MOSFET turn-off if the Inductor is not clamped properly and causes Avalanche breakdown in the MOSFET. The fig. 4.4 shows the Avalanche operation.

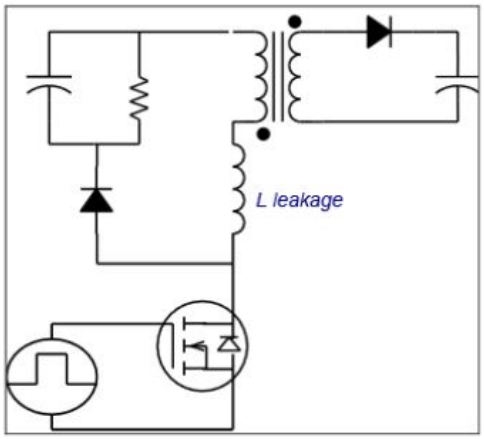


Figure 4.3: Flyback Converter circuit

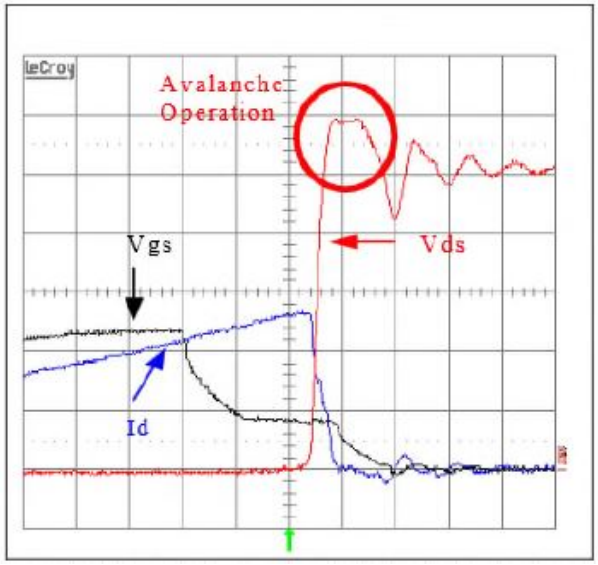


Figure 4.4: Flyback Converter Switch Under Avalanche Waveform

4.3.3 Automotive Injector Coil

In the automotive injector coil circuit such as shown in fig. 4.5, the energy is stored in the Solenoid inductance during MOSFET is ON. As the MOSFET is turned-off the Inductor discharges through the MOSFET causing the MOSFET to operate in the Avalanche.

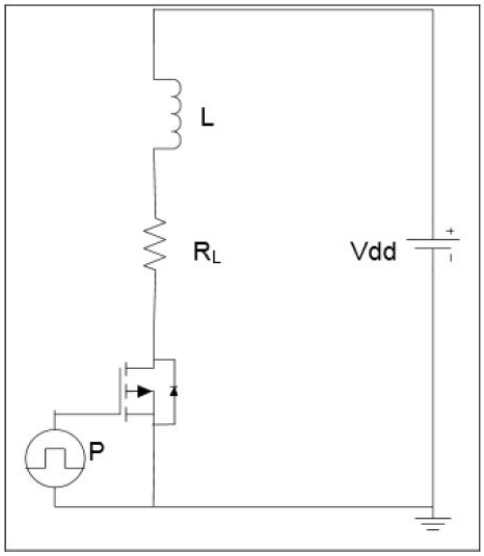


Figure 4.5: Automotive Injector Coil Circuit

4.4 Avalanche Simulations

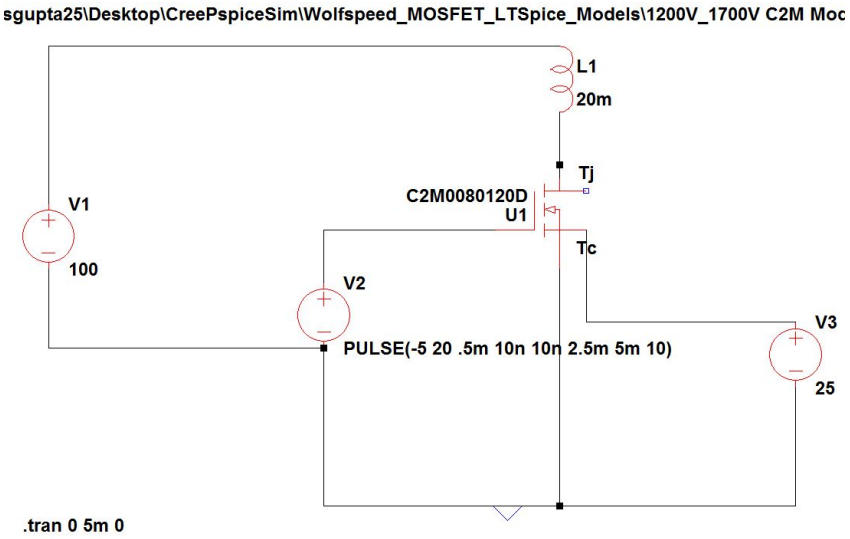


Figure 4.6: Simulation Test Circuit for MOSFET Avalanche Characterization

Avalanche operation Simulations are done in LTSpice for a 1200V SiC MOSFET from CREE. Fig. 4.6 shows the overall simulation circuit. The Simulations done are non Electro-

thermal. The simulations were done for different Avalanche current values. Fig. 4.7 and fig. 4.8 shows the simulation waveforms for 10A and 14 A respectively.

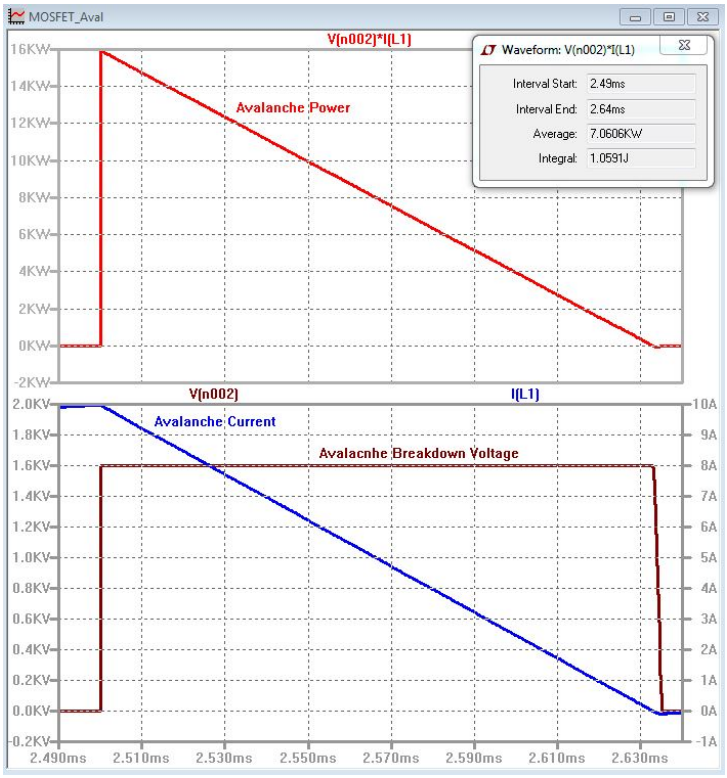


Figure 4.7: 1200V SiC MOSFET Simulation of Avalanche Operation at Avalanche Current of 10A

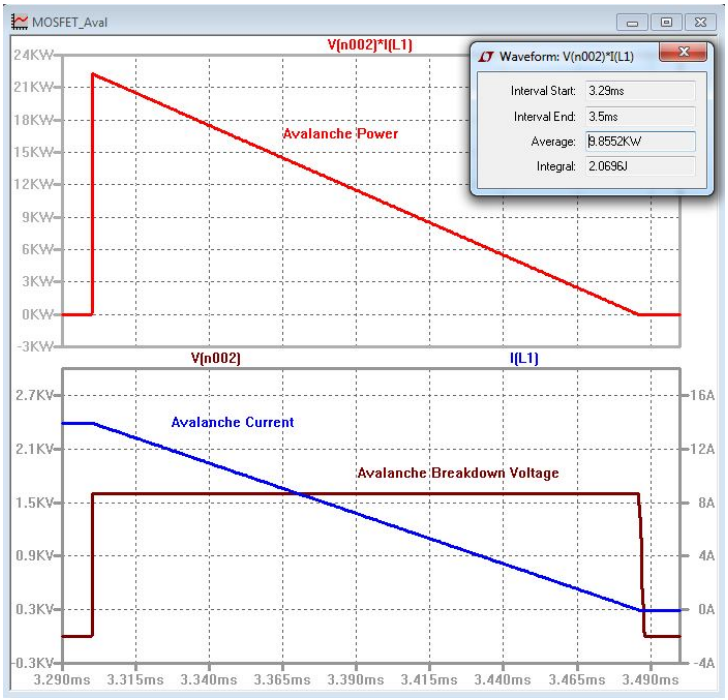


Figure 4.8: 1200V SiC MOSFET Simulation of Avalanche Operation at Avalanche Current of 14A

4.5 Test Procedure and Lab Setup

The fig. 4.9 shows the test circuit used for determining the Avalanche Energy Capability for Power MOSFETs [26] [27]. In the circuit the current is first increased in the Inductor by switching ON the Power Device (here MOSFET) and then the Power Device is turned OFF so that the Inductor energy is dumped in the device. The fig. 4.10 shows the expected output waveforms with $V_{(BR)eff}$ as the actual breakdown voltage of the device and I_0 as the inductor current. V_{DD} is the supply voltage chosen as 50V and a 20 mH Inductor (L) is used in all the tests.

Eq. 4.4 and eq. 4.5 gives the Avalanche energy for the proposed setup.

$$t_{AVAL} = \frac{I_0 * L}{V_{BReff} - VDD} \tag{4.3}$$

$$E_{AVAL} = 1/2 * I_0 * V_{BReff} * t_{AVAL} \tag{4.4}$$

$$or,$$

$$E_{AVAL} = 1/2 * L * I_0^2 * \frac{V_{BReff}}{V_{BReff} - VDD} \tag{4.5}$$

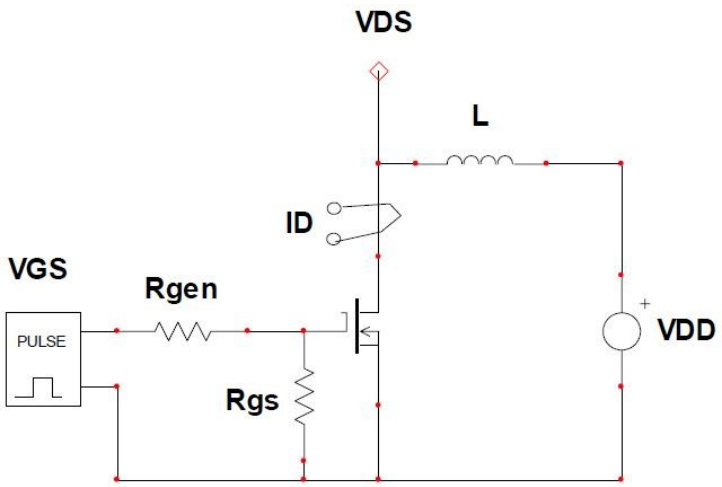


Figure 4.9: Test Circuit for MOSFET Avalanche Characterization

4.5.1 Test Setup Issues

During the test setup for MOSFET Avalanche test, some issues surfaced. One critical problem was the Inductor-Capacitor Resonance when low value Capacitor was used in the setup as shown in the fig. 4.11. To overcome this problem a very high value Capacitor 800 uF was used so that the resonance frequency becomes very small and the resonance time period is large. This helped in reaching the desired current values for the test.

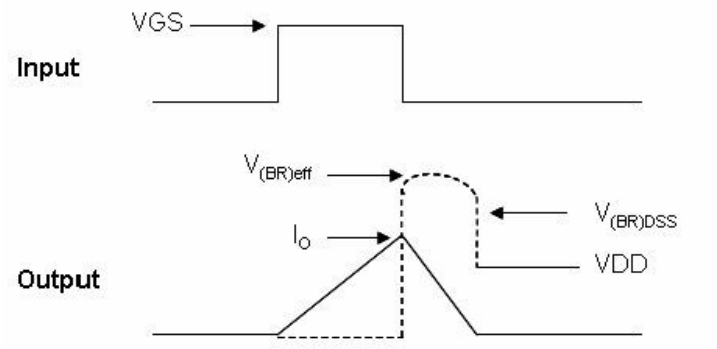


Figure 4.10: MOSFET Avalanche waveforms

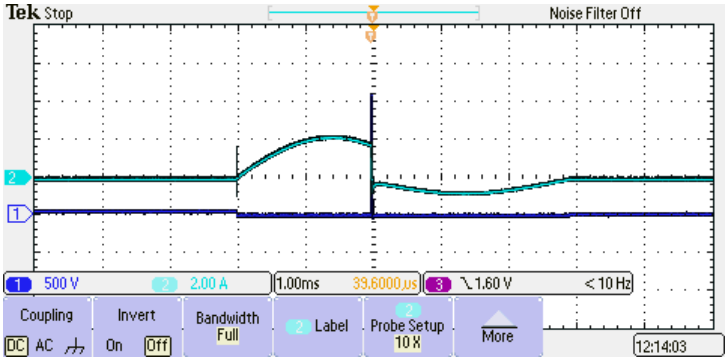


Figure 4.11: Resonance issue in MOSFET Avalanche Setup

4.5.2 Test Results

Avalanche Energy Tests are performed on 1200 V and 900 V SiC MOSFET's and 1200 V Si IGBT to determine the Max. Avalanche Energy capability of the devices. The results are tabulated in the Table 4.1. At least 3 samples of each devices were tested and an average value is given in the table. The CREE X3M0010090 900 V device is an automobile graded device. Therefore its Avalanche Energy Capability is far significant than the other devices tested and its maximum capability couldn't be determined due to Inductor current saturation. The Test Waveforms are shown in the Appendix A.

Table 4.1: Avalanche Energy

Device	Max. Avalanche Current	Average Avalanche Energy
MONOLITH Sample A 1200 V MOSFET	14.3 A	1.25 J
MONOLITH Sample B 1200 V MOSFET	14.5 A	1.23 J
CREE 1200 V MOSFET	14 A	1.17 J
IXYS Si IGBT IXYP20N120C3	10.6 A	.46 J
CREE X3M0010090 900 V	$> 15A$	$> 1.8J$

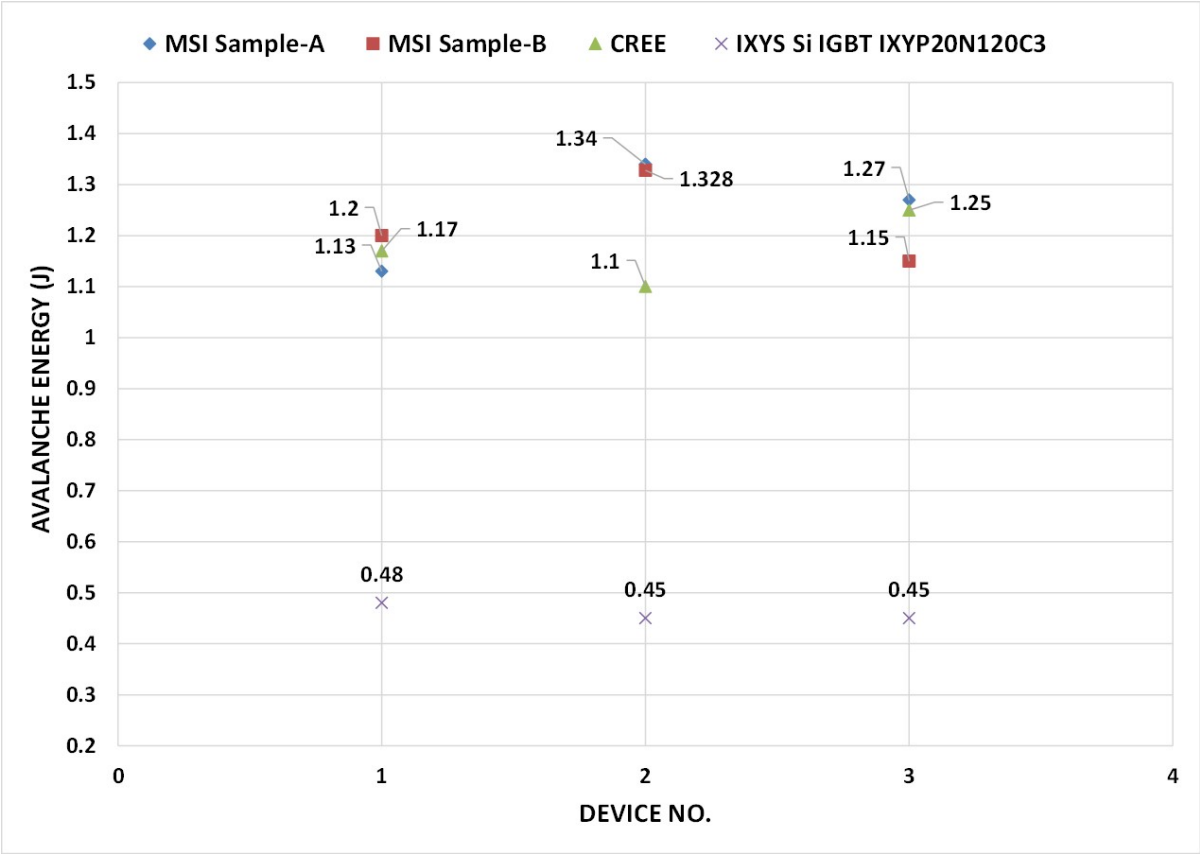


Figure 4.12: Avalanche Energy Data of the 1200 V devices

Chapter 5

Diode Avalanche Characterization

Researchers have touched the Avalanche Energy characterization of 600 V JBS Diodes [28], but there is a significant need for investigation and examination of 1200 V SiC JBS Diodes in terms of Single Pulse Avalanche Energy Capability.

The theoretical analysis of Avalanche phenomenon is identical to the MOSFETs analysis as presented in the section 4.1. The avalanche energy characterization of the Diodes is important for many applications. One potential application is presented in the next section. With increasing number researches in Electric Cars and going for higher battery voltages, will require improvement in Avalanche capability of presently used devices. As will be seen in the following sections SiC JBS offers great Avalanche capability and will be suitable for automotive applications.

5.1 Automotive Electronic Module

Electronic modules in automotive applications usually have a reverse battery protection device to safe guard against the reverse current surge [29]. JBS diode in series as shown in fig. 5.1 is one of the protection scheme generally used. Due to a constant forward voltage drop across the diode when the system is working there would be power dissipation across it, hence JBS is preferred over P-i-N diode owing to lower forward voltage drop across it. The Power losses will heat up the JBS diode depending on the load current and therefore it should be rated for higher working temperatures. Also from fig. 5.2 the forward voltage drop increases with temperature thus making it a positive feedback loop [6].

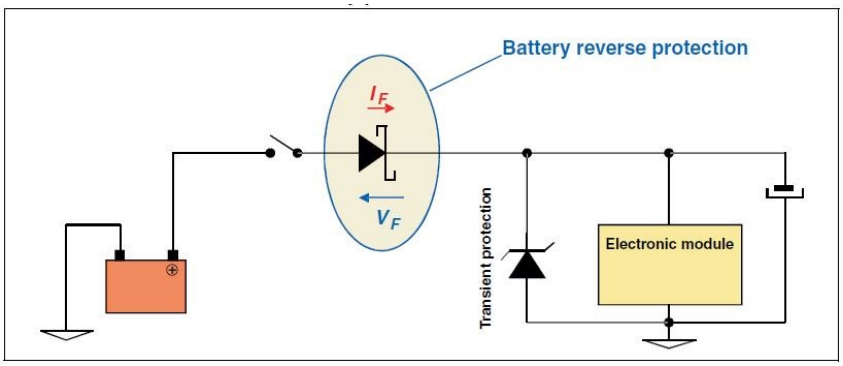


Figure 5.1: Automotive Electronic Module

The JBS diode suppresses the reverse current transients by going into Avalanche mode and therefore the Avalanche energy Capability is an important factor in selecting the device for the Battery reverse protection scheme. SiC JBS Diode works well for higher temperature range and have much better Avalanche energy capability as compared to Si JBS diodes. In this work the single pulse avalanche capability of various 1200 V/10 A SiC JBS diodes are tested.

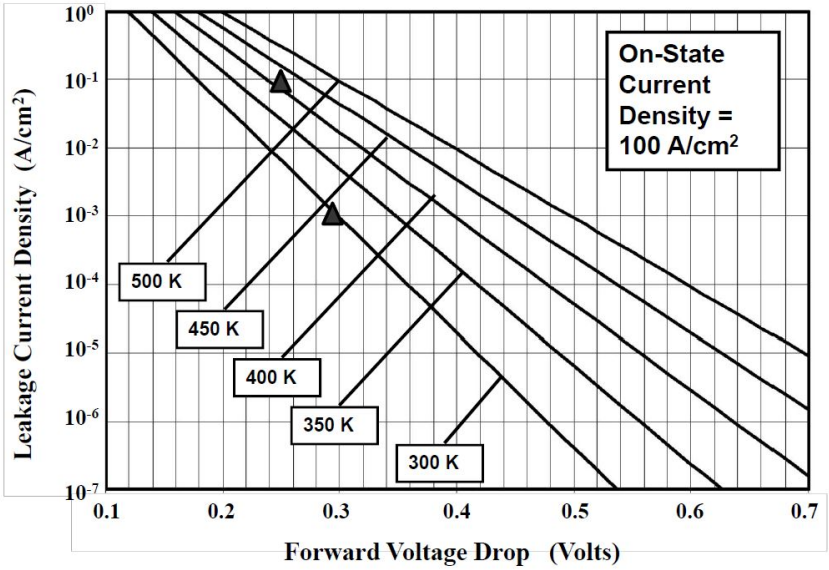


Figure 5.2: Forward Voltage drop variation with Temperature

5.2 Diode Avalanche test Circuit

The fig. 5.2 shows the test schematic for the Diode Avalanche Characterization [30]. The circuit works as following:
The driving switch (here a MOSFET) is switched ON to ramp up the current in the inductor. When the desired value of current is reached, the driving switch is turned OFF and the DUT (DIODE) undergoes Avalanche condition. The Inductor value is chosen 20 mH. The Driving switch should have much higher breakdown Voltage rating than the JBS Diode(DUT). The Voltage across the DUT (V_{BR}) and the Current through it (I_{AV}) is measured. The Avalanche energy is then given by the time integral of product of V_{BR} and I_{AV}.

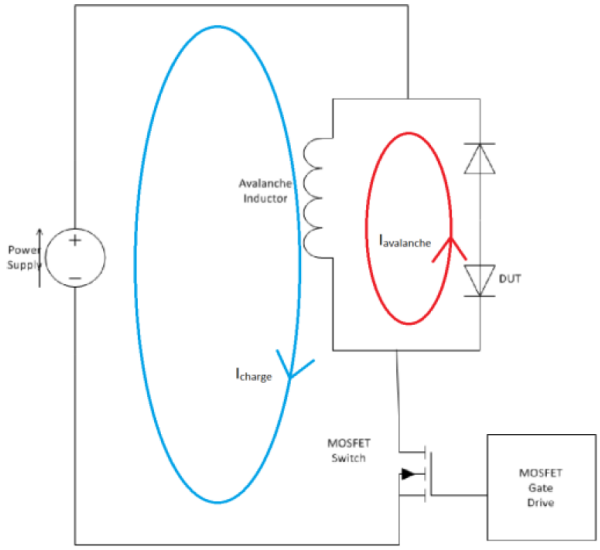


Figure 5.3: Diode Avalanche test Schematic

$$E_{AVAL} = \int (V_{BR} * I_{AV}) dt \tag{5.1}$$

In the actual test setup a 3.3 kV IXYX IGBT is used to ensure that the driving switch does not experience any Avalanche. Also the Inductor value is fixed to 20 mH to evaluate the total Avalanche Energy for each device.

5.3 Avalanche Operation Simulations

To verify the theoretical analysis of the setup proposed in section 5.2 for diode Avalanche Characterization, Simulations are carried out in LTspice software. The Simulations done are non Electro-thermal. LTspice model of CREE C4D10120A 1200V SiC JBS Diode is used for the simulations. The fig. 5.4 gives the test schematic for the simulation. Same LTspice model of CREE C4D10120A 1200V SiC JBS Diode is used as anti-parallel diode (U1). Also a 1700V SiC MOSFET is used as driving switch.

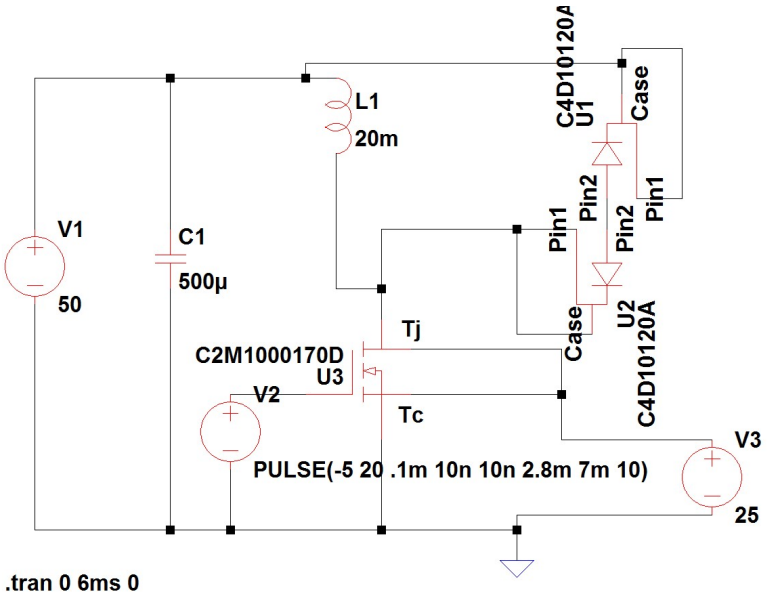


Figure 5.4: Diode Avalanche test Schematic for simultation

Fig. 5.5 and fig. 5.6 shows the Avalanche behavior of 1200V SiC JBS Diode at Avalanche current of 6.4A and 10A respectively. The values of current for these simulations is particularly chosen to verify the test results obtained in section 5.4. Table 5.1 summarizes the results obtained.

Table 5.1: Avalanche Energy

Avalanche Current A	Avalanche Energy
6.4 A	410.66 mJ
10 A	1.01 J

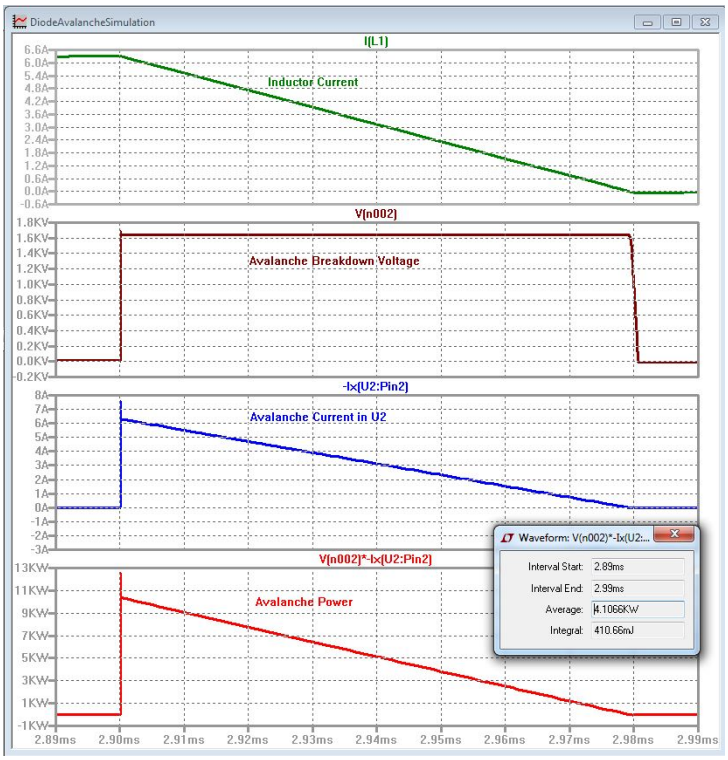


Figure 5.5: 1200V SiC JBS Simulation of Avalanche Operation at Avalanche Current of 6.4A

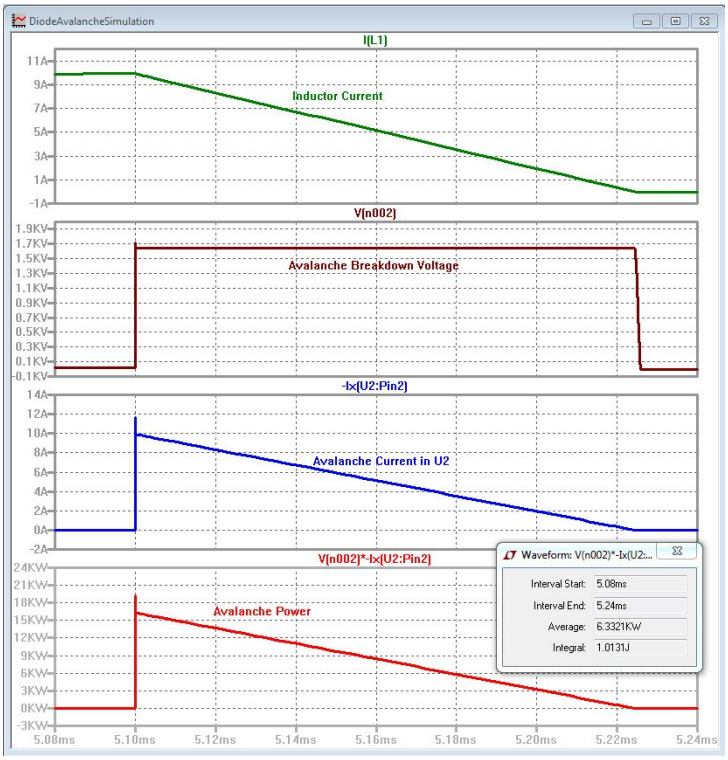


Figure 5.6: 1200V SiC JBS Simulation of Avalanche Operation at Avalanche Current of 10A

5.4 Experimental Results

The fig. 5.7 shows the lab setup for the Diode Avalanche Characterization. A 20 mH Inductor is used for all the tests. The gate driver for driving the MOSFET switch is discussed in section 2.1. A high bandwidth Pearson probe is used for the current measurement and a differential voltage probe is used for high voltage measurement. The test box described in section 3.4.1 is also used here.

The table 5.2 summarizes the results obtained for various manufacturer. The devices are tested for their maximum single pulse Avalanche Energy capability, using 20 mH Inductor by varying the Inductor current,upto a current value where the device fails. As can be observed from the table Monolith Semiconductor, CREE and Rohm have nearly same Avalanche characteristics with Monolith having the highest capability of 346.1 mJ. The tested Infineon's device sample has the least Avalanche failure Energy.

After it was determined that all the samples failed well before their rated current values i.e. 10 A, another test was conducted with the Inductor current fixed to 10 A. Three devices from each manufacturer (including 3 different lot samples from Monolith Semiconductor Inc.) are tested and the results are compiled in the fig. 5.8. Average Avalanche Energy at 10 A, for

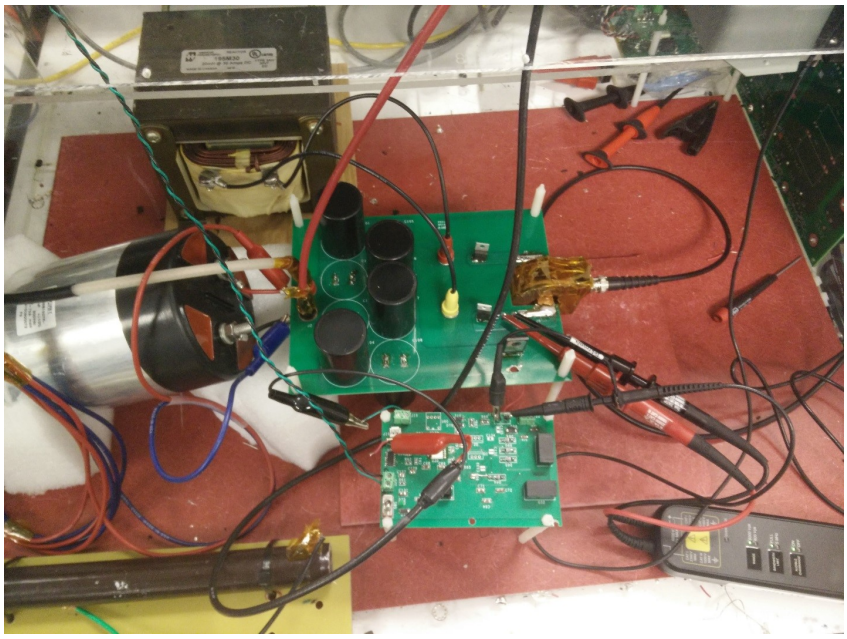


Figure 5.7: Experimental Setup for Diode Avalanche test

each manufacturer is summarized in table 5.3. The results are comparable to the previous tests with only exception of Rohm device sample, which has very low Avalanche failure Energy at 10 A as compared to the earlier case.

The JBS Diode Avalanche Operation waveforms are presented in the Appendix A. The simulation results obtained in table 5.1 matches closely to the test results at Avalanche Current of 6.4A but the simulation model fails to predict the failure of the JBS diode. The test waveforms are also in close proximity to the simulated waveforms.

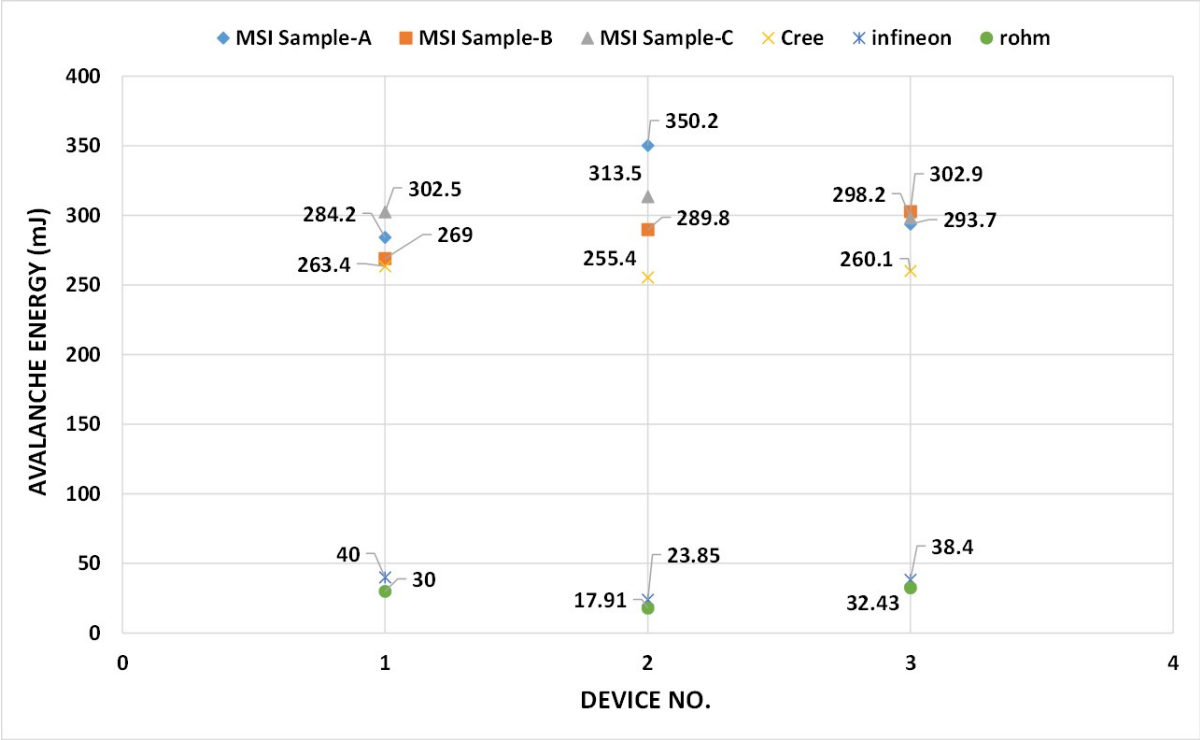


Figure 5.8: Avalanche Energy Results for the tested 1200 V JBS Diodes at $I_{AV} = 10A$

Table 5.2: Avalanche Energy Test of SiC JBS Diode

Company Name	Device	Maximum Avalanche Current	Avalanche Failure Energy
CREE	C4D10120A-1200V, 10A	6.4 A	302.4 mJ
ROhm	SCS210KGC-1200V, 10A	6.8 A	270 mJ
Infineon	IDH10S120AKSA1-1200V, 10A	1.6 A	41 mJ
Monolith Semiconductor	1200V, 10A	6.2 A	346.1 mJ

Table 5.3: Avalanche Energy Test of SiC JBS Diode at 10A

Company Name	Device	Average Avalanche Failure Energy
CREE	C4D10120A-1200V, 10A	259.6 mJ
ROhm	SCS210KGC-1200V, 10A	26.8 mJ
Infineon	IDH10S120AKSA1-1200V, 10A	34.1 mJ
Monolith Semiconductor Sample A	1200V, 10A	309.4 mJ
Monolith Semiconductor Sample B	1200V, 10A	287.2 mJ
Monolith Semiconductor Sample C	1200V, 10A	304.7 mJ

Chapter 6

Conclusion and Future work

6.1 Conclusion

The work presented in this thesis proposes the test setups and procedures for ruggedness characterization of SiC Power Devices. Detailed analysis of Short Circuit Characteristics of 1200V SiC MOSFETs is done to determine its Short Circuit withstand capability and also the factors affecting the failure. Some device layout suggestions are also presented to improve upon the Short Circuit withstand capability. After testing enough devices and establishing the minimum short circuit withstand time for the 1200V SiC MOSFET, a Protection Circuitry is also proposed for fast and reliable protection against short circuit in the systems. The main advantage of this protection scheme is its fast detection of the over-current (around 1.5us) and then soft turn-off (reducing the di/dt voltage spikes). This scheme can be used in many applications such as motor-drive and Power distribution.

Switching energy losses are calculated for 1200V SiC MOSFET to compare the results with a similar rated Si IGBT. Lower Switching losses in SiC MOSFET allows going for higher switching frequency and thus reduction in the size of the magnetic components.

Single pulse Avalanche energy tests were done on 1200V SiC MOSFET to determine its Avalanche energy capability. The tests results demonstrated that the SiC MOSFETs can withstand a significant amount of Avalanche energy (around 1J). Thus these devices can work well in Avalanche conditions. 1200V SiC JBS diodes from different companies were also tested for their single pulse Avalanche Energy capabilities. The results showed that the SiC JBS diodes are capable of withstanding good amount Avalanche energy before failing.

6.2 Future Work

Short Circuit analysis done in this work is at a room temperature ($25°C$). Testing at different Temperatures is needed to check variations of short circuit characteristics with temperature. Analysis of an another test, the load under short circuit, is required to compare it with the tests results in this work.

Repetitive Avalanche test on MOSFET and JBS Diode is needed to check the characteristics variations as reported in some text [28]. The Single Pulse Avalanche Energy capability defines the design limits but the repetitive Avalanche will effect the system operations.

A 5 kW Dual Active Bridge (DAB) Converter is to be built utilizing the characterization data obtained in this work. The DAB with high switching frequency and energy density will also demonstrate the ruggedness characteristics of the 1200V SiC MOSFET.

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APPENDIX

Appendix A

Test Waveforms

A.1 Double Pulse test at 800V

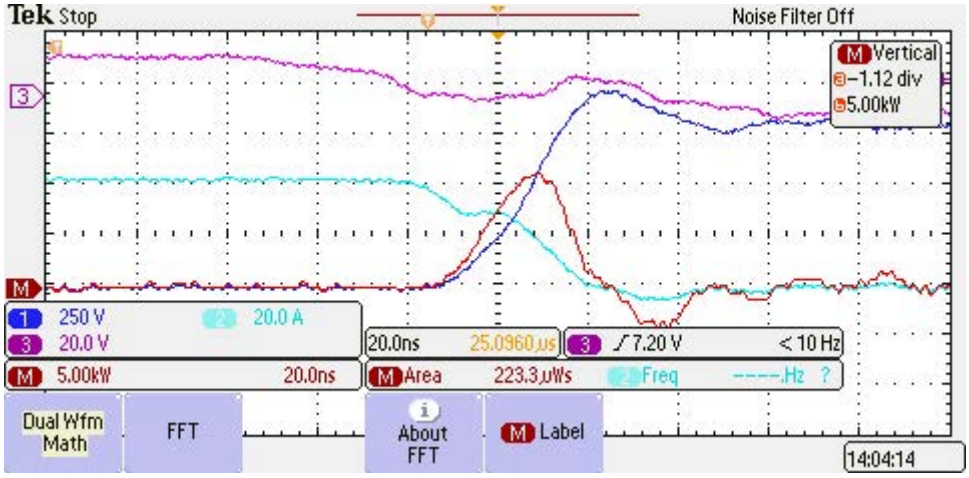

Figure A.1: Turn OFF waveforms for 1200V SiC MOSFET at Vds of 800V and Id of 40A

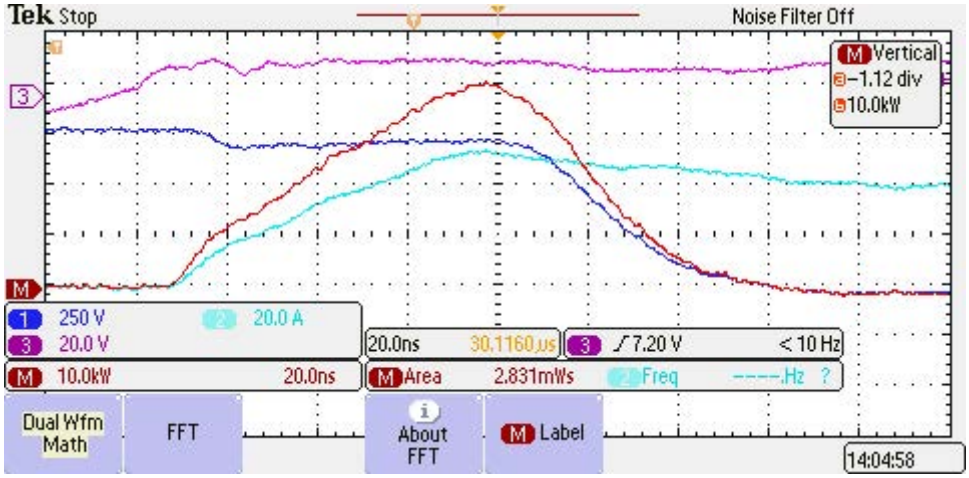

Figure A.2: Turn ON waveforms for 1200V SiC MOSFET at Vds of 800V and Id of 40A

A.2 Short Circuit Waveforms

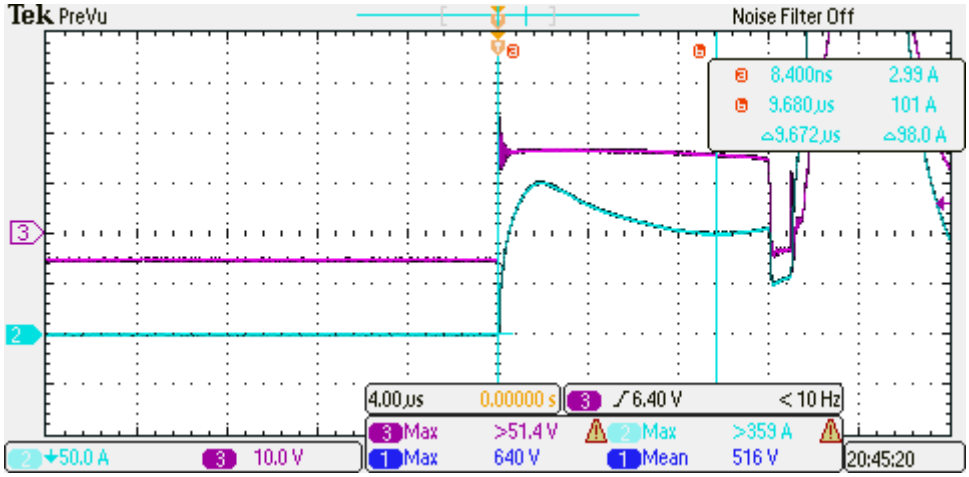

Figure A.3: Short Circuit Failure Waveform at $V_{DS} = 600V and V_{GS} = 16V$

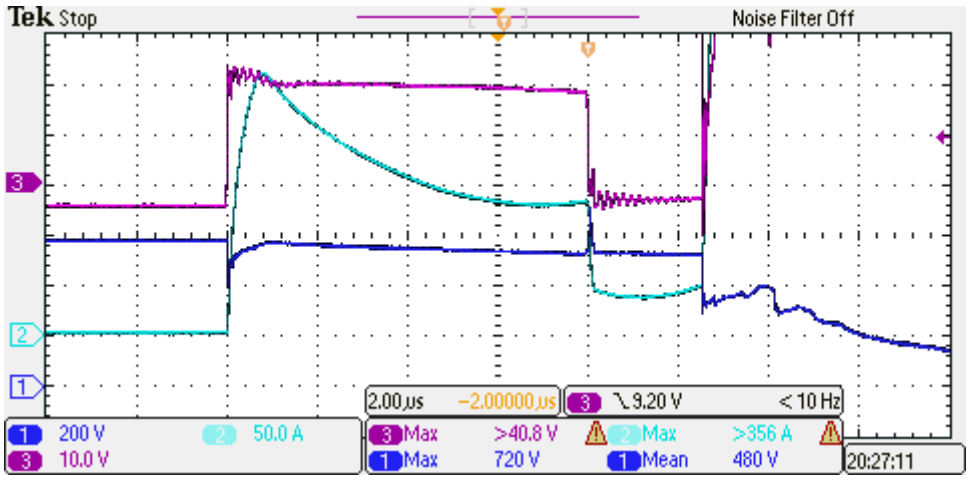

Figure A.4: Short Circuit Failure Waveform at $V_{DS} = 600V and V_{GS} = 20V$

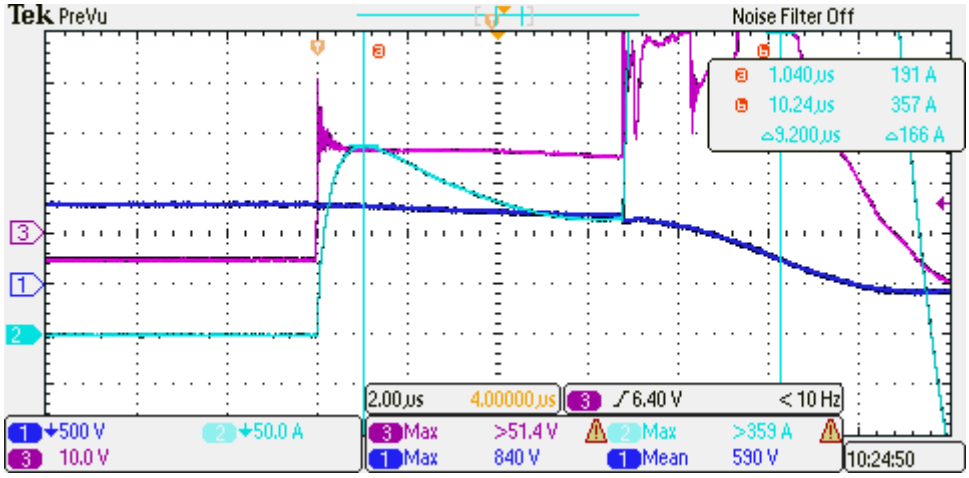

Figure A.5: Short Circuit Failure Waveform at $V_{DS} = 800V and V_{GS} = 16V$

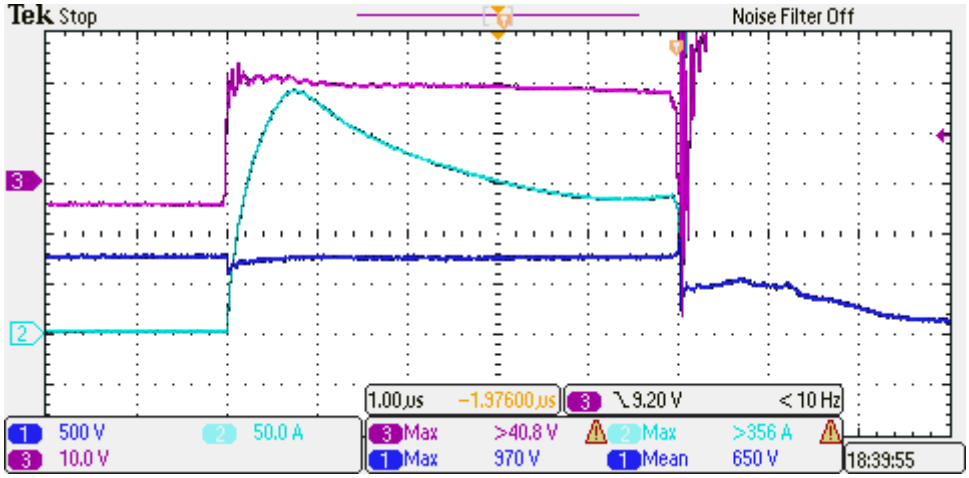

Figure A.6: Short Circuit Failure Waveform at $V_{DS} = 800V and V_{GS} = 20V$

A.3 MOSFET Avalanche Waveforms

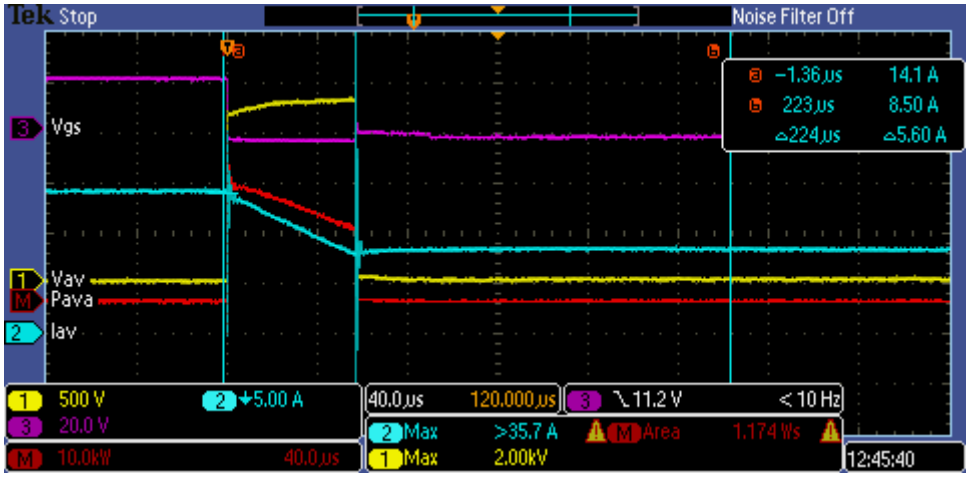

Figure A.7: CREE 1200V SiC MOSFET Avalanche Failure

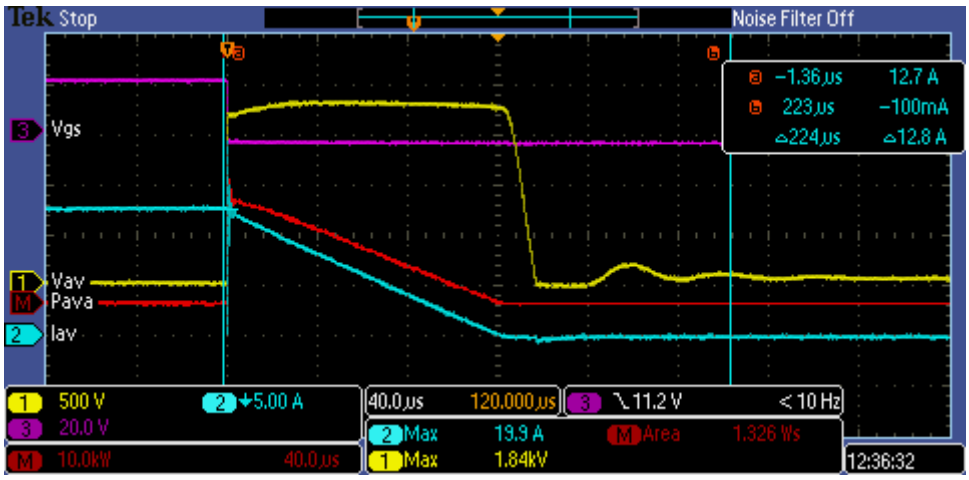

Figure A.8: MONOLITH 1200V SiC MOSFET Avalanche Failure

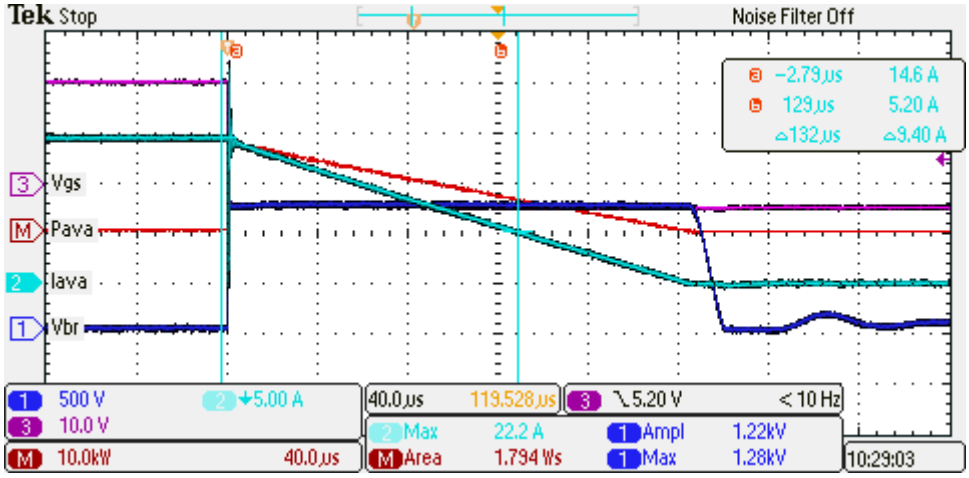

Figure A.9: CREE 900V SiC MOSFET Avalanche Failure

A.4 Diode Avalanche Waveforms

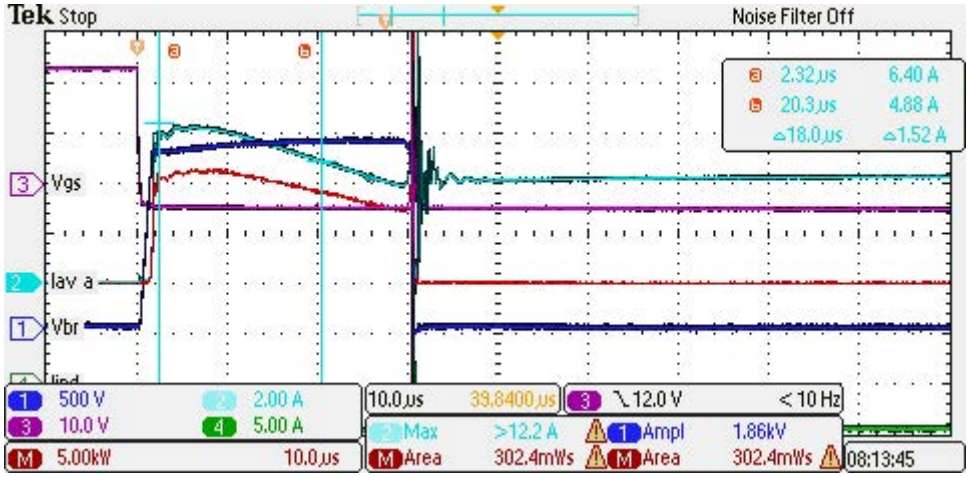

Figure A.10: CREE 1200V SiC JBS Diode Avalanche Failure

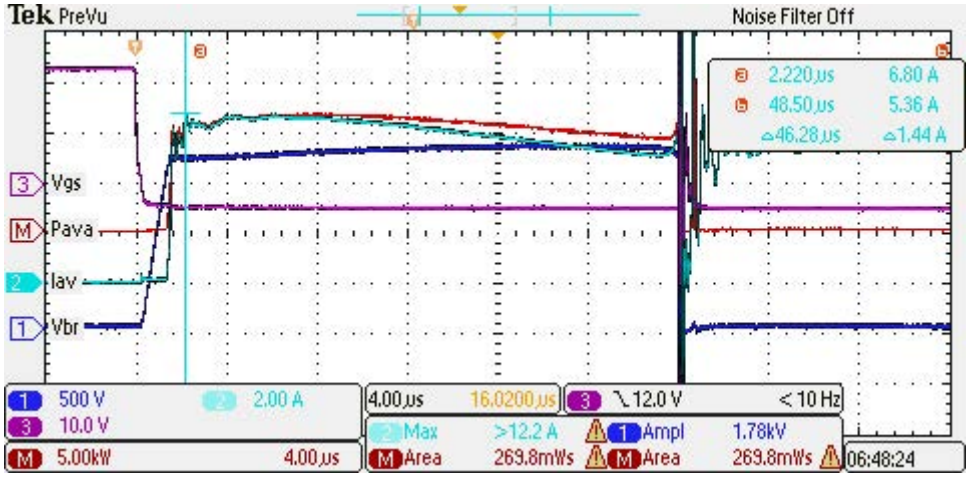

Figure A.11: Rohm 1200V SiC JBS Diode Avalanche Failure

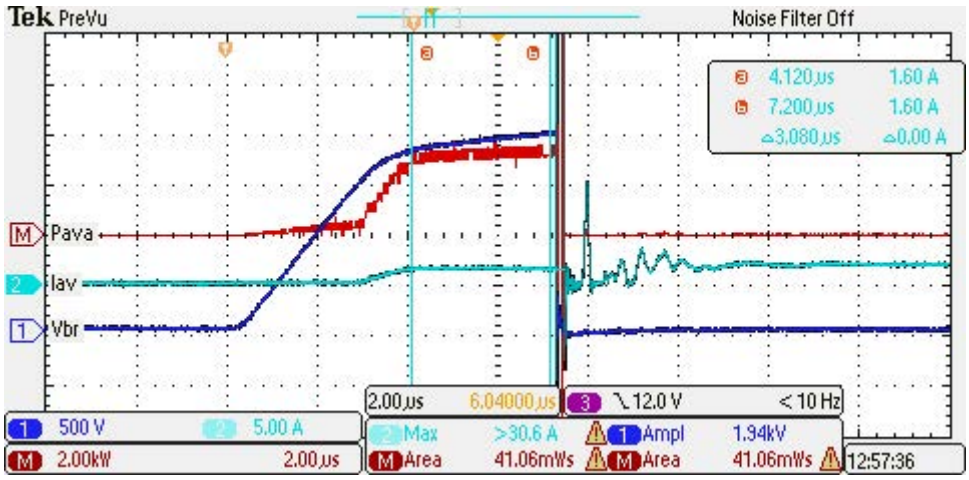

Figure A.12: Infineon 1200V SiC JBS Diode Avalanche Failure

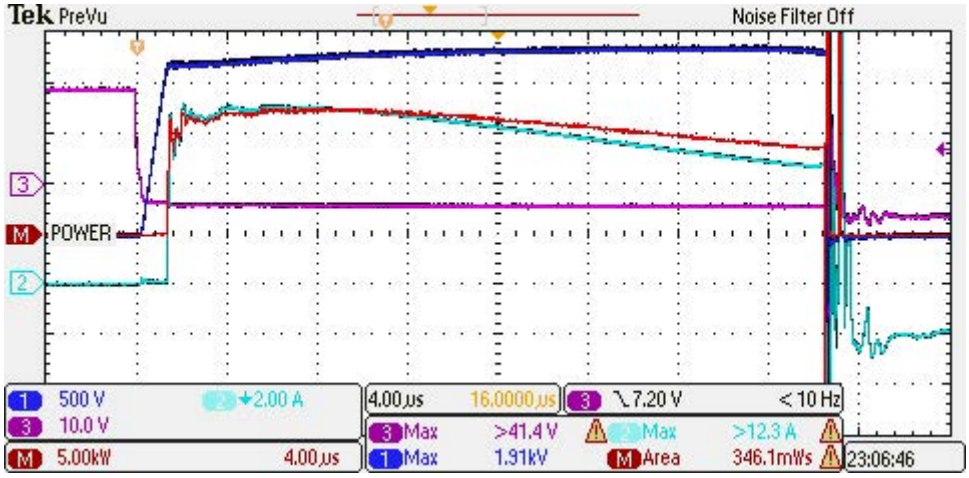

Figure A.13: Monolith 1200V SiC JBS Diode Avalanche Failure