ABSTRACT

SHRIVASTAV, ASHISH SANJAY. High Efficiency GaN FET based Flexible Electrical Power System for Cube-Satellites using Pulse Frequency Modulation. (Under the direction of Dr. Subhashish Bhattacharya.)

This thesis proposes an efficient and configurable electrical power system (EPS) for Cube-Satellites (CubeSats). Different versions of EPSs, which are DC-DC converters, are designed and tested using Silicon and Gallium Nitride FETs. The thesis discusses the requirements, specifications, architecture and implementation of EPS. It presents the EPS which is developed as a test-bed for testing and developing various algorithms like pulse frequency modulation (PFM) or light load management, maximum power point tracking (MPPT), constant current-constant voltage (CC-CV) charging of battery. The system is controlled by DSP-TMS 320F28335 which also controls the multi-phase voltage supplies and path switching circuit to direct the power from solar panels to load converters. To benchmark the performance of EPS, factors like efficiency and switching frequency are optimized. Previous vresions of EPS were developed using Silicon FETs rated at 40V, 5.4A. The devices were switched at 150kHz. Efficiency and power loss analysis of the EPS using Silicon FET were done extensively as a part of this thesis.

To mitigate the power loss at a higher switching frequency, EPC 2016 eGaN FETs were used to design the revised version of EPS. The EPC2016 eGaN FET is a 3.4 sq.mm, 100 VDS, 11 A device with a maximum R_{DSON} of 16 mΩ. To reduce the size of filters, optimum switching frequency of the converters with GaN FETs is increased to 600kHz. GaN FETs are radiation hardened devices and thus a better choice for applications like CubeSat. Efficiency of 94 % is achieved for a DC-DC converter with GaN FET. The revised Electrical Power System - EPS aims to reduce power losses and also have all the capabilities of its silicon counterpart in a smaller form factor.

To further reduce the power loss, “Light Load Management” technique is discussed and implemented. It is also know as pulse frequency modulation (PFM) technique which is used to reduce switching losses at light load conditions. In PFM, efficiency profile starts from 74 % as compared to 0 % in PWM.

High Efficiency GaN FET based Flexible Electrical Power System for Cube-Satellites using Pulse Frequency Modulation

by
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A thesis submitted to the Graduate Faculty of
North Carolina State University
in partial fulfillment of the
requirements for the Degree of
Master of Science

Electrical Engineering

Raleigh, North Carolina

2016

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Chair of Advisory Committee

DEDICATION

To my parents and family members.

BIOGRAPHY

Ashish Shrivastav was born on May 30, 1989 in Mumbai (Maharashtra), India. He did his schooling from St. Mary's English School, Mumbai. He graduated from Sardar Patel Institute of Technology, Mumbai with a Bachelor in Electronics Engineering. He joined North Carolina State University in 2013 for M.S. in Electrical Engineering with specialization in Power Electonics. Since May 2014, he has been associated with Future Renewable Electrical Energy Delivery and Management (FREEDM) Systems Center during his study at North Carolina State University. His research focuses on design of hardware and software of power converters using GaN devices.

Ashish was an Executive Engineer in Industrial Automation and Drives Technology(IADT) at Siemens India since 2012. He worked with automation and commissioning of automation systems, SCADA and industrial drives of Siemens. Many of his projects were based on SIMOTION technology for Grab Ship Unloaders. He was employed with Intersil Corporation, CA as an Application Engineering Intern in May 2015. His prime focus was on characterization and validation of power management integrated circuits (PMICs) for mobile display.

ACKNOWLEDGEMENTS

I express my sincere gratitude and thank my advisor, Dr. Subhashish Bhattacharya for the guidance he has provided me during my graduate program at North Carolina State University. Working with Dr Bhattacharya has been an insightful experience and he gave me good opportunities to work on different projects including CubeSat, Wave Energy Converters(WEC) and GaN device based flyback converter.

I thank Dr Douglas Hopkins for accepting to become a member of the committee. I thank you for sharing your views and inputs for the CubeSat project and its presentation.

Dr Alexander Dean, I express my sincre gratitude for your support and direction. Your course on Embedded Controls and Design has been very helpful for the execution of the CubeSat project.

I thank FREEDM Systems Center for sharing the resources for this project.

I thank Shikhar Singh for introducing me this project and for his constant guidance and help. I appreciate the valuable suggestions from my seniors and friends, Samir Hazra on WEC, Ankan De, Sachin Madhusudan, Krishna Mainali, Awneesh Tripathi, Ritwik Chattopadhyay, Kasu Naidu, Avik Juneja Anirudha Mahajan, Mohd. Sameer Khan, Abhay Negi and Li Qi at FREEDM Systems Center. I extend my gratitude towards the staff members of the center, especially Karen Autry and Colleen Reid for the facilities and support. I thank Hulgize Kassa for his supervision assuring my safety in the laboratory.

I thank my colleagues and my seniors, Mike Ogier, Amit Tiwari, Swarup Doshi, Terry, Seenu, Arun, Shyam at Intersil Corporation for helping me in the CubeSat project.

I thank Prathamesh, Swaroop, Anish, Rohit, Ameya, Pratik, Yaman, Ronak, Shreya, Sayali, Dishit, Ashwin, Ganpati, Juhi and others for making this journey a memorable one.

I would like to thank my family members, Papa, Mummy, Dadima, Chachu, Chachi, Priti, Rachana, Kundan, Uday, Mahima and Kanika for their constant support and love.

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Introduction

CubeSats, miniature satellites, are playing an increasingly larger role in space exploration, technology demonstrations, scientific research and educational investigations. These miniature satellites provide a low-cost platform for various missions, including planetary space exploration; Earth observation; fundamental Earth and space science; and technology demonstrations such as cutting-edge laser communications, energy storage, in-space propulsion and autonomous movement capabilities. They also allow educators an inexpensive means to engage students in all phases of satellite development, operation and exploitation through real-world, hands-on research and development experience. There has been a rising emergence of researchers, universities and professional institutions constituting towards the development and launching of these CubeSats.

CubeSat is a generic term for a miniature satellite which is designed using commercial off-the-shelf components for development of its electronics framework [1] which capcitates anyone to build a satellite. A CubeSat has a volume of 1 liter, which translates into a cube having a 10 cm edge. A typical CubeSat weighs approximately 1 kilogram. The most remarkable feature of such satellites is the simplified development cycle; the use of off-the-shelf hardware and easy access to software resources has led to rapid rise in the number of the CubeSats deployed. They provide an economic approach for academia to contribute towards space research. CubeSats are highly modular and can be used to form larger satellites. The electrical system of a CubeSat is driven by the EPS, the powerhouse of the CubeSat. It is responsible for powering the various components of the CubeSat which includes the control unit, servo mechanisms, scientific equipment and communication modules.

This thesis discusses the design and development of an efficient, economic, multiphase, scalable electrical power system of a CubeSat. The electrical power system is a smart configuration of DC-DC converter which includes battery charging unit, solar power charger and multi-phase DC-DC converter serving as point of load converters.

Chapter 2 introduces the CubeSat with its technical requirements and specifications. Various building blocks and subsystems of the CubeSat are discussed in this chapter.

Chapter 3 discusses the architecture of electrical power system and previous work done on the development of electrical power system (EPS) for CubeSats. Extensive work has been done by Shailesh Notani [2] in his thesis on the development of the first version of the EPS board. Mihir Shah [3] followed the work of Notani in the exhaustive testing and software development for the EPS. Shikhar Singh [4] in his thesis explained the efficient method of software development for EPS by code profiling. This work builds on the work of Notani, Singh and Shah. It is more focused on the development of EPS using GaN FETs while the previous work was done on Silicon FETs.

Chapter 4 explains the development of EPS using GaN devices and the transient analysis of the EPS at different load conditions of different blocks of EPS. It deals with the hardware development of EPS using EPC 2016 GaN FETs. Efficiency analysis of GaN FET based EPS is presented in the chapter. Hardware design of EPS is explained with the help of schematic diagrams.

Chapter 5 is focused on the power loss analysis of Silicon based EPS. Different types of power losses are analysed and the efficiency analysis of Silicon based EPS is done. Break down of different power losses motivates to focus on the specific areas to boost the total efficiency.

Chapter 6 deals with the novel technique of "Light Load Management" of DC-DC converters and its role in EPS. It is also known as pulse frequency modulation (PFM) technique for boosting the light load efficiency of converter. Various building blocks of the PFM modelling are discussed and the results are compared with the Silicon FET based EPS. PSIM modelling

is done and its schematic diagram is explained for the understanding of PFM.

Chapter 7 deadls with the implementation Active Clamped Flyback converter design for 100 watts using GaN device GS 66508P by GaN Systems. To reduce excess voltage surge across the switch in flyback, active clamping is implemented using an auxiliary switch. The active clamped flyback converter is tested and compared with flyback topology without clamping.

Chapter 8 concludes with the summary of the thesis and the scope of future work in this project.

Chapter 2

CubeSat

2.1 Introduction to CubeSat

A CubeSat is a miniaturized small satellite used for space explorations and is made up of multiples of 10x10x11.35 cm cubic units called as 1U. 1U of CubeSat weighs 1.33 kilograms (2.9 lb) [5] and made up of commercial off-the-shelf (COTS) components for its electrical systems and structure. CubeSats are most commonly put in orbit by deployers on the International Space Station, or launched as secondary payloads on a launch vehicle [6].

CubeSat Project was a collaboarative effort between Prof. Jordi PuigSuari at California Polytechnic State University (Cal Poly), San Luis Obispo, and Prof. Bob Twiggs at Stanford University's Space Systems Development Laboratory (SSDL) which was initiated in 1999 [7]. The purpose of the project is to provide a standard for design of picosatellites to reduce cost and development time, increase accessibility to space, and sustain frequent launches. Presently, the CubeSat Project is an international collaboration of over 100 universities, high schools, and private firms developing picosatellites containing scientific, private, and government payloads. The main reason for reducing the size of the satellites is to reduce the cost of deployment and these satellites are often suitable for launch in multiples, using the excess capacity of larger launch vehicles. The CubeSat design specifically minimizes risk to the rest of the launch vehicle and payloads. Encapsulation of the launcherpayload interface takes away the amount of work that would previously be required for mating a piggyback satellite with its launcher.

In recent years larger CubeSat platforms have been proposed, most commonly 6U (10x20x30 cm or 12x24x36 cm) and 12U (20x20x30 cm or 24x24x36 cm), to extend the capabilities of CubeSats beyond academic and technology validation applications and into more complex science and national defense goals. In 2014 two 6U Perseus-M CubeSats were launched for maritime

surveillance with lifetime of 1 year, and these two CubeSats represent the largest CubeSats flown as of 2015 [8] as shown in Figure 2.1.

Figure 2.1: Perseus-M

Since nearly all CubeSats are 10x10 cm (regardless of length) they can all be launched and deployed using a common deployment system called a Poly-PicoSatellite Orbital Deployer (P-POD)as shown in Figure 2.2, developed and built by Cal Poly[9]. Most CubeSats carry one or two scientific instruments as their primary mission payload. CubeSats can be classified based on mass [10] as shown in Table 2.1 .

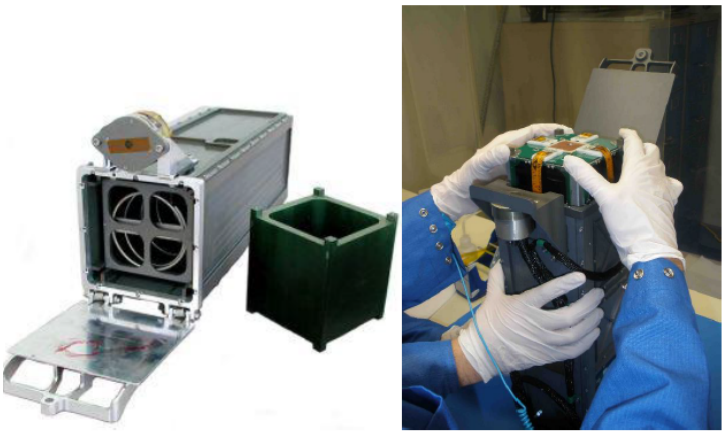

Figure 2.2: P-POD

Table 2.1: Classification of CubeSat

Type	Mass (kg)	Cost (US $)	Time of Development
Minisatellite	100 to 500	10 to 50 M	3 years
Microsatellite	10 to 100	2 to 10 M	1 year(approx)
Nanosatellite	1 to 10	0.2 to 2 M	1 year(approx)
Picosatellite	0.1 to 1	20 to 200 k	less than 1 year
Femtosatellite	0.01 to 0.1	0.1 to 20 k	less than 1 year

1U CubeSats shown in Figure 2.3 [11] belong to the genre of picosatellites.

Figure 2.3: 1 U CubeSat

2.2 Subsystems of a CubeSat

Different subsystems of a CubeSat are as shown in Figure 2.4 [12] :

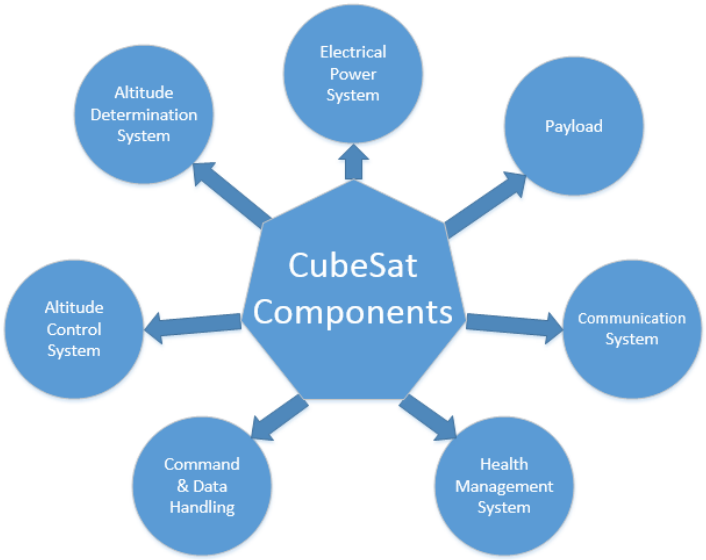

Figure 2.4: CubeSat Subsystem

2.2.1 Attitude Determination and Control System (ADCS)

The Attitude Determination and Control Subsystem (ADCS) keeps the satellite in proper orbit and orientation. The ADCS architecture is a crucial subsystem for any satellite mission since precise pointing is often required to meet mission objectives like pointing the antenna in an orientation to establish a good communication with the ground station, the solar panels towards the sun and the imaging camera towards the earth.. The accuracy and precision requirements are even more challenging for small satellites where limited volume, mass, and power are available for the attitude control system hardware. ADCS shown in 2.5 [13] consists of a permanent magnet to stabilize the satellite about earths magnetic field. It possesses sensors like magnetometer to determine the satellites orientation and send it to Control and Data Handling subsystem, sun sensors to detect the direction of sun and accelerometers to detect the motion of satellite.

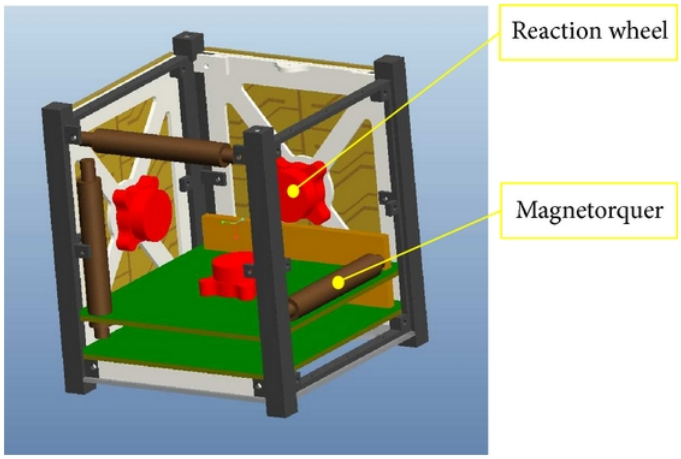

Figure 2.5: Altitude Control Subsystem

2.2.2 Command and Data Handling

The Command and Data Handling (CDH) system is the controller of the satellite. It is the main decision taking element in the CubeSat. It is responsible to synchronize all other subsystems, provide communication with ground station, store and process data from sensors and detect and manage faults. This subsystem communicates with all other subsystems and maintains their operation along with providing communication interface between subsystems and ground station.

2.2.3 Health and Management

The Health and Management subsystem relays the information about the health status of various building blocks of the CubeSat. This information is relayed to the ground station.

2.2.4 Communication Subsystem

The Communication subsystem is the data link between CDH subsystem and the ground station to communicate control commands. It relays the status and health data through a full duplex communication system. Communication system is made up of the antenna, terminal node controller and the radio transceiver.

2.2.5 Payload

Payload consists of experimental equipments, individual tasks like imaging or distributed tasks like weather monitoring. Payload and its application are used to create specifications for all the other subsystems of the satellite. Payloads can be magnetic and radiation sensors, weather monitoring equipments, cameras.

2.2.6 Structure

The structure is the framework of the CubeSat. Materials used in the structure must feature the same coefficient of thermal expansion as the deployer to prevent jamming. Specifically allowed materials are four Aluminum alloys: 7075, 6061, 5005, and 5052. Aluminum used on the structure which contacts the P-POD must be anodized to prevent cold welding, and other materials may be used for the structure if a waiver is obtained.[5] Beyond cold welding, further consideration is put into material selection as not all materials can be used in vacuums. Structures often feature soft dampers at each end, typically made of rubber, to lessen the effects of impacting other CubeSats in the P-POD. Structure of a 1 U CubeSat is seen in 2.6 [14].

Figure 2.6: A skeletonized 1U structure with computer offered by Pumpkin Inc

2.2.7 Electrical Power System

The Electrical Power Subsystem (EPS) is responsible to regulate power supply to all the subsystems. It is an between the solar panels and subsystems to harness the solar power store the energy in the battery. This stored energy is used to provide electrical power to other subsystems. It possesses the ability to regulate and respond to conditions like no power, over current, etc. but it is primarily controlled by Command and Data Handling subsystem. EPS is discussed in detail in this thesis.

2.2.8 Software

The software is divided into two categories. The ground station software is responsible to communicate with the satellite and display status of the satellite along with payload experimental data to ground crew. Flight software is responsible for the control and operations of CubeSat. It should support various modes like communications mode, idle mode and power save mode along with handling emergency conditions that arise during the flight.

Chapter 3

Architecture of Electrical Power System

3.1 Electrical Power System

CubeSats use solar cells to convert solar light to electricity that is then stored in rechargeable lithium-ion batteries that provide power during eclipse as well as during peak load times.[15] These satellites have a limited surface area on their external walls for solar cells assembly, and has to be effectively shared with other parts, such as antennas, optical sensors, camera lens, propulsion systems, and access port. Lithium-ion batteries feature high energy-to-mass ratios making them well suited to use on mass-restricted spacecraft. Battery charging and discharging is typically handled by a dedicated electrical power system (EPS). The EPS is the powerhouse of the CubeSat. It is responsible for powering the various components of the CubeSat which includes the control unit, servo mechanisms, scientific equipment and communication modules which constitutes different subsystems. It runs various algorithms to maintain storage devices in healthy condition, protect subsystems under electrical failures, extract peak power from PV arrays, etc. It is directly responsible for efficient power distribution in the satellite. Figure 3.1 [3] shows the general architecture of the CubeSat EPS. The EPS consists of solar panels, and two lithium ion batteries along with the DC/DC converters. The battery charging circuitry interfaces with the solar panels and the battery. The point of load converter generates a regulated bus voltage for the subsystems by harnessing the energy stored in the battery. There is a direct path for power from the solar panels to the point of load converter. The control for the battery charging converter and the point of load converter is either through a central digital controller or an analog control is implemented for them. The EPS also has additional circuitry for temperature monitoring of solar panels, over current protection, over voltage protection and one point of load circuitry which generates the rail voltage for the satellite on which all

the subsystems are attached. The health monitoring system and the communication features is optional.

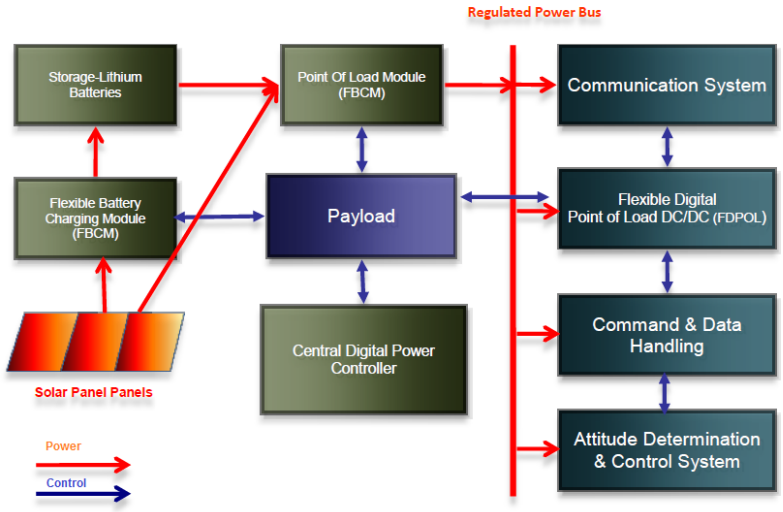

Figure 3.1: EPS Arcitecture of CubeSat

As seen in the Figure 3.1, important blocks of an EPS are as follows:

1. Flexible Battery Charging Module: Flexible Battery Charging Module (FBCM) is an important interface between solar panels and batteries. FBCM harnesses solar power to charge these lithium-ion batteries. The FBCMs are converters which perform CC-CV charging of the battery.

2. Flexible Digital Point of Load Converter: Flexible Digital Point of Load (FDPOL) Converter is responsible to generate a regulated power bus which powers other subsystems and payloads. In the absence of battery power, point of load converter can extract the power from the solar panels as well by using proper path switching circuit.

3. Controller: The Controller controls FBCM and FDPOL and runs various health and protection algorithms. It communicates with Command and Data Handling (CDH) Subsystem to receive commands regarding the system. It ensures proper path switching between solar panels, FBCM, lithium-ion batteries and FDPOLs.

3.2 Features of EPS

Important features of an EPS are as follows:

1. Size
   As the size of a 1U CubeSat is 10cm x 10cm, the size of EPS should not be more than 10 x 10cm. This poses a design constraint on PCB compactness.

2. Scalability
   There are multiple subsystems of a CubeSat and each subsystem requires electric power. A CubeSat EPS should be able to power multiple peripherals with varying power requirements. This means that the EPS should be able to regulate multiple voltage rails with transients limited to the specifications. Hence the EPS should have multiple point of load converters producing different output voltages.

3. Robustness
   The CubeSat operates in extreme conditions as it is deployed in space. It operates at intense temperature gradients with continuous exposure to radiation. An EPS should be able to sustain such conditions and should be radiation resistant with wide temperature range of operation.

4. Reliability
   An EPS should be able to withstand possible malfunctions. It should have failure backup features. In case of failure of any power module, there should be an alternate path switching circuit to keep up the power rails healthy. There should be enough storage devices to make the system fault tolerant.

5. Efficiency
   A CubeSat operates has a limited power budget. Batteries are the primary storage devices and the size and weight constraints limit its capacity. The EPS should be optimized for high efficiency so that all the available energy is utilized for useful purposes. Higher efficient control techniques should be implemented to prolong the battery life. Much emphasis of this thesis is on light load management with effective software control and by using efficient GaN FETs.

3.3 Previous Work

Various academic and professional institutions are taking interest in building CubeSats using commercial off-the-shelf (COTS) components for its electrical systems and structure. "CUBESAT KIT by Pumpkin Inc" [16] and "CLYDE SPACE" [17] are few of these companies which

have been working on EPSs for different CubeSats . Initially EPSs of these companies were analysed and then development of CubeSat EPS was done with these related architectures as reference.

3.3.1 CUBESAT KIT

In the year 2000, the team of CUBESAT KIT was assisting Stanford University and Santa Clara University on RTOS embedded software for microcontrollers destined for microsatellite missions. As the CubeSat standard for picosatellites gained acceptance, the CubeSat Kit was born for developing off-the-shelf CubeSat kit.CubeSat Kit EPS is a product by Pumpkin ©Inc. CubeSat Kit EPS uses linear voltage regulators to generate voltage rails of 3.3V and 5V along with unregulated battery power rail. Use of linear regulators reduces switching noise but reduces the efficiency of the converters. CUBESAT KIT EPS and its block diagram can be seen in Figure 3.2 and Figure 3.3.

Figure 3.2: CUBESAT KIT EPS

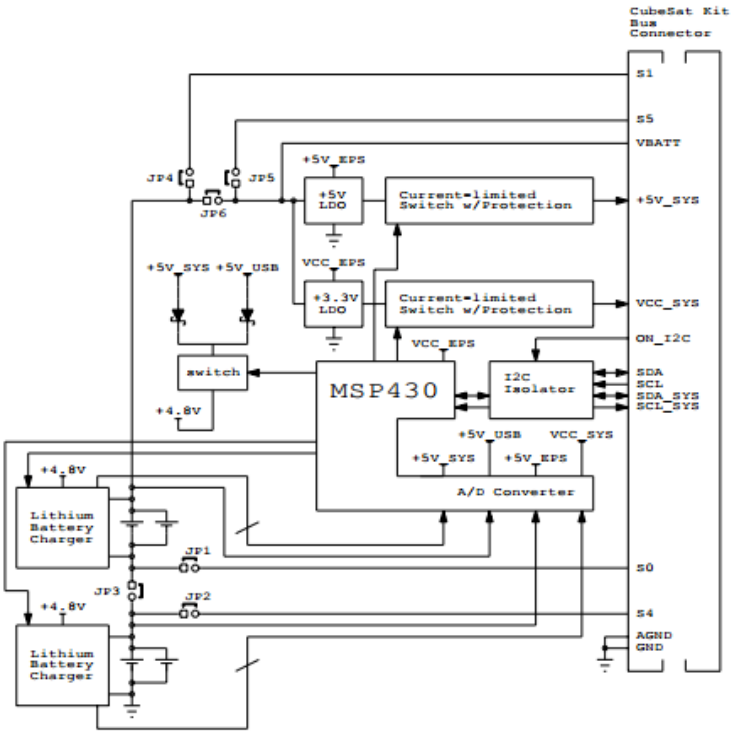

Figure 3.3: Block Diagram of CUBESAT KIT EPS

These EPS boards are modular and can be stacked to boost the output current. USB connector is used to charge the batteries.It has auto-resettable current fuse for over current protection.

3.3.2 Clyde Space

Clyde Space is the World leading CubeSat vendor having a combined experience in over 50 space programmes. They have been designing, manufacturing, testing and supplying power system electronics, solar panels and batteries for space programmes since 2006. Clyde Space customers include international universities, commercial companies and government organisations. Figure 3.4 shows the architecture and hardware of the second generation of Clyde Space CubeSat Electronic Power System [18]. Battery Charge Regulators (BCR) connects to solar panels with in built Maximum Power Point Tracker (MPPT). Each BCR can be connected in parallel to two solar panels on the opposite faces of the Cubesat. Energy from solar panel charges the batteries and provides power to distribution modules via a switched network. The output of the distribution modules is an unregulated Battery Voltage Bus, a regulated 5V supply Bus and a regulated 3.3V supply Bus. Protections features like Over-Current Bus Protection and Battery Under Voltage Protection are implemented.

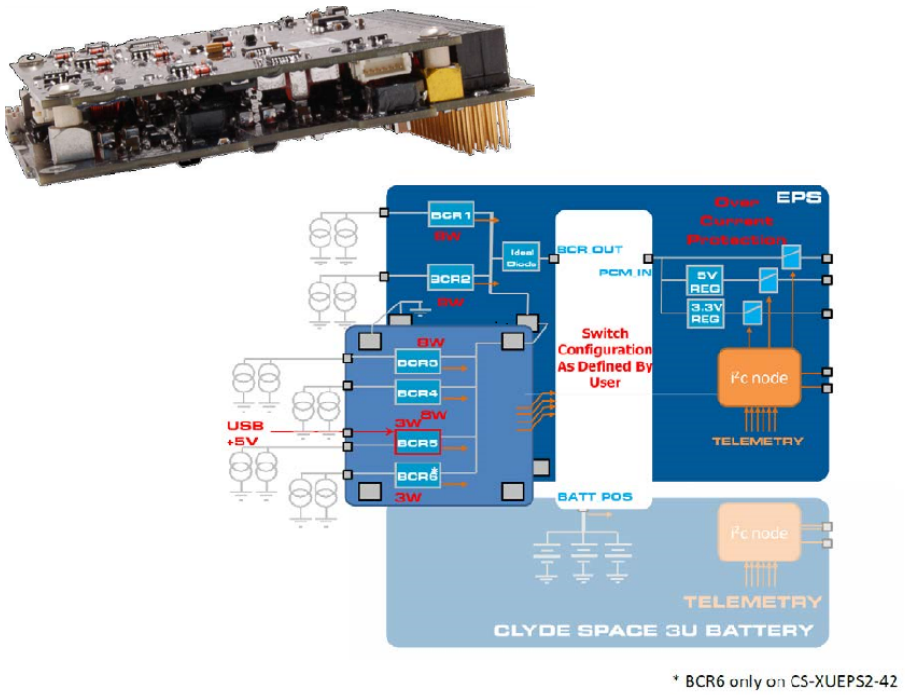

Figure 3.4: Clyde Space EPS Hardware and Architecture

3.4 CubeSat EPS using Silicon MOSFETs and GaN FETs

The primary focus of this research has been the design of intelligent and efficient EPSs for the CubeSat. A number of versions of the EPS have been developed with incremental upgrades and revisions. The first three Generations of the EPS are based on Silicon MOSFETs switching at 150 KHz [4] [19]. Figure 3.5 depicts the basic EPS architecture. The solar panels feed into the FBCM flexible battery charging modules which are responsible for charging the lithium batteries. The FBCMs are DC-DC converters which performs CC-CV charging of the battery. Lithium ion batteries are used which are rated at 7.2V and 2.2Ah. To charge these batteries, FBCMs are rated at 7.2 V output voltage. The switching circuitry directs the output of the FBCMs to the desired battery packs. It has four FDPOLs flexible digital point of load converters which produce DC voltage rails from 3.3 V to 12V. There are two synchronous buck and two synchronous boost converters. The solar panels can directly be connected to the input of the FDPOLs in case of battery failure. The path selection circuitry connects the output of one of the battery packs to the FDPOL's input.

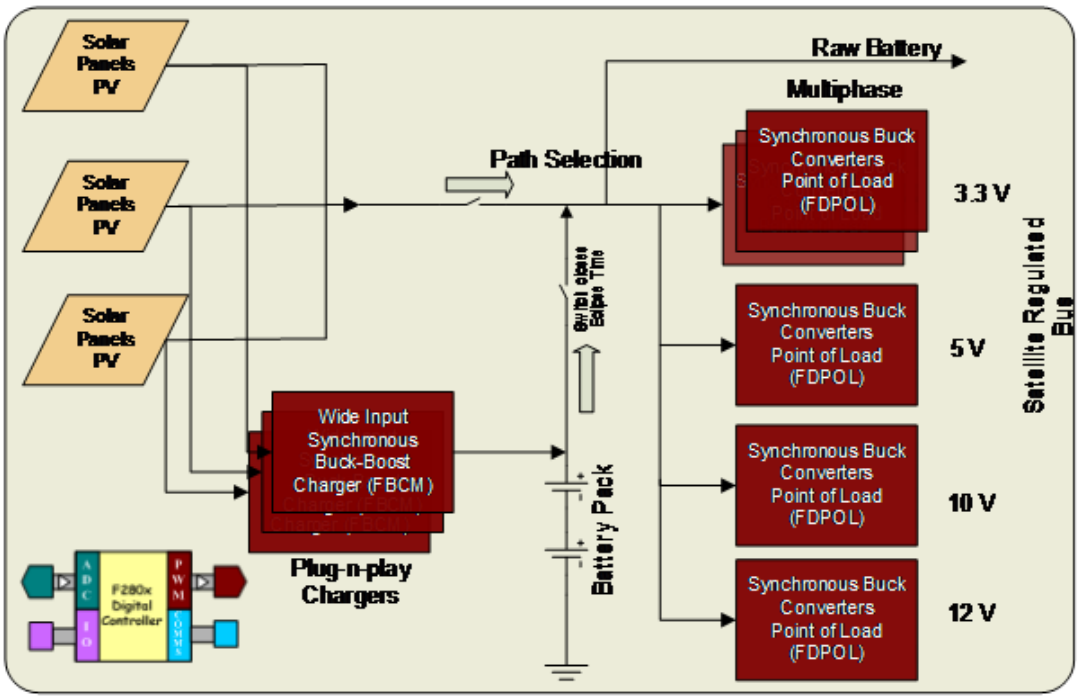

Figure 3.5: CubeSat EPS Architecture

3.4.1 Generation 1: CubeSat EPS

Figure 3.6 shows the first Generation EPS board which implemented the proposed features and necessary hardware design as explained by Shailesh Notani in his thesis [2]. The software models of the various constituents like the solar panel connections, the MPPT control loop and the FBCM and FDPOL control loop modeling were verified using this generation along with preliminary hardware testing.

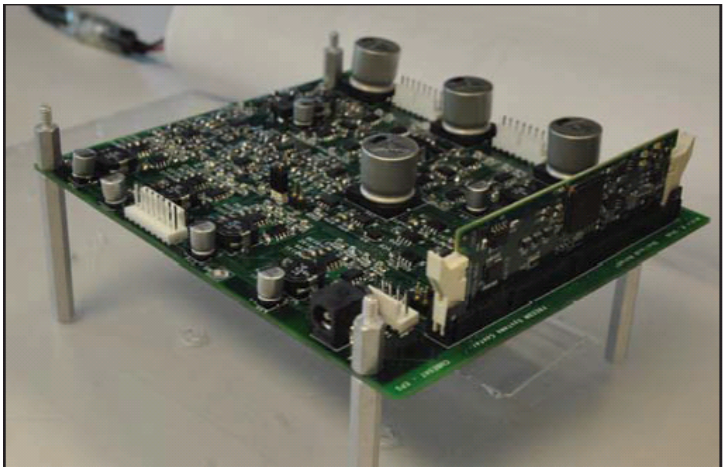

Figure 3.6: CubeSat EPS : Generation 1

3.4.2 Generation 2: CubeSat EPS

The second generation of the EPS comprised of certain upgrades and modifications to the first generation. Exhaustive hardware testing of the board by simulation of all the practical conditions which the CubeSat might encounter was done in this revision by Mihir Shah as part of his thesis [3]. A current sensor card for the EPS was also developed which enabled the use of current control techniques. Figure 3.7 shows the second generation EPS with the current sensor card.

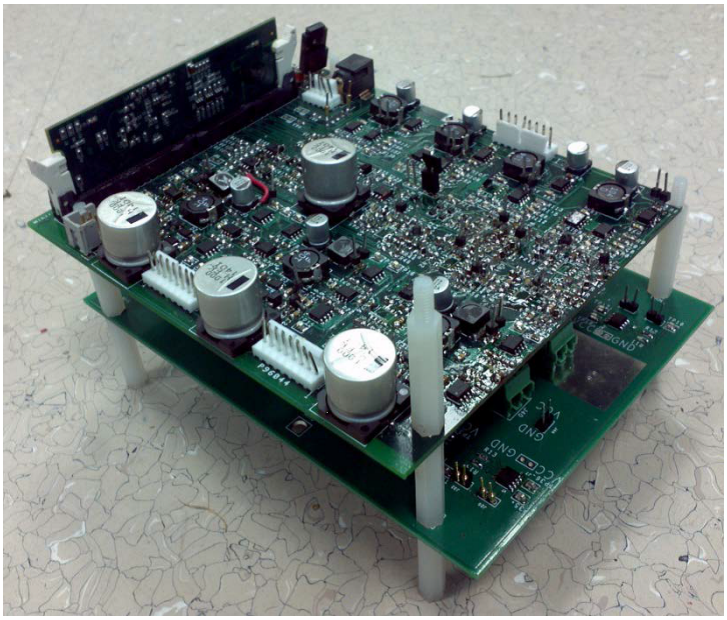

Figure 3.7: CubeSat EPS : Generation 2

3.4.3 Generation 3: CubeSat EPS

Figure 3.8 shows the third generation of the Silicon based EPSs. This board is highly optimized and compact measuring 5 x 4 inches. Shikhar Singh, in his thesis [4], designed this version using less hardware components compared to the previous generations and has integrated current sensing functionality.

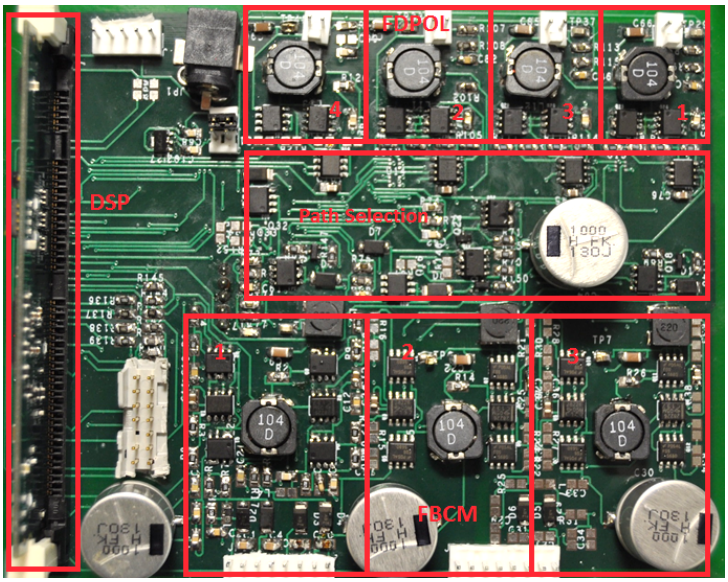

Figure 3.8: CubeSat EPS : Generation 3

3.4.4 Generation 4: CubeSat EPS using GaN FETs

This thesis focuses on the 4th generation of CubeSat EPS using GaN FETs. The system uses the EPC2016 [20] FETs. The devices are triggered using TIs LM5113 half bridge gate driver and the circuit is designed to switch at 600KHz. The design is very compact measuring 4.5 x 2.5 inches. GaN FET based EPS is covered in detail in subsequent chapters.

Chapter 4

GaN FET based EPS

4.1 Why GaN?

When high power density applications like Switch Mode Power Supplies (SMPS) are discussed, Silicon bipolar diodes are known to limit the efficiency due to their reverse recovery behaviour and the resulting switching losses. Bandgap materials like Silicon Carbide (SiC),Gallium Nitride (GaN) or Gallium Arsenide (GaAs) are preferable to overcome these disadvantages.

GaAs and GaN are compound semiconductors which fall into categories of elements with either three or five valence electrons. Boron, aluminum, gallium, indium, and thallium are Category III elements. Nitrogen, phosphorus, arsenic, antimony, and bismuth are Category V elements. Combining a Category III element with a Category V element produces a covalent bond with eight electrons, yielding a unique semiconductor. Such semiconductors have higher electron mobility than silicon, so theyre more useful at higher frequencies. GaAs and GaN have been found particularly useful for microwave power amplifiers and high frequency Switch Mode Power Supplies. GaAs and GaN can be used for high electron mobility transistors (HEMTs) which is also called a hetrostructure FET (HFET) or modulation-doped FET (MODFET). It is usually made with GaAs or GaN with extra layers and a Schottky junction as seen in Figure 4.1 and Figure 4.2 [22]. Depletion mode is the most common configuration. The pseudomorphic or pHEMT version improves performance by using extra layers of indium to further speed electron movement. These devices work at frequencies up to 20 GHz or so. The substrate in a GaN HEMT is usually sapphire or silicon carbide for best heat reduction, although silicon can be used. The 2DEG means two-dimensional electron gas, a layer of gas made of electrons that can move in any direction but vertical. LDMOS transistor is a special version of the standard enhancement-mode FET which is designed for high power dissipation.

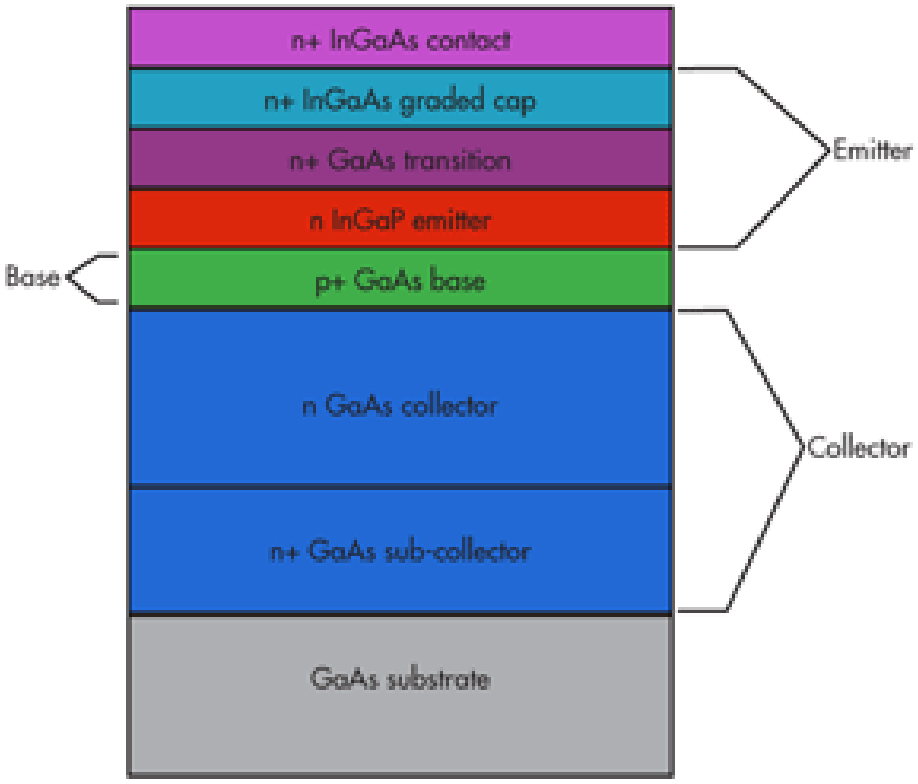

Figure 4.1: GaN HEMT

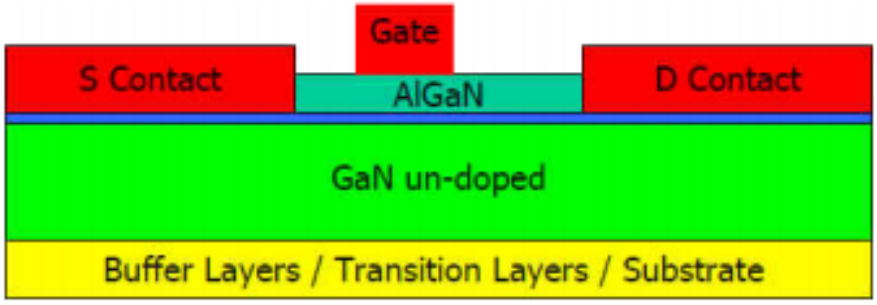

Figure 4.2: Lateral MOSFET using GaN with transitional layer material to align the lattice using Si or SiC as a substrate

Electrical properties of GaN, Si and GaAs FETs are as follows in Table 4.1

Table 4.1: Electrical properties of GaN, Si and GaAs FETs

Material Property	Si	GaN	GaAs
BandGap (eV)	1.1	3.4	1.4
Critical Field (M V/cm)	0.3	3.5	0.4
Electron Mobility (cm.cm/V-sec)	1450	2000	8500
Electron Saturation Vel (M cm/secs)	10	25	44

The electrical properties of GaN make it an ideal choice of material for optoelectronic, high-power and high frequency devices. Because GaN offers very high breakdown voltage, high electron mobility and saturation velocity, it is also an ideal candidate for high-power and high-temperature microwave applications like RF power amplifiers at microwave and mm frequencies, and high-voltage switching devices. The junction capacitance of GaAs devices is much smaller compared to SiC (more than 5 times), even though SiC diodes can operate at higher current densities. Avalanche capability is higher in GaAs. In SiC bipolar current flow can lead to defect growth and finally to the destruction of the device. GaAs power amplifiers are available with power levels up to about 5 W. That is roughly the upper power limit for GaAs devices, since they cannot withstand the high voltages, currents, and heat levels of silicon or GaN. But by using multiple devices in push-pull or parallel or combining amplifier outputs in transformers or networks, power levels up to about 20 to 40 W are possible. The junction capacitance of GaAs devices is much smaller compared to SiC (more than 5 times), even though SiC diodes can operate at higher current densities. Avalanche capability is higher in GaAs. In SiC bipolar current flow can lead to defect growth and finally to the destruction of the device. GaNs high power density, or its ability to dissipate heat from a small package, makes it so impressive. While GaAs has a basic power density of about 1.5 W/mm, GaN has a power density ranging from 5 to 12 W/mm. It also has high electron mobility, meaning it can amplify signals well into the upper-gigahertz ranges. Typical transistor cut off frequency is up to 200 GHz. Furthermore, GaN can do all this at relatively high breakdown voltages levels, up to 80 V or so. The downside to GaN is its high cost. The materials are expensive, and the processes to make devices are costly. As volume increases, production costs will come down but will still remain way above the process costs of bulk CMOS or even higher-cost GaAs production. Hence GaN finds its use in high efficiency applications like Switch Mode Power Supplies (SMPS).

4.2 GaN FET based EPS

As mentioned in the previous section, the EPS performs power management in the CubeSat. It is responsible for harnessing power, battery management and power rail supply. A good EPS should be scalable, robust, compact and efficient. Figure 4.3 shows the block diagram of the EPS which is a scaled down version comprising of one FBCM and two buck FDPOLs which produce DC voltages of 3.3V and 5V using EPC 2016 GaN FET. Characteristics of EPC 2016 GaN FET and its counterpart- Silicon FET [19],[20] are tabulated in 4.2.

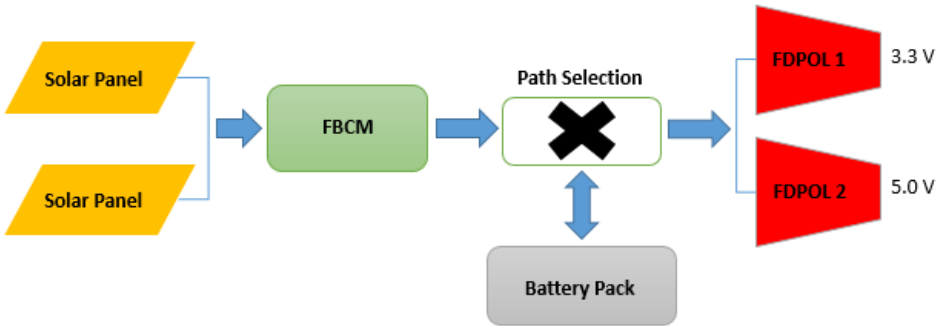

Figure 4.3: Architecture of EPS using GaN FET

Table 4.2: Characteristics of GaN and Silicon FETs

Device	GaN FET	Silicon FET
Device Type	eGaN EPC 2016	Emode DMN4027SSD
VDS	100 V	40 V
I_D	11 A	5.4 A
R_{DSON}	16 mΩ	47 mΩ
$V_{GS\ TH}$	1.4 V	1.2 V
Q_{GD}	0.7 nC	3.3 nC
Q_{RR}	0.0 nC	5.1 nC

As seen in the modified GaN based EPS architecture, there are two FDPOLs and an FBCM

with the specifications in Table 4.3 [21].

Table 4.3: EPS Specifications

EPS Blocks	Voltage Specification
FDPOL 1 Output Voltage	3.3 V
FDPOL 2 Output Voltage	5.0 V
FBCM Output Voltage	7.2 V
Lithium ion Battery	7.2 V and 2.2 Ah

To optimize the switching frequency with respect to efficiency, efficiency is measured at different switching frequencies from 100 KHz to 2 MHz for typical load of 200mA for FDPOL2 at 5V as seen in the Figure 4.4.

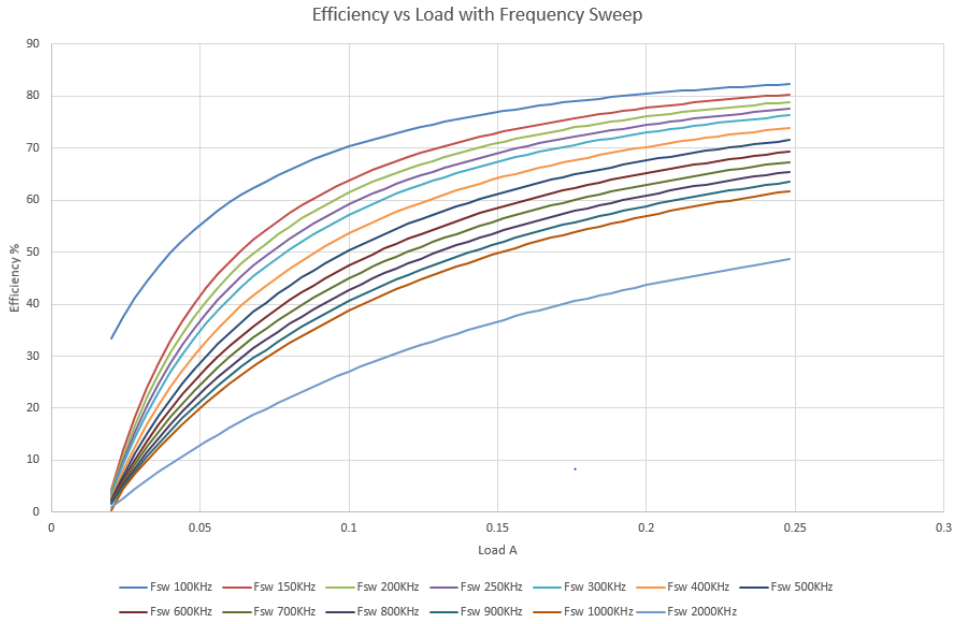

Figure 4.4: Efficiency of GaN based EPS with Frequency Sweep

It is evident from the Figure 4.4 [23] that optimum switching frequency of 600KHz gives

a beter fit for efficiency and switching frequency. Switching frequency of 600KHz is selected for further tests. The EPC 2016 GaN devices are triggered using TIs LM5113 half bridge gate driver. The design is very compact measuring 4.5 x 2.5 inches. The GaN EPS board can be seen in the Figure 4.5. The EPC 2016 GaN FETs under microscope can be seen as Figure 4.6.

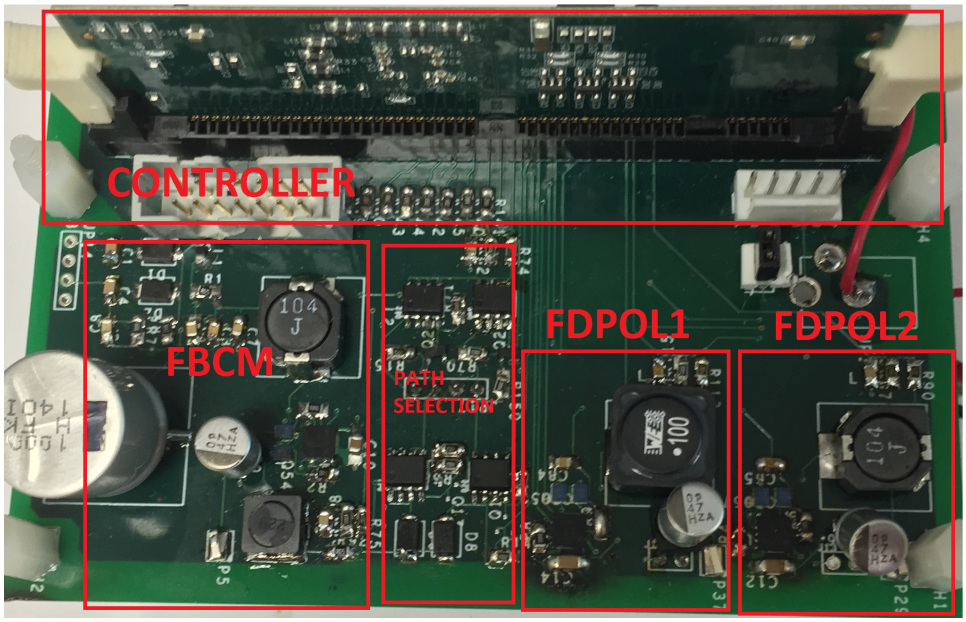

Figure 4.5: PCB for GaN based CubeSat EPS

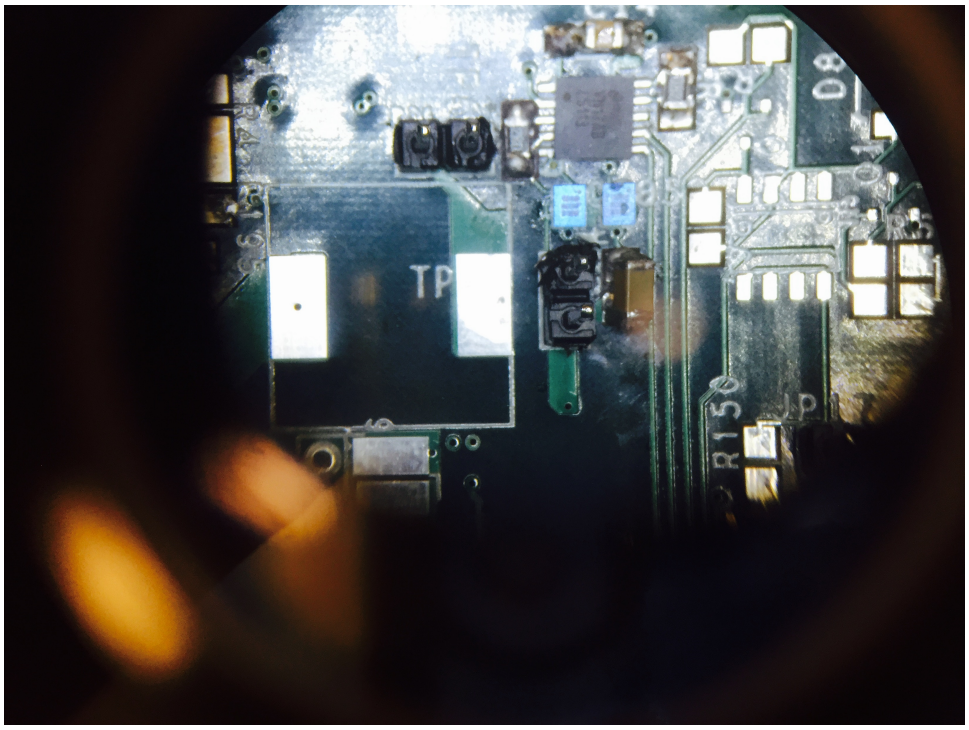

Figure 4.6: EPC 2016 : GaN FET under microscope

4.3 Hardware Design of GaN based EPS

Different functional blocks of an EPS are as follows:

4.3.1 Flexible Battery Charging Module

The Flexible Battery Charging Module (FBCM) is responsible for harnessing solar power to keep the battery banks adequately charged. It forms the interface between the solar panels and the batteries and works like a photovoltaic battery charging system. It is essentially a synchronous boost converter which is programmable on the fly. The FBCM can operate in the constant current or constant voltage mode depending upon the battery state. Schematic of FBCM is in the Figure 4.7. As the battery is rated at 7.2 V, FBCM output voltage is 7.2 V.

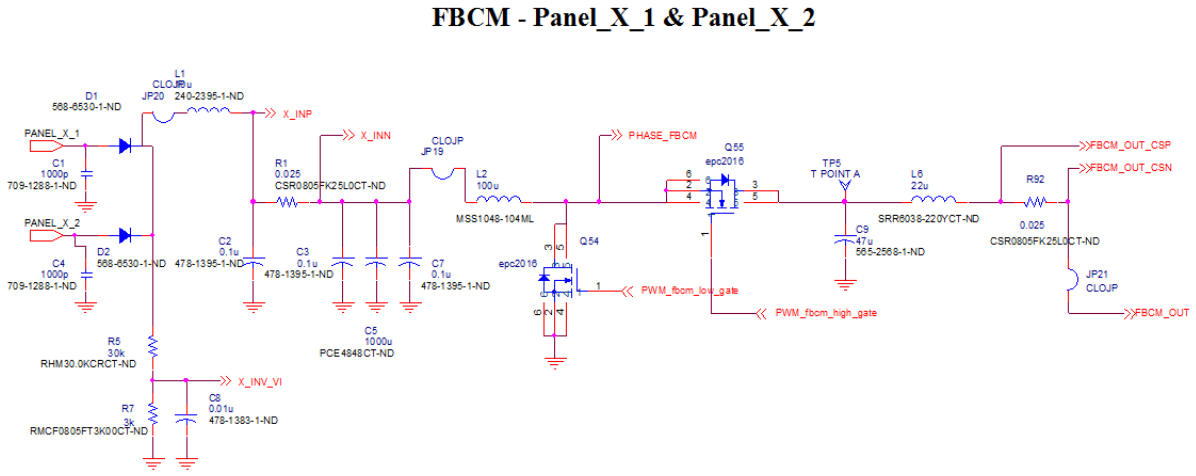

Figure 4.7: Schematic of FBCM

4.3.2 Flexible Digital Point of Load Converter

Flexible Digital Point of Load Converter (FDPOLs) are synchronous buck converters. The ability to provide multiple output voltages enables the operation of multiple peripherals and scientific equipments. The EPS consists of two FDPOLs. These produce rail voltages of 3.3V and 5V. The converters are flexible in the sense that they can be programmed to produce any output voltage within specified parameters. The FDPOLs are powered by the batteries on-board the CubeSat. Schematic of FBCM is in the Figure 4.8 and the gate driver LM5113 is in the Figure 4.9.

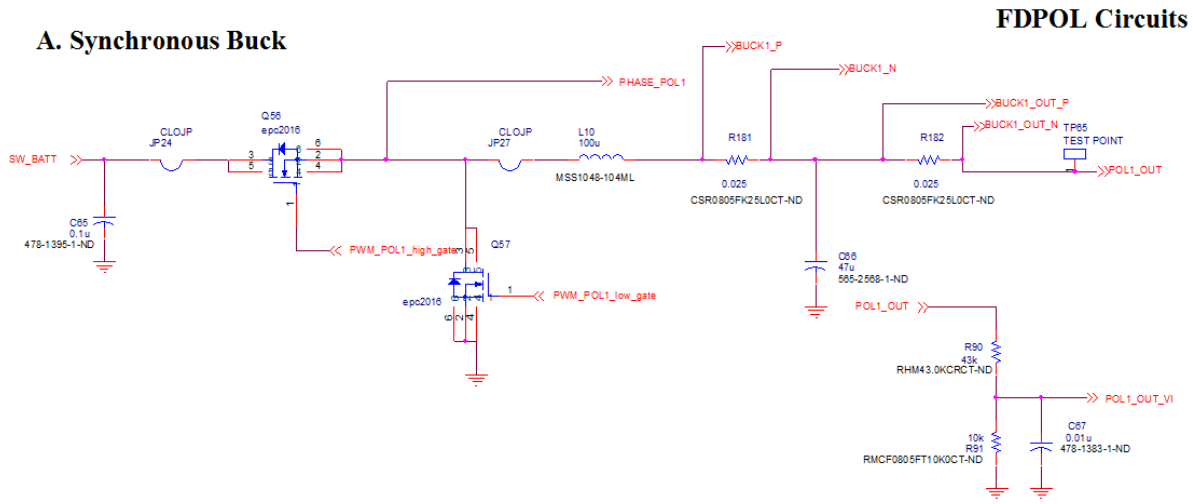

Figure 4.8: Schematic of FDPOL

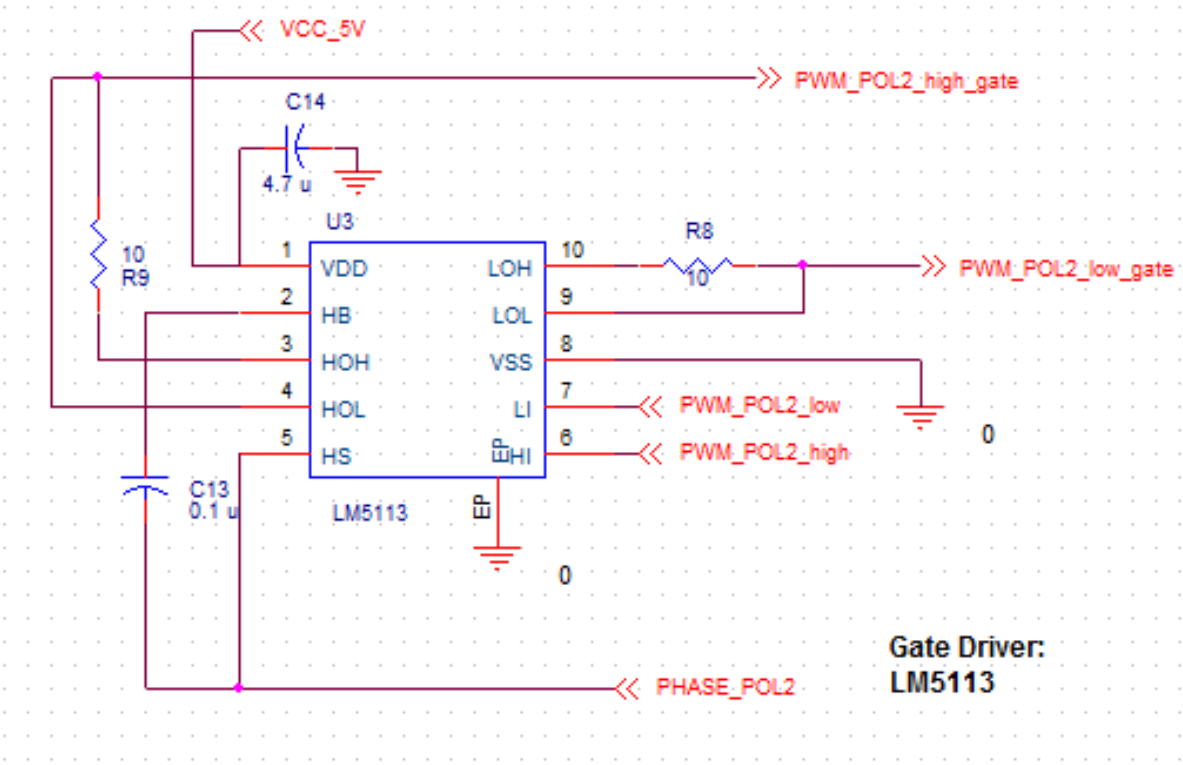

Figure 4.9: Gate Driver Schematic: LM5113

4.3.3 Path Selection

The EPS consists of an assembly of p-type MOSFET switches which are responsible for routing the power to various modules on the board. The output of the FBCM can be routed to either of the two batteries or it can be directly used to power the FDPOLs. The pass transistors are also used to route the power from either of the batteries to the input voltage rail of the FDPOLs. When one battery charges, the other is used to power the input bus. Path selection circuit is in the Figure 4.10.

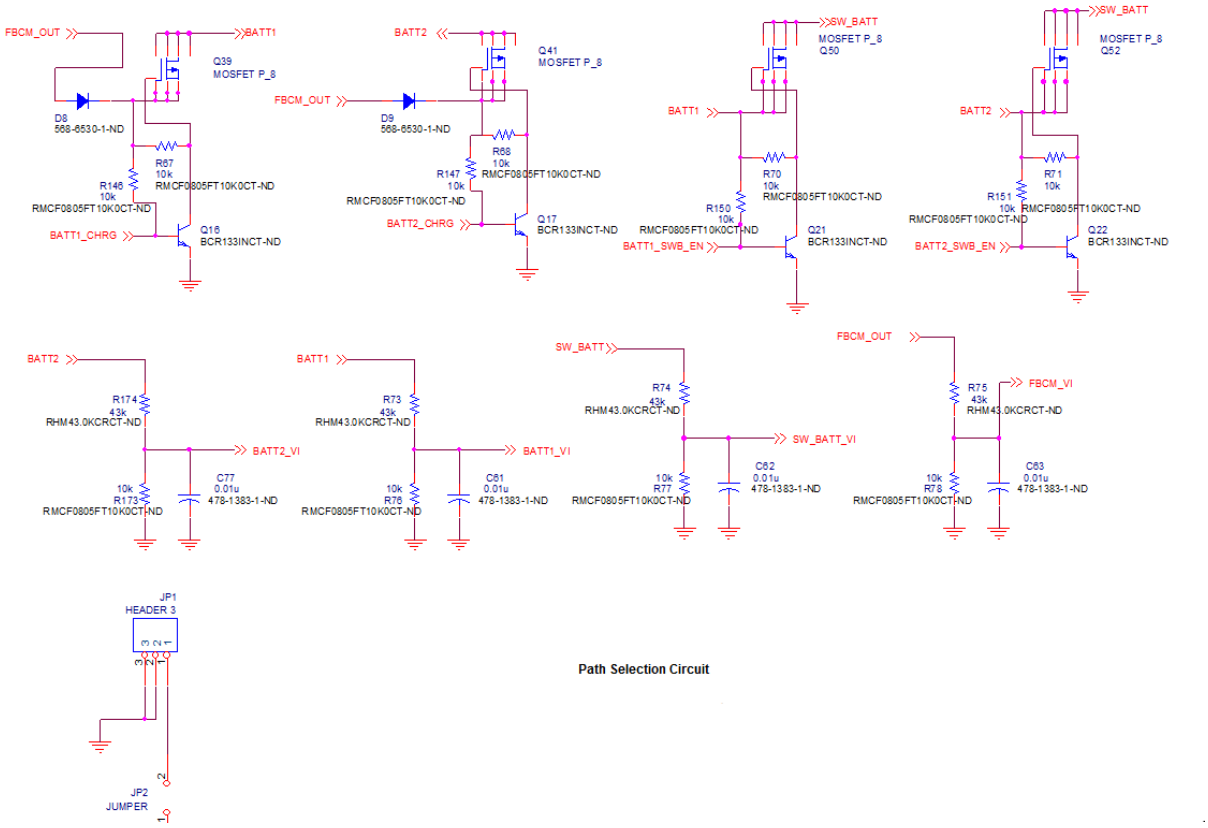

Figure 4.10: Path Selection

4.3.4 Controller and Sensing Circuitry

A digital controller sits at the heart of the EPS and is responsible for proper operation of the system. The system uses TIs TMS320F28335 DSP which runs at 150MHz. The proper operation of the EPS requires that voltages and currents at critical junctions be continuously monitored. The voltages are fed into the ADC of the controller and since these voltages exceed the maximum

limit for the ADC, the voltage being monitored is fed to controller via a resistor divider network. Since very high value resistors are used, minimal losses are incurred. The current is measured by measuring the potential difference across a low loss sense resistor measuring 25 mΩ; the difference is fed into a current sense amplifier whose output is read by the ADC.

4.4 Controller Design of GaN based EPS

4.4.1 FDPOL Compensator Design

The two synchronous buck converters are designed to output a voltage of 3.3V and 5V. A small signal model of the converter is developed. Eq. 4.1 represents the transfer function of the synchronous buck converter as shown in the 4.11. Gvd is the small signal duty cycle to output voltage transfer function. This transfer function needs to be regulated to maintain a constant output voltage with acceptable overshoot and settling times.

$$G_{VD(s)} = \frac{[V_g R_o/(R_o + r_L)](1 + sr_c C)}{1 + [C(r_c + \frac{R_o r_L}{R_o + r_L}) + \frac{L}{R_o + r_L}]s + [LC(\frac{(R_o + r_c)}{R_o + r_L})]s^2} \tag{4.1}$$

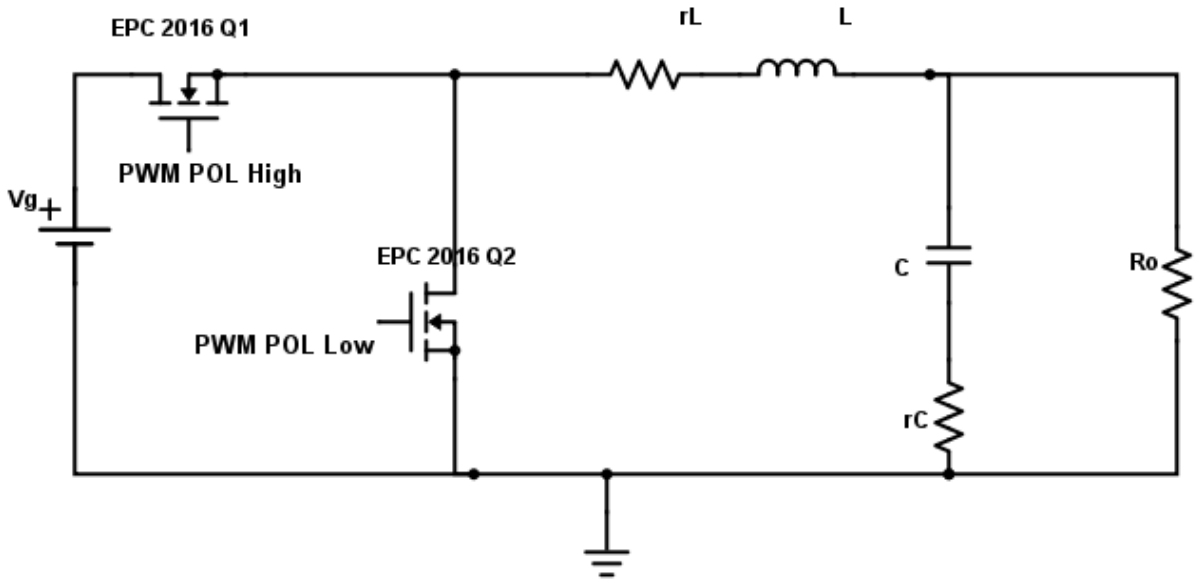

Figure 4.11: FDPOL Schematic

The analog transfer function is converted into discrete time transfer function using zero

order hold with a sampling period of 100 μs and a PI compensator is designed for the same. Figure 4.12 is the step response for a 20 Ω load and 3.3 V output voltage which makes it a step change in current from 0A to 165mA. Figure 4.13 is a 5 V converter and is a step change from 0 A to 250 mA.

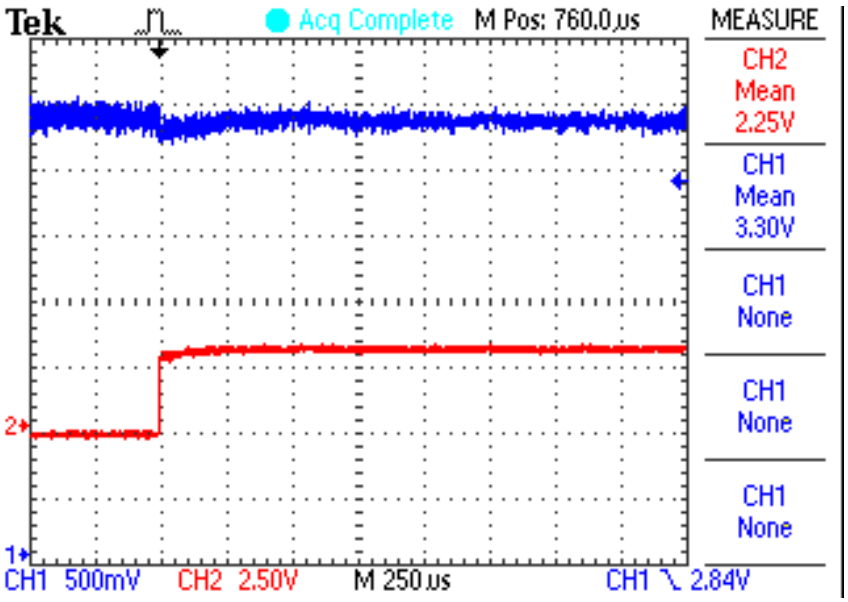

Figure 4.12: Closed Loop Response - Buck Converter at 3.3 V

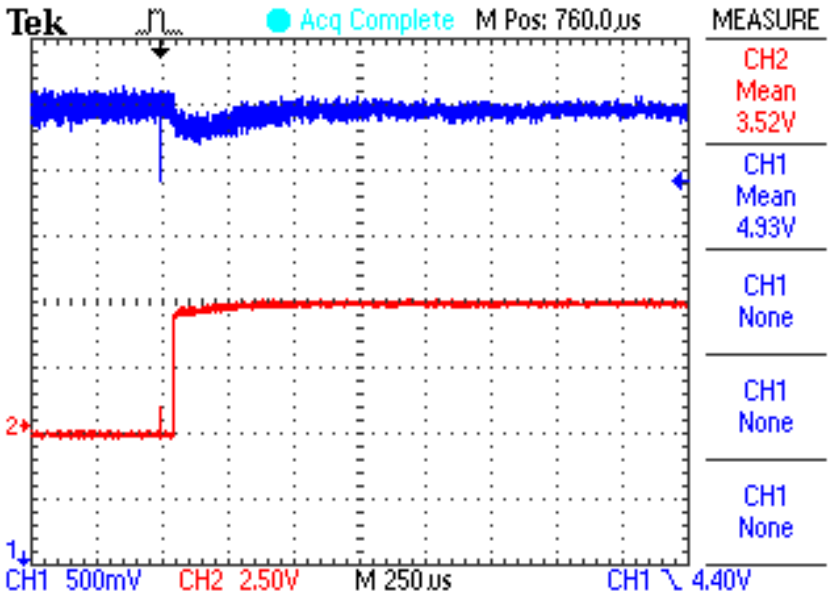

Figure 4.13: Closed Loop Response - Buck Converter at 5 V

4.4.2 FBCM Compensator Design

The purpose of a flexible battery charging module (FBCM)is to provide an interface between the solar panel and the battery. The compensator design procedure for an FBCM is different from that of an FDPOL as the FBCMs module acts as a photovoltaic battery charging system. As FBCM is a synchronous boost converter, a small signal model for a boost converter can be applied for its regulation. The small signal duty cycle to output voltage transfer function is given by Eq. 4.2, Eq. 4.3 for the boost model shown in theFigure 4.14 [4].

$$G_{VD(s)} = \frac{[(R_o + r_c)](1 + sr_cC)[-(sL + r_L)(R_o + r_c) + (D'^2)(R_o^2)][R_oV_g]}{P_{(s)}[D'R_o(D'R_o + r_c) + r_L(R_o + r_c)]} \tag{4.2}$$

where,

$$P_{(s)} = s^2LC(R_o+r_c)^2+s[L(R_o+r_c)+r_LC(R_o+r_c)^2+D'R_or_cC(R_o+r_c)]+(R_o+r_c)+D'R_o(D'R_o+r_c) \tag{4.3}$$

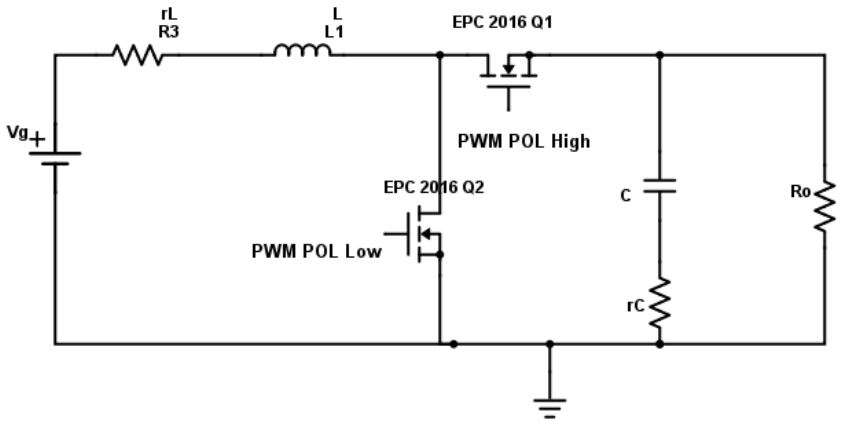

Figure 4.14: FBCM Schematic

The batteries are charged using constant current - constant voltage (CC$\longleftrightarrow$CV) technique. To accomplish this, a dual loop control scheme is employed. This enables the converter to operate in constant current as well as constant voltage mode.

Constant Voltage Mode

A PI compensator is implemented for the discrete time transfer function of the boost converter. Figure 4.15 shows the step response of a boost converter powering a battery load in constant voltage mode. The red trace is that of the battery voltage while the blue trace represents the converter output voltage. The FBCM input voltage is 4V and the output is 7.2V.

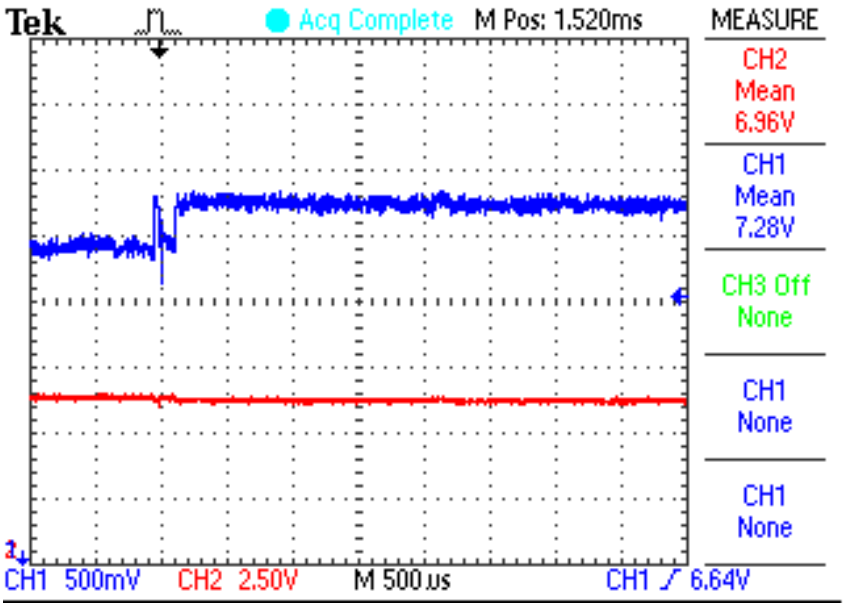

Figure 4.15: FBCM Boost Constant Voltage Mode-Converter Output voltage

Constant Current Mode

Charging the battery with constant current poses a challenge as the control loop runs in voltage mode control. The regulation of output current requires sensing it, which in turn requires a high bandwidth current sensor. This is difficult to accomplish for digital systems employing a low sampling rate. Hence, a tradeoff is established which regulates current within acceptable range. Some implementations have used inductor current control for regulating output current while others control algorithms are based on battery current control. However, a direct control scheme for the output current was found to perform better for the CubeSat application. Figure 4.16 shows the control loop diagram of FBCM running in constant current mode. This scheme employs two control loops $\Longrightarrow$outer current loop and inner voltage loop. The voltage loop is similar to the voltage control loop employed in constant voltage control. The outer current loop measures the output current and compares it to the desired current reference. The error term is fed to a PI compensator which generates the voltage reference. The voltage loop runs around 10 times faster than the current loop. Figure 4.17 shows the FBCM running in constant current mode. The red trace depicts the battery voltage while the blue trace shows the current. The current reference is set at 0.45A and current measurement scale is 1Vto 0.34A.

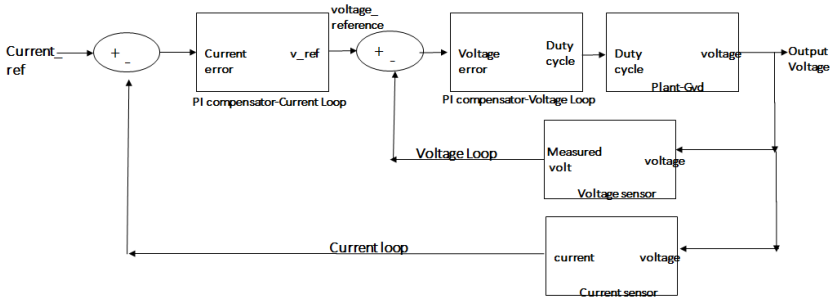

Figure 4.16: FBCM Constant Current Mode Control Loop Block Diagram

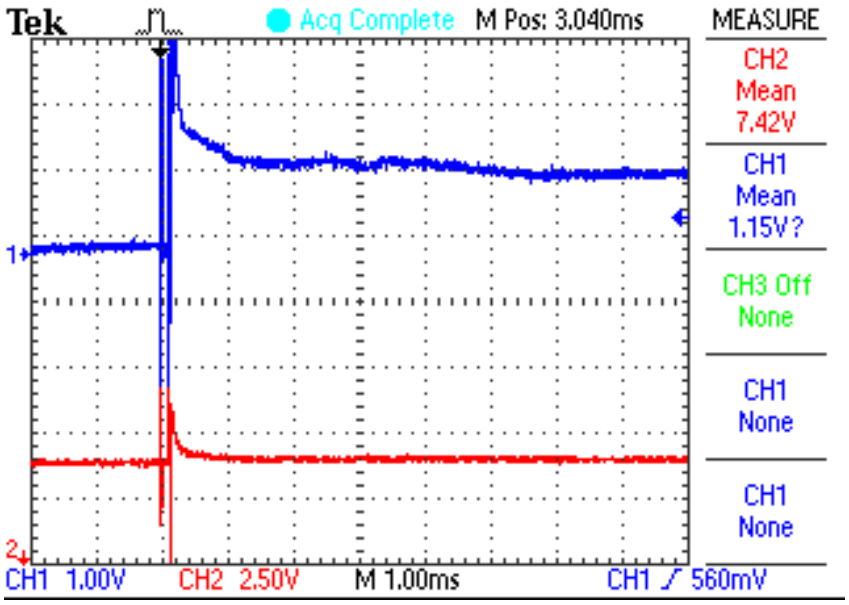

Figure 4.17: FBCM Constant Current Operation

Path Selection

The path selection feature of the EPS provides enhanced configurability and scalability and ensures that the FDPOLs get necessary input power and remain in operation. Assuming that initially battery 1 is powering the FDPOLs and battery 2 is on standby; if battery 1 gets discharged, battery 2 is connected to the FDPOL input while battery 1 is connected to the FBCM output for charging. The traces in Figure 4.18 demonstrate the path selection feature and it also shows the effect of changing FDPOL input on the FDPOL output voltage. The

yellow trace shows the output of FDPOL buck converter operating at 3.3V. The purple and green traces show voltages of battery 1 and 2 respectively. The blue trace shows the FDPOL input. Initially, battery 1 is connected to input of FDPOL. When the voltage of battery 1 starts to decrease, the FDPOL input voltage decreases along with it (the blue trace follows the purple trace). If the voltage goes below a certain threshold, the path is switched and battery 2 is connected to the FDPOL input (the blue trace now follows the green trace).

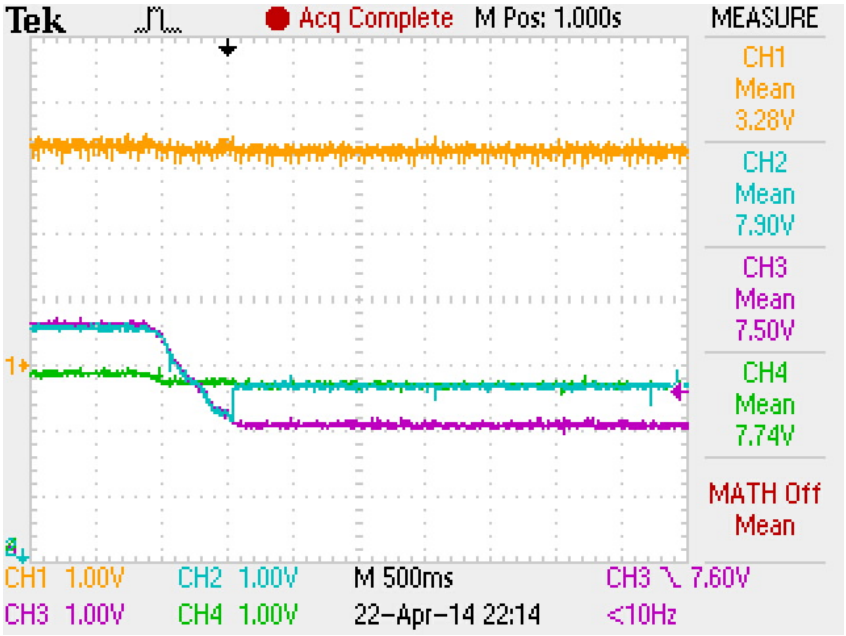

Figure 4.18: FBCM Path Selection

Chapter 5

Power Loss Analysis: Silicon Mosfet based EPS

The primary focus of this research has been the design of intelligent and efficient Electric Power System (EPSs) for the CubeSat. Efficiency is a very critical design constraint for EPS of CubeSat. To design an efficient converter it is important to analyze the power loss. Power loss of a synchronous buck or boost converter includes several factors: MOSFET loss, inductor loss, printed-circuit board (PCB) loss, etc. MOSFET-related power loss is composed of conduction loss and switching loss. For a synchronous Buck converter, sum of high side (HS) and low side (LS) FETs' conduction loss contributes to total Conduction loss. This loss is independent of switching frequency. Switching loss consists of HS FET switching loss, LS FET switching loss, LS body diode loss, gate drive loss and FET's output capacitance loss. A single Buck FDPOL of Silicon based EPS is analyzed in detail to benchmark the results with reference to GaN based EPS. Mosfet takes finite time to turn on and off. During the turnon and turnoff transitions, due to the clamping effects of the low side device, the HS device is affected by both high current and high voltage at the same time as they overlap for a very short time, which induces switching losses as seen in Figure 5.1 [24].

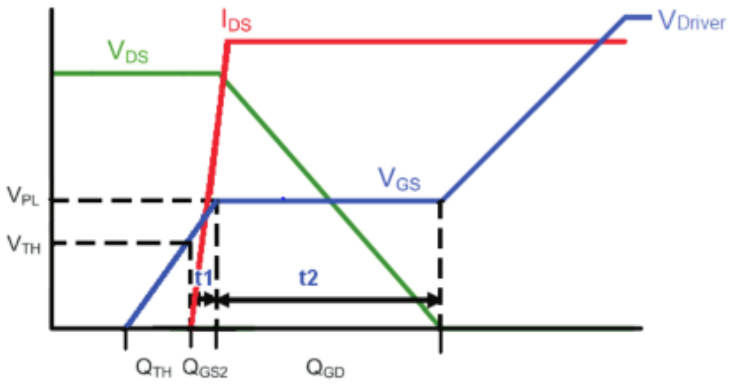

Figure 5.1: Device Turn On Waveform

Detailed analysis of power loss is as follows:

1. Switching Loss
2. Conduction Loss
3. Body-Diode Loss

5.1 Switching Loss

As mentioned, the clamping effect of LS switch causes a definite voltage and current across HS switch for a short time causing switching loss. Consider the turn off mechanism of HS switch as shown in Figure 5.2.

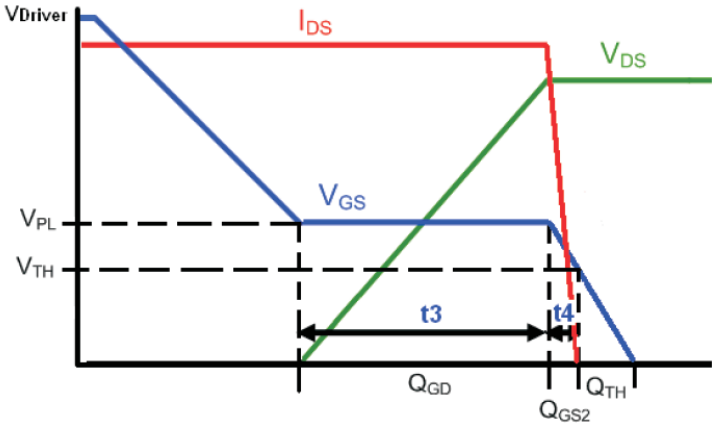

Figure 5.2: Device Turn Off Waveform

Referring to the Figure 5.3, Channel 2 (C2) is the gate voltage with respect to ground (VG), Channel 3 (C3) is the source voltage with respect to ground (VS) of HS switch. Channel 1 (C1) is the drain current of HS (ID HS) and Channel 4 (C4) is the drain current (ID LS) of LS switch. The trace F1 is the gate-source voltage (VGS) by taking the difference of C2-C3. It can be seen that there is a voltage plateau of 1.1V for 40ns. During this voltage plateau of VGS, HS MOSFET turns off and the drain current ID HS (C1) goes to zero, while the LS MOSFET turns on and the drain current ID LS (C4) reaches the inductor current. When closely observed, as the gate drive voltage VG goes to zero during turn off, the drain current ID HS will fall towards the off state at 0 Ampere. If noticed, source voltage C3 (VS) drops to zero in 20 ns but ID HS goes to 0 A in 40 ns. This rate of change of drain current through PCB tracks will generate a backward voltage V_b as given in Eq. 5.1 [25].

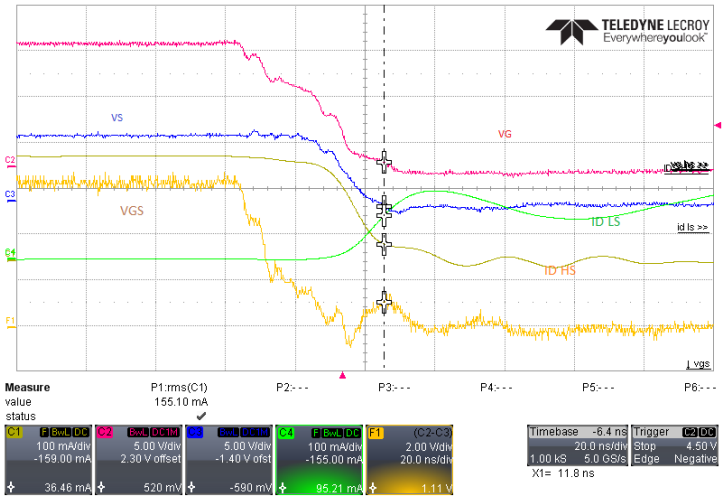

Figure 5.3: High Side Si-Mosfet Turn Off

$$V_b = L\frac{dI_{drain}}{dt}. \tag{5.1}$$

This backward voltage Vb pulls the source voltage in a negative direction with respect to the gate hence allowing current to continue to flow though the gate voltage is firmly held to ground. As the current falls linearly, the backward voltage is given by 5.2 , which creates a voltage plateau of fixed level with time until current completes its transition.

$$L\frac{dI_{drain}}{dt} = constant. \tag{5.2}$$

The voltage plateau of VGS=1.1 V is barely above the gate threshold voltage VGS_{th} of 1.0 V and thus the channel is not fully enhanced. This causes the HS mosfet to operate as a current source where the current level is maintained by the voltage plateau. Thus the drain current flows through the HS mosfet while the voltage across it is V_{cc} causing higher losses during the turn off. This explanation can be extended for turn on instant of HS mosfet but the turn On loss is lower than the turn Off loss because in the turn-on transition, the HS MOSFET is actively being driven by the gate driver; and hence, we have fast transition controlled to a large degree by the gate driver and to a lesser degree by the source parasitic inductance. Turn-off transition of HS mosfet is driven by the back EMF voltage as seen in 5.2. Turn on sequence can be seen in Figure 5.4.

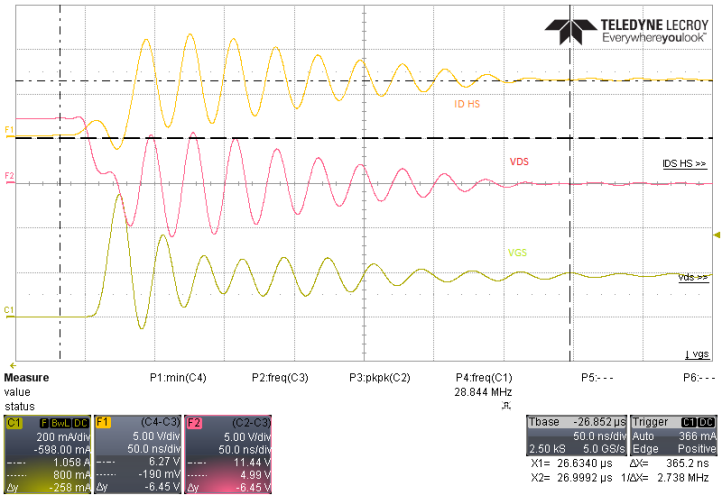

Figure 5.4: High Side Si-Mosfet Turn On

Referring to Figure 5.5, equations for switching power loss can be given as in equations 5.3, 5.4, 5.5, 5.6.

$$P_{HSSW} = P_{HSSWON} + P_{HSSWOFF} \tag{5.3}$$

$$P_{HSSWON} = 0.5 x V_{IN} x [I_{OUT} - \frac{I_{RIPPLE}}{2}] x F_{SW} x \frac{Q_{SW}}{I_G} \tag{5.4}$$

$$P_{HSSWOFF} = 0.5 x V_{IN} x [I_{OUT} + \frac{I_{RIPPLE}}{2}] x F_{SW} x \frac{Q_{SW}}{I_G} \tag{5.5}$$

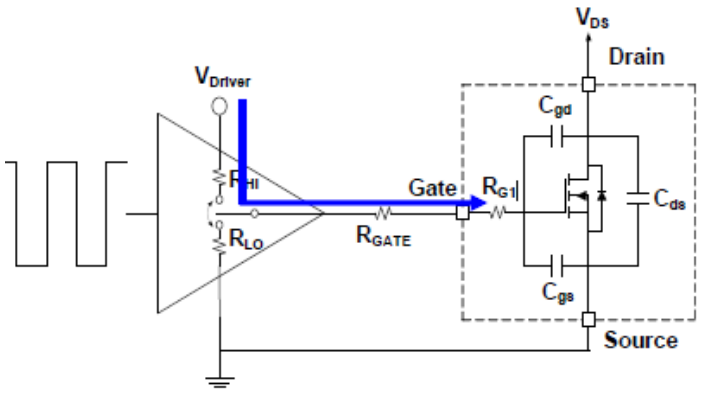

Figure 5.5: High Side Si-Mosfet Schematic

$$I_G = \frac{V_{DRIVER} - V_{PL}}{R_{HI} + R_{GATE} + R_{G1}} \tag{5.6}$$

5.2 Conduction Loss

The other source of power loss for switches is conduction loss across HS and LS which is given as equation 5.7.

$$P_{cond} = I_{rms}^2 x R_{DSON} \tag{5.7}$$

Conduction Loss is comprised of HS mosfet conduction loss and LS mosfet conduction loss. RMS current through HS and LS mosfets is a function of duty cycle and conduction period as seen in Figure 5.6, Figure 5.7, Figure 5.8 and Figure 5.9 [26].Thus conduction loss is highly dependent on the on-resistance of the mosfet and the RMS current through the device. On-resistance R_{DSON} is quite low for GaN as compared to Silicon mosfets.
Silicon mosfet: DMN4027 SSD13 is used for silicon version of EPS which has R_{DSON} of 47 mΩ. GaN EPC 2016 is used for GaN version which has R_{DSON} of 16 mΩ. Hence conduction loss for GaN device is comparatively lesser than Silicon counterparts. This can be confirmed from the efficiency curves in the next section for both Silicon and GaN based EPS.

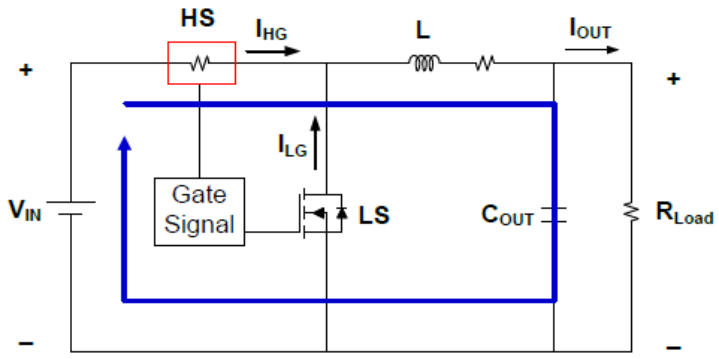

Figure 5.6: High Side Si-Mosfet Conduction schematic

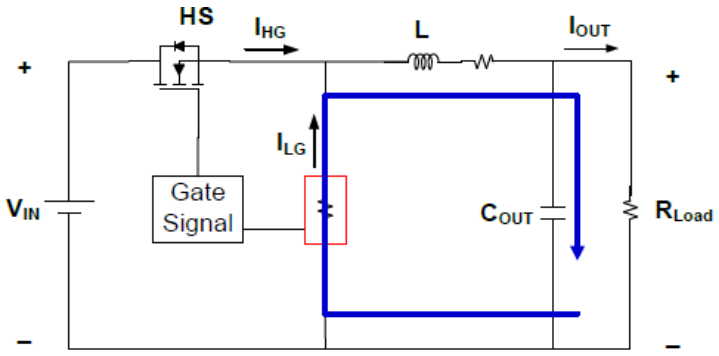

Figure 5.7: Low Side Si-Mosfet Conduction schematic

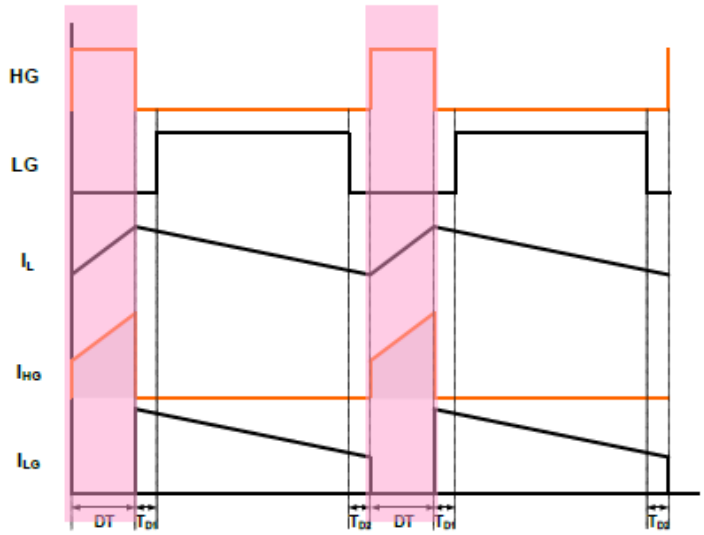

Figure 5.8: High Side Si-Mosfet Conduction ON Period

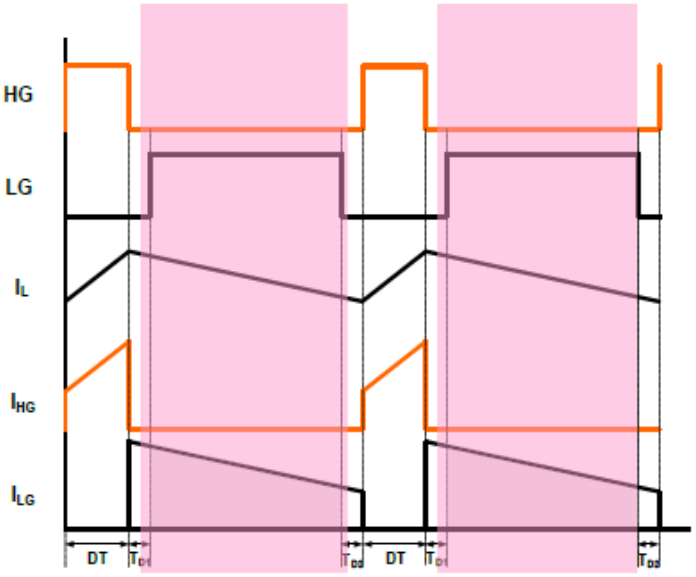

Figure 5.9: Low Side Si-Mosfet Conduction ON Period

Conduction Loss for HS and LS mosfets can be calculated as given in equations 5.8 and 5.9.

$$P_{cond_HS} = I^2_{rms,HS} x R_{DSON,HS} \tag{5.8}$$

$$P_{cond_LS} = I^2_{rms,LS} x R_{DSON,LS} \tag{5.9}$$

Where,

$$I_{rms,HS} = \sqrt{Dx[I^2_{OUT} + \frac{I^2_{RIPPLE}}{12}]} \tag{5.10}$$

$$I_{rms,LS} = \sqrt{[1-D]x[I^2_{OUT} + \frac{I^2_{RIPPLE}}{12}]} \tag{5.11}$$

High Side and Low Side drain currents and gating sequence can be seen in Figure 5.10 and Figure 5.11.

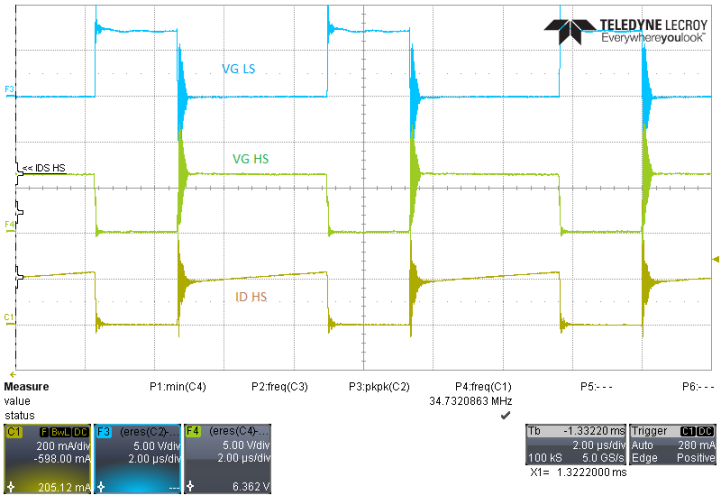

Figure 5.10: HS Drain current and Gating Sequence in Si-EPS

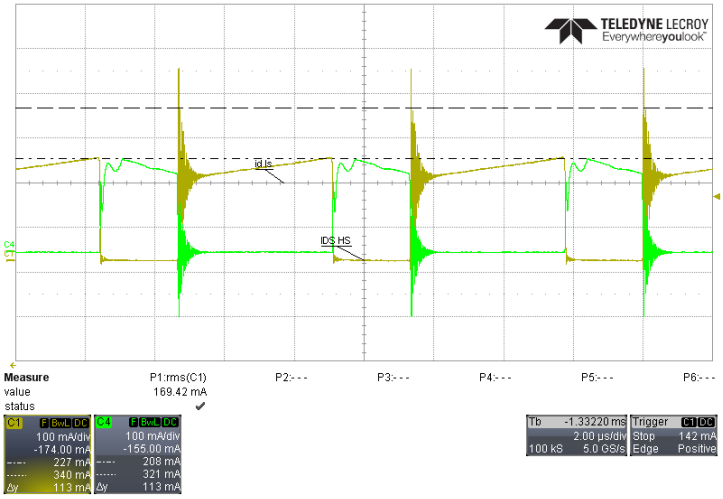

Figure 5.11: HS and LS Drain current in Si-EPS

5.3 Body-Diode Loss

Definite dead time is required during turn off and turn on of respective switches to prevent the cross-conduction of HS and LS mosfets. Dead time induces body diode conduction loss when LS mosfet's body diode conducts during rising edge dead-time between LS mosfet turnoff and HS mosfet turnon and falling edge dead-time between HS mosfet turnoff and LS mosfet turnon as shown in Figure 5.12.

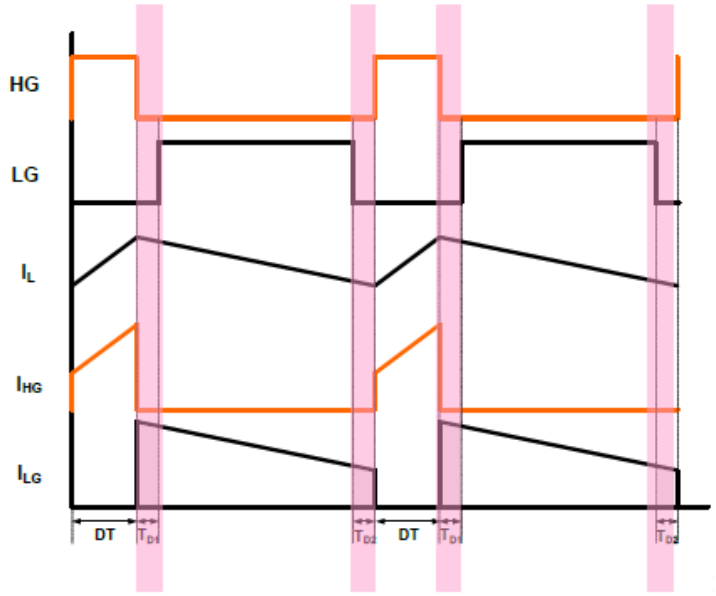

Figure 5.12: Body diode conduction during dead time

Dead time body diode conduction loss can be quantified as equation 5.12.

$$P_{deadtime} = V_{SD}x[(I_{OUT} - \frac{I_{RIPPLE}}{2})xt_{deadtime(rise)} + (I_{OUT} + \frac{I_{RIPPLE}}{2})xt_{deadtime(fall)}]xF_{sw} \tag{5.12}$$

$T_{deadtime}$ for silicon mosfet based EPS is 0.3μsec at F_{sw}=150KHz.
Efficiency sweep vs load for Silicon based EPS can be seen in Figure 5.13 and the calculated power loss at 0.2 A is tabulated in Table 5.1 [27].

Table 5.1: Power Loss: Calculation and Measurement at Io= 0.2A

Power Loss (W)	Measured (W)	Calculated (W)	Error (W)
-	0.142312	0.1229	0.01941

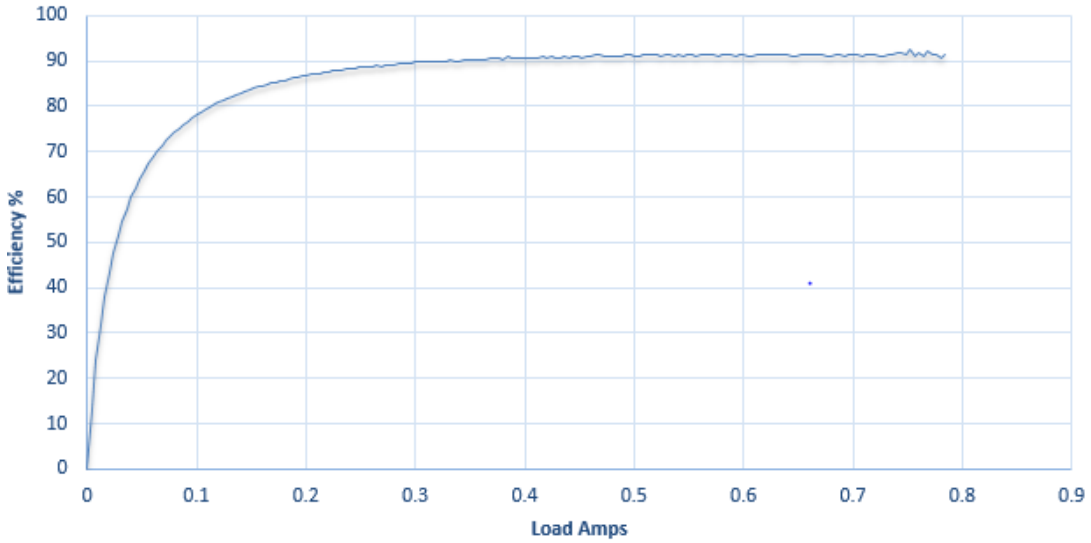

Figure 5.13: Efficiency vs Load of Silicon -EPS

Chapter 6

Pulse Frequency Modulation

Switching DC/DC converters are very effective in terms of efficiency over a wider range of input voltage. LDOs suffer from efficiency when the voltage headroom between input and output voltage increases. Voltage regulation in switching converters is achieved by pulse width modulation (PWM) that switches the power MOSFETs in a closed loop control. PWM works well for mid-range to heavy load conditions but efficiency of converters in PWM mode is severely hit in light load conditions. This can shorten battery life in applications like cubesat when the "standby" mode time is considerable. This could reduce overall efficiency if a system frequently operates at light load. As mentioned in previous chapter, losses of a synchronous converter can be grouped as conduction loss, switching loss and also fixed loss which is consumed by the controller of closed loop control and is constant. In a broader sense these losses can be explained as dc losses and ac losses. The dc losses are determined mainly by on-resistance (R_{DSON}) in the low-side and high-side MOSFETs and the DC resistance (DCR) of inductor which scales up with the load current. The ac losses consist mainly of switching losses which is a dead-time loss. The ac losses are proportional to the MOSFET switching frequency. At typical medium load conditions, conduction or dc loss dominates the switching loss and increases with load as shown in the Figure 6.1. Switching loss remains constant over the full range of load [28].

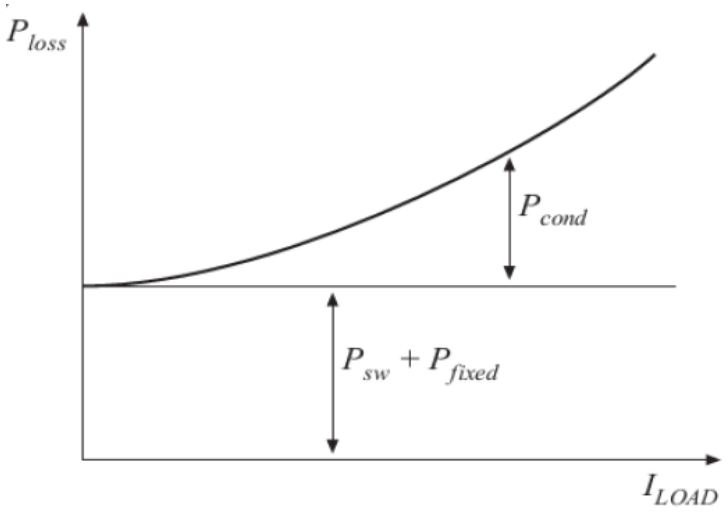

Figure 6.1: Variation of Losses in a Fixed Frequency Converter

When the converter is under light load, the gate-drive losses, which heavily depends on the switching frequency, consumed when charging and discharging the gate capacitances of the power MOSFETs during switching transitions, dominate over conduction loss. Thus, to improve efficiency of switching converters at light loads it is important to make the switching loss scalable with load current as shown in the Figure 6.2.

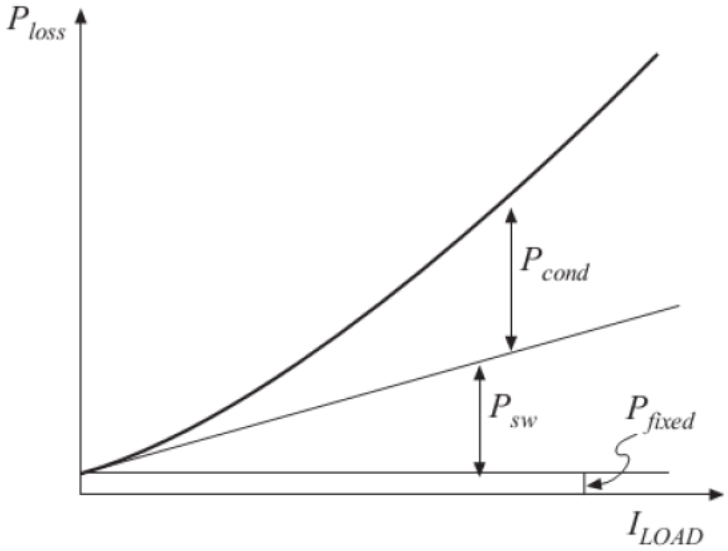

Figure 6.2: Variation of Losses in a Variable Frequency Converter

This can be achieved by implementing a modified modulation technique- pulse frequency modulation (PFM) which is also known as Light Load Management. Total system efficiency is further improved when the converter automatically selects between the two modes: PFM and PWM, to give the best efficiency for any given load. For synchronous converters, at light loads the inductor current can change from positive to partially negative. As the inductor current goes negative it discharges the output capacitor and thus it causes more loss which can reduce the efficiency of the converter. To avoid this the synchronous converter is made to operate as a non-synchronous converter by stopping the inductor current to go negative. In PFM mode a zero current detection circuit is required to switch OFF the lower MOSFET as soon as the inductor current goes negative. PFM mode lowers the switching frequency, thereby lowering the switching losses in the converter.

6.1 PFM Control Architecture

The important blocks of PFM Control architecture are as follows:

1. Hysteritic Comparator for Upper and Lower Threshold Output Voltage
2. Current Sensing Block
3. Zero Current Detection
4. Boundary condition for PFM to PWM
5. Inductor Peak Current Limit for PFM

6.1.1 Hysteritic Comparator

In pulse frequency modulation mode (PFM), power switches are controlled by output voltage thresholds. Hysteritic comparator is a better choice for control of switches for voltage thresholds [29],[30]. Referring to the schematic of PFM architecture in the Figure 6.3, hysteretic comparator can be explained as follows.

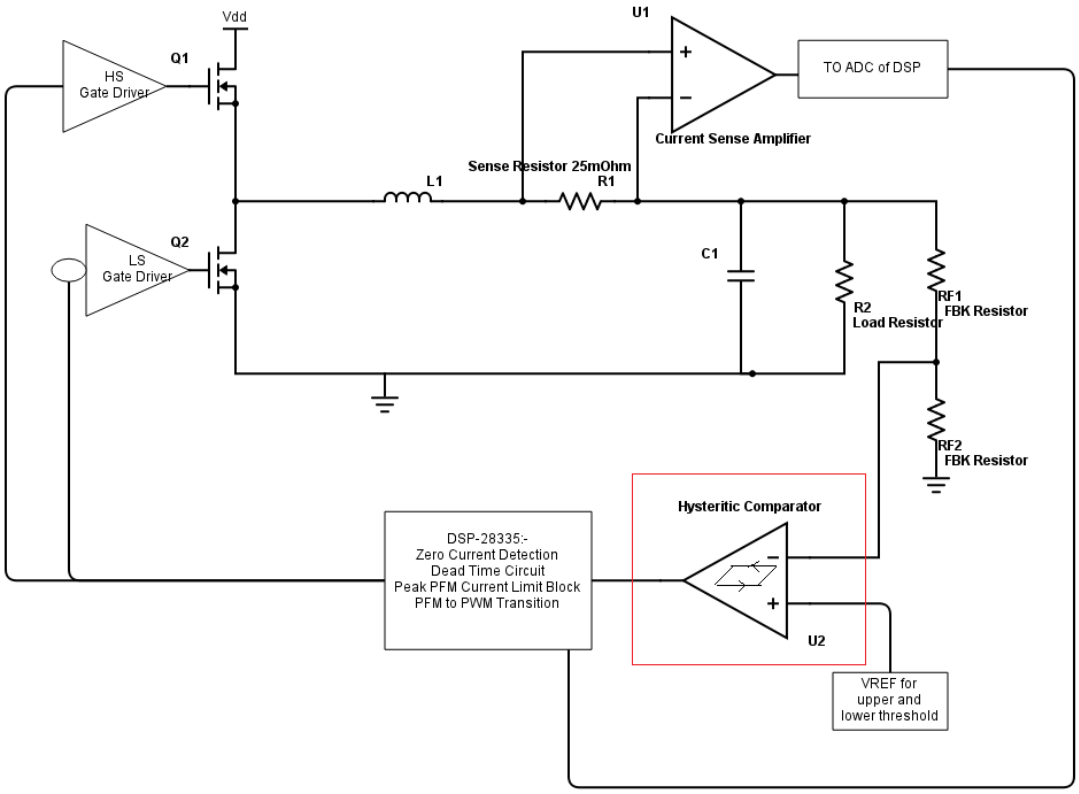

Figure 6.3: PFM Architecutre: Hysteritic Comparator

If the output goes lower than the lower threshold voltage, the hysteritic comparator trips and turns ON the HS MOSFET. HS MOSFET remains ON till the peak PFM inductor current limit is reached. Inductor current will increase for time interval dt1 until it reaches the current limit as given by the Eq. 6.1.

$$dt1 = \frac{I_{PEAKPFM} x L}{V_{IN} - V_{OUT}}. \tag{6.1}$$

Once the limit is reached, the LS MOSFET turns ON. During this interval, inductor current decreases as given by the Eq. 6.2.

$$dt2 = \frac{I_{PEAKPFM} x L}{V_{OUT}}. \tag{6.2}$$

Once this period is over, HS MOSFET turns ON again and this sequence repeats till the upper threshold voltage of the hysteretic comparator. Thus, there are two references for the hysteretic comparator- Upper and Lower thresholds to take the decision.

6.1.2 Current Sensing

Average current sensing method is implemented for sensing current. In this method the average current flowing through the inductor is sensed. The average current to be sensed is proportional to the DC voltage drop across the sense resistor of 25 mΩ in series with the inductor. In steady state the inductor acts as a short and hence no DC voltage drop across it. Thus, the DC voltage drop across the sense resistor is a measure of load current as seen in the Figure 6.4. Since the typical load is less than 1 Amp, power loss across the sense resistor is negligible. The potential drop across the sense resistor is fed to the current sense amplifier MAX9920 with a current sense gain of 7.5 to boost the voltage so that the ADC of DSP TMS320F28335 can sense it without any effect of noise.

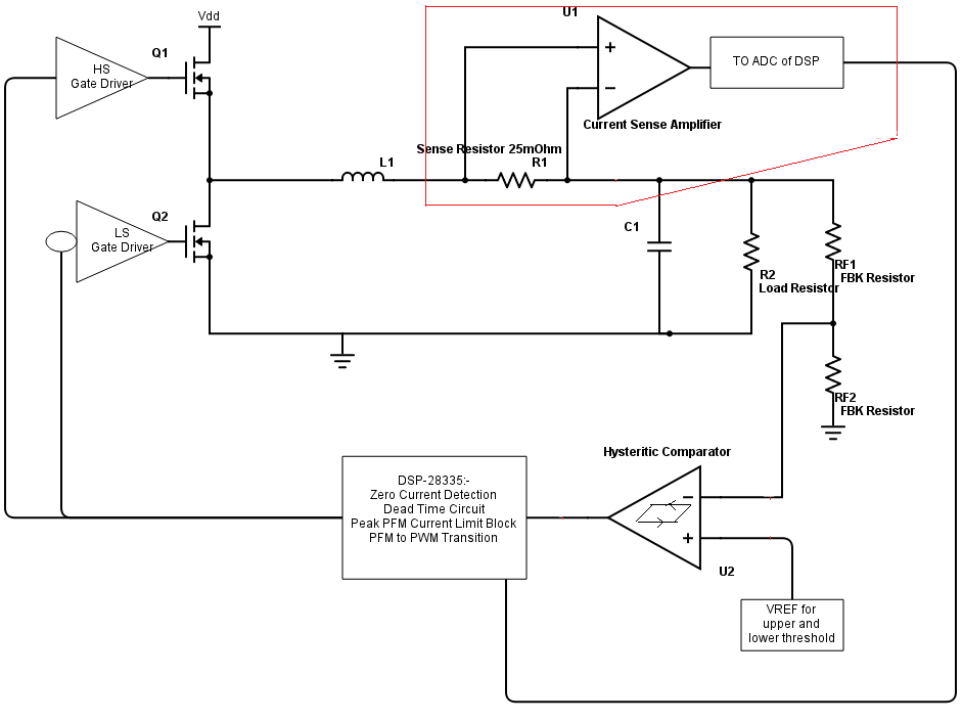

Figure 6.4: PFM Architecutre: Current Sense

6.1.3 Zero Current Detection

Zero Current Detection is a very critical block towards functioning of PFM. When the load becomes smaller, inductor current can change its polarity to go negative. Output capacitor is discharged by this negative inductor current and causes additional losses. To prevent this loss

it is important to clip the inductor current to 0 Amp from going to negative value. Therefore, efficiency can be further increased by operating the converter in a nonsynchronous mode, in which a zero crossing detection circuit would turn OFF the LS MOSFET when the inductor current goes negative. Zero current detection is the action taken by DSP on the sampled inductor current as seen in the Figure 6.5.

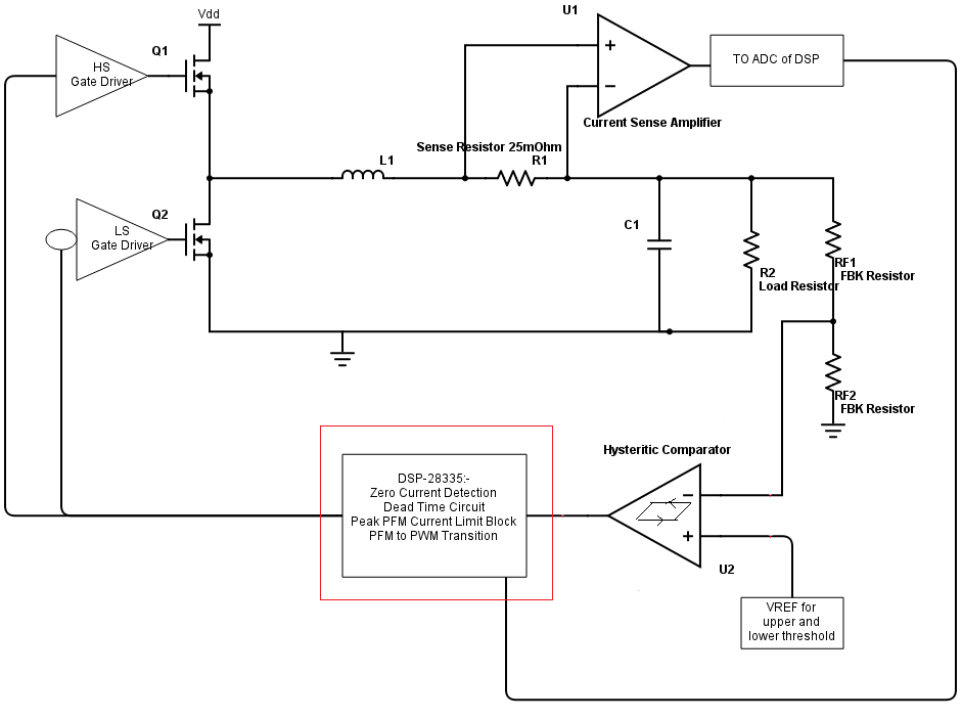

Figure 6.5: PFM Architecutre:Zero Current Detection

6.1.4 Boundary condition for PFM to PWM

This is a configurable limit to make a transition from PFM to PWM as the load increases from light load condition to moderate or higher loads. This boundary condition for PFM to PWM depends on the optimum value of inductor current based on efficiency. Further tests that are conducted for FDPOL, this boundary condition of PFM-PWM transition is set at 100 mA. Boundary condition is set in DSP as shown in the Figure 6.5.

6.1.5 Inductor Peak Current Limit for PFM

As explained in the previous subsection, inductor current increases till the peak PFM inductor current limit is reached. This limit is adjustable but it is important to note that this current limit is set specifically for PFM mode, and is different from the overcurrent-protection threshold of the converter. This limit also affects the output voltage ripple. The peak inductor current limit decides the ON time for HS MOSFET. Inductor peak current limit is set in DSP as shown in the Figure 6.5.

6.2 PFM Modelling and Hardware

As explained in the previous section, in PFM control, both HS and LS FETs are controlled by set threshold of output voltage and peak inductor current limit. Since PFM is useful only for light loads, the efficiency deteriorates at higher loads with PFM control and hence PFM$\Longleftrightarrow$PWM changer is also required to be a part of control. Much emphasis is laid on the positive inductor current and not allowing it to go below zero. Thus synchronous buck converter is made to operate like an asynchronous buck converter by turning the LS OFF when the inductor current tries to approach less than 0 A. It is important to have the synchronous functioning of the five essential blocks of PFM namely, Hysteretic Comparator for voltage threshold, Current Sensing block, Inductor Peak Current Limit for PFM, Zero Current Detection, Boundary condition for PFM to PWM. The PFM operation and PFM to PWM transition can be well elaborated in the Figure 6.6 [31].

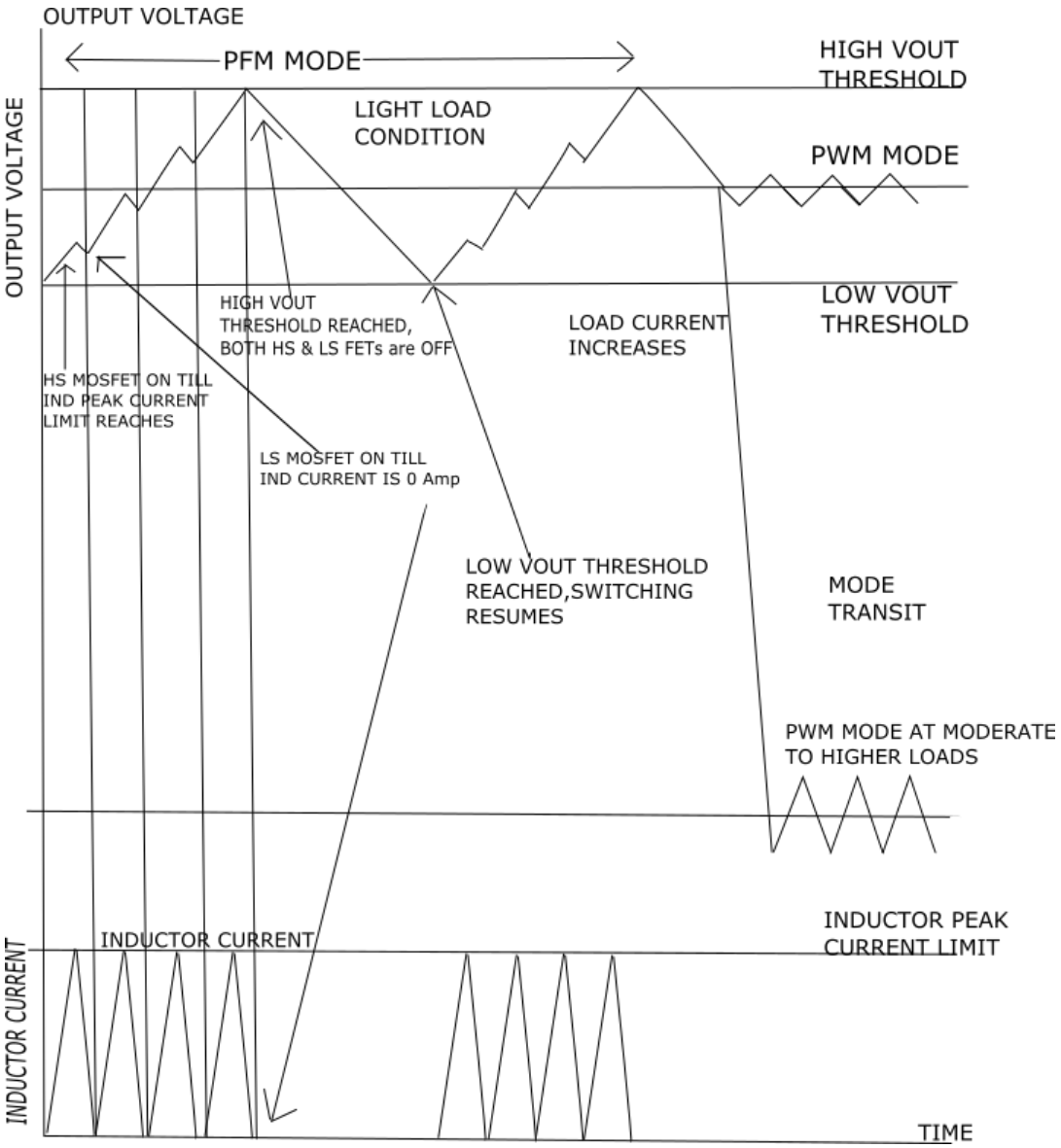

Figure 6.6: PFM Mode Operation and PFM-PWM Transition

When the output voltage reaches lower threshold, HS FET is ON. Inductor current increases till the inductor peak current limit is reached. Once this limit is reached, HS FET turns OFF and LS FET is turned ON. LS FET is ON till the inductor current is positive. As the inductor current reaches zero and tends to become negative, zero current detection detects it and turns LS FET OFF and switches ON the HS FET. This sequence repeats till the output voltage increases to upper threshold voltage. As the upper threshold of output voltage is reached, both HS and LS FET turns OFF. During this the switching doesn't take place and this is called as

the 'sleep phase'. The reason for reducing power loss in this control mode is mainly due to the 'sleep phase' as the output voltage reaches above high threshold and thus both the switches are turned OFF till lower threshold is reached and thus capacitor sources power to the load. To maximize this phase, threshold difference must be increased and thus voltage ripple increases. As the load current increases above the boundary condition for PFM$\Longleftrightarrow$PWM, PFM mode terminates and the switches are controlled by PWM mode. This transition can be further seen in the efficiency vs load curve.

PFM mode is modelled in both Matlab/Simulink and PSIM [23]. The PSIM blocks for PFM-PWM control are shown in the Figure 6.7.

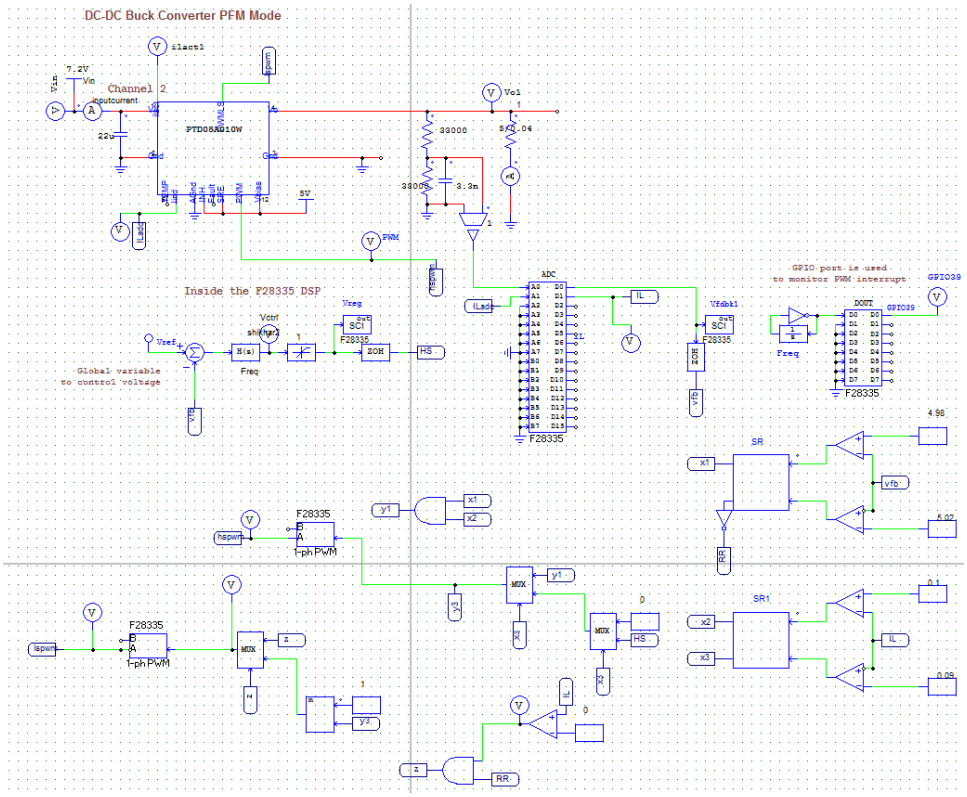

Figure 6.7: PFM-PWM Controller Modelling in PSIM

PFM controller can be seen in the Figure 6.8.

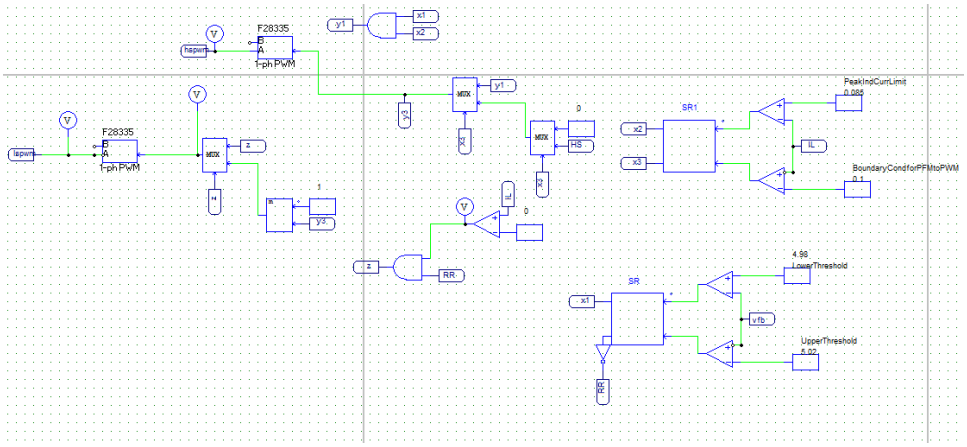

Figure 6.8: PFM Controller in PSIM

6.2.1 Hysteritic Comparator

Hysteritic comparator is seen in Figure 6.9. The hysteretic comparator is comprised of two comparators for lower and upper threshold levels followed by an SR Latch to latch the decision of the comparator till the next threshold limit is reached.

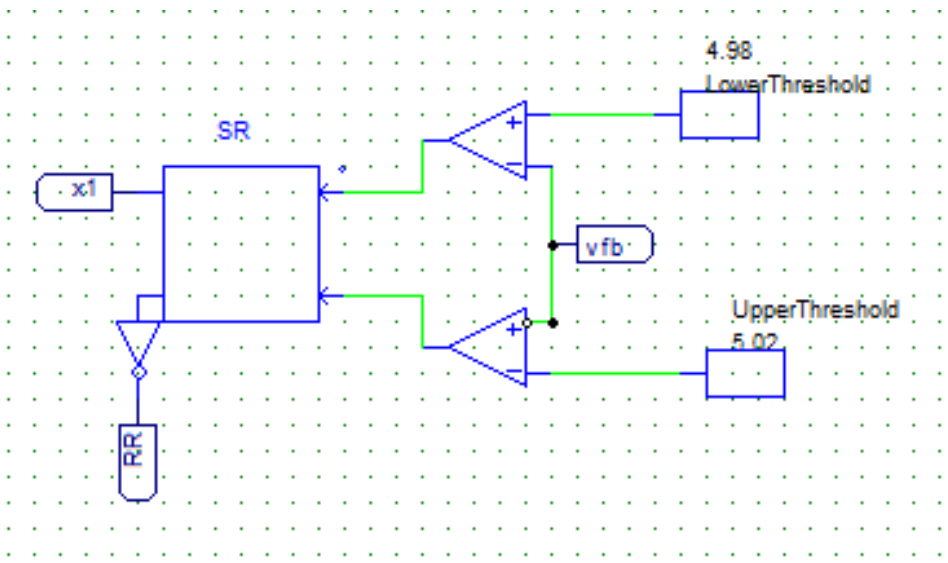

Figure 6.9: Hysteritic Comparator in PSIM

6.2.2 Current Sensing

As mentioned, average current sensing of inductor current is implemented by using the current sense resistor and current sense amplifier MAX9920 of Maxim Integrated. Buck FDPOL with a 25 mΩ current sense resistor is shown in the schematic Figure 6.10.

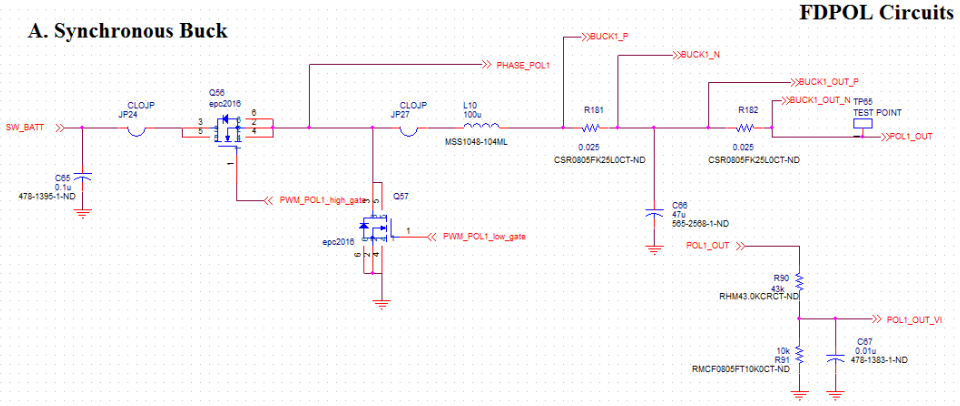

Figure 6.10: Current Sensing Schematic

The differential voltage across the current sense resistor is connected across a current sense amplifier as shown in the Figure 6.11.

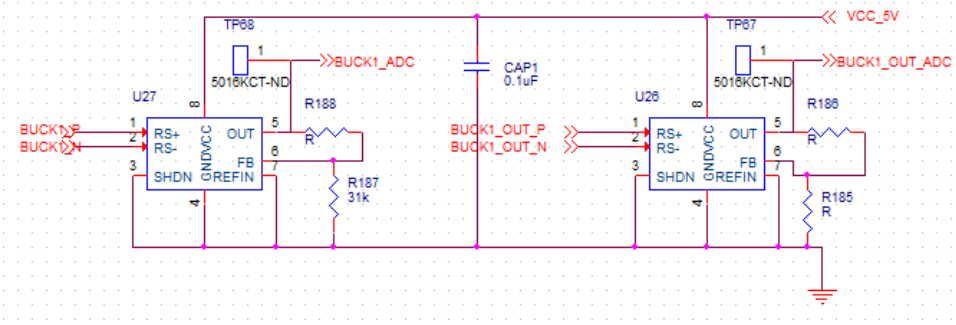

Figure 6.11: Current Sensing Amplifier

6.2.3 Inductor Peak Current Limit and Boundary Condition for PFM-PWM

Inductor Peak Current Limit and the boundary condition for PFM-PWM can be seen in the Figure 6.12. Peak Inductor PFM current limit and the boundary condition for PFM $\Longleftrightarrow$ PWM

are fed to comparators to compare with the inductor current followed by SR Latch to latch the condition. As the boundary condition limit is reached, the SR Latch is reset and the PWM module is driven by the digital compensator's output.

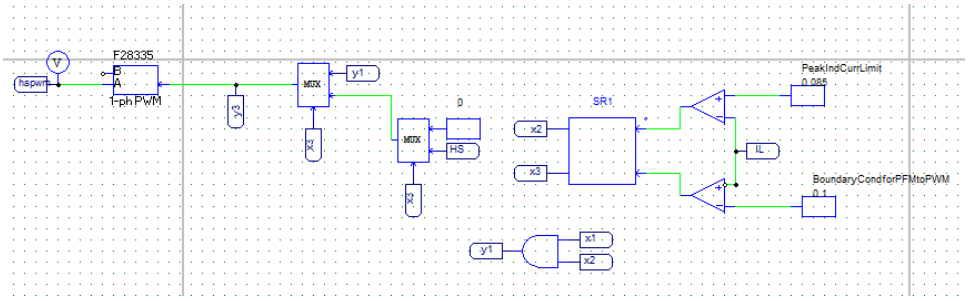

Figure 6.12: Inductor Peak Current for PFM in PSIM

6.2.4 Zero Current Detection

Zero Current Detection block can be seen in the Figure 6.13. As the inductor current reaches zero, the PWM block for LS MOSFET is completely turned OFF to prevent the inductor current from going negative.

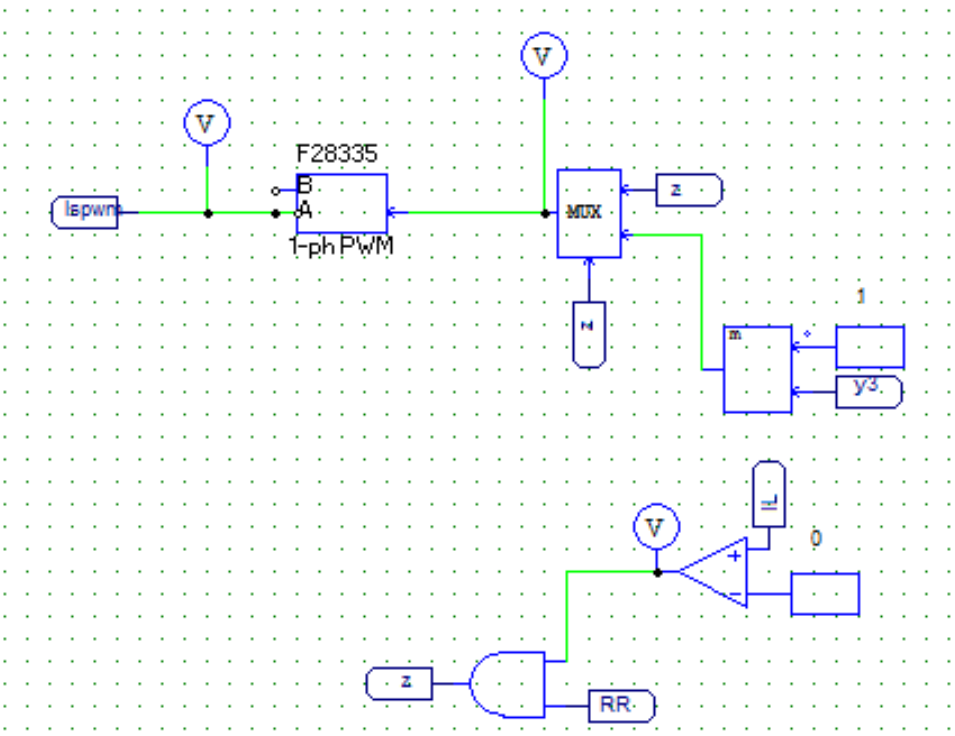

Figure 6.13: Zero Current Detection for PFM in PSIM

6.3 Mathematical Analysis of PFM

As the circuit turns on in PFM mode, the inductor current increases as shown in the Figure 6.14. The current increases for time interval dt1 as mentioned in Eq. 6.3 until it reaches the peak PFM inductor current limit $I_{PEAK\ PFM}$.

$$dt1 = \frac{I_{PEAKPFM} x L}{V_{IN} - V_O} \tag{6.3}$$

where, V_{IN} is the input voltage, V_{OUT} is the output voltage and L is the inductance of the inductor.

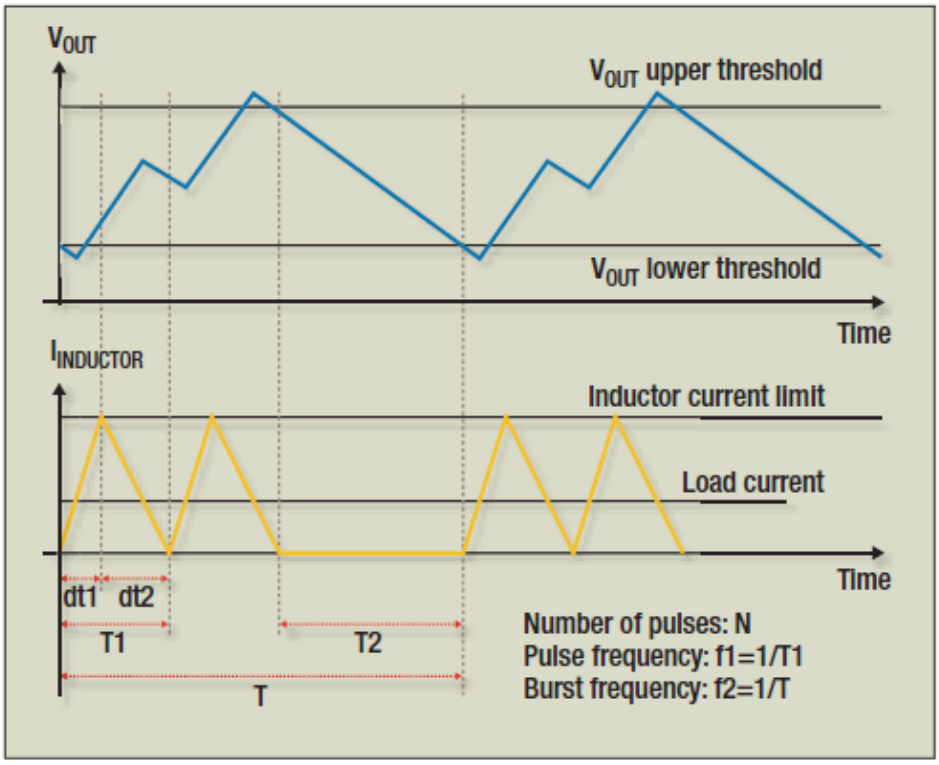

Figure 6.14: PFM mode Characterized by Time Intervals

As the peak PFM inductor current limit is reached, HS FET turns OFF and LS FET turns ON and the inductor current decreases. The inductor current decreases till it reaches zero during interval dt2. This time interval dt2 is given in Eq. 6.4.

$$dt2 = \frac{I_{PEAKPFM} x L}{V_O} \tag{6.4}$$

The pulse frequency is determined as ,

$$f1 = \frac{1}{dt1 + dt2} = \frac{1}{T_1} = \frac{V_{OUT} x (V_{IN} - V_{OUT})}{I_{PEAKPFM} x L x V_{IN}} \tag{6.5}$$

The charge provided by the inductor pulses and the charge supplied by the output capacitor (C_{OUT}) to the load should be equal within a single burst period to maintain a stable dc output voltage across C_{OUT}. The burst frequency, including N pulses and the sleep phase for ripple voltage V_R is determined as Eq. 6.6.

$$f2 = \frac{1}{NxT_1 + T_2} = \frac{1}{T} = \frac{2I_{OUT}(\frac{I_{PEAKPFM}}{2} - I_{OUT})}{I_{PEAKPFM}xC_{OUT}xV_R} \tag{6.6}$$

These time intervals can further be expressed as functions of L and Cout. Consider the time intervals for inductor current and output voltage as shown in Figure 6.15[32].

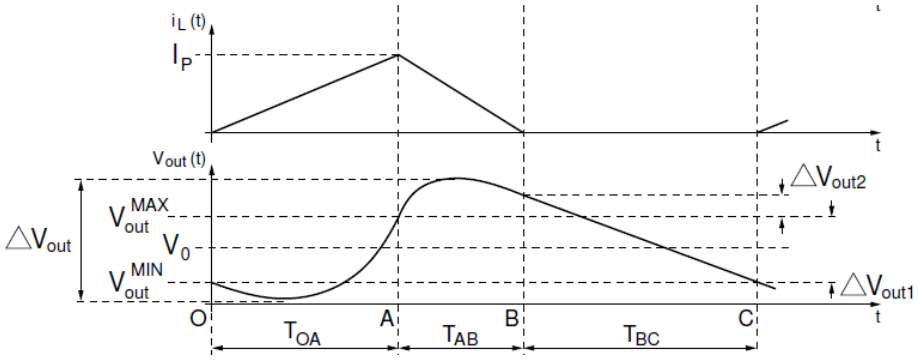

Figure 6.15: PFM mode Characterized by Time Intervals-2

The period can be split into T_{OA}, T_{AB} and T_{BC}. T_{OA} and T_{BC} are considered more in detail. Eq. 6.3 can also be written as Eq. 6.7.

$$L\frac{d_{iL(t)}}{dt} = V_{IN} - V_{OUT} \tag{6.7}$$

The inductor current can also be written as a function of time as mentioned in Eq. 6.8.

$$iL(t) = \frac{I_{PEAKPFM}}{T_{OA}}t \tag{6.8}$$

The equation for peak PFM inductor current limit can be written as 6.9.

$$I_{PEAKPFM} = \frac{V_{IN} - V_{OUT}}{L}T_{OA} \tag{6.9}$$

The current flowing through the capacitor C_{OUT} (C) is given as Eq. 6.10,

$$iC(t) = iL(t) - I_{OUT} \tag{6.10}$$

Capacitor voltage $v_C(t)$can be calculated by integrating the combined Eq. 6.8, Eq. 6.9 and Eq. 6.10.

$$v_C(t) = \frac{I_{PEAKPFM} x t^2}{2xCxT_{OA}} - \frac{I_{OUT} t}{C} + v_C(t0) \tag{6.11}$$

Since $V_R = \triangle V_{OUT} = V_{\text{High Threshold}} - V_{\text{Low Threshold}} = v_C(t_A) - v_C(t_0)$, T_{OA}) can be expressed as Eq. 6.12,

$$T_{OA} = L \frac{I_{OUT} + \sqrt{I_{OUT}^2 + \frac{2CV_R(V_{IN} - VOUT)}{L}}}{V_{IN} - V_{OUT}} \tag{6.12}$$

From Eq. 6.12,$I_{\text{PEAK PFM}}$ can be calculated as Eq. 6.13,

$$I_{PEAKPFM} = I_{OUT} + \sqrt{I_{OUT}^2 + \frac{2CV_R(V_{IN} - VOUT)}{L}} \tag{6.13}$$

During T_{BC}, both the FETs are off and the loading current discharges the output capacitance. Assuming $i_L(t)$ to be constantly zero, $i_C(t) = I_{OUT}$, hence $v_C(t)$ is given as Eq. 7.1.

$$v_C(t) = -(t - t_B)\frac{I_{OUT}}{C} + v_C(t_B) \tag{6.14}$$

The output voltage decreases linearly until it reaches $V_{\text{Low Threshold}}$. From Eq. 7.1, T_{BC} or the sleep phase can be calculated as Eq. 6.15.

$$T_{BC} = C\frac{V_R}{I_{OUT}} \tag{6.15}$$

Thus from Eq. 6.12 and Eq. 6.15, it can be inferred that the pulses and the peak PFM inductor current limit is directly proportional to inductor L and sleep phase is directly proportional to capacitor C.

6.4 Simulation and Results

The main requirement for the PFM to operate is to restrain inductor current from going to negative. This will avoid any additional loss incurred from negative current and hence the efficiency of the converter increases. This can also be verified from the efficiency results without PFM control where the graph start from almost 0 % whereas efficiency curves in PFM control starts from a higher value at light load.

Simulation Results are as follows:

The output voltage ripple and the discretized sampled inductor current in PFM mode at light load in PSIM is seen in the Figure 6.16. The out put voltage ripple with inductor current from the sense amplifier can be seen in the Figure 6.17. As it can be seen from the figure, inductor current is clipped to a non negative value.

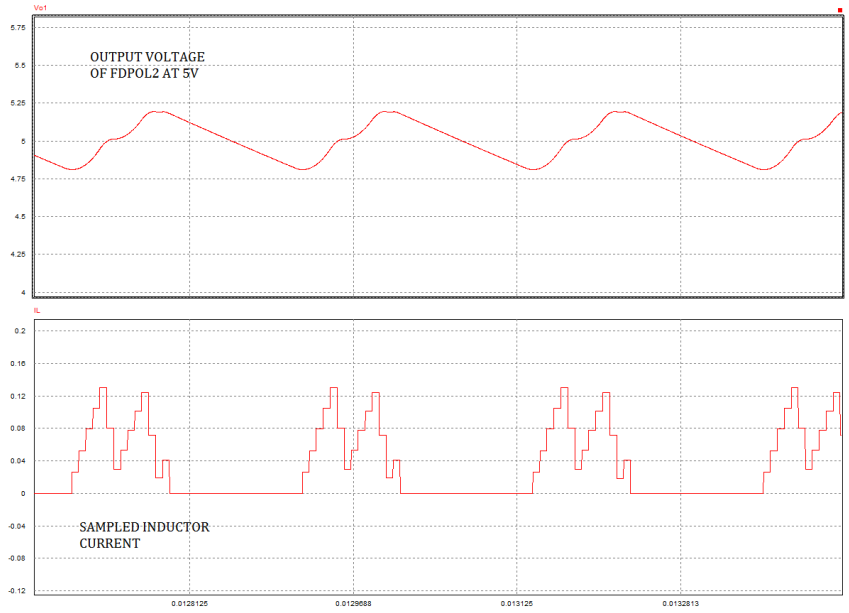

Figure 6.16: Output Voltage and the Sampled Inductor Current in PFM mode in PSIM

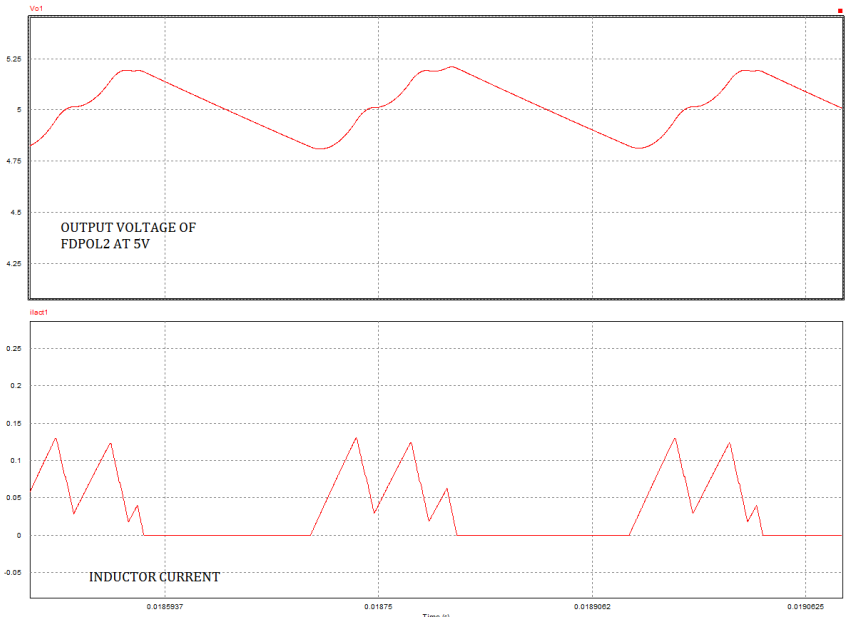

Figure 6.17: Output Voltage and the Inductor Current in PFM mode in PSIM

The specifications of FDPOL2 used for PFM are as follows

Table 6.1: Specifications of FDPOL2 used in PFM

Converter	FDPOL2 Buck Converter
Switching Frequency	600KHz
Output Voltage	5 V
Ripple voltage	40 mV
Peak Inductor PFM Current	90 mA
PFM-PWM Boundary Current Limit	100 mA

6.5 Test Results

In light load condition FDPOL2 is operated and tested. It can be seen in the Figure 6.18 that the inductor current is positive and in accordance to the Figure 6.6. Output voltage ripple is 25 mV.

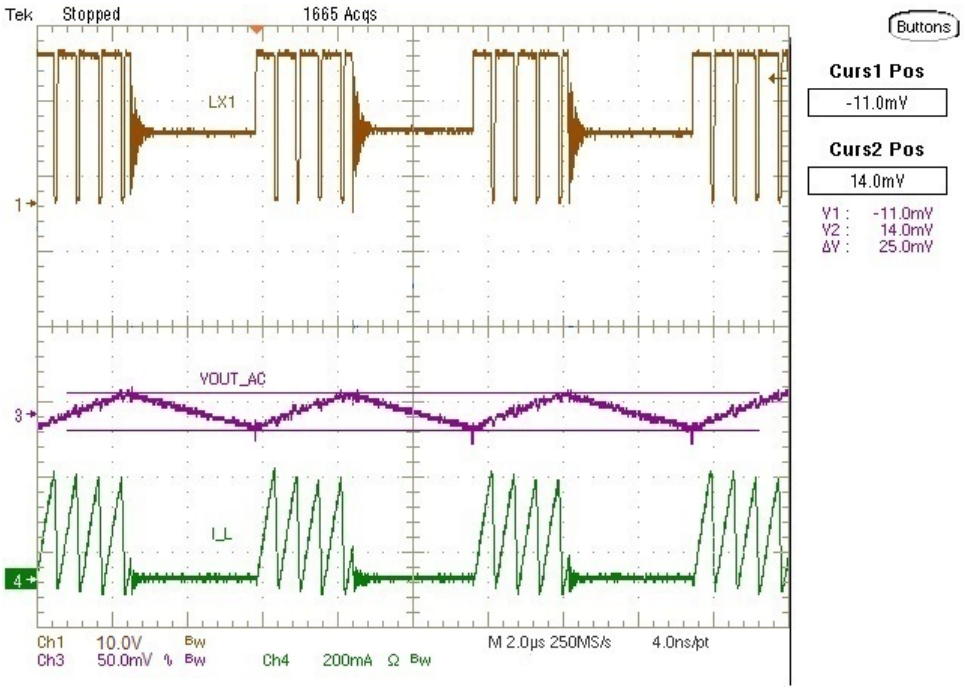

Figure 6.18: Output Voltage and the Inductor Current in PFM mode

As mentioned, number of pulses depends on the inductor value and the duration of sleep phase depends on the value of capacitance. The effect of inductance can be seen in the Figure 6.19. As the inductance decreases, number of inductor current pulses increases for the voltage to reach upper threshold voltage as seen in the Figure 6.20.

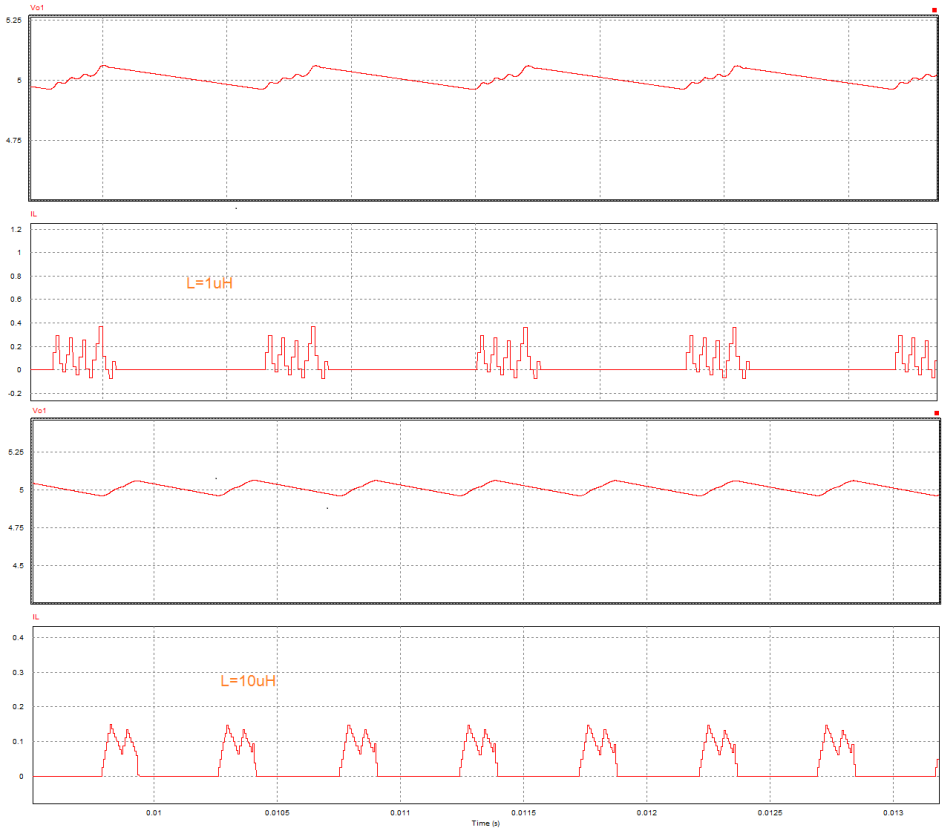

Figure 6.19: Effect of Inductance (Simulation) on number of Pulses in PFM mode

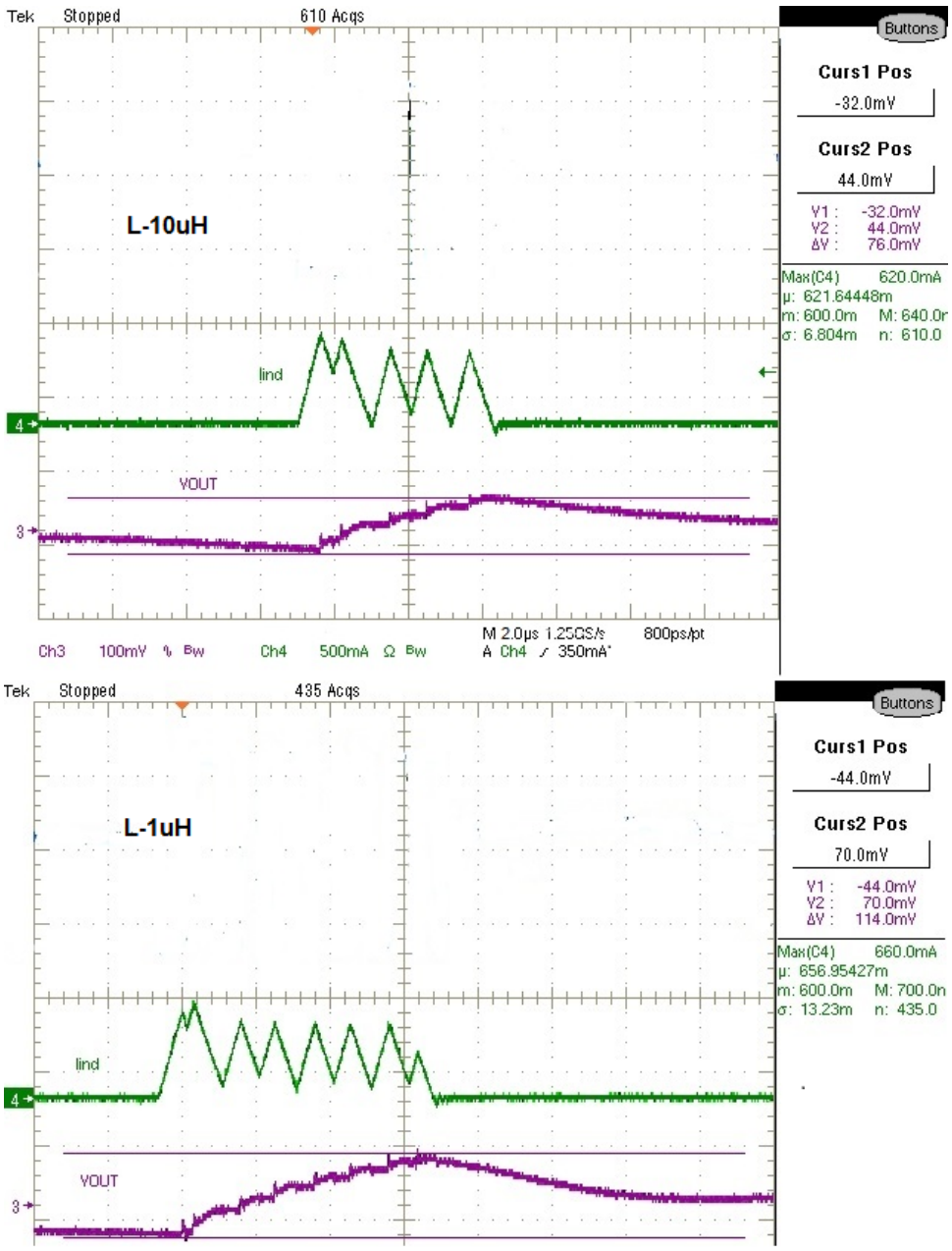

Figure 6.20: Effect of Inductance on number of Pulses in PFM mode

Similarly, the effect of capacitance is seen on the duration of sleep phase. As the capacitance increases, the duration of sleep phase increases and the voltage ripple decreases as seen in the Figure 6.21.

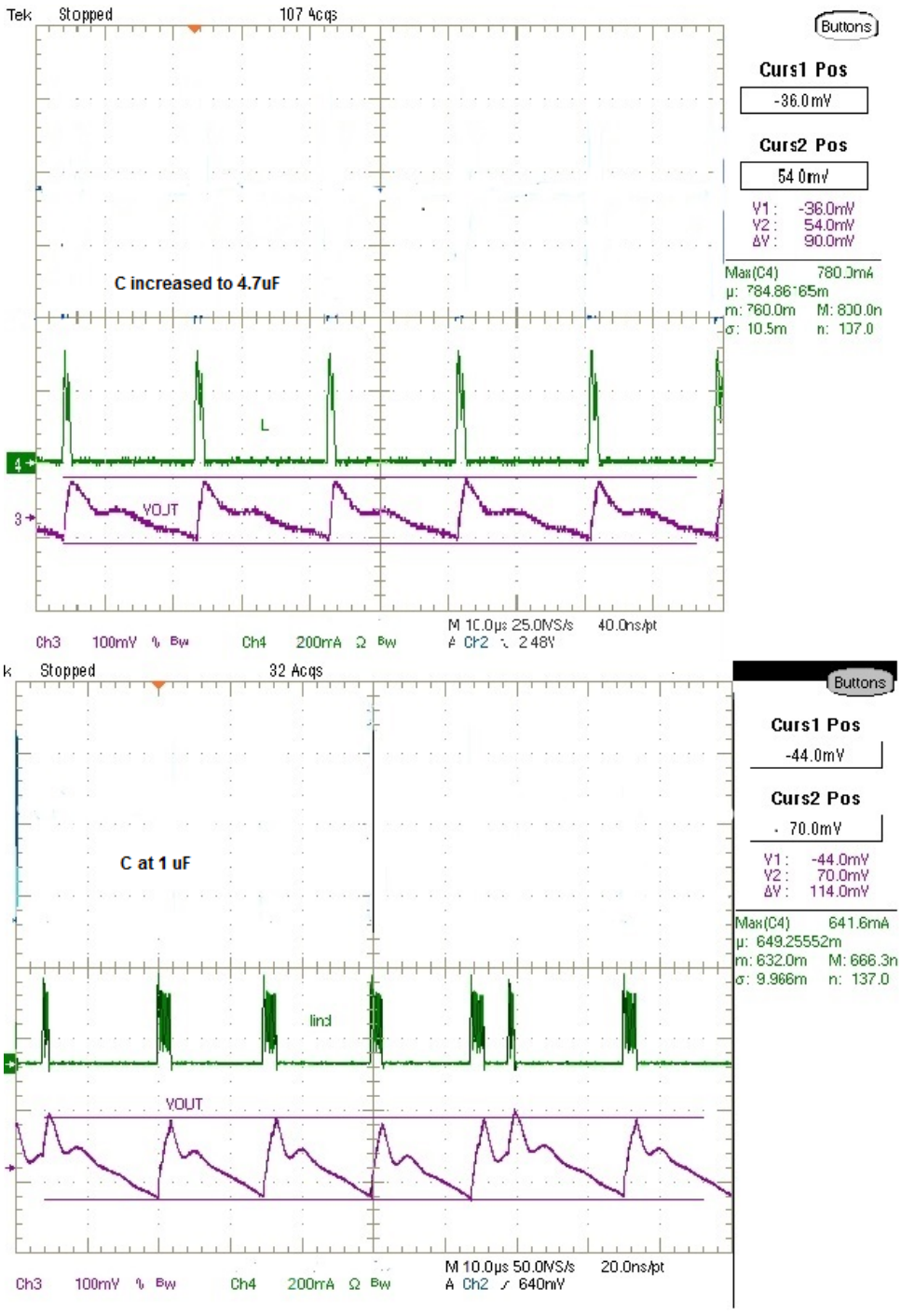

Figure 6.21: Effect of Capacitance on Sleep phase in PFM mode

Efficiency analysis is done on the FDPOL 2 converter for different modes: PWM only and PFM-PWM changeover as seen in the Figure 6.22 and Figure 6.23. It is noticed that the efficiency curve for PFM mode starts from 76 % as compared to 0 % in PWM mode at light load. These combined efficiency results from Silcion and GaN based EPS can be in Figure 6.24.

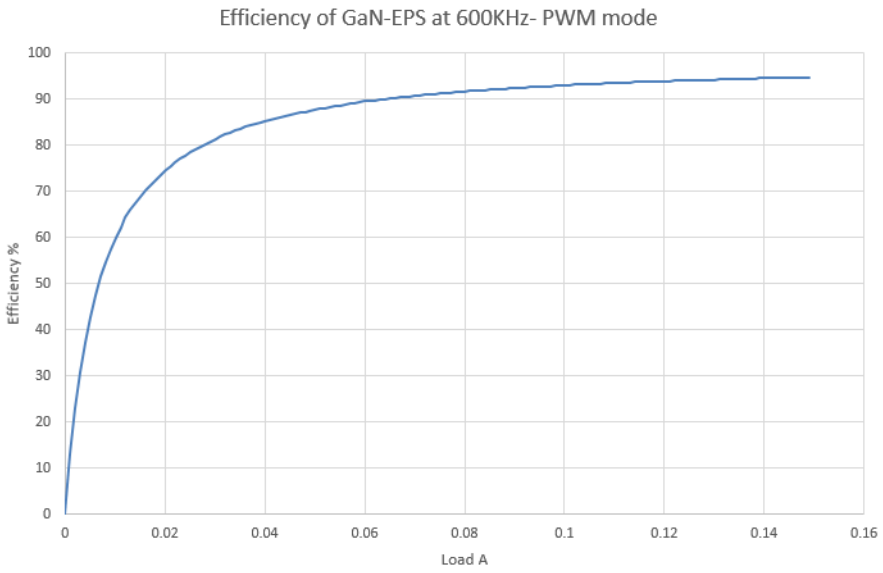

Figure 6.22: Efficiency vs Load in PWM

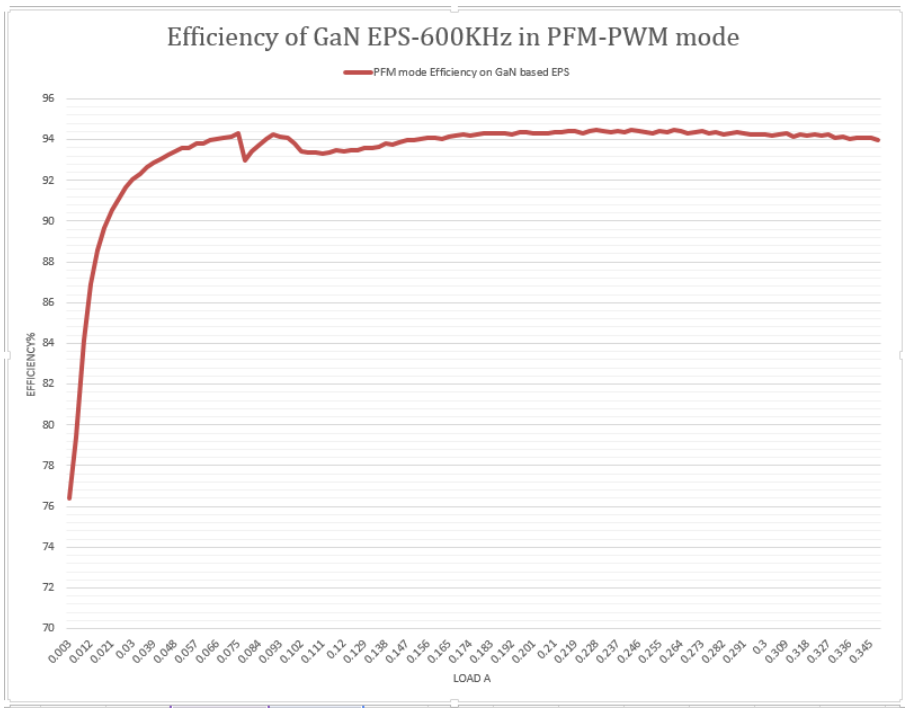

Figure 6.23: Efficiency vs Load in PFM-PWM

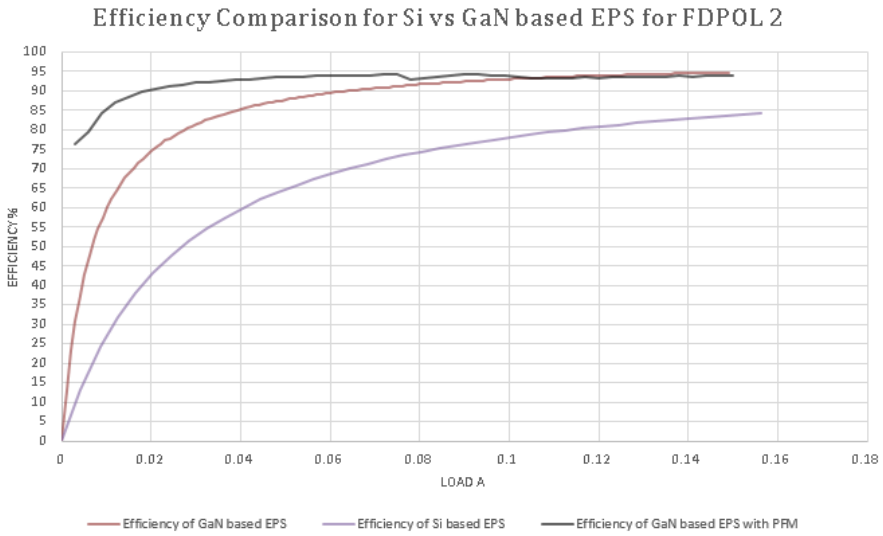

Figure 6.24: Efficiency vs Load in PWM-PFM in Silicon and GaN based EPS

Chapter 7

Active Clamped Flyback using GaN

Flyback converters are dc-dc isolated converters using transformers. Based on the transformers turn ratio and duty cycle, flyback converters can be modeled as buck boost converters. Flyback converters are used in many applications ranging from laptop power supplies to LED lighting systems interfaced with photovoltaic source. The drawback of flyback converter is the relatively high voltage and current stress reflected to its switching device. High RMS current and peak voltage are major issues in a flyback converter and thus requiring an oversized switch to operate it. These high peak voltage and current will reduce the efficiency and increase switching losses. To increase the total efficiency of converter and to reduce voltage stresses across the device, active clamping is implemented to absorb the surge energy stored in the leakage inductance of the transformer. This clamps the turn OFF voltage spike across the devices and helps to achieve ZVS [33].

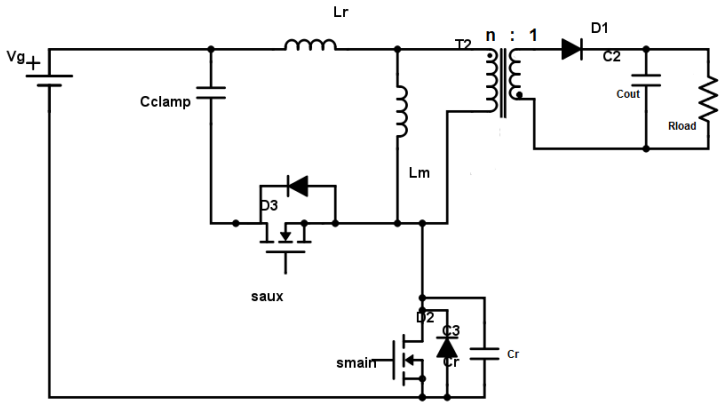

Figure 7.1: Schematic of Active Clamped Flyback Converter

As seen in the Figure 7.1, magnetizing inductance is Lm and leakage inductance is L_r. C_r is the resonating capacitance in parallel to the main switch smain. Capacitance C_r resonates with L_r to enables ZVS for Smain. Following assumptions are made for the working of active clamped flyback converter:

1. L_r (includes the transformer leakage inductance) is much less than the transformer magnetizing inductance, L_m. It is typically 5% to 10% of L_m.
2. The resonant period period generated by the L_r and C_{clamp} is much longer than the maximum off time of smain (T_{off}=(1-D)T_s) as given in the .

$$\pi\sqrt{L_r \times C_{clamp}} >> T_{off} \tag{7.1}$$

3. Sufficient energy is stored in L_r to completely discharge C_r and turn on smain's body diode.

7.1 Operation of Active Clamped Converter

The operation of Active clamped converter is broken down into following stages[34]:

7.1.1 T0-T1

At T0, switch smain is on, and the auxiliary switch, S2, is off. The diode D1 is reversed biased and the magnetizing inductance is linearly charged as shown in Figure 7.2.

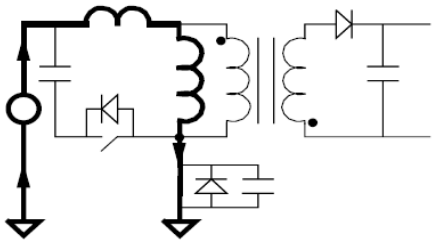

Figure 7.2: Time: T0 to T1

7.1.2 T1-T2

The switch smain is turned off at T1. Resonating capacitor C_r is charged by the magnetizing current through L_r. Charge time is very brief, leading to an approximately linear charging characteristic as shown in Figure 7.3.

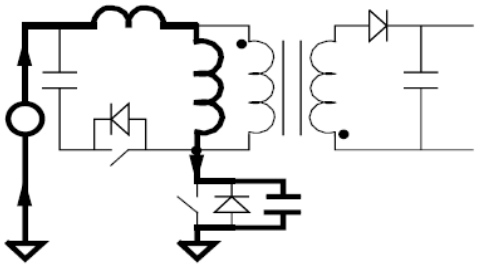

Figure 7.3: Time: T1 to T2

7.1.3 T2-T3

At the onset of T2, capacitor C_r is charged enough to turn on the antiparallel diode D3 across saux. As C_{clamp} is much higher than C_r, magnetizing current flows through C_{clamp} to charge it as shown in Figure 7.4.

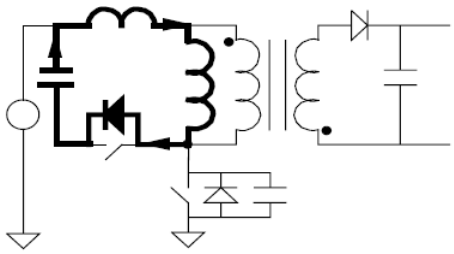

Figure 7.4: Time: T2 to T3

7.1.4 T3-T4

At the onset of T3, voltage across the mangetizing inductance decreases to the point where the diode D1 is forward biased. The primary side of the transformer is clamped to NV_o. During this time, L_r and C_{clamp} begin to resonate. In order for saux to achieve ZVS, the device should be turned on before the current through C_{clamp} reverses direction as shown in Figure 7.5.

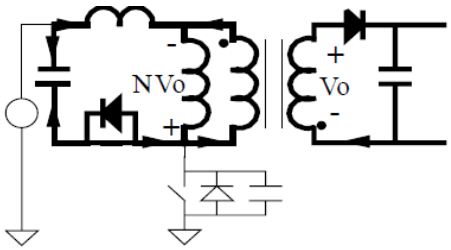

Figure 7.5: Time: T3 to T4

7.1.5 T4-T5

At the onset of T4, saux is switched Off. Now L_r and C_r begin to resonate. The transformer primary voltage remains clamped at NVo as C_r is discharged as shown in Figure 7.6.

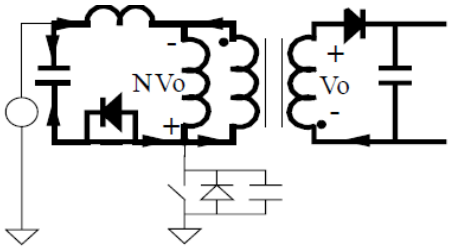

Figure 7.6: Time: T4 to T5

7.1.6 T5-T6

As the energy in L_r is greater than the energy in C_r, at T5, C_r will be discharged to conduct body diode of smain as shown in Figure 7.7. It is during this interval that switch smain can be turned on under zero-voltage conditions.

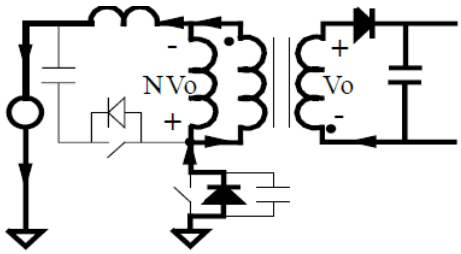

Figure 7.7: Time: T5 to T6

7.1.7 T6-T7

At this instant, smain is ON and secondary current decreases as the resonating inductor current decreases. This reverse biases the diode D1 as shown in Figure 7.8. The magnetizing and resonant inductance begin to charge again, starting another switching cycle.

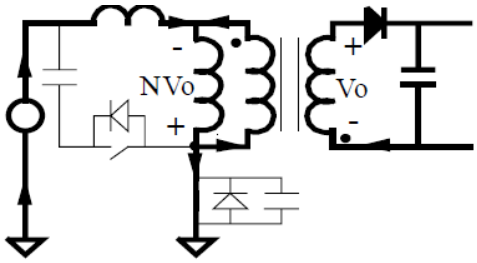

Figure 7.8: Time: T6 to T7

The steady state waveform of active clamped flyback converter is shown in Figure 7.9.

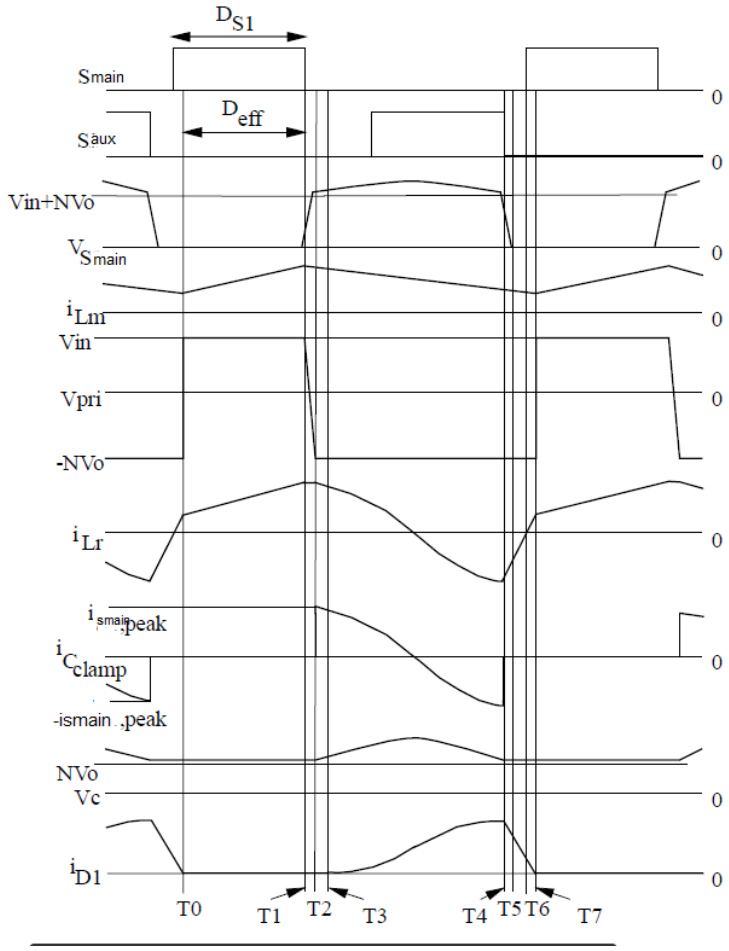

Figure 7.9: Steady State Waveform

Based on the calculation for the active clamping, following is the specifications for the circuit as given in Table 7.1.

Table 7.1: Specifications of Active Clamped Flyback

Parameter	Value
Input Voltage	170 to 210 V DC
Output Voltage	20 V
Load	5 A
Turns ratio	7:1 (45 turns to 6 turns)
Duty Cycle	0.4
Fsw	150kHz
L_m	1 mH
L_r	100μH
C_r	less than 8nF
C_{clamp}	18nF
Core	ETD 59
Device	GS66508P GaN Systems
Gate Driver	CRD001 Cree Gate Driver

For the active clamping, GaN FET GS66508P of GaN Systems was used with the following specifications. The device can be seen in Figure 7.10.

Table 7.2: Device Characteristics: GS66508P

Parameter	Value
Device name	GS66508P
Drain-to-Source Breakdown Voltage	650 V
Drain-to-Source On Resistance	55 mΩ
Gate Threshold Voltage	1.4 V
Drain Current max	30 A
Duty Cycle	0.4

Figure 7.10: GS 66508P

7.2 Setup for Active Clamped Flyback

The active clamped flyback setup was tested at switching frequency of 150kHz using the gate drivers CRD001 by Cree Devices as seen in the Figure 7.11.

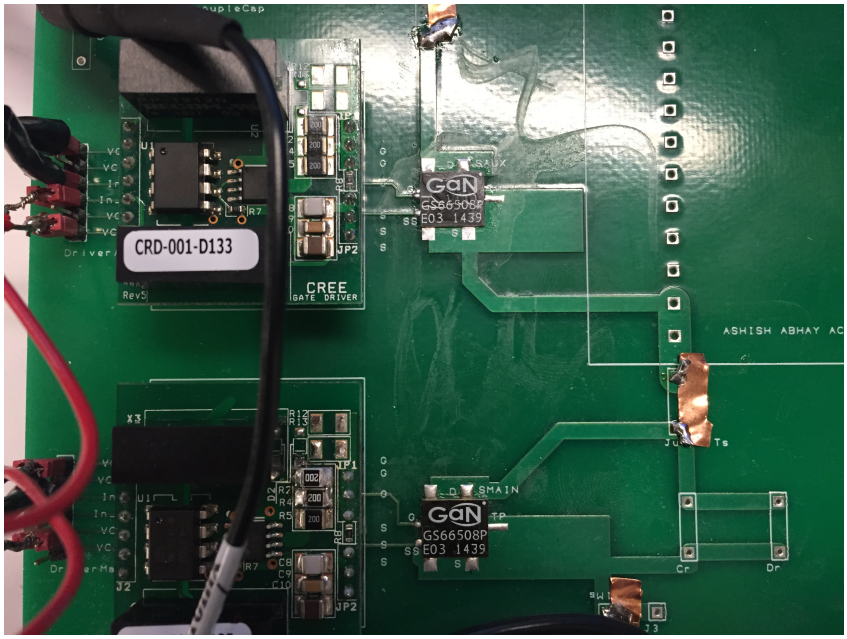

Figure 7.11: PCB for Active Clamped Gate Driver

To ensure thermal protection, heat sink was mounted on the top surface of GS 66508P and was force cooled by fans in the glass cage as seen in Figure 7.12 and Figure 7.13.

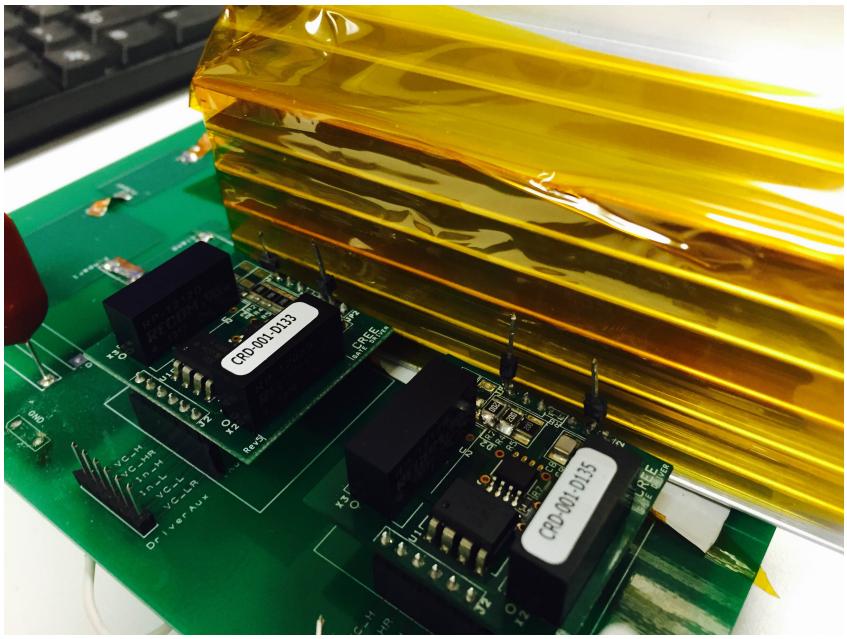

Figure 7.12: Thermal Heat Sink Protection for GS 66508P

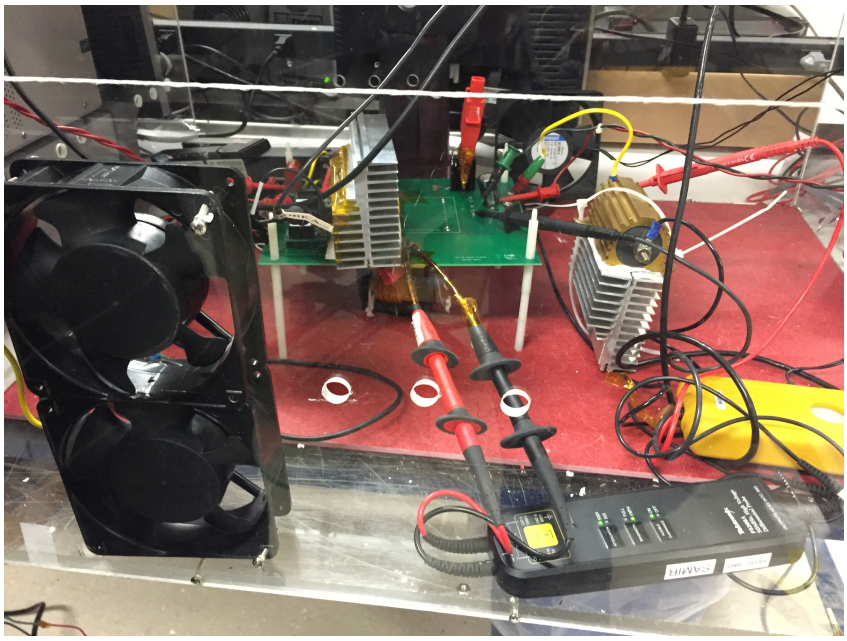

Figure 7.13: Test Setup for Active Clamped Flyback

7.3 Results and Waveforms

7.3.1 Test on Flyback

Initially, the test was conducted in flyback configuration by disabling the active clamping to check the voltage stress level across the smain switch. Since the voltage stress across the smain switch was too high, the input voltage was limited to 100 V, as the VDS max across the switch crossed 400 V as seen in Figure 7.14.

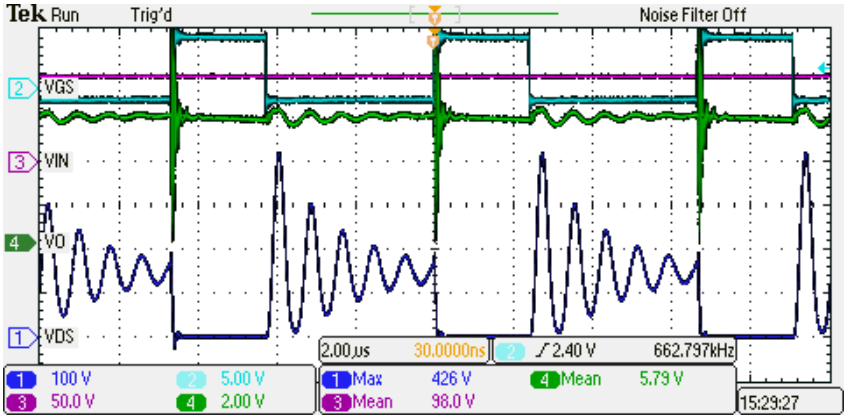

Figure 7.14: Results for Flyback Converter at Vin=100 V

7.3.2 Test on Active Clamped Flyback

As the surge voltage across the device increased tremendously in flyback configuration, active clamping was tested. The input voltage was gradually increased to 180 V with the voltage stress across the smain switch clamped to only 385 V. Results can be seen in the Figure 7.15.

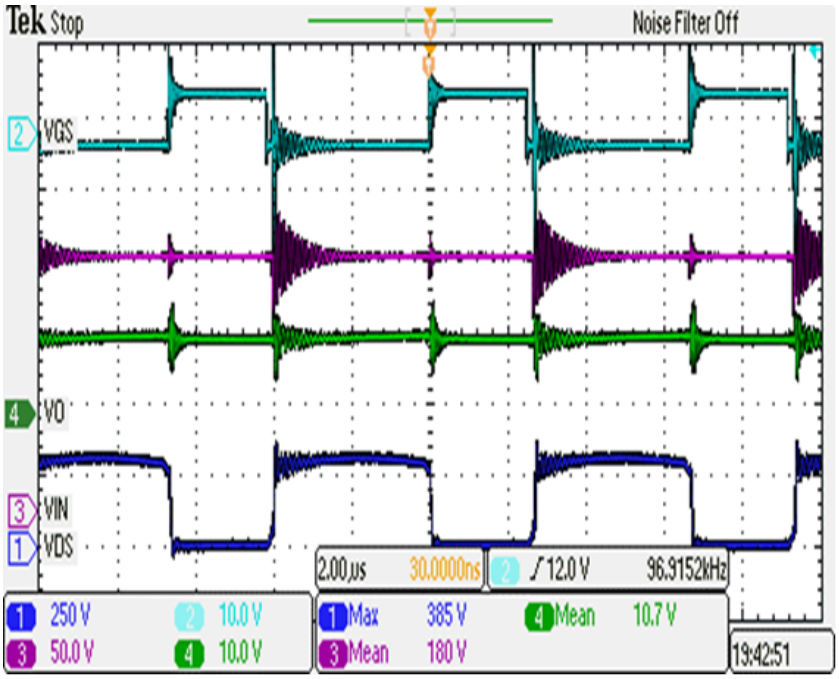

Figure 7.15: Results for Active Clamped Flyback Converter at Vin=180 V

To further test the converter both in flyback and active clamped flyback configuration, the input voltage was varied and the device voltage was measured as it can be seen in Figure 7.16. Thus the voltage stress across the device is reduced drastically.

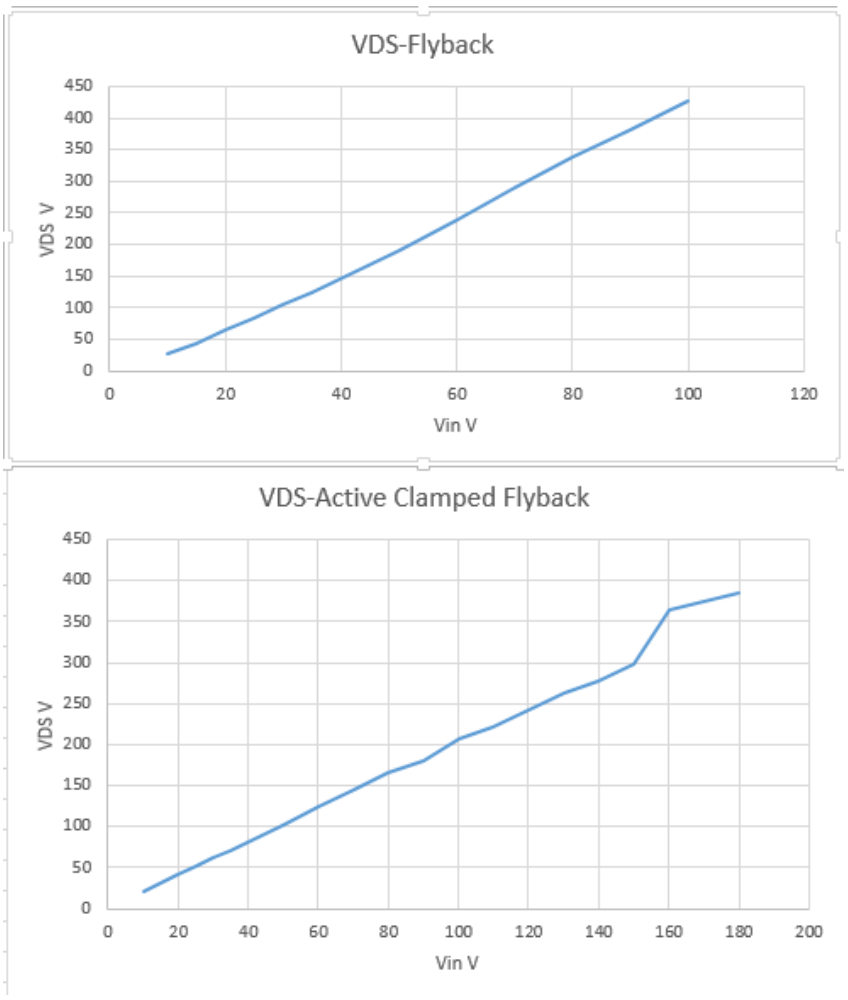

Figure 7.16: Flyback vs Active Clamped Flyback Converter at Different Input Voltage

Chapter 8

Conclusion and Future Work

The develoment of an efficient and configurable electrical power system for CubeSats has imparted a clear understanding of the functioning of high frequency switching DC-DC converters using both silicon and gallium nitride FETs. The CubeSat EPS can be considered as an effective test-bed to understand a wide range of embedded and power electronics applications. The digital control of these converters with different algorithms for battery charging, maximum power point tracking, pwm-pfm control is a very challenging part. The control of multi-phase point of load converters requires regulation at different points. Multiple tasks are handled by the controller and synchronization between these tasks with the duty cycle update at regular sampling intervals is another challenge. The EPS board implements all these features with effective path switching cicuit. The EPS software is modular and additional converters can be added with ease. A digital control scheme for battery charging is implemented which directly regulates output current. A digital (P and O) MPPT controller is designed which ensures that the panels operate at peak efficiency. A battery state machine is implemented which keeps a track of the battery parameters and switches between the constant current and constant voltage charging modes.

High frequency, high efficiency GaN FET based EPS is developed. The EPS should comply with the Rad-Hard space requirements listed below in Table 8.1 [35]. This is to reduce the amount of aluminium shielding required and thus to reduce the weight of the EPS by using the radiation hardened GaN FETs.

Table 8.1: Radiation Categories for Hardware

Category	Total Ionising Dose(kRad)	Single Event(SE) Latch-Up(MeV)	SE Upset(MeV)
Rad hard	100 minimum	Up to 120	Up to 120
Rad Tolerant	100 minimum	Up to 120	Up to 120
Commercial	3 to 20	1 to 120	1 to 120

Use of high frequency GaN devices reduces the size of filter components which reduces the size of printed circuit board. On-resistance R_{DSON} is quite low for GaN as compared to Silicon mosfets which further reduces the conduction loss.

Detailed power loss analysis is done on silicon based EPS. Efficiency profiles are observed at different loads for silicon and GaN FET based EPS. To reduce switching loss, pulse frequency modulation is implemented. This is also known as Light Load Management. As inspected in previous chapters, with PFM, light load efficiency starts from 70 % as compared to 0 % with PWM switching control. PFM is an efficient technique for portable applications when light load is the condition in idle state which extends the battery life.

PFM architectures do offer some advantages for DC/DC conversion, including better low-power conversion efficiency, lower total solution cost, and simple converter topologies that do not require control-loop-compensation networks, but are less popular than PWM devices due to some notable drawbacks. The first is the control of EMI. Filtering circuits for a fixed-frequency switching converter are much easier to design than those for a device that operates across a wide range of frequencies. Second, PFM architectures tend to lead to greater voltage ripple at the output that can cause problems for the sensitive silicon being supplied. Third, PFM operation at low (or even zero) frequency increases the transient response time of the switching converter that could lead to slow response and consumer disappointment in some portable applications. However, by combining the merits of a PWM architecture with those of a PFM device in a dual-mode switching converter, manufacturers can offer a solution with high efficiency across its entire operating range. The EMI concerns associated with PFM are mitigated to a great extent because the root cause of such interference is fast switching at high currents and high voltages, whereas in dual-mode converters, variable-frequency operation is only used during low-current and low-voltage operation.

For GaN FET based EPS, EPC 2016 device was analysed and compared with silicon mosfet. In future, different GaN devices can be used to further reduce the power loss and achieve higher efficiency. Power loss analysis of GaN based EPS can be done in future to quantify the efficiency results in detail. DSP control loop time needs to be optimized for PFM control. DSP clock ticks were measured for PWM control but for PFM algorithm this issue can be addressed to optimize the loop time. The present implementation of the EPS has one FBCM and two FDPOL modules. These will be increased to provide additional voltage domains and interface to more solar panels. The next step towards improving system performance would be to further study control loop performance over a wide range of sampling frequencies and loads and carry out power and loss calculations. The battery charging system will be improved by implementing charge detection algorithms to know the state of charge of batteries.

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