ABSTRACT

NARWAL, AJIT SINGH. Control and Dynamics of Modular Multilevel Converters (Under the direction of Prof. Subhashish Bhattacharya).

Modular Multilevel Converters have found potential in areas of MVDC and HVDC applications for several reasons such as scalability, reduced voltage stresses, modularity amongst others.

This work spans the design, development, analysis, and testing of MMC based VSCs on different platforms. The focus is on module voltage balancing algorithms, steady state performance such as active and reactive power control, and fault behavior in a back-to-back MMC system. Both half-bridge and full-bridge topologies were employed in the following work.

The MMC system was modeled on platforms such as MATLAB, PSCAD/EMTDC, RTDS, and Xilinx FPGA as part of HIL test-bed.

Control and Dynamics of Modular Multilevel Converters

by
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DEDICATION

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BIOGRAPHY

Ajit Narwal was born in Haryana, India, on August the 4th in 1986. He completed his Bachelor's degree in Electrical Engineering from Delhi College of Engineering, University of Delhi. Following his undergrad degree he worked at National Thermal Power Corp's Engineering Office in Delhi as an Executive Engineer for a few years before joining North Carolina State University in 2011, where he worked as a Research Assistant at FREEDM labs on topics of power electronics under the guidance of Prof. Subhashish Bhattacharya.

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I wish to express my gratitude to my adviser, family, and to my fellow researchers for their patience and unending support making this research possible.

I would also like to thank all my friends, without whom I would have graduated a year earlier.

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Chapter 1: Motivation

Modular converters have become a focus of research recently after finding applications in HVDC and MVDC technology. Their applicability has also penetrated the domain of MV drives and power amplifiers rendering their design, study and analysis an exciting field of study in the area of power electronics research.

The motivation behind this work was to explore the behavior of modular converter topologies in steady-state and dynamic conditions for applicability in practical systems.

Chapter 2: Present HVDC Technologies

2.1 Introduction

Line-commutated converter (LCC) technology based HVDC systems is a mature technology and has been around since 1954. These have been historically used for interconnection of asynchronous ac ties and for bulk power transmission over long distance from power plants to load centers. The converter switch used here is the thyristor. These can be triggered into conduction by a gating signal; however, the turn-off is dependent on naturally occurring current zero state. Thyristors, power electronics and the use of conventional equipment have lent a high degree of reliability to such systems resulting in a robust technology with low losses (Figure 1).

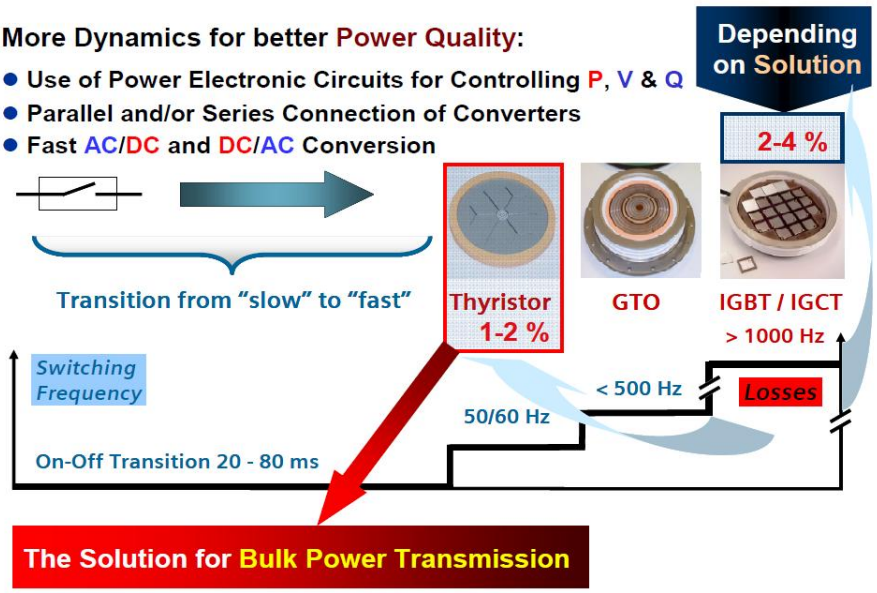

Figure 1. Power electronics for HVDC and FACTS- Transient performance and losses [1].

Further advances in semiconductor technology has paved way for fully-controlled semiconductor devices (Table 1) which find applications in high-voltage, high-power converters. These can be employed in various voltage-source converters (VSC) schemes for HVDC applications switching at higher frequencies than line frequency. Switching at higher frequencies, typically through SPWM (Sinusoidal PWM) has direct bearing on the harmonic content of the currents and voltages. However, higher PWM frequencies are limited by the losses in the devices, along with the heat sink design. Both these factors are related to power being handled by the component. Switching losses, directly related to higher frequency gating operation, are one of the major factors in a VSC application [2].

Table 1. Fully-controlled power semiconductor devices

Acronym	**Type**	**Full Name**
IGBT	Transistor	Insulated Gate Bipolar Transistor
IEGT	Transistor	Injection Enhanced Gate Transistor
GTO	Thyristor	Gate Turn-off Thyristor
IGCT	Thyristor	Integrated Gate Commutated Thyristor
GCT	Thyristor	Gate Commutated Turn-off Thyristor

2.2 LCC versus VSC HVDC Systems

The employment of VSC technology in HVDC applications has some key advantages over LCC based HVDC systems. These are summarized as follows [3]:

a) Commutation failure due to grid fault or ac voltage dips are eliminated.

b) The VSC can be operated at a small short-circuit ratio (weak system), including networks lacking generation and can even energize a passive or dead grid (black start capability) [4], [5], [6].

c) LCCs normally have a minimum active power output 5% below rated power for the converter to remain in CCM and enable current commutation of valves; VSCs, however, transmission has no minimum dc current limits [7]. This makes VSCs favorable for power transmission with varying power [8]. For e.g., wind farms.

d) Both active and reactive power at each terminal can be controlled independently within the rating of the equipment [9]. Because the converter active and reactive powers can be set to positive or negative values, the converter is said to operate in all four quadrants on the PQ plane [10].

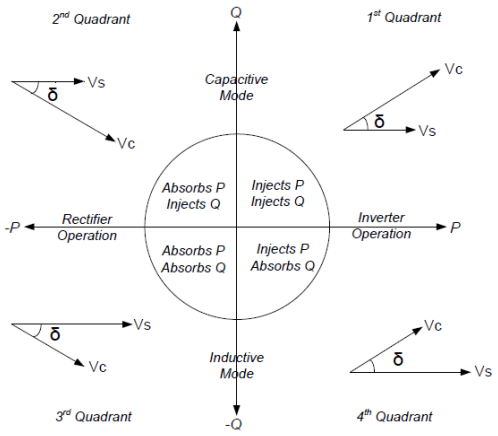

Figure 2. P-Q diagram of a VSC [11]

Figure 2 explains the operation of a VSC in all four quadrants of the PQ map. In the first quadrant both the active and reactive power are positive which means that the converter injects both powers to AC system which shows the capacitive mode of inverter operation. The converter output AC voltage magnitude is higher than AC bus voltage and leads AC bus voltage by an angle δ.

In the second quadrant, the active power is negative and the reactive power is positive which explains the capacitive mode of rectifier operation. In this case, the converter output AC voltage amplitude is higher than AC bus voltage but it lags the AC bus voltage by an angle δ.

Both the powers in the third quadrant are negative which means converter absorbs both powers from the AC system which explains the inductive mode of rectifier operation. In this case, the AC bus voltage magnitude is higher than the converter output AC voltage and it leads by an angle δ.

In the fourth quadrant, the active power is positive and the reactive power is negative which explains the inductive mode of inverter operation. Here the converter output AC voltage leads the AC bus voltage but its magnitude is less than the AC bus voltage.

According to the converter MVA capacity and system requirements, converter can operate in any mode (i.e. capacitive or inductive) of rectifier or inverter operation [11].

e) Voltage polarity on the dc side is always the same and power is reversed. This allows VSCs to be suited for DC grid designs [5]. The constant voltage polarity further allows a more economic cable design. Cross-linked polyethylene cables are less

costly, lighter, and smaller in diameter than traditional mass impregnated cables and hence preferable [12].

f) VSC stations can be designed to eliminate flicker and selected harmonics in the ac grid [13].

However, VSCs do have some shortcomings in comparison to LCC based HVDC systems:

a) In LCC systems DC line-line faults can be cleared at the converter by eliminating firing pulses to the thyristor gates which, henceforth, will block the voltages. However, in VSCs the freewheeling diodes are capable of conduction even if the switch gates are off. The faults, therefore, have to be suppressed by opening the AC breaker feeding the converter [14]. Hence the absence of a reliable DC breaker capable of isolating DC faults restricts the application of VSC HVDC.
b) Power losses are considerably higher, typically 1.7% per converter [15].
c) Relatively newer technology; and
d) Voltage limits due to power device limitations. In order to limit the voltage across each semiconductor, series connected IGBTs must be switched absolutely simultaneously. This requires sophisticated gate drive circuits to enforce voltage sharing under all conditions [14].

Summarily, VSC transmission can be used in applications for which LCC HVDC systems are used. The above points lead to a high degree of utility of the VSC HVDC in cases such as:

a) Interconnection to a small isolated network: [3]

Communities in remote areas, or on small islands, may rely on diesel generation for their electricity supply. The cost of provision of electrical energy in such locations may be very high, because advantage cannot be taken of the benefits of large-scale generation available in the main networks.

Additionally, generation of the energy using small diesel generators is more damaging to the environment, than when using large-scale generation in a major network, with its more efficient generators and operating modes. Therefore, transmission of energy from the main network may be economically and environmentally attractive.

VSC Transmission may offer a good solution to such power transmission if overhead line or submarine ac transmission is not feasible, e.g. if the distance is large, or if an underground cable solution is considered advantageous.

VSC Transmission is advantageous compared to a LCC HVDC solution for the supply of power to an isolated/passive network, because synchronous compensators are not necessary for the operation of the VSC [4], [7]. Additionally, whilst the power loss of a VSC Transmission scheme can be 2 or 3 times higher than that of a LCC HVDC scheme, the difference would be reduced in this application by the relatively large power loss associated with the operation of a synchronous compensator, which would be necessary, when using LCC HVDC [15].

b) Interconnection between weak power systems

For weak ac network applications the control of the ac network voltage is particularly important. When a LCC HVDC scheme is used, the large ac harmonic filters and shunt capacitors used to provide reactive power compensation actually reduce the ac voltage stability of the system, since the reactive power support reduces as the ac voltage reduces. Therefore, the application of LCC HVDC schemes is typically limited to systems where the short circuit power at the point of connection of the LCC HVDC terminal is at least three times the rating of the scheme. Special control methods can be used when operating at lower short circuit level, but these typically require a higher rating of the converter station equipment. Alternatively, additional reactive power support, in the form of SVCs or STATCOMs, can be applied at the point of connection, to improve the ac voltage stability [4], [7].

As a VSC Transmission scheme is capable of controlling the reactive power at its ac terminals independently of the real power flow between terminals (subject to overall rating limitations), it provides a good solution for the interconnection of networks, where the ac network at one or both terminals is weak [4], [5], [9], [10].

c) Reinforcement of weak AC tie-lines for stability improvement

When an ac transmission line is embedded in a geographically large ac network with major load and generation centers at its extremities, a fault within either of the centers can cause major power oscillations on the ac tie line. If the tie line is weak (e.g. because of its length or

because of its rating relative to the network), then the power oscillations may exceed the over-current setting of the line protection, resulting in a trip of the line. The power oscillations may also have a significant impact on the ac voltage along the line and at the termination points.

The power oscillations can be damped by the insertion of controlled series compensation, or, less effectively, by the use of controlled shunt reactive power compensation. A more effective solution would be the installation of a parallel VSC Transmission scheme. Studies have shown that a VSC Transmission scheme can increase the stability limit on a weak ac tie line by more than the rating of the VSC Transmission scheme, by suitable modulation of the real power transfer of the VSC Transmission scheme and the reactive power at its terminals.

d) Connection of distant loads (off-shore oil and gas platforms)

As an oil or gas reservoir is emptied, the power required to extract and transport the oil or gas increases. Where the production platform is located off shore, and at significant distance from the coast, the electrical power required for the operation has typically been produced by diesel or gas turbine generators located on the production platform. However, as the power requirement increases, additional generating plant becomes necessary and consideration may be given to obtaining the electrical power from the on-shore ac network. The advantages of obtaining the power from the shore include:

- Manpower intensive generation plant on the platform can be removed.

- CO_2 emissions are reduced since the efficiency of an on-shore generation plant is higher, which may also include renewable generation plant.

When the distance to the shore is large, transmission by means of ac may not be feasible, and HVDC transmission may be considered. The use of VSC Transmission provides the following advantages:

- The VSC Transmission equipment is compact, making the installation on existing platforms feasible.
- There is no need for synchronous compensators since the VSC Transmission scheme is self-commutating, and controlled reactive power can be provided, independently of the active power being transmitted.
- The VSC Transmission scheme can provide variable frequency power supply to the offshore motors, acting as a variable speed motor drive.

e) Connecting of remote wind-parks

Wind generation is currently one of the most economical sources of renewable generation, and is the fastest growing sector of electrical power generation. As more and more wind generators are installed there is a tendency for the wind farms to be located further away from population centers, partly because of better wind conditions and partly to reduce the visibility of and audible noise from the wind turbines. Wind conditions are often best in offshore locations and many new offshore wind farms with ratings of 500MW and more are under consideration in several countries.

Whilst a HVDC terminal occupies more space and costs significantly more than an equivalently rated ac substation, HVDC Transmission provides the following advantages:

- The transmission distance can be much larger, enabling connection at a more suitable point in the ac network.
- The HVDC scheme will provide de-coupling between the main ac network and the wind farm network, improving the ride through capability of the wind farm during faults in the mainland ac network.
- The frequency of the offshore network can be allowed to vary with the speed of the wind, increasing the efficiency of the wind farm.

Despite several advantages offered by the conventional 2-level voltage source converter, further improvements are introduced in employing the MMC (Modular Multilevel Converter) topology.

2.3 MMC HVDC Systems

The following are some distinct advantages offered by multilevel converters:

a) Modular realization. This lends the advantage of scalability to different power and voltage levels with achievement of dynamic voltage sharing of power devices.
b) Waveform quality. The waveform is expandable to any number of voltage steps. These converters generate low THD output voltages (and draw input currents with

low distortion) with reduced *dv/dt* stresses. Therefore, electromagnetic compatibility (EMC) problems are reduced [16].

c) System redundancy. The technology uses approved semiconductor devices which increases system availability with redundant modules. Ultimately the investment and life cycle cost of the system is reduced because of use of standard components.

d) Generation of small common-mode (CM) voltages. This reduces stress in motor bearings running on MMC drives. Additionally, CM voltage can be eliminated by using advanced modulation strategies such as proposed in [17].

e) Switching frequency. MMCs can operate at both fundamental switching frequency and high switching frequency PWM. It should be noted that lower switching frequency usually means lower switching loss and higher efficiency [18].

The employment of several switches in multilevel converters renders an obvious disadvantage to the circuit, i.e. greater power semiconductor switches. Even though a lower rated switch can be used but it would require a complex gate drive circuit and additional control for each module in the converter. This makes the overall terminal expensive and complex.

Chapter 3: Concept and Control of Modular Multilevel Converter

A reduction in the size of voltage steps and also the related voltage gradients can be reduced or minimized if the AC voltage produced by the converter is selected in smaller increments in comparison with a two or a three level converter. As discussed above the harmonic content and the high-frequency noise go down with the increment of the number of discrete voltage steps. It also allows for the converter to operate at a lower switching frequency.

Four main topologies are known for multilevel converters [19]:

a) Diode-clamped type (NPC and up with DC-link capacitors [20]-[22] (Figure 3).
b) Capacitor-clamped type (with flying capacitors and DC-link capacitors [23], [24] (Figure 4).
c) Cascade H-bridge type (with separate DC-sources, without common DC-link [25], [26] (Figure 5).
d) Modular multilevel converter type (without DC-link capacitors). This type enables direct and fast control of the DC-link voltage via the switching states of the sub-modules [27]-[32] (Figure 6).

In this work the focus is on the modular multilevel type with a back-to-back system of converters being implemented using this topology. Additionally, a modified cascaded H-bridge type converter topology was also explored and a back-to-back system was also implemented using that topology.

3.1 Structure of Modular Multilevel Converters

Modular Multilevel Converters (or M^2LC) are also called half bridge modular converters. The structural basis of the half-bridge voltage source converters is a single sub-module (or cell) (Figure 7) which is two semiconductor devices (IGBTs in this work) connected in series with

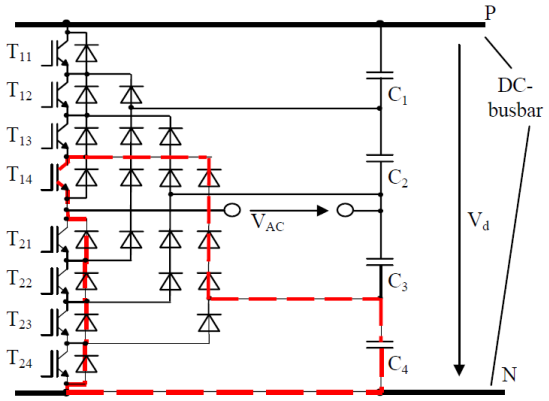

Figure 3. Diode-clamped converter (5-level) [19]

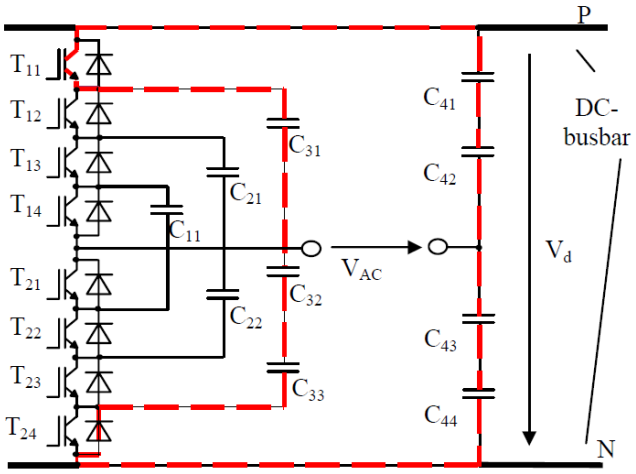

Figure 4. Capacitor-clamped converter (5-level) [19]

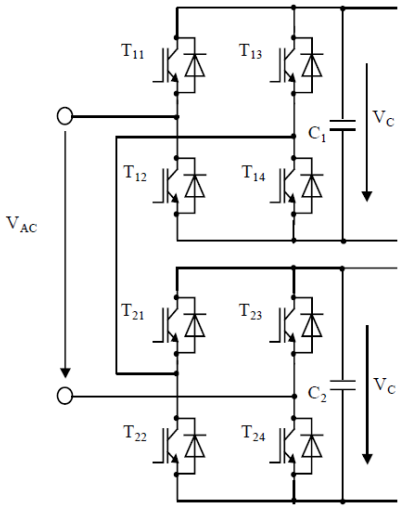

Figure 5. Cascaded H-bridge converter (5-level) [19]

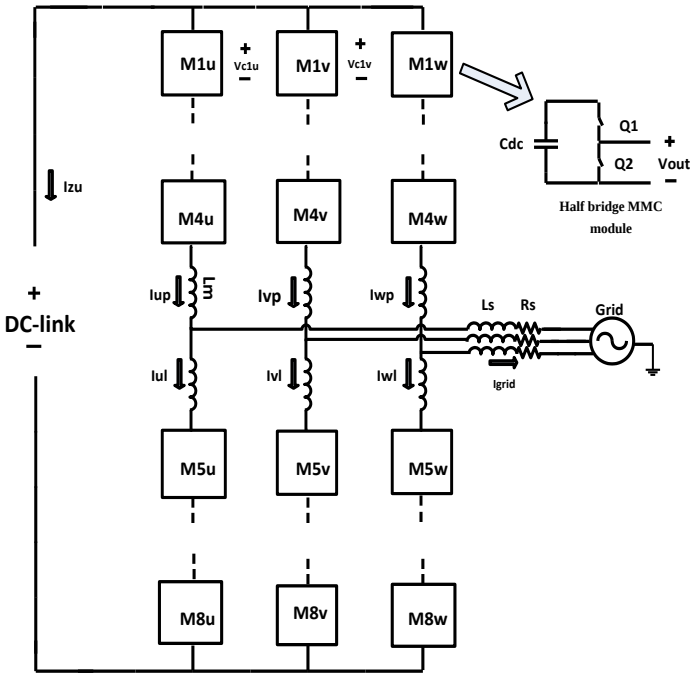

Figure 6. Modular multilevel converter (5-level) [16]

a dc capacitor in parallel with them. Switching 1, upper IGBT in Figure 7, results in V_{out} being assigned the voltage across the dc capacitor; alternatively switching 2, lower IGBT, bypasses the capacitor. This operation is used to switch modules to create a stair-case waveform at the output of the string made from series connection of the sub-modules (Figure 6) [16]. The number of levels of output voltage depends in the number of sub-modules in the string; $m = n + 1$ with n being the number of sub-modules per phase in the converter. Each phase is divided into two arms, upper and lower, each containing $n/2$ sub-modules with both arms connected by a decoupling inductor.

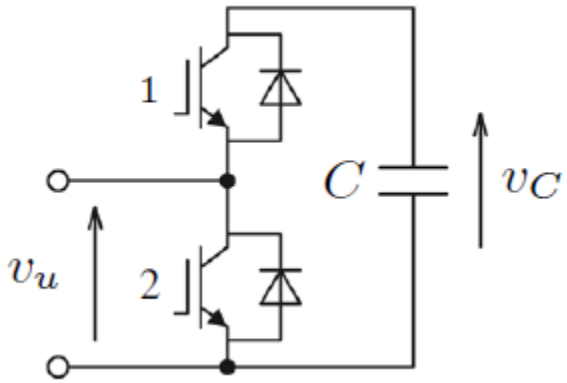

Figure 7. A single sub-module of the MMC structure

The basic idea and the MMC design with the output waveform generated by the converter can be better visualized through Figure 8.

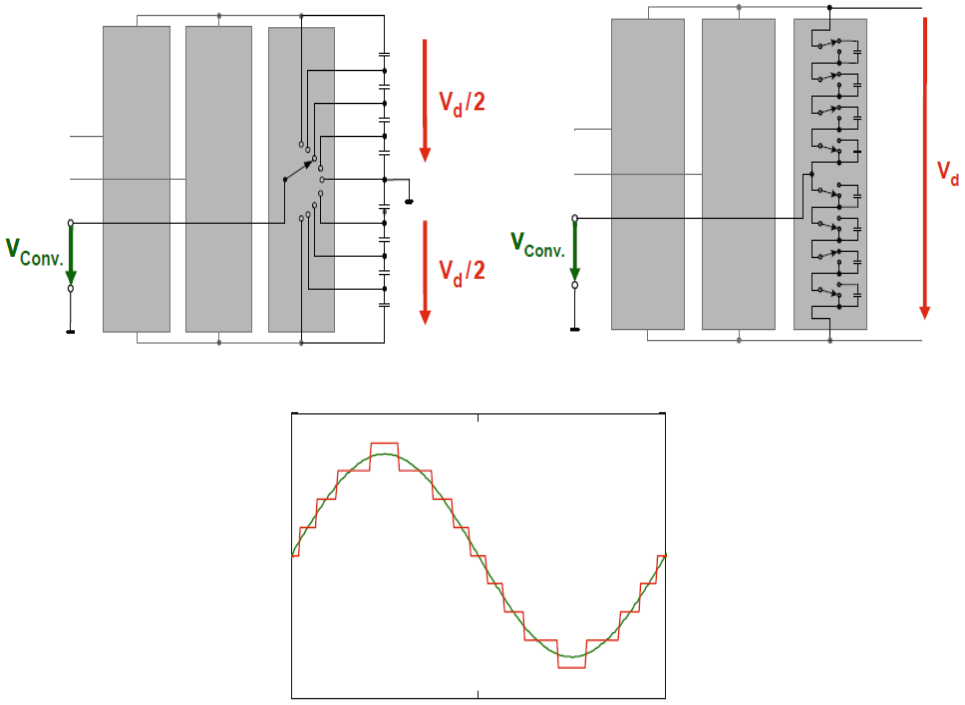

Figure 8. The basic idea of the MMC approach; the implementation; and the resulting output waveform [33]

Three different states are relevant for the proper operation of the sub-module, illustrated in Figure 9 [33].

a) Energization. Both IGBTs are switched OFF:

   This can be compared with the blocked condition of a two-level converter. Upon charging, i.e. after closing the AC power switch, all sub-modules of the converter are in this condition. Moreover, in the event of a serious failure all sub-modules of the converter are put in this state. During normal operation, this condition does not occur. If the current flows from the positive DC pole in the direction of the AC terminal

during this state, it charges the capacitor. When it flows in the opposite direction, the freewheeling diode D2 bypasses the capacitor.

b) Capacitor ON. IGBT 1 is switched ON, IGBT 2 is switched OFF:

Irrespective of the current flow direction, the voltage of the storage capacitor is applied to the terminals of the sub-module. Depending on the direction of flow, the current either flows through D1 and charges the capacitor, or through IGBT1 and thereby discharges the capacitor.

c) Capacitor OFF. IGBT 1 is switched OFF, IGBT 2 is switched ON:

In this case, the current either flows through IGBT2 or D2 depending on its direction which ensures that zero voltage is applied to the terminals of the sub-module (except for the conducting- state voltage of the semiconductors). The capacitor voltage remains unchanged.

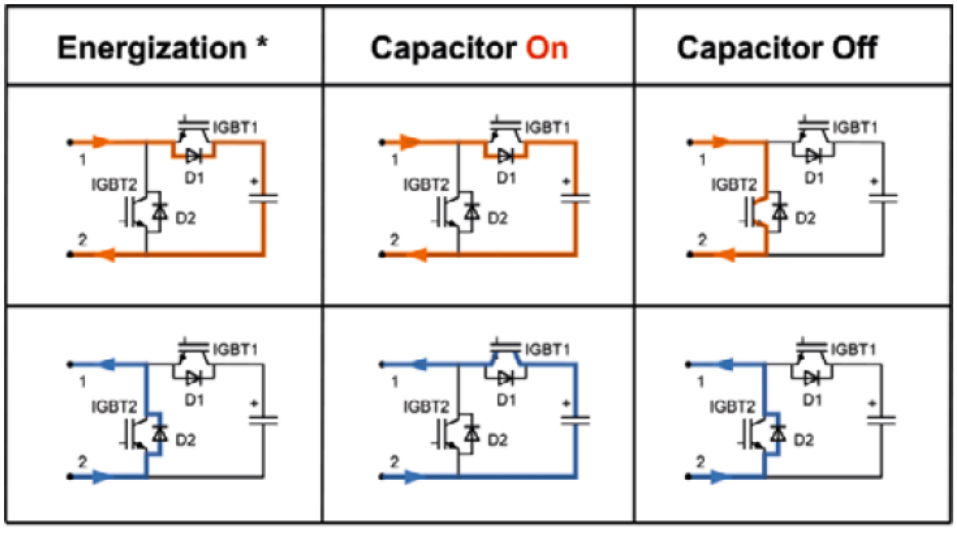

Figure 9. States and current paths of an MMC sub-module [33]

It is possible to separately and selectively control each of the individual sub-modules in all phase units. The two converter arms of each phase unit represent a controllable voltage source. The total voltage of the two converter arms in each phase unit equals the DC voltage, and by adjusting the ratio of the converter arm voltages in one phase unit, the desired sinusoidal voltage at the AC terminal is achieved [33].

A prime challenge in implementing MMCs is voltage balancing of the dc capacitor. Several schemes have been discussed in this domain [34]-[36]. The balancing scheme in this work has been derived from [34] with additional control loops for increased voltage regulation and harmonic reduction.

3.2 Capacitor Voltage Balancing

This section is dedicated to voltage balancing algorithm for sub-modules in an MMC circuit. We shall consider a case of an MMC inverter (Figure 10) for this exercise.

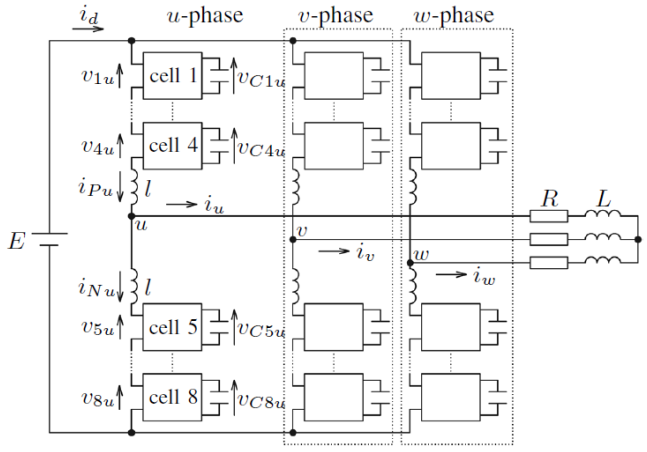

Figure 10. Circuit configuration of a double-star-configured modular multilevel inverter [34]

The SPWM control method is derived from [34] and a switching frequency of 540 Hz is employed.

Figure 10 shows a three-phase inverter based on the MMC. Each leg of the circuit consists of a stack of eight sub-modules and two buffer inductors. Let's consider the *u*-phase sub-modules because the operating principle in each phase is identical and independent of each other.

The following circuit equation exists in Figure 10:

$$E = \sum_{j=1}^{8} v_{ju} + l\frac{d}{dt}(i_{Pu} + i_{Nu}) \tag{1}$$

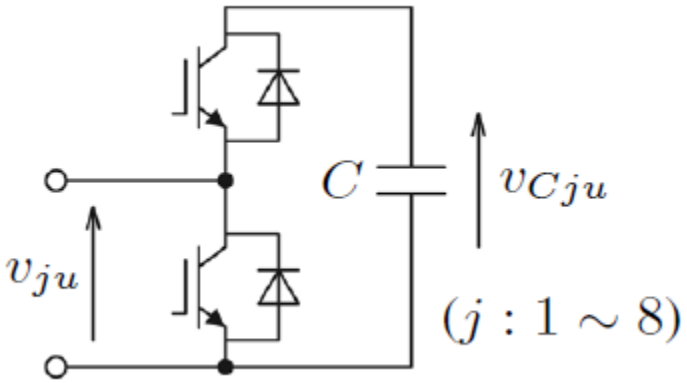

Figure 11. A sub-module of the MMC circuit [34]

(The subscript *j* implies the number of each sub-module)

In (1), E is a supply dc voltage, v_{ju} is an output voltage of each sub-module, l is the buffer inductance, and i_{Pu} and i_{Nu} are positive and negative arm currents, respectively.

The KVL (Kirchhoff's voltage law) loop given by (1) is referred to as the "dc loop", which is irreverent to the load. Let the circulating current along the u-phase dc loop be i_{Zu} as follows:

$$i_{Zu} = i_{Pu} - \frac{i_u}{2} = i_{Nu} + \frac{i_u}{2} = \frac{1}{2}(i_{Pu} + i_{Nu}) \quad [33] \ (2)$$

The voltage balancing control of 24 floating dc capacitors in Figure 10 can be divided into

1) Averaging control; and
2) Balancing control

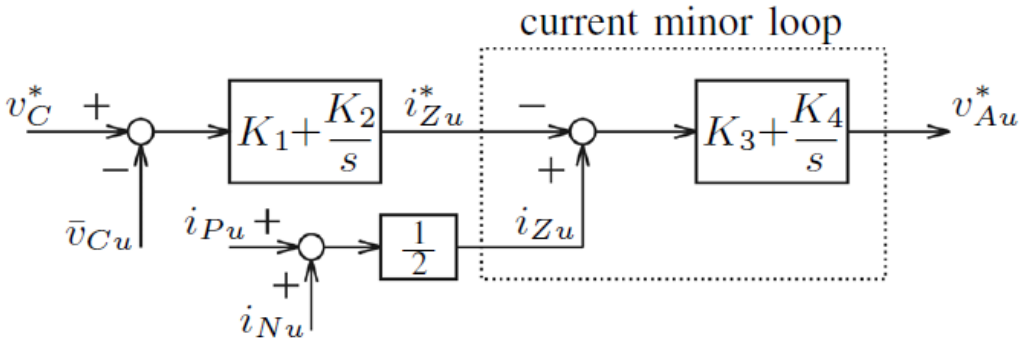

Figure 12. Block diagram of dc-capacitor averaging voltage control [34].

3.2.1 Averaging Control

Figure 12 shows a block diagram of the averaging control. It forces the u-phase average voltage $\overline{v_{Cu}}$ to follow its command v_C^* where $\overline{v_{Cu}}$ is given by

$$\overline{v_{Cu}} = \frac{1}{8}\sum_{j=1}^{8} v_{Cju} \qquad \text{[34] (3)}$$

Let a current command of i_{Zu} be i_{Zu}^*, as shown in Figure 12. It is given by:

$$i_{Zu}^* = K_1(v_C^* - \bar{v}_{Cu}) + K_2\int(v_C^* - \bar{v}_{Cu})dt \qquad \text{[34] (4)}$$

Voltage command obtained from the averaging control, v_{Au}^* is given by:

$$v_{Au}^* = K_3(i_{Zu} - i_{Zu}^*) + K_4\int(i_{Zu} - i_{Zu}^*)dt \qquad \text{[34] (5)}$$

When $v_C^* \geq \bar{v}_{Cu}$, i_{Zu}^* increases. The function of the current minor loop in Figure 12 forces the actual dc-loop current i_{Zu} to follow i_{Zu}^*. As a result, this feedback control of i_{Zu} enables $\overline{v_{Cu}}$ to follow its command v_C^* without being affected by the load current i_u.

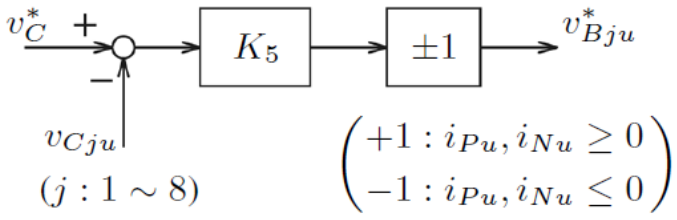

Figure 13. Block diagram of dc-capacitor balancing control [34]

3.2.2 Balancing Control

The use of the balancing control described in [37] forces the individual dc voltage to follow its command v_C^*. Figure 13 shows a block diagram of the *u*-phase balancing control, where

v^*_{Bju} is the voltage command obtained from the balancing control. Since the balancing control is either based on i_{Pu} or i_{Nu}, the polarity of v^*_{Bju} should be changed according to that of i_{Pu} or i_{Nu}. When $v_C{}^* \geq v_{Cju}$ (j:1 to 4) in the positive arm of Figure 10, a positive active power should be taken from the dc power supply into the four sub-modules. When i_{Pu} is positive, the product of v_{Bju} (= v^*_{Bju}) and i_{Pu} forms the positive active power. Finally, v^*_{Bju} for j = 1 to 4 is represented as:

$$v^*_{Bju} = K_5(v^*_C - v_{Cju}) \quad \text{for } i_{Pu} \geq 0 \text{; and} \qquad \text{[34] (6)}$$

$$= -K_5(v^*_C - v_{Cju}) \quad \text{for } i_{Pu} \leq 0$$

While v^*_{Bju} for j = 5 to 8 is represented as:

$$v^*_{Bju} = K_5(v^*_C - v_{Cju}) \quad \text{for } i_{Nu} \geq 0 \text{; and} \qquad \text{[34] (7)}$$

$$= -K_5(v^*_C - v_{Cju}) \quad \text{for } i_{Nu} \leq 0$$

Figure 14 shows a voltage command of each sub-module v^*_{ju}.

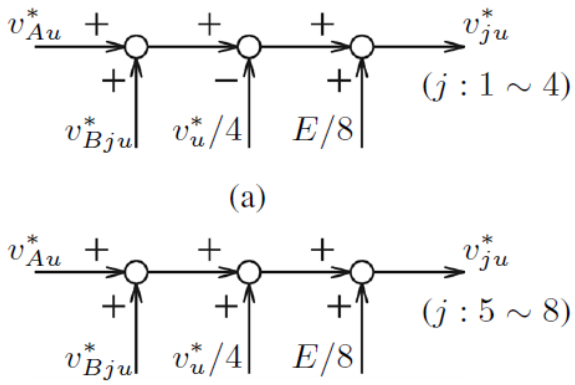

Figure 14. Voltage command of each arm: (a) Positive arm; and (b) negative arm [34]

The positive arm and negative arm commands are obtained as follows:

$$v_{ju}^{*} = v_{Au}^{*} + v_{Bju}^{*} - \frac{v_u^{*}}{4} + \frac{E}{8} \qquad (j\text{: 1 to 4}) \qquad \text{[34] (8)}$$

$$v_{ju}^{*} = v_{Au}^{*} + v_{Bju}^{*} + \frac{v_u^{*}}{4} + \frac{E}{8} \qquad (j\text{: 5 to 8}) \qquad \text{[34] (9)}$$

Where v_u^{*} is the ac-voltage command from the current controller (Section 3.3.5).

Note that Figure 14 includes the feed-forward control of the dc supply voltage, E. The voltage command v_{ju}^{*} is normalized by each dc-capacitor voltage v_{Cju} (a small amount of non-zero voltage is added to the component to avoid a division by zero situation). This is further followed by comparison with a triangular waveform having a maximum value of unity and minimum value of zero and carrier frequency f_C. The carrier waveform dedicated to each sub-module are phase shifted with respect to each other by a factor of $2\pi/n$ where n is the number of sub-modules in each phase (here n = 8). The phase shifting is essential for cancelling harmonics in the grid currents and improving current control for the VSCs.

The sub-module voltage balancing controller thus discussed can be utilized for different MMC configurations (example single terminal, back-to-back two terminal system [16], multi-terminal system or multi-staged MMC circuit with other converters such as dual active bridges [38].

However, implementing a VSC requires additional controls such as innermost current control, outer terminal voltage control, and the outermost power flow control. Additionally, for single-line to ground fault a negative sequence current controller must be employed [16].

These are traditional controllers and have been discussed briefly in the next sections.

3.3 Higher-level Controls

The implemented system with two terminals has a function to transfer power between two terminals. Therefore, the control structure has several controllers to transfer power. Figure 15 depicts the entire control structure. The voltage margin method for VSCs is used for this [39].

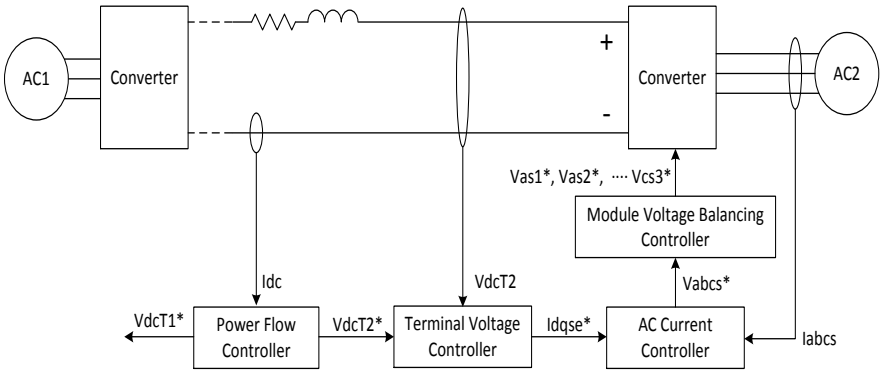

Figure 15. Back-to-back system control structure

Power flow controller determines the flowing power between the two terminals. The transferred power can be controlled by controlling the dc current, I_{dc}. To control the dc current, power flow controller decides the terminal voltage commands for the individual terminals [39].

This section briefly deals with the concept of voltage margin method used to control the power flow between two terminals (T1 and T2) of a back-to-back system.

3.3.1 Voltage Margin Control of VSCs [39]

A control scheme called the voltage margin method was used for the two-terminal dc link (terminal A and B). Figure 16 shows the *Ed-P* (*Ed* is terminal voltage, *P* is the associated power) characteristics of terminal A.

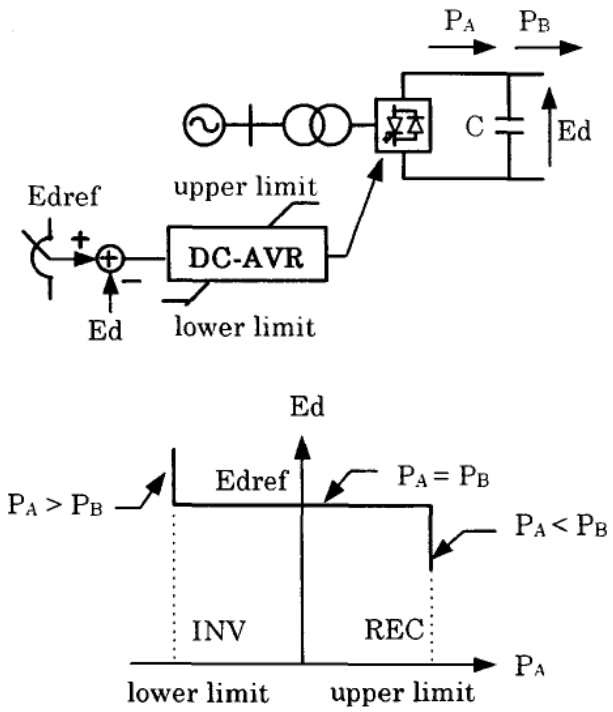

Figure 16. Ed-P characteristics of terminal A [39]

The dc voltage control (DC-AVR) is the fundamental control in the voltage source converter system just as dc current control is the basic function in the current sources converter system. The DC-AVR tries to keep the dc voltage to the reference value *Edref* by adjusting P_A, until P_A reaches the upper limit or the lower limit. For example, if the dc voltage is lower, the DC-AVR increases P_A until it reaches the upper limit to maintain the dc voltage. When P_B is

larger than the upper limit, however, the dc voltage decreases further. On the contrary, if the dc system voltage is higher than *Edref*, the DC-AVR reduces P_A. When P_B is smaller than the lower limit, however, the dc voltage increases further.

The voltage margin method is introduced in the voltage source converter system as shown in Figure 17. The voltage margin is defined as the difference between the dc reference voltages of the two terminals. When the active power is to be transmitted from terminal B to terminal A, the voltage margin is subtracted from the dc reference voltage for terminal A.

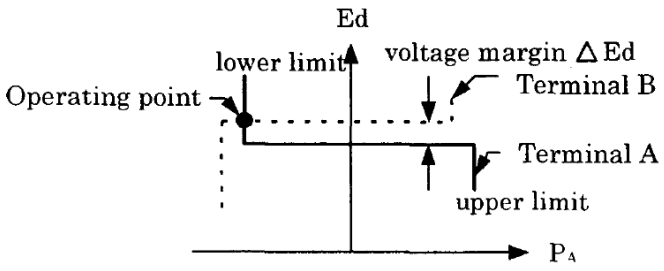

Figure 17. Operating point in voltage margin method [39]

Now that the terminal voltages of the individual terminals have been decided, each terminal is assigned their individual Terminal Voltage Controllers. This controller controls the terminal voltage with ac source power. Therefore, Terminal Voltage Controller generates the ac voltage reference for each terminal. These ac voltage references are divided into every sub-module voltage reference through Voltage Balancing Controller.

To control the power flow, two terminals can be simply modeled with inductor and resistor in dc grid as shown in Figure 18.

3.3.2 Power Flow Controller

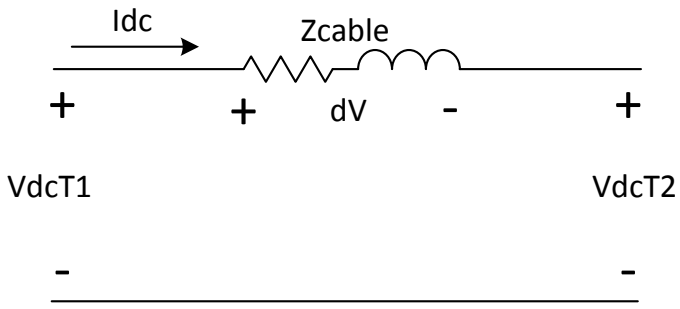

Figure 18. Two terminal model with dc grid impedance

The sending power from terminal one, T1, can be derived as (10). And the receiving power at T2 can be written as (11). Hereafter, the transferred power is defined as average power of sent power and the received power.

The transferred power can be calculated as (12).

$$P_{sent} = V_{dcT1} I_{dc} \tag{10}$$

$$P_{received} = V_{dcT2} I_{dc} \tag{11}$$

$$P = \frac{V_{dcT1} + V_{dcT2}}{2} I_{dc} \tag{12}$$

The dc current can be determined with the dc grid impedance and the voltage difference between the two terminals as (13).

$$I_{dc} = \frac{dV}{Z_{cable}} \tag{13}$$

So, the transferred power can be rewritten with the cable impedance and the voltage difference between two terminals as (14).

$$P = V_{dc\_avg} \frac{dV}{Z_{cable}} \tag{14}$$

Assuming that the dc average voltage is varying slowly, the transferred power can be determined by the dc current. As a result, Power Flow Controller should control the dc current, I_{dc}, by adjusting the voltage difference between the two terminals. Power Flow Controller can be implemented as shown in Figure 19.

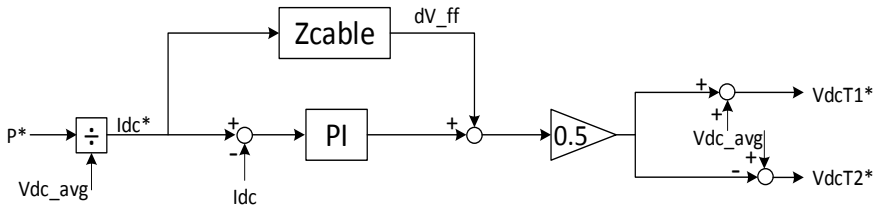

Figure 19. Power Flow Controller

According to the power reference, P^*, the dc current reference can be determined. PI-controller can be control the dc current. The control gain can be decided with cable parameters. The output of this controller is the voltage difference between the two terminals. This voltage difference is divided by two and added and subtracted from the terminal voltage references. To increase the dynamic performance of this controller, the voltage difference to generate the desired dc current can be used as feed-forward controller as *dV_ff*. This feed-forward value can be simply calculated with the known cable parameters. This parameter

error can be compensated by the PI-controller. The bandwidth of this Power Flow Controller should be lower than the Terminal Voltage Controller [16].

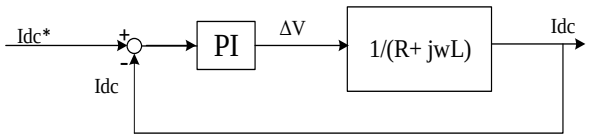

Figure 20. PI design for Power Flow Controller

$$\frac{1}{R+sL}\left(\frac{k_i}{s}+k_p\right)\left(I_{dc}^{*}-I_{dc}\right)=I_{dc} \tag{15}$$

$$\Rightarrow I_{dc}^{*}=\left(\frac{s^2L+s(R+k_p)+k_i}{k_p s+k_i}\right)I_{dc} \tag{16}$$

$$\Rightarrow \frac{I_{dc}}{I_{dc}^{*}}=\left(\frac{k_p s+k_i}{s^2L+s(R+k_p)+k_i}\right) \tag{17}$$

By canceling the pole of the system that comes from the *R-L* with a zero of the PI regulator, the transfer function of the closed loop system can be set as that of the first-order low-pass filter.

The values of k_p and k_i can be selected as:

$$k_p = Lw_c \tag{18}$$

$$k_i = Rw_c \tag{19}$$

Where w_c is set to be the bandwidth of the controller.

Selection of the PI gains as in (18) and (19) reduces (17) to:

$$\frac{I_{dc}}{I_{dc}^{*}} = \left(\frac{Lw_c s + Rw_c}{s^2 L + s(R + Lw_c) + Rw_c} \right) \tag{20}$$

$$= \left(\frac{w_c (Ls + R)}{(s + w_c)(Ls + R)} \right) \tag{21}$$

$$= \frac{w_c}{(s + w_c)} \tag{22}$$

From (22) it can be seen that the bandwidth of the regulator, w_{bw}, is set as w_c. Hence, after deciding the bandwidth, the gains are calculated directly from the parameters of the system.

3.3.3 Terminal Voltage Controller

The DC link voltage, V_{dcT} increases when the active power from the ac source is larger than the power consumed by the load and vice versa. Hence, dc link voltage can be regulated by adjusting active power to a dc link from an ac source. Hence the *q-axis* current (real current) reference can be composed of the feed-forward term, which corresponds to the estimated load power, and a term to regulate dc link voltage as given in (23). As a feedback controller to regulate dc link voltage, an integral and proportional (IP) regulator can be used to prevent overshoot of dc link voltage even with a step change of dc link voltage reference. The block diagram of an IP dc link voltage regulator including the feed-forward term is shown in Figure 21, where the *d-axis* current (reactive component of current) reference is set to zero to keep power factor as unity.

$$i_{qse}^{*} = -k_p V_{dcT} + k_i \int (V_{dcT}^{*} - V_{dcT})dt + \frac{P^{*}}{\left(\frac{3V_m}{2}\right)} \tag{23}$$

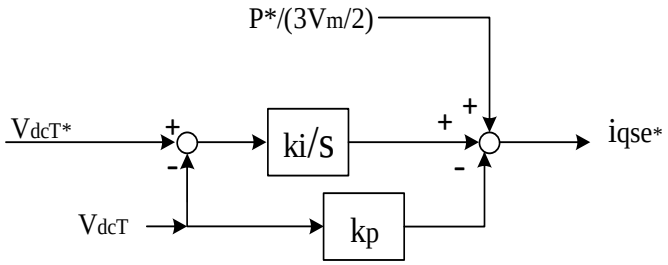

Figure 21. Control block diagram of the dc link voltage controller

The differential equation to represent the dc link voltage can be represented as:

$$\frac{C}{2}\frac{dV_{dcT}^{2}}{dt} = P_{in} - P_{out} \tag{24}$$

Where C is the total capacitance in the dc link. In case of MMC VSC this C is related to the sub-module capacitance by:

$$C = \frac{3C_{dc}}{n} \tag{25}$$

Where *n* is the number of sub-modules in a single arm of the MMC VSC circuit.

If the feed-forward compensation for load power is perfect, then dc link voltage can be described by (26) in terms of error of dc link voltage, $(V_{dcT}^{*} - V_{dcT})$, and gains of the IP regulator.

$$\frac{C}{2}\frac{dV_{dcT}^{2}}{dt} = \frac{3}{2}V_m\left(-k_p V_{dcT} + k_i \int (V_{dcT}^{*} - V_{dcT}\right)dt \tag{26}$$

Equation (26) is a non-linear differential equation, and it can be linearized at an operating point using small signal analysis. At this operating point, V_{d0}, dc link voltage can be represented as (27) by the small signal analysis.

$$V_{dcT}^2 \approx V_{dcT0}^2 + 2V_{dcT0}(V_{dcT} - V_{dcT0}) \tag{27}$$

Equation (27) can be substituted into (26), and then a linearized differential equation at an operating point can be derived as follows:

$$CV_{dcT0}\frac{dV_{dcT}}{dt} = \frac{3}{2}V_m\left(-k_pV_{dcT} + k_i\int(V_{dcT}^* - V_{dcT}\right)dt \tag{28}$$

From (28), a transfer function between reference dc link voltage and actual dc link can be obtained as follows:

$$\frac{V_{dcT}(s)}{V_{dcT}^*(s)} = \frac{\dfrac{\dfrac{3}{2}V_mk_i}{CV_{dcT0}}}{s^2 + \dfrac{\dfrac{3}{2}V_mk_p}{CV_{dcT0}}s + \dfrac{\dfrac{3}{2}V_mk_i}{CV_{dcT0}}} \tag{29}$$

$$= \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{30}$$

Where ω_n stands for the natural un-damped frequency and ζ stands for the damping coefficient. The gains of an IP regulator can be calculated through the frequency domain analysis. Under the assumption of well-regulated dc link voltage, the operated point will follow the reference command. The gains can be set as:

$$k_p = 2\zeta\omega_n \frac{CV_{dcT}^*}{\frac{3}{2}V_m} \tag{31}$$

$$k_i = \omega_n^2 \frac{CV_{dcT}^*}{\frac{3}{2}V_m} \tag{32}$$

With these gains, the control bandwidth of a dc link voltage regulation loop, w_{bw}, is given by [40]:

$$\omega_{bw} = \omega_n \left[\left(1-2\zeta^2\right)+\sqrt{4\zeta^4-4\zeta^2+2}\right]^{0.5} \tag{33}$$

To prevent overshoot of dc link voltage, the damping factor, ζ, should be higher than one. If ζ is selected as 1.2, then w_{bw} is half of ω_n from (33). For power factor control, given by (34),

$$PF = \frac{i_q^e}{\sqrt{i_d^{e^2} + i_q^{e^2}}} \tag{34}$$

a d-axis current reference can be set as (35)

$$i_d^{e^*} = i_q^{e^*} \frac{\sqrt{1-PF^2}}{PF} \tag{35}$$

For unity power factor the d-axis current should be regulated to zero, this implies that maximum power per ampere is being obtained. If a VSC has to be operated as a leading power factor to an ac source, the d-axis current should be regulated as a positive value. In general, the ac distribution network, as well as the power factor at the ac source with industrial loads such as motors and lightings is usually lagging. Therefore, the VSC should

be operated in leading power factor range to compensate for the lagging power of the largely inductive loads [40].

The terminal voltage reference which is the output which is the output of Power Flow Controller is used as reference of Terminal Voltage Controller of the each terminal. Terminal Voltage Controller is illustrated in Figure 22. This Terminal Voltage Controller generates the d/q axis current references of the ac side. Torque coefficient can be determined from the positive sequence voltage of AC voltage source. "NF" means a notch filter which is to remove the two times frequency of the AC fundamental frequency. If there is unbalance in AC side, the voltage variation of the two times fundamental frequency component happens. To increase the dynamic performance, the power reference can be used as feed-forward control. The d-axis current reference can be calculated with the reactive power reference.

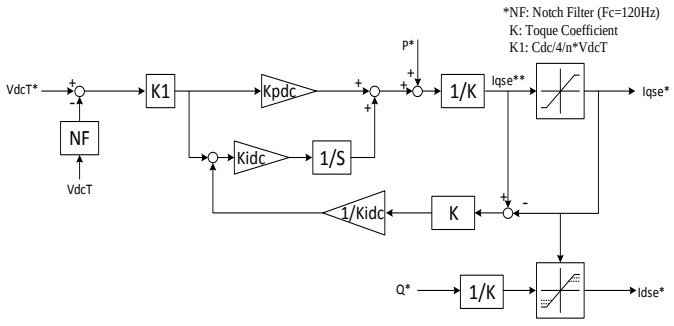

Figure 22. Terminal Voltage Controller

The current references are limited by the rated current of the switching devices. Therefore, simple anti-windup loop is added in the integral feed-back control loop to generate the q-axis

current reference [41], [42]. The limit of the d-axis current reference is varying according to the q-axis current reference value [16]. We should briefly look at what an anti-windup loop is before moving on the current control of the VSCs in the following section.

3.3.4 Anti-Windup [41], [42]

All physical variables in the control system are bounded by physical limitations. As an example consider a generic current regulator, the output of which is the input to the power amplifier such as a three-phase-controlled rectifier, which decides the terminal voltage of DC machine. In this case the magnitude of the voltage is limited by input source voltage of the amplifier whatever the output of the regulator itself is. If the terminal voltage is saturated by the physical limitation but if the output of the regulator is not bounded at that physical limitation, then the control system including a DC machine is out of control of the closed loop, where the regulator output has nothing to do with the input to the physical system under control. In this case the response to the command of the control system is sluggish and oscillatory and is uncontrollable by the regulator.

To prevent this situation, the output of the regulator can be simply bounded by a limiter as shown in Figure 23. However, if the integrator terms are included in the output of the regulator, then the output of the integrator itself is not bounded by the limiter and it would be wound up above the limited value of the regulator though the output of the regulator is limited. This phenomenon is called “wind-up.” If the wind-up of the integrator of the regulator occurs, then the input to the integrator, which is the regulation error, should have a sign opposite to that of the output of the integrator for a while to clear the wind-up. In this

reason, the response would have a large overshoot or undershoot because of the integrator wind-up. In the worst case the control system may be unstable.

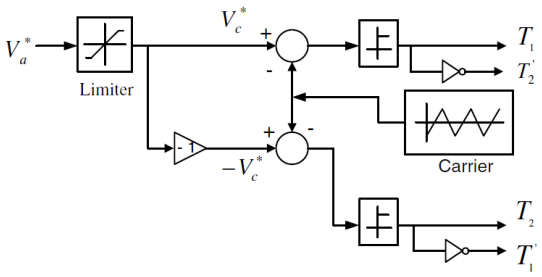

Figure 23. Control block diagram of PWM signals for a four-quadrant dc/dc converter

In a conventional PI regulator implemented with operational amplifier (OP Amp), the output of OP Amp including the integrator itself is inherently limited by the supply voltage such as $+V_{cc}$ or $-V_{cc}$. To limit the output of the integrator further, back-to-back Zener diodes can be used as shown in Figure 24.

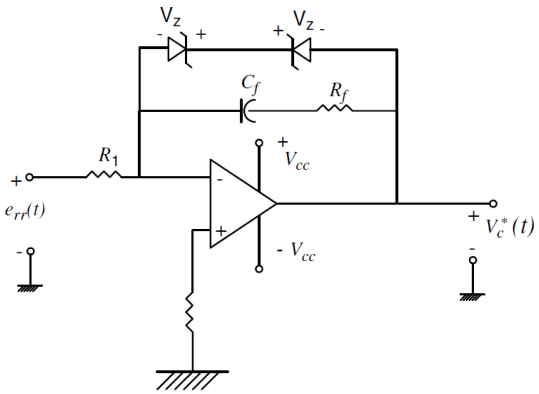

Figure 24. PI regulator implemented using an Op-Amp with Zener diodes to limit output of the integrator

In case of DSP using fixed-point operation, or computer simulation the output of the integrator should be properly bounded with consideration of the physical limitation of the variables. The limitation of the integrator output, which is called an “anti-wind-up,” can be done as shown in Figure 25.

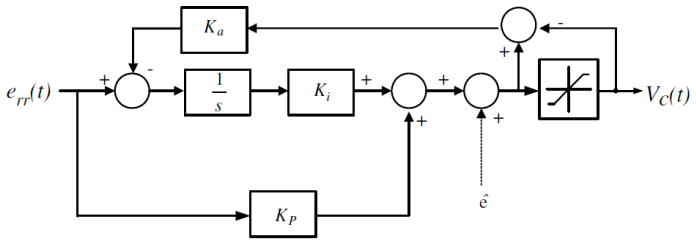

Figure 25. Implementation of anti-windup controller

K_a is usually set as $1/K_p$. However, in general, such a setting gives a reasonable performance, but the anti-wind-up gain, K_a, can be tuned to get better performance in the range of 1/3 to 3 times of K_p. This anti-windup function should be incorporated not only in a PI regulator but also in any regulator that has integral terms [40].

3.3.5 Current Control

A boost rectifier or a VSC with a grid input can be viewed as a circuit in Figure 26. Here it is assumed that the instantaneous sum of the three EMF voltages is zero: $e_{as} + e_{bs} + e_{cs} = 0$. And EMF is sinusoidal and its angular velocity is ω_e.

The circuit in Figure 26 can be described by (36).

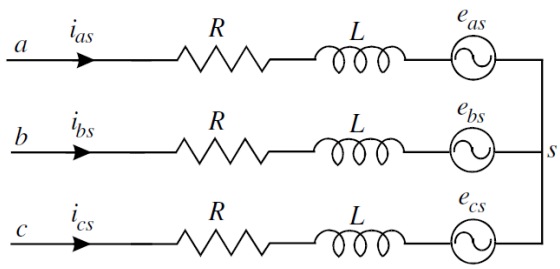

Figure 26. Balanced three-phase RL EMF circuit

$$V_{as} = Ri_{as} + L\frac{di_{as}}{dt} + e_{as}$$

$$V_{bs} = Ri_{bs} + L\frac{di_{bs}}{dt} + e_{bs} \quad (36)$$

$$V_{cs} = Ri_{cs} + L\frac{di_{cs}}{dt} + e_{cs}$$

Equation (36) can be rewritten in a stationary direct-quadrature (d-q) reference frame as (37). Because of the balanced impedance and EMF, there is no *n*-term voltage and current in the *d*-*q*-*n* axes.

$$V_{ds}^{s} = Ri_{ds}^{s} + L\frac{di_{ds}^{s}}{dt} + e_{ds}^{s} \quad (37)$$

$$V_{qs}^{s} = Ri_{qs}^{s} + L\frac{di_{qs}^{s}}{dt} + e_{qs}^{s}$$

The equation (37) can be further expressed in synchronously rotating frame, whose rotating speed is ω_e, as in (38):

$$V_{ds}^e = Ri_{ds}^e + L\frac{di_{ds}^e}{dt} - \omega_e L i_{qs}^e + e_{ds}^e \tag{38}$$

$$V_{qs}^e = Ri_{qs}^e + L\frac{di_{qs}^e}{dt} - \omega_e L i_{ds}^e + e_{qs}^e$$

If all the electrical variables of the circuit in Figure 26 vary sinusoidally at angular frequency, ω_e, then the variables in (38) are just dc quantities. Therefore, the design methodology in Power Flow Controller (Section 3.3.2) can be directly used here in current regulator. Figure 27 shows a typical current PI regulator in the synchronous *d-q* frame.

Since there are two axes here in *d-q* frame, so two sets of regulators are used for three-phase circuit. All the gain tuning is the same as in section 3.3.2. The only difference is the feed-forwarding voltages including e_{ds}^e and e_{qs}^e, but also decoupling terms (+ $\omega_e L i_{ds}^e$ in *q*-axis and - $\omega_e L i_{qs}^e$ in *d*-axis). See equation (39).

$$V_{ds\_ff}^e = -\omega_e L i_{qs}^e + e_{ds}^e \tag{39}$$

$$V_{qs\_ff}^e = +\omega_e L i_{ds}^e + e_{qs}^e$$

See Figure 27 for the generic PI controller for current control.

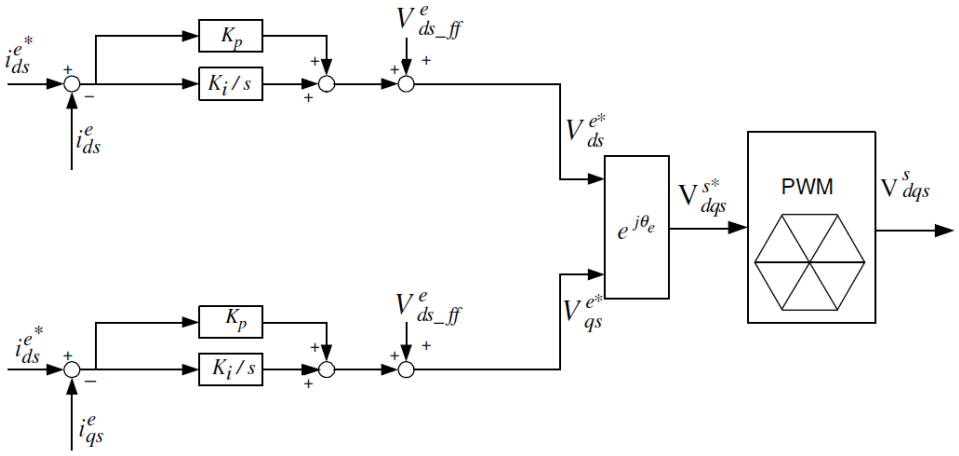

Figure 27. Current control for balanced three-phase circuit

As in section 3.3.3 the PI regulator gains can be adjusted to set the controller bandwidth as w_{bw}.

$$k_p = Lw_{bw} \tag{41}$$

$$k_i = Rw_{bw} \tag{42}$$

As mentioned earlier this scheme is only applicable for balanced three-phase circuits, which is mostly encountered in steady-state operations as far as power electronics and systems is concerned. However, this work also includes the line-ground (L-G, L-L-G) performance of the back-to-back MMC system. In the cases of faults additional currents are encountered because of the loss of inherent assumption in the current controller that there are no zero or negative-sequence currents flowing in the circuit. However, this assumption is invalid in the case of faults. To account for mitigation of these entities additional controls are included which are similar in structure to the positive (or regular) controls encountered till now. This is discussed briefly in the following section.

3.3.6 Dual Current-control Scheme for Line-ground Faults [16]

To develop the control structure for the MMC in d-q reference frame, modeling of the power electronics system is essential. The modeling used in this paper is based on the principal circuit analysis writing voltage and current equations for storage elements known as state equations. The general scheme of a three-phase VSC is shown in Figure 28.

The state equations of each VSC in the $d-q$ synchronous reference frame under unbalanced operating conditions can be separated into two independent equations; one each for positive and negative sequence.

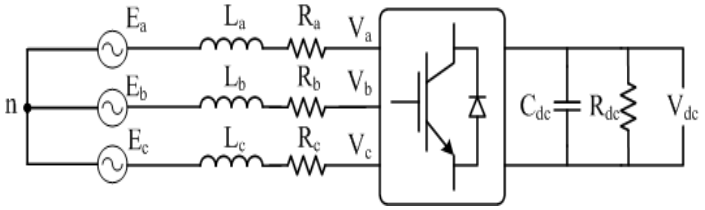

Figure 28. Structure of a voltage source converter

Low-frequency network disturbances such as distortion, voltage dips, phase-variation and amplitude variation of the input voltage can be described by a sum of positive, negative and zero sequence components of the input voltage of fundamental frequency. Therefore, an unbalanced three-phase input voltage can be represented as (43) [16].

$$E_{dqs} = e^{j\omega t}E_{dq}^{p} + e^{-j\omega t}E_{dq}^{n} = e^{j\omega t}(E_d^p + jE_q^p) + e^{-j\omega t}(E_d^n + jE_q^n) \qquad \text{[16] (43)}$$

The unbalanced three-phase input current is also expressed in the same manner as the input voltage. With the unbalanced input voltage and input currents, the input complex power is obtained by (44).

$$S_{in} = \frac{3}{2} E_{dqs} I_{dqs}^{*} = \frac{3}{2} (e^{j\omega t} E_{dq}^{p} + e^{-j\omega t} E_{dq}^{n})(e^{j\omega t} I_{dq}^{p} + e^{-j\omega t} I_{dq}^{n})^{*} \qquad \text{[16] (44)}$$

Applying (43) to (44), the instantaneous active power and instantaneous reactive power are obtained as (45).

$$\begin{aligned} S_{in} = &\left[P_o^{in} + P_{c2}^{in} \cos(2\omega t) + P_{s2}^{in} \sin(2\omega t) \right] \\ &+ \left[Q_o^{in} + Q_{c2}^{in} \cos(2\omega t) + Q_{s2}^{in} \sin(2\omega t) \right] \end{aligned} \qquad \text{[16] (45)}$$

Where,

$$\begin{aligned} P_o^{in} &= 1.5(E_d^p I_d^p + E_q^p I_q^p + E_d^n I_d^n + E_q^n I_q^n) \\ P_{c2}^{in} &= 1.5(E_d^p I_d^n + E_q^p I_q^n + E_d^n I_d^p + E_q^n I_q^p) \\ P_{s2}^{in} &= 1.5(E_q^n I_d^p - E_d^n I_q^p - E_q^p I_d^n + E_d^p I_q^n) \\ Q_o^{in} &= 1.5(E_q^p I_d^p - E_d^p I_q^p + E_q^n I_d^n - E_d^n I_q^n) \\ Q_{c2}^{in} &= 1.5(E_q^p I_d^n - E_d^p I_q^n + E_q^n I_d^p - E_d^n I_q^p) \\ Q_{s2}^{in} &= 1.5(E_d^p I_d^n + E_q^p I_q^n - E_d^n I_d^p - E_q^n I_q^p) \end{aligned} \qquad \text{[16] (46)}$$

Real instantaneous active power, $P_{in}(t)$ is delivered to the dc link and determines the dc voltage level. Hence, if $P_{in}(t)$ varies with time for P_{c2} and P_{s2} being non-zero, then the dc voltage fluctuates. To avoid this, the coefficients of P_{c2} and P_{s2} should be eliminated. The dc component Q_o of the instantaneous reactive power should also be nullified. Q_o represents the average reactive power exchanged with the network, and it should be nullified to achieve

unity power factor. Using an additional condition on the average active power, four equations are obtained in (47) [43], [44].

$$\frac{2}{3}\begin{bmatrix} P_o^{in} \\ Q_o^{in} \\ P_{s2}^{in} \\ P_{c2}^{in} \end{bmatrix} = \begin{bmatrix} \frac{2}{3}P_o^{in} \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} E_d^p & E_q^p & E_d^n & E_q^n \\ E_q^p & -E_d^p & E_q^n & -E_d^n \\ E_q^n & -E_d^n & -E_q^p & E_d^p \\ E_d^n & E_q^n & E_d^p & E_q^p \end{bmatrix} \begin{bmatrix} I_d^p \\ I_q^p \\ I_d^n \\ I_q^n \end{bmatrix} \qquad [16]\,(47)$$

In the control scheme, the positive sequence current is regulated in the positive synchronous frame by one controller and similarly a negative-sequence current controller is employed for the negative sequence currents [43]-[46].

$$\begin{aligned} V_d^p &= E_d^p - (PI)(I_d^{p*} - I_d^p) + \omega L I_q^p \\ V_q^p &= E_q^p - (PI)(I_q^{p*} - I_q^p) - \omega L I_d^p \\ V_d^n &= E_d^n - (PI)(I_d^{n*} - I_d^n) - \omega L I_q^n \\ V_q^n &= E_q^n - (PI)(I_q^{n*} - I_q^n) + \omega L I_d^n \end{aligned} \qquad [16]\,(48)$$

Finally, the output of the converter defined in the stationary reference frame as (49) is controlled through Sine PWM.

$$V_s = e^{j\omega t}(V_d^p + jV_q^p) + e^{-j\omega t}(V_d^n + jV_q^n) \qquad [16]\,(49)$$

The combined controls for the positive and negative sequence currents is in Figure 29. Notice that it is simply an addition of negative sequence current controller to Figure 27.

The negative sequence power controller is designed to eliminate the negative sequence currents by fixing the command reference to zero [35], [45].

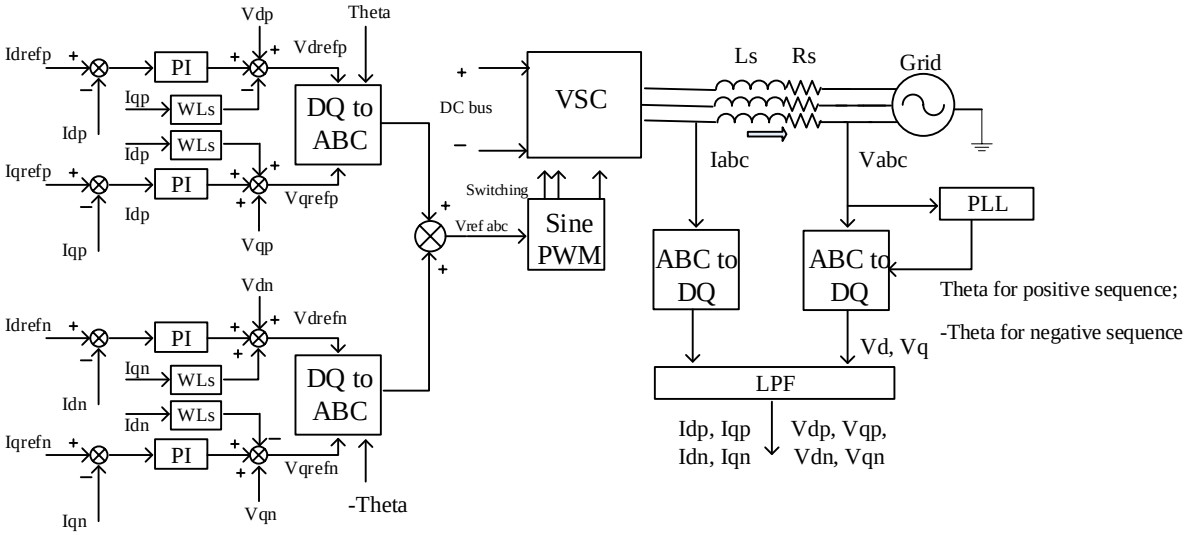

Figure 29. Current controller

Chapter 4: Dynamic Performance Evaluation of the MMC

In this work an MMC based back-to-back system of converters was implemented. The overall system block diagram is in Figure 30. The system was simulated on various platforms including MATLAB PLECS, PSCAD/EMTDC and RTDS.

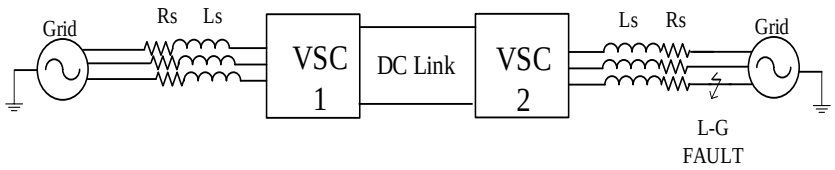

Figure 30. Back-to-back MMC HVDC system

Table 2. System specifications

Grid1, Grid2	3.3 kV line-line RMS
DC bus	9 kV
System rating	1 MVA
DC capacitance	1 mF
Grid Inductance	8 mH
Sub-modules/phase	8
SPWM frequency	540 Hz
Equivalent switching frequency	4320 Hz (= 540 Hz×8)
Capacitor nominal voltage	2.25 kV (= 9 kV/4)
Decoupling inductance	5 mH (12%)

4.1 Back-to-back MMC PSCAD/EMTDC Results

4.1.1 Steady-state Results

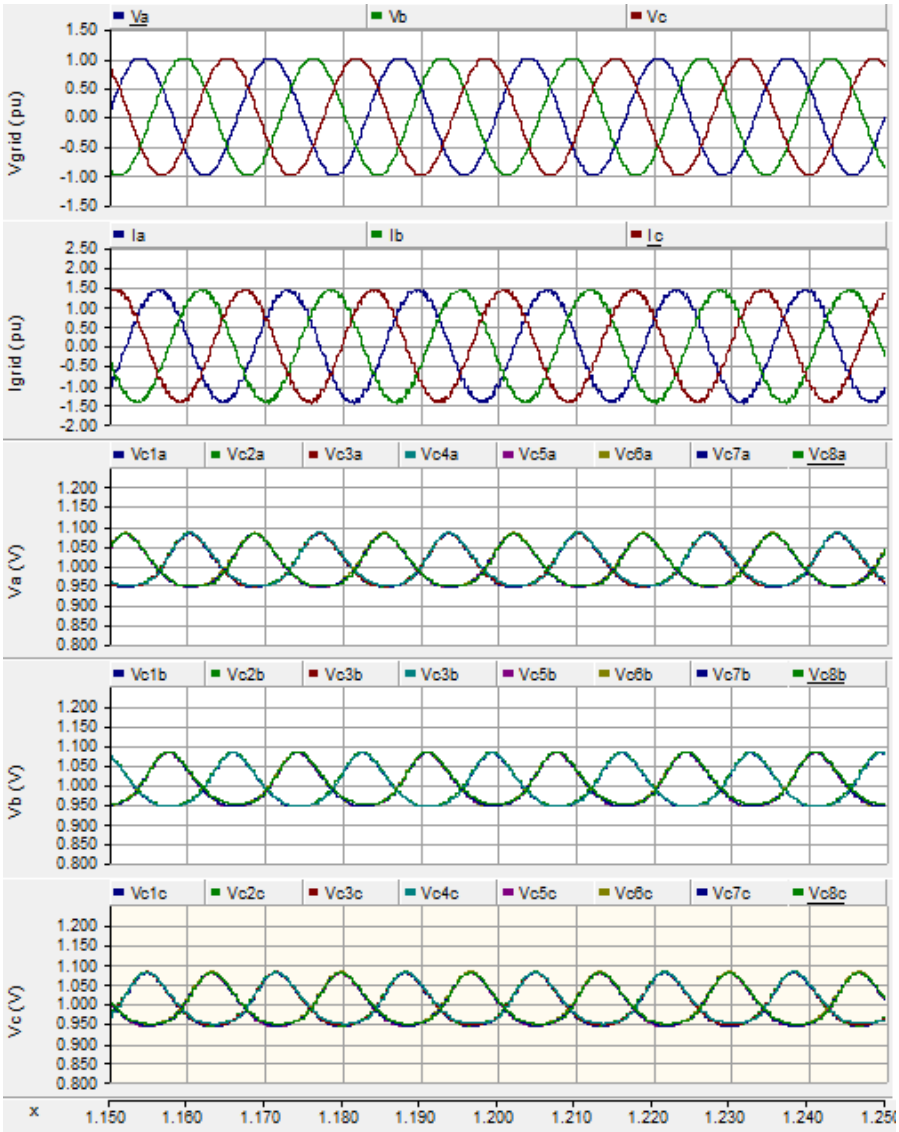

Figure 31. Steady state sending end waveforms. a) Grid voltages; b) Grid currents; Sub-module dc capacitor voltages: c) Phase-A; d) Phase-B; and e) Phase-C (pu)

It is evident from the current waveforms that MMC based VSCs do not require filters since the currents are perfect sinusoids. Also, the power factor for chosen here is unity and the peak-to-peak ripple in capacitor voltages is 0.102 kV, which is 10.2% of the set sub-module dc capacitor voltage (2.25kV).

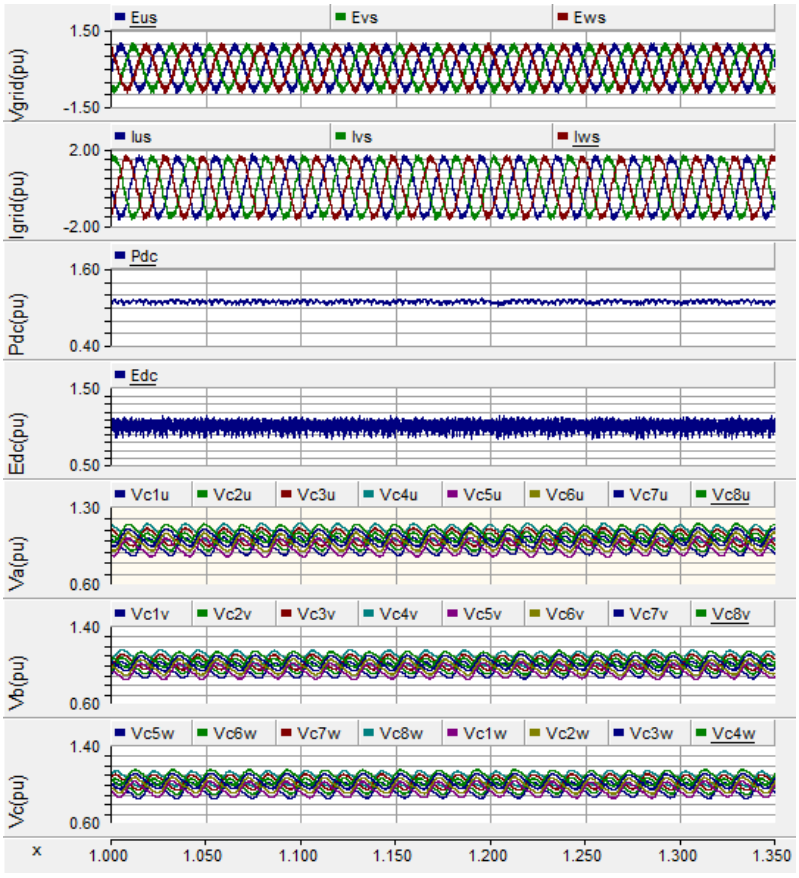

Figure 32. Steady state receiving end waveforms. a) Grid voltages; b) Grid currents; c) Power transfer; d) Terminal voltage; Sub-module dc capacitor voltages: e) Phase-A; f) Phase-B; and g) Phase-C (pu)

4.1.2 L-G Fault Case Results

Line-ground fault cases (100 ms each) were simulated on both sending and receiving ends. The following waveforms correspond to the fault on the receiving end (Figure 33), and the sending end (Figure 34).

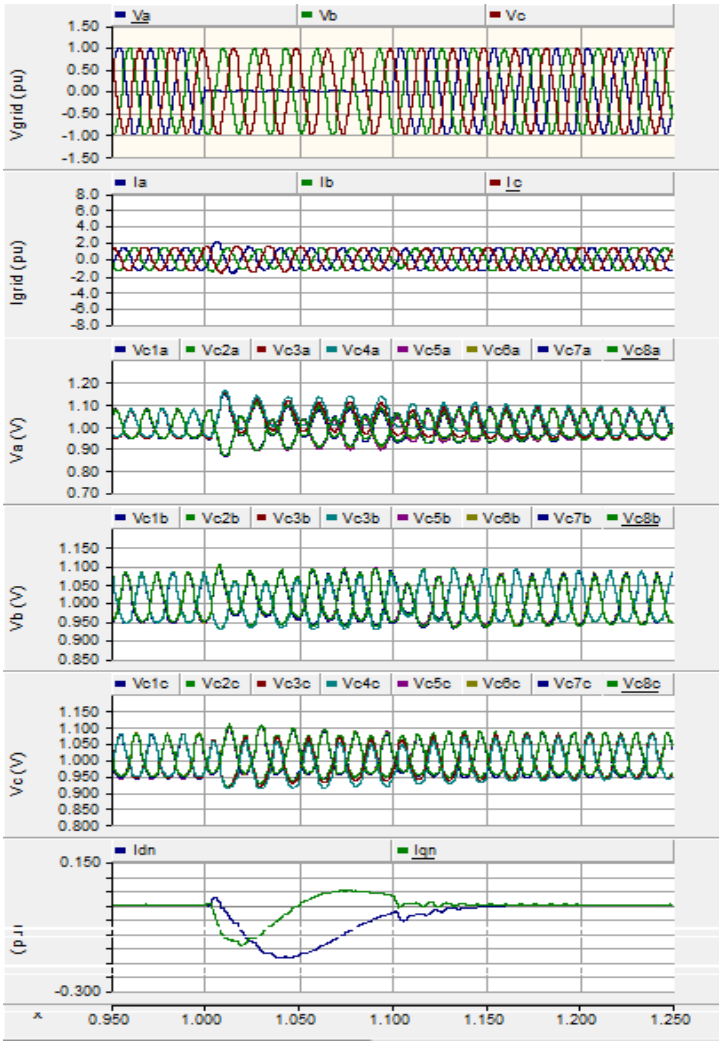

Figure 33. L-G fault receiving end. a) Grid voltages; b) Grid currents; Sub-module dc capacitor voltages: c) Phase-A; d) Phase-B; e) Phase-C; and f) Negative sequence currents (pu)

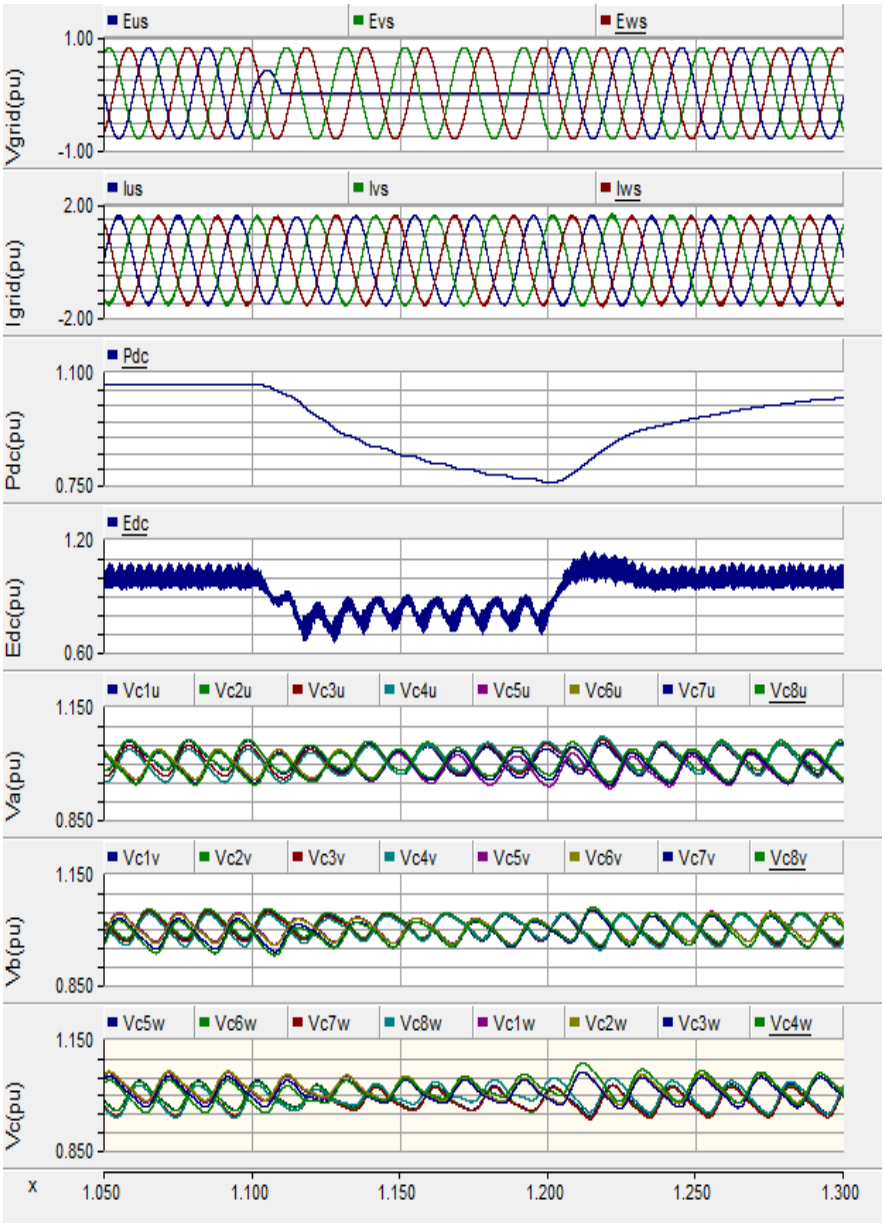

Figure 34. L-G fault sending end. a) Grid voltages; b) Grid currents; c) Power transferred; d) Terminal voltage; Sub-module dc capacitor voltages: e) Phase-A; f) Phase-B; and g) Phase-C (pu)

A quick note about the sub-module capacitance:

The capacitance of sub-module capacitor is critical parameter in this system. According to this capacitance, not only the voltage variation of sub-module but also the terminal voltage

variation is determined. Especially, the voltage variation during the ac side fault is severely influenced by the capacitance. Generally, the voltage variation can be decreased as the capacitor size is increased. However, the small capacitor is preferred for cost, maintenance, volume and so on. When any voltage ripple reduction technique is not applied, the voltage variation can be calculated as (50).

$$\Delta V_{pp} = \frac{V_s I_s}{4\pi f C V_{dc\_avg}} \tag{50}$$

Additionally, the inertia of the capacitors has to be considered for selecting the value of the capacitance. The time constant, H, is given by:

$$H = \frac{\frac{1}{2} C_{dc} V_{dc}^2}{MVA} \tag{51}$$

This ratio (milliseconds) decides the ride-through capability of the capacitors. What this means is that the capacitor will hold energy equal to the power consumed by the rated load over a time period H milliseconds. Thus, the value selected has a significant effect on the fault performance of the MMC. Now, capacitor selection, in practice, is decided also by the availability, maintenance, and the voltage rating of the sub-module parallel device and hence the terminal voltage for the system.

Dual current controller performance

As discussed in section 3.3.6, the dual current control was employed for optimal fault performance and negative sequence current mitigation. In Figure 35 it can be seen that upon the disabling of the negative sequence controller, (till 1.2 seconds) I_{dn} and I_{qn} increase to

about 0.40 per unit; however, these are contained when the negative sequence controller is enabled. As a comparison Figures 33 and 35 can be compared for controller performance.

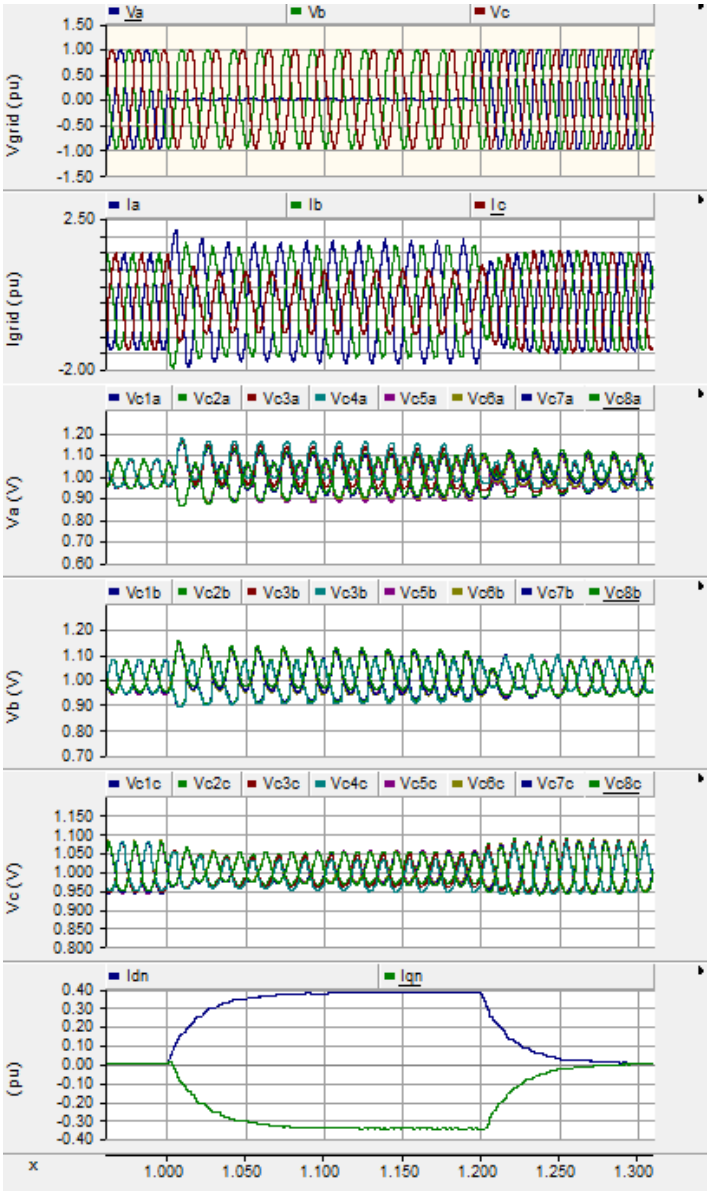

Figure 35. Dual current controller performance. a) Grid voltages; b) Grid currents; Sub-module dc capacitor voltages: c) Phase-A; d) Phase-B; e) Phase-C; and f) Negative sequence currents (pu)

4.2 MMC RTDS Implementation

For MMC implementation the first step would be to use an rtds_vsc_MMC5 component from the small time step library.

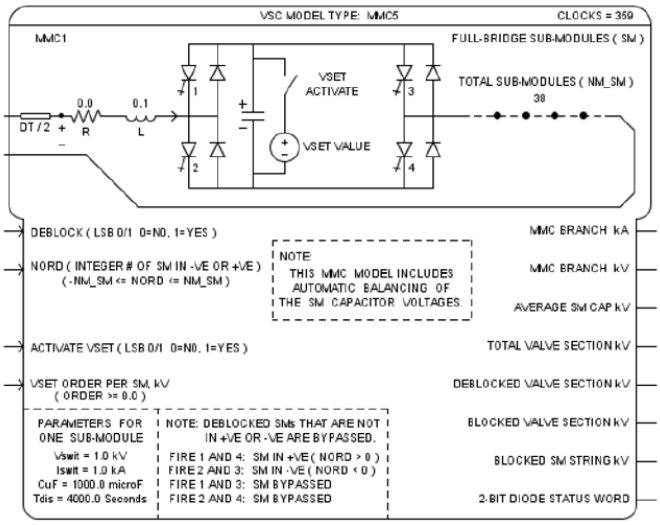

Figure 36. Icon of rtds_vsc_MMC5 model component

This model has the advantage that it provides for the balancing of sub-module capacitor voltages internally. Since, the balancing algorithm is out of the picture, the higher level VSC control algorithms can be implemented considering infinite bandwidth of the balancing algorithm. The model executes on both GPC and PB5 processors and supports full-bridge as well as half-bridge operation. The only input that this component needs is a 0/1 for the sub-module to be blocked or de-blocked and a number for telling the component that how many sub-modules are to be inserted in the arms (either positively or negatively).

As the next step, the rtds_vsc_CHAINV5 component should be used. It is different from the previous version that it takes gating pulses from PWM signals.

In the case of the rtds_vsc_CHAINV5 model, the firing pulse words for individual sub-modules are packed into a number of larger integer control words that can be read by the model. Firing pulse words containing two (2) bits each are used for the half−bridge sub-modules while three (3) bit firing pulse words are used for the full−bridge sub-modules valves. Consequently, up to 16 two−bit half−bridge firing pulse words can be packed into each 32 bit integer control word.

Similarly, up to 10 three−bit full−bridge firing pulse words can be packed in each 32 bit integer control word. We can specify the number of large control words to use and the number of firing pulse words that are in each control word. The only requirement is that there should be one firing pulse word per SM.

Within a given control word, there must be no space between neighboring firing pulse words. If the contiguous group of firing pulse words does not include the least significant bit (LSB), then the we must specify the right shift required to shift the contiguous group of bits so that it begins at the LSB. Once shifted, the firing pulse bits for the first sub-module are always the least significant bits of the 1st control word.

Since, each small time step bridge has a limitation of 16 electrical nodes, so for simulating higher number of sub-modules, multiple small time step bridges can be connected through a t-line interface model (Figure 37). These t-line models can also be expanded for more than two terminals. In this work, t-line models were extensively used for making connections

between small time step bridges, intra-rack as well as in conjuring massive circuits spanning all the three racks implying inter-rack communication. This is only possible since the processor cards on RTDS are daisy chained which makes for higher computational power. For more details RTDS user manual shall come handy [47].

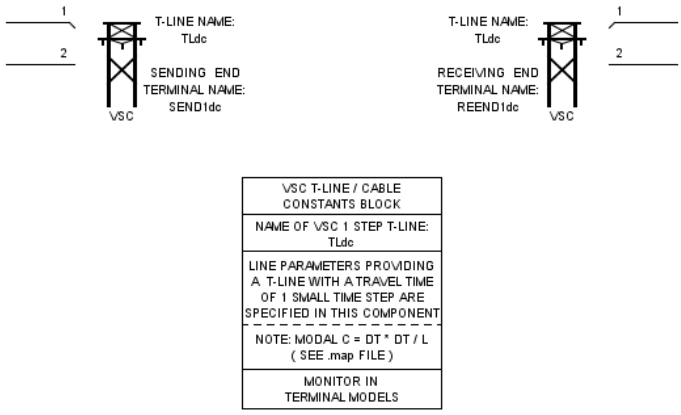

Figure 37. RTDS t-line model

In the beginning, all the power sub-modules are blocked (i.e., no gate pulses) till the sub-module capacitors charge through the IGBT anti-parallel diodes (Figure 9). Once charged and the terminal voltage stabilized, the sub-modules are de-blocked and the controller comes into picture. Up till here the power transfer reference is still zero. The dc breaker is turned on after the sub-module capacitor voltages settle at the reference value. Now, power can be ramped up or down as desired.

4.2.1 Steady-state Results

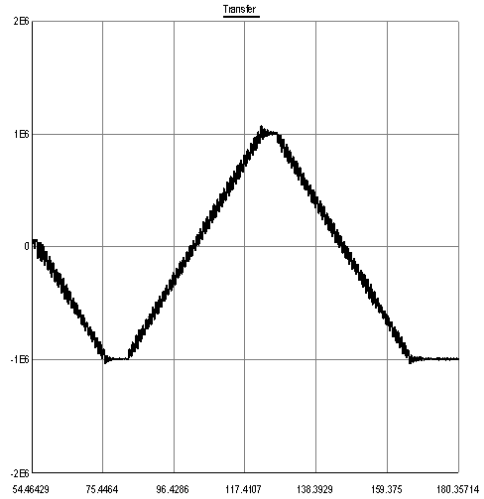

Figure 38. Steady state power transfer (W) between the back-to-back HVDC terminals

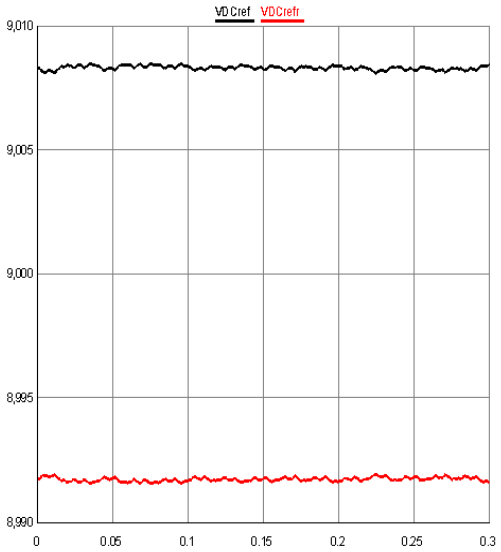

Figure 39. Terminal voltages (V) at power transfer of 1 MW. (Sending end in red)

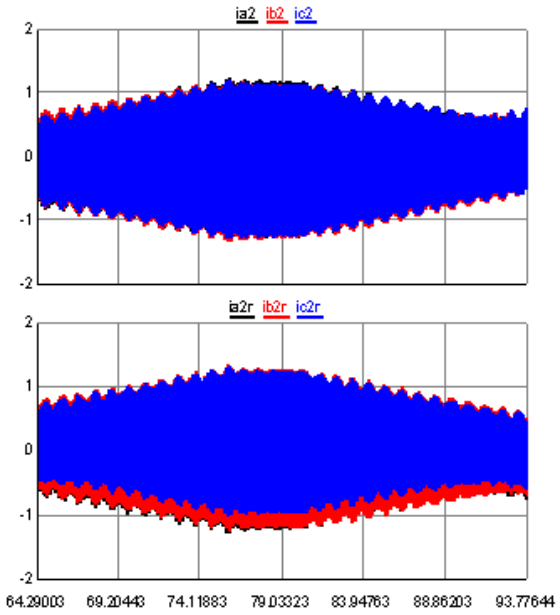

Figure 40. Grid currents (pu). Receiving end on top

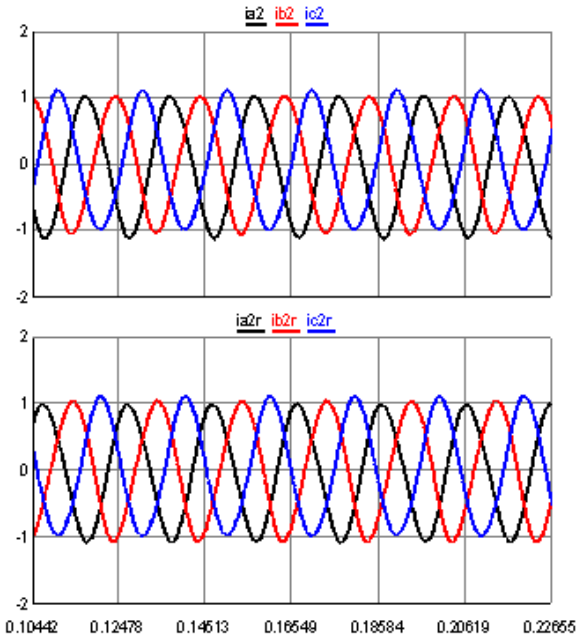

Figure 41. Grid currents (pu). Receiving end on top (zoomed)

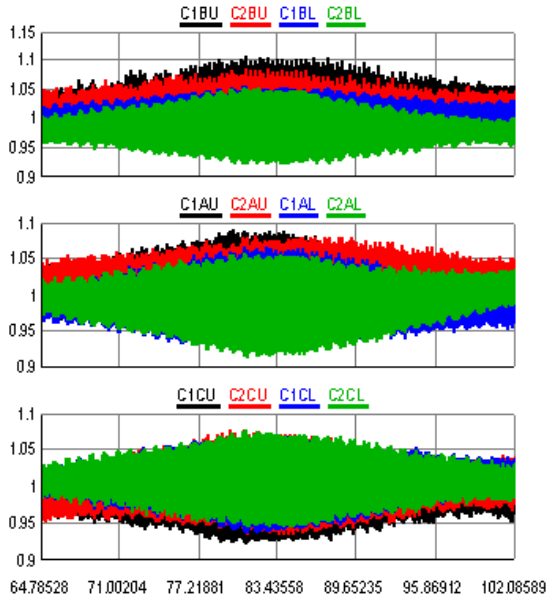

Figure 42. Receiving-end sub-module capacitor voltages for power ramp up and ramp-down (pu)

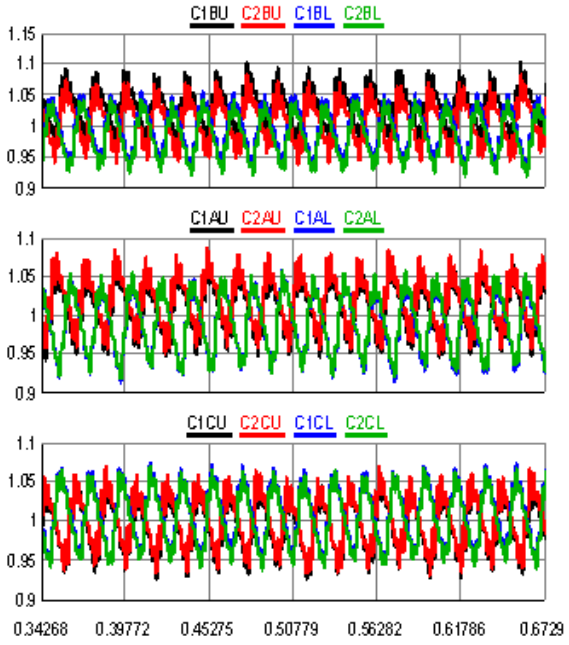

Figure 43. Zoomed view of Figure 42

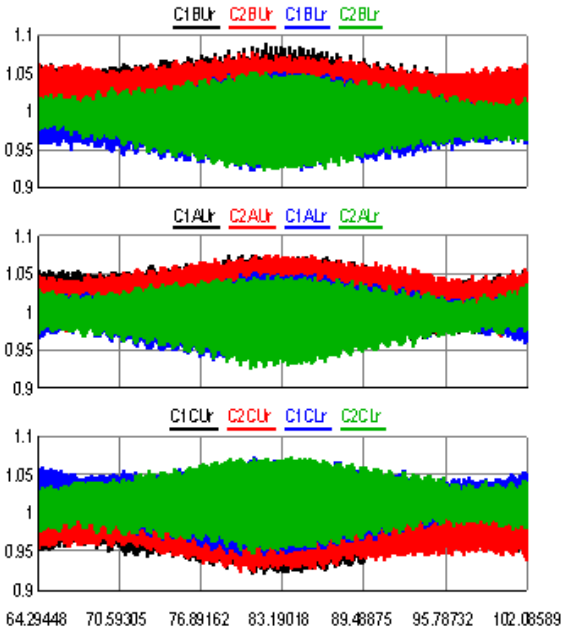

Figure 44. Sending-end sub-module capacitor voltages for power ramp up and ramp-down (pu)

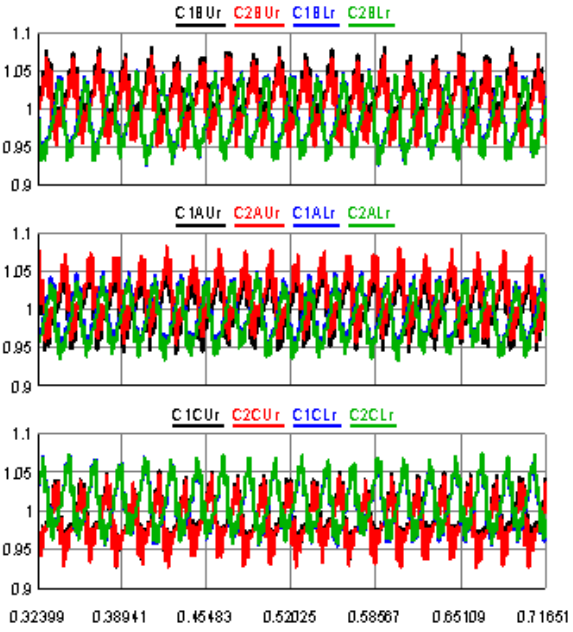

Figure 45. Zoomed view of Figure 44

4.2.2 Step Response

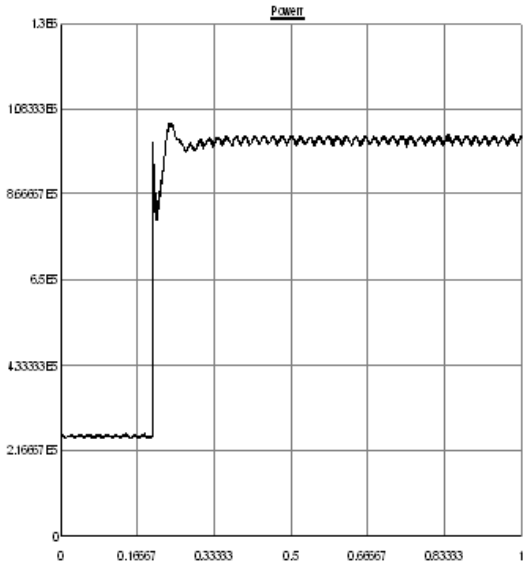

Figure 46. Power command increment of 0.2 pu to full load, W

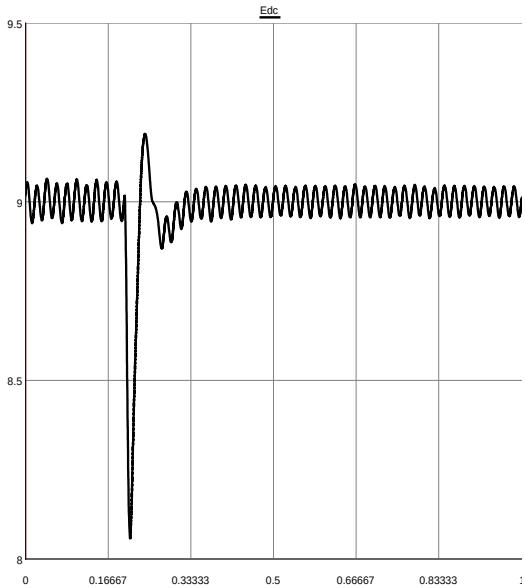

Figure 47. Terminal voltage, kV

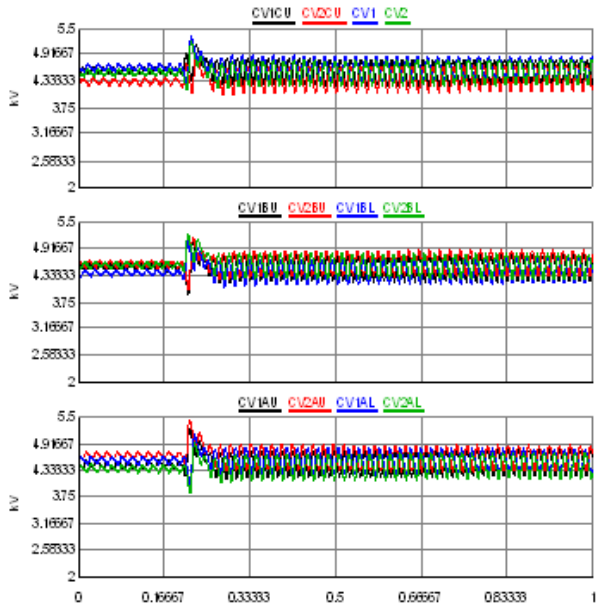

Figure 48. Sub-module capacitor voltages (kV)

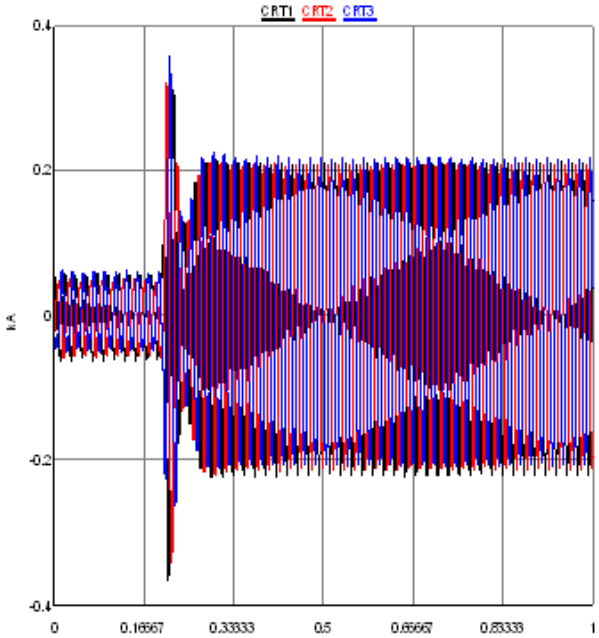

Figure 49. Grid side currents (kA)

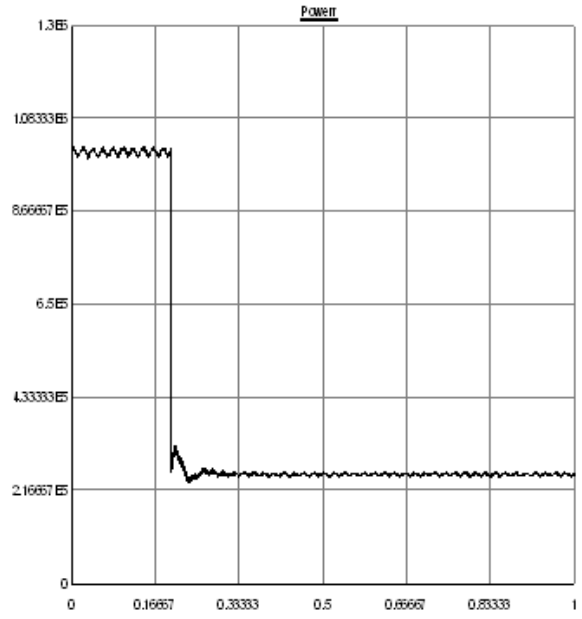

Figure 50. Power command decrement from full load to 0.2 pu, W

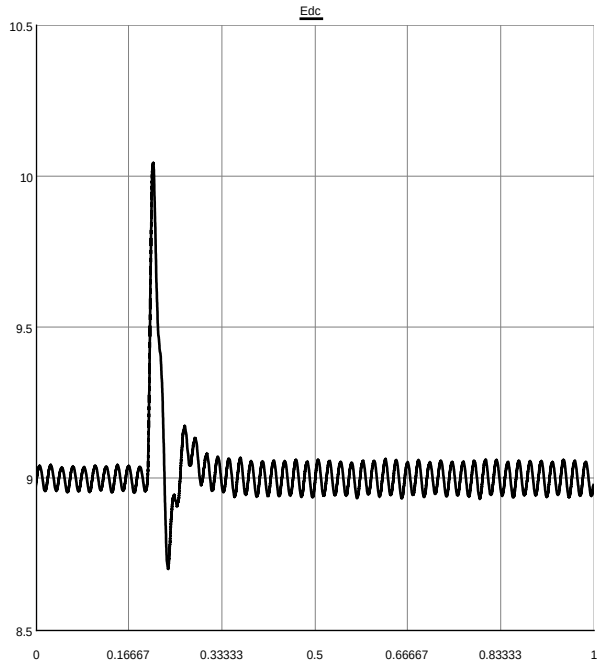

Figure 51. Terminal voltage, kV

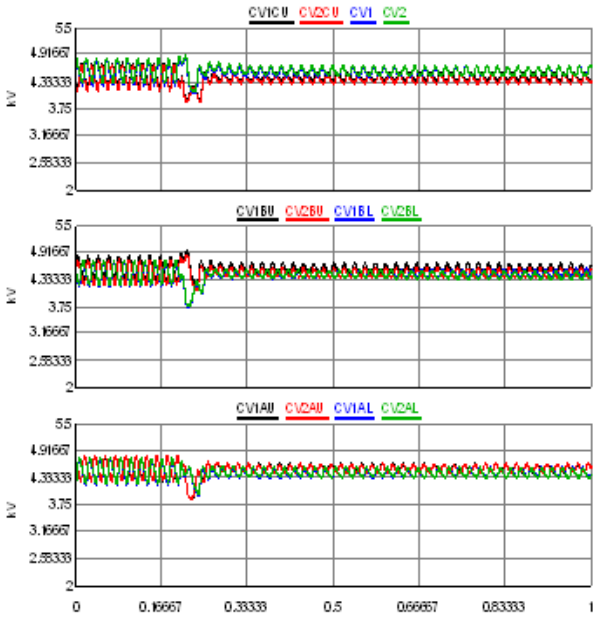

Figure 52. Sub-module capacitor voltages (kV)

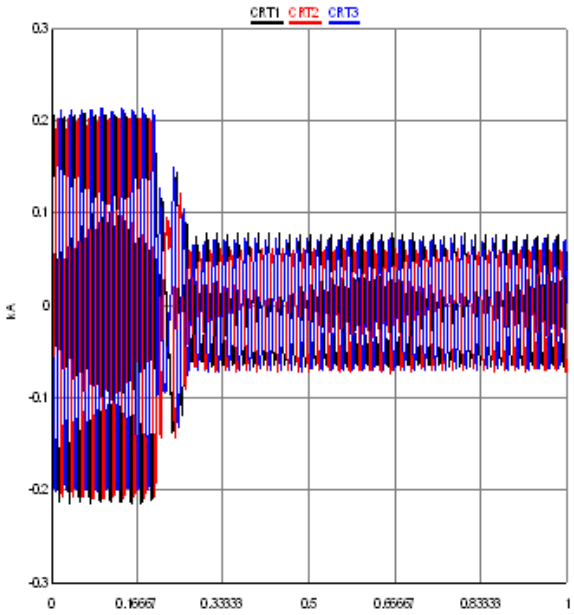

Figure 53. Grid currents (kA)

It is evident from Figure 41 that there is an unbalance in the grid currents in the three phases. Phase-C current magnitude is slightly higher in comparison with the other two. This is caused by an unbalance in the sub-module dc capacitor voltages which is a result of a lower number of sub-modules in each arm of the MMC (two in the above case). Figure 54 shows that similar controls with a higher number of sub-modules slightly improves the current unbalance when the number of sub-modules per arm is increased to four.

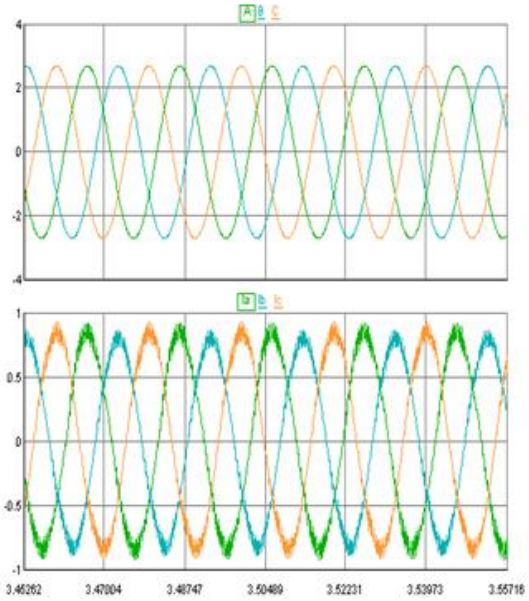

Figure 54. System steady-state operation: a) Grid voltages (kV); and b) Grid currents (kA)

However, it should be added that since these are just two data points, it is unlikely to be conclusive statement that this is an entirely number-of-sub-module dependent phenomenon and not a controls problem altogether.

4.2.3 L-G Fault Case Results

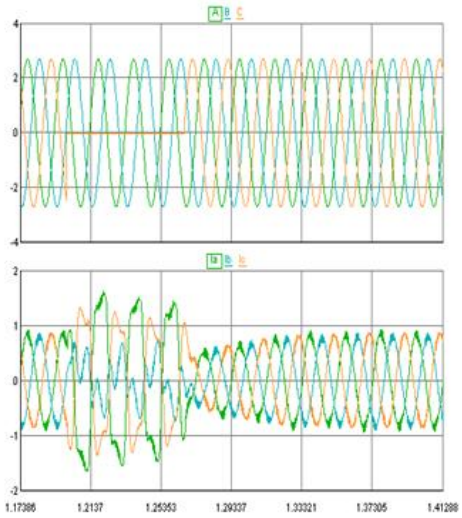

Figure 55. Single line-ground fault on Phase-A: a) Grid voltages (kV); and b) grid currents (pu)

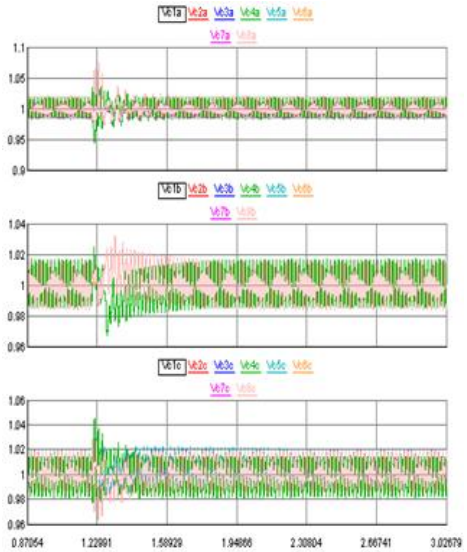

Figure 56. Sub-module capacitor voltages (pu)

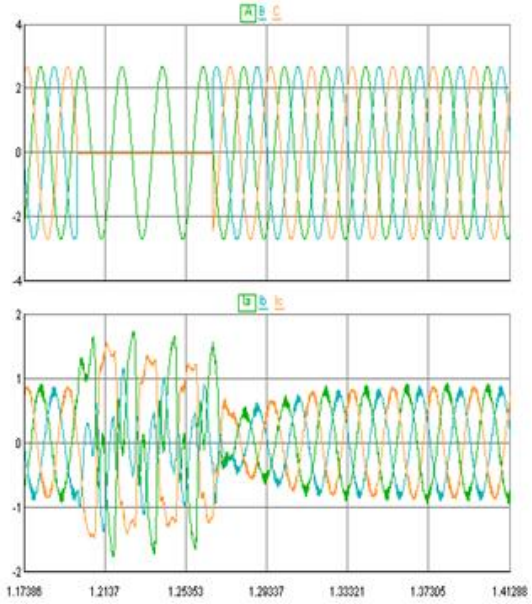

Figure 57. Line-line-ground fault on Phase-A and B: a) Grid voltages (kV); and b) grid currents (pu)

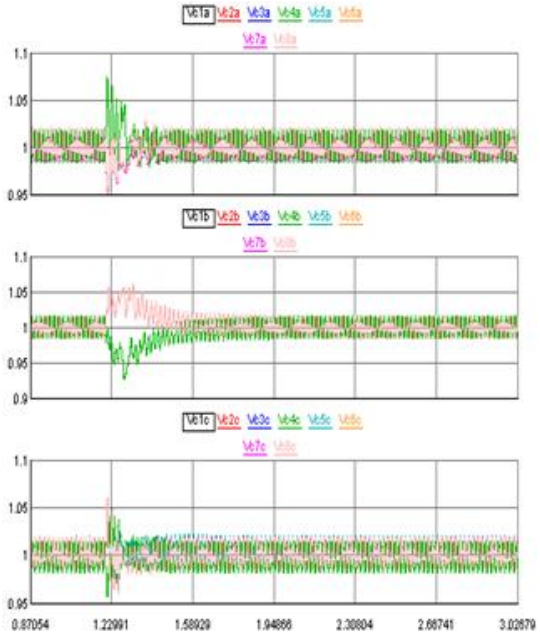

Figure 58. Sub-module capacitor voltages (pu)

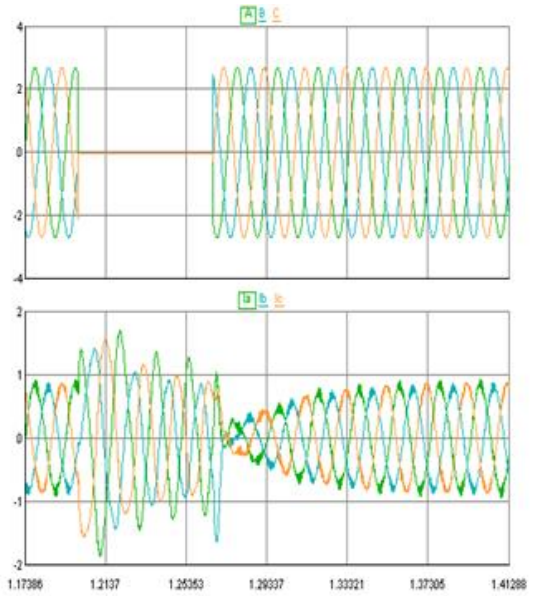

Figure 59. Line-line-line-ground fault: a) Grid voltages (kV); and b) grid currents (pu)

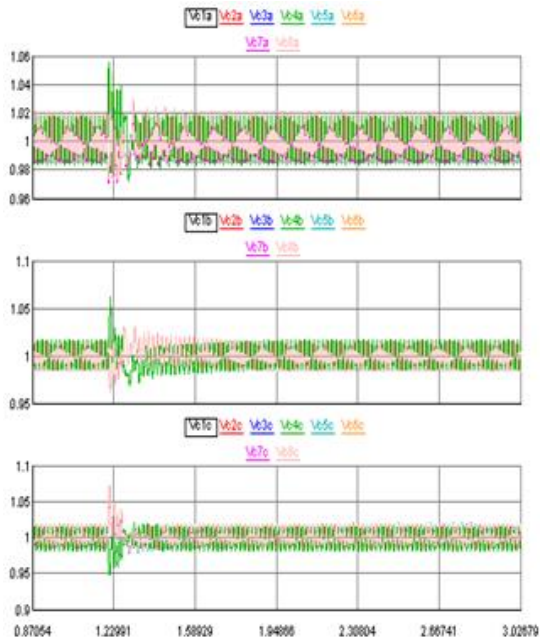

Figure 60. Sub-module capacitor voltages (pu)

Chapter 5: High Power Medium-voltage DC Amplifier System Based on MMC for Ship Board Power System Studies

5.1 Problem Background and Proposed Solution

In regard to MMC-based VSCs, there are several topologies that can be derived for specific applications. One such application is a dc amplifier system for ship-board power supplies. In this chapter, an MMC based high-power medium voltage DC amplifier is proposed. This amplifier system will provide a variable medium voltage dc bus with fast dynamic response. High power medium voltage DC amplifier system is required to validate new technologies like new high power non-linear loads based on power electronics, in all electric ships as part of the proposed medium voltage (MVDC) ship power system. Thyristor based medium voltage DC amplifier with series active inverter (SAI) in series with DC bus has been reported in the literature, where the series active Inverter compensates the slow dynamics of the thyristor converter and facilitates fast dynamic response. However, this system has disadvantages like cost of extra series active Inverter (SAI) in DC bus and cost of AC filter to provide reactive power support on the grid side. In general AC side filter rating will be about 40 to 50% of the thyristor converter rating.

This chapter proposes a new high power MMC-VSC (Voltage Source Converter) based DC amplifier system. This topology, apart from providing fast dynamic response, eliminates the series active filter in DC bus and AC filters on grid side of the converter and hence has savings on the cost, size and additionally reduces the complexity of the system.

The Office of Naval Research (ONR) in its Next Generation Integrated Power System (NGIPS) Technology Development Roadmap has envisioned an MVDC (Medium Voltage

Direct Current) power generation system anticipating increasing electric load requirements for combatant ships and submarines [48]-[50]. The need for such power systems will increase in the coming decades owing to increased propulsion and ship service power demands for future combatants armed with advanced sensors and weapons such as rail-guns and lasers [50]-[53].

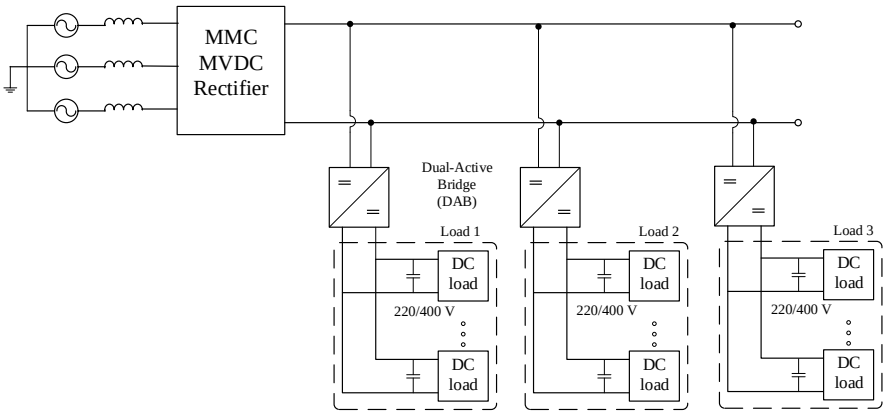

Figure 61. MMC MVDC test-bed

This shift from MVAC/HFAC system in favor of an MVDC supply system is attributed to factors such as decoupling prime mover speed from the frequency of the bus; enabling power conversion equipment operation at frequencies an order of magnitude higher than with the HFAC system, resulting in smaller transformers; reducing engineering concerns with respect to EMI and EMC; potential reduction in cable weight; increased ability to control fault currents to considerably lower levels than with AC systems; and paralleling of generators

without time critical phase matching amongst many others. However, the lack of design practices with respect to fault detection and isolation techniques; the implementation of design to overcome stability issues; standardized method establishment for controlling prime mover power and sharing loads between power generation modules; grounding strategies and a method for connecting to shore power are among the technical challenges that preclude an MVDC implementation of a shipboard MVDC system [50], [54].

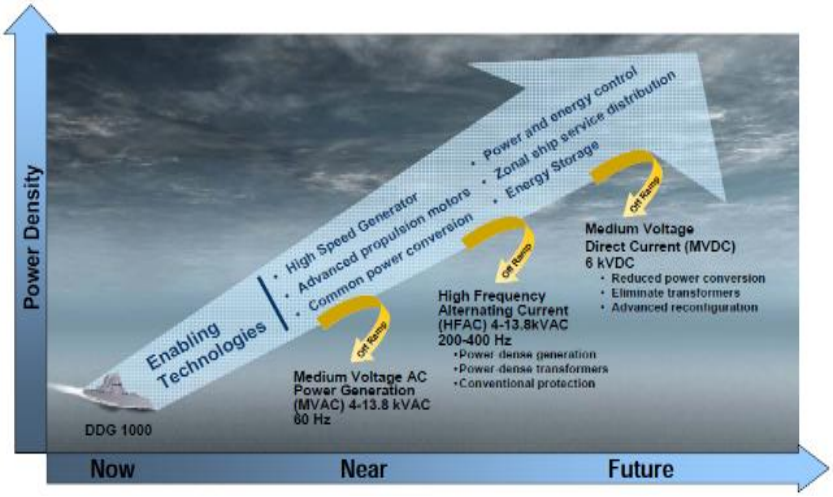

Figure 62. Next Generation Integrated Power System (NGIPS) Technology Development Roadmap [50]

In order to assist in de-risking the new MVDC technologies and developing new design practices, a test bed with sufficient experimental control capabilities is required. In particular, a highly controllable medium voltage dc bus must be generated. This can be done with a medium-voltage dc power amplifier system [50]. A conceptual MVDC system for meeting the requirements has been proposed before in [55]. It consists of a thyristor-based MVDC

amplifier system with an SAI meeting the steady state and dynamic performance. This paper proposes an alternative topology based on MMC converter [28] for MVDC amplifier system. This system apart from meeting the desired steady state conditions (Section 5.3) as well as dynamic performance over the proposed system in [55], saves significant amount of cost and size by eliminating series active Inverter in the DC bus and AC filters on grid side and it also reduces the electricity meter bill cost for the MVDC amplifier during testing with improved input power factor.

5.2 MVDC Amplifier Requirements

In order to test new megawatt range apparatus on surface ships and submarines, including loads as well as sources with different rating and developing new design practices for ship board power system, the desired steady state output voltage and current requirements are depicted in Figure 63 [56] and the desired dc bus dynamic response specification [55] are shown in Table 3.

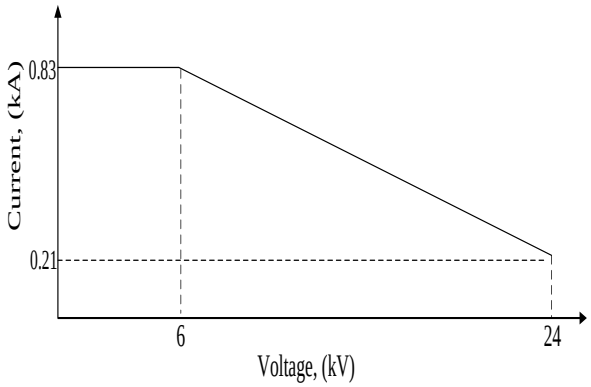

Figure 63. MVDC system steady-state voltage and current requirements [56]

Table 3. Dynamic dc bus specifications

Thyristor based MVDC amplifier specification with Series Active Inverter (SAI)		
Rise time and fall time	16 ms	0.3 pu step request
Recovery time after step load	13 ms	0.4 pu load change request
Voltage excursion after step load	0.32 pu	Maximum
Total DC voltage ripple $\|V_{RIPPLE-PP}\|/\|V_{DC}\|*100\%$	3%	Through entire DC output voltage range
Error of DC voltage component $\|V_{DC}- V_{DCREF}\|/\|V_{DCREF}\|*100\%$	<1.5%	Through entire DC output voltage range

In marine MVDC systems, there is a mega-watt scale active front-end (AFE) rectifier which converts the ac power generated by synchronous generators to medium-voltage dc power [49], [50]. This active front-end rectifier being the main source of the dc-bus is usually based on Insulated-Gate Bipolar-Transistor (IGBT) or Insulated-Gate-Commutated-Thyristor (IGCT) power semiconductor technologies. At such high power medium-voltage dc application two level and three level converters (diode clamped and Neutral Point Clamped (NPC) topologies based on IGBT/IGCTs cannot support several kHz switching frequency due to power loss limitations and hence resulting low bandwidth characteristic of a few hundred Hz. Furthermore, as ships become more and more electric, loads onboard are becoming more energy demanding for a given energy consumption. High power active dc loads of very varying and non-linear nature like electromagnetic launchers, rail guns, and high power radars are expected in increasing number onboard combatant ships [52], [53].

The combination of low front-end converter bandwidth and these new types of loads is expected to create stability challenges with regard to medium-voltage dc link [50].

To design an MVDC test bed with mega-watt scale, an MVDC amplifier was proposed based on thyristor converter and high bandwidth SAI at DC side to meet steady state requirements and dynamic response respectively [55]. But it has disadvantages including cost burden of the SAI; poor input power factor at low dc bus voltages (as firing angle is low); and cost of the AC side filter. This paper proposes an alternative MVDC amplifier system based on an MMC-VSC converter. To validate the MMC converter for MVDC amplifier, a 2 MW MMC system with circuit parameter (Table 4) was used for simulation in PSCAD and RTDS.

Table 4. MMC MVDC rating for analysis and simulation

Line to Line RMS voltage	4kV
Rated power	2MW
DC link voltage	7 to 12kV
Module DC capacitor	500μF
Valve arm reactor	10mH (0.15pu)
AC side source inductance	31.3μH
Switching frequency	950Hz

The MMC topology and controls are similar to those derived in Chapter 3.

5.3 Performance Results (MMC versus Thyristor-based MVDC Amplifier)

The simulations were carried out in EMTDC/PSCAD and RTDS for analyzing the dynamic performance of the MVDC amplifier system based on a MMC-VSC based front-end

technology. The system in RTDS, initially, is delivering 1.33 MW at 9 kV DC, thereafter at *t*=26 s the reference voltage is increased to 10.5 kV (0.3 pu increase, with 5kV as 1.0 pu) with the system delivering 1.83MW. At *t*=28 s the output power demanded by the load is decreased to 0.9 MW and subsequently at *t*=29 s the output power demand is again increased to 1.833 MW. The dynamic response results from PSCAD/EMTDC are shown in Figure 64-70. Sub-module dc capacitor voltage balancing and input unity power factor operation of MMC converter are shown in Fig. 71 and 72.

Table 5. Dynamic performance specifications of Thyristor-based [48], and MMC-based MVDC amplifier

	MMC VSC-based MVDC amplifier specs	**Thyristor-based MVDC amplifier specs with SAI**	
Rise time and fall time	< 15ms	16 ms	0.3 pu step voltage request
Recovery time after step load	20ms	13 ms	0.4 pu load change request
Voltage excursion after step load	0.1pu	0.32 pu	Maximum
Total DC voltage ripple $\lvert V_{RIPPLE\text{-}PP}\rvert/\lvert V_{DC}\rvert*100\%$	< 0.1%	3%	Through entire DC output range
DC voltage error $\lvert V_{DC}-V_{DCREF}\rvert/\lvert V_{DCREF}\rvert*100\%$	< 0.1%	<1.5%	Through entire DC output range

The results from Table 5 illustrate that, MMC VSC-based MVDC amplifier has superior dynamic performance than a thyristor-based MVDC amplifier [38]. Though the recovery time for step change in load is little more in MMC MVDC amplifier, the peak overshoot and undershoots are significantly lesser in comparison and hence at high power loads see an almost constant DC bus.

5.3.1 MVDC Amplifier Results in PSCAD/EMTDC

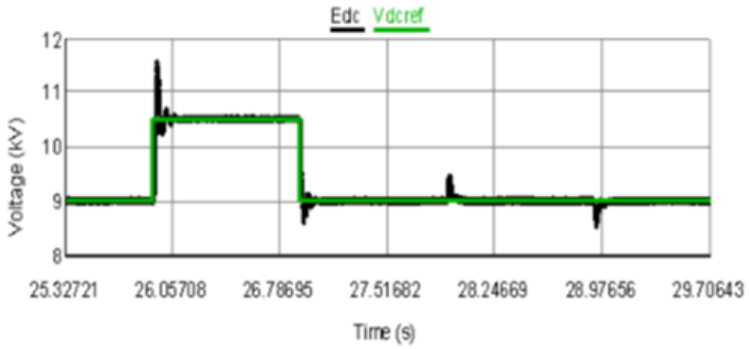

Figure 64. Dynamics of output voltage versus reference dc bus

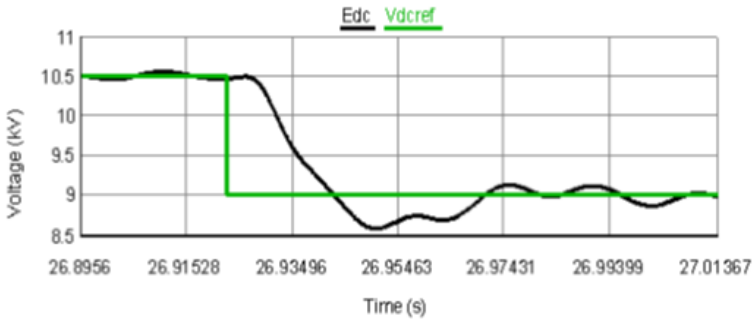

Figure 65. Dynamics of dc bus for a 0.3pu step-down in reference voltage and a 35% reduction in power

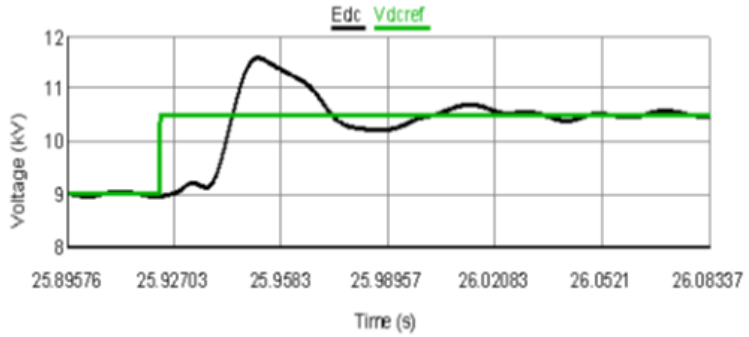

Figure 66. Dynamics of dc bus for a 0.3pu step-up in reference voltage and a 35% increase in power

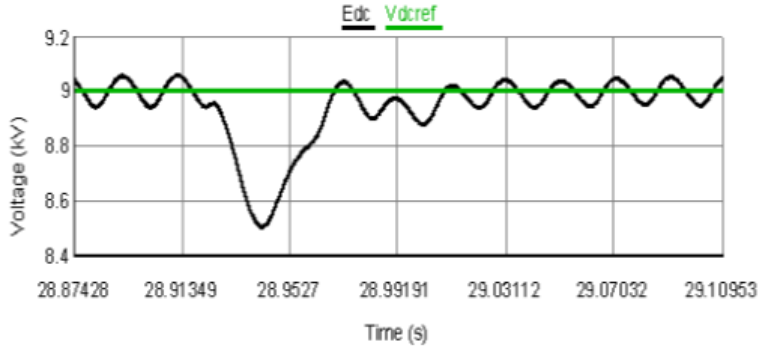

Figure 67. Dynamics of dc bus voltage for a 50% reduction in load

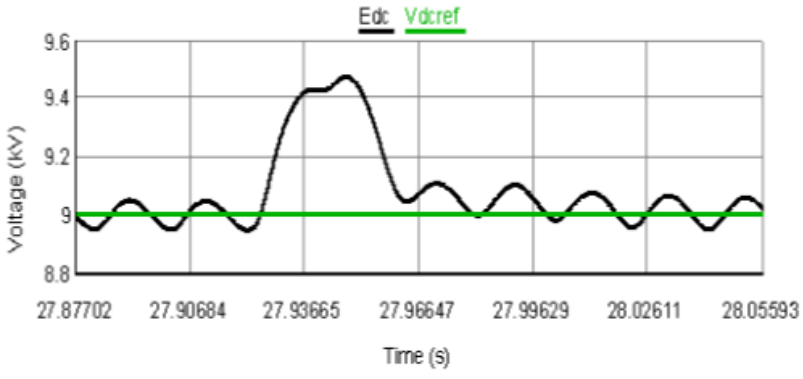

Figure 68. Dynamics of dc bus voltage for a 50% increase in load

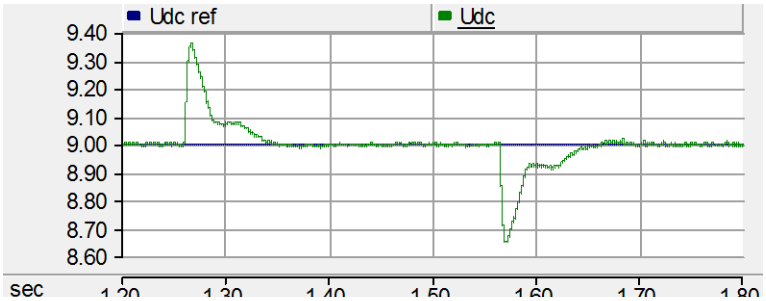

Figure 69. Dynamic response of dc bus for a 0.5 pu change in load

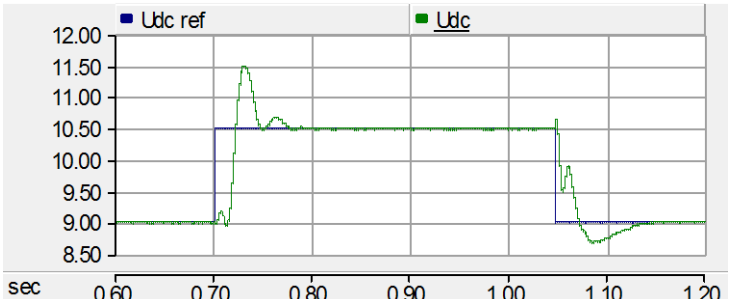

Figure 70. Dynamic response of dc bus for a step change in voltage

5.3.2 System Performance Results in RTDS

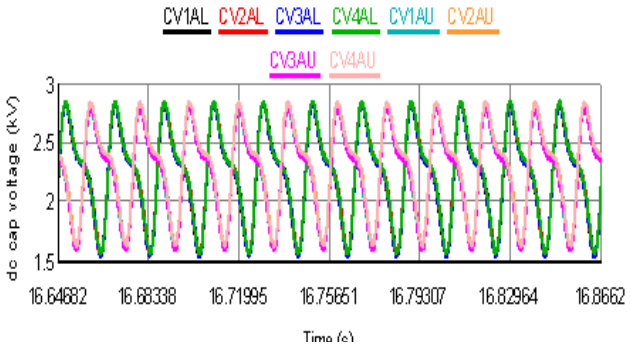

Figure 71. Sub-module capacitor voltages

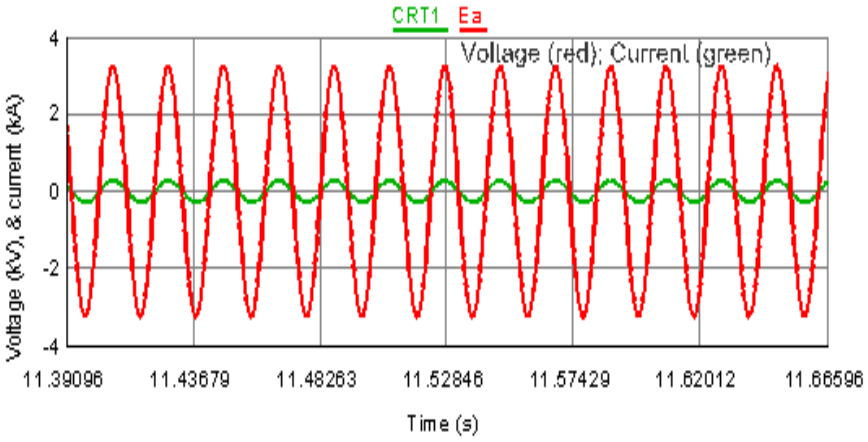

Figure 72. Unity power factor operation of the MMC VSC

It is evident from the results that the MMC-VSC is a cost effective alternative topology that can be used as MVDC amplifier test-bed for studying the ship-board power supply system [38]. System advantages include superior dynamic performance, operation at unity power factor along with elimination of the series active inverter and AC filters on the grid side.

Chapter 6 Resilient Multi-terminal Networks with High-voltage High-frequency Electronics

6.1 Introduction

This chapter focuses on the implementation of a two terminal HVDC network. Here each HVDC terminal connects to the AC voltage source through HVDC converter which will be discussed in the section 6.2. The converter discussed here is different from that in chapter 3 on two basis. One, that it is a full bridge modular converter, or cascaded H-bridge converter as discussed in [19]. And second, that it employs series resonant converters (SRC) to step up the terminal voltage and additionally providing isolation for the full bridge-converter sub-modules in case of a dc fault.

Most of the control issues faced here were similar to that of MMC VSCs; however, additional control loops were required because of the SRC converters in the circuit. An average model of the SRC converter was used because two reasons. One, hardware limitations in RTDS. This is because RTDS simulates every electrical node in each time step for associated signals, and since it is real-time so the computation is limited by the number of electrical nodes that can be simulated on it. A major chunk of memory allocation of the processor cards was assigned to the system modeling and only an average model could be simulated with the switched model of the H-bridge VSC. Second, the switching frequency limits for RTDS small-time step simulation blocks is close to 4 kHz [47]. This frequency is not sufficient for a switched SRC model; however, an averaged SRC model performs satisfactorily in RTDS. This was confirmed by the comparison of the system simulation

results in PSCAD/EMTDC, where switching model and also averaged model was implemented, with that of RTDS results.

6.2 HVDC Converter Station and Specifications

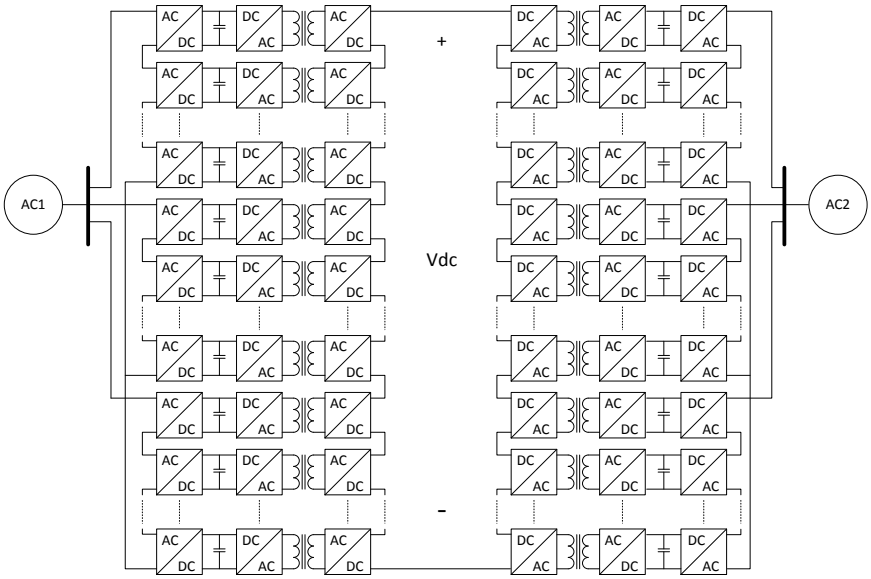

Figure 73. Two-terminal HVDC system structure

Figure 73 depicts the entire system configuration. The HVDC converter is based on stacking of single phase ac/dc power sub-modules in series. The input and output terminals in power conversion are isolated by a high-frequency transformer.

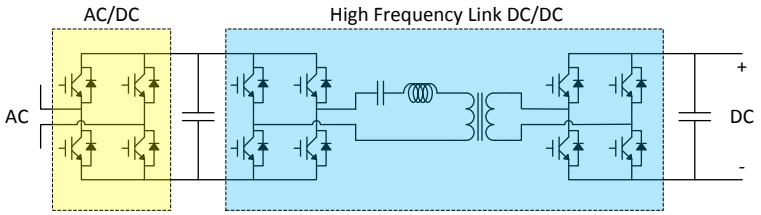

Figure 74. Power conversion sub-module with high-frequency dc-dc converter

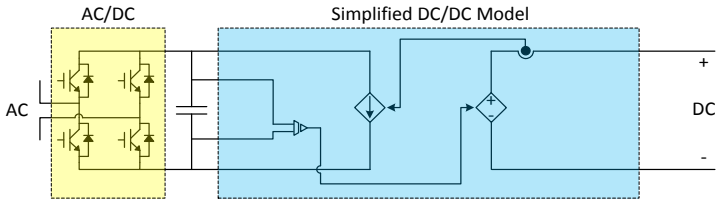

Figure 75. Power conversion sub-module with simplified dc-dc converter model

Every power conversion sub-module consists of two stages; ac/dc converter sub-module and high-frequency link dc-dc converter as shown in Figure 74. For the average model implementation, the simplified structure with employed which used one dependent current source and one dependent voltage source as shown in Figure 75.

Table 6. System parameters

Total sub-modules (per phase)	9 EA (3EA)
Module DC capacitor voltage	1 kV
Module rated power (Total)	1 MVA (9MVA)
AC/DC converter PWM switching frequency	540 Hz
AC input voltage	3.182 kV (line-line RMS) / 2.6 kV(phase peak)
AC input impedance (inductance)	328uH (11%)
AC input impedance (resistance)	11mΩ (1%)

6.3 System Controls

The controls employed here are similar to those discussed in section 3.2 and 3.3. The extra features are discussed here.

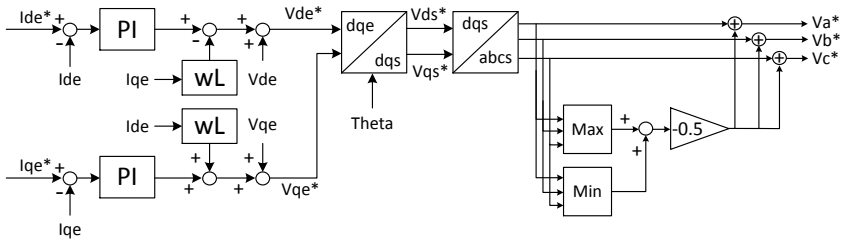

Figure 76. Current control block

Figure 76 shows the current controller in detail. The grid angle is detected by a PLL based only on the positive sequence voltages, as shown in Figure 77.

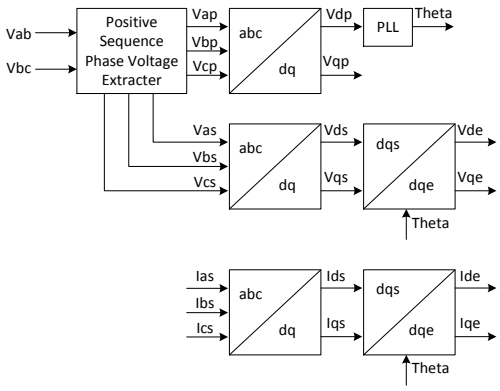

Figure 77. Grid angle detection and feed-forward voltage

However, the feed-forward voltage is calculated with the measured voltage which means the sum of the positive sequence voltage and the negative sequence voltage. The conventional PI control in the synchronous reference frame was used. To implement the SVPWM, the min-max method was used. The output of ac Current Controller is used for the reference voltage of the every ac/dc converter sub-module. Before using these output voltages as reference voltages of ac/dc converter sub-module, the voltage balancing between capacitor voltages of all ac-dc converters should be considered. The scheme followed here is similar; however additional phase-balancing loops are added for added balancing features. These features are briefly discussed hereafter.

Since the HVDC converter in this system is operated with the floating capacitors of ac-dc converter sub-modules, the voltage balancing of these capacitors is very important. This HVDC converter should have three different voltage control functions. First, the HVDC converter has to control the sum of the entire capacitor voltage as the terminal voltage. This terminal voltage is used as dc voltage in the dc grid. This terminal voltage control is already achieved through Terminal Voltage Controller which is discussed in section 3.3.3. Second, the sums of each phase floating capacitor voltages should be balanced with those of other phase floating capacitor voltages. If every phase has three power conversion sub-modules like the ones in Figure 74, the sum of three capacitor voltages of a-phase ac-dc converters should be balanced with those of b-phase and c-phase ac-dc converters. Third, the capacitor voltages in same phase should be balanced. That means that three series connected floating capacitor voltages in a-phase should be balanced with each other. Hereafter, the second

voltage balancing issue is called as the phase voltage balancing and the third voltage balancing one is called as module voltage balancing.

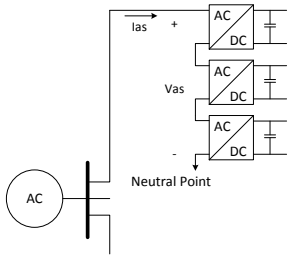

Figure 78. A-phase ac-dc converter configuration of an HVDC terminal

The phase voltage balancing can be achieved by controlling the common mode voltage. A phase power can be calculated by multiplication of phase voltage and phase current as (52). The phase voltage and current can be illustrated as Figure 78. When the phase voltage and current can be expressed as (53)-(55), the phase power can be rewritten as (56)-(58).

$$P_a = V_a I_a \tag{52}$$

$$V_a = V_s \cos(\omega t) \qquad I_a = I_s \cos(\omega t + \phi) \tag{53}$$

$$V_b = V_s \cos\left(\omega t - \frac{2\pi}{3}\right) \qquad I_b = I_s \cos\left(\omega t - \frac{2\pi}{3} + \phi\right) \tag{54}$$

$$V_c = V_s \cos\left(\omega t + \frac{2\pi}{3}\right) \qquad I_c = I_s \cos\left(\omega t + \frac{2\pi}{3} + \phi\right) \tag{55}$$

$$P_a = \frac{1}{2} V_s I_s \cos\phi + \frac{1}{2} V_s I_s \cos(2\omega t + \phi) \tag{56}$$

$$P_b = \frac{1}{2} V_s I_s \cos\phi + \frac{1}{2} V_s I_s \cos\left(2\omega t + \frac{2\pi}{3} + \phi\right) \tag{57}$$

$$P_c = \frac{1}{2}V_s I_s \cos\phi + \frac{1}{2}V_s I_s \cos\left(2\omega t - \frac{2\pi}{3} + \phi\right) \quad (58)$$

If the common mode voltage is added into all three voltage reference, the phase power varies by the common mode voltage. When the common mode voltage is like (59), the phase power can be rewritten as (60)-(62). Since this common mode voltage will be used for phase voltage balancing, this voltage in (59) is notated as V_{pb}.

$$V_{pb} = V_{cm}\cos(\omega t + \varphi) \quad (59)$$

$$P_a' = P_a + \frac{1}{2}V_{cm}I_s \cos(\varphi - \phi) + \frac{1}{2}V_{cm}I_s \cos(2\omega t + \varphi + \phi) \quad (60)$$

$$P_b' = P_b + \frac{1}{2}V_{cm}I_s \cos\left(\varphi - \phi + \frac{2\pi}{3}\right) + \frac{1}{2}V_{cm}I_s \cos\left(2\omega t + \varphi + \phi - \frac{2\pi}{3}\right) \quad (61)$$

$$P_c' = P_c + \frac{1}{2}V_{cm}I_s \cos\left(\varphi - \phi - \frac{2\pi}{3}\right) + \frac{1}{2}V_{cm}I_s \cos\left(2\omega t + \varphi + \phi + \frac{2\pi}{3}\right) \quad (62)$$

Each phase power has an average power and a high frequency power of which frequency is two times the fundamental frequency. The average power of each phase power can be written as (63)-(65).

$$P_{aavg}' = \frac{1}{2}V_s I_s \cos\phi + \frac{1}{2}V_{cm}I_s \cos(\varphi - \phi) \quad (63)$$

$$P_{bavg}' = \frac{1}{2}V_s I_s \cos\phi + \frac{1}{2}V_{cm}I_s \cos\left(\varphi - \phi + \frac{2\pi}{3}\right) \quad (64)$$

$$P_{cavg}' = \frac{1}{2}V_s I_s \cos\phi + \frac{1}{2}V_{cm}I_s \cos\left(\varphi - \phi - \frac{2\pi}{3}\right) \quad (65)$$

The average power of each phase power can be controlled by adjusting the magnitude of the common mode voltage V_{cm} and the phase φ. The frequency of this common mode voltage is the fundamental frequency. Figure 79 shows the HVDC converter in the view of the phase power.

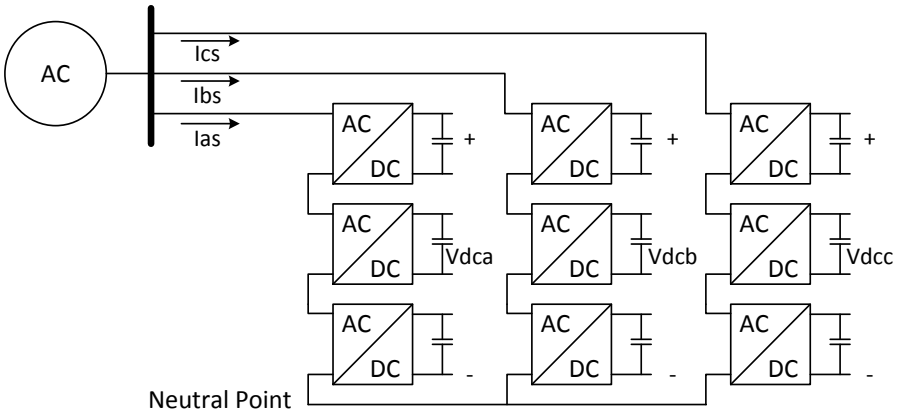

Figure 79. HVDC converter with phase voltages and currents

The average power of each phase power with the common-mode voltage can be written in the stationary d-/q-axis reference frame.

$$\begin{bmatrix} P'_{davg} \\ P'_{qavg} \end{bmatrix} = \frac{1}{2} V_{cm} I_s \begin{bmatrix} \cos(\varphi - \phi) \\ \sin(\varphi - \phi) \end{bmatrix} \tag{66}$$

Meanwhile, the phase voltage unbalance can be analyzed with the energy unbalance between the phase capacitors. The energy unbalance in three phase capacitor can be written with the phase voltage variation as (67). This three phase energy unbalance can be expressed in the stationary *d-q* axis reference frame as (68).

$$\begin{bmatrix} \Delta J_{aavg} \\ \Delta J_{bavg} \\ \Delta J_{cavg} \end{bmatrix} \approx C_p V_{pavg} \begin{bmatrix} \Delta V_{aavg} \\ \Delta V_{bavg} \\ \Delta V_{cavg} \end{bmatrix} \tag{67}$$

$$\begin{bmatrix} \Delta J_{davg} \\ \Delta J_{qavg} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \Delta J_{aavg} \\ \Delta J_{bavg} \\ \Delta J_{cavg} \end{bmatrix} \tag{68}$$

$$\begin{bmatrix} P^*_{dpavg} \\ P^*_{qpavg} \end{bmatrix} = \frac{K_p s + K_i}{s} \begin{bmatrix} -\Delta J_{davg} \\ -\Delta J_{qavg} \end{bmatrix} \tag{69}$$

$$V_{pb} = \cos(\omega t + \phi^*)\, P^*_{dpavg} - \sin(\omega t + \phi^*)\, P^*_{qpavg} \tag{70}$$

This *d-q* axis energy variation can be compensated by the added phase power by common-mode voltage. To balance the phase energy variation, the phase energy variation should be controlled as zero. The average phase voltage should be calculated. Figure 80 shows how to obtain the average phase voltage and how to balance these average phase voltages. The *d-q* axis phase voltage variation is multiplied with effective phase capacitor and the average of the three phase voltages. These calculated values can be expected as the *d-q* axis energy variation. These energy variations are feed to the PI controller. The outputs of the PI controller should be the added power reference to compensate the energy variation as (69). This added power can be achieved with the common mode voltage as (66). So, the *d-q* axis power references are transformed to the stationary common-mode voltage like (70).

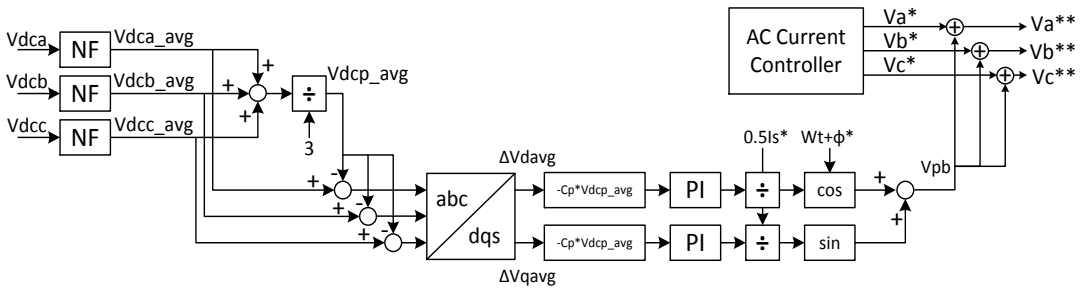

Figure 80. Phase-voltage balancing control

The individual sub-module balancing controls are derived from section 3.2.

A note about the sub-module capacitance values

As discussed in section 4.1.2, the capacitance of the sub-module is a critical parameter of the system. The voltage variation equation with respect to the capacitance value is given by (50). Figure 81 shows the peak to peak voltage variation according to the capacitance in the case of Table 6. When the capacitance is 10mF, the voltage variation of AC/DC converter is about peak to peak 300V at the full load condition.

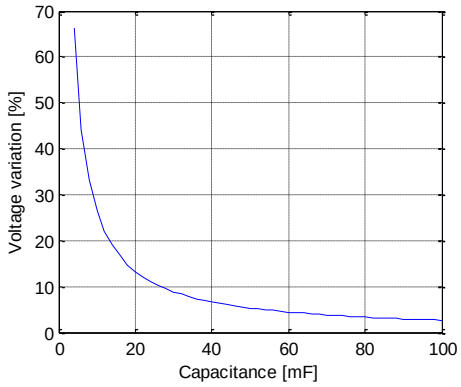

Figure 81. Sub-module output voltage ripple with respect to sub-module capacitance

6.4 DC Fault Detection and Recovery

A VSC based HVDC transmission system is vulnerable to DC side fault, but the VSC based HVDC system configuration considered in this chapter has the feature to be protected against DC fault with the appropriate control algorithm without using DC circuit breakers. In fact, this advantage allows us to use AC circuit breakers instead of DC circuit breakers for DC fault protection. The proposed control algorithm of VSC based HVDC transmission system for DC fault operation is shown in Figure 82.

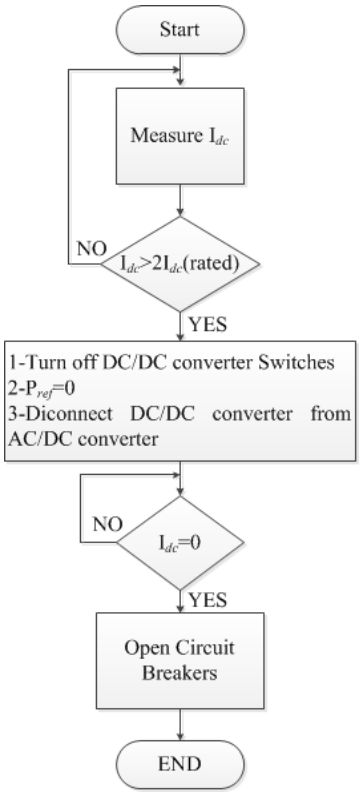

Figure 82. Controller sequence for VSC HVDC system operation under dc fault condition

According to the control scheme for DC fault operation (Figure 82), DC fault is detected when the measured value of DC side current is twice the rated value of DC side current. Once DC fault is detected at time t_0, the reference value of active power flow is changed to zero. Also, once fault is detected, all switches of DC/DC converters are turned off, and DC/DC converters are disconnected from AC/DC converters. As a result, the total energy of all DC capacitor voltages is discharged in DC side inductor *(L)* and cable resistance *(R)* as can be shown in Figure 83.

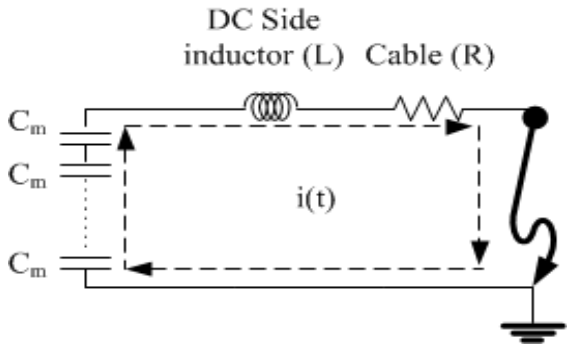

Figure 83. Equivalent circuit of VSC based HVDC transmission system when dc fault is detected (sub-module capacitor discharge mode)

The control strategy for recovery after dc fault is shown in Figure 84. When dc fault is cleared, dc-dc converters are connected to ac-dc converter, and all switching signals of dc-dc converters are enabled to charge dc-dc capacitor voltages. Once dc bus voltage is regulated at its reference value, terminal 1 is connected to terminal 2, and the reference value of active power flow is ramped up from zero to the rated value.

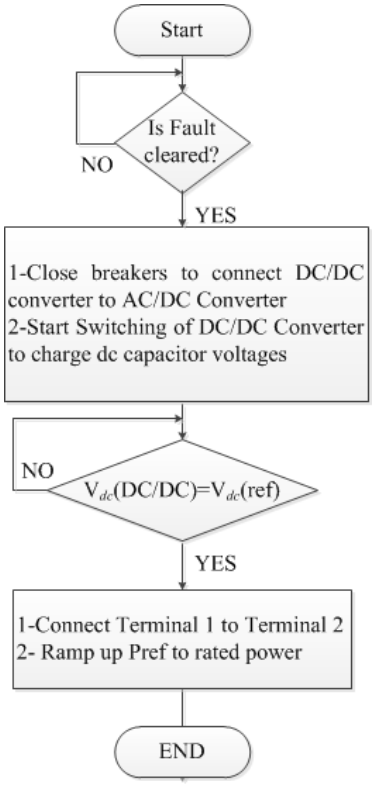

Figure 84. Controller sequence for VSC HVDC system recovery after dc fault

6.5 RTDS Simulation Results

To verify the controls the back-to-back system was simulated in RTDS. Similar to the MMC case in chapter 4, in the beginning, all the power sub-modules are blocked till the sub-module capacitors charge through the IGBT anti-parallel diodes (Figure 9). Once charged and the terminal voltage stabilized, the sub-modules are de-blocked and the controller comes into picture. Up till here the power transfer reference is still zero. The dc breaker is turned on after the sub-module capacitor voltages settle at the reference value. Now, power can be ramped up or down as desired.

Results from three cases are discussed here:

6.5.1 Steady-state Power Transfer

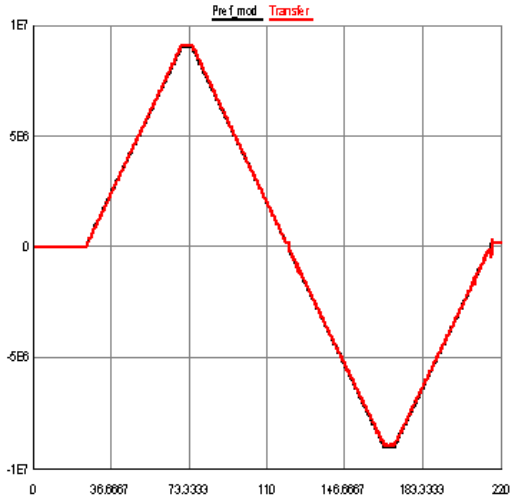

Figure 85. Power reference following from +9 MW to -9 MW

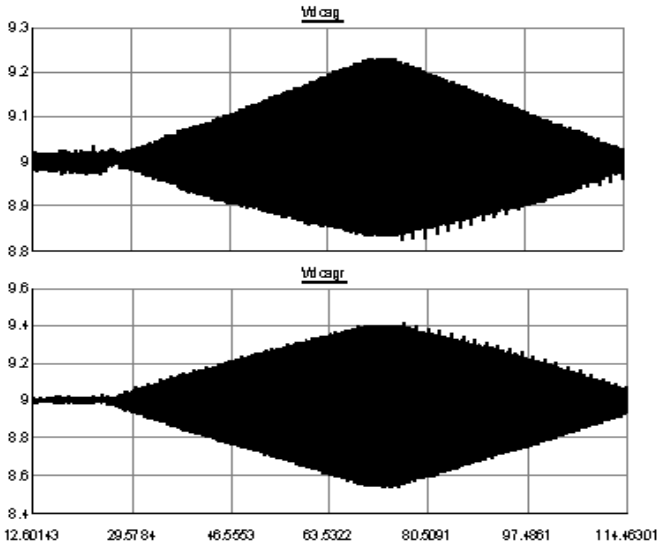

Figure 86. Terminal voltages, kV (receiving end on top)

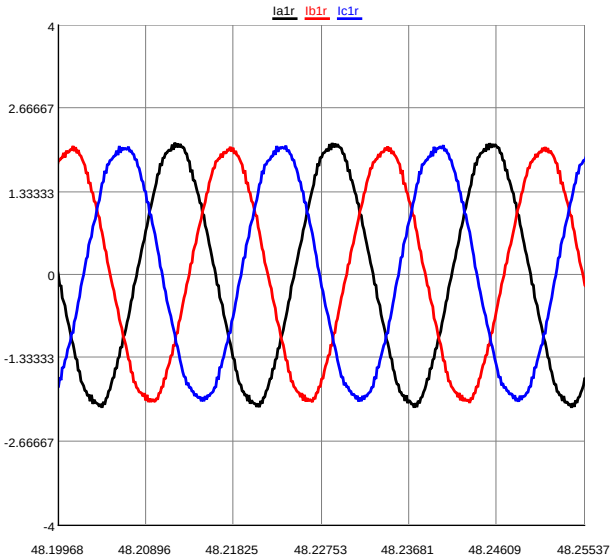

Figure 87. Sending end grid currents (kA)

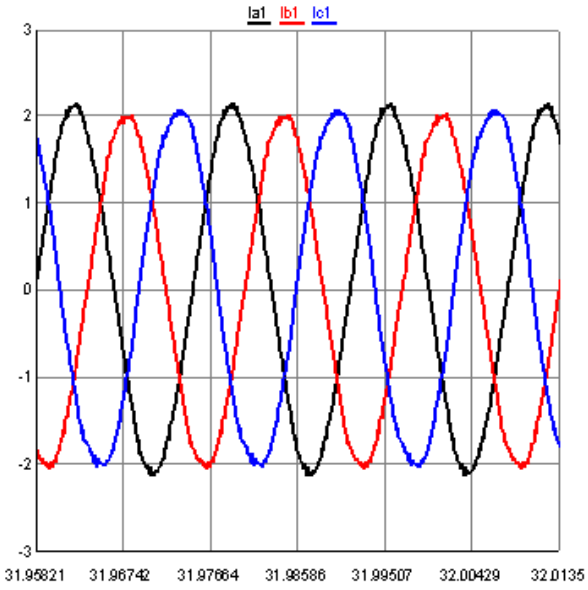

Figure 88. Receiving end grid currents (kA)

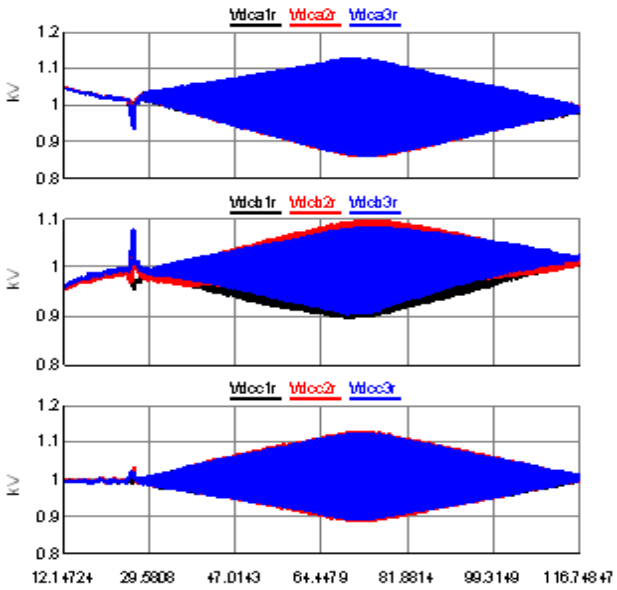

Figure 89. Sending end sub-module capacitor voltages

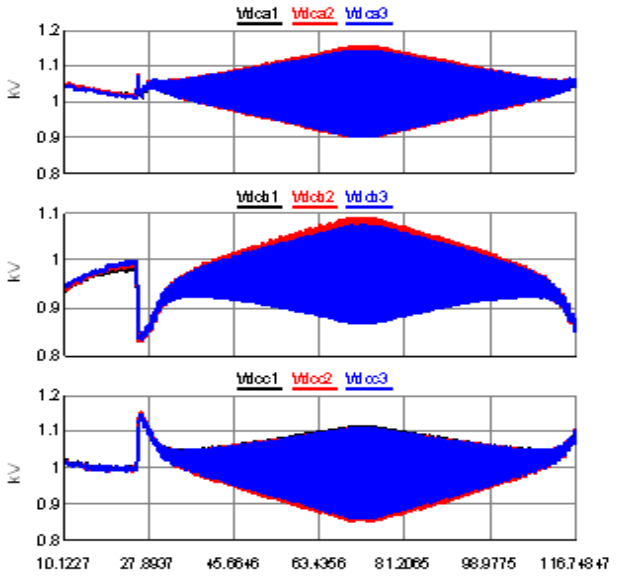

Figure 90. Receiving end sub-module capacitor voltages

6.5.2 Single Line-ground Fault

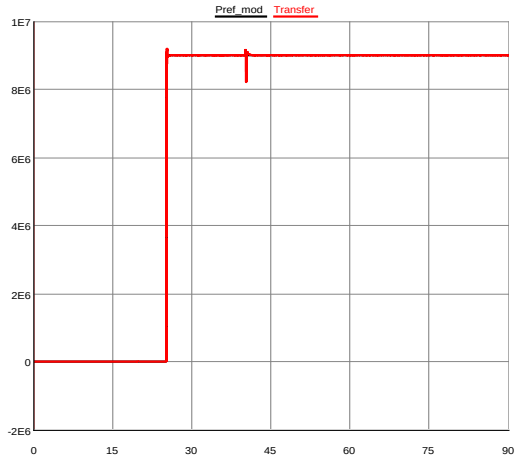

Figure 91. Power reference following from +9 MW under SLG fault

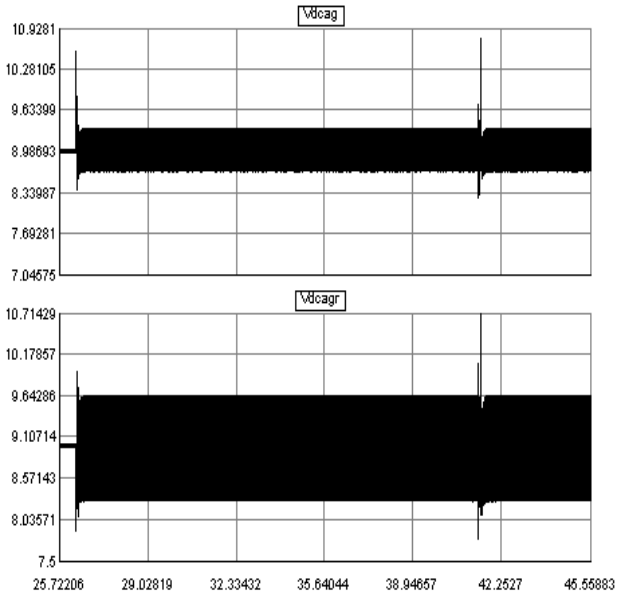

Figure 92. Terminal voltages, kV (receiving end on top)

6.5.3 DC Line-ground Fault and Recovery

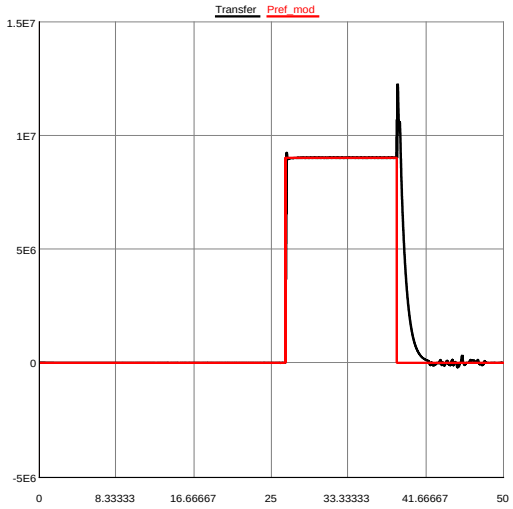

Figure 93. Power transfer with a dc fault lasting 100 ms, W

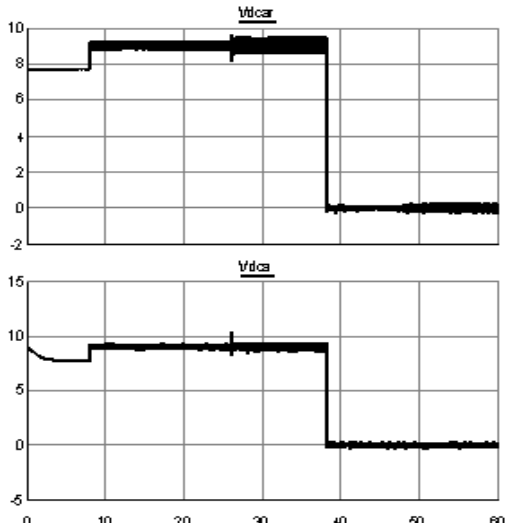

Figure 94. Terminal dc bus voltages, kV (sending end on top)

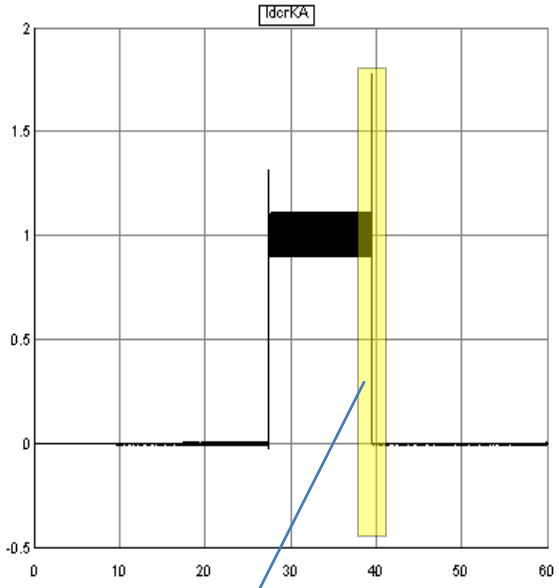

Figure 95. DC current, kA

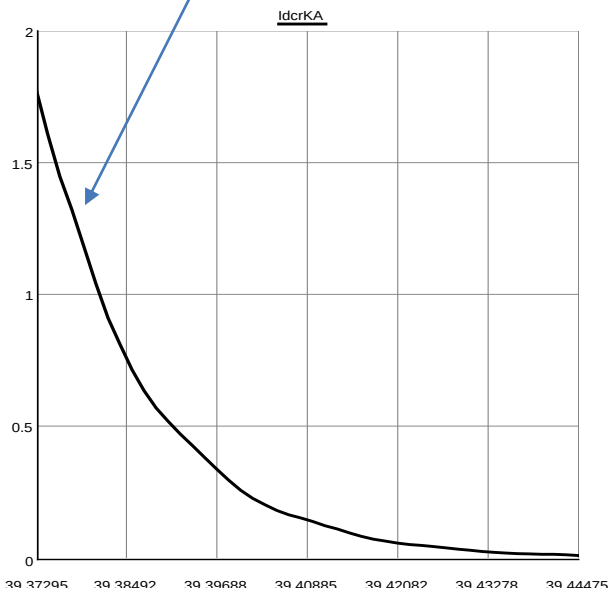

Figure 96. DC current (in kA) zero-crossing time (70 ms)

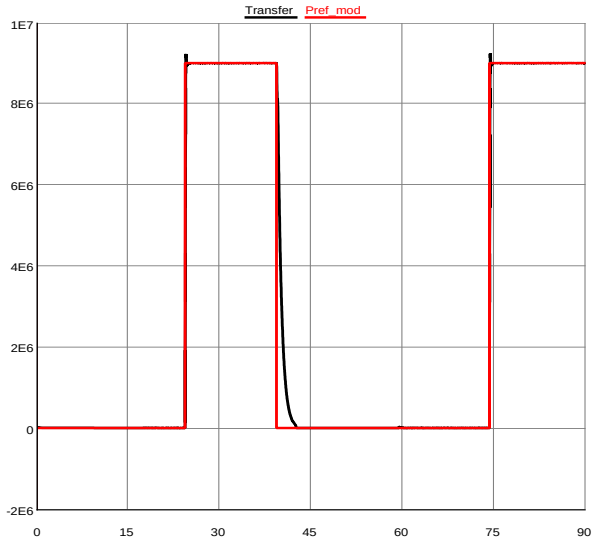

Figure 97. Power transfer curve during fault recovery, W. (See section 6.4)

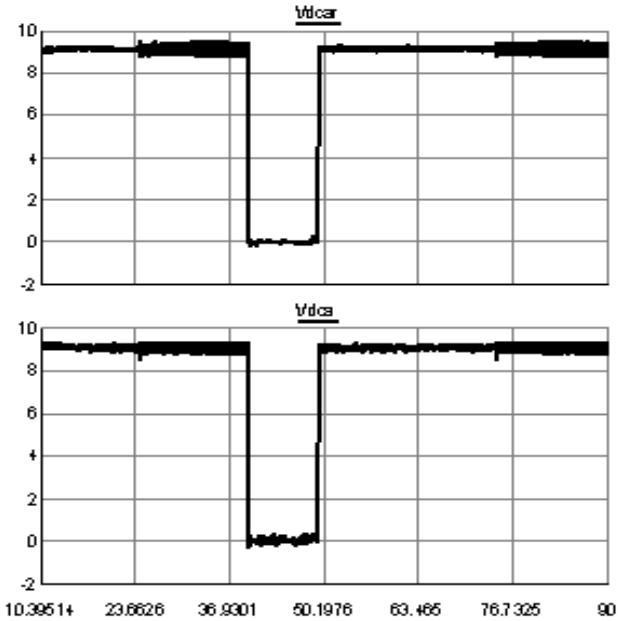

Figure 98. Terminal voltages during fault-recovery period, kV (Receiving end on top)

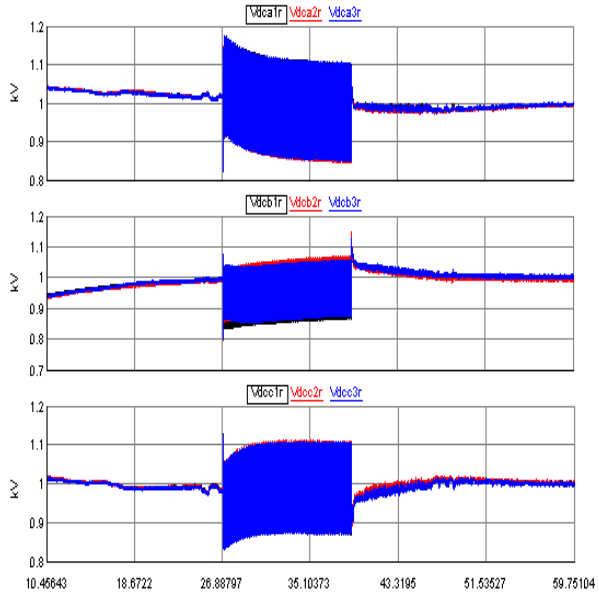

Figure 99. Sub-module capacitor voltages (sending end)

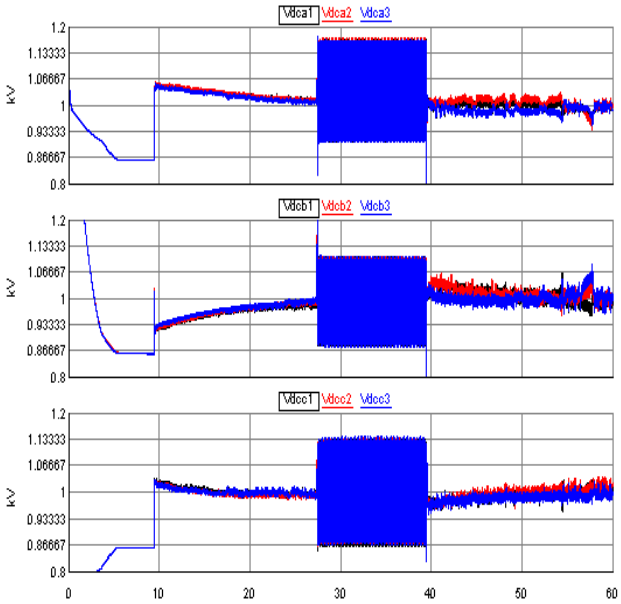

Figure 100. Sub-module capacitor voltages during fault-recovery period (sending end)

Chapter 7: MMC Hardware-in-loop (HIL) Implementation

The MMC converter system was implemented in HIL with a Xilinx Virtex5 ML507 board. The interface between the Xilinx board and RTDS was written in VHDL employing a GTFPGA card from RTDS [47].

The RTDS interface module for the ML507 FPGA provided an interface to the RTDS for controller implementation outside RTDS. The structure of the interface is in Figure 100.

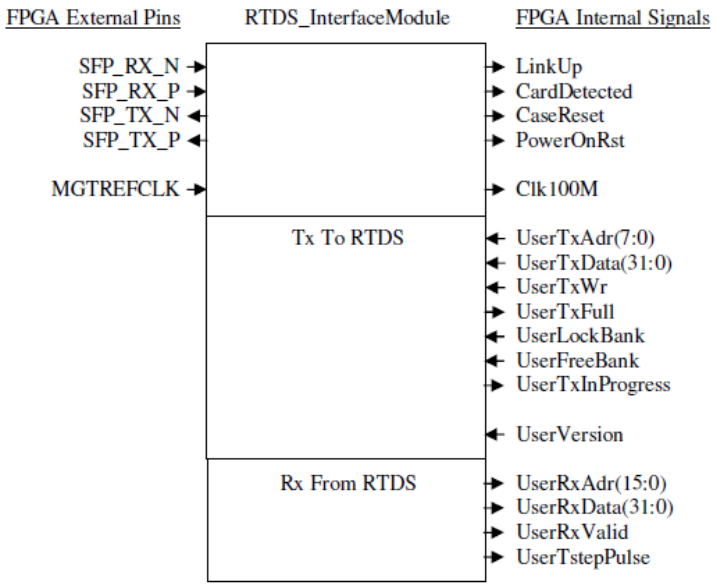

Figure 101. RTDS, Xilinx Virtex 5 ML507 interface structure [47]

The Data received from the RTDS is presented on a 32-bit data bus together with a 16-bit address bus. A time step synchronization pulse is provided. The ports in Figure 100 are described briefly in the following section.

Receiving from the RTDS

Table 7. Ports for receiving data from RTDS [47]

Port	Direction	Description
UserRxAdr(15:0)	Output	16 bit address – bits 1:0 are always '0'
UserRxData(31:0)	Output	32-bit data
UserRxValid	Output	Qualifies UserRxAdr and UserRxData as valid
UserTstepPulse	Output	Synchronization signal to RTDS backplane time step

All signals are synchronous to Clk100M.

- UserTstepPulse will be asserted for 1 clock cycle. It is delayed from the backplane time step by the propagation delay of the link, about 400nsec (untested value yet to be verified).
- UserRxValid will be asserted for 1 clock cycle. UserRxAdr and UserRxData are valid only when UserRxValid is high.
- The RTDS can send up to 64 variables to the GTFPGA. This is a restriction based on ease of development of the model and can easily be changed should there be a need.

Sending data from the FPGA to the RTDS

Data sent to the RTDS uses a 32-bit data bus and an 8 bit address bus. The end destination is a 64 x 32-bit memory accessible by the GPC processors. The bandwidth of this interface is

higher than the serial link to the RTDS so buffering is required and extra status signals are provided to handle data flow.

- UserTxAdr addresses the 64 x 32bit GPC end memory space. Only 32 bit accessibility is supported so bits UserTxAdr(1:0) are always ‘0’.

- UserLockBank and UserFreeBank allow data sets sent to the GPC to be read as complete units.

Issues may arise if the data read by the GPC processor is not all from the same set of data sent by the GTFPGA. For example, if the GTFPGA is sending 3 variables representing 3-phase voltages, it may be important for the GPC to read the data in such a way that all 3 variables are guaranteed to be from the same sample.

This is accomplished on the GPC end by using 2 banks of memory. When a new set of data is to be sent to the GPC, pulsing the UserTxWr when the UserLockBank input is high will lock the bank that the GPC processor is not reading from (if the GPC processor has a bank locked) OR will lock the bank that was least recently freed (if the GPC processor has no bank locked). The subsequent data that is sent by the GTFPGA will be sent to that bank. As soon as the data set is sent the bank should be unlocked so the GPC processor can have access to it. This is done by pulsing the UserTxWr when the UserFreeBank input is high.

Table 8. Ports for sending data to RTDS [47]

Port	Direction	Description
UserTxAdr(7:0)	Input	8-bit address – bits 1:0 are ignored as only 32 bit writes are supported
UserTxData(31:0)	Input	32-bit data
UserTxWr	Input	Qualifies UserTxAdr, UserTxData, UserLockBank and UserFreeBank as valid
UserTxFull	Output	Tx buffer is full, writes that happen when UserTxFull=' 1' will be dropped
UserLockBank	Input	Indicate beginning of data set… lock bank in double buffer
UserFreeBank	Input	Indicate end of data set. Makes bank usable by GPC Processor
UserTxInProgress	Output	Indicates when data is being put on link.
UserVersion(7:0)	Input	8 bit version field passed back to the rack for version reporting (visible from "status" command)

When a single write happens to the Tx port, the 32 bits of data, 8 bits of address and other protocol overhead is sent back to the RTDS. The UserTxInProgress signal indicates when this has all been put on the link. It does not however account for transmission delay to the RTDS so when UserTxInProgress goes to '0', the last data still has about 400nsec (untested value yet to be verified) before it will be available to the GPC processor.

Several other ports need to be mapped correctly to external pins of the FPGA for the reference clock and the RTDS serial connection. See [47].

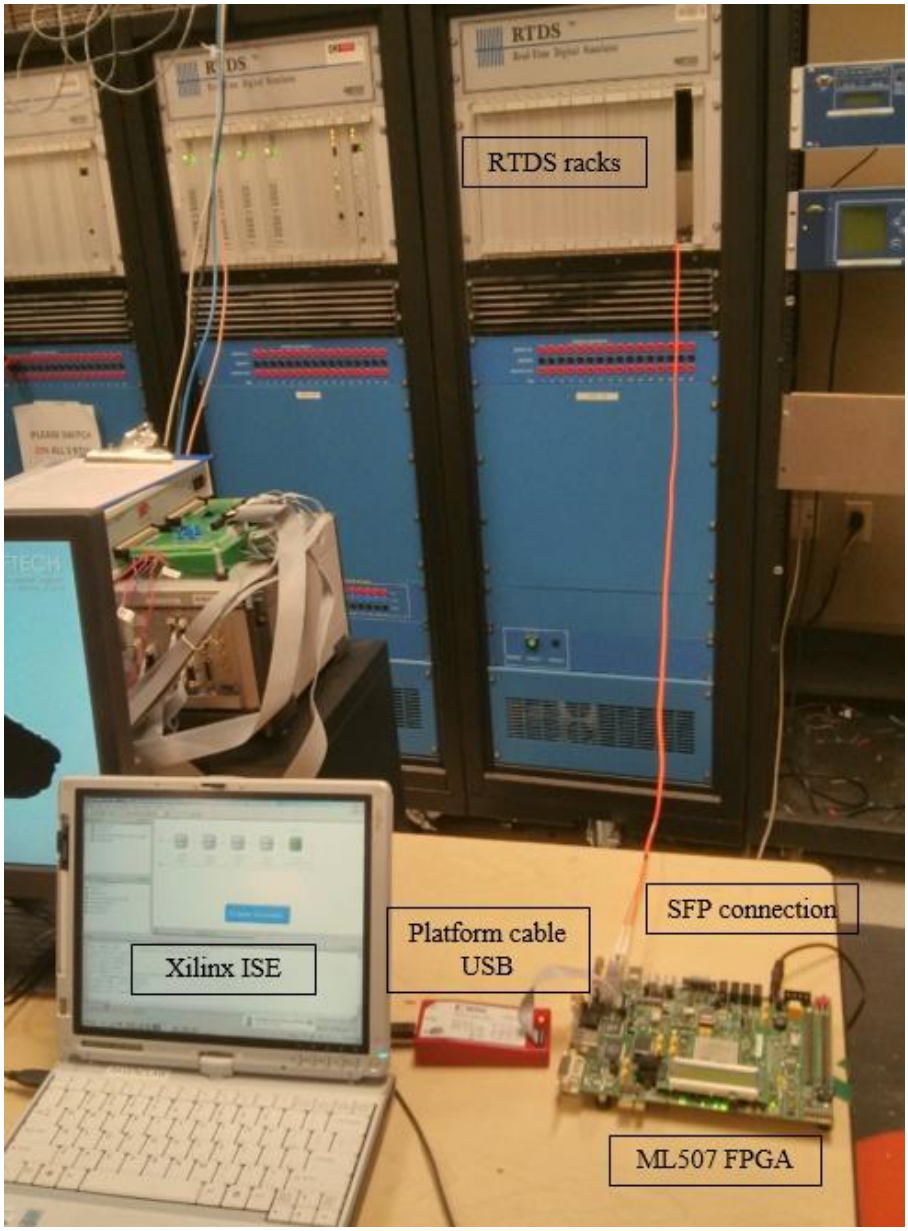

Figure 102. HIL setup

The open loop results with the above HIL setup were obtained as follows:

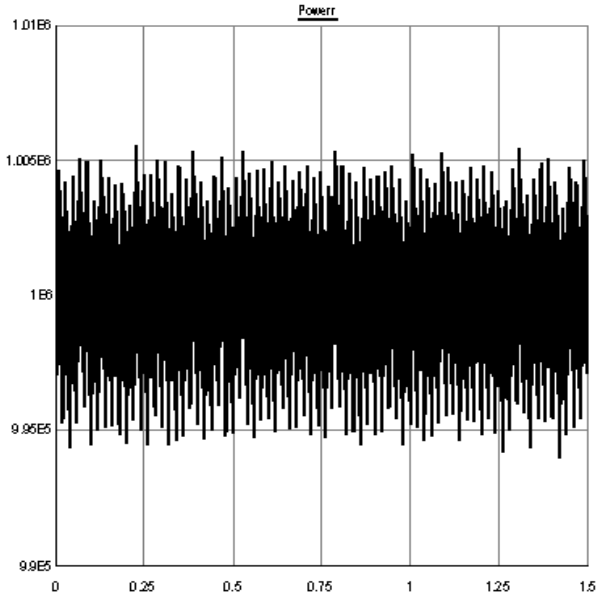

Figure 103. Power transfer 1 MW

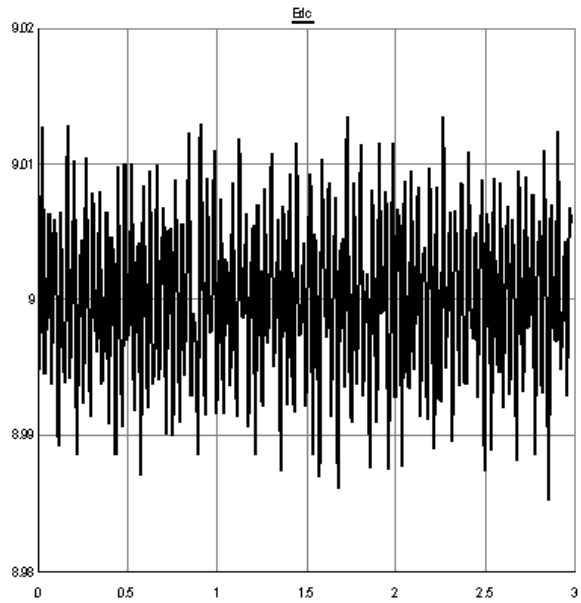

Figure 104. Terminal voltage

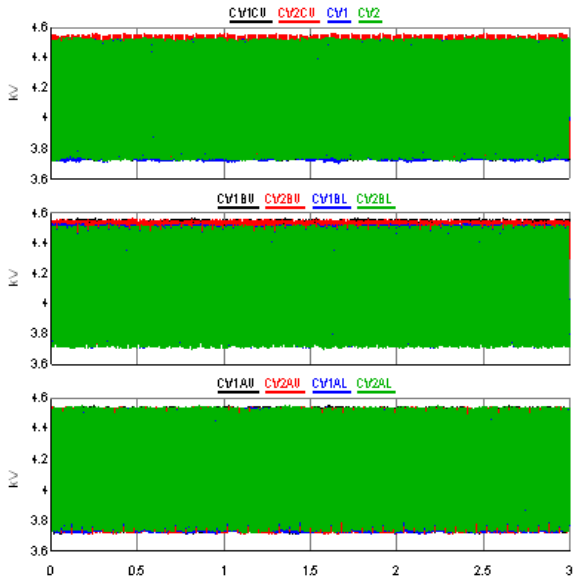

Figure 105. Sub-module capacitor voltages

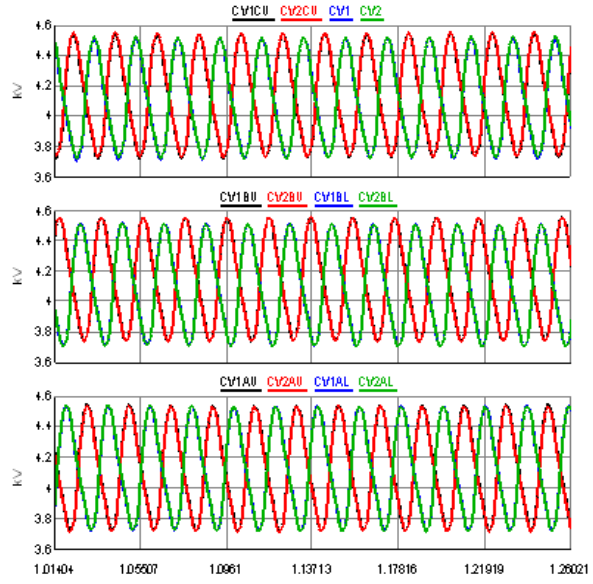

Figure 106. Zoomed portion of sub-module capacitor voltages

Chapter 8: Conclusions and Future Work

This project included implementation and validation of a back-to-back MMC HVDC system through simulation and HIL during steady-state and fault conditions. Another aspect was to apply the MMC converter for application in the ship-board power supply system and finally in a resilient two-terminal H-bridge based converter system for AC and DC fault studies.

Proposed future work includes implementation of the multi-terminal inter-connected HVDC system with all terminals as MMCs/full-bridge and a hybrid system comprising both topologies.

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