ABSTRACT

TEWARI, KARAN. Investigation of High Temperature Operation Emitter Turn Off Thyristor (ETO) and Electro Thermal Design of Heatpipe Based High Power Voltage Source Converter Using ETO. (Under the direction of Dr. Alex Q. Huang).

The Emitter Turn Off Thyristor (ETO) is an emerging high power device that can be considered as a Mosfet-GTO hybrid. It is very suitable for high power applications due to many of its significant advantages in terms of usability and performance benefits. The switching loss, leakage loss and conduction loss of the ETO are recorded as a function of junction temperature in order to gain a better understanding of the thermal performance. An effort is made in order to understand what limits the operation of semiconductor devices beyond a certain temperature limit. All this is then combined to develop a closed loop thermal model which is used to study the thermal stability. Thermal instability at high temperatures is caused primarily by the large leakage current, which rises exponentially with rise in temperature. Thermal stability can be maintained as long as the change rate of losses remains low enough such that the losses can be carried out of the switching junction of the device by means of the thermal conductance. This condition and the loss characteristics were used to predict the high temperature operating limit of the ETO. Multilevel converters have become an important technology in high-power applications, especially for Flexible AC transmission system (FACTS) applications. In this thesis, a high power (megawatt range) modular Voltage Source Converter (VSC), using the newly developed Emitter turn-off (ETO) Thyristor, is proposed and a design methodology is developed for the various parameters of such a system. One of the main constraints in the design of such a system is essentially the design of the cooling system to carry the large heat generated

by the various components such as switches, diodes and passives. Heat pipe based cooling system is very attractive for very high power applications. The hardware configuration, thermal calculation as well as component selection and design are presented in this thesis. Based on the electrical configuration of the new VSC, loss calculations are done for Statcom operation under different operation modes for components such as ETO and diodes, and the heat removal capability that is required from the heat pipes is determined. 3D Finite Element simulations are done on ANSYS software to understand the working and the selection of heat pipes. Electro-thermal simulations are done using thermal resistances of various components of the VSC including the thermal resistance of heat pipes obtained from tests.

Investigation of High Temperature Operation Emitter Turn Off Thyristor (ETO) and Electro Thermal Design of Heatpipe Based High Power Voltage Source Converter Using ETO

By

Karan Tewari

A thesis submitted to the Graduate Faculty of

North Carolina State University

In partial fulfillment of the

Requirements for the degree of

Master of Science

Electrical Engineering

Raleigh, NC

2006

Approved by:

_____	_____
Dr. Subhashish Bhattacharya Co-Chairman of Advisory Committee	Dr. Mesut Baran

_____

Dr. Alex Q. Huang
Chairman of Advisory Committee

To

Mom, Dad, Swati, Varun and Ankita

BIOGRAPHY

Karan Tewari was born in Deolali, Maharashtra, India in 1982. He received his BS degree in Electrical Engineering in 2004. Later, he joined NC State University in 2004 as a master's student in Electrical Engineering. He has been working as a research assistant in the Semiconductor Power Electronics Center over the course of 2004-2006, where he has done research on high power Voltage Source Converters and thermal stability analysis of semiconductor devices and cooling system solutions for high power converters. His other research interests include GaAs based power amplifier design, high speed analog circuit design and DC-DC converters.

ACKNOWLEDGMENTS

I am grateful to my advisor, Dr. Alex Q. Huang, for his guidance and support throughout the work that led to this thesis as well as during the writing process. His motivating words and sharp direction has helped me in the completion of my work and research towards the completion of this thesis. None of this would have been possible without his support. I am also grateful to my committee members, Dr. Subhashish Bhattacharya and Dr. Mesut Baran for help and suggestions throughout the research. I would like to commend my Co-chair Dr. Bhattacharya's friendly yet professional approach, and his invaluable guidance and advice towards my thesis.

I would also like to thank Bin Chen, Shoubhik R. Doss, Ding Li and Dr. Bin Zhang with whom I have worked during the course of this research. I would like to extend a special thanks to Bin Chen, with who I had wonderful discussions during the course of this research. His keen knowledge and interest in power electronics and circuits was an inspiration. I often looked up to him for problems that I faced during my research.

I would like to extend my special thanks to Chong Han, Wei Liu, Wenchao Song, Zhaoning Yan, Tiefu Zhao and Peter Liu with whom I spent a great time during the course of my Masters. The friendly discourses were always welcome refreshment, and their cooperation was a source of motivation.

I also thank Dr. Zhong Du for over seeing my work and providing vital advice and guidance. The friendly atmosphere in the lab that was present was a really important and comforting feeling, and much goes to the family-like group of students at SPEC. Special thanks is due to Mr. Sung Kuen Lim, with whom I had many intellectual and friendly discussions. The great work of Mr.

Jinseok Park in helping everyone in the lab with problems related to PCs and in always making everyone laugh with his great jokes also is worth appreciating.

I would like to extend a special thanks to all students at SPEC for their support and warmness. Mr. Jerry Kirk made life at SPEC very easy, by helping in many vital issues, and I thank him for his great work.

Encouragement from my friends outside of SPEC was also really helpful, and their support is really valued.

Finally, I thank my parents for their encouragement throughout my education. Their support means everything to me.

TABLE OF CONTENTS

LIST OF FIGURES

Chapter 1

LIST OF TABLES

CHAPTER 1

Loss Characteristics of the Emitter Turn-Off Thyristor

1.1 The Emitter Turn Off Thyristor

The ETO [1] is a MOS-controlled Thyristor that is suitable for high power applications due to improved switching performance and simplified control. Compared to the conventional GTO, the ETO is turned off under hard driven conditions, has a large reverse biased safe operating area (RBSOA), built in sensors for over-current protection, and has fully optical control, and all of these features enable the ETO to outperform many of its competitor devices.

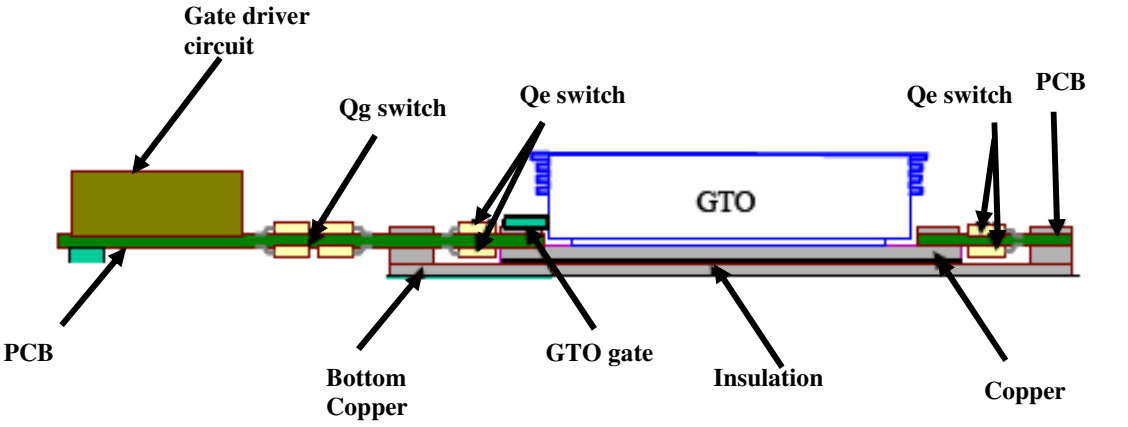


Figure 1-1. Cross section of the ETO

The ETO can be though of as a GTO-MOSFET hybrid [2, 3] device as shown in Figure 1-1. The two MOSFETs are operating as a complementary pair to help the GTO's turn-off. Once the emitter switch QE is turned off and the gate switch QG is turned on, the GTO cathode current will be diverted to its gate almost instantly, realizing so-called "unity gain" turn off condition, which means the GTO gate current equals the anode current. In this condition, GTO can be

safely turned off without any dv/dt snubber due to the much more uniform turnoff process, and the minimum on/off time can also be reduced due to its uniformly temperature distribution across the junction during switching. Figure 1-2 illustrates the structure and the basic operating principle of the ETO [4].

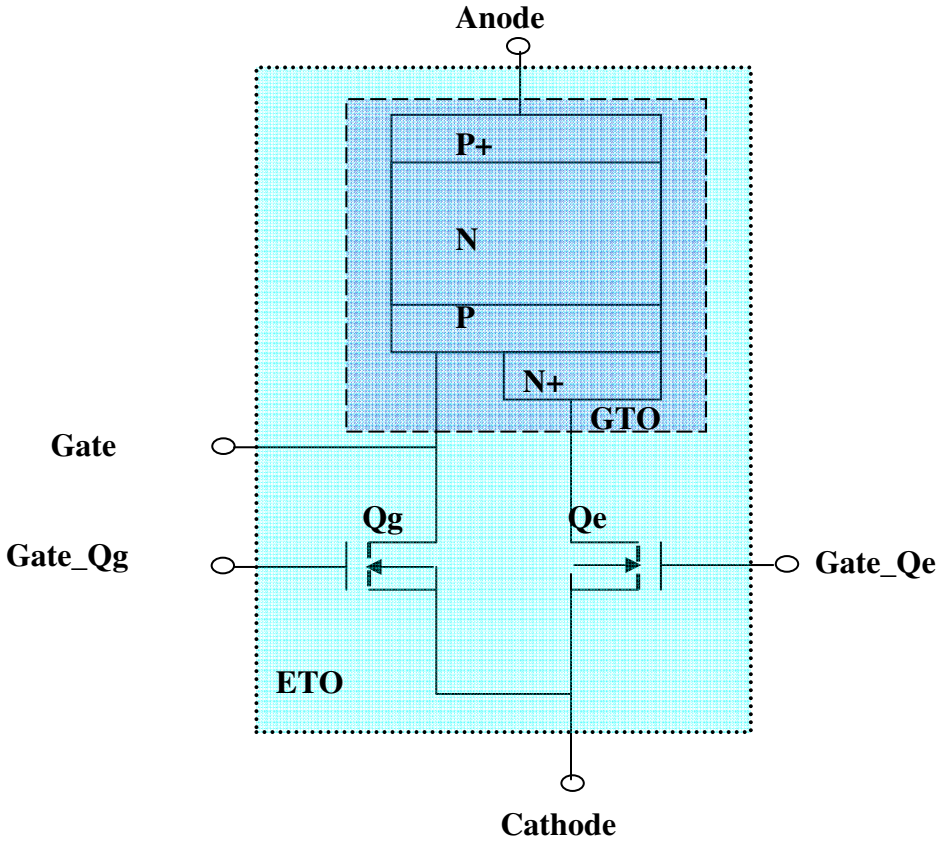


Figure 1-2. Basic Operating Principle of ETO

The benefit of the unity gain turn-off is two-fold. First, the storage time, which is the time needed for the gate-current to remove all minority charges in the p-base region, is now significantly decreased to about l psec. Second, unlike traditional GTO, the turn-off of an ET0 is changed to an open base PNP process that further ensures the current uniform distribution among

GTO cells over the turn-off transient. Consequently, the snubberless turn-off capability of the ET0 has been demonstrated as shown in Fig.3. Other significant advantages of this device are self gate drive power generation, lower gate drive power

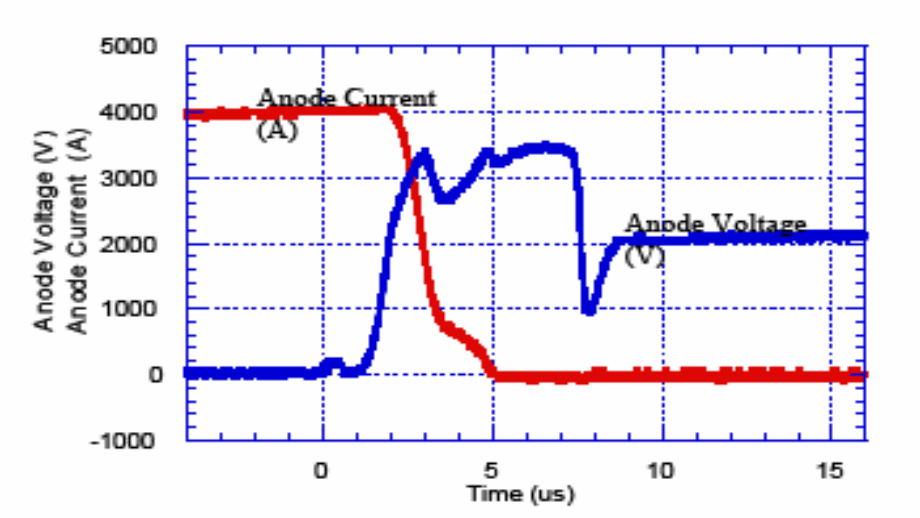


Figure 1-3. Turn off waveform of the 4.5kv/4.0kA ETO

requirement, higher frequency operation, and low system cost resulting from all of the above advantages. Fig.1 shows the picture of the 4.5 kV, 5 kA ETO. The ETO utilizes double side press-pack cooling package and achieves small thermal resistance. According to the measurement, the thermal resistance from junction to ETO case with double side cooling is about 12.6K/kW. In the last chapter, the thermal stability of the ETO has been studied and presented, with an effort on highlighting its excellent thermal behavior.

Figure 1-4. The 4.5kV 4.0kA Generation III ETO

1.2 Loss Characteristics

Thermal conditions significantly affect the performance of power electronics devices. In more general terms, high temperature generally degrades the properties of semiconductor materials. In unipolar devices such as MOSFET this happens largely due to reduction of carrier mobility with increased temperature as [4]:

$$\mu_T(T) = \mu_{300}\left(\frac{T}{300}\right)^{-2.3} \quad (1)$$

Where μ_T is the electron mobility and μ_{300} is the mobility at 300K. In bipolar power devices such as the ETO, however, the increase of lifetime at high temperature is the fundamental reason of its degraded switch performance at high temperature because this will results in higher losses. Another major effect that is true for both unipolar and bipolar devices is the increased leakage current at high temperature.

An obvious method of studying the device thermal limits is to study the device total losses at high temperature. To achieve this, the switching loss, conduction loss and leakage losses were measured at various temperature points and different operating conditions.

1.2.1 Switching loss

The switching loss was measured using the 'pulse tester' setup shown in Figure 1-5. The setup uses a high voltage DC power supply connected to a cap bank, and through an inductive load to the DUT (ETO). It is equipped with a di/dt snubber to limit the rate of current rise. There is an electric heater regulating the junction temperature of the ETO, and single pulses are fed to the DUT to turn it on and off. The turn off loss is hence measured at different temperature

conditions, at a step of every 10 degree Celsius. When the testing begins, the ETO is turned on in order to test its turn-on characteristic. Then the load current begins to commutate into the ETO from the freewheeling diode. The di/dt snubber inductor Lsnubber determines the rate of current transfer. So by choosing the value of Lsnubber, the desired turn-on di/dt of the ETO can be obtained for characterization of its turn-on performance. Shortly after the total current of the load inductor commutated into the ETO, the ETO is commanded to turn-off. The anode current of the ETO increases linearly. When anode current reaches the desired value, the ETO is command to turn off. The total load current will still go through the ETO until its anode voltage reaches the bus voltage. Then the ETO's anode current begins to be commutated to the free-wheeling diode and the clamp circuit. The ETO will see a voltage spike due to the stray inductance of the circuits. However this spike is limited to a safe value by the clamp circuit. The ETO has the highest stress during the interval when the current and voltage are simultaneously high. After the ETO's turn-off process ends, the ETO will block a voltage equal to the DC bus voltage. The current is still freewheeling through the load inductor, the free-wheeling diode and the snubber inductor Lsnubber.

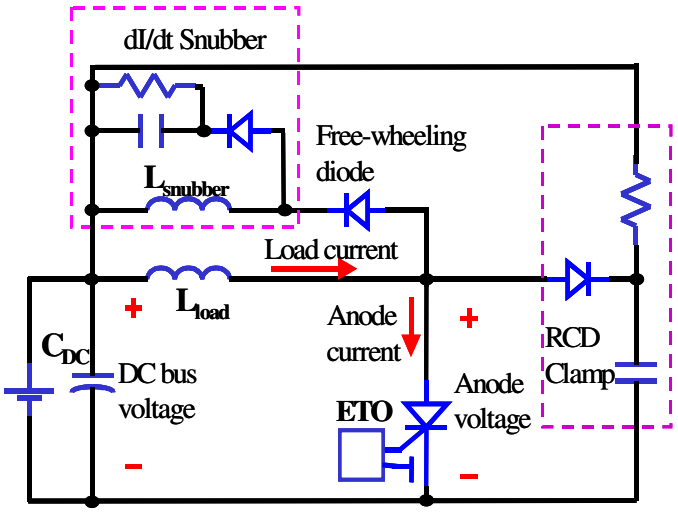


Figure 1-5. The pulse tester schematic used to measure Turn-Off loss

The loss is obtained by the integration of the voltage and current across the device, and is primarily due to the losses incurred by the device during turn off. The turn on losses is really small as the rate of current increase is limited by the use of a turn on di/dt snubber. Even in all practical implementations, the ETO is always used with a di/dt snubber primarily to protect the anti-parallel diode. For example, in the voltage source converter for FACTS applications, the ETO is always used with a di/dt snubber, and hence the turn on loss is negligible. So this does not have a bearing on our analysis. Figure 1-6 shows the variation of the turn off energy at 500V/500A with the junction temperature. This temperature is externally controlled with the use of an electric heater which is placed below the ETO cathode. The variation of this turn off Joules/pulse is seen to be almost linear, and equations for it are presented in the following pages.

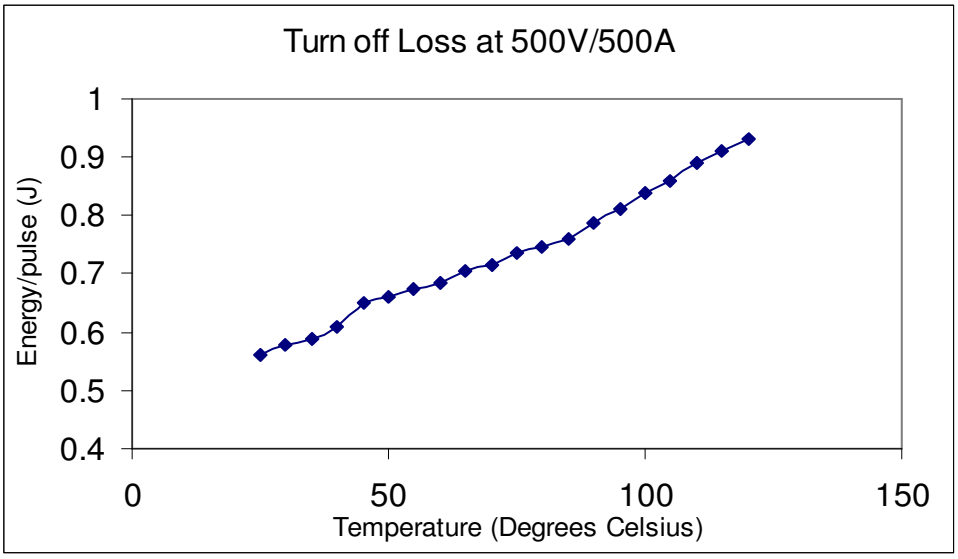


Figure 1-6. Turn off loss of ETO at 500V/500A with variation in operating junction temperature

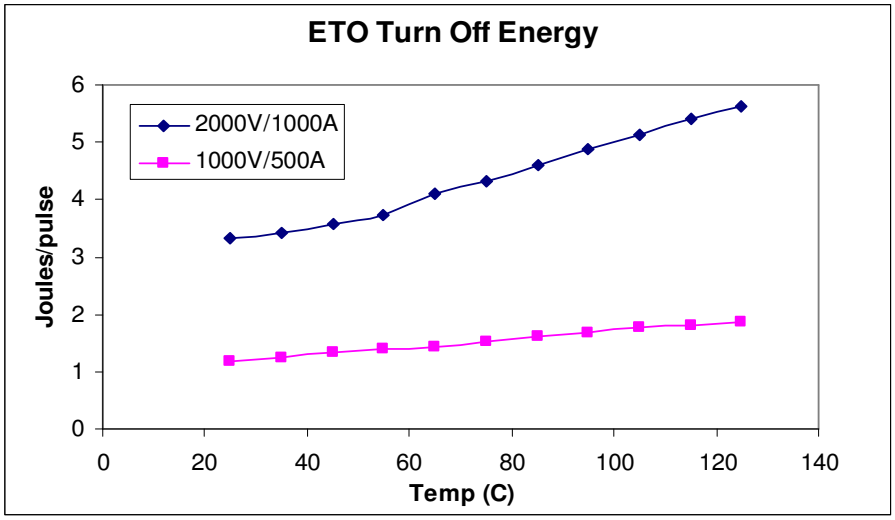


Figure 1-7. Turn off loss of ETO at 2000V/1000A and 1000V/500A with operating junction temperature

Fig 1-7 shows the almost linear rise of the turn off loss at 2000V/1000A and at 1000V/500A with junction temperature. The turn off loss shows almost a linear rise and is expressed as the following dependence on temperature at 2000V/1000A:

$$E_{off} = (0.245T + 2.535)J / Pulse \qquad (2)$$

It is worth mention here that the pulse tester used here to measure the turn off loss of the ETO has a clamp capacitor of value 1.5uF. The turn off loss is dependent on the value of clamp capacitor used with the device, as the voltage spike depends on the clamp capacitor.

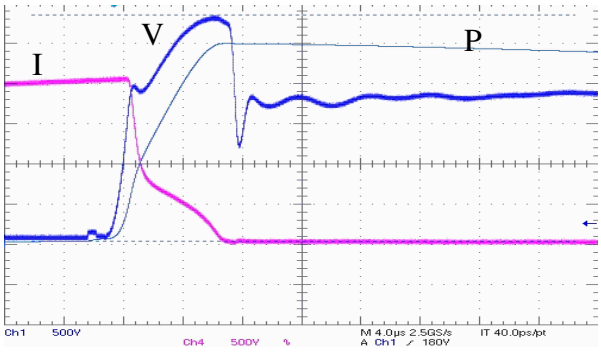


Figure 1-8.Voltage and Current waveforms during measurement of turn off loss at V=2000V and I=1000A

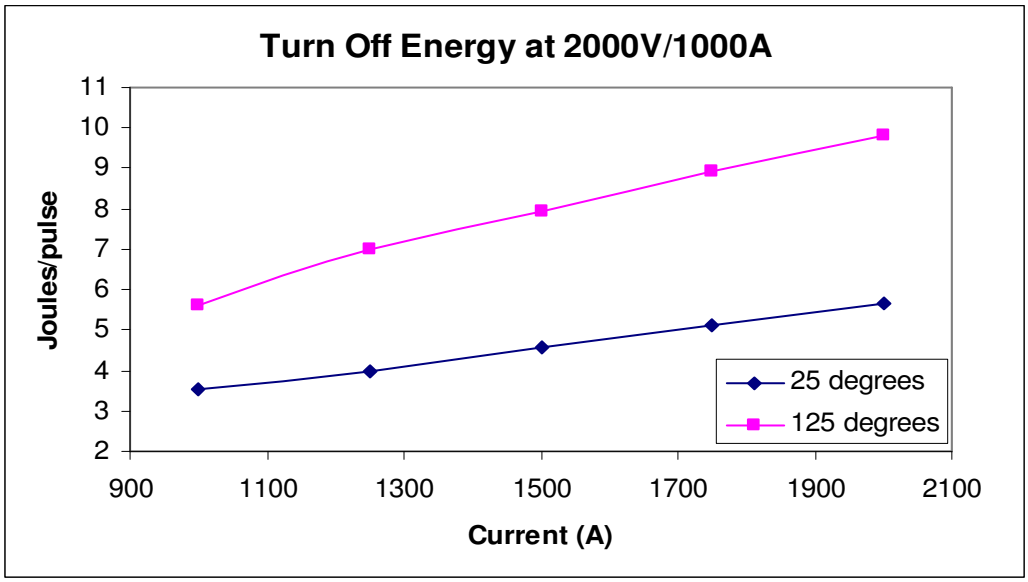


Figure 1-9. The variation of turn off loss at 2000V with current at 25 and 125 degrees Celsius

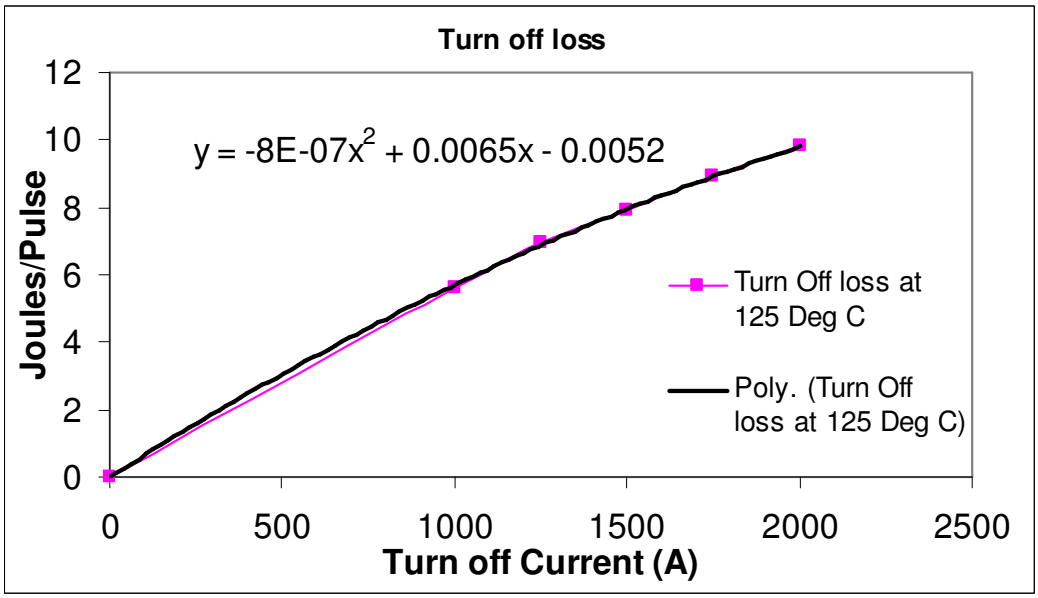


Figure 1-10. The variation of turn off loss with current at 125 Deg C, showing quadratic behavior with current

The figures above (Figure 1-9 and 1-10) show the variation of turn off loss at temperatures of 25 degrees Celsius and 125 degrees Celsius. It is seen that the turn off loss shows an almost linear

behavior with current. The variation is almost linear but not entirely. Erroneous results may occur if we assume linear variation. This assumption can lead us to the incorrect result of a non-zero loss with zero current being turned off, and this is slightly ambiguous. In other words, we would get finite turn off loss even at zero current. Then there are two ways to deal with this, either we can drop the constant term from the linear equation expressing the turn off loss versus current, or just assume a more realistic quadratic variation with current as shown in the Figure 1-10. In this curve, the solid line represents the quadratic curve-fit for the turn off loss at 2000V at different temperatures.

In dealing with design of converters, we generally make the calculations simple by dropping the constant part of the equation as shown below for equation (2) that can be modified into equation (3) as shown below:

$$E_{off} = (0.245T + 2.535)J / Pulse \cong \mathbf{0.245T\ J/Pulse} \quad (3)$$

However, when more accuracy is desired when dealing with a wider range of currents, including low values, we use the quadratic equations describing the variation of loss. For example, variation of turn off loss of the ETO at 2000V and 125 degrees Celsius junction temperature can be expressed as:

$$Eoff = -8 \times 10^{-7} I^2 + 0.0065I - 0.0052J / pulse \quad (4)$$

1.2.2 Leakage loss

To investigate the thermal stability, it is imperative to study the leakage current in the device, and hence the leakage characteristics of the ETO are studied to see how the leakage current changes with temperature. The basic temperature limit of the ETO is the Silicon semiconductor

material. At high temperature, the intrinsic carrier concentration increases rapidly, and at sufficiently high temperatures, the leakage current gets noticeably large. The exponential rise of the leakage current is the major contributing factor in the thermal instability at high temperatures. Experimental studies are done to measure the leakage current. The test setup and the equivalent circuit are shown in Figure 1-11. An electric heater is used to regulate the junction temperature. The heater is placed below the cathode of the ETO. The test is carried out at reverse bias voltage of 2000V.

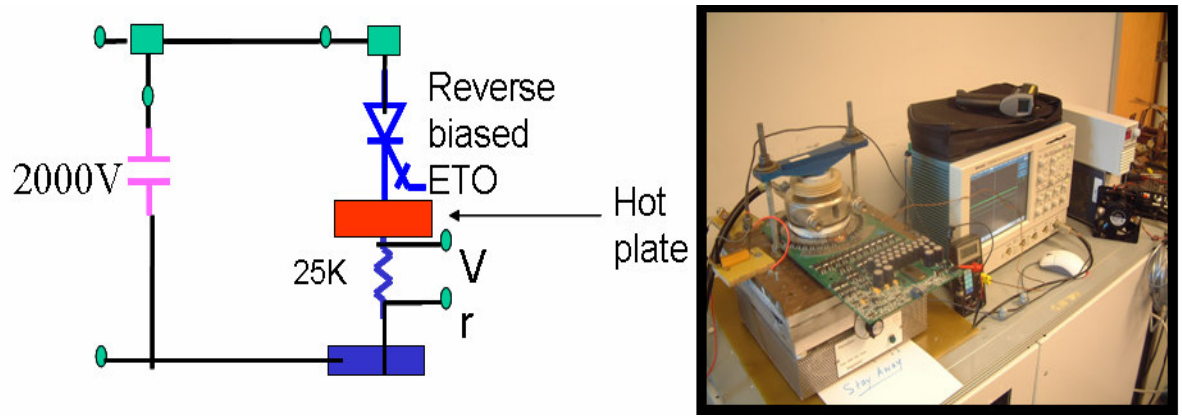


Figure 1-11. Set-up for the measurement of leakage current

The ETO is reverse biased to ensure that the device doesn't turn on. The leakage current is made to flow through a 25Kohm resistor in order for it to be measurable through the voltage drop across the resistor. Measured result is shown in Figure 1-12. It can be seen from the results that the leakage current is almost negligible at low temperatures. However, as the junction temperature rises, the leakage current rises exponentially to about 4mA at 125 degrees Celsius. The exponential rise of the leakage current can be expressed by:

$$I_{leak} = 0.2536\, e^{(0.079\,T)} \tag{3}$$

Where T is the junction temperature in degrees Celsius.

The above mentioned equation can be extrapolated to obtain leakage current at higher temperatures, till about 200 degree Celsius using (2), and it is expected that the leakage current is about 2 A at 200 degrees Celsius. So, at high temperature, the leakage current rises exponentially, contributing to the total power loss. The primary reason for this is the high rate of carrier generation at high temperature.

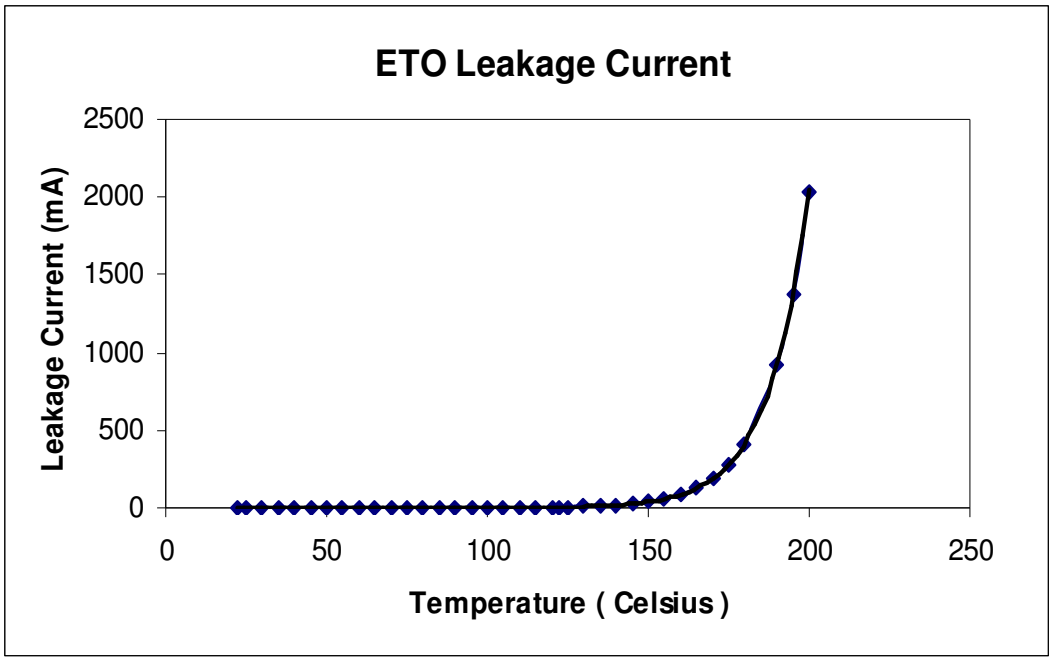


Figure 1-12. Leakage current rise with junction temperature at reverse bias voltage of 2000V

The leakage current was also measured for the IGCT [6], a commercial semiconductor device manufactured by ABB, and compared with that for the ETO. In the analysis for thermal stability done in Chapter 2, it is seen that the exponential rise of leakage current with temperature is the major cause of thermal instability at high temperatures. The exponential rise of loss caused by leakage current leads to exponential rise in the junction temperature of the device if the heat is

not carried out. In Figure 1-13 shown below, it is observed that the ETO has superior performance in terms of leakage current at high temperatures. Tests were done on two different available IGCTs, the 5SHY35L4511 and the 5SHY35L4503. They were tested up to 150 Degree Celsius, and the results are plotted below. It is seen that the two IGCTs show much higher rate of rise of leakage current versus temperature as compared to the ETO. While the leakage current across the ETO is only 3mA at 125 °C, the two IGCTs reach values that are much higher. The 5SHY35L4511 reaches 70mA, while the 5SHY35L4503 reaches 100mA at 125 °C. This would, as we would see later, directly correspond to greater thermal stability for the ETO at higher temperatures. The ETO shows much better performance in this regard.

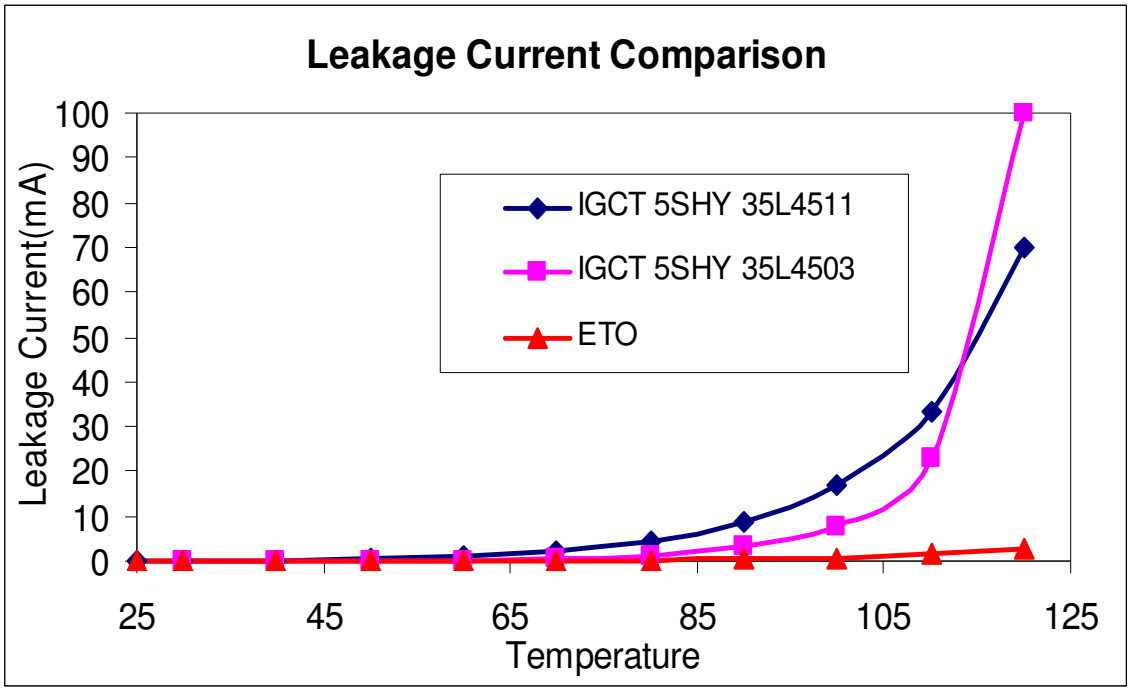


Figure 1-13. Leakage current comparison between IGCT and ETO at DC Voltage of 2000V

1.2.3 Conduction loss

In order to measure the conduction loss, a very simple circuit was used. The conduction loss can be measured by measuring the on-state voltage when the ETO conducts high current through it. Since, measurement of the conduction state involves a very high current, of the order of a few kilo Amps, care had to be taken to use a low voltage source. This was achieved through the use of a large cap bank, with several capacitors in parallel to produce the large current. A switch was used to disconnect the cap bank from the low voltage source before turning on the ETO. The ETO was turned on in order to discharge the capacitor, and make the large resulting current to flow through it. The conduction voltage waveform was recorded to get values of $V_{on,}$ at different currents and temperatures. The temperature was regulated using the same electric heater as before. The pulse width of the optical signal which is used to fire the device is ensured as long enough to enable the current to discharge fully to zero. The graph shows the current first peaking and then dying down to zero. The value of V_{on} is measured at different currents. This is repeated at different temperatures to obtain the on state characteristics as well as the conduction loss curves.

The following curves show the on state voltage drops across the GTO, the Qe MOSFETs and the ETO respectively, at 25℃ and 125 ℃. these tests were done as part of earlier research on the ETO, but do not include information about variation of conduction loss with temperature. They are shown in Figure 1-14, 1-15 and 1-16.

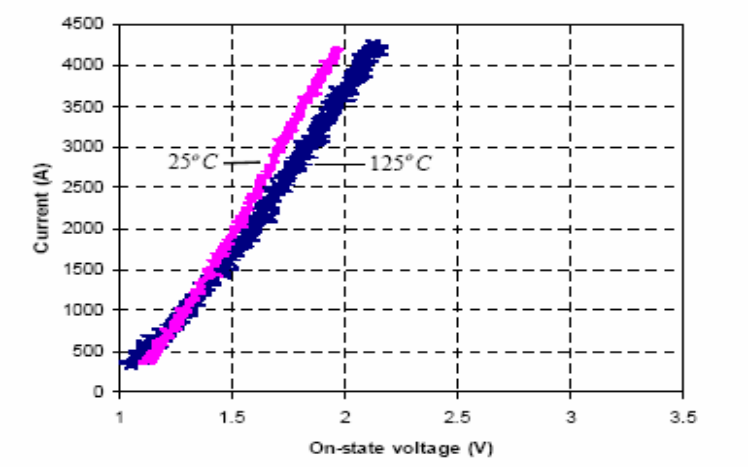


Figure 1-14. On-state voltage across GTO

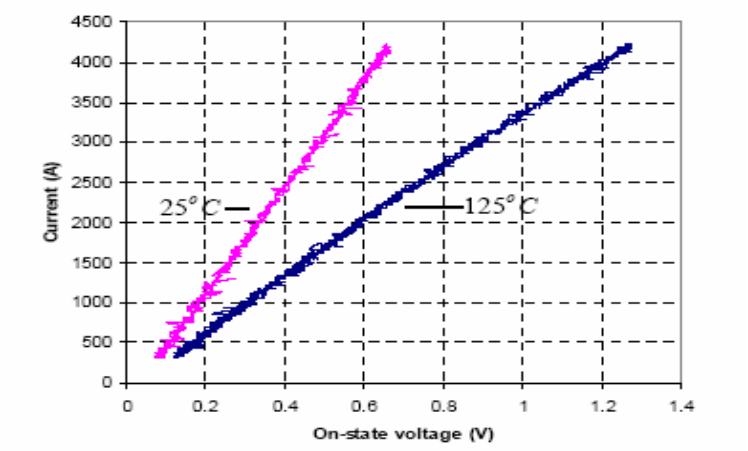


Figure 1-15. On-state voltage across Qe MOSFET

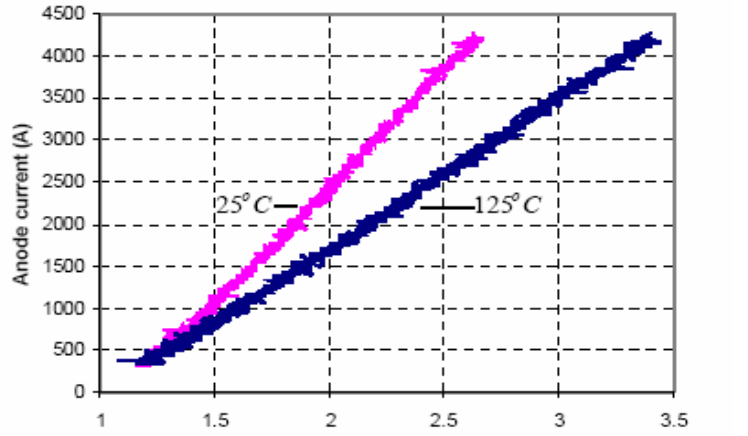


Figure 1-16. On-state voltage across ETO

It can be seen from the previous three figures that the ETO has a little higher voltage drop than that of the GTO due to the voltage drop of the emitter switch. The bigger voltage drop leads to a higher conduction loss. On the other hand, the ETO has more resistive I-V characteristic, which is good for current sharing in the parallel connection application, than that of the GTO due to the resistive I-V characteristic of the emitter switch. Furthermore, the positive temperature co efficiency I-V is very important to avoid the positive feedback of current crowding. The tests are done on the ETO to get the conduction loss versus

temperature. Figure 1-17 shows the simple set-up to measure conduction loss, as mentioned before. The voltage and current through the ETO during the test are shown in Figure 1-18.

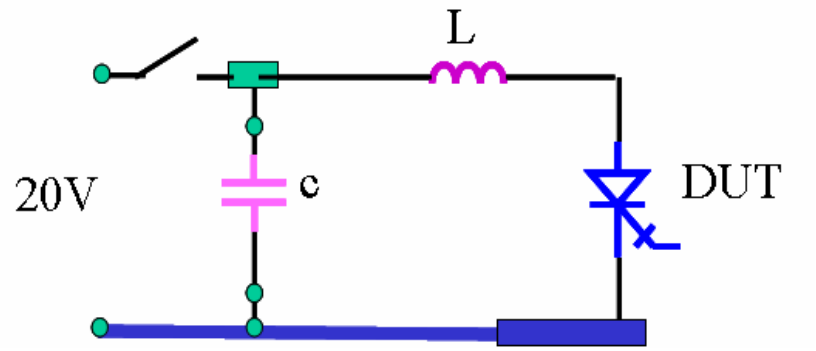


Figure 1-17. Test setup for conduction loss

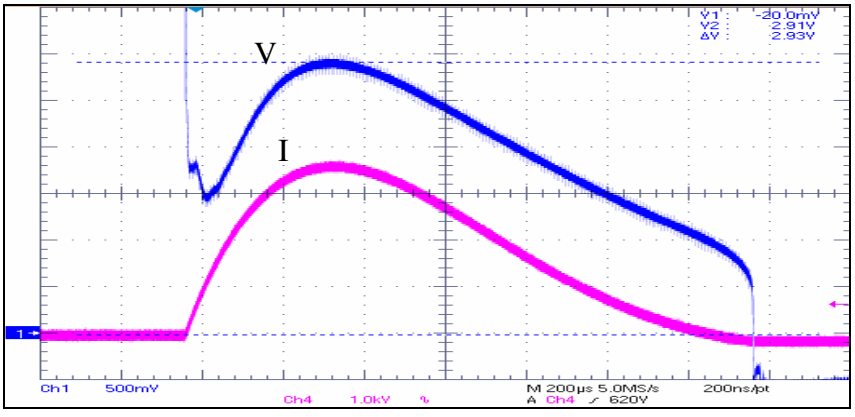


Figure 1-18. Voltage and current waveforms across ETO

The variation of the on state voltage with current and temperature is shown in Figure 1-19 and Figure 1-20. The conduction loss in kW can be represented by the equation (for 1000 A):

$$Eon = 0.0002\,T + 0.3134 \text{ Joules} \quad (5)$$

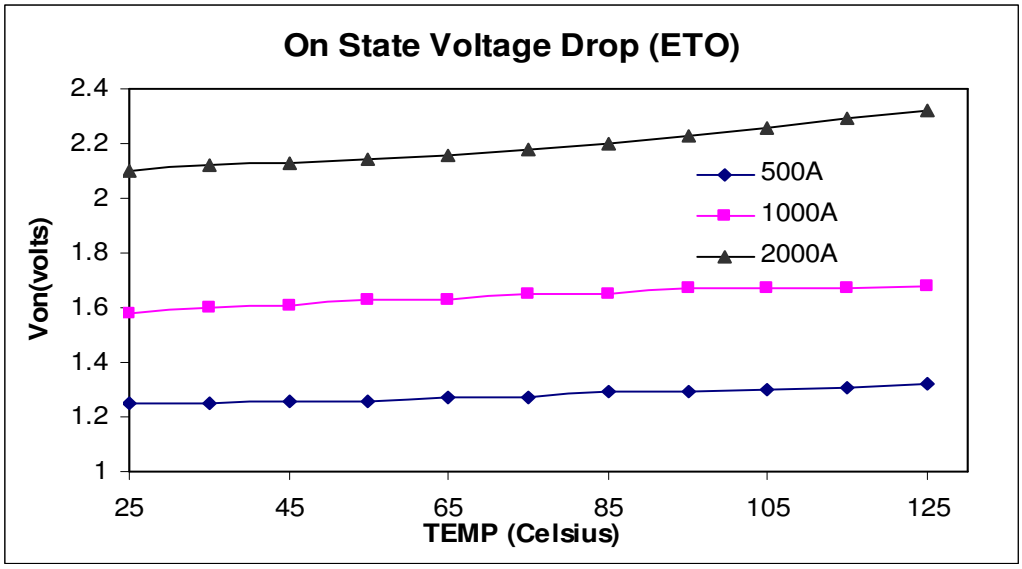


Figure 1-19.On-state voltage across the ETO at different currents versus operating junction temperature

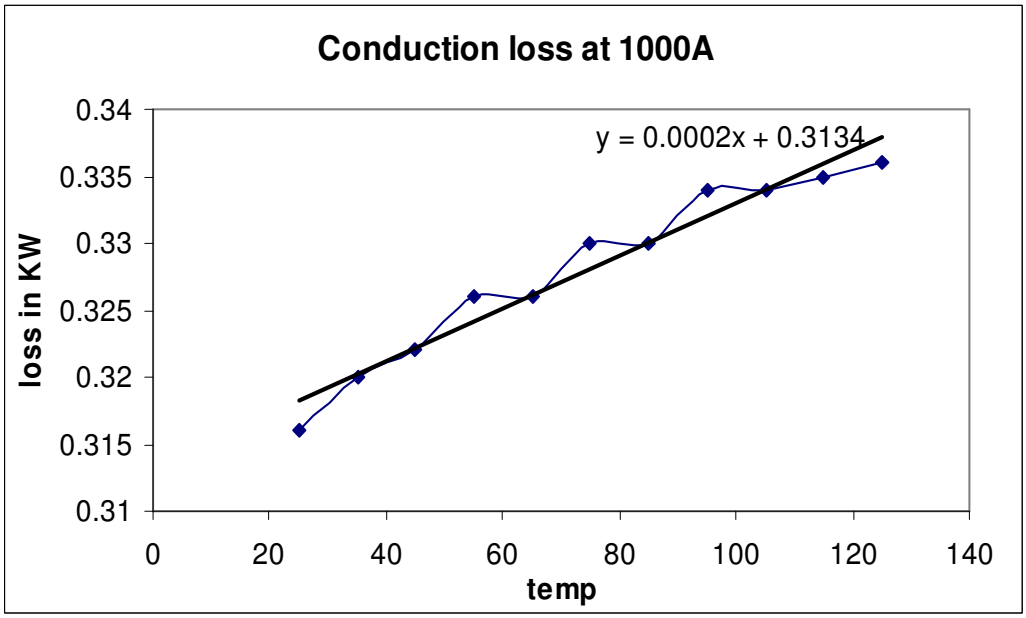


Figure 1-20. Linear variation of conduction loss at 1000A DC current versus junction temperature

The on state voltage is independent of the circuit topology. It can be seen from the above results that the conduction loss for a given current, at different temperature remains almost the same, and also that the conduction loss would form a small part of the total loss, when it is computed for a switching cycle.

1.3 Total loss of ETO

The total loss in the ETO is the sum of the turn-off (switching) loss, conduction loss, and the leakage loss.

$$P_{total}(T_j, f_s, I) = \left[E_{on}(T_j) + E_{off}(T_j)\right] f_s + DV_{on}(T_j) + (1 - D) V_{dc} I_{leak} \quad (6)$$

The ETO has negligible turn on loss because of the use of a turn-on snubber inductor, to limit the maximum di/dt. The use of this turn on snubber is essential for the ETO since it is based on the GTO, which is a large area device. For the GTO, during turn on, with the formation of positive feedback, after the anode current exceeds the latching current, the gate has little control over the turn-on process. The rise of the anode current is dictated by the physical process of the device as well as the constraints of the external circuit. Since the slowly applied gate current initially only turns on a small area of the GTO, the turn-on process begins with a small cathode area close to gate contact and spreads to adjacent regions. The typical spreading speed is about 5000 cm/s. To avoid the localized overheating effect and to prevent turn-on failure in the device, an external inductor is usually used in the external circuit to limit the anode current rise rate to a level below the critical di/dt. We hence neglect the small value of the turn on losses for the ETO. In the

equation 6, we see that the total power loss is a function of the junction temperature, switching frequency and the current. The turn off joules/pulse is multiplied by the switching frequency to get the average turn off loss. The conduction loss is multiplied by the duty cycle (D) of the ETO and the leakage loss is multiplied by (1-D). At these low loss levels, which happen at low junction temperatures, the leakage current is a small fraction of the total loss. As shown in Figure 1-21, at low temperatures such as 55 degree Celsius, the leakage loss is negligible as compared to the other losses. The switching loss is dominant followed by the conduction loss. Also, as shown in the next figure, Figure 1-22, the leakage loss is still low; almost zero percent of the total loss, at 125 degree Celsius. This is because as seen in Figure 1-12, the leakage current of the ETO is almost constantly low till 150 Degree Celsius, after which it starts rising exponentially.

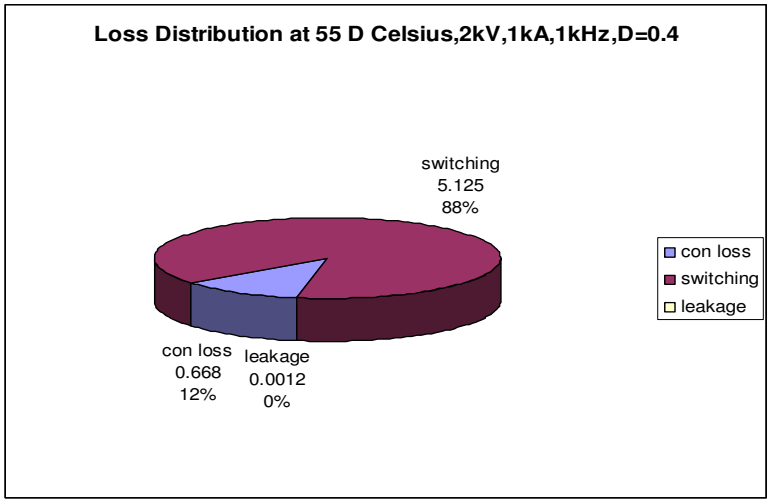


Figure 1-21. ETO loss distribution at 55 Degrees Celsius Junction temperature

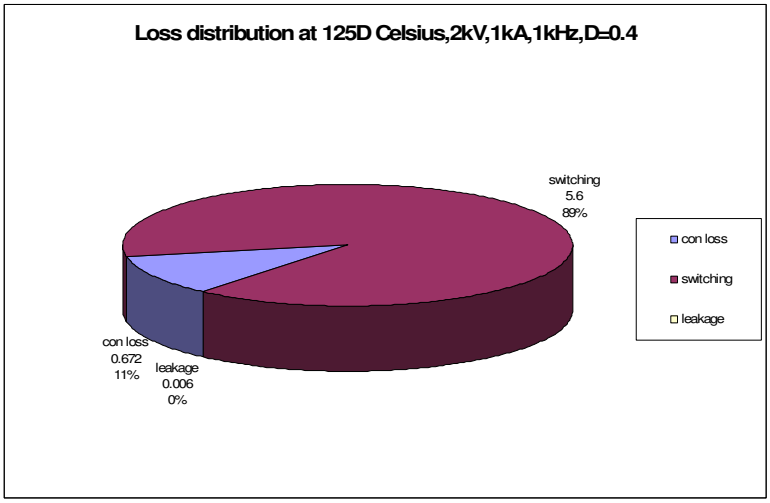


Figure 1-22. ETO loss distribution at 125 Degrees Celsius Junction temperature

At low temperatures, the loss is lower for low duties since the rise in conduction loss due to rise in D is the dominant part of total loss change. However, as the temperature increases, the total loss for lower duty cycles tends to be higher than that for higher duties. This happens because at higher temperatures beyond 150 Degree Celsius, leakage loss starts increasing exponentially, and its contribution to total loss also shows a similar trend. As seen in the Figure 1-23, at 200 degree Celsius, the contribution of leakage loss becomes 30 % of the total loss. The switching and conduction losses are also rising with temperature, but their rise is linear at best.

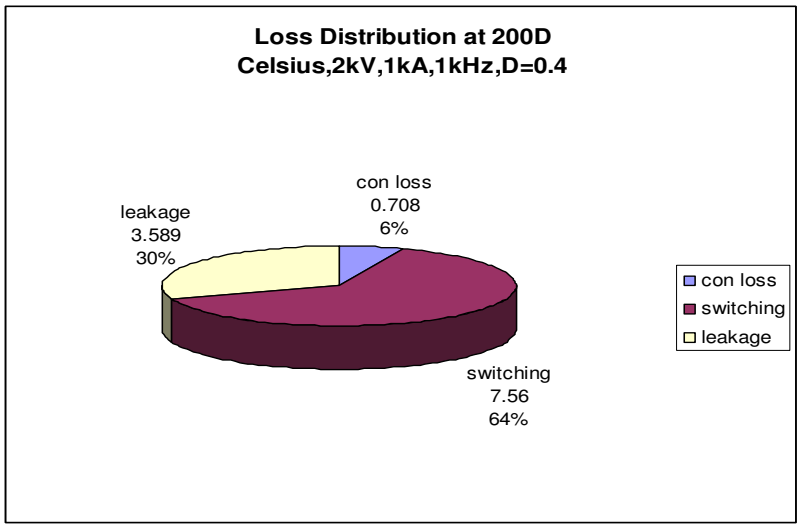


Figure 1-23. ETO loss distribution at 200 Degrees Celsius Junction temperature

The curves in figure 14 are a plot of the total loss versus junction temperature. It can be seen that the total power loss in the ETO rises exponentially with increase in the junction temperature. Since the switching loss and conduction loss are linear functions of temperature, the total loss curve shown in Figure 1-24 and Figure 1-25 are linear till a certain point, after which it rises exponentially due to exponential rise in leakage current beyond that point. Since the leakage loss is dependent on the complement of the duty cycle, so at higher temperatures, higher duty cycle implies lower loss. This is evident from Figure 1-25 where we see the loss at temperatures below 160 degree Celsius as being higher for high duties of the ETO, with 0.6 being the maximum. At higher temperatures, the loss is low for the highest duties. In other words, reduction in Duty Cycle leads to lower losses, and hence can lead to lower junction temperatures, and this happens at lower loss levels.

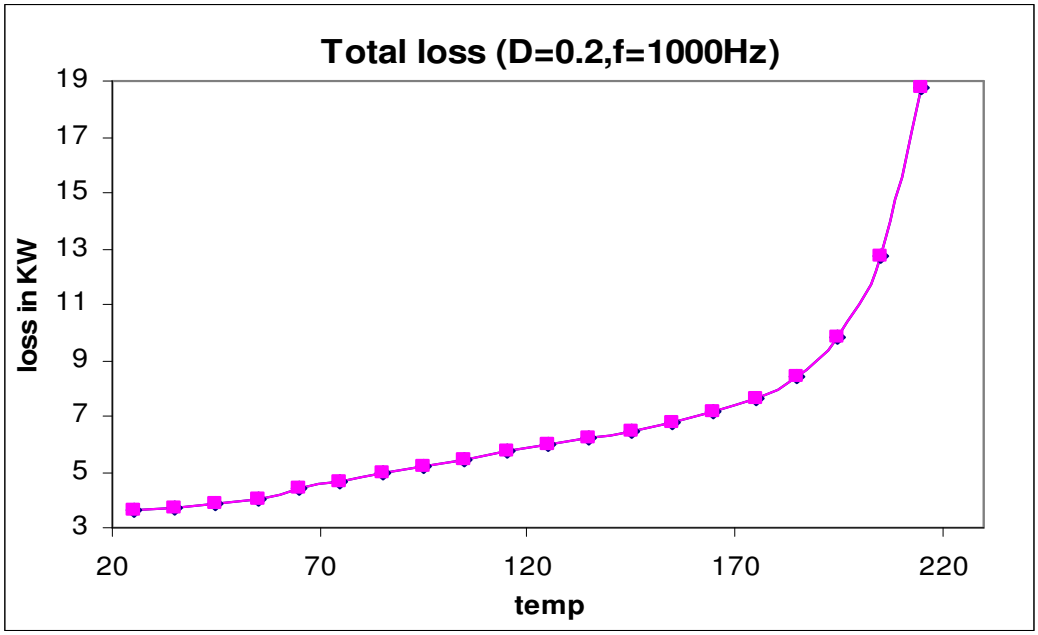


Figure 1-24. Total loss curve at Vdc=2kV,Ipk=1kA,D=0.2,f=1kHz

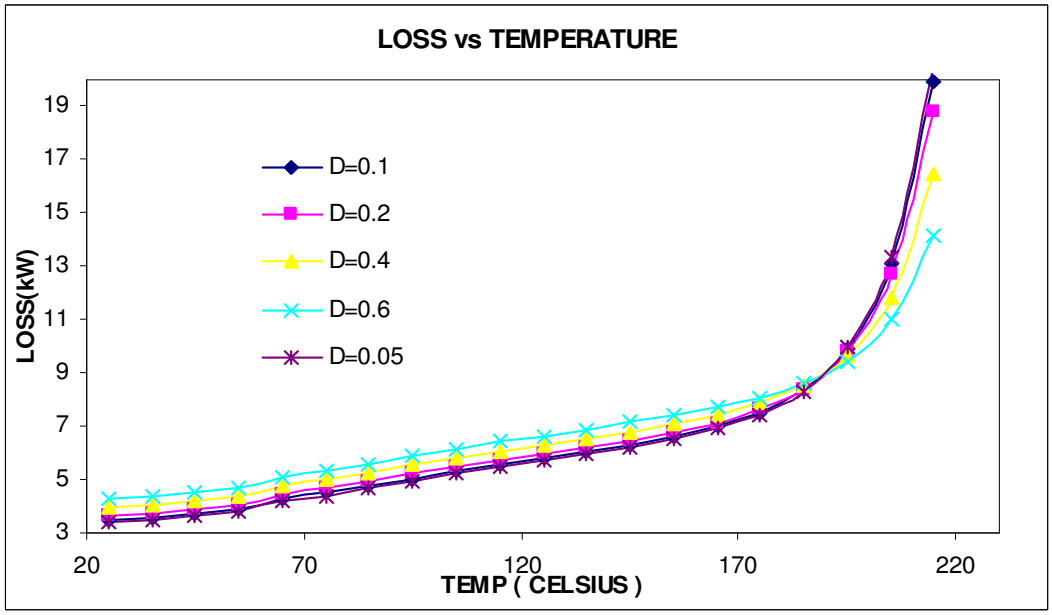


Figure 1-25. Total loss curve for different values of Duty cycle at Vdc=2kV,Ipk=1kA,f=1kHz

CHAPTER 2

Investigation of High Temperature Operation of ETO

2.1 Closed Loop Thermal Model

As mentioned earlier, the total losses generated in the ETO operation, including the switching loss, the conduction loss, and the leakage loss must be carried out of the switching junction to ensure smooth operation of the device, without build up of heat. The thermal impedance of the device represents its ability to transfer heat out of its switching junction. This value depends on primarily the semiconductor material and packaging. As mentioned earlier in, the losses are a function of the temperature and total loss is hence a function of the junction temperature too. A closed loop thermal system can hence be modeled as shown [7].

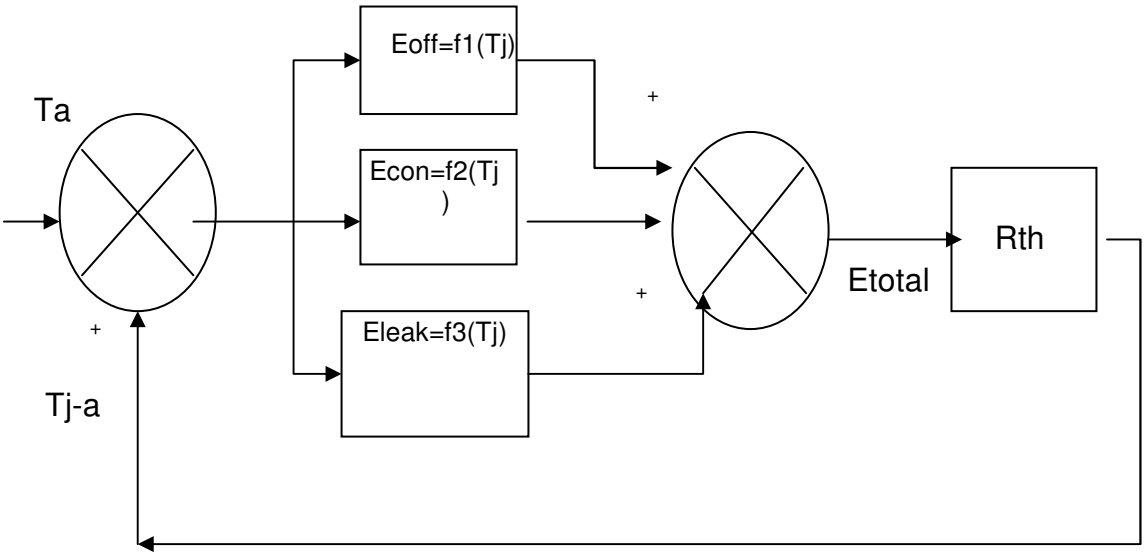


Figure 2-1. Closed loop thermal model for the ETO

The operating temperature of the device is determined by the closed loop represented above, and is dependent on the amount of heat generated and the ability to carry it out of the junction, as

also on the ambient temperature. $\mathbf{R_{th}}$ is the thermal resistance from the junction to the ambient. $\mathbf{T_a}$ represents the ambient temperature. The bias point of the above thermal loop can be represented as:

$$T_j = T_a + R_{th}P_{total} \qquad (7)$$

The closed loop with positive feedback can be explained intuitively. The losses, as seen before are strongly dependent on the junction temperature of the ETO. So, as the ETO starts switching, the losses increase a little bit in the very initial period. As a result, the temperature increases. Now, since the temperature has increased, that means the loss also has to increase (since loss is a function of temperature), which means that the temperature increases again. This explains the feedback mechanism shown in the thermal model. This continues till the amount of heat being produced equals the amount of heat being carried away from the junction. This is typically done by using different kinds of cooling methods, all of which work on the basic principle of providing a low thermal resistance path from the junction of the device to the ambient to which heat can flow. The operating junction temperature Tj must be kept below a certain temperature rating Tjmax. This temperature rating is provided by the manufacturers to ensure reliability and long device lifetime. This temperature is typically believed to be around 125 degree Celsius for Silicon devices, and around 600 degrees Celsius for devices made from wide band gap materials such as SiC. This number for silicon is not based on any limit imposed by operating capability, but is simply a standard which is used in order to ensure long life of the devices being used.

In order to ensure stability for the thermal loop shown in the above figure, it is important that the change rate of the total loss with respect to junction temperature times the thermal impedance be less than unity, or in other words, the loop-gain be less than unity.

$$(dP / dT_j) R_{th} \leq 1 \qquad (8)$$

Equation (8) poses an additional constraint on the junction temperature, which may be higher or lower than the device rated junction temperature as provided by the manufacturer $T_{jmax.}$ This may alter the device safe operating area. These results and equations 6, 7 and 8 shall be used to conduct experiments on the ETO to study its thermal stability. Plots of equation (8) shall be used to determine the maximum operating temperature of the device.

2.2 Thermal resistance of the ETO

In order to get the thermal resistance of the ETO, experiments are carried out on a boost converter topology, connected to a high power DC source, and a large cap bank. A large boost inductor is used to boost up the current, and the DUT is the Generation-3 ETO. A large resistor bank is connected to the output capacitor, to help in the operation of the boost circuit, and to also prevent its output voltage from rising too high. The boost converter is controlled using a PWM generating control board for the ETO. The duty cycle and frequency of operation can be adjusted. The test is carried out at different duty cycles and frequencies. The boost converter is operated in the discontinuous conduction mode with a small duty cycle. The purpose of using this configuration is to generate losses on the ETO and monitor the temperature rise on it case at different points and get the thermal network for the ETO. The schematic and setup for the Boost converter are shown in Figure 2-2 and Figure 2-3 respectively.

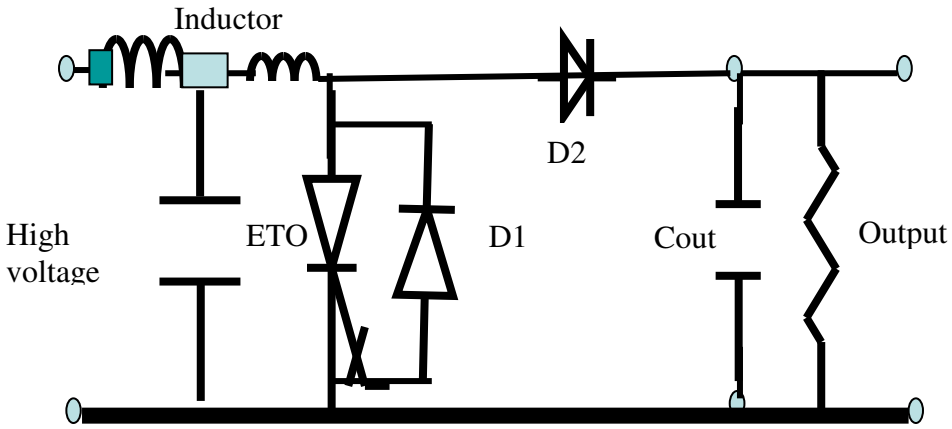


Figure 2-2. Schematic of the Boost converter

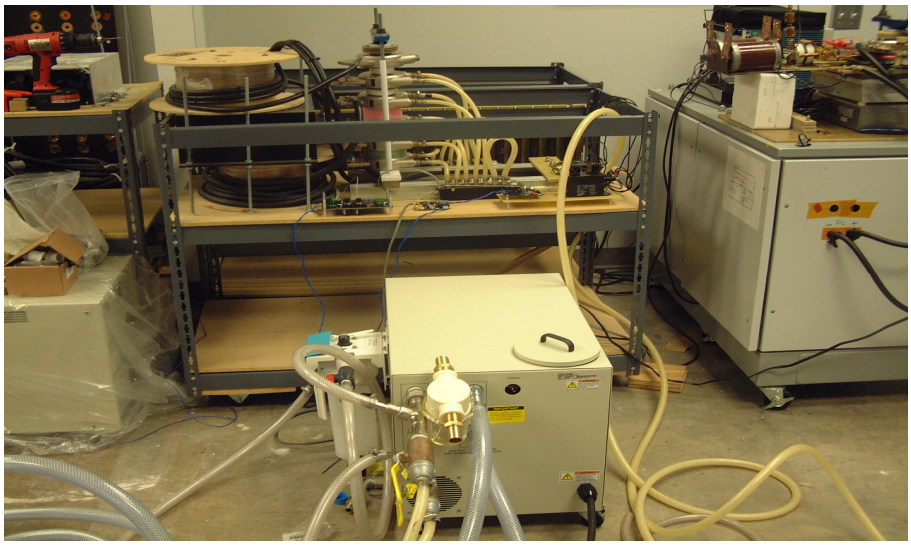


Figure 2-3. Boost converter Setup

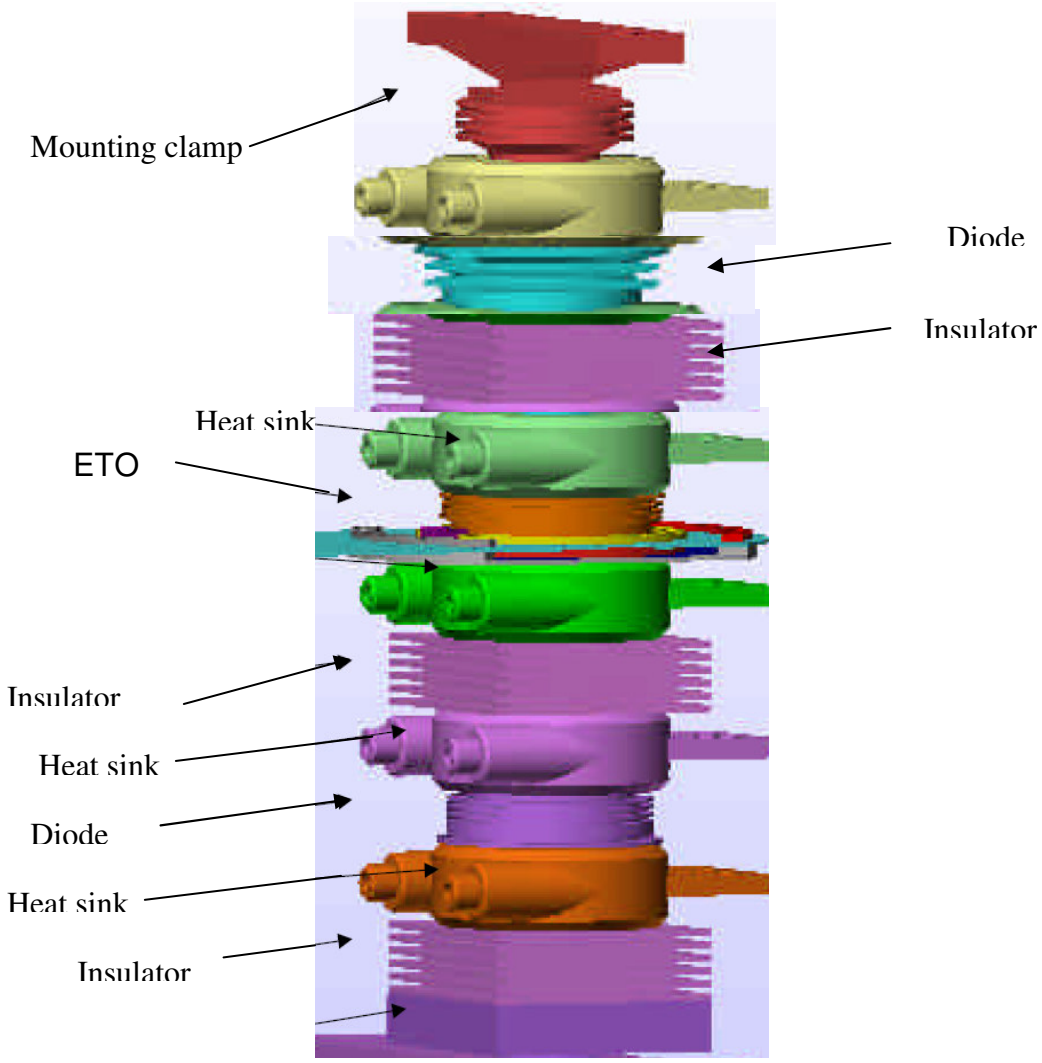


Figure 2-4. The Boost converter stack set-up

The stack configuration is shown here. An interesting aspect of the configuration is the use of thermal insulation in between the anti parallel diode and the ETO and between the feed forward diode and the ETO. This is done so as to ensure that the temperature rise on the various sensing points is only due to losses on the ETO and not contributed to by the diodes as well. The diodes, particularly the feed forward diode, have losses in the form of switching loss and reverse

recovery loss. The losses for this setup are measured using the oscilloscope by performing integration of the voltage and current across the ETO. Care had to be taken to adjust the offset in the Ragowski coil. Double sided cooling is employed for the ETO using water cooled ABB heat sinks. NESLAB water to water heat exchanger (chiller) is used to provide the cooling water flow through the heatsinks. This chiller transfers heat into a heat exchanger located outside the laboratory. Water flow rate is fixed at 10 Liter per minute (LPM) coming out of the chiller. Some features of the chiller used for this experiment are shown below in Figure 2-5:

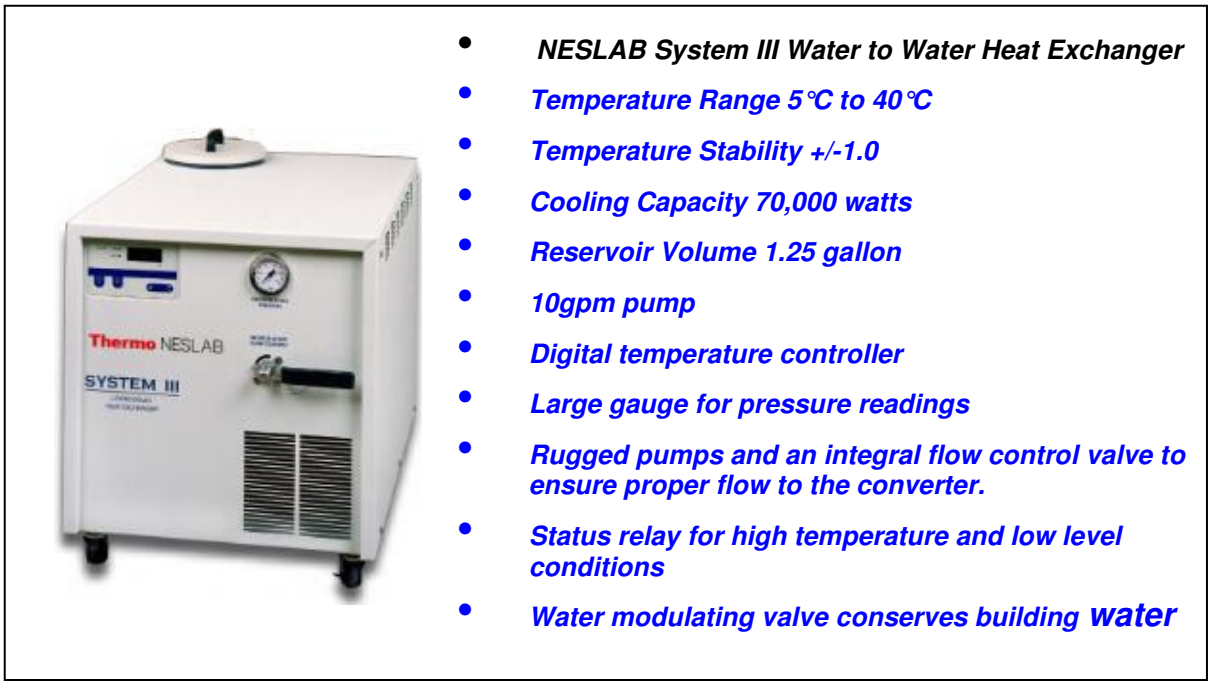


Figure 2-5. The Neslab chiller used in the boost test

The chiller is basically a Heat Exchanger that uses the cooling of the lab's central water system while eliminating all the problems associated with building water. The water supply circulates through one side of the heat exchanger while the System pumps temperature controlled water out

of a secondary circuit directly to the boost. Our equipment will be protected from contaminants commonly associated with building water systems because we can control the quality of the fluid that the system circulates. The experiment is performed for about 30 minutes until the temperature of the junction and the cooling water reached a steady state. The steady state ambient temperatures and case temperatures were recorded to attain the thermal resistance. The following points were used to measure the thermal resistance of the ETO from the junction to the case:

- anode of the GTO
- cathode of the GTO
- cathode of the ETO, that is the bottom copper plate
- inlet water temperature

Thermocouples and digital thermometers were used to measure the temperatures on the ETO, and the water inlet temperature was read off from the chiller digital display. These points are shown on the ETO in Figure 2-6. The anode of the ETO, cathode of the GTO and the cathode of the ETO that is the bottom copper plate as shown in the figure, were the three points where thermocouples were installed to record the temperature.

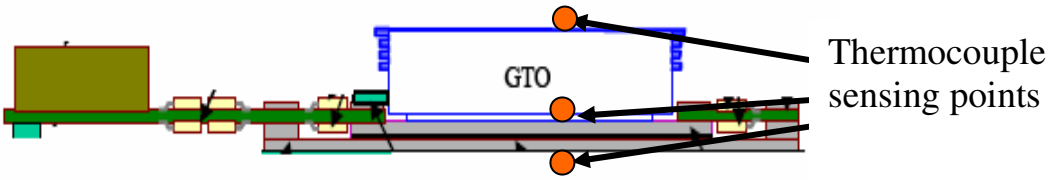


Figure 2-6. The points of temperature measurement on ETO

Table I. Thermal resistance information from the GTO datasheet

Parameter	Symbol	Conditions	min	typ	max	Unit
Thermal resistance junction to case	$R_{th(jc)}$	Double side cooled			11	K/kW
	$R_{th(jc)A}$	Anode side cooled			20	K/kW
	$R_{th(jc)C}$	Cathode side cooled			25	K/kW
Thermal resistance case to heatsink (Double side cooled)	$R_{th(ch)}$	Single side cooled			6	K/kW
	$R_{th(ch)}$	Double side cooled			3	K/kW

The thermal impedance model of the ETO is shown in fig. 13, which is obtained after measuring the temperatures at 3 different points on the ETO. Some parameters in the network are know apriori from the datasheet of the GTO shown in Figure 2-7.

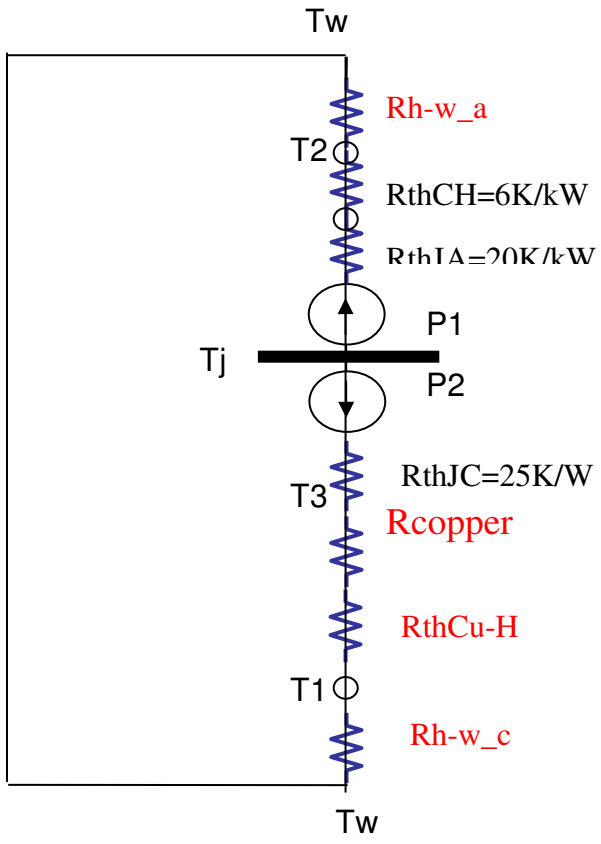


Figure 2-7. The thermal resistance network of the ETO

Following are the different component thermal resistances of the thermal network of the ETO:

- Junction to anode, RthJA
- Junction to cathode, RthJC
- Copper, Rcopper
- Case to anode heatsink, RthCH
- Heat sink to water on anode and cathode side, Rh-w_a and Rh-w_c respectively
- Contact resistance from copper to heat sink, Rthcu-h

Of all the thermal resistances mentioned above, the ones in Figure 2-8 in red are unknown to us, and the tests were basically targeted at getting experimental values for the same. From the datasheet of the ABB GTO, we can get numbers for the first two thermal resistances. We can see that the thermal resistance from the junction to the case for double sided cooling is not the same on the anode and the cathode side. It is 20K/kW on the anode side and 25K/kW on the cathode side. Also, the data sheet gives us information on the contact resistances between the cathode and anode with the heat sink. It is 6K/kW on either side of the junction. As we can recall, the ETO has two copper plates on the cathode side, below the GTO, which would obviously have their own thermal resistances. Also, the thermal resistance of the heatsinks to water on both sides of the junction needs to be found out. P1 and P2 represent the power (heat) flow in the two directions from the switching junction. These two are not identical since the thermal network is asymmetric about the junction. The junction to case thermal impedance is about 12.6K/KW for double sided cooling for the GTO, as mentioned before (from the datasheet). Tests are done at different power loss levels on the ETO in the boost converter set up, and temperatures are recorded at steady state. One such test and its results are shown in the following lines:

Power loss = 2.75kW = P1 + P2

T1 = 55 °C

T2 = 88 °C

T3 = 79 °C

Tw = 32 °C

Also, the values of Rh-w_a and Rh-w_c can be obtained from the data sheet of the heatsinks as shown in Figure 2-9. This figure shows us a plot of the thermal resistance of the heat sink from case to water, as a function of the flow rate of water. The important thing is the contact area of the heatsinks with the ETO. The thermal resistance of the heat sink shown in this plot is valid assuming a complete area contact with the device being cooled.

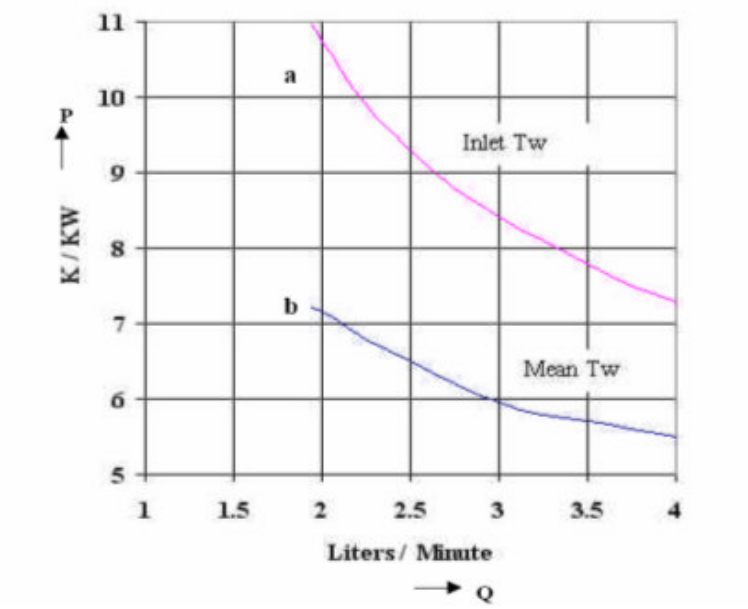


Figure 2-8. The thermal resistance plot of heat sink versus flow rate of water through it

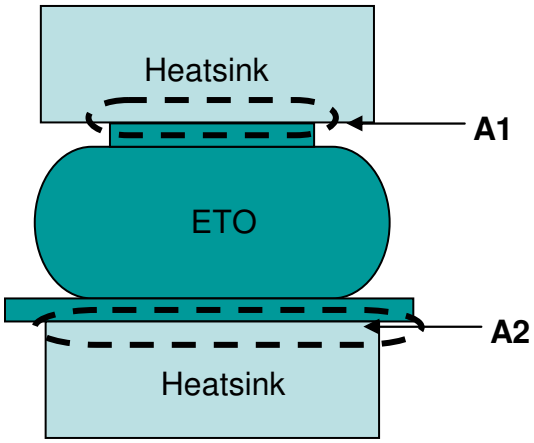


Figure 2-9. Different contact areas of heat sinks with anode and cathode side of ETO

The GTO has a contact area that is smaller than the actual diameter of the device. This means that the GTO's contact area is much smaller than the contact area of the heat sink. The diameter of the GTO's contact on the anode side is 72mm, which implies an area A1 of 4096 square mm. The diameter of the heat sink's contact area is 108mm, which means an area A2 of 9156 square mm. we see that A2 is approximately twice that of A1, as seen in Figure 2-10, and hence the associated thermal resistance should be half on the cathode side. Since the cathode side has a full contact area, we can obtain the thermal resistance of that heat sink from the curve in Figure 2-10 as 20.5K/kW. This is also verified experimentally, from the values of temperatures T1, T2, T3 and Twater, as:

Rh-w_a = 20.54K/kW

Rh-w_c = 10.2K/kW

From the values of temperatures at different measurement points, we can get the following results:

P1 = 1.46 kW

P2 = 1.29 kW

Rcopper = 15.5K/kW

The value of Rthcu-h, i.e. the thermal contact resistance from the copper plate to the heat sink is clubbed with Rcopper. So Rcopper is not only the thermal resistance of the Copper itself as a material, but also includes resistance to heat flow provided by contact non -uniformities. All the above mentioned values are then fitted into the thermal model to obtain the thermal network. When all these values are put together, we obtain the thermal resistance of the water cooled heat sink from junction to ambient as **24.7K/kW**. The important observation here is that heat flows unequally from the junction to the two sides, that is the anode and the cathode, with more heat flowing towards the anode side. The ratio of P1 and P2 in fig. xx is 1.13. Thus, heat through the anode side is 1.13 times that flowing through the cathode. The thermal model is shown in fig. 13, and this can be very effectively used in order to predict the operating junction temperature of the ETO at steady state. This can be made possible once we know the power loss through the ETO, and any two of the temperatures T1, T2, T3 or Tw. Typically, the value of Tw can be directly read off from the digital display on the chiller. So all we need is one thermocouple, and a means to integrate the voltage and current to find power loss, in order to obtain the operating steady state junction temperature. In the figure below, P1 and P2 represent the heat flows from the junction toward the anode and cathode respectively. So we can back-calculate the junction temperature from the basic thermal equations. We can then use the thermal resistance in order to determine the maximum allowed power dissipation on the ETO, while keeping it under the 125 °C mark of operating junction temperature. Let us assume an inlet water temperature from the chiller into the heat sink as 30 °C. Then, we get the allowed ΔT as 95°C. So we can now get the power loss as 95/24.7 that is 3.86kW. This number can obviously be increased if we were to

operate the chillers with cooler inlet water for the heat sinks. The final thermal network of the ETO is shown below in Figure 2-11.

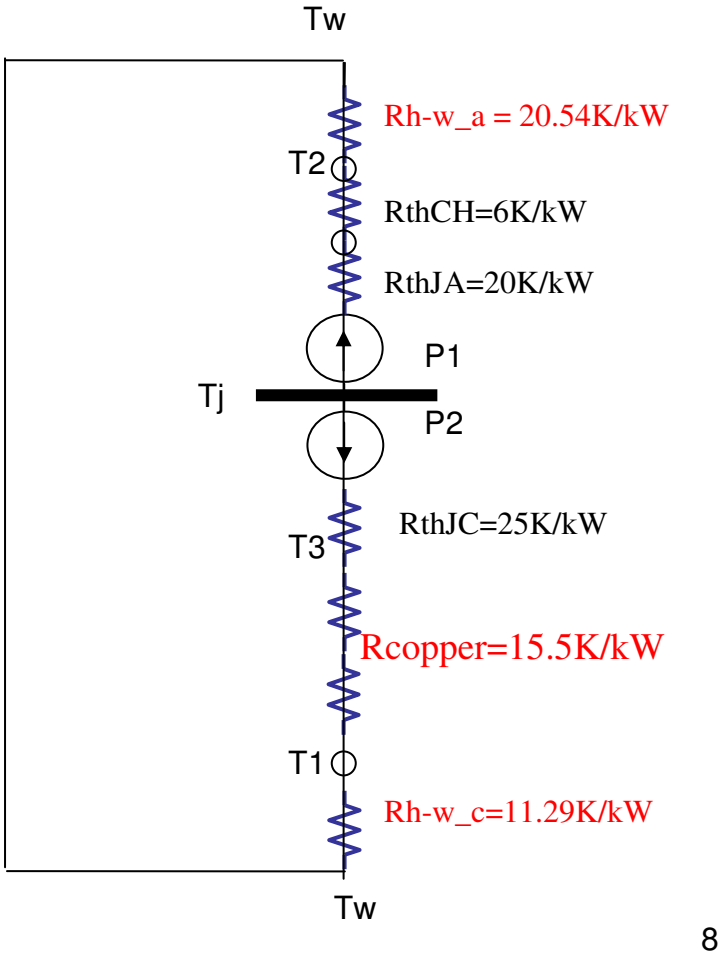


Figure 2-10. Thermal resistance model of the ETO

2.3 Thermal Stability

In order to study the high temperature stability, we shall use equation (8), which states that the change rate of total loss should be less that the thermal conductivity, for thermal stability, as highlighted previously. In other words, the heat being produced due to the losses should be carried out of the junction avoiding build up of temperature. Hence, plots of dp/dt times Rth were constructed using the data gathered from loss curves that were made experimentally in chapter I. These are shown in Figure 2-12. It is seen that the product of dp/dt and R_{th} remains almost constant at lower temperatures, and below numerical value of 1. As the temperature rises, these curves cross over the line y=1, indicating thermal instability. At this point, the increase rate or loss with temperature becomes too high. The level of heat becomes higher than the capability of the cooling system to carry away the heat. The important point here is that the operating conditions of the ETO in the Boost converter are the same as in the previous chapter. (Vdc=2kV, f=1.0kHz, Ipk=1.0kA)

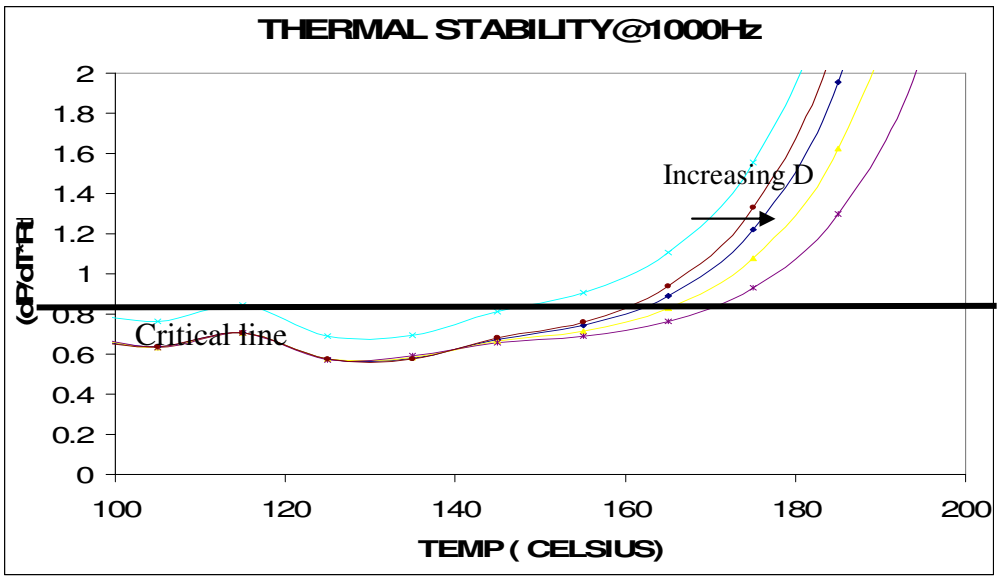


Figure 2-11. Plots of (dP/dt)Rth at various Duty cycles

The intersection of point with ($\frac{dp}{dt}R_{th}=1$) (critical line) gives the maximum operating junction temperature for the ETO under different duty cycles for 1000Hz operation. At duty cycle of 0.2, it is seen that the intersection point is at 175 degrees Celsius. This implies that the device under those conditions would operate under thermally stable conditions up to 175 degrees Celsius. As the duty cycle is reduced, the curves shift toward the left, and at a duty of 0.05, maximum junction temperature reduces down to 165 degrees Celsius.

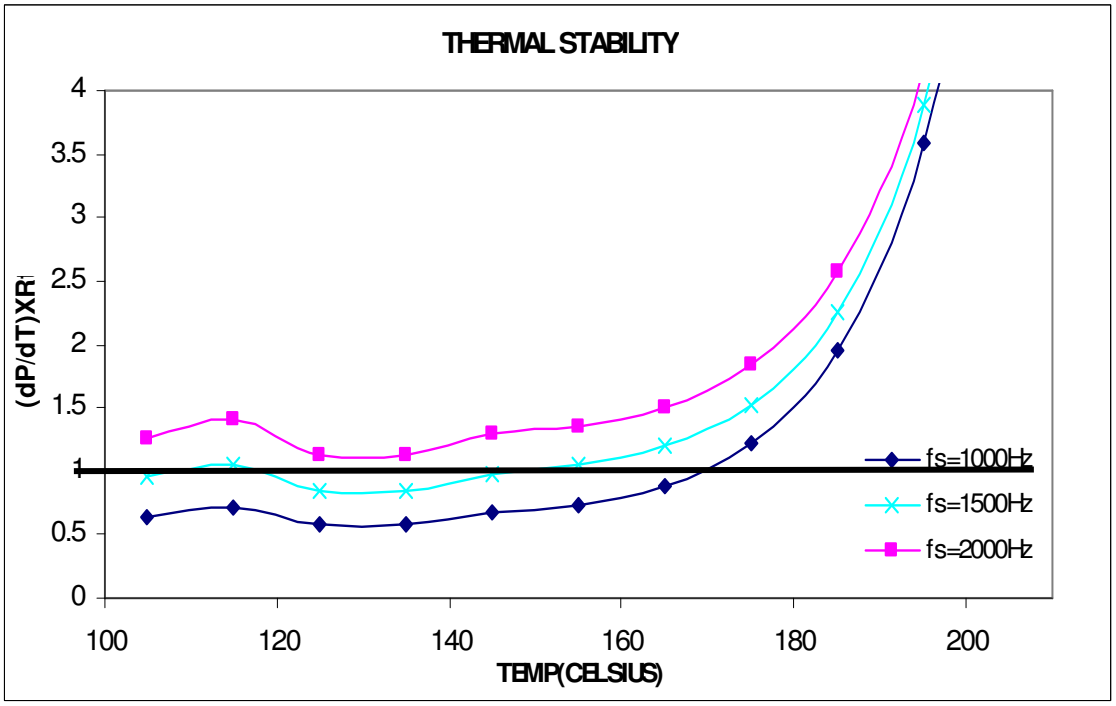


Figure 2-12. Plots of (dP/dt)Rth at 1KHz,1.5kHz and 2KHz frequencies

The region of the curves beyond the point of intersection with the horizontal line represents thermal runaway condition, that is, more heat is produced within the junction of the ETO, than can be taken out through the thermal conductance.

If the switching frequency is increased, it leads to more compact passive elements and better electrical performance [8,9]. Increase in switching frequency has a direct impact on the total loss, as the switching loss is proportional to the switching frequency (equation (6)). The maximum junction temperature at which the device can operate thus reduces significantly with rise in frequency. As shown in Figure 2-13, Tjmax shifts from 175 degrees at 1000 Hz, to less than 100 Degrees at 2000Hz. Hence for high temperature operation, it is desirable to keep the switching frequency around 1000Hz, or lower for better performance.

2.4 Experimental demonstration of high temperature operation capability of ETO

In order to prove the high temperature operation capability, tests were done on the same Boost converter at 2kV, 1kA, 1kHz and 0.02 duty at discontinuous mode operation. The losses were high because of the high output voltage and output current of the ETO. The losses were slowly increased step by step as shown in Table II. The flow rate was kept fixed at 2LPM. The temperature measurement points were kept the same as mentioned before, that is the cathode and anode of the GTO and the cathode of the ETO, using thermocouples. Loss was measured using Textronic oscilloscope. So the input voltage from the high power DC supply that is used with the boost converter is increased step by step and thus the output of the converter also increases step by step. In the process, as seen in the table, the loss also increases, and the converter is operated in each step until steady state operating temperature is reached, and the temperature is recorded. Figure 2-13 shows the turn off waveform of the ETO in the converter. The measured losses were 5.2kW and the steady state operating junction temperature reached 160 degrees Celsius.

Table II. Operating conditions during a series of high temperature testing on ETO

Vout(kW)	Iout(kA)	FlowLPM	Tanode	Tcathode	Tcopper	Tw	Loss(kW)	Tj
1.6	.76	2	79.2	77	53.3	32	3.0	119
1.8	.82	2	84	78.4	49.1	28	3.4	130
1.95	.92	2	91	85	51.9	28	4.5	136.1
2.0	.97	2	97	91	55	30	4.75	147.5
2.12	1.00	2	104	96.7	57	30	5.25	160.1

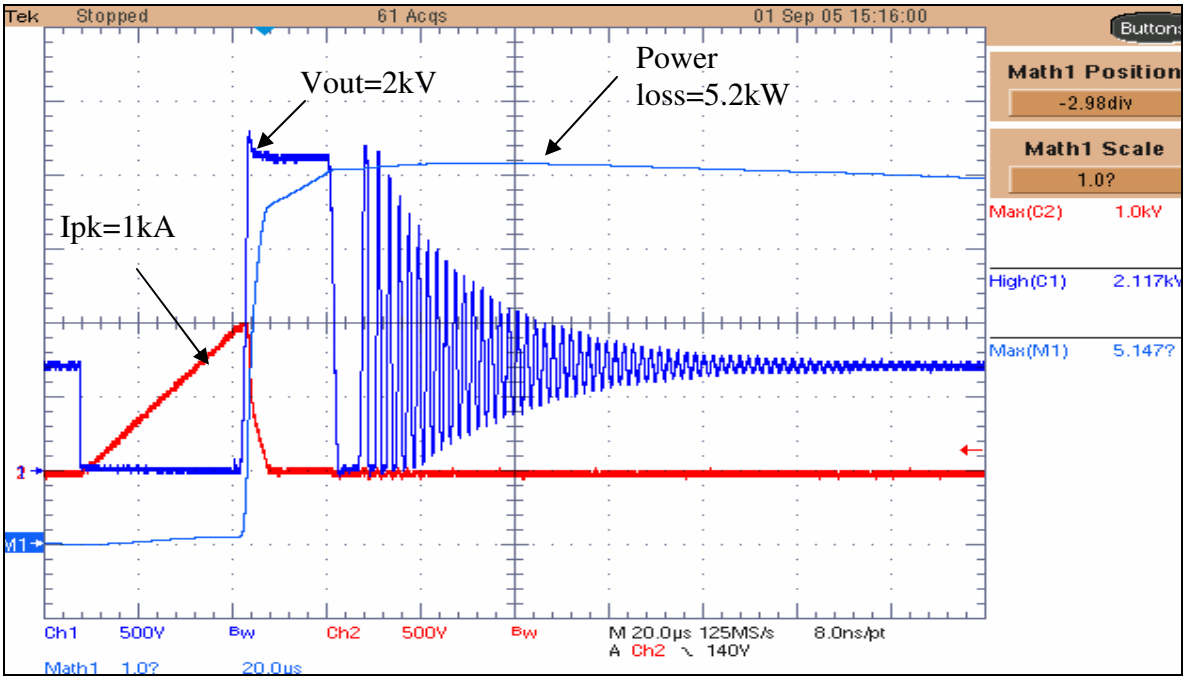


Figure 2-13. Switching at 2kV, 1kA, 1 kHz in the Boost Converter

In addition to steady state recording, dynamic measurements were also done on the cathode temperature of the ETO, with a given power loss. As shown in Figure 2-14, at time t=0 a power loss of 4.2kW was subjected on the ETO. The temperature is recorded until it reaches steady state. From the steady state temperature of the cathode and the power loss, we can then obtain the junction temperature at this level since we know the thermal resistance. At 4.2kW, the steady state junction temperature reaches 120 °C. At this point, the power loss is increased further to 4.5kW, and the temperature of the cathode takes about 4.5 minutes to settle to steady state. At this point, the junction temperature reaches 134 °C. After this the converter is shut down, with water still flowing to cool down the devices, and we can plot the cooling curve of the ETO.

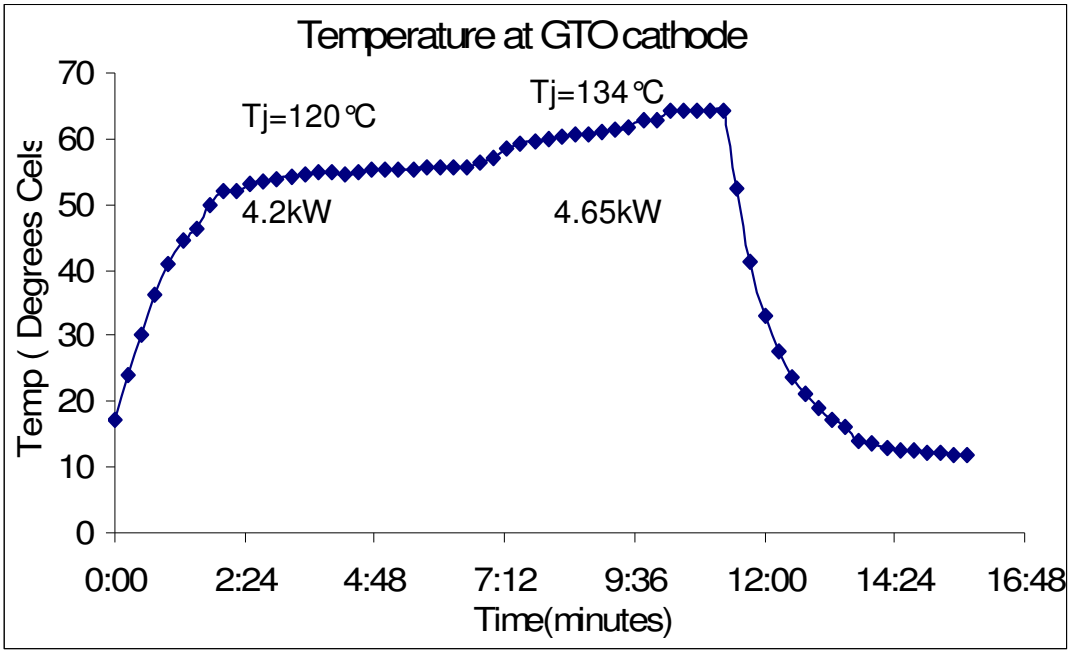


Figure 2-14. Instantaneous temperature profile of ETO at GTO cathode at different power loss levels

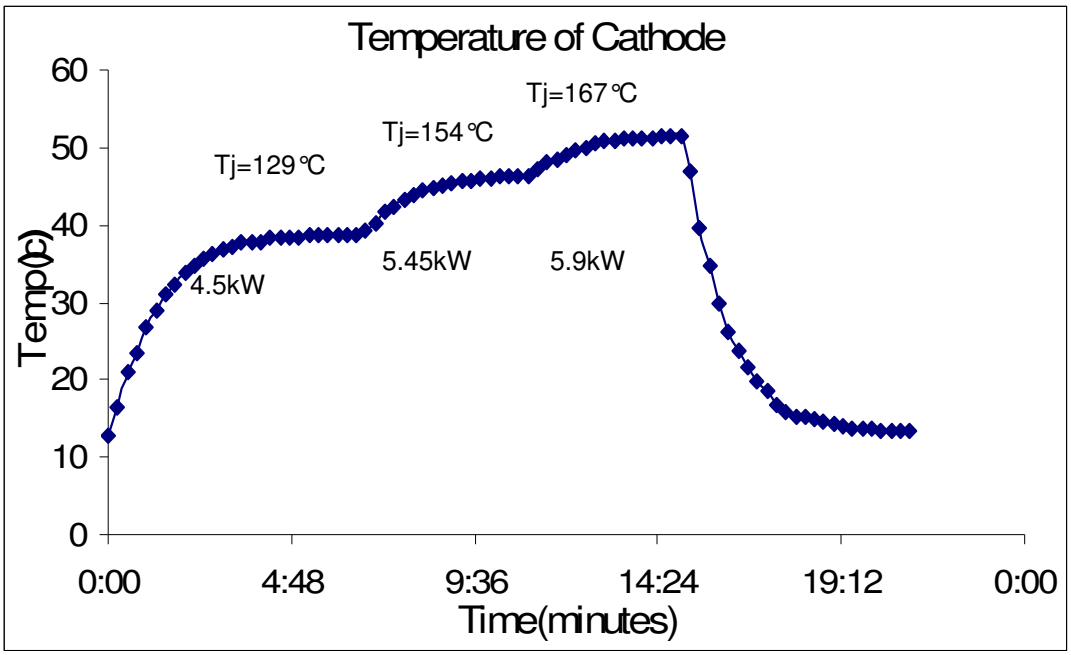


Figure 2-15. Instantaneous temperature profile of ETO cathode at different power loss levels

The test is then done with higher power loss as shown in Figure 2-15. The temperature is plotted for losses of 4.5kW, 5.45kW and 5.9kW. It is seen that the temperatures plotted in the curve of Figure 2-14 are much higher in comparison to the temperature of the cathode in curve of Figure 2-15. For example, at power loss of 4.2kW, the temperature of the cathode of the GTO used in the ETO is around 55 °C at steady state, and at a much higher power loss of 4.5kW, the temperature of the bottom copper plate of the ETO (which is the cathode) is much lower, around 40 °C. This is because of the higher thermal resistance from the bottom copper plate to the switching junction, which implies higher temperature drop. An important thing to be noted here is that the power loss numbers shown in these two curves of figures 2-14 and 2-15 are losses obtained at steady state. Before steady state is obtained, the power loss is little less, and slowly

increases with increasing junction temperatures. This can be understood if we go back to Figure 1-24 which shows the variation of power loss with temperature.

We can see that in Figure 2-15 the junction temperatures for the loss numbers are 129°C, 154°C and 167°C respectively. The ETO operates at the high operating junction temperature of 167°C for a long duration of time successfully. This demonstrates the successful high temperature operation capability of the ETO. At this point, the device is still thermally stable since the product of change rate of losses with respect to temperature and the thermal resistance is less than one.

2.5 Failure of ETO in High Temperature Operation

The ETO was being subjected to continuous thermal cycling as part of the research on high temperature operation of the device that is alternate heating and cooling periods. In one test among a series of such tests, the ETO was subjected to a power loss of 5.65kW, with the aim of reaching a high operating junction temperature. The various conditions of this test are highlighted below as operating conditions of the device:

- Vout = 1.95kV
- Ioutpeak = 877A
- Switching energy = 4.8J
- Switching frequency = 1.16 kHz
- Power loss = 5.65kW
- Water cooling temperature = 11°C

The curve showing the temperature at the cathode is given below in Figure 2-16. It is seen that the temperature at which the ETO fails is a cathode GTO temperature of 72 °C. With a power

loss of 5.65 kW, we can calculate the heat flow towards the cathode side from Figure 2-10 of 2.8kW. The thermal resistance of the ETO from the cathode of the GTO to the junction is about 30K/kW, including contact resistance. So we can calculate the junction temperature at the fail point as (30*2.8 + 72) which is 156 °C. The temperature profile seems to be flattening out just as the failure occurs. This could indicate absence of thermal runaway, but does not completely rule it out, since sudden change in junction temperature might not reflect as a rise in cathode temperature.

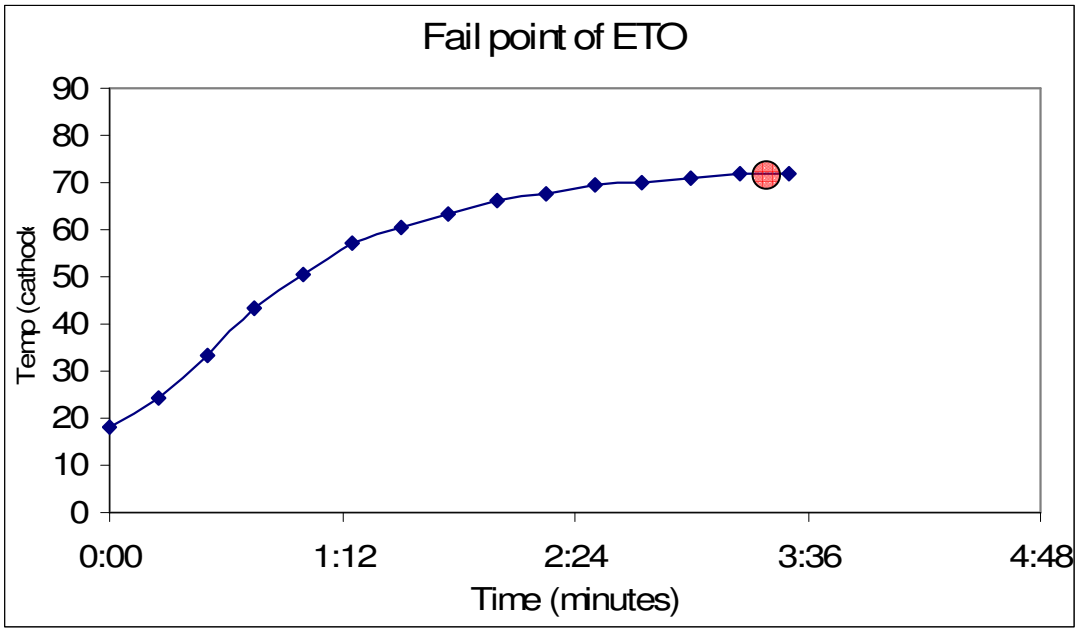


Figure 2-16. Temperature rise before failure of ETO in high temperature test

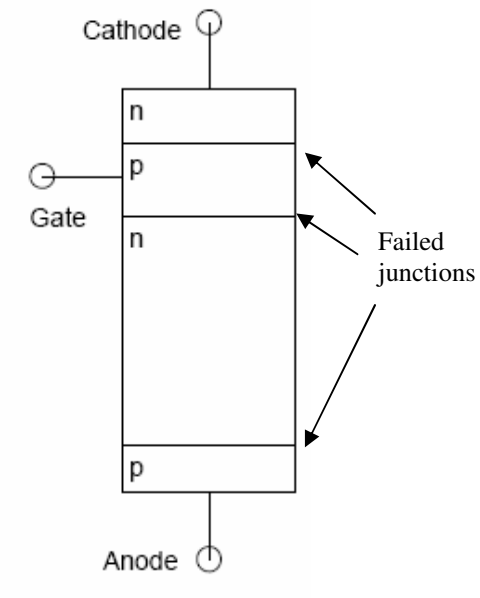


Figure 2-17. All three junctions on the GTO failed during the test

It was observed that all three p-n junctions on the GTO were failed short during the failure of the ETO. The failure can be attributed to thermal stress that the ETO was subjected to during the high temperature testing that involved fast heating and cooling periods. Pressure distribution on the boost converter stack also needs to be very even and near 40kN of force, in order to ensure proper operation. There is also a need to use accurate temperature sensing and recording methods to ensure right results.

CHAPTER 3

High Power Voltage Source Converter for FACTS Applications

3.1 Introduction

Multilevel voltage source converter structure has been developed to overcome inadequacy in power semiconductor voltage ratings so that they can be applied to high-voltage electrical systems such flexible AC transmission systems (FACTS) and custom power system applications [10]-[12]. As shown in Figure 3.1, there are three well-known multilevel voltage source converters; these are the diode-clamped converters, flying-capacitor converters and cascaded converters with separated dc sources. In reactive power compensation, the cascaded converter with separated dc capacitors is the most feasible topology for many reasons [13]. For the same number of output voltage levels, the number of main switches and main diodes is the same for all three topologies. The clamping diodes and balancing capacitors, however, are not needed in the cascaded multilevel converter. The cascaded converter, therefore, requires fewer main components. Moreover, the cascaded converter has the same structure for each level; the desirable power rating of the system can therefore be simply adjusted by connecting a different number of the identical modules.

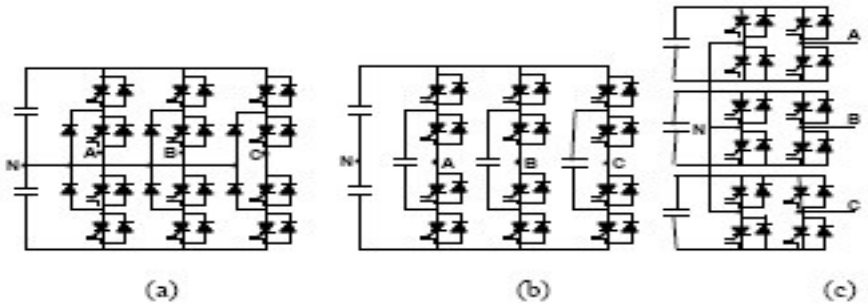


Figure 3-1. (a) Diode-clamped, (b) flying-capacitor and (c) cascaded converters

This makes the modular concept possible and makes the entire converter structure simple to implement. On the other hand, in the cases of diode-clamped and flying-capacitor converters, the same layout cannot be used for different power ratings because they need extra clamping diodes and voltage balancing capacitors, respectively. For multilevel voltage source converters, to achieve sinusoidal-like voltage waveforms as well as desired power capabilities, there are three possible approaches. Firstly, to keep the same switching frequency for all levels, more dc power sources are required to decrease the total harmonic distortion (THD) in the output waveforms. This approach minimizes the switching loss of the semiconductor devices, as well as the output voltage THD of the converter system. The second approach is to keep the same number of levels and to increase the switching frequency. The key requirement for this approach is to achieve improved system response where the switching loss is no longer a major concern. The last approach is to adjust both the number of levels and the system switching frequency. This approach can be specifically optimized for a given system. Practically, the first approach is suitable in high-voltage applications such as transmission power networks, which is preferred the high-power, high-voltage power electronic system with limited system response. On the other hand, in distribution power networks, fast-response medium-voltage power electronic systems are more attractive. Based on the different power levels of the applications, the cascaded multilevel converter is obviously the most preferable topology because of its flexible hardware configurations. Figure 3-2, for example, shows a STATCOM system using a seven-level cascaded converter.

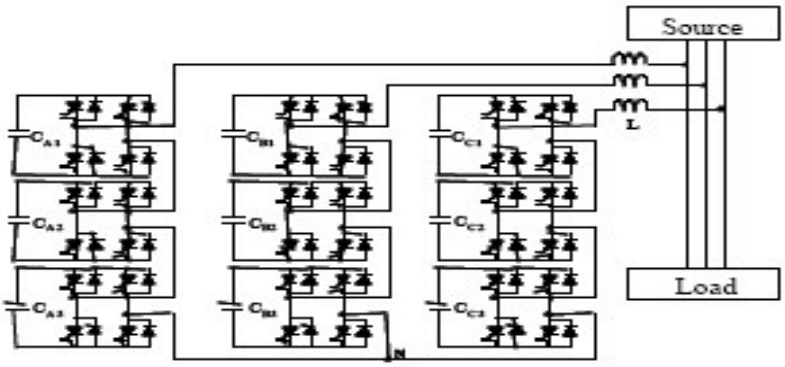
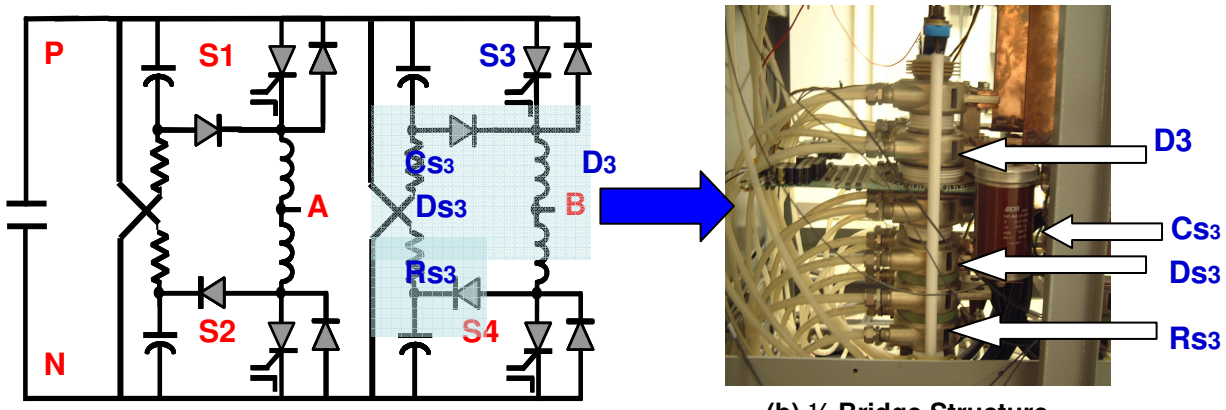


Figure 3-2. STATCOM system using a seven-level cascaded converter

3.2 The Modular Voltage Source Converter (H-Bridge Building Block-HBBB)

In order to realize the above mentioned converters, more specifically the cascaded multi level converter, a voltage source converter with a modular design is implemented. The circuit diagram for the H-Bridge structure based voltage source converter is shown below. The structure is made up of four ¼ bridges, each of which is a stack consisting of one ETO device, its anti parallel diode, the RCD clamp, and water cooled heat sinks to provide the required cooling to remove heat generated by losses in the system.



(a) Structure of the modular VSC

(b) ¼ Bridge Structure

Figure 3-3. The H-Bridge Voltage Source Converter

It is clear from Figure 3-3(a) that an HBBB, which consists of an H-bridge converter and a dc power source, is a common part in a high-power application using a cascaded converter. The specifications for the power stage of the proposed ETO-based H-bridge converter are tabulated in Table III.

Table III. Power stage specifications of HBBB

Main Device (ETO)	4kA/4.5kV ETO
Bus Voltage	2kV
Output rms current	1kA
Switching Frequency	1kHz
Power Capability	1.5MVA

At the full load, the H-bridge converter is capable to operate at the bus voltage of 2 kV and output rms current of 1 kA. The power capability is approximately 1.5 MVA and is determined by the thermal and electrical capabilities of four 4kA/4.5kV ETOs. Although the ETO has the snubberless turn-off capability, a small dv/dt snubber circuit is required to reduce the switching loss and to increase the long-term switch reliability. Because of the poor performances of a high-power diode, its reverse recovery increases the stress on the ETO. As a result, the di/dt is needed to reduce such switch stress. The schematic of the proposed H-bridge converter with dissipative snubber discharge and a dc capacitor is shown in Figure 3-3. S1 to S4 are the main switches, which are the ETOs, and D1 to D4 are the main anti-parallel diodes. The snubber circuit

proposed by McMurray [14] is comprised of dv/dt capacitors CSN, di/dt inductors LSN, auxiliary diodes DSN, and discharge resistor RSN, where N ranges from 1 to 4. To optimize the HBBB structure, several considerations are needed to be concerned. The building-block concept is applied to the layout of the HBBB so that it can be simply manufactured. To achieve high-power density, the designed layout is as compact as possible. To minimize the voltage overshoot in the output waveform resulting in the main switch voltage stress, the stray inductance in the layout must be kept as small as possible. Hence, the H-bridge converter must be as close to the dc capacitor bank as possible. Likewise, the capacitor snubber loop is needed to be as small as possible. To simplify the structure of the building block, the Hbridge circuit shown in Figure 3-3 is divided into four identical ¼ H Bridges. The structure of the ¼ H Bridge shown in Figure 3-3(b), for example, consists of a main switch S2, an Antiparallel diode D2, a snubber capacitor DS2, and a discharge resistor RS2. To form an H-bridge converter, four ¼ H-bridge stacks are electrically connected by copper bus bars. A dc capacitor bank and snubber inductors are then connected to the H-bridge converter to complete an HBBB, as shown in Figure 3-4. For reactive power compensation, the dc sources in the HBBB mainly supply or absorb only the reactive power between the power system and the converter; therefore, there is no need for dc power supplies other than dc capacitors. The voltage source converter discussed above needs cooling for its various components, and the cooling system is designed using water based heat sinks, that are connected to water to water heat exchangers. There is elaborate piping between these heat sinks as can be seen in Figure 3-4. The heat exchangers or chillers are connected to external heat exchanger which transfers the heat from the water to the outside air. A total of 3 chillers are needed for three voltage source converters for a three phase system as shown in Figure 3-5. The characteristics of the chillers have been discussed in Chapter 2 in Figure 2-5.

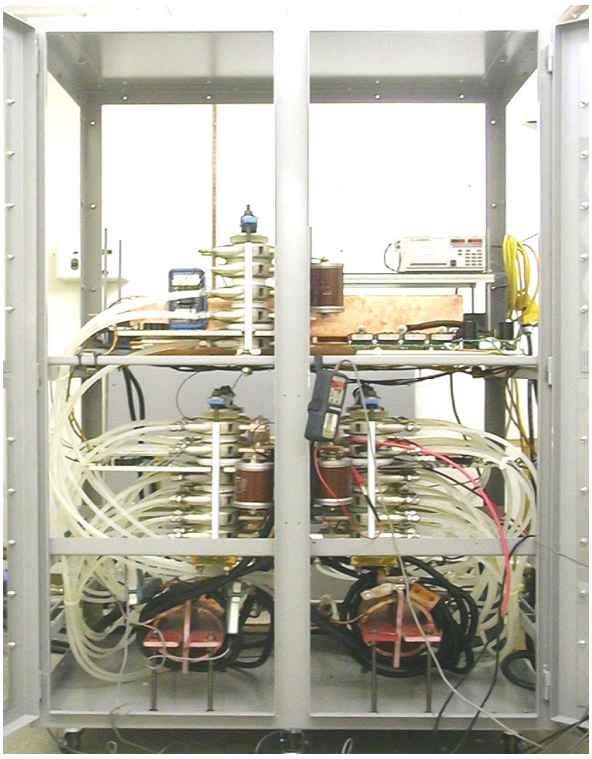


Figure 3-4. The complete H-Bridge Voltage Source converter

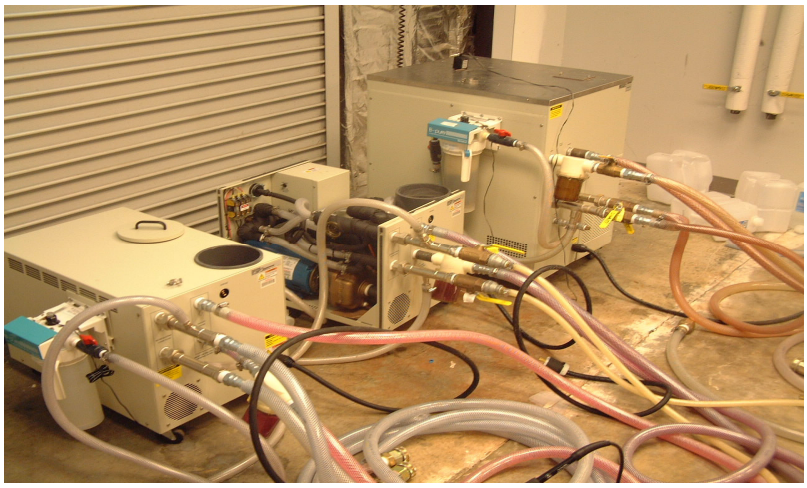


Figure 3-5. The three chillers needed for a three phase voltage source converter

3.3 Possible areas of Improvement

3.3.1 DC Power Supply

The four ETOs in the Voltage Source Converter need a DC power supply for their gate driver board. Also, the current sensors that are used in the Voltage Source converter need a DC power supply for their operation. This DC power is produced by using AC/DC converters on the VSC itself. This DC power is then chopped using a chopper board on the VSC. In order to make sure there is a good amount of isolation between the VSC and the AC supply, there is a need for isolation transformers. These isolation transformers are placed on the VSC. These three components, namely the AC-DC converters, choppers and the isolation transformers shown in Figure 3-6 are costly and also bulky equipment. This increases the overall cost and volume of the Voltage Source Converter. If there is a way that can eliminate the need for all these, that would result in a much more compact and reliable design.

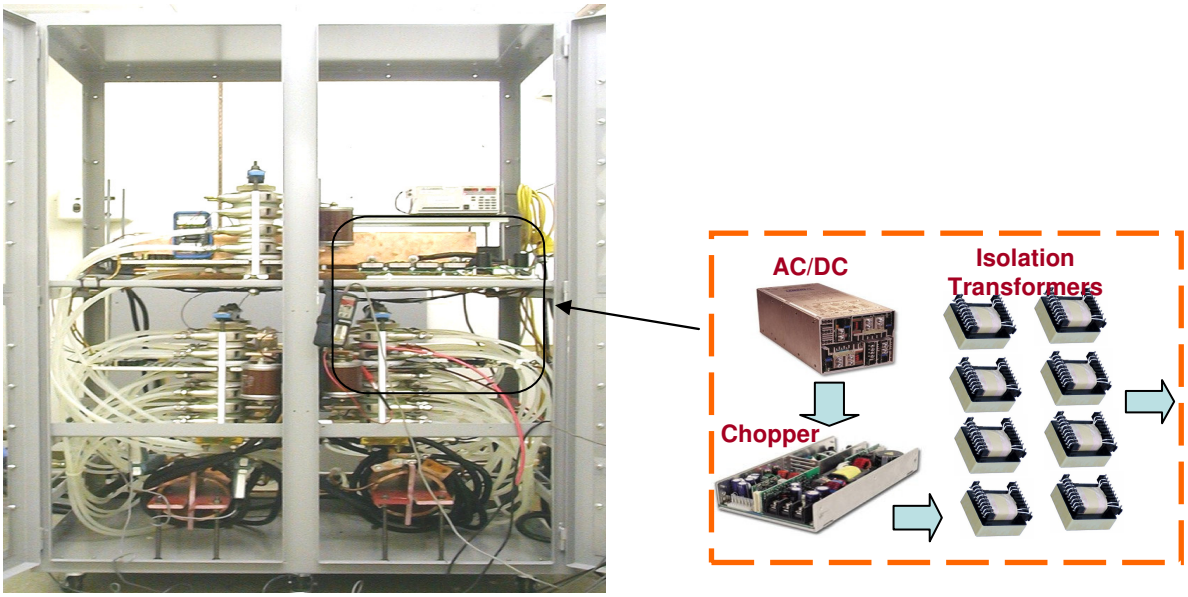


Figure 3-6. Dc power supply in Voltage source converter

3.3.2 ETO based DC Circuit Breaker

Due to its fast switching speed, snubberless turn-off capability and built-in current sensing, the ETO is a superior high-power semiconductor device suitable for the applications in dc circuit breakers. Like a high-speed fuse in a high-power system, the ETO-based dc circuit breaker is installed between the energy storage component and the positive bus bar of the HBBB, as shown in Figure 3-7. Without the over-current protection, if a shoot-through fault occurs in the phase leg, say, of switches S1 and S3, the energy on the dc bus capacitor will be dumped through these two switches. The switches as well as the dc capacitors will probably be destroyed because the fault current increases very rapidly to an extremely high level, at a rise rate dictated only by the bus voltage and di/dt snubber inductance. With the dc circuit breaker, once the fault current reaches the threshold level, the over-current protection is triggered and the fault current is cut off after a delay time. The Solid state circuit breaker occupies a lot of space, means additional cost, and also makes cooling system requirement

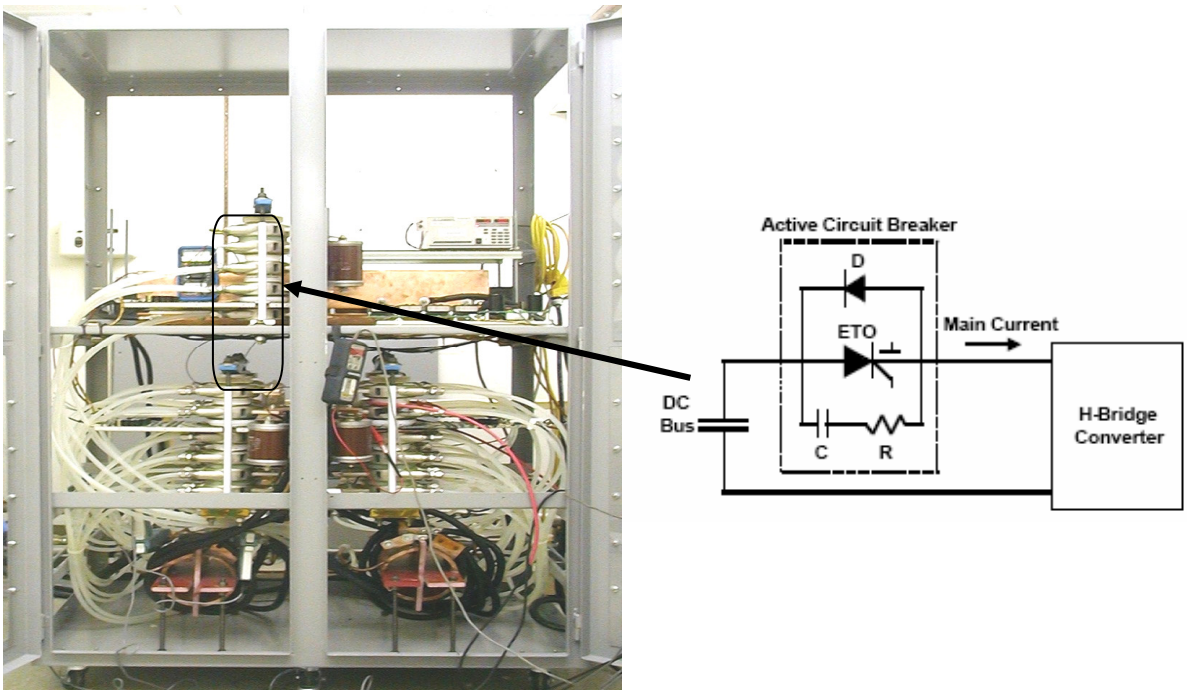


Figure 3-7. Solid State Circuit Breaker in Voltage source converter to protect VSC against Shoot through fault

elaborate. If we could eliminate this circuit breaker, and at the same time cater to the risk of a shoot through fault through the phase leg of the Voltage Source Converter, then it would mean a lot of saving in terms of cost and volume.

3.3.3 RCD clamp and di/dt snubber

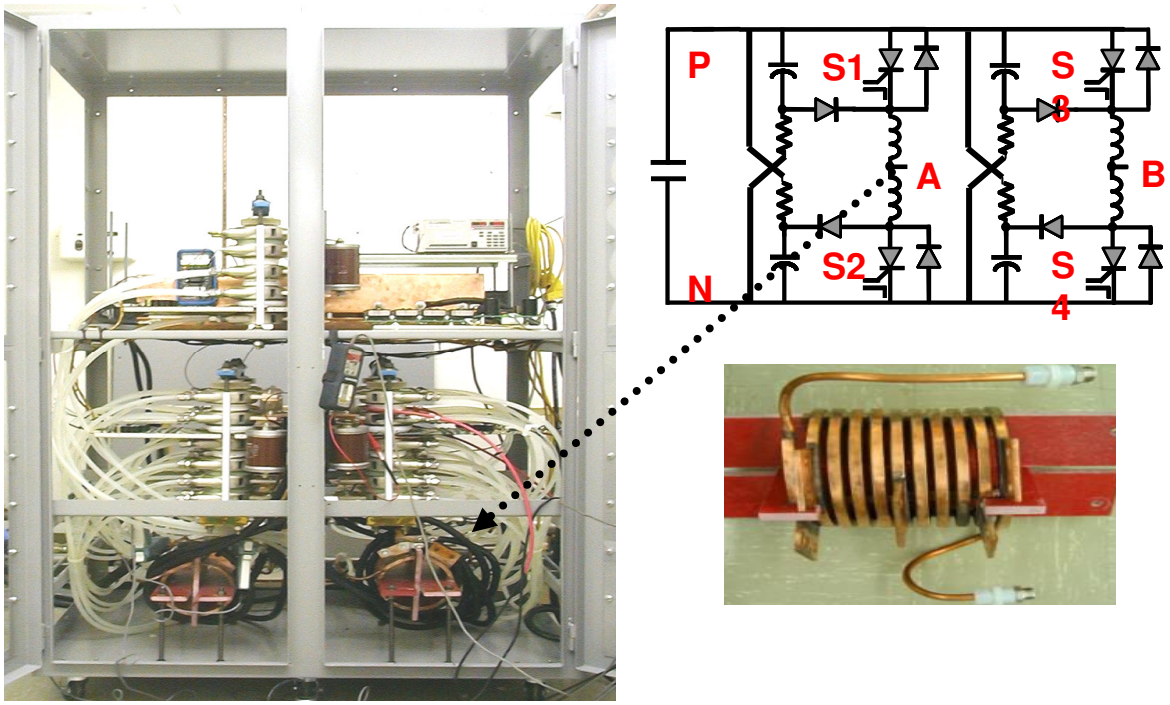


Figure 3-8. di/dt snubber in Voltage source converter

As mentioned earlier, a di/dt snubber is needed in order to control the di/dt during turn on, on the diodes. The ABB diodes can typically withstand di/dt ratings of around 800A/us. So, we make use of inductors for each diode. The inductor used is an air-core inductor, which offers many advantages over its counterpart such as iron core. Some of the advantages are fewer losses, lighter weight and less interfering EM field radiation. The only issue is that in this present VSC design, we are using 4 inductors in total. The actual implementation involves use of two big inductors, and each of these is divided into two parts, one for each stack. Also, these inductors are water cooled and need water pipes to feed in and take out the water. If we could somehow

use just one inductor as a di/dt snubber instead of four, which would greatly reduce the size of the VSC. Also, it would be highly desirable to use an air cooled inductor instead of a water cooled one. All this would give a more compact and efficient design. Another important and possible area of improvement comes into the picture if we take a look at the RCD clamps in the present VSC. These clamps, comprising of a resistor, a diode and a capacitor are used in order to clamp the voltage across the ETOs such that over voltage across the ETO during turn off is controlled. Four such clamps are used, one for each ETO, as shown in Figure 3-9. The VSC design is such that there are 4 quarter bridge structures, each with one switch and its other components such as clamp and Anti parallel diode. One possible major improvement could be the reduction of the number of clamps that we have from 4 to 1. In other words, if we use just one RCD clamp for all four ETOs, we could greatly reduce the size of the converter. A look at the figure below tells us that if we remove the resistors, diode and capacitor from the stack, the size of the stack would get reduced by half. Then we could use only 2 stacks instead of 4, leading to great improvements in terms of size and cooling requirements.

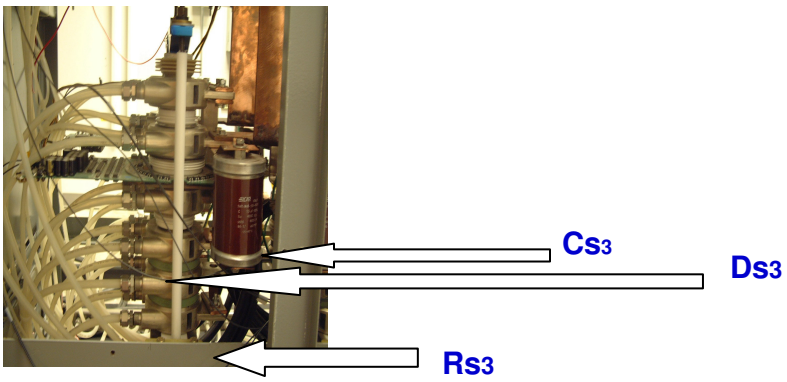


Figure 3-9. ¼ Bridge Structure and RCD clamp

3.3.4 Voltage and Current Sensors

As mentioned before, there are voltage and current sensors mounted on the converter to aid in the status feedback and digital control of the VSC. These sensors occupy space and are expensive. The current sensors also need a DC power source for their operation. Elimination of these sensors would lead to great improvements in design.

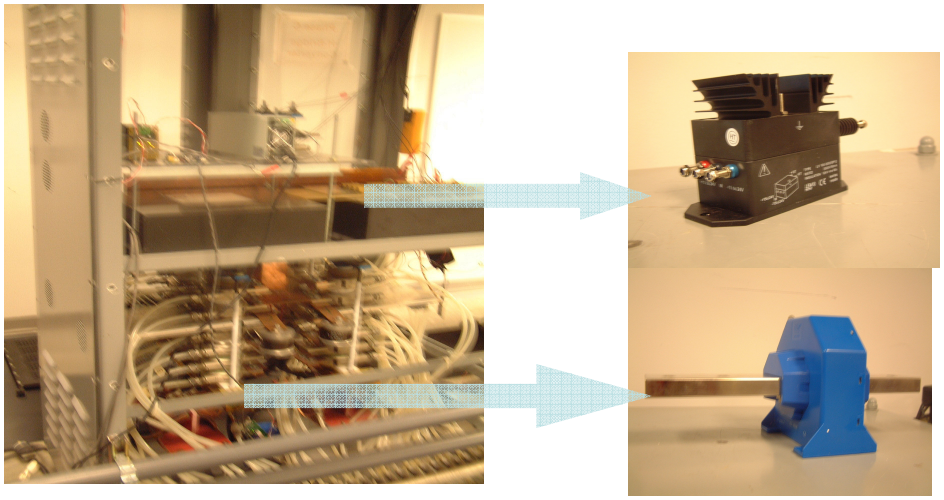


Figure 3-10. Voltage and current sensors in water cooled VSC

3.3.5 Cooling System

The most important area of consideration is the use of water cooling versus air cooling methods. Traditional water cooling methods are used widely across industry and businesses because of the good thermal resistances and low cost. However, water cooling has several drawbacks associated with it such as:

- Need for a chiller and heat exchanger
- Elaborate pipes
- Need for isolation between power electronics and water

- Large volume consumption
- Related maintenance issues
- Use of de ionized water
- Leaks and associated problems

All of the previously mentioned problems can be taken care of, if we go for a simplified air cooling system. There is hence a need for an air cooled heat radiator or heat sink that can meet the thermal requirements of traditional water cooled system. The heat sinks should not be too large as to make their use impractical in voltage source converters. Conventional fans should suffice in taking heat away from the radiators. There should be no maintenance issues involved with the heat sinks and radiators. Just simple air cooled heat sinks mounted on the ETOs and diodes is not a very feasible idea since that would have enormous size constraints. So, as we shall see in the next section, in order to facilitate all the above mentioned requirements, and obviate the traditional problems associated with both air and water cooling, we go for cooling using **Heatpipes**. Heatpipe has a lower total thermal resistance than solid conductors, enabling them to transfer heat more efficiently and evenly. It's totally passive heat transfer system, having no moving parts to wear out and requiring no energy to operate. Heat from the electronics is absorbed by the heatpipes and transported to the fins which are cooled by natural or forced convection.

Also, in order to facilitate all other possible improvements mentioned before, the newly developed generation 4 ETO is used. This is elaborated in the next chapter.

CHAPTER 4

Design of Heat pipe based Voltage Source Converter

4.1 Introduction

Multilevel converters have become an important technology in high-power applications, especially for Flexible AC transmission system (FACTS) applications. Several multilevel converter topologies have been developed to demonstrate their superiority in high-voltage applications ([14]-[17]).

In this section, a high power (megawatt range) modular Voltage Source Converter (VSC), using the newly developed Emitter turn-off (ETO) Thyristor ([18], [19]), is proposed and a design methodology is developed for the various parameters of such a system. One of the main constraints in the design of such a system is essentially the design of the cooling system to carry the large heat generated by the various components such as switches, diodes and passives. Conventional systems employ water based cooling systems to achieve the goal. Such a system imposes many limitations on the structure such as need for good isolation, elaborate pipes, expensive heat exchangers and maintenance.

In this chapter, design of a new cooling system is presented that is based on the air cooled heat pipe system, and offers many advantages. Through the use of heat pipes, we can avoid the electrical isolation issue of cooling system in high voltage FACTS application. The heat pipe also helps to increase the VSCs efficiency, power density and reliability, and we can do away with the cumbersome and elaborate water cooling system. The hardware configuration, thermal calculation as well as component selection and design are presented in this paper. Based on the electrical configuration of the new VSC, loss calculations are done under different operation

modes for components such as ETO and diodes, and the heat removal capability that is required from the heat pipes is determined. 3D Finite Element simulations are done on ANSYS software to understand the working and the selection of heat pipes. Electro-thermal simulations are done using thermal resistances of various components of the half bridge structure that is used including the thermal resistance of heat pipes that is obtained from tests, to validate the thermal design. The key to the overall design is to ensure a steady state operating junction temperature of ETOs under 125°C for maximum reliability. Heat pipes are custom-manufactured from Bosari after preliminary design and analysis, and tested to prove their heat carrying capability. Thermal impedance (R-C) network for the ETO is developed to aid in thermal management, which is proposed to be integrated in the overall design. Finally, AUTOCAD is used to develop the overall structure of the modular VSC with the fans used to cool the heat pipes.

The proposed modular VSC can be used to form a cascaded multilevel converter for reactive power compensations such a Static Var Compensator (STATCOM) and a static synchronous series compensator (SSSC). By electrically connecting these identical building blocks, the cascaded multilevel converter topology can be easily implemented. Thanks to their identical layouts, the VSCs can be easily manufactured. In summary, some of the advantages of this new converter as compared to the older water cooled converters are as follows:

- **Improved Snubber design**
- **No need for solid state CB**
- **No need for Voltage and Current sensors**
- **No auxiliary power supply**
- **No voltage isolation issue allowing (>100kV) floating application**
- **Fully optical control**

The VSC is to be based on the new generation 4 ETO, whose features and advantages are explained in the following points.

Main features of the new improved Generation IV ETO are as follows:

- Self gate drive power generation
- Built-in Temperature sensor
- Built-in over current protection
- Built-in current sensor
- Fully optical control
- Built-in voltage sensor

Because of these improvements in the previous version of the ETO, the new generation 4 ETO can be used to greatly satisfy many of the requirements of a new improved modular voltage source converter, such as elimination of voltage and current sensors, elimination of auxiliary power supply and fully optical control. The new converter also has an improved snubber design and improved RCD clamp, which will be shown in the next section.

4.2 Loss Calculations

The topology of the modular VSC is shown in Figure 4-1. This is an H-bridge structure employing four ETOs (S1-S4) and their anti-parallel diodes (D1-D4). An inductor L is used to limit di/dt at turn-on and a RCD clamp is used to limit the over voltage at turn-off of the ETOs. As can be seen, this new configuration employs only one di/dt snubber inductor, as against 4 in the previous Voltage Source Converter described in the previous chapter.

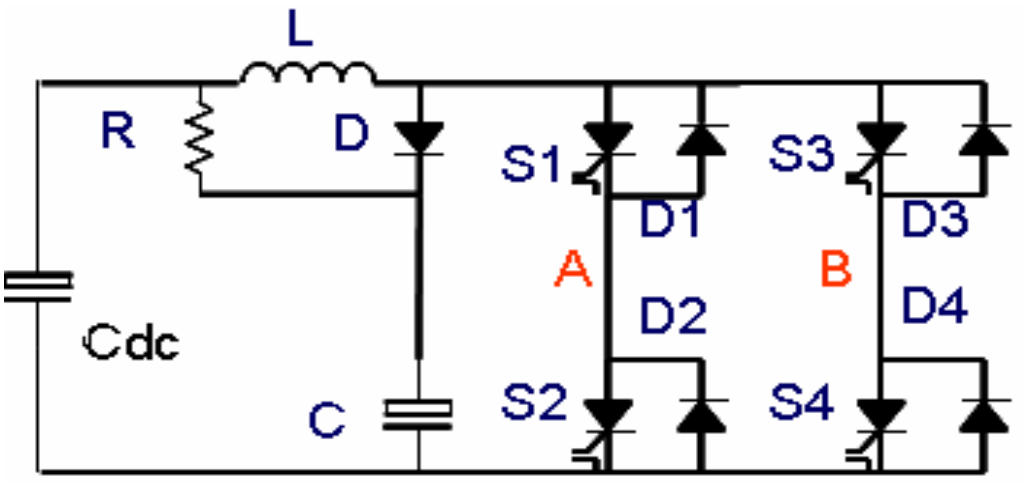


Figure 4-1. Topology of new modular VSC

Losses from the switching components need to be determined in order to design the cooling system. The target application for this high power VSC is chosen as a Statcom with an operating DC bus Voltage of 1.5kV for the ETO at an rms current of 1.4kA. The switching frequency is 600Hz and SPWM method is chosen for the loss calculations with modulation index varying between 0.6 and 0.9. These conditions are taken as the basis of our calculations and design.

From extensive tests done on a 4500V/4000A ETO [20], we can express the turn-off loss using equation (9) and the on state voltage equation (10) at 125°C junction temperature, 1.5kV DC bus voltage.

$$E_{off}(I) = 0.004 \cdot I \tag{9}$$

$$V_{on}(I) = 0.0057 \cdot I + 1.03 \tag{10}$$

Where I represents the current,

The ETO turn-on loss is neglected since it is very small compared with the turn-off loss (due to use of turn-on snubber). Then the switching loss of the ETO is given by (11).

$$P_{sw}(I_{pk}) = f_{sw} \cdot \frac{1}{2\pi} \cdot \int_0^{\pi} E_{off}(I(\alpha)) \cdot d\alpha \tag{11}$$

Here f_{sw} is the switching frequency,

$$I(\alpha) = I_{pk} \cdot \sin(\alpha) \tag{12}$$

The rms current varies between the capacitive and inductive modes (M=0.9 and M=0.6), with standby mode at M=0.75.

$$I_{pk} = (M - M_{s\tan dby})V_{dc} / X_L \tag{13}$$

Here XL is taken as 10% of the system impedance and stands at 0.16ohms.

Switching duty cycle of the ETO is given by the following expression:

$$D(\alpha) = \frac{1}{2} \cdot (1 + M \cdot Sin(\alpha + \varphi)) \tag{14}$$

Here M is the modulation depth, α is the angle within the sine wave (which also varies linearly from -90 to +90 between the inductive and capacitive modes) and φ is the angle of the load impedance. Then the conduction loss is given by:

$$P_{cond}(I_{pk}) = \frac{1}{2\pi} \cdot \int_0^{\pi} I(\alpha) \cdot V_{on}(I(\alpha)) \cdot D(\alpha) \cdot d\alpha \tag{15}$$

Using the above equations, we can calculate the losses in the ETO at different modulation index. We assume φ=0 in our application.

Similar calculations can be done for the anti-parallel diode which is chosen as ABB fast recovery diode 5SDF 10H4502 [21]. The loss characteristics are obtained for this diode experimentally at 125°C, and can be expressed as:

$$E_{switching}(I) = 0.0001I + 0.433 \tag{16}$$

$$V_{on}(I) = 5.674.10^{-4} \cdot I + 2.307 \tag{17}$$

The switching loss includes the turn off loss and reverse recovery loss of the diode. Using similar equations as for the ETO we can obtain the loss of the diode at different modulation index. The results are plotted in Figure 4-2. It is seen that the loss is maximum at the capacitive mode of operation (M=0.9) and lesser at inductive mode (M=0.6). This is because in capacitive mode, the ETOs switch more current. Losses are taken as zero during standby mode (M=0.75). The small amount of losses in this mode (standby) is essentially neglected for the purpose of this analysis.

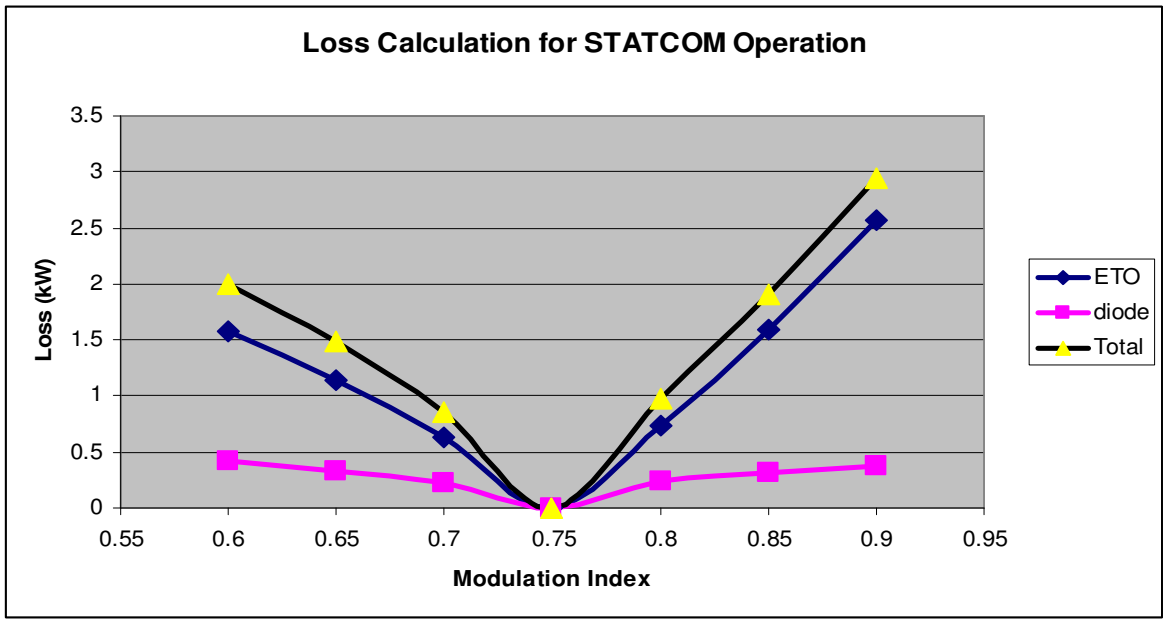


Figure 4-2. Losses of ETO and Diode versus Modulation Index in Statcom mode at Vdc=1.5kV, Irms=1.4kA, Fsw=600Hz

In the figure shown above, loss of the ETO is seen to vary from capacitive mode where it is at 2.6kW, and reduces down to zero for standby mode. The loss again increases as we enter the inductive mode, rises almost linearly, as we reduce the modulation index, until reaching a maximum at M=0.6. The loss number here stands at 1.6kW. The diode loss follows a similar trend, and varies from capacitive mode to stand by to inductive from 400watts down to zero, and then again to little higher than 450 watts. In case of the antiparallel diodes, it is seen that the loss is higher for the inductive mode than for the capacitive, unlike the ETO. This is because the antiparallel diode conducts for the time when the switch of the half bridge is off. The total loss for one ETO and its antiparallel diode is thus plotted as shown in Figure 4-2. The number reaches 3kW during capacitive mode of operation. Thus, in one VSC, which would have 4 ETOs and 4 antiparallel diodes, the losses of the switching components would total to 12kW, which needs to be removed out by a cooling system. The main target of this cooling system is to keep the junction temperatures of the ETOs and diodes well below 125°C. For keeping reliability of these switches, it is prudent not to be very close to 125°C operating junction temperature. Hence, as we would later see, it is desirable to keep the junction temperatures around 110°C.

The physical arrangement for the VSC is to consist of two half bridge structures, each of which has 2 ETOs and 2 diodes, including the heat pipes. In this first possible case, we can think of using double sided cooling for each diode and ETO. This would give us a structure as shown below in Figure 4-3 consisting of a total of 6 heat pipes.

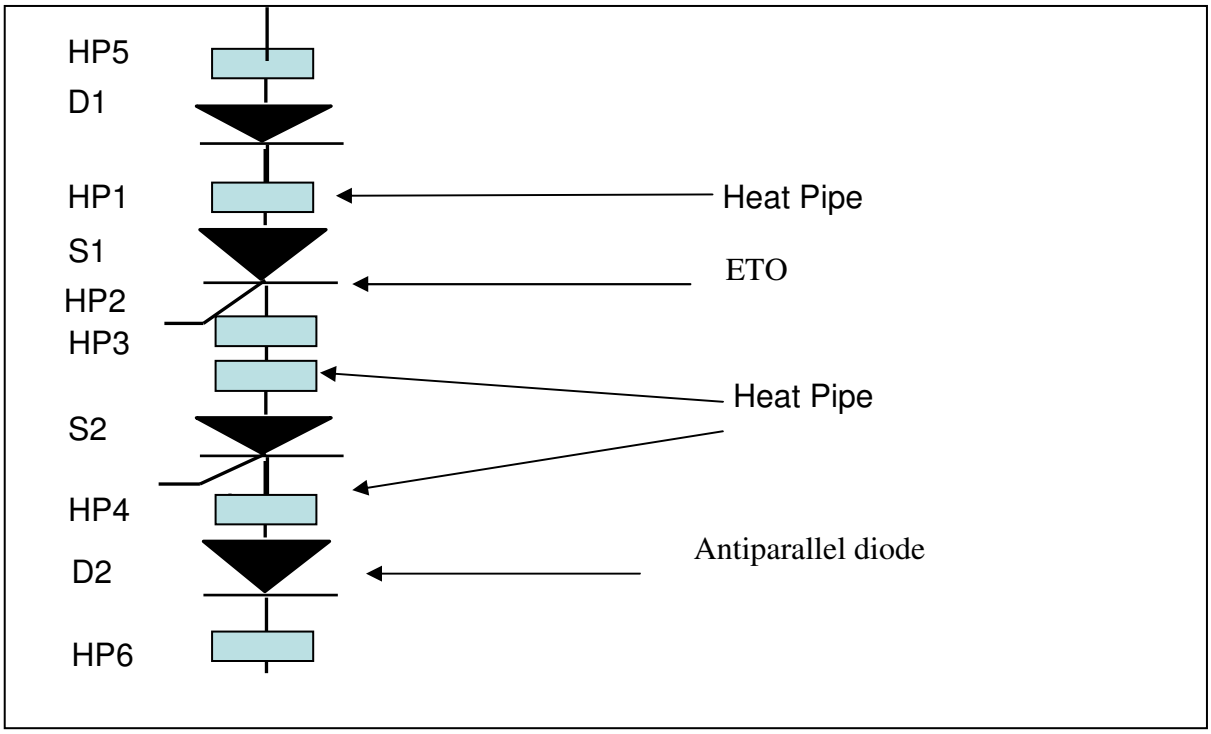


Figure 4-3. Possible physical arrangement of the stack in modular VSC showing ETOs, diodes and Heatpipes

The goal of this air cooled voltage source converter is to attain a high power density converter with minimum cost and minimum number of component count. In order to reduce cost, it is prudent to minimize the number of heat pipes and hence a total of 4 heat pipes are to be used, for double sided cooling of the ETO, and only single sided cooling for the diodes, as shown in Figure 4-3. This kind of an arrangement would mean higher heat flow into each heat pipe, especially into HP1 and HP4. So it is essential to check whether this kind of a smaller and cheaper arrangement would fit the cooling requirement. We also need to determine what is the worst case heat flowing into HP1-HP4 in order to design heatpipes that can dissipate the worst case heat produced into the ambient with a sufficient margin built in, keeping operating junction temperatures of switching components well below 125°C. The figure only shows physical arrangement of the stack, without any copper connections. In order to determine the rating or the

capability of the heat pipe that is to be used, we can assume that heat from the ETO distributes equally in the two directions, i.e. toward the anode and the cathode.

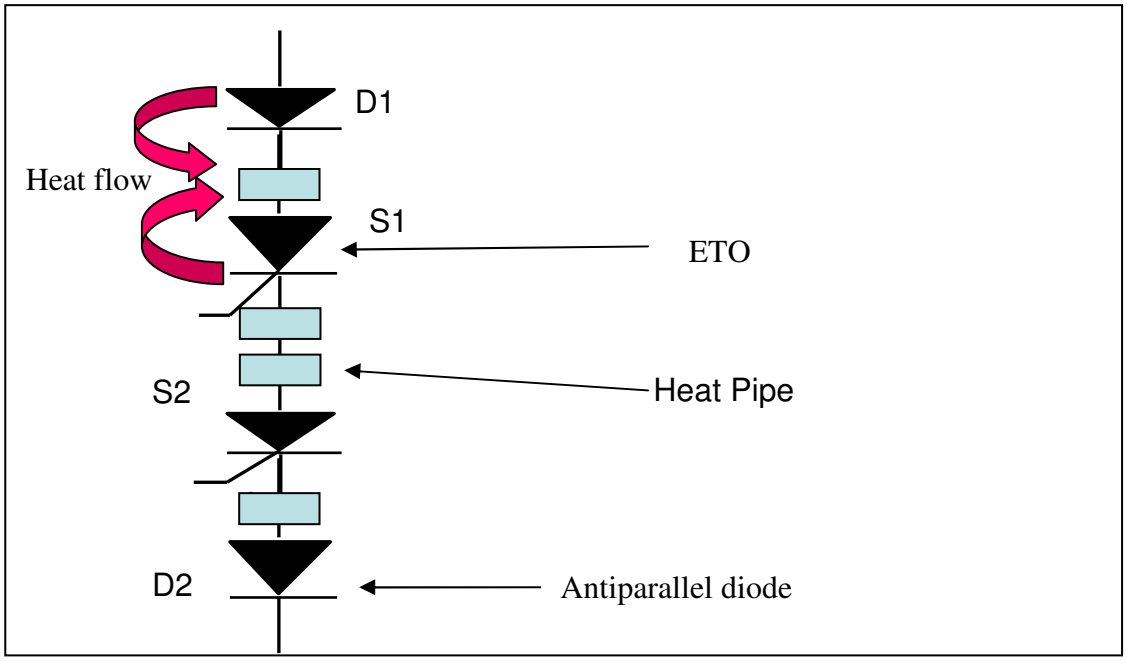


Figure 4-4. Physical arrangement of the stack in modular VSC showing heat flow into heatpipes from ETO and diodes

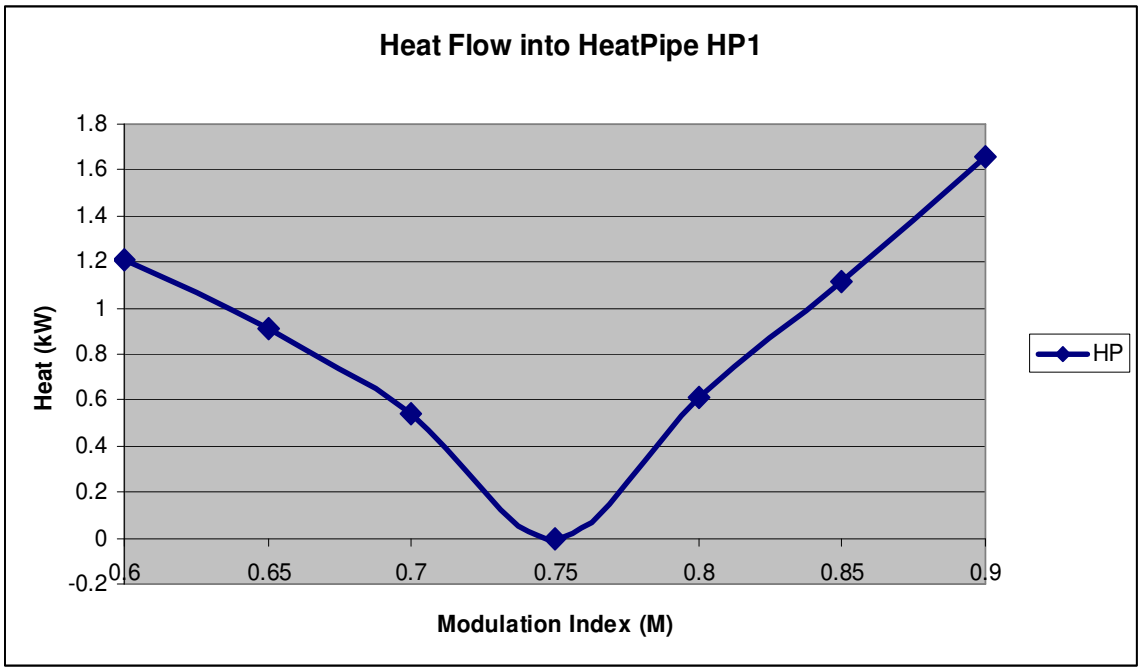


Figure 4-5. Heat flow into Heat pipe vs. Modulation index

This simplifying assumption is not the actual case of course since the thermal resistance of the ETO from junction to anode and junction to cathode is not same. However, with that assumption, we can obtain the heat flowing into every heat pipe as shown in Figure 4-5. The heat flow is calculated and plotted for HP1, which is also the same for HP4, by adding half of the heat loss for an ETO, and adding the loss of the diode. This is done for different values of modulation index. The operating values of modulation index, as mentioned before are from 0.6 to 0.9. The maximum heat that flows into each heat pipe is at M=0.9, and is about 1.7 kW. So we need to have heat pipes that are designed to carry 2.0kW (with some safety margin) of heat out of the switching devices, while maintaining their junction temperature well below 125°C at typical ambient temperature.

4.3 Cooling System Design

Heat pipe [22] consists of a vacuum tight envelope, a wick structure and a working fluid. The atmosphere inside the heat pipe is set by equilibrium of liquid and vapor. As heat enters at the evaporator, this equilibrium is upset generating vapor at a slightly higher pressure. This higher pressure vapor travels to the condenser end where the slightly lower temperatures cause the vapor to condense giving up its latent heat of vaporization. The condensed fluid is then pumped back to the evaporator by the capillary forces developed in the wick structure. This continuous cycle transfers large quantities of heat with very low thermal gradients. A heat pipe's operation is passive being driven only by the heat that is transferred. This passive operation results in high reliability and long life. The operating mechanism of the heat pipes is explained in figure 4-6.

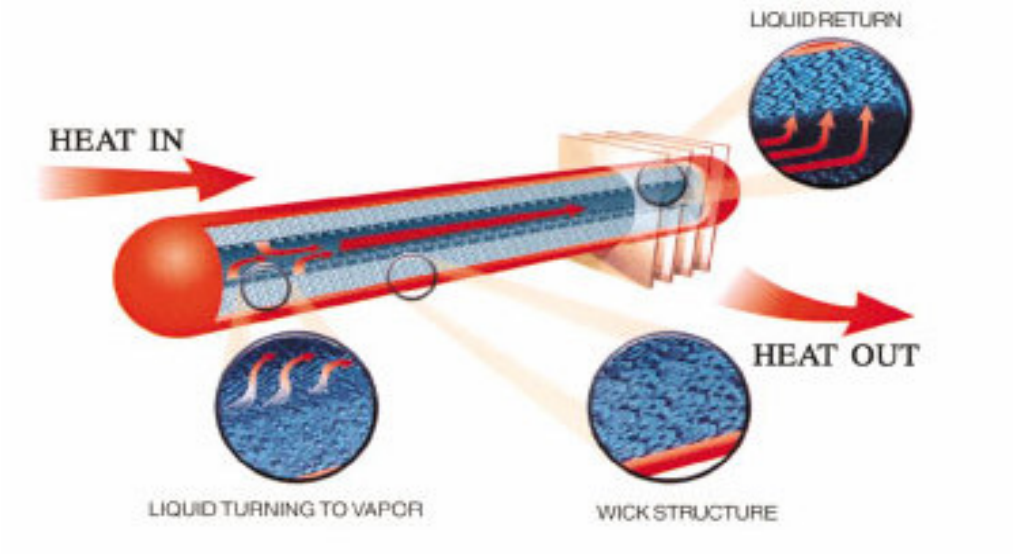


Figure 4-6. Operation mechanism of a typical heatpipe

Heat pipe has a lower total thermal resistance than solid conductors, enabling them to transfer heat more efficiently and evenly. It's totally passive heat transfer system, having no moving parts to wear out and requiring no energy to operate. Heat from the electronics is absorbed by the heat pipes and transported to the fins which are cooled by natural or forced convection. The long pipe that transfers heat from the heatsink to the fins, from where it then enters the atmosphere, has negligible thermal resistance, since the heat is transferred very effectively by the flowing fluid. Heat pipes with the specifications (heat carrying capability) of 2kW and the required dimensions were designed by BOSARI, to be used with the ETOs and diodes.

4.4 Heatpipe Design-Ansys Simulations

Based on dimensions and structure of heat pipe provided by Bosari, 3D ansys simulations were done to determine capability of heat pipes with forced air cooling. This was done by modeling a

section of the heat pipes with small number of fins, and the pipes were modeled as a larger single pipe of copper as shown in Figure 4-7.

4.4.1 Model I-Ansys Simulations

The first model used is shown in the following figure, which has only the fins modeled with a fixed initial temperature of 320K applied to the fins. This was done with a view to understanding the cooling mechanism of a stack of fins when subjected to cool air, with temperature lower than initial fin temperature. The temperature of the fins was set at 320 K and the cooling air was being blown at 290K.

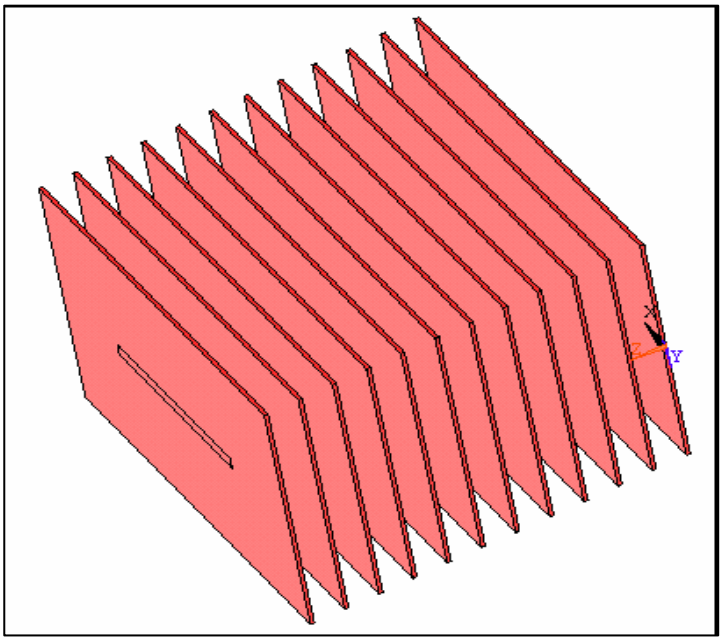


Figure 4-7. Simple fin model of the heat pipe with high initial temperature on the fin stack

Air is blown on the fins, in a plane parallel to the fins in order to cool down the fin stack. This is accomplished using 3D volume of air. The velocity profile, temperature distribution and the pressure distribution is shown in the following pictures.

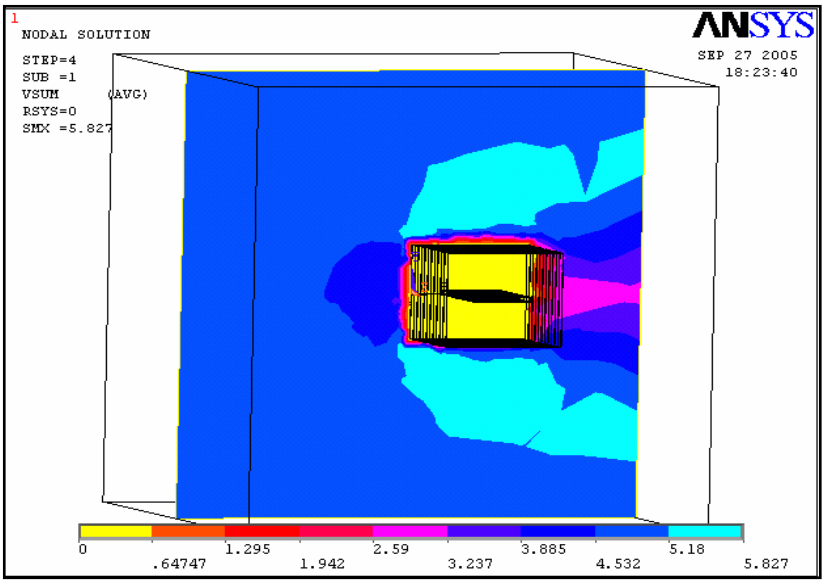


Figure 4-8. Velocity Distribution on the air volume in ansys for heat pipe model 1

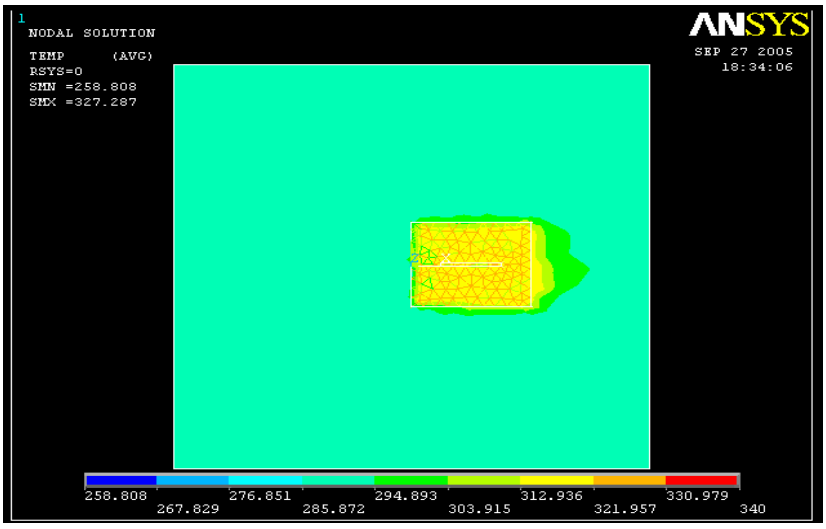


Figure 4-9. Temperature Distribution on the fins in ansys for heat pipe model 1

It is seen that air flowing at 5m/s is able to cool down the fin stack to 310K from 320K. The velocity profile and the pressure distribution are shown in the Figure 4-8 and 4-9. As expected, the pressure of air right in front of the fin stack is almost zero, and so is the velocity of air right behind the fins.

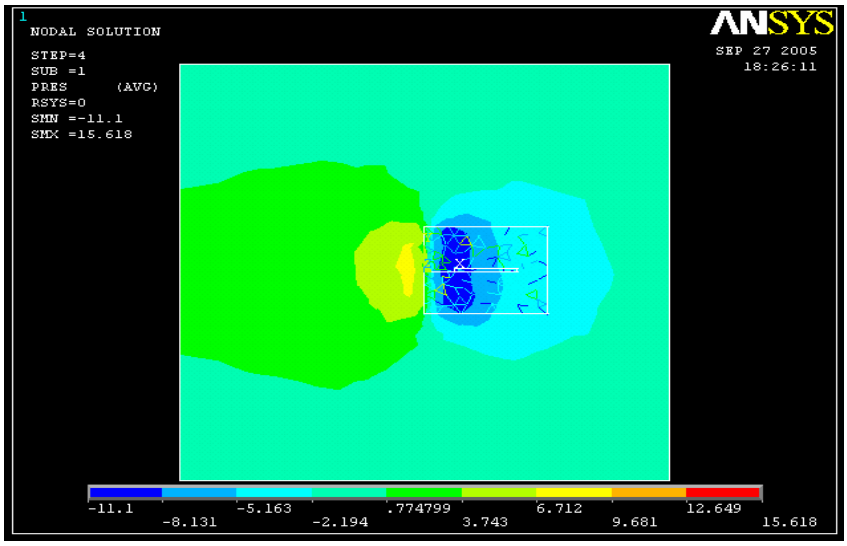


Figure 4-10. Pressure distribution in the vicinity of the fins in Ansys for heat pipe model 1

4.4.2 Model II-Ansys Simulations

Model I used in the above section can be reduced to a much smaller model by using symmetry as shown in Figure 4-11. This would help us in reducing the large amount of time and calculation taken in doing the complicated 3D finite element analysis on Ansys. This fin stack is also subjected to high temperature of around 330 K and cool air is blown on it at 5m/s. We shall call this model as Model II.

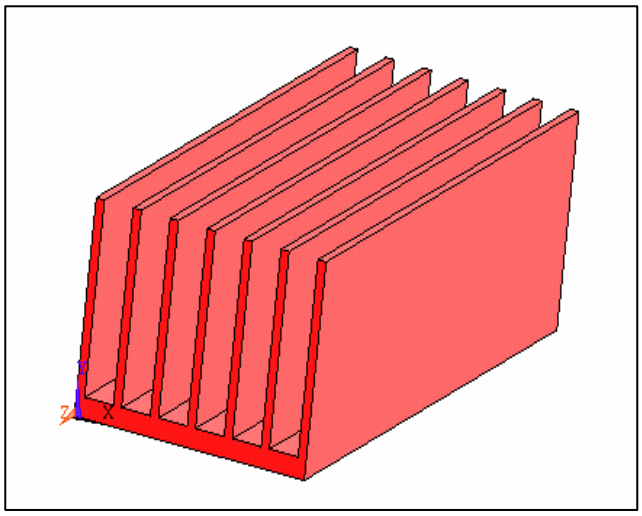


Figure 4-11. Model II using half symmetry for Ansys

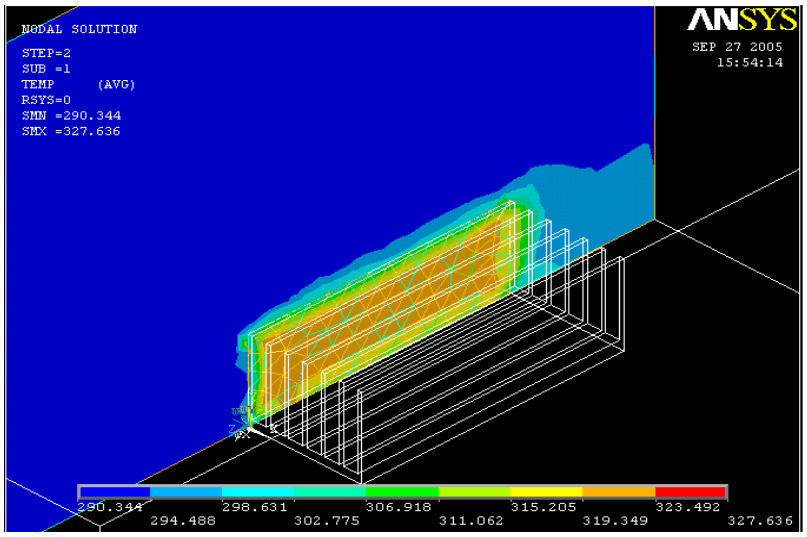


Figure 4-12. Temperature distribution across fins of Model II

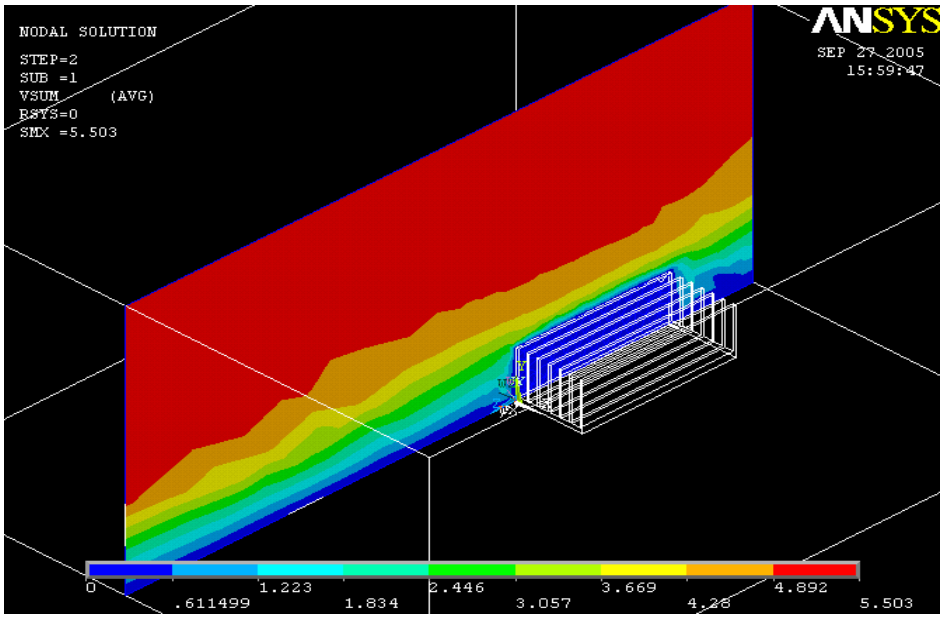


Figure 4-13. Velocity profile distribution across fins of Model II

Simulations show that air flow of 5m/s can cool the fin stack down from 330K to 310 K, with cooling air temperature of 290K. If the cooling air velocity is brought up to 6m/s, the fin stack is cooled down to 300K.

4.4.3 Model III-Ansys Simulations

Its worth mention here that the pipes of the heat pipe that transfer heat from the heat sink attached to the heat generating device, such as ETO, has not been modeled in models I and II. So we develop a new model that includes, very crudely, a part of copper below the fin stack of model II which will generate the heat flux flowing into the fins. The important premise here is that thermal resistance along the length of the heat pipe is zero, since heat is transferred along the length of the heatpipe by heat carrying fluid, as mentioned before. So we now have Model III, with a simple rectangular block that is glued to the fin stack from below, and generating a heat

flux equivalent to a heat flow of 1kW on the fins. The goal here is to see the thermal response of this model and get an idea of the heatpipe performance when it would be subjected to 2kW of heat flow. Since this structure represents only half of the structure, the heat on this is only 1kW. The model is shown below in Figure 4-14. The temperature profile on the front of the heatpipe is shown in Figure 4-15.

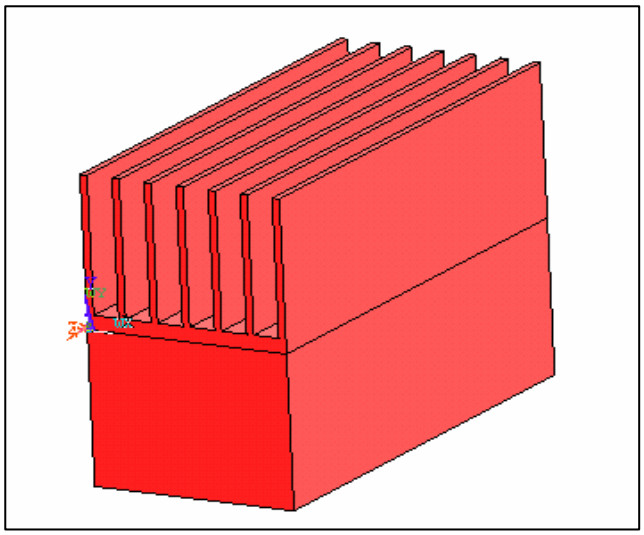


Figure 4-14. Model III with solid cubical base to generate heat flux: crude heatpipe model

FEM simulations on this structure reveal an important aspect of this kind of design : although a heatpipe in the direct path of cool air is nicely cooled, the velocity of air after striking the heatpipe dies down to near zero, and thus if a heatpipe is placed directly behind one, it cannot be sufficiently cooled. Figure 4-16 demonstrates the velocity profile behind one such heatpipe. The next figure, Figure 4-17 demonstrates a similar thing. We have 2 heatpipes one after the other, each subjected to 1kW heat flow. Since these are half structures, it is equivalent to a loss of 2kW on the whole heatpipe.

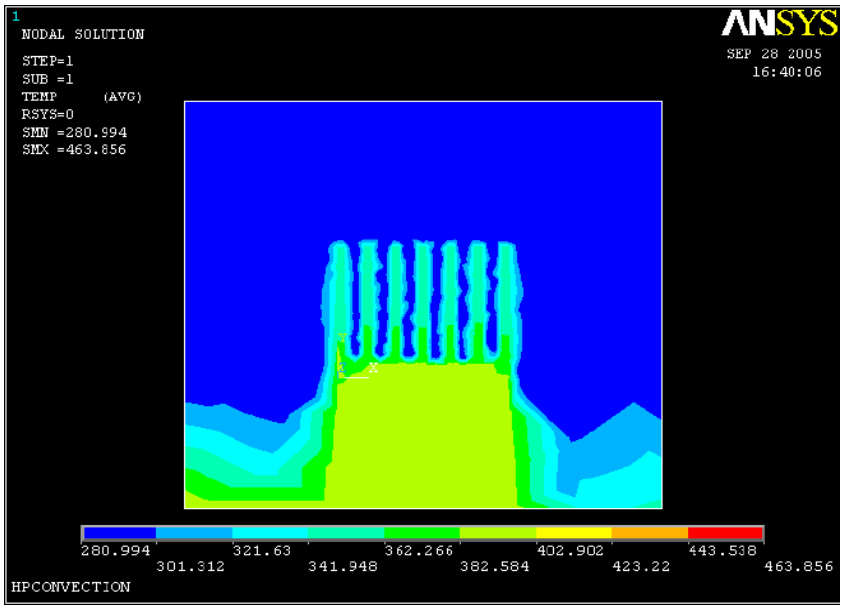


Figure 4-15. Model III showing temperature profile on front side of heatpipe

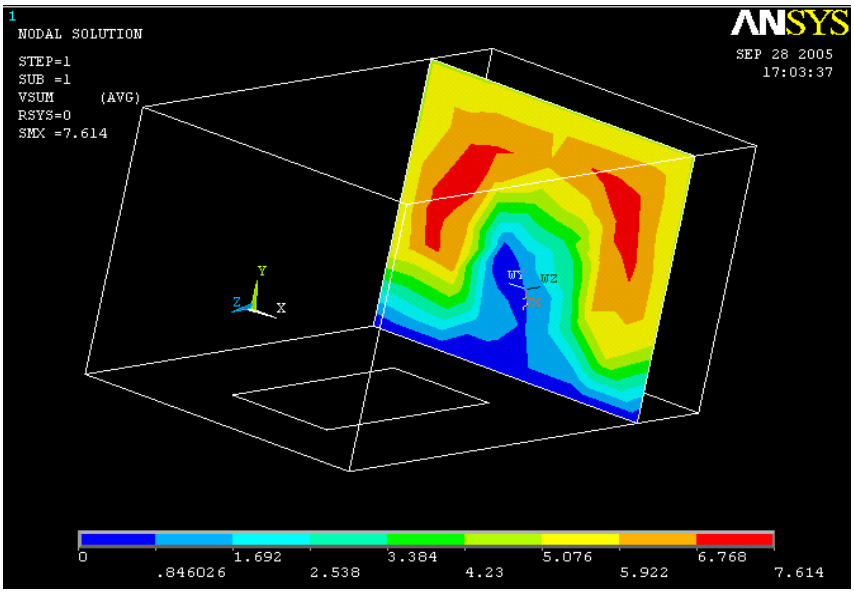


Figure 4-16. Model III showing air temperature profile behind heatpipe

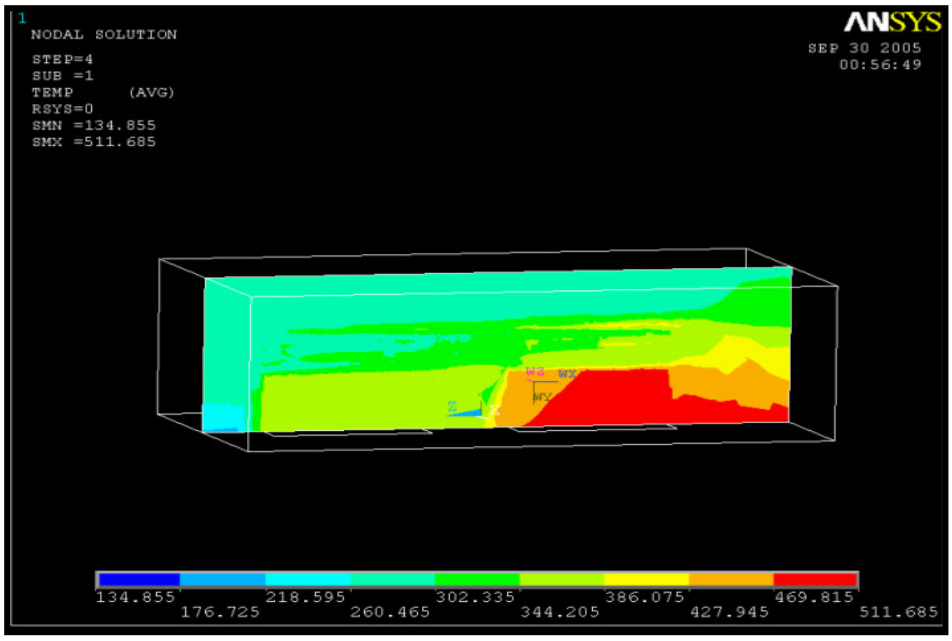


Figure 4-17. Model III showing temperature profile of 2 heatpipes one after the other

It is seen that if air is blown on the heatpipes from the left of the first heatpipe at a velocity of 6m/s, which is a typical air velocity from big fans used to cool heatpipes, at a temperature of 30 Degrees Celsius, the temperature profiles across a cut out section along the length of the heatpipes are as shown. While the first heatpipe is cooled down to about 340K (67 degrees Celsius), the second one reaches temperatures of 475K (about 200°C). This would certainly damage the heatpipe as well as the switch that it is being used to cool. It is also seen that the first heatpipe is cooled to much higher temperatures with 2 heatpipes placed one after the other, than if it is single. As shown by earlier Ansys results, this case cools the heatpipe to about 30 °C higher. The reason for this is the change in backpressure when there is obstruction to the flow of air behind one heatpipe.

4.4.4 Model IV-Ansys Simulations

A better model was then used for further improved simulation results. In this model, the center pipes were modeled as a cylinder. The fins were modeled as structures in continuity to the center rod, thus providing a more realistic model. Only half of the structure was actually simulated with a loss of 1kW on the center copper rod. The outer box in Figure 4-18 represents air flow volume, with air blowing across the fins at 6m/s and temperature of 20°C. The part of the heat pipe from the heat sink to the copper pipes is not modeled as it is assumed that this has negligible thermal resistance due to flow of heat carrying fluid. It is also assumed that along the length of copper pipes, the thermal gradient is very small. The main contribution of thermal resistance is from the fins to the air. Figures 4-19 to 4-22 are temperature profiles across this model with air flowing through the fins at 6m/s. It is seen that the heat pipe can effectively transfer heat from the fins to the air without much rise in temperature. It is seen from these Ansys results is that we obtain a thermal resistance of 15K/kW from the heat pipes to the ambient at a flow rate of 6 m/s.

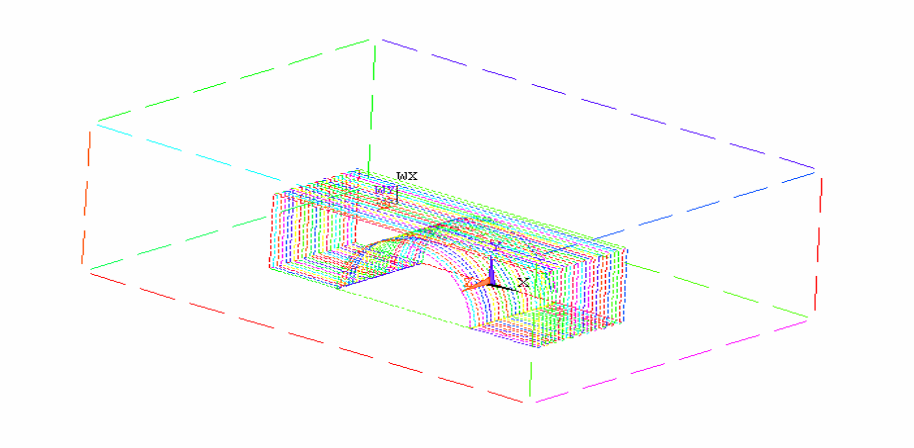


Figure 4-18. Model IV of Heatpipe used in Ansys

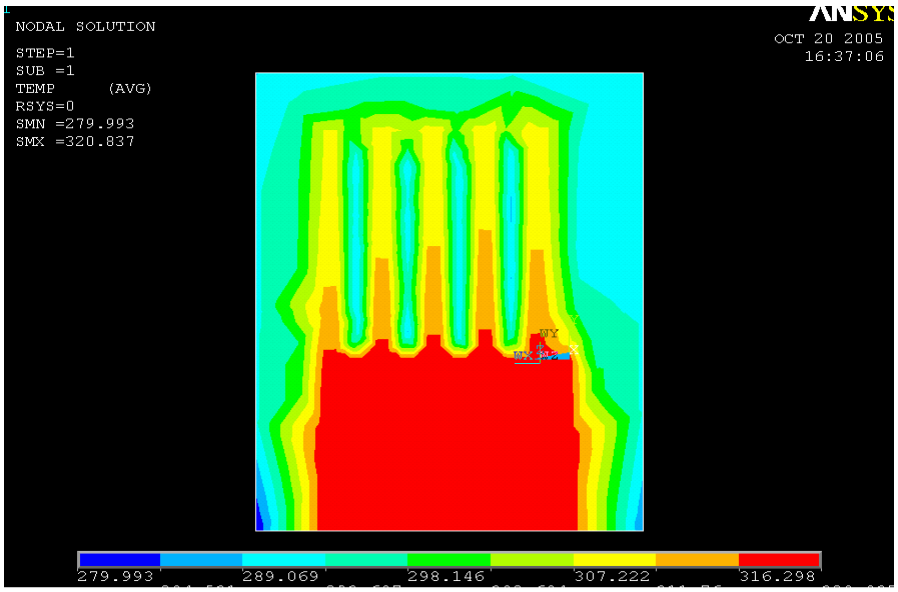


Figure 4-19. Temperature profile of cutout section across heat pipe model with cooling air flow at 6m/s

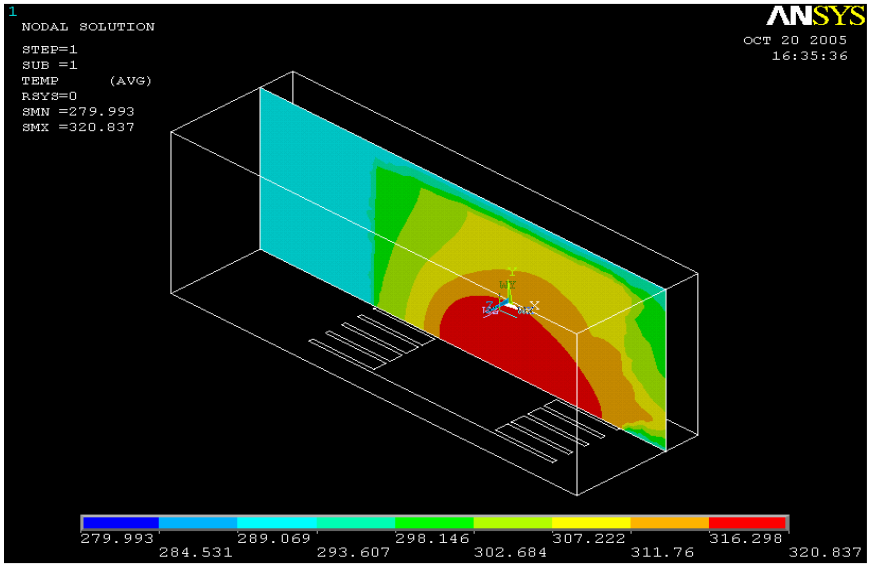


Figure 4-20. Temperature profile of side cutout section across heat pipe model with cooling air flow at 6m/s

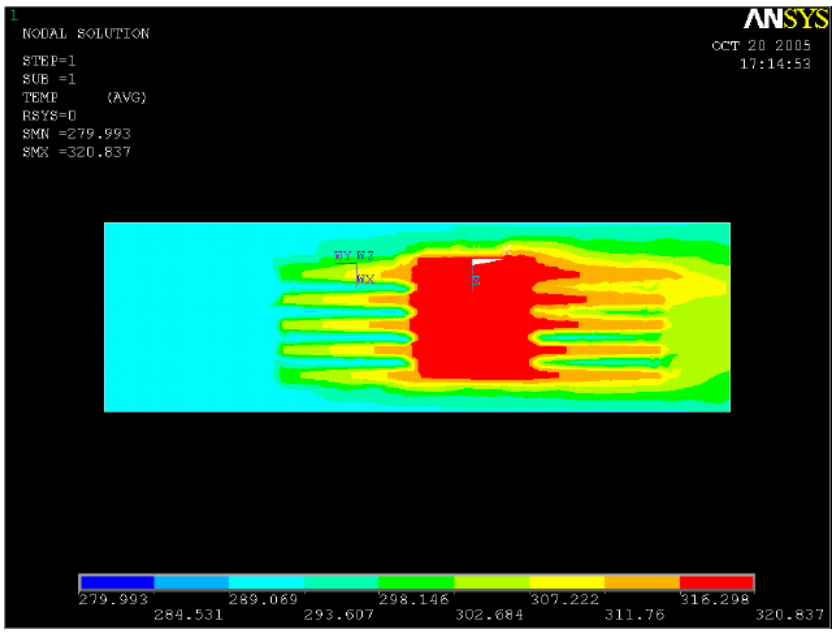


Figure 4-21. Temperature profile of top cutout section across heat pipe model with cooling air flow at 6m/s, with the left part being the front and the right being the rear part of heatpipe subjected to air flow

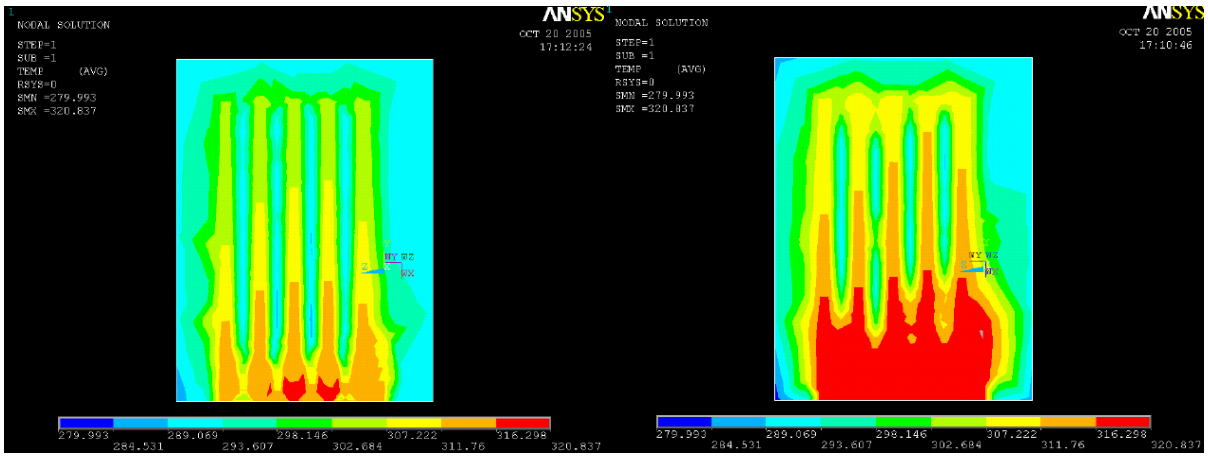


Figure 4-22. Temperature profile of cutout section across heat pipe model with cooling air flow at 6m/s, left profile is of front portion and right one is of back portion of heatpipe

4.5 Heatpipes - Design and Testing

Through simulations done on Ansys we can obtain the variation of fin temperature with air speed, and thus also the thermal resistance variation of the heatpipe with air speeds. As explained in the operation of the heatpipe in the beginning of this section, forced convection cooled heatpipes display much lower thermal resistance as compared to natural convection cooled heatpipes. In other words, if we cool a heatpipe with cool air at certain velocity, it enables faster and better heat transfer from the fluid in the heatpipe to the fins to the ambient air, resulting in much cooler junction temperatures of devices being cooled. Another important point here is that gravity assisted cooling inside heatpipes leads to much better performance, as that enables the heat carrying fluids inside the heatpipe to rise with natural convection too. For optimum performance of heatpipe, it should be mounted at 5 to 90 degrees with the horizontal. In the Ansys simulations, this effect has been ignored, since thermal resistance along the length of the heatpipe is ignored. Thus the results may be little higher than actually seen. The figures on this page show variation of thermal resistance and fin temperature with air speed, as obtained from Ansys simulations on Model IV.

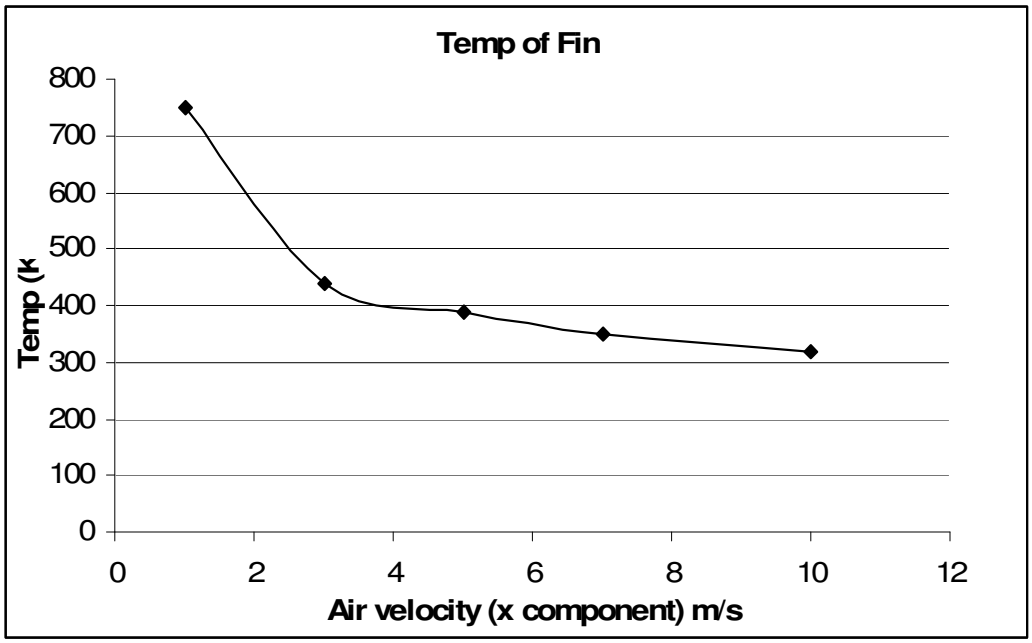


Figure 4-23. Fin temperature variation of heat pipe model IV with cooling air flow rate in Ansys

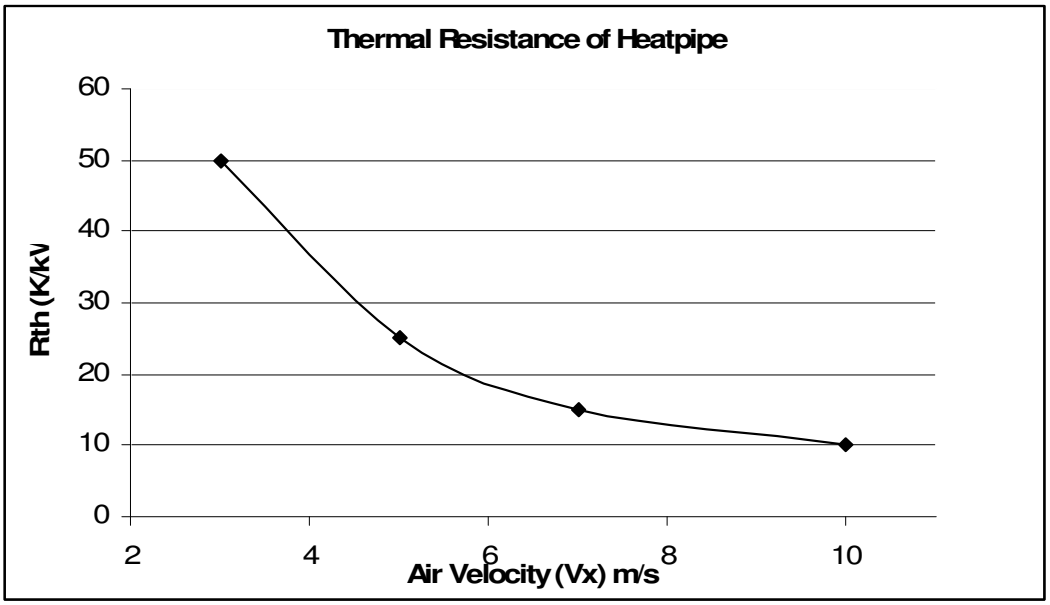


Figure 4-24. Thermal resistance variation of heat pipe model IV with cooling air flow rate in Ansys

The above two graphs highlight the importance of concentrated air flow on the heatpipes from fans in order to maximize performance of these cooling devices.

Figure 4-25(a). Heat pipe custom designed and manufactured by Bosari

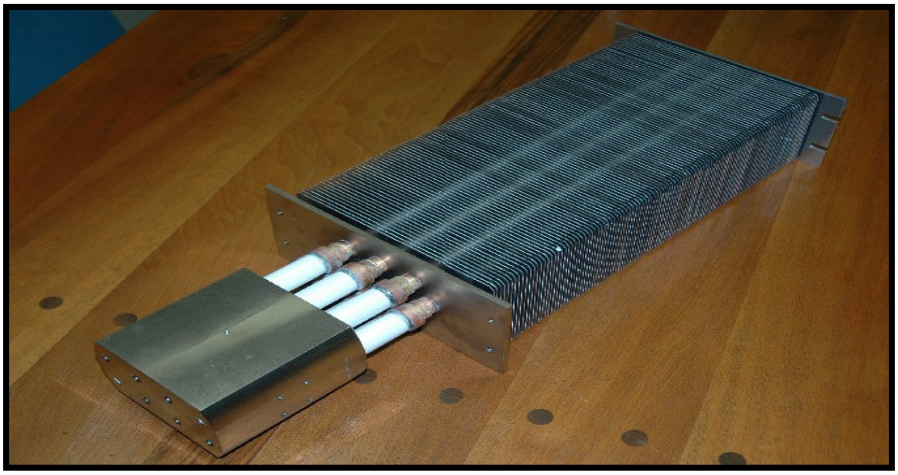


Figure 4-25(b). Heat pipe custom designed and manufactured by Bosari-another view

Figures 4-25(a),(b) shows the heat pipes designed by Bosari which are to be used in the modular VSC The above two figures show the heatpipe manufactured by Bosari Thermal Management based on design parameters provided to them.

The heat pipes were tested by Bosari after construction, and Figure 4-26 represents the results in the form of temperature at the heat sink with different heat flowing into the heat pipes, plotted

w.r.t. time. The temperature of cooling air is 20°C, and the points 1-4 on the top curves represent heat flow into heat pipe of 1.8, 2.0, 2.2, and 1.8kW respectively. We can calculate the thermal resistance of the heat pipes from the steady state values of temperature at the heat sink surface at different power levels. At 2.2 kW, the temperature at the surface of the heat sink at steady state is 80°C; the air temperature is around 25°C. So after deducting a contact thermal resistance between heater and heatpipe of 5K/kW, we get the thermal resistance of heat pipe from contact point to air as 20K/kW (this is at 4m/s flow rate of cooling air). This is slightly higher that the Ansys results (15K/kW), but those results were at

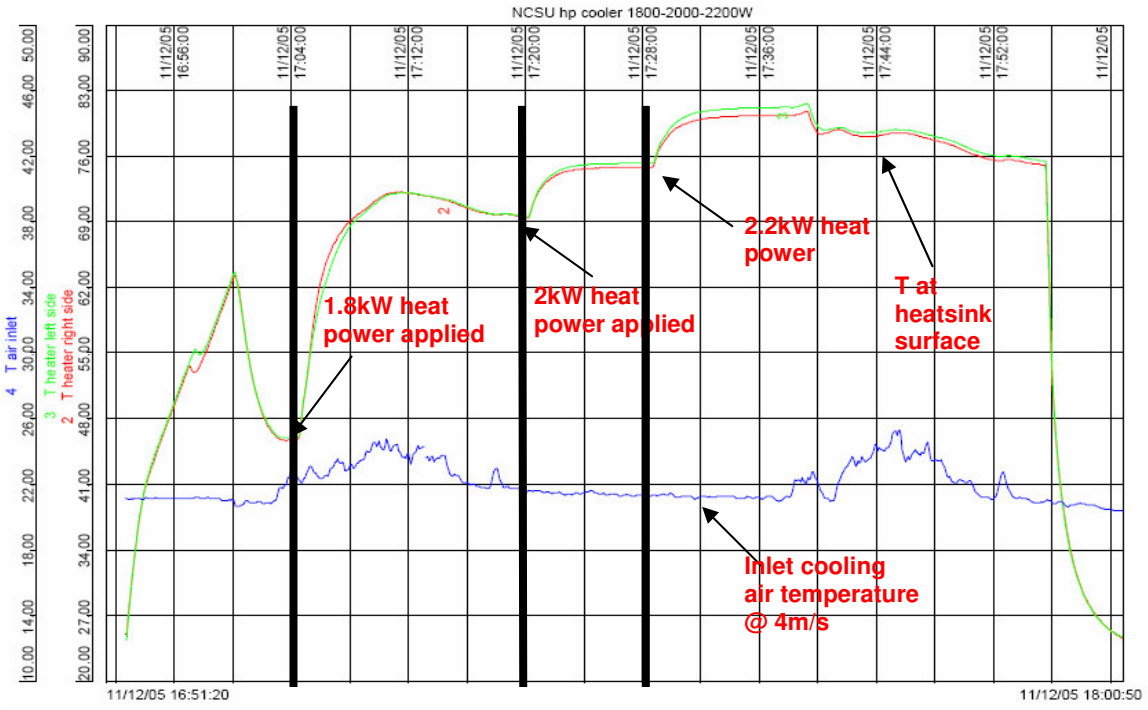


Figure 4-26. Heat pipe testing results by Bosari Thermal management

6m/s air flow, so this is acceptable. It is worth mention here that this test was done with the heat pipes in the vertical position as this gives that best results with forced convection. These Bosari tests give us results which can be summarized as follows:

- The inlet air temperature is maintained at 21 °C, and velocity at 4m/s
- The test is done at 3 different power levels of 1.8, 2.0 and 2.2kW
- The temperature at each level is allowed to reach steady state and is measured at the heater surface, extremely close to the contact point
- At 2.0 kW, Theatsink = 75 ºC, T amb = 25 ºC

  Rth = 25 ºC/kW however, there is a contact thermal resistance of 5-6 ºC/kW.
- Hence, Rth(heatsink-ambient) = 20 ºC/kW
- At 2.2kW, Theatsink = 80 ºC, Tambient = 25ºC so Rth (excluding surface contact resistance) = 20 ºC/kW

In order to make sure that the stack shown in Figure 4-4 will actually be cooled sufficiently by the heat pipes, we need to do a simple thermal network simulation of the half bridge stack shown in Fig.3, with only 4 heatpipes. The purpose of these simple simulations is to make sure that at the thermal resistance levels predicted by Ansys/Bosari, and at the calculated loss levels for the ETOs and the diodes, can the junction temperatures of the switching devices remain at sufficiently low levels (below 125 ºC).

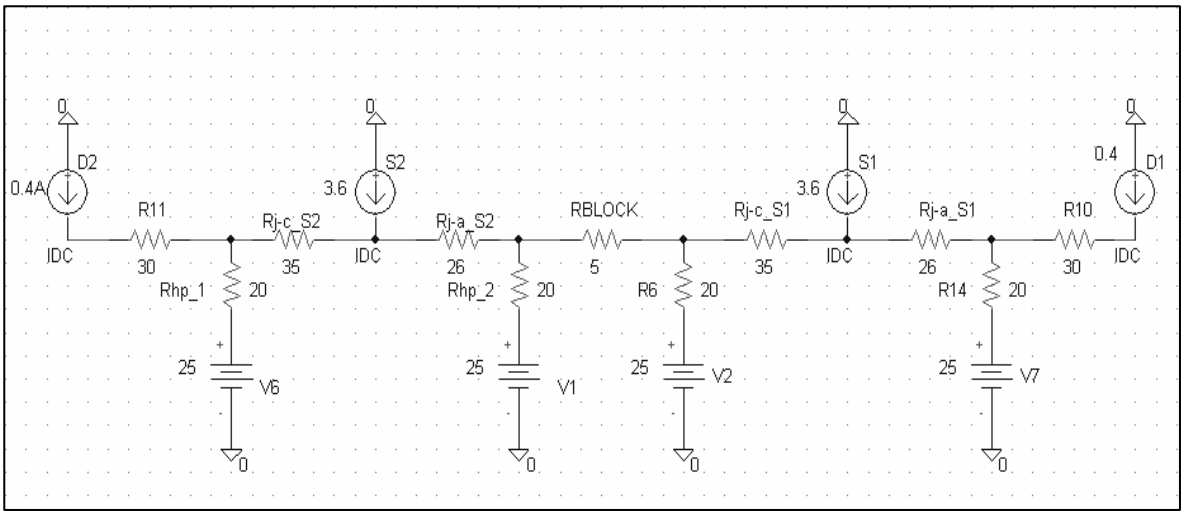


Figure 4-27. Thermal network for junction temperature simulation of VSC half bridge stack

The simulation is done by converting all thermal parameters such as thermal resistance, heat and temperature to their electrical equivalents, i.e., resistance, current and voltage. Figure 4-27 represents this network, having all the actual thermal resistances of the ETO and diode (junction to anode and cathode), and the heatpipe. The thermal resistance of the ETO is not symmetrical across the junction due to the presence of copper plates at the cathode side, and this is visible from the thermal circuit in Figure 2-10. Contact thermal resistances have also been added. Current sources represent heat flow from the junctions of the switching components and voltage sources represent ambient temperature. RBLOCK represents separation between the two heat pipes in the middle. The network was simulated at the original design values of Vdc=1.5kV, Irms=1.4kA, f=600Hz with varying values of modulation index, and the results are shown in Figure 4-28. The shaded values in figure 4-27 represent the junction temperatures of the ETOs and diodes. The results for different values of M are plotted in Figure 4-29. It is seen that the temperatures are well below 125°C over all operating ranges, and that S1 and D1 are hotter than

S2 and D2. This is primarily due to the unsymmetrical thermal resistance network as shown in Figure 4-27. For values of M from 0.6 to 0.85, the junction temperatures of all ETOs and diodes are well below 125°C, in fact they are below 80°C. for M=0.9, that is the full capacitive mode, the junction temperatures of the ETOs reach about 110 °C, and that's higher because the losses at this operating region are highest. This plot of junction temperatures proves that we can do pretty well with 4 heatpipes, and thus do not need 6 heatpipes as discussed earlier.

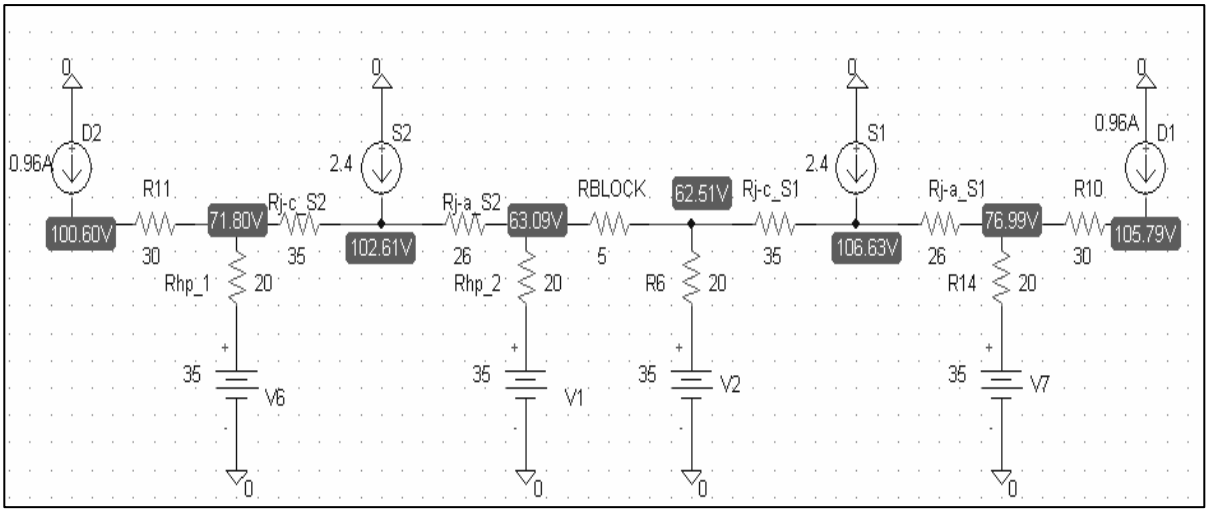


Figure 4-28. Simulated Junction temperatures at Vdc=1.5kV,Irms=1.4kA,f=600Hz,M=0.9

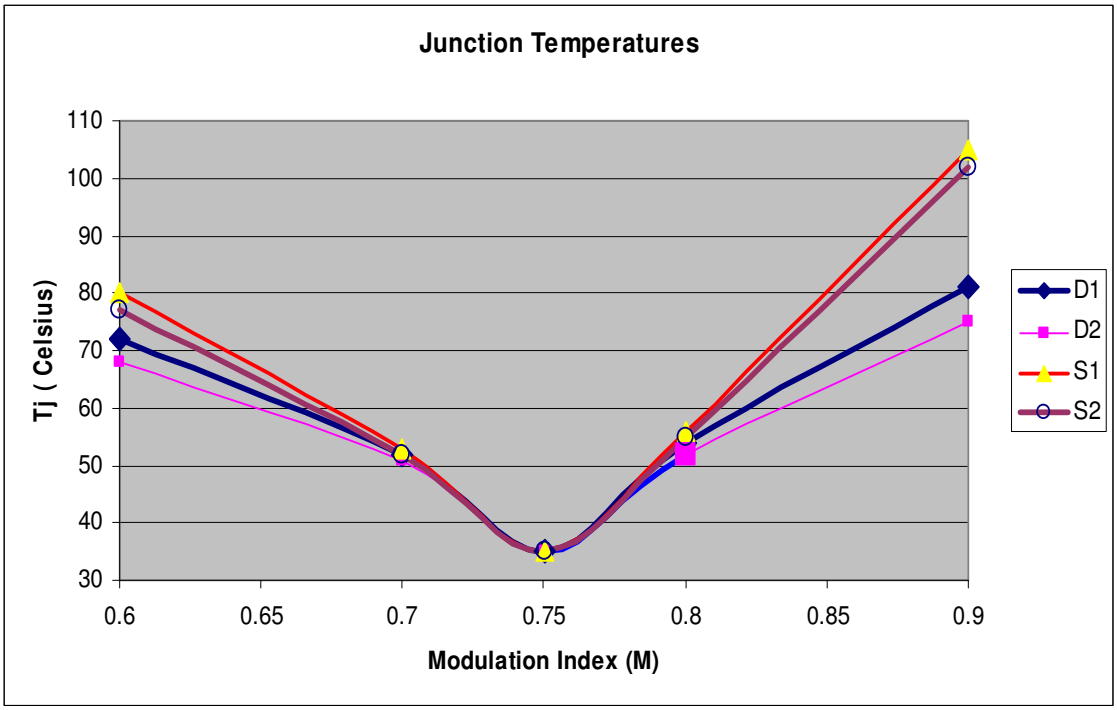


Figure 4-29. Simulated Junction temperatures of diodes and ETOs at Vdc=1.5kV, Irms=1.4kA, f=600Hz at different Modulation Index

Thus based on the validity of the structure shown in Figure 4-4 before, we can construct a voltage source converter using AutoCAD, with all the exact dimensions of the ETO, diode, heatpipe, RCD clamp, etc. The configuration places two heatpipes around one ETO, and thus provides double sided cooling for the ETO. The antiparallel diodes are to be single side cooled as shown in Figure 4-30 (a),(b). There is a spacer in between the two heatpipes in the center, so that their fins do not touch each other. ABB clamps are used to provide the necessary mounting force of 40kN for the press pack devices. The result is a highly compact designed voltage source converter, with passive cooled heatpipes. Figures 4-30 (a), (b) and (c) show the side, isometric and top views of this modular Voltage Source Converter respectively. The RCD clamp is also

included in the figures. The snubber inductor is not shown. Also, copper connections are not included in the AutoCAD drawings.

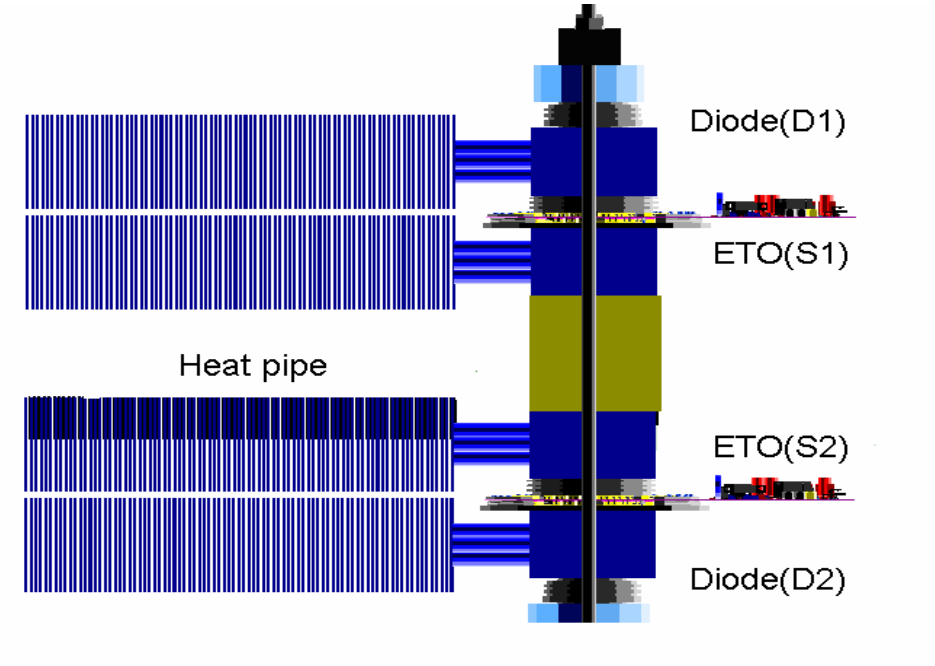


Figure 4-30(a). Side profile of modular VSC half bridge stack

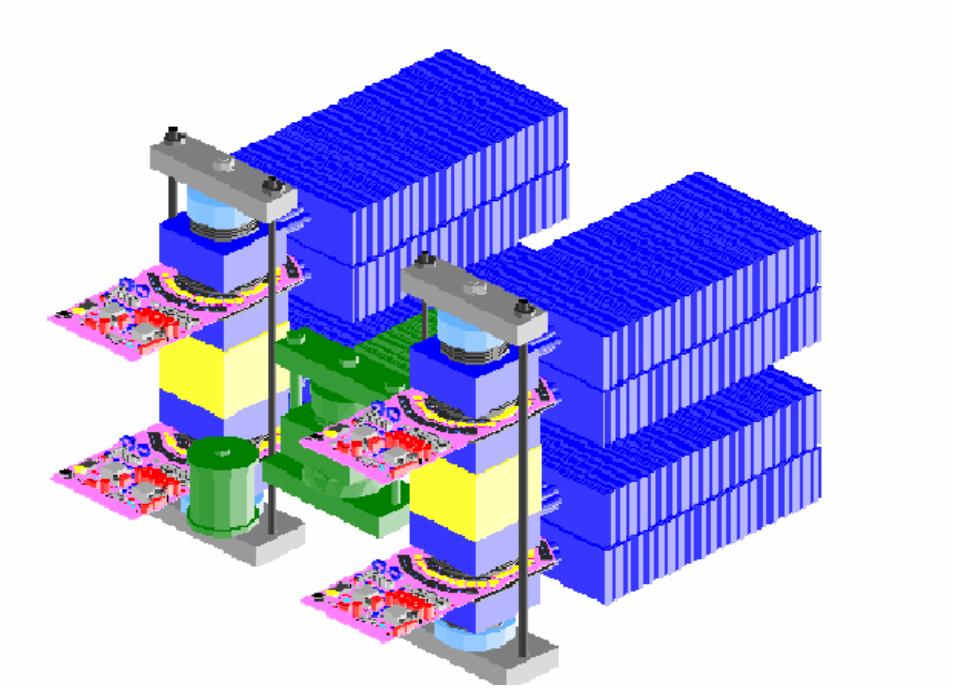


Figure 4-30(b). Isometric view of modular VSC half bridge stack

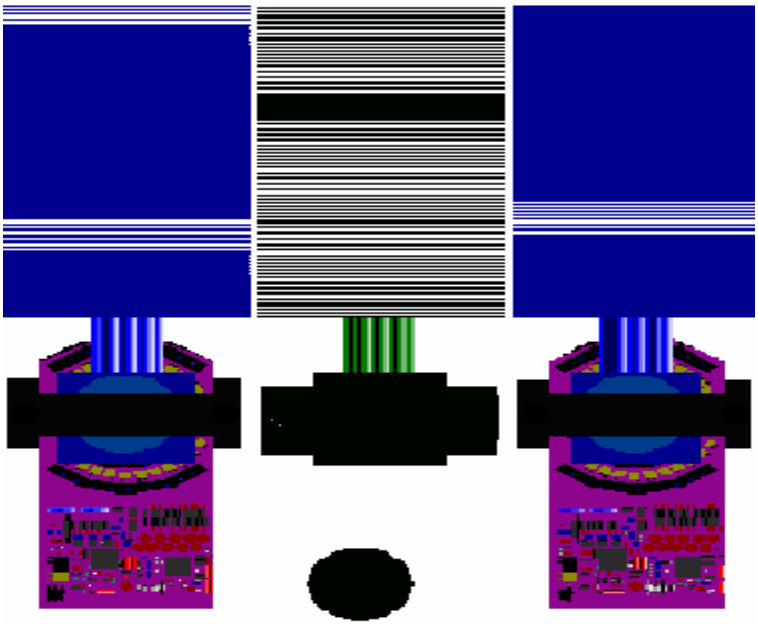


Figure 4-30(c). Top profile of modular VSC half bridge stack

The next step is to determine direction of air flow on the heatpipes. There are lots of possible configurations to blow air on to the voltage source converter. Some of these are shown below: (arrows indicate direction of air flow)

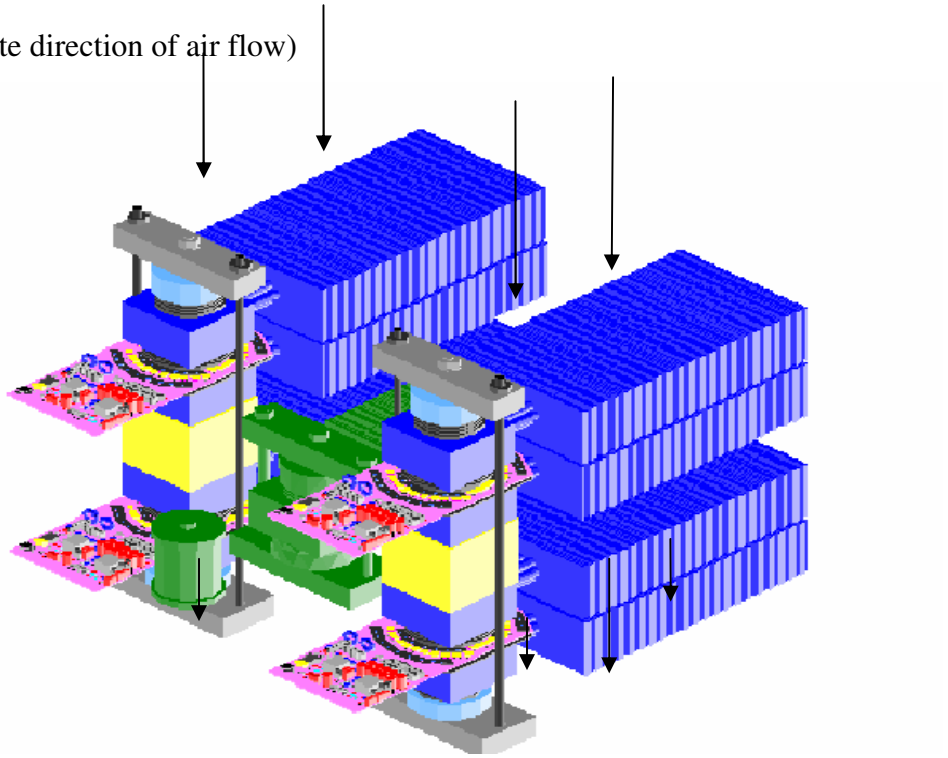


Figure 4-31(a). First possible configuration of VSC with air flow indicated by arrows

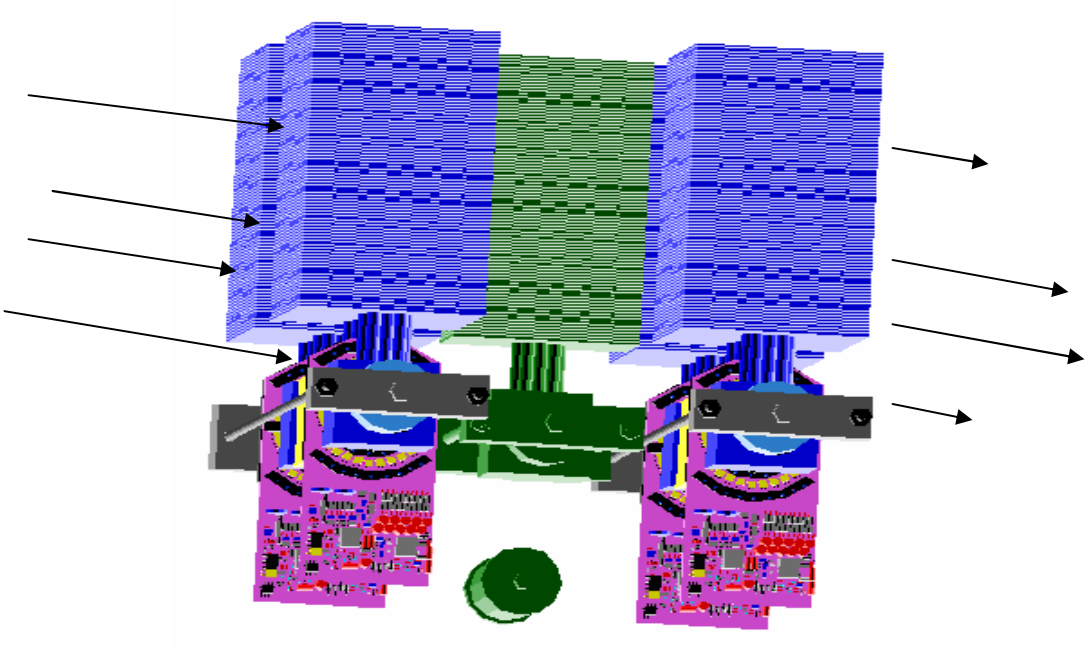


Figure 4-31(b). Second possible configuration of VSC with air flow indicated by arrows

Figure 4-30(a) shows a possible way of blowing air on heatpipes using fans. There are few problems with this approach. Firstly, the heatpipes need to be at an angle of 5 to 90 degrees with the horizontal. This configuration does not allow for this. Also, as seen earlier, if cool air is blown on one heatpipe dissipating about 2kW of heat, by the time it comes out through the fins, the air temperature gets elevated by a large amount. Thus it is largely incapable of cooling any more heatpipes thereafter. This problem was highlighted through Ansys simulations shown in Figure 4-17. The first configuration has 4 heatpipes in the same path for air, and hence this would be highly ineffective. Moreover, there would be problems of back pressure involved with this approach. The second structure in Figure 4-31(b) looks better with the gravity assisted operation since the heatpipes are vertical. However, this has similar problems since the heatpipes

are placed behind one another. This creates problems of elevated temperature and back pressure. In order to alleviate all these problems we need a structure that not only uses heatpipes in a vertical orientation, but also ensures that each heatpipe receives cool air at the ambient temperature directly. This would mean equal operating temperatures for all devices being cooled by heatpipes. The figure below is one possible solution.

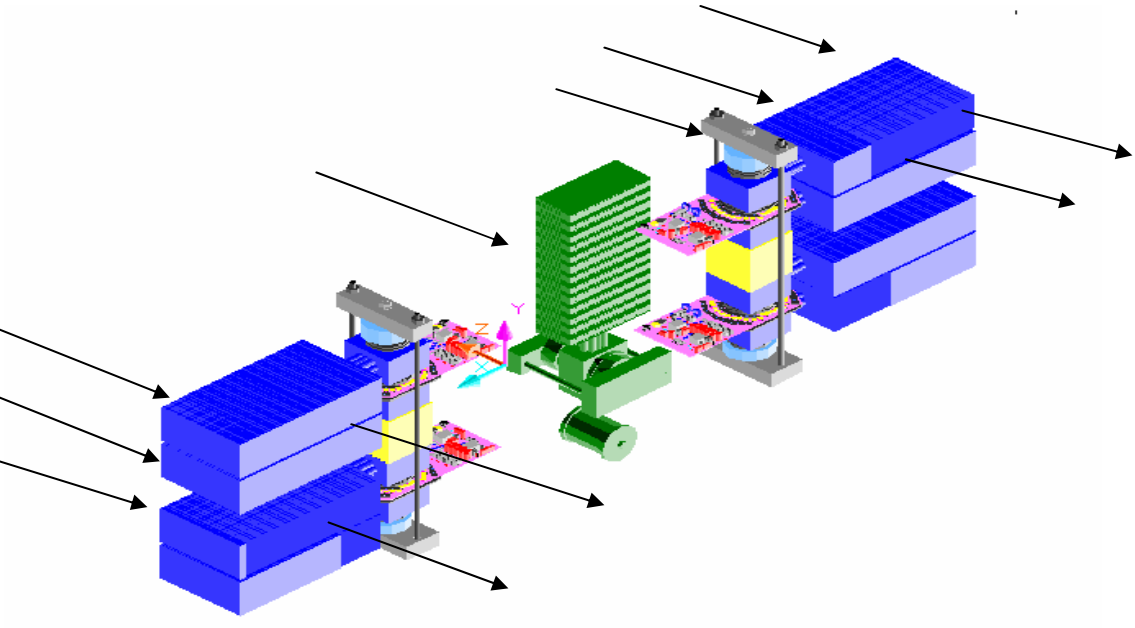


Figure 4-31(c). Third possible configuration of VSC with air flow indicated by arrows

This arrangement in Figure 4-31(c) meets all of the above mentioned requirements, if the left and right stacks are just made vertical. The center heatpipe is needed for cooling the RCD clamp components, namely the diode and the resistor. The problem with this configuration is the large size of the converter. The other problem is the complications involved in completing copper connections between various parts of the stacks. So a better solution is required which is included in the next figure.

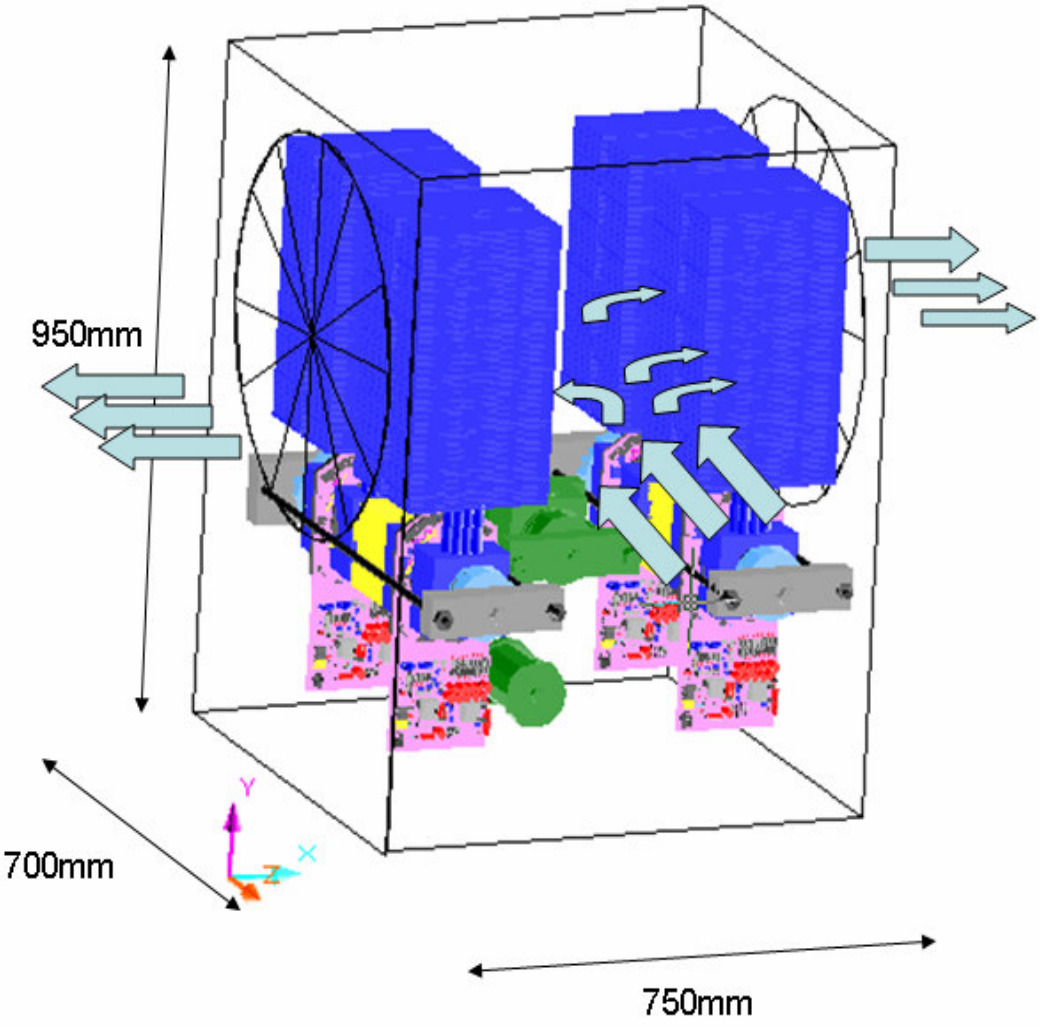


Figure 4-32. Conceptual drawing of modular VSC structure with fans and air flow indicated by arrows

Figure 4-32 shows the final design of the Voltage Source Converter, with the air flow, fans and dimensions indicated. The structure guarantees good cooling for all heatpipes. The idea behind this kind of an implementation is to pull air from a different plane than which it is going to be blown into. In the figure, air is sucked in from the z direction, and then blown towards the positive and negative x directions. This makes sure that the two half bridge stacks are placed

close to each other, and at the same time both receive cool air and transfer heat to this cool air at the same time. The kind of fan that can be used for such air flow is the centrifugal fan which is shown in the Figure 4-33 below. Its operation can be understood by the help of the arrows. There is a motor at the back of the fan, which enables it to suck air from the x direction, and blow it out in the positive z direction, as shown. The hot air, which gets heat from the fins of the heatpipe, blows out of the structure by the help of two big fans on the positive and negative x directions/faces of the voltage source converter as shown in Figure 4-32. These fans help in sucking out this air. The heatpipes in the VSC are supposed to be mounted vertically as shown. This maximizes the heat transfer from the heat pipes to the ambient air.

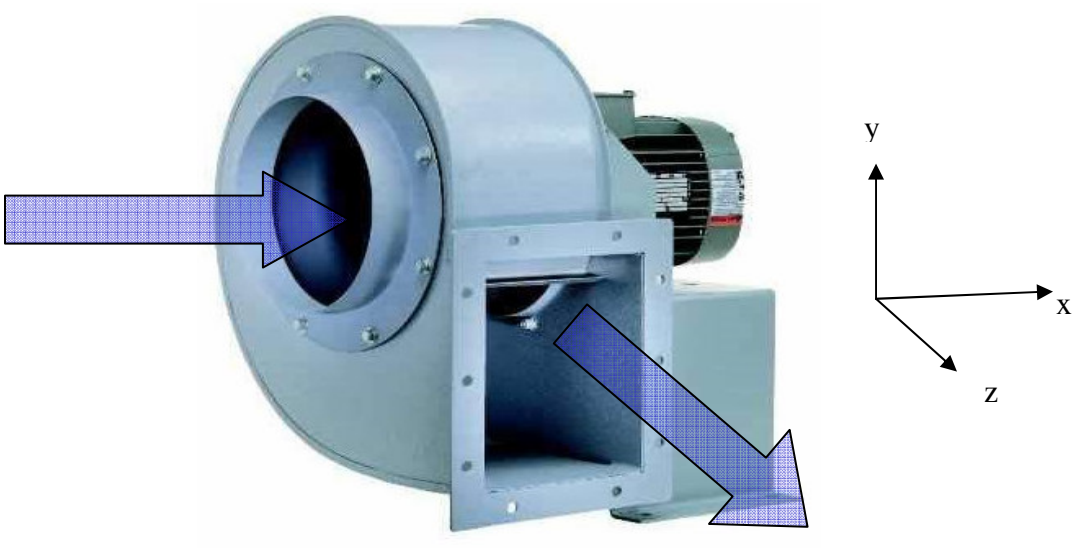


Figure 4-33. Centrifugal fan and its air flow directions

4.5.1 Heatpipe testing

The performance of the heatpipes is tested by using them to cool an ETO operating in a DC-DC Boost Converter. The converter is operated so that it the ETO generates losses, due to which there is heat flow into the heatpipes, which are employed for double sided cooling of the ETO. For this purpose, a new boost converter is assembled, that has two heat pipes as the cooling devices. The converter structure is shown in Figure 4-33. The electrical structure is identical to the water cooled boost converter structure discussed in section 2.2 and shown in Figure 2.2., consisting of the ETO with its anti-parallel diode, the feed forward diode, and the boost inductor. There is also a capacitor bank and a resistor bank on the output side of the converter. The converter structure is shown in Figure 4-33. The ETO is subjected to double side cooling using two heat pipes, and the two diodes have single sided cooling as shown. The heatpipes are mounted in the vertical position, so as to allow maximum cooling capability of the heatpipes. Copper connections are also shown in the figure. Thermocouple is connected to the cathode of the ETO to record the temperature rise of the ETO. The aim of these tests is to determine the thermal resistance of the heat pipes as a function of air speed on the heat pipe fins. The air is being blown on the heat pipes using axial fans.

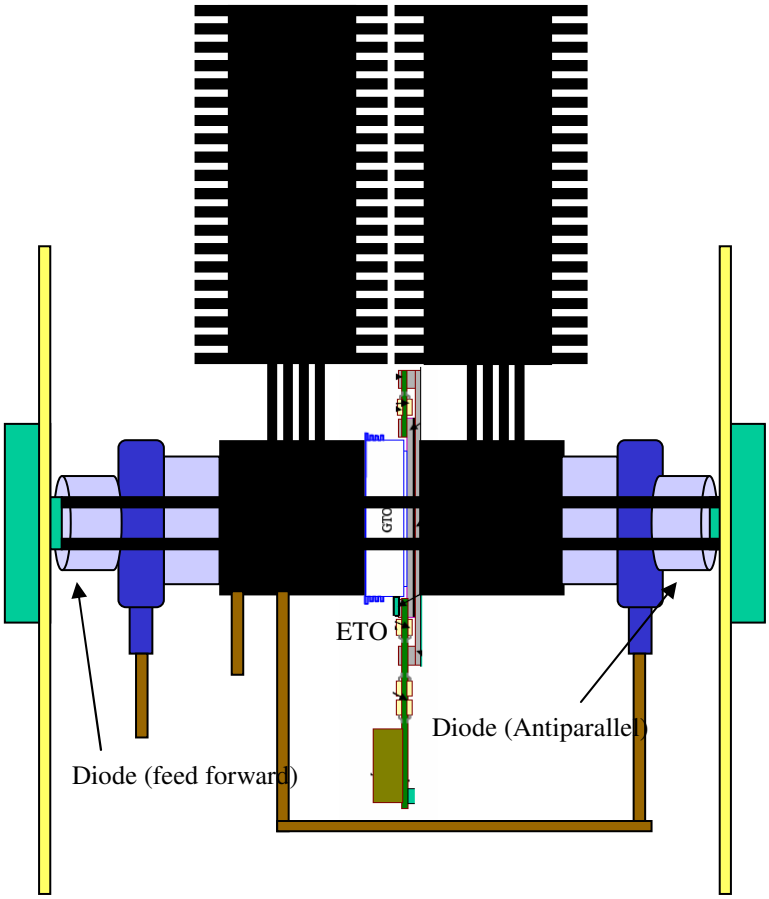


Figure 4-33. The boost converter setup with heat pipes

The first test was done on the converter without blowing any air on the heat pipes. The power loss on the ETO was 500 Watts, which means that the flow into each heat pipe was about 250 Watts each. Here again it is assumed for simplicity that out of the switching junction of the ETO, equal heat flows towards the cathode and the anode side of the ETO. The temperature of the cathode was recorded and is plotted in Figure 4-34. It is observed that the temperature of the cathode keeps rising, and the heatpipes are incapable in cooling down the ETO without any air flow. This shows that the thermal resistance of the heat pipe is very large with no air flow. This has been predicted by the curve on Figure 4-24, and is reproduced here in Figure 4-34. this plot

of thermal resistance of the heatpipe versus air flow rate tells us that at no air flow rates we can expect a very large thermal resistance of the heatpipes.

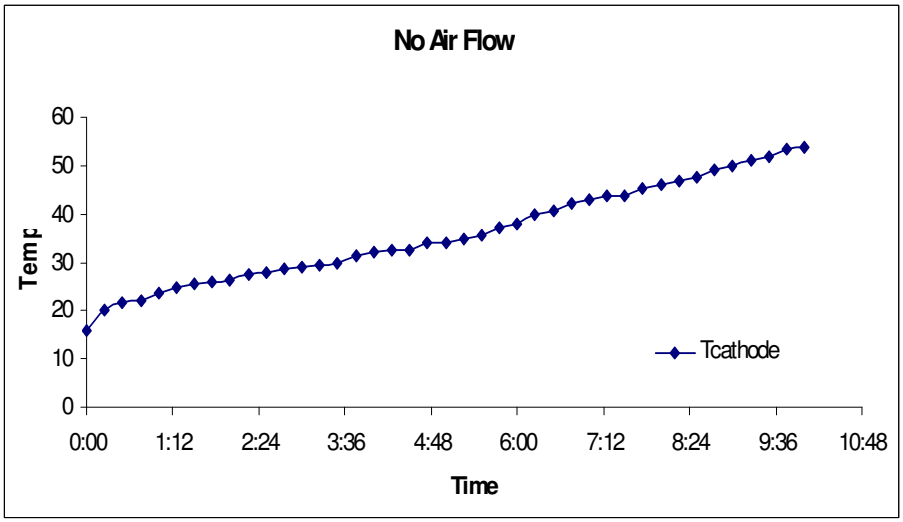


Figure 4-34. Temperature profile across cathode of ETO with 500W power loss on ETO, with no air flow on heatpipes

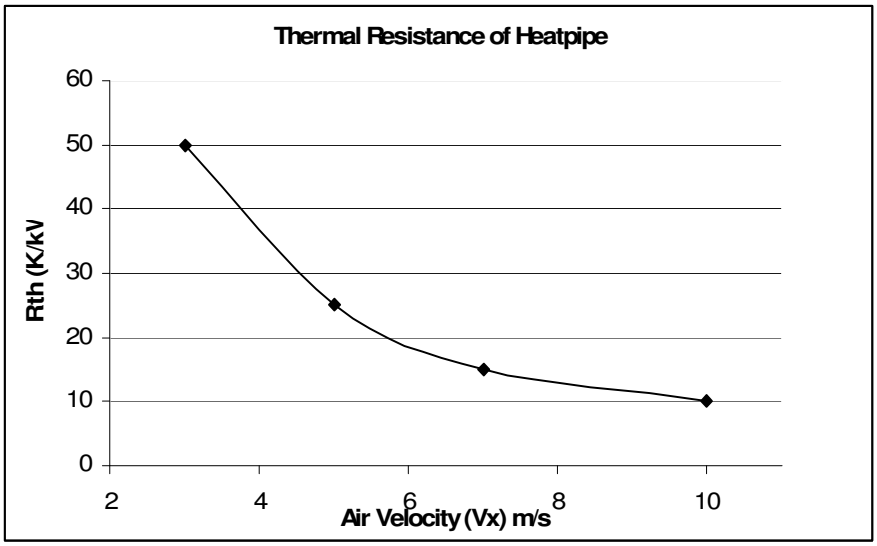


Figure 4-35. Simulated Thermal resistance variation of heat pipe with cooling air flow rate

Unconstrained air flow on the heat pipe surface tends to lead to non uniform air distribution on the fin surface of the heat pipe. This is because air has the tendency to flow through low pressure

areas, and if air is not forced to flow in a tunnel or duct onto the fins of the heat pipe, it just blows through the sides of the heat pipe.

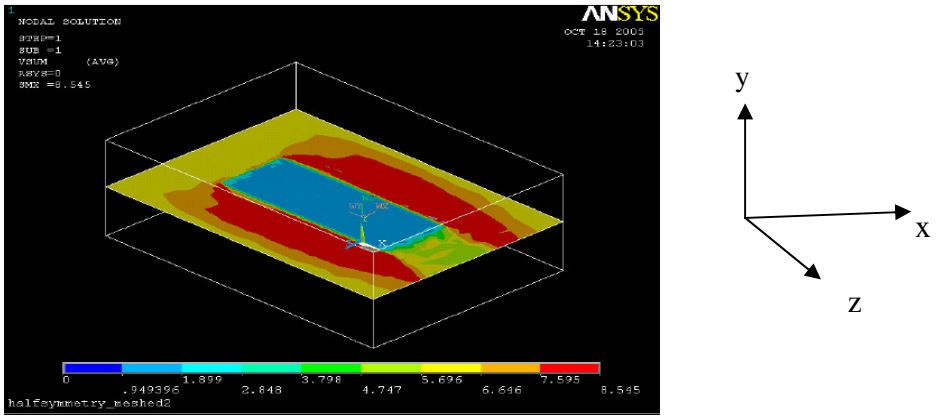


Figure 4-36. Unconstrained Air flow (without ducts) through a heat pipe as simulated on Ansys

This is illustrated in Figure 4-36, which is an Ansys simulation result of air flow on a heat pipe model. We see the velocity of air across a cut out section along the length of the heatpipe, with air flowing on it from one side in the positive Z direction. The large cube represents the air flow volume of the simulation. We can see that the average Z component of air velocity inside the fins of the heat pipe (blue color) is really low, around 1m/s when the air flow is about 6m/s coming out of the fan. Most of the air just flows through the sides of the heat pipe, without entering the fins, and this is the red colored part on the ansys simulation. These results can be somehow improved if we can constrain the air flow to take place through the fins. This can be done by creating some kind of a duct or a tunnel exactly of the size and dimensions of the radiating area of the two heat pipes, and blowing air through them. Thus the air would not escape out through the low pressure areas around the heatpipe fins, and would be forced to flow through the fins.

In Figure 4-37, we see the heat pipes being subjected to air from a single large fan placed behind them, with no duct or tunnel. The blue rectangle represents the air flow profile coming out of the

fan. The numbers represent air velocity in meters per second on the particular area. The velocity of air coming out of the fans towards the heatpipes is 4.5 m/s. The air velocity on the sides of the heat pipes is really small, around 0.6 meters per second. In the middle of the two heat pipes, the velocity is slightly higher, around 2.5 meters per second. This setup was used and the test was repeated with the boost converter. The non uniform air flow was used to cool the ETO, which was operated in the Boost converter to generate a loss of 500 Watts. With 250 watts flowing into each heat pipe, the temperature on the cathode is sensed and plotted in Figure 4-38. It is seen that the rise in temperature up to steady state is about 30 °C. We can thus calculate the thermal resistance of the heat pipe from the cathode of the ETO to the ambient as 100K/kW. This is really high, which indicates that we need directed air flow on the heat pipes in order to provide faster air flow on the fins of the heatpipes in order to extract the best performance out of them.

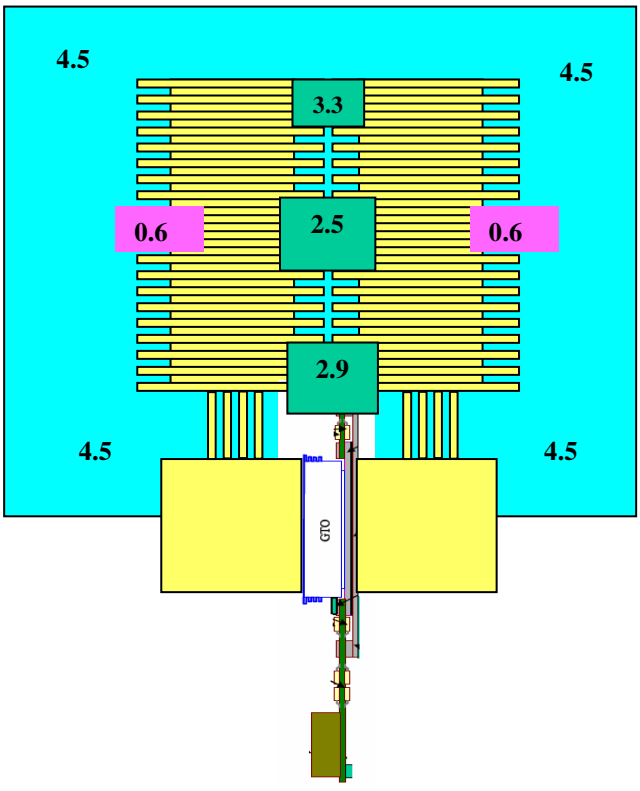


Figure 4-37. Air flow through heat pipes on the boost converter with single fan without duct

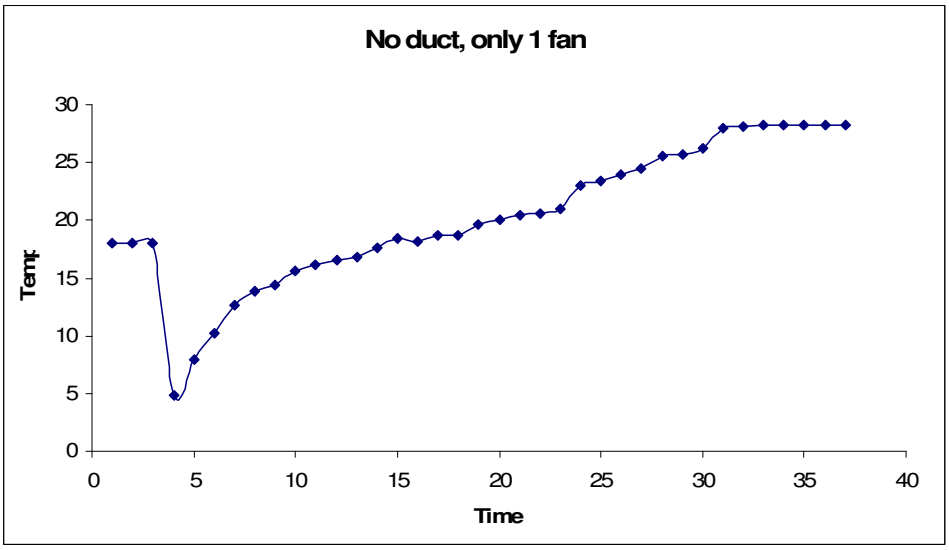


Figure 4-38. Temperature across cathode with 500W power loss on ETO, and cooling from single fan blowing undirected air flow on the two heat pipes at 4.5m/s

Ducts were created around the heat pipes from the fans to concentrate air flow on the heat pipes so that it does not escape from the sides of the heat pipe fins. The walls of the duct reduced the air flow volume represented by the outer black rectangle in Figure 4-39 to the smaller rectangle, thus concentrating air flow on the fins. Also, two fans were used, one on either side of the structure, with one pushing air into the duct, and the other pulling it out. The velocity of air at different points in the boost converter stack is shown in the figure below. We can see that the velocity is much better than without ducted air flow. The velocity on the sides of the fins is about 4.3 meters per second, and in the center of the structure is about 3.6 meters per second.

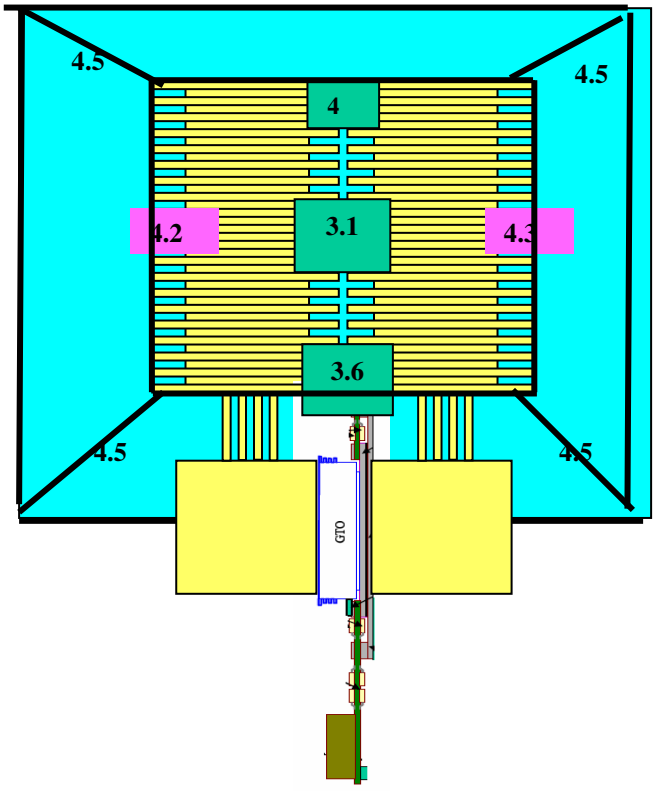


Figure 4-39. Air flow through heat pipes on the boost converter with double fans blowing directed air through duct

With this setup, the ETO was switched at 1 kHz in the same boost converter, with different output voltages and currents, to generate different power loss. The thermal response of the system is plotted in terms of the cathode temperature of the ETO at different power loss levels. The converter is run at a particular loss level until the temperature reaches steady state. The curve is plotted in Figure 4-40 as shown below.

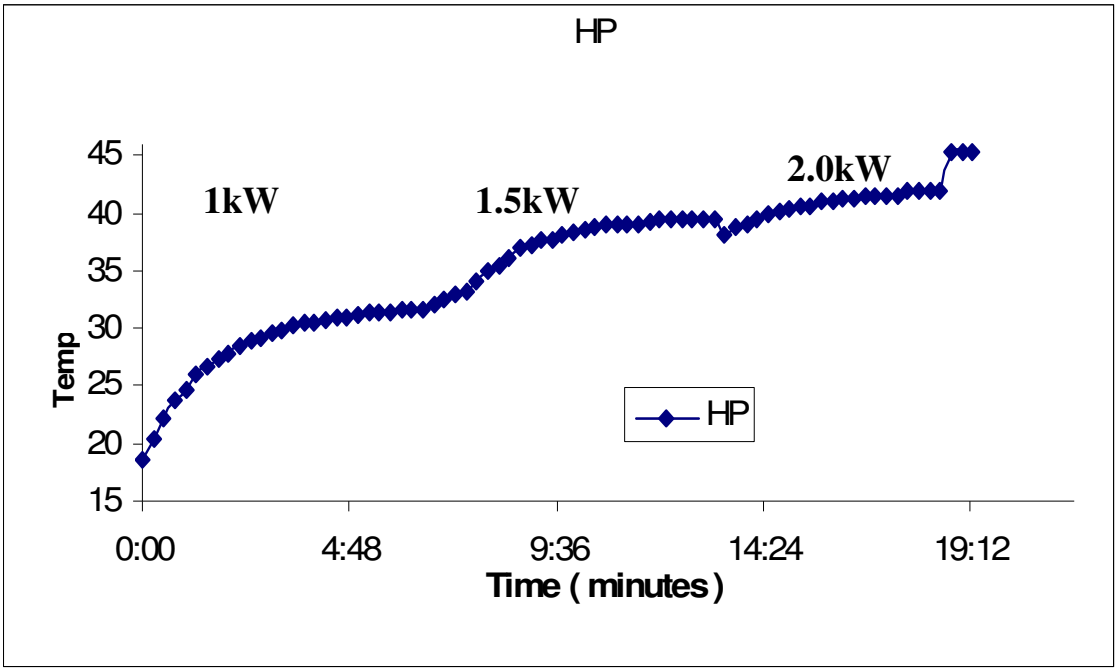


Figure 4-40. Cathode temperature versus time for different power loss, with double sided cooling on the ETO using heatpipes subjected to ducted air flow

Figure 4-40 shows that the cathode temperature reaches steady state within approximately 5 minutes every time the power loss level is increased. The cathode temperature at steady state condition with power loss of 1kW, 1,5kW and 2kW is 33, 38 and 42 °C respectively. From the above results we can calculate the thermal resistance of the heat pipes from the cathode of the ambient air. In the above test, the ambient air flow is about 18 °C, and the temperature at the cathode is 30 °C, at a power loss of 1kW. So the thermal resistance is about 24K/kW. But this includes the thermal resistance of the contact between the ETO and the heat sink of the heat pipe, since the measurement point is the cathode of the ETO and not the heatsink itself. If we assume it as 4K/kW, we get the thermal resistance of the heat pipe from its case to the ambient as approximately **20K/kW**.

The above test results are also compared with water cooling results. The test is basically done on the same boost converter, with the heat pipes replaced with water cooled heat sinks that are

cooled with the help of a chiller. This boost converter was also used in previous tests such as those documented in section 2.2. The ETO is subjected to similar power loss in both cases, and the temperature of the cathode is recorded using thermocouples.

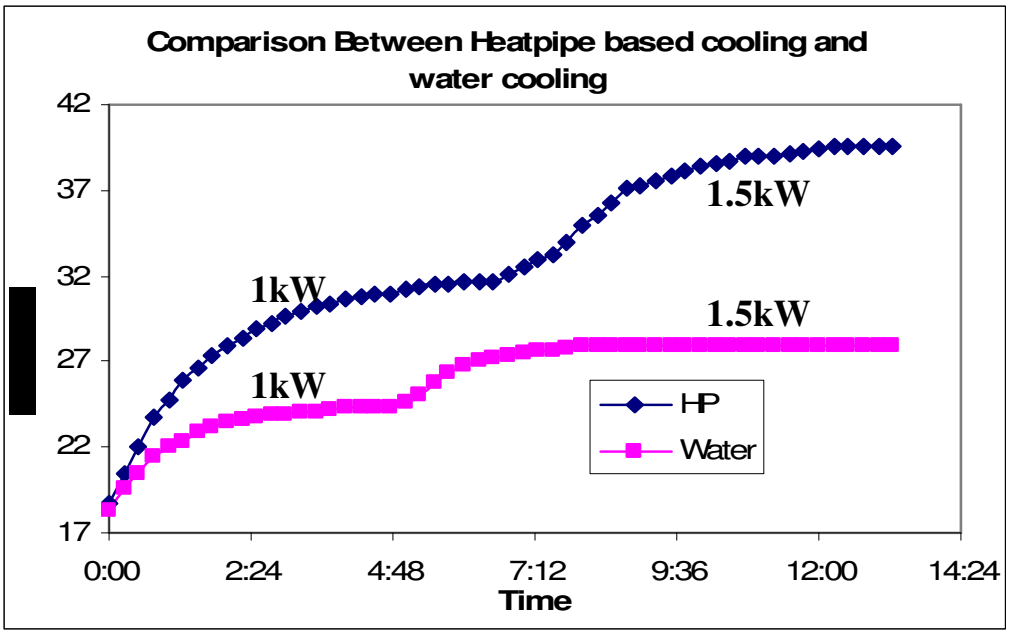


Figure 4-41. Comparison of performance of water cooling and air cooling using heat pipes at different power loss levels (cathode temperature versus time)

It can be seen from the above curves that the temperatures at steady state for same loss are lower in the case of water cooling than heat pipe based air cooling. For example, at 1kW power loss, the ΔT in the case of water cooling is about 7 °C, indicating a thermal resistance of about 14 K/kW from the cathode to the inlet water. In the case of heat pipe based air cooling, the delta T is about 13°C, indicating a thermal resistance of about 26K/kW from the cathode to the ambient inlet air from the fans. So the thermal resistance of the heat pipe based cooling from the ETO case to the ambient is roughly twice that of water based cooling.

However, the thermal resistance from the ETO junction to the ambient still needs to be calculated. As mentioned before in chapter 2, the thermal resistance of the water cooled ETO at 2 liters per minute is 24.7K/kW. Also, the distribution of the thermal network was discussed and shown in Figure 2-10. It was discussed earlier in Chapter 2 and shown in Figure 2-9 that due to unequal areas of contact at the anode and cathode side between the ETO case and the heat sinks, which is in the ratio of 1:2, the thermal resistance of the top heat sink is much higher than the bottom heat sink, almost in the ratio of 2:1. Due to this, the advantage of a lower thermal resistance of the water cooled heat sink is offset at the anode side due to a large Rth from the upper heatsink to water of around 20K/kW. In the case of the heatpipe, the contact area between the heat sink of the heat pipe and the ETO on the anode and cathode side is almost the same, and is in the ratio 3.141:4. As a result, the thermal resistances of the two sides are almost same. If we assume a contact thermal resistance of 5K/kW between the heat pipe and the ETO, then the total thermal resistance network becomes as shown in Figure 4-42. The total thermal resistance comes out to be about 27K/kW, which is almost comparable to that obtained with water cooled heat sinks. It is worth mention here that this thermal resistance is obtained at 4.5 meters per second of air flow with ducts to control flow of air through the fins of the heat pipe. This value can be improved if air flow rate can be improved. Also, if the air flow rate drops down, the thermal resistance number can be deteriorated significantly, with the trend shown in figure xx.

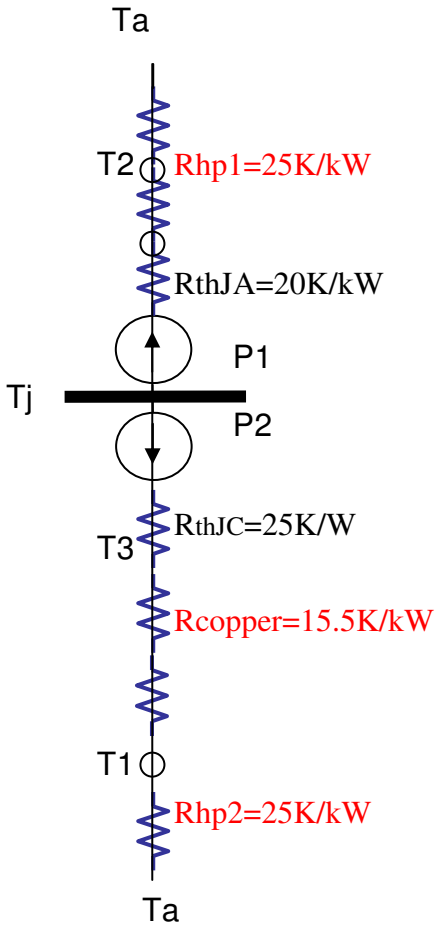


Figure 4-42. Thermal resistance network of ETO with heatpipes

CONCLUSION

The Emitter Turn Off Thyristor (ETO) is a very promising high power device with tremendous potential for extensive use in the Power Electronics industry. The ETO is turned off under hard driven conditions, has a large reverse biased safe operating area (RBSOA), built in sensors for over-current protection, and has fully optical control. These factors and many more make it a strong contender for use as a switch in many FACTS applications.

This thesis highlights the good thermal characteristics of the ETO, and also the excellent loss characteristics. Dependence of switching loss, conduction loss and leakage loss on junction temperature is studied. Switching loss and conduction loss show good linear variation with temperature, even at high values of operating junction temperature. Leakage loss presents an exponential rise with temperature, with low value till about 150 ºC, beyond which it becomes a major part of the total loss of the ETO. The thermal stability of the device is studied by building a closed loop thermal model which incorporates the loss characteristics and the thermal resistance model of the device. This model is used to predict the high temperature operation limit, which is dependent on the thermal stability of the device. It is seen that it is the leakage loss rise with increasing junction temperature that contributes to thermal instability at high temperature. The closed loop thermal model shows that the ETO should operate with thermal stability up to 165-170 ºC junction temperature at a total loss of around 5kW. This is experimentally corroborated by running the ETO in a boost converter configuration and generating high loss, and the ETO runs at steady state operating junction temperature in excess of 165 ºC for a long duration.

Multilevel Voltage Source Converter (VSC) structure has been developed in the industry to overcome inadequacy in power semiconductor voltage ratings so that they can be applied to high-voltage electrical systems such flexible AC transmission systems (FACTS) and custom power system applications. Out of the three well-known multilevel voltage source converters; the diode-clamped converters, flying-capacitor converters and cascaded converters with separated dc sources, the cascaded converter is the most advantageous. Clamping diodes and balancing capacitors, are not needed in the cascaded multilevel converter which implies fewer main components. Moreover, the cascaded converter has the same structure for each level; the desirable power rating of the system can therefore be simply adjusted by connecting a different number of the identical modules. This thesis presents the design methodology and analysis of a new modular design voltage Source converter (VSC) for FACTS applications. Possible improvements in conventional water cooled VSCs are studied and targeted as features to be incorporated in the new VSC. One of the main improvements is the use of air cooled heatpipes to cool the different loss (heat) producing components in the VSC, and many advantages are presented. The design is to be based on and use the advantages of the Generation IV ETO such as fully optical control, voltage/current sensing capability and self gate drive power generation capability. A simplified voltage clamp and di/dt snubber is to be used in the new design.

In order to design the heatpipe based cooling system, loss calculations are done for the VSC based on application as a STATCOM taking 125 ºC junction temperature as a design criterion. Based on loss calculations for the ETO and the anti parallel diodes, maximum heat flow into the heatpipes is calculated. 3D finite element simulations are done on different models developed for the heatpipes to understand the working of the heatpipe and to gain knowledge of the expected thermal resistance. A thermal resistance of 20K/kW is predicted from the case to the ambient at

6m/s air flow rate. Heatpipes are procured and tested using a Boost converter topology, in which two heatpipes are used to cool an ETO which produces the desired amount of heat. The thermal performance is shown to be excellent by making the heatpipes cool large amounts of heat. In order to verify the validity of the stack design for the VSC, thermal simulations are done in order to predict the junction temperatures at worst case losses. It is seen that the junction temperatures of the ETOs and diodes in the VSC operating with worst case losses in STATCOM mode at Vdc=1.5kV, Irms=1.4kA and fsw=600Hz remain well below 125 ºC.

Heatpipes operating in vertical position with fans blowing ducted air at 4m/s act as excellent cooling devices, with capability to dissipate large amounts of heat. Autocad design of the converter is done, including the clamps, ETOs, diodes, heatpipes and RCD clamp. A converter with dimensions 750mm X 950mm X 700mm is designed, which is small compared to conventional VSCs that employ traditional water cooling. Centrifugal fans are to be used as the main cooling fans for the individual heatpipes, having the advantage of better back pressure.

A novel heat pipe based cooling system is thus designed for high power VSC using the ETO. With the use of heat pipes in the cooling system, we can eliminate many disadvantages of water cooling methods, such as isolation issues, need for a big heat exchanger and chillers, low reliability, maintenance costs etc. Heat pipes help in increased reliability of the system as they are totally passive devices. Larger power density levels can be realized by their use, as the size of the modular VSC is much smaller. Junction temperatures can be controlled by regulating the external air flow rate on the heatpipe.

REFERENCES

[1] Bin Zhang, Yunfeng Liu, Xigen Zhou, Josh Hawley and Alex Q. Huang, *"The high power and high frequency Operation of the emitter turn off thyristor*" Industrial Electronics Society, 2003. IECON'03. The 29th Annual Conference of the IEEE Volume 2, 2-6 Nov. 2003 Page(s):1167 – 1172

[2] Y. Li, A. Q. Huang and F. C. Lee, "Introducing the Emitter Turn-Off Thyristor (ETO)," IEEE Industry Applications Society 33st Annual Meeting Oct. 12-15, 1998, pp. 860-864.

[3] Yuxin Li, Alex Huang, and Kevin Motto, "Experimental and Numerical Study of the Emitter Turn-off Thyristor," IEEE Transactions on Power Electronics, Vol.15, No.3, pp561-574, May 2000.

[4] Kevin Motto, Yuxin Li, Zhenxue Xu, and Alex Q. Huang**, "**High frequency operation of a megawatt voltage source inverter equipped with ETOs", APEC 2001. Sixteenth Annual IEEE , Volume: 2 , 2001Page(s): 924 -930 vol.2.

[5] B.J. Baliga, Power Semiconductor Devices. Boston, MA: PWS publishing, 1995, p433

[6] Datasheet IGCT 5SHY35L4511, 5SHY35L4503

[7] Kuang Shen*, "Thermal Stability of high frequency IGBT operation",* IEEE transactions on industrial electronics, VOL 47, No1, page9

[8] Dewei Xu, Haiwei Lu, Lipei Huang, Satoshi Azuma, Masahiro Kimata, and Ryohei Uchida, *"Power LossAnd Junction Temperature Analysis ofPower Semiconductor Devices",* IEEE transactions onIndustry applications, VOL 38, No5, page1426

[9] S. Clemente*, "Transient thermal response of power Semiconductors to short power pulses",* IEEE Trans. Power Elec. Vol.8, 1993, pp.337-341

[10] B. T. Ooi, G. Joos, and X. Huang, "Operating principles of shunt statcom based on 3-level diode-clamped converters," IEEE Trans. On Power Delivery, vol. 14, No. 4, Oct. 1999, pp. 1504-1510.

[11] F. Z. Peng, J. S. Lai, J. McKeever, and J. VanCoevering, "A multilevel voltage-source inverter with separate dc sources for static var generation," IEEE Trans. on Ind. Appl., vol. 32, No. 5, Sept.-Oct. 1996, pp. 1130-1138.

[12] K. V. Patil, R. M. Mathur, J. Jiang, and S. H. Hosseini, "Distrubution system compensation using a new binary multilevel voltage source inverter," IEEE Trans. on Power Delivery, vol. 14, No. 2, April 1999, pp. 459-464.

[13] W. McMurray, "Efficient snubbers for voltage-source GTO inverters," IEEE Trans. on Power Elec., vol. PE-2, No. 3, July 1987, pp. 264-272.

[14] J-S Lai and F. Z. Peng, "Multilevel converters – a new breed of power converters," IEEE Trans. on Ind. Appl., vol. 32, No. 3, May/June 1996, pp. 509-517.

[15] A. Nabae, I. Takahashi, and H. Agaki, "A new neutral-point-clamped PWM inverter," IEEE Trans. on Ind. Appl. vol. IA-17, No. 5, Sept./Oct. 1981, pp. 518-523.

[16] P. M. Bhagwat and V. R. Stefanovic, "Generalized structure of a multilevel PWM inverter," IEEE Trans. on Ind. Appl., vol. IA-19, No. 6 Nov./Dec, 1983, pp. 1057-1069.

[17] K. V. Patil, R. M. Mathur, J. Jiang, and S. H. Hosseini, "Distribution system compensation using a new binary multilevel voltage source inverter," IEEE Trans. on Power Delivery, vol. 14, No. 2, April 1999, pp. 459-464.

[18] Siriroj Sirisukprasert, Zhenxue Xu, Bin Zhang, Jason Lai, and Alex Q. Huang, "A High-Frequency 1.5 MVA H-Bridge Building Block for Cascaded Multilevel Converters using Emitter Turn-Off Thyristor", IEEE2002

[19] Siriroj Sirisukprasert, Yunfengliu, Zhenxue Xu, Bin Zhang, and Alex Q. Huang, etc. "Power Stage and Control Design for the ETO-Based Cascaded-Multilevel Converter for FACTS Application", IEEE2003.

[20] Karan Tewari, Alex Huang, Bin Chen, Ding Li, Subhashish Bhattacharya," Investigation of the high temperature operation of the Emitter Turn off Thyristor", Industrial Electronics Society, IECON 2005

[21] ABB fast recovery diode 5SDF 10H4502 datasheet

[22] "About Heat pipes", Thermacore International