ABSTRACT

RAMAMURTHY, ANAND. Flexible Digital Electrical Power System Design and Modeling for Small Satellites. (Under the direction of Dr. Subhashish Bhattacharya.)

This thesis presents an optimum design and complete modeling of a small satellite power system. The key idea is to create a modular design which is flexible, scalable and applicable for higher power systems with the same architecture. Centralized power system control architecture is proposed for the satellite power system. The basic idea behind the architecture is to digitally control multiple power stages with a single high performance controller. The satellite power system stores solar energy in energy storage devices and distributes the energy to different satellite sub systems. Applying digital control techniques makes the system design flexible and also makes it modular. A wide input synchronous buck-boost based flexible battery charging module (FBCM) is proposed which efficiently integrates the solar panels to the batteries. The FBCM is followed by a digitally programmable flexible point of load module which essentially provides the regulated DC bus for the satellite sub systems.

This thesis also focuses on the system modeling aspect of energy storage, power conversion and digital power control involved in the satellite power system. The energy storage device, mainly Lithium based batteries were modeled at different state of charges (SOC) using Electro chemical Impedance Spectroscopy (EIS). EIS based impedance measurements were fitted to a standard electrochemical battery model. The AC impedance model of the battery was integrated to the power supply control loop. The battery impedance

changes with SOC of the battery and its effect on the control loop was observed. Based on the battery impedance based control loop performance, a dynamic compensation technique was proposed to optimally stabilize different control loops in the battery charging cycle. The system model and design aspects were verified using a synchronous buck based charging system and a non synchronous boost based charger. A labview based user interface was designed for the power modules to enable the user to re-program, optimize and design the power system.

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Flexible Digital Electrical Power System Design and Modeling for Small Satellites

by
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DEDICATION

I dedicate this work with humility to the Almighty Lord.

BIOGRAPHY

Anand Ramamurthy was born on 7th November, 1983, in Chennai, India. He received his Bachelors degree in 2005 in Electrical Engineering from the Shanmugha Arts Science Technology Research Academy, Thanjavur, India. In fall 2007, he started his graduate studies in the Department of Electrical and Computer Engineering at North Carolina State University, Raleigh, North Carolina, USA. From 2005-2007 he worked as an Applications Engineer for Texas Instruments ODC, India. He was a product applications expert for microcontroller product line focusing mainly on power electronics applications. He subsequently worked on power management analog integrated circuits like PWM controllers and DC/DC converters. In the summer of 2008, he worked for Intersil Corporation, as an applications intern designing multi-phase high current DC/DC converters for compute applications. His research interests include AC/DC, DC/AC, Solar Power Management, multi-phase high current VRM applications, Memory power circuits, Battery power management and LED Lighting applications.

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I thank members of the PMM group for inspiring me with very lively group discussions. My special thanks go to Mr. Liyu Yang, Mr. Tiefu Zhao, Mr. Xiaohu Zhou, Mr. Gaurav Bawa, Mr. Zhigang Liyang, Mr. Gang Yao Wang and Mr. Jinseok Park for always being there to have discussions about my research. I thank Mr. Li Nan an exchange student from Zhejiang University who helped me develop the Flexi-sat Digital Power Designer Software. I also thank my friends Sameer Mundkur, Shoabhik Doss, Vishal Khawarey, Vikas Kumar, Aditya Ramachandran and Sachin Pawar for making my stay at NC State University a memorable experience.

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1.Introduction

1.1 Background and Motivation

The success of the small satellite industry has paved the way for increased capability of small spacecrafts. Currently, small spacecrafts are being used as teaching tools by many universities and organizations all over the world, but commercial and scientific applications are now becoming a reality on these very small satellite platforms. Small satellites are increasingly used in science and exploration missions that include astrophysics, astrobiology, space physics, lunar sciences etc. They also act as a platform for technology demonstrations in the field of propulsion, communication, mass reduction- MEMS, autonomous operations, novel space architectures and power switching devices.

It is possible to construct a modular space craft using a number of modules with identical mechanical and electrical interfaces, but with each performing a specific function to achieve its required tasks. Figure 1 shows the different subsystems present in a small satellite. Each of the subsystem modules work together and they communicate with each other for the proper functioning of the system as a whole.

The concept of modularity enables a responsive and flexible space craft design. This thesis will focus mainly on the design of a modular space craft power system which enable the proper interface of the energy source and energy storing devices and in turn provides adequate power to the satellite subsystems.

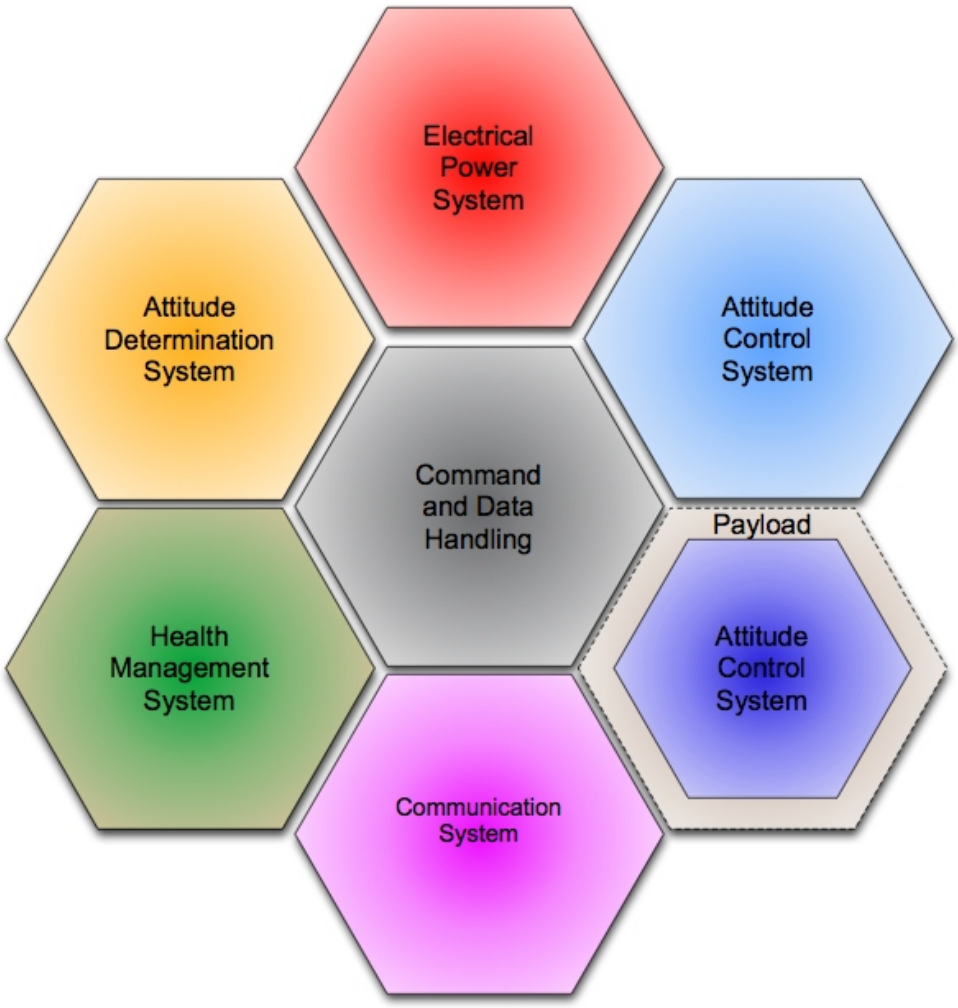


Figure 1 Small Satellite Subsystems

Photovoltaic cells forms the major source of energy and rechargeable lithium ion batteries acts as the energy storage device. Small satellites can have a range of power requirements from as little as a watt or two, to a few kilo watts. Despite this extensive range of power requirements, a typical mission will be launched into a low earth orbit and the majority will have fixed solar array that encounter varying solar illumination characteristics across a typical orbit. Most will also experience frequent eclipse periods. [1][2][3]

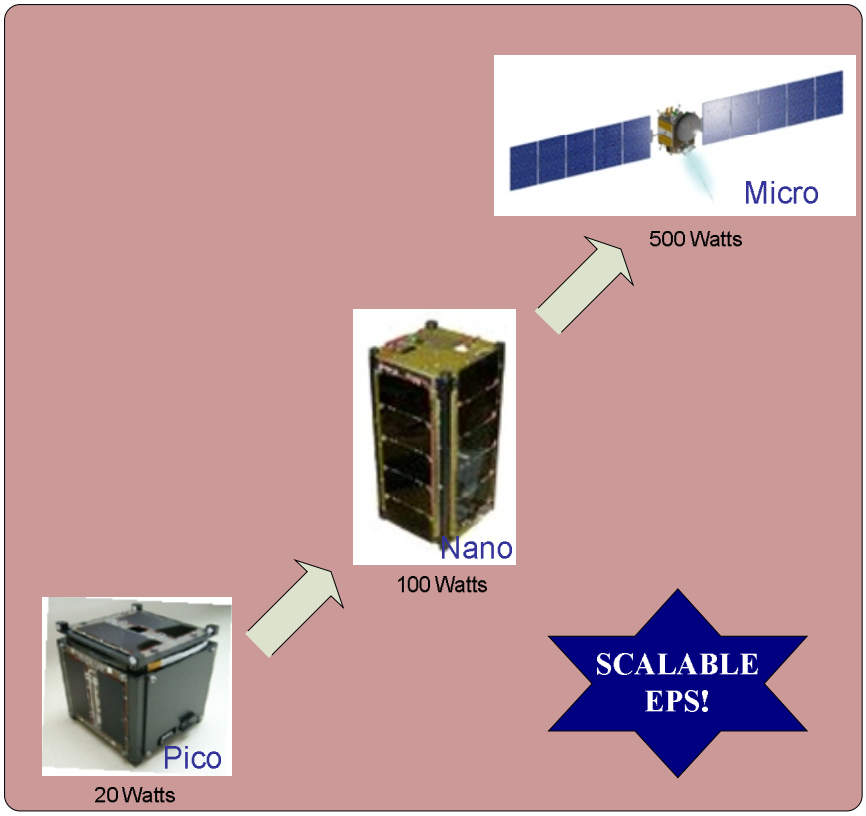


Figure 2 a Scalable Electrical Power System

The challenge for the power supply designers is to design a system that can handle multitude of mission profiles and be scalable in power handling capability. What is essentially in demand is an efficient, low mass/volume system which is a flexible design that avoids the need of system redesign with each set of mission requirements. Figure 2 shows the different types of small satellites and their power requirements.

The motivation of this thesis is to illuminate the design and modeling aspects of a flexible electrical power system that caters a range of power requirements but yet provides a seamless interface and support to the satellite subsystems.

1.2 Thesis Organization

The thesis has been organized as follows: Chapter 2 describes the power system architecture of small satellites. The power delivery path, battery charger topologies and point of load converter systems are discussed. After the power system architecture, each of the power system components is modeled and their behavior at different operating conditions is derived. The DC/DC power stage topology open loop and closed loop control models for charge control and point of load voltage conversion is discussed in Chapter 3. In Chapter 4 the main energy storage device- Lithium batteries are modeled at various states of charges. The behavioral model of the battery holds the key to a proper closed loop operation. In Chapter 5, the maximum power point tracking techniques and details about photovoltaic cells are discussed. In Chapter 6, digital control and compensation techniques are discussed. Quantization effects of the digital components in the control loop path is analyzed and modeled.

The key to flexibility and scalability is the ability to reconfigure the system as suited to the application. In Chapter 7, the Flexi-DC digital power system designer software is described. The software is essentially used to assist in the closed loop design and compensation. The system parameters are given as inputs to the software and the compensation parameters are determined. Then the system information is programmed into the memory of the digital controller based platform. Experimental results of a synchronous buck and non-synchronous boost based battery charging module is also discussed. Finally, Chapter 8 contains the conclusions of the thesis with scope for future work.

Chapter 2

2. Satellite Power System Architecture

2.1 Introduction

The goal is to create a smart power system for small satellites which adapts to mission power requirements. The power management system should offer flexibility, scalability and reliability**.** A modular design approach with plug-and-play operation is proposed in this work which offers a complete digital power management with sophisticated control approaches for more efficient and reliable operation. The architecture focuses on efficient interface of the solar panels to the energy storage devices as well as supplying to the load. Various design approaches and power stage architectures are discussed in this chapter.

2.2 Power Generation and Availability

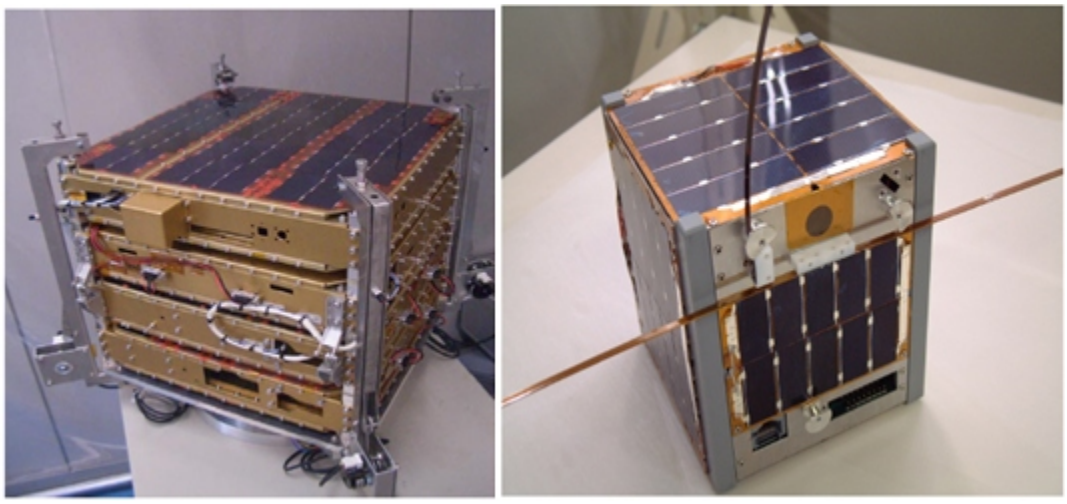


Figure 3 SOHLA-2, University of Tokyo and 1U-Cubesat from Clyde space, Inc

The Figure 3 left picture shows a 1U (10cmx10cmx10cm) cubesat with a usable exposed area of 500cm^2 for the solar panel to be mounted over its side. The picture in the right is also a microsatellite class spacecraft with a larger area for mountable solar panels. Of the available solar cell technologies, the GaInP2/GaAs/Ge multi-junction cell is the only real alternative for a miniature spacecraft. The multi-junction solar cell is highly efficient and also has a terminal cell voltage of 2V which is at least double that of all the other cell technologies like single junction GaAs and silicon [1].

In the LEO (Low earth orbits) small satellite orbits the earth 16 times a day with an orbit period of 90 minutes. Each orbit has a sun time of 60 minutes and has eclipse time of 30 minutes. The average load power available from the solar array also depends upon the number of faces of the satellite that is facing the sun. Most of the satellites do not have auto sun tracking systems so most of the times one to two of the faces are only facing the sun at any time. The usable power available might again be lowered by temperature changes that do not allow the solar panel to stay in its peak power point. The challenge for the power designers here is to efficiently convert the energy available and store them for use during the eclipse period. The mechanical structure of the satellite also creates challenges for the power designer to design the power conversion system that is as compact as possible in the mean time which are efficient and reliable [1].

2.3 Existing Satellite Power System Architecture

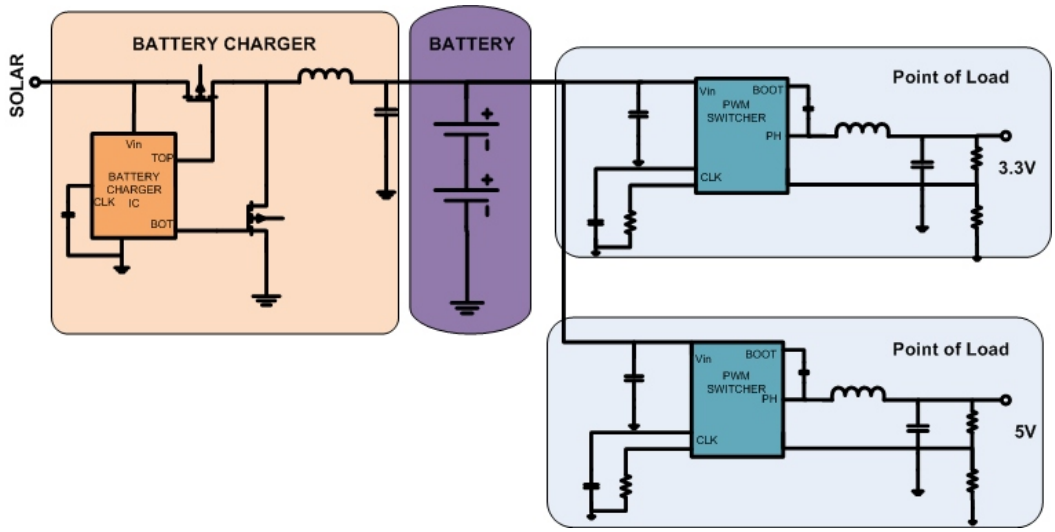


Figure 4 EPS Module for cubesat, block diagram.

2.3.1 Description

Figure 4 shows the block diagram of the electrical power system use in most of the small satellites. The EPS will have a micro-controller that monitors the health of the power system and communicates with the other subsystems. As shown in the block diagram, the highlighted blocks are the DC/DC converters for charging the battery and to provide the point of load voltage for the subsystem's regulated power bus. The highlighted battery charging stage is controlled by an analog controller, the point of load stage is a switching regulator. In this architecture, the solar panels are connected to the battery in a direct connection topology. It consists of two 3.7V Lithium Poly batteries in series and they have a regulated bus of 3.3V and 5V respectively.

2.3.2 Limitations of the existing architecture

1) The EPS is designed for a narrow input voltage range; the number of solar panels cannot be increased or decreased in order to suit a particular mission design.

2) The EPS is tailored to work for a 1U system and the same module cannot be used in a 2U or a 3U system.

3) Direct connection topology has been used and it has many disadvantages even though it is simple.

4) The architecture has DC/DC power stage controlled by integrated circuits for analog control which does not offer flexibility or scalability, it has its operating condition limitations and the designer is constrained by the analog circuitry/controller.

5) The point of load regulated power stage has the capability of supporting a fixed load and cannot support payload or special subsystems that might require a higher current level.

6) The control is de-centralized and the load shedding and power down/sequencing features might need additional circuitry.

2.4 Direct Connection and Path Selection Topologies.

2.4.1 Description

Two main topologies are commonly used for the electrical power system: direct connection and path selection topology. Direct connection topologies isolate the PV source from the battery pack and system by connecting the battery pack positive terminal and the charger stage output to the system power bus as shown in Figure 5. In such a system, the maximum power delivered from the PV panel to the system power bus is limited by the

charger settings; the PV power supply is isolated from the system power bus by the charger power stage.

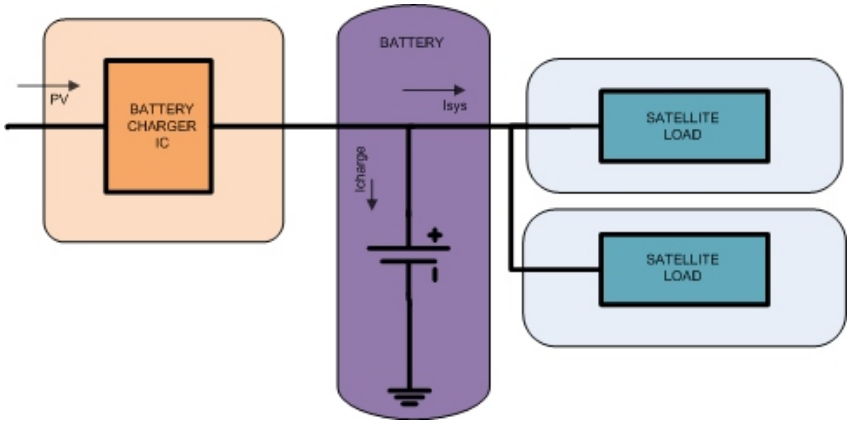


Figure 5 Direct Connection Topology

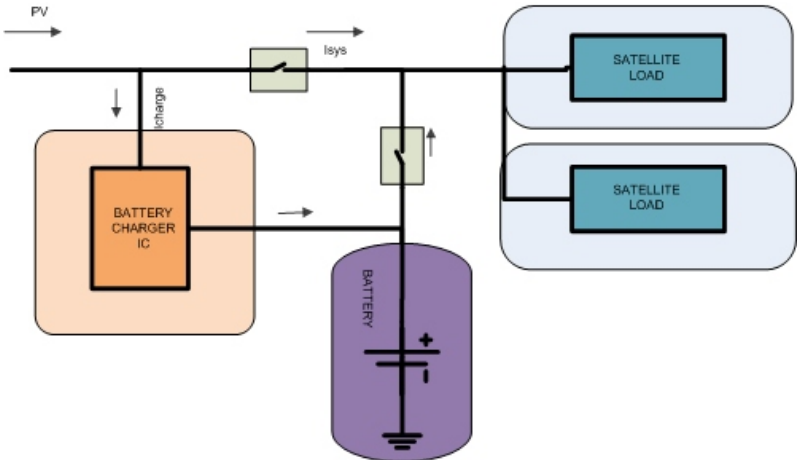


Figure 6 Path Selection Topologies

In path selection topologies, the input power is split between the charger stage and the system. As shown in Figure 6, the power sharing is made possible by the switching network that provides independent paths for the charger stage power and system power. The PV panel is directly connected to the system power bus.

2.4.2 Advantages of Direct Connection Topology

1) Some types of direct connection topologies achieve the highest efficiency when the system is powered by the battery most of the time, due to the elimination of the switch between the system and the battery.

2) Direct connection topologies are simpler and more cost effective.

3) The total charge current and the system current can be limited to a desired value by setting the charge current limit to a certain value.

2.4.3 Disadvantages of Direct Connection Topology

1) If the system always demands high current (but lower than the regulation current), the charging cycle never terminates. Thus, the battery is always charged, and the life time may be reduced.

2) Because the total current regulation threshold is fixed and the system always demands some current, the battery may not be charged with a full charge rate and thus may lead to a longer charger time.

3) If the battery voltage is too low, highly depleted, or totally dead or even shorted, the system voltage is clamped by the battery and it cannot operate even when the PV is present.

2.4.4 Advantages of Path Selection Topology

1) Capable of carrying high system load current.

2) The precharge, constant current fast charge, and termination functions all work well and are not affected by the system load.

3) Independent of each other, the system load does not impact the battery charger.

4) Even if the battery pack voltage is too low, for instance, highly depleted, the system still operates well as long as the input power is on.

5) Efficiency possibly higher than direct connection when there is significantly higher voltage difference between the input and system voltages.

2.4.5 Disadvantages of Path Selection Topology

1) The topology is more complex, and the cost is higher.

2) The efficiency can be affected when the battery powers the system due the loss due to the on resistance of the switch connecting the battery and the system.

3) Higher system line voltage variation range.

Considering the merits of the path selection topology, we opted to use the path selection topology for our flexible digital electrical power system.

2.5 Centralized Power System Architecture

The architecture that is proposed for a modular power system design is shown in Figure 7. The heart of the power system is a central controller that controls the other modular power stages in the system. The sub-modules of the power systems are the Flexi Battery Charging Module (FBCM) and the Flexi Digital Point of Load (FDPOL) module. The solar panel can directly charge the battery but it would result in an inefficient, unreliable way of charging the battery. The FBCM module charges the battery from the solar panel and also does it in such a manner that it extracts the maximum power from the solar panel. The FDPOL module then converts the unregulated battery voltage or the solar panel voltage to a regulated power bus that caters to the other sub-systems of the satellite. As mentioned before

the central controller forms the heart of the power control system. The central controller communicates with other subsystems like the communication subsystem, the command and data handling subsystem and also the payload. The connectivity of the power controller to all the other subsystems helps in maintaining the over all health of the power system and also makes it controllable from the ground station.

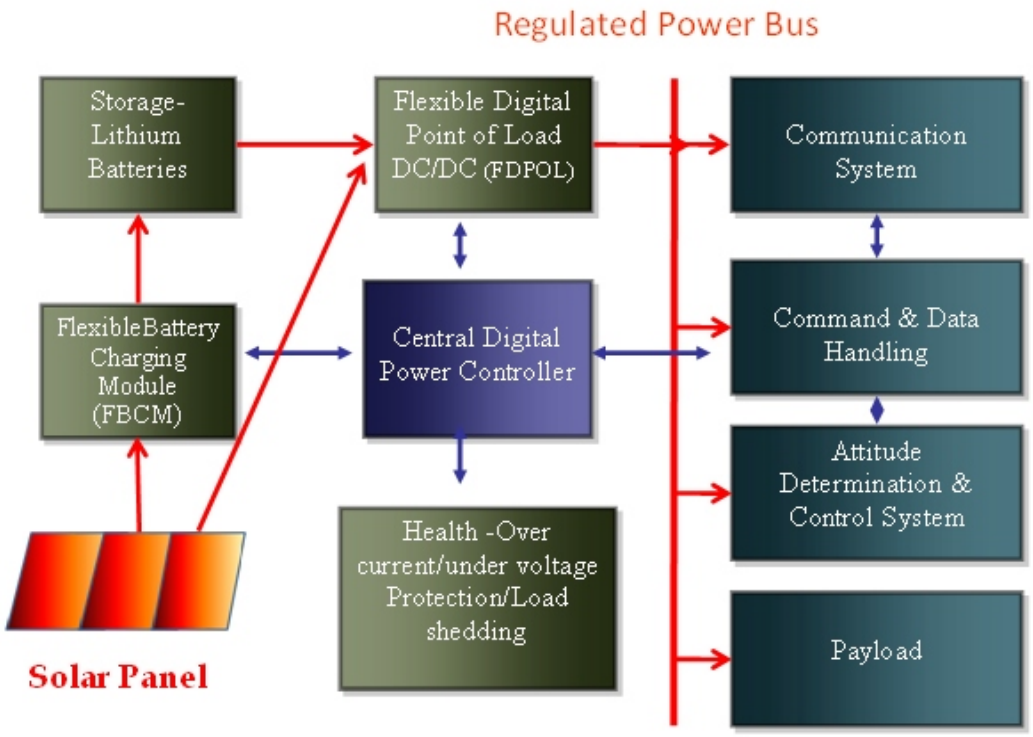


Figure 7 Centralized Power System Architecture for small satellites

2.6 Flexible Battery Charging Module (FBCM)

Figure 8 shows the Flexible Battery Charging Module structure as suited for a modular design option for small satellite. FBCM forms the critical interface between the

solar panels and the energy storage device. As already discussed in section 2.2, not all the solar panels mounted on the sides are facing the sun, hence we cannot possibly connect all the solar panels in parallel doing do will clamp the voltage of the solar cells to the lowest available voltage. The solution to this problem if we want to connect all the solar panels in parallel is to use the modular FBCM for a pair of faces together. Thus the FBCM can interface the solar panels to the batteries irrespective of the number of faces available. The Figure 8 also shows that solar panels of different voltages (9V,15V,25V) are interfaced to battery using the charging module.

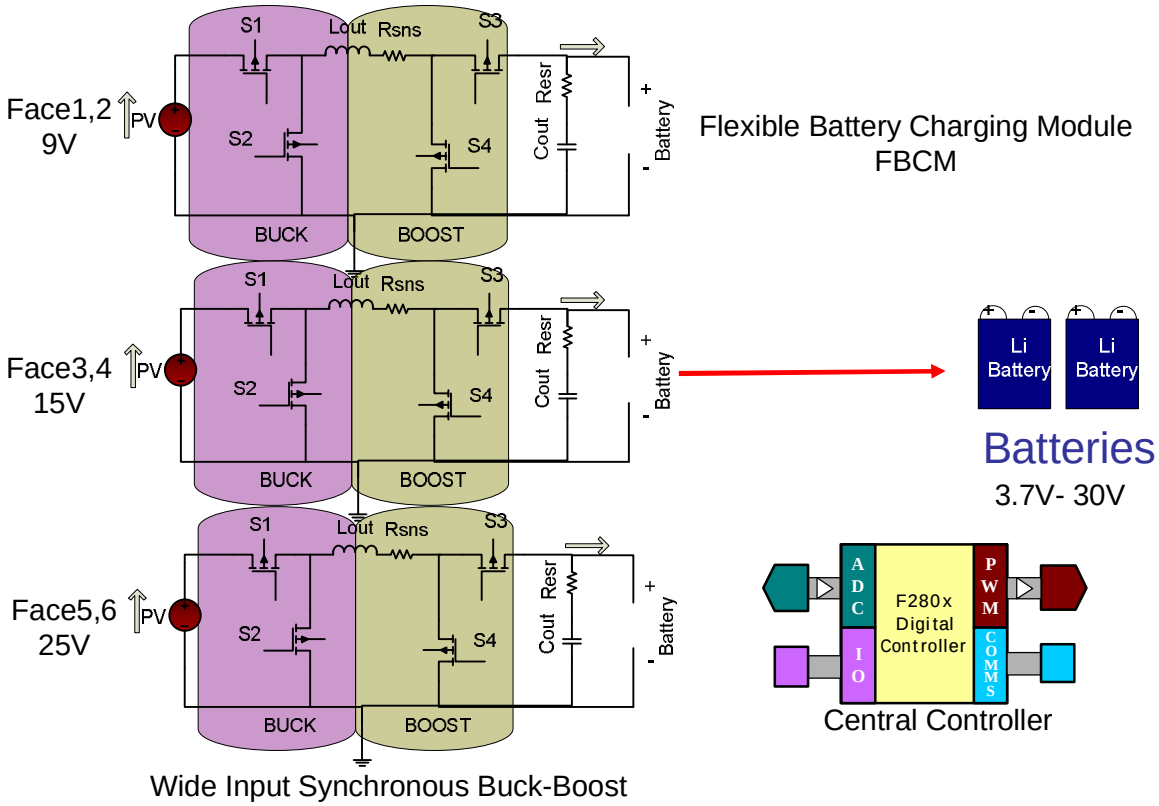


Figure 8 Flexible Battery Charger Module (FBCM) Structure

The FBCM directs all the energy to the storage cells, which are made flexible and for a wide range of voltages or number of batteries. The number of cells used in the small satellites usually varies with different missions and the type of payloads used. And thus the FBCM itself is a wide input-output converter that takes a wide range of input voltage as well as output voltage. The central digital power controller controls the power stage and also makes the power system flexible. The FBCM is user programmable using the Flexi-sat Digital Power Designer Software. The user can configure the FBCM with the required output voltage (battery voltage), the operating frequency, charging current and adjust loop compensation parameters.

2.7 Flexible Digital Point of Load Module (FDPOL)

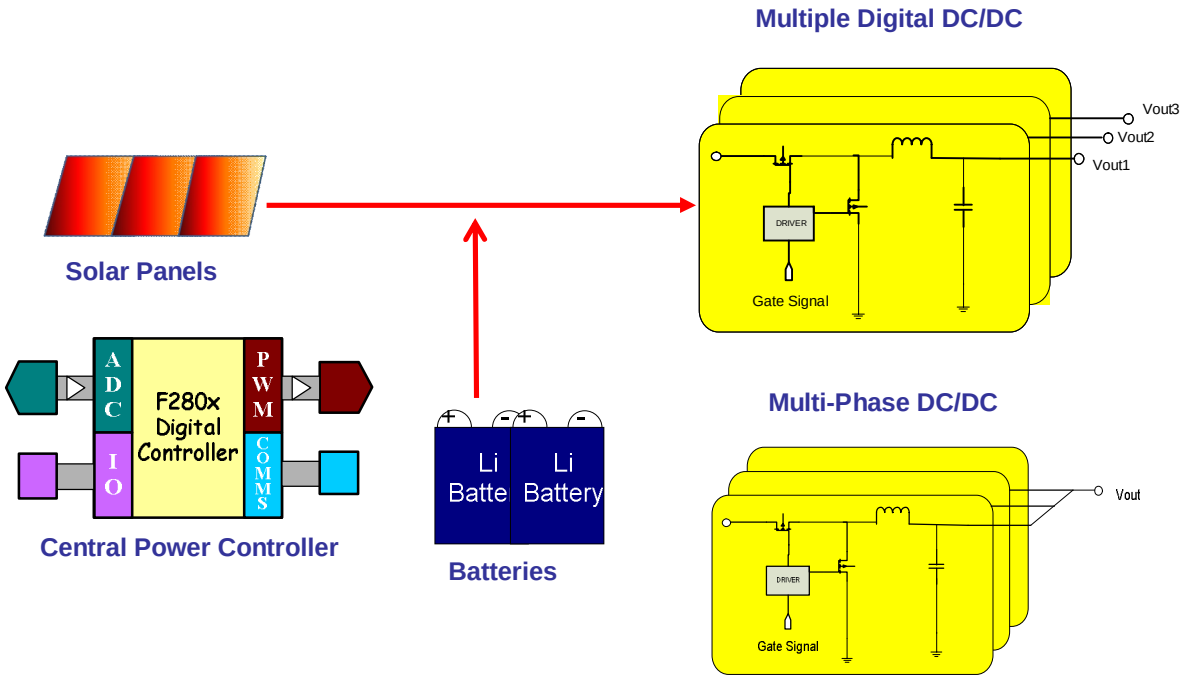


Figure 9 FDPOL modules providing regulated DC Bus for the satellite sub systems

In Figure 6 the block diagram shows the part of the path selection topology. During the sun time the FBCM modules are directly connect the solar panels to the battery. While during the eclipse time the batteries power the FDPOL power stages. This is shown in Figure 9. The switch is not shown here but both the solar panel and the battery is shown as the source for the FDPOL. FDPOL modules convert unregulated DC bus voltage from the battery and as well as the solar panel to a regulated DC bus. As the name suggests, these modules are made with the flexibility of changing the point of load voltages since they are digitally controlled. The most common voltages that are used are 1.8V, 3.3V, 5V, 12V and 15V etc. Since they are powered from both solar panel and the battery the FDPOL modules it is made suitable for higher system line voltage variation range.

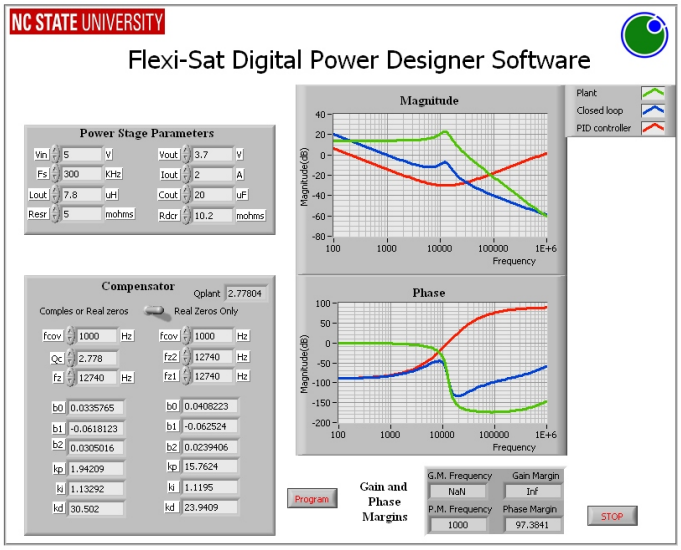


Figure 10 Flexi-sat Digital Power Designer Software configuring the FDPOLs

The central controller can control 10 independent PWM signals and hence they can support 10 independent power stage phases. Out of these phase they can be easily paralleled for applications that require higher currents. Parallel operation of FDPOL is quite simpler

because of the digital controller feature and also since it is a voltage mode controller, there is no requirement for current sharing. Typically there are 3 BCM modules and there are 7 slots allotted for the FDPOL modules. The FDPOL operation is programmed by the Flexi Digital Power Designer Software which allows the user to program the regulated voltage, current and switching frequency, independent modules and which modules are paralleled. Figure 10 shows how the FDPOL is configured using the flexi-sat software.

Chapter 3

3. Power Stage Modeling

3.1 Introduction

The power topology selection for the FBCM and FDPOL is mainly discussed in this chapter. The FBCM is primarily a solar based Lithium Ion battery charger with a very wide input and output range. A synchronous buck boost topology is selected that can operate in a multi mode fashion. The FDPOL is a point load converter which is almost always a buck converter that can power low voltage applications like DSP, FPGA, transmitter and receivers etc. The FDPOL steps down the battery voltage to a regulated DC voltage for these applications.

3.2 Power stage topology for FBCM

3.2.1 Non-inverting Buck Boost Converter

While both synchronous buck and boost topologies are used in high efficiency applications but little attention has been given to integrating the two topologies together for wide input applications. For a wide input application, usually a single ended primary inductance converter (SEPIC) is used but the trend in most applications is to use the topologies that incorporate less number of external components and move closer to cost effective designs. Because SEPIC converters uses two inductors and two capacitors to transform energy from the source to the load, the single inductor, non inverting buck-boost converter, irrespective of its complexity is clearly most suitable for a cost effective, less

space consuming, low power application [10]. Figure 11 shows the non inverting buck-boost topology used in the FBCM.

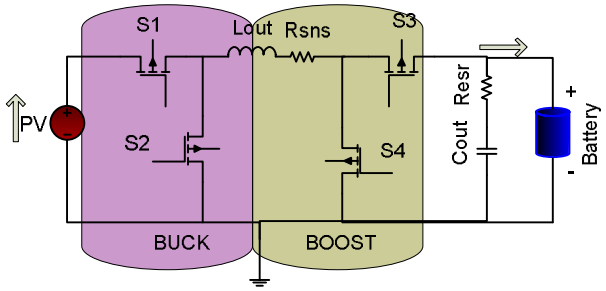


Figure 11 Buck boost topology for FBCM

3.2.2 Principle of Operation- Buck Mode

The non inverting buck-boost converter is capable of converting the source supply voltage to higher and lower voltages to the load terminal with voltage polarity unchanged. Four high speed MOSFETS (S1-S4) are employed to control the energy flow from the supply to the load terminal.

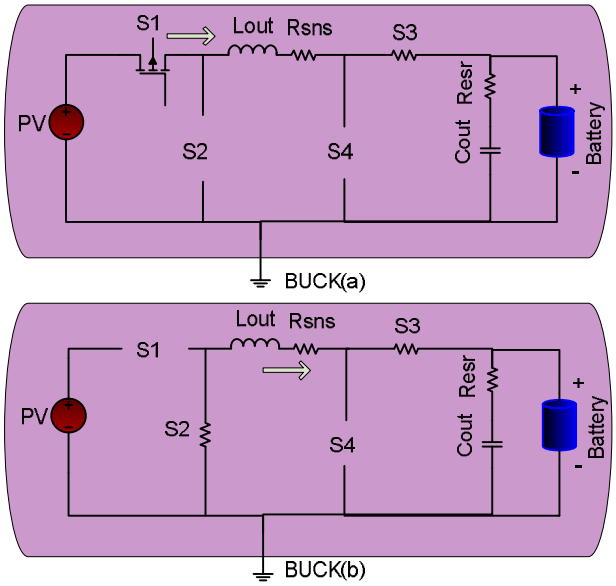


Figure 12 Buck Inductor charge and (b) Inductor discharge

Due to the variations of the supply voltage, the power converter is able to operate in buck, and boost mode. When the supply voltage is higher than the desired load voltage, the converter is set up for buck operation. In buck operation mode, the MOSFET S3 is always on and S4 is always off. The simplified equivalent circuit of the power converter for the inductor charge and discharge in buck operation is shown in Figure 12.In Figure 12(a) the MOSFET S1 is closed while S2 remains open, thus the supply voltage charges the inductor. In the inductor charging cycle, the inductor current will increase nearly linearly and the capacitor will supply output current to the load. In Figure (b), we close the MOSFET S2, and open the MOSFET S1 to engage the inductor discharge mode. In this mode, the energy stored in the inductor will be delivered to the capacitor (charging the capacitor) and the load. The current from the inductor will decrease linearly during the inductor discharge period. In the mode, the average load voltage V_0 is equal to DV_{in}, where D is the duty cycle.

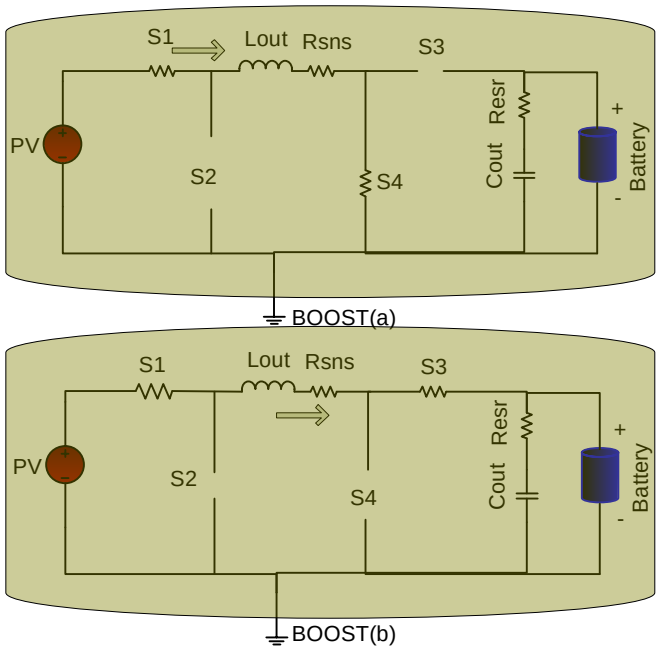


Figure 13 (a) Boost Inductor charge and (b) Inductor discharge

3.2.3 Principle of Operation- Boost Mode

When the supply voltage is lower than the desired load voltage, the converter is set up for boost operation. In the boost mode operation, the MOSFET S1 is always on and S2 is always off. The simplified circuits of the power converter inductor charge and discharge in boost operation is shown in Figure 13. In Figure 13(a) the MOSFET S4 is closed while S3 is open, thus the supply voltage charges the inductor. In Figure 13(b), we close the MOSFET S3, and open the MOSFET S3 to engage the inductor discharge mode [11]. In this mode, the average load voltage V_0 is equal to V_{in} / (1-D), where D is the duty cycle.

Even though the non inverting buck boost topology is set to work at a wide range of input and output voltages. But in this work the buck boost operation of the converter is not considered just for simplicity sake. Thus the FBCM is usually not operated at an input voltage level that is closed to the out put voltage during which the power converter topology is optimized to perform at its best.

3.3 Power stage topology for FDPOL Module

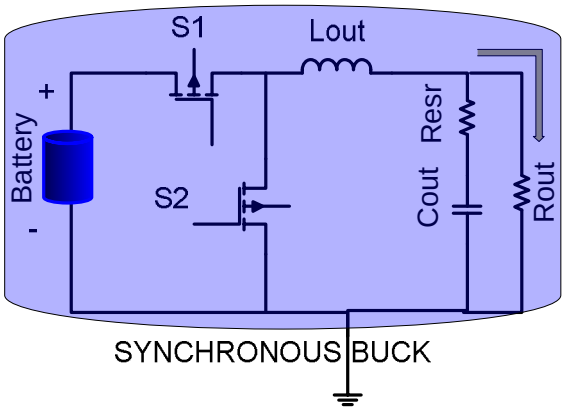


Figure 14 Synchronous buck stage used for FDPOL modules

The FDPOL shown in Figure 14 module consists of synchronous buck stage DC/DC converter which builds the regulated bus for providing point of load supply voltage for the powering the satellite subsystems. Typically the small satellite voltage bus will need low voltage DC regulated bus voltages like 12V, 5V, 3.3V, 1.8V which is stepped down from the battery power supply. According to the regulated bus voltage requirements the battery voltage is chosen in such a way that the battery voltage is always greater than the regulated bus voltage such that a synchronous buck topology can be used. The synchronous buck topology is very efficient and compact. The FDPOL modules are plug and play type of cards which can be attached in parallel if a higher current requirement is there.

The operating principle of a synchronous buck module is already discussed in the 3.2.2. The small signal dynamic characteristics of the FBCM and FDPOL will be discussed in the next chapter.

3.4 Modeling FBCM & FDPOL Buck converters

3.4.1 Average AC Modeling- Continuous Conduction Mode (CCM)

Figure 15 shows the linear equivalent circuit models for different states of a synchronous buck converter. Figure 15(a) shows the state 1 during which the voltage source charges the inductor. In Figure 15(b) the discharging of the inductor is shown. For the DFBCM case, the load is a battery instead of a resistive load. The current in the resistive load is always linear but not in the case of the battery. We showed in chapter 4 that the charge current and the charge resistance is a non linear quantity and it is described by the Butler-

volmer Equation. But for the sake of modeling the battery load is considered to be linear for a very small duration of time. After considering the linear state equations, they are averaged by using duty cycle of the switch as a weighing factor. Then the dynamic quantities are perturbed and the DC terms are separated and the first order AC terms are considered and the non-linear AC terms are eliminated.

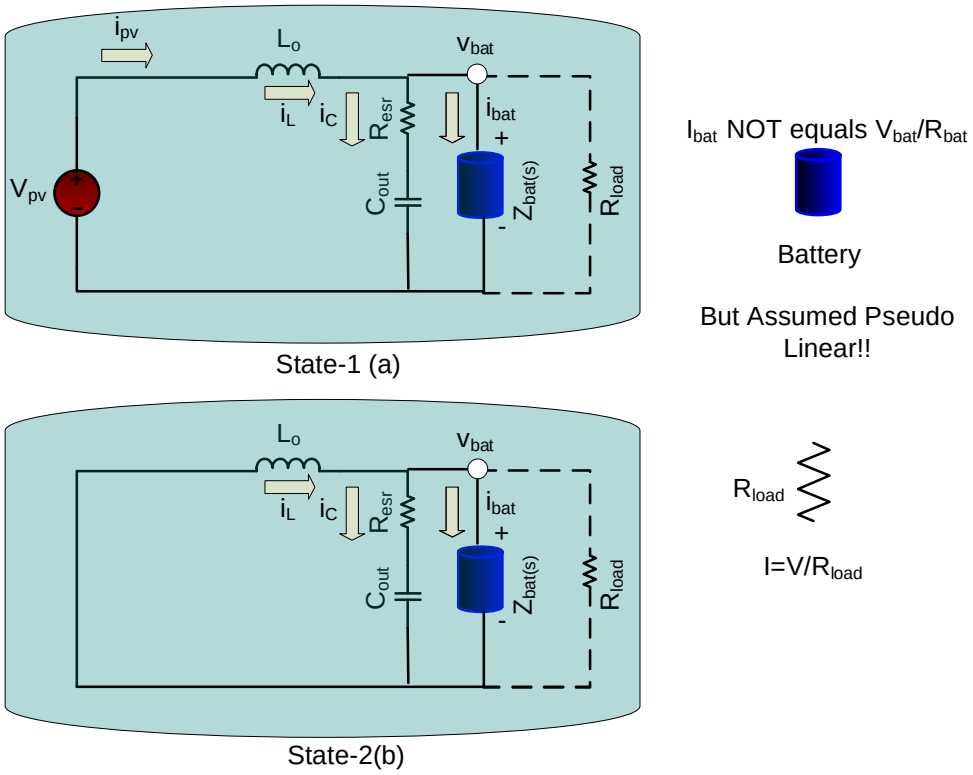


Figure 15 Linear equivalent circuit for each state of the converter in CCM

From the averaged and linearized AC terms from the averaged state equations that we get the control transfer functions for the dynamic current and the voltages.

3.4.2 Open loop transfer functions

3.4.2.1 Open loop transfer functions- Continuous Conduction Mode (CCM)

The open-loop control to output transfer function is given in eq. (3.1):

$$G_{vd} = \frac{\hat{V}_0}{\hat{d}} = V_{in} R_{load} \frac{(1+\frac{s}{w_{z1}})}{l_2 s^2 + l_1 s + l_0} \qquad (3.1)$$

The G_{vd} transfer function is for the case of FDPOL and not for FBCM. In the case of FBCM the $R_{load}=Z_{bat(s)}$.

The open-loop control to charge current transfer function (FBCM Constant Current Mode) is given in eq. (3.2)

$$G_{iLd(s)} = \frac{\hat{i}_L}{\hat{d}} = V_{pv} \frac{(1+\frac{s}{w_{z2}})}{l_2 s^2 + l_1 s + l_0} \qquad (3.2)$$

The open-loop control to input current transfer function is given in eq. (3.3):

$$G_{ipvd(s)} = \frac{\hat{i}_{pv}}{\hat{d}} = \frac{(a_2 s^2 + a_1 s + a_0)}{l_2 s^2 + l_1 s + l_0} \qquad (3.3)$$

In which,

$$w_{z1} = \frac{1}{C_{out} R_{esr}} \qquad (3.4)$$

$$w_{z2} = \frac{1}{C_{out}(R_{esr} + Z_{bat}(s))} \qquad (3.5)$$

$$l_2 = C_{out} L_{out} Z_{bat}(s) + C_{out} L_{out} R_{esr} \qquad (3.6)$$

$$l_1 = C_{out} Z_{bat}(s) R_{esr} + L_{out} \qquad (3.7)$$

$$l_0 = Z_{bat}(s) \qquad (3.8)$$

$$a_2 = C_{out} L_{out} Z_{bat}(s) I_L + C_{out} L_{out} R_{esr} I_L \qquad (3.9)$$

$$a_1 = C_{out} D Z_{bat}(s) V_{pv} + C_{out} D R_{esr} V_{pv} + C_{out} R_{esr} Z_{bat}(s) I_L + I_L L_{out} \qquad (3.10)$$

$$a_0 = Z_{bat}(s) I_L + D V_{pv} \qquad (3.11)$$

$$Z_{bat}(s) = \frac{R_L L s}{R_L + L s} + R_{ohm} + \frac{R_1}{1 + R_1 C_1 s} + \frac{R_{ct}}{1 + R_{ct} Y_2 s^{n2}} \qquad (3.12)$$

Where,

$Z_{bat}(s)$ = The AC impedance of the battery

R_L = the parallel resistance to the inductance in the battery

R_{ohm} = Ohmic resistance of the battery

R_1 = the parallel resistance to C1

C_1= Capacitance of the constant phase element Q1

R_{ct} = Charge transfer resistance

Y_2 = Admittance of the constant phase element Q2

n_2 = power of the admittance of the constant phase element Q2

The equivalent circuit diagram of the battery is shown in figure 4.6.

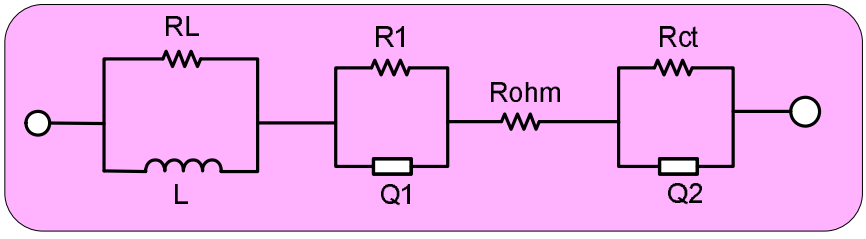


Figure 16 Equivalent circuit diagram of the battery

3.4.2.2 Battery Impedance Plots

Figure 17 shows the battery impedance gain and phase plots at very low frequencies and at medium frequencies. All the impedance curves shows that there is a low frequency pole and a zero which explains the dip in the phase plot but the gain plot remains low after the pole. There is a zero at zero frequency cause by the inductance but it comes into effect only at very high frequencies. And thus it can be ignored. The important fact about the zeros and poles in the battery impedance curve is that this impedance is coming in parallel with the output capacitor and with the R_{esr} of the capacitor. Thus the battery impedance curves behaves differently.

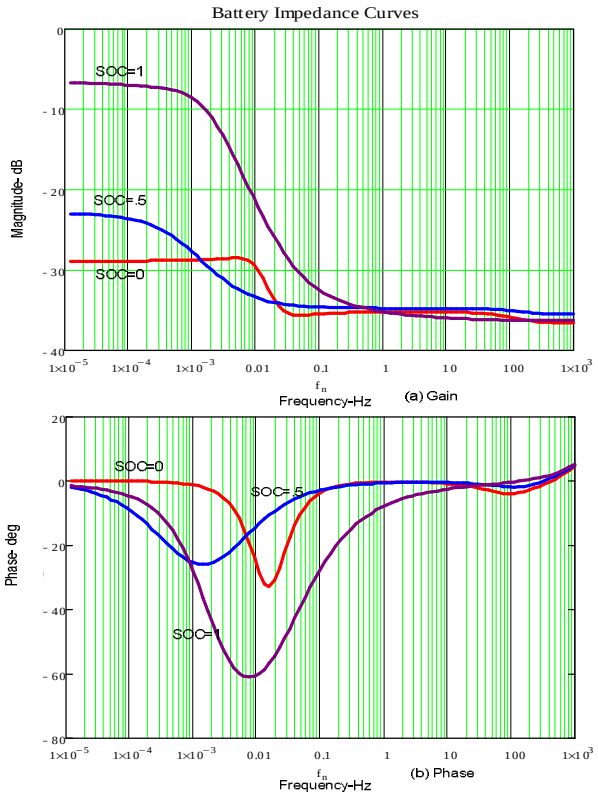


Figure 17 Battery Impedance (a) Gain and (b) phase plots at SOC=1, SOC=.5, SOC=0

3.4.2.3 Control-to-Output Voltage Transfer Function for FDPOL

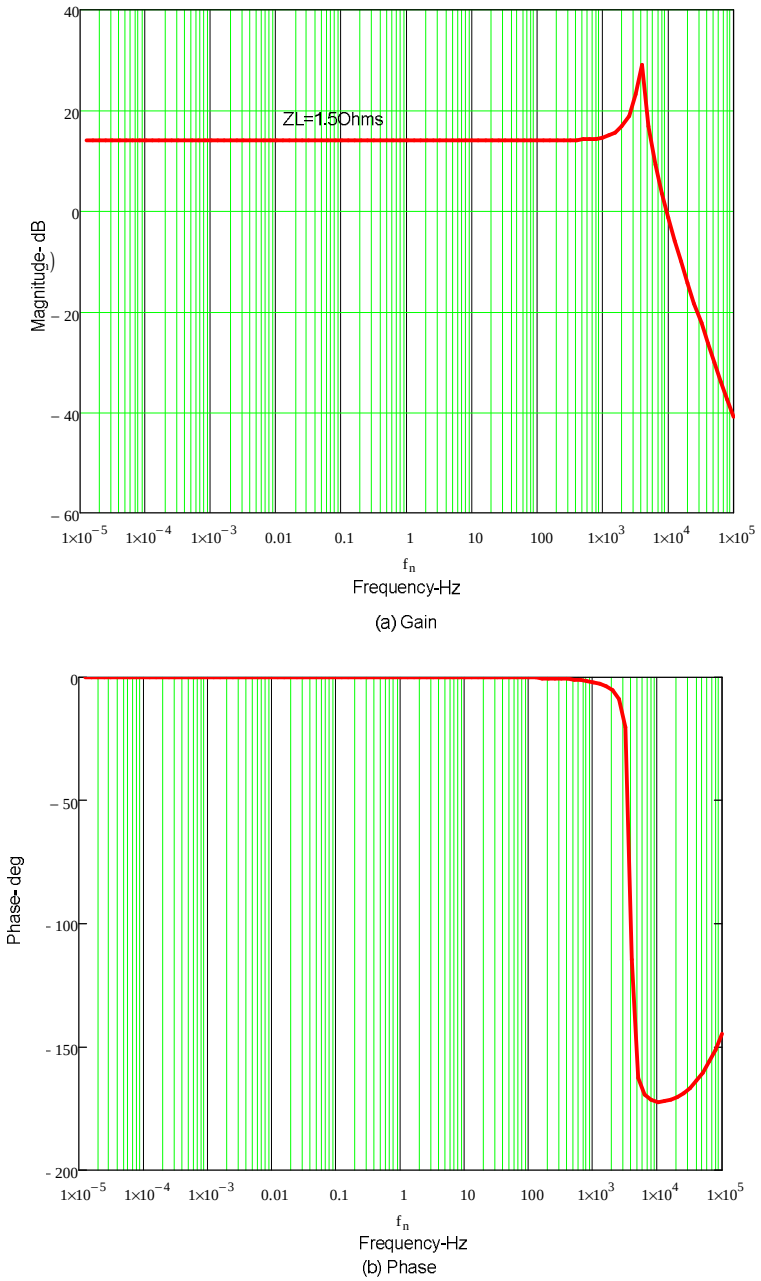


Figure 18 Control-to-Output Voltage Transfer Function (a) Gain and (b) phase plots

3.4.2.4 Control-to- Charge Current Transfer Function – Constant current mode

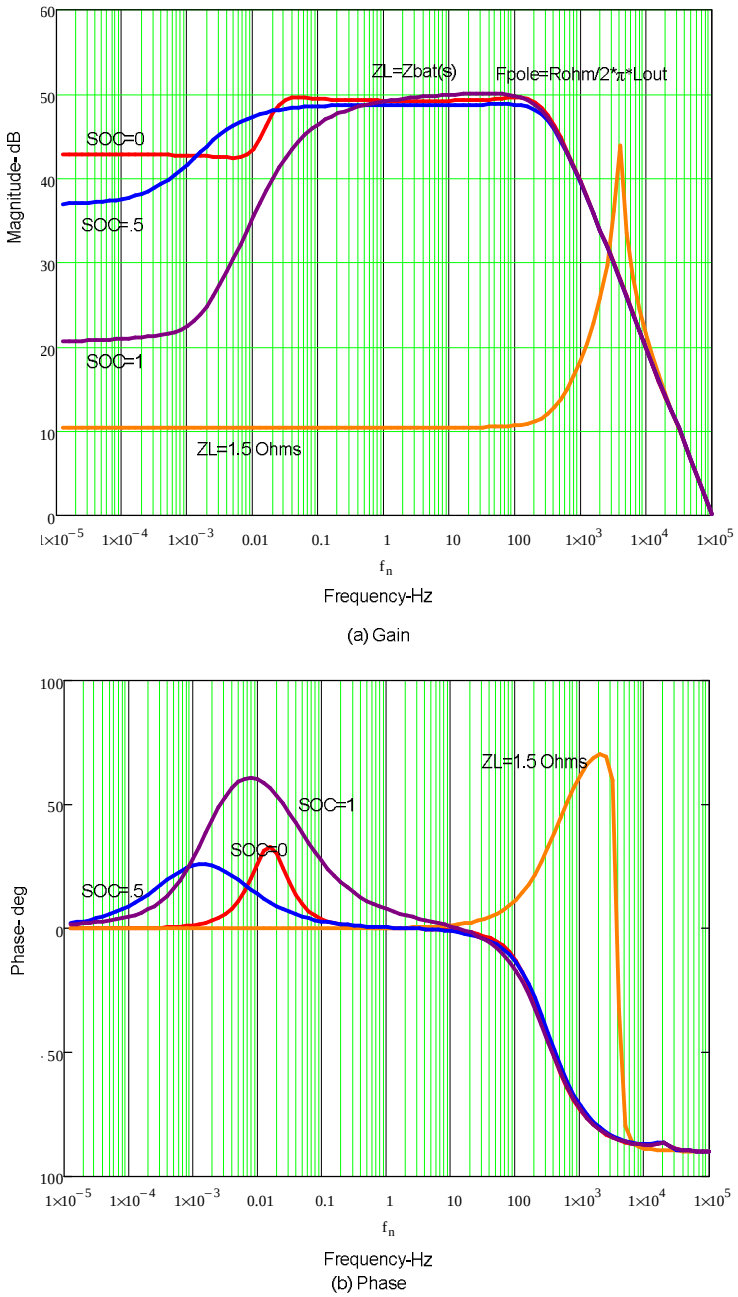


Figure 19 Control-to- Charge Current Transfer Function (a) Gain and (b) phase plots at SOC=1, SOC=.5, SOC=0 and ZL=1.5Ohms

3.4.2.5 Control-to-Input Current Transfer Function

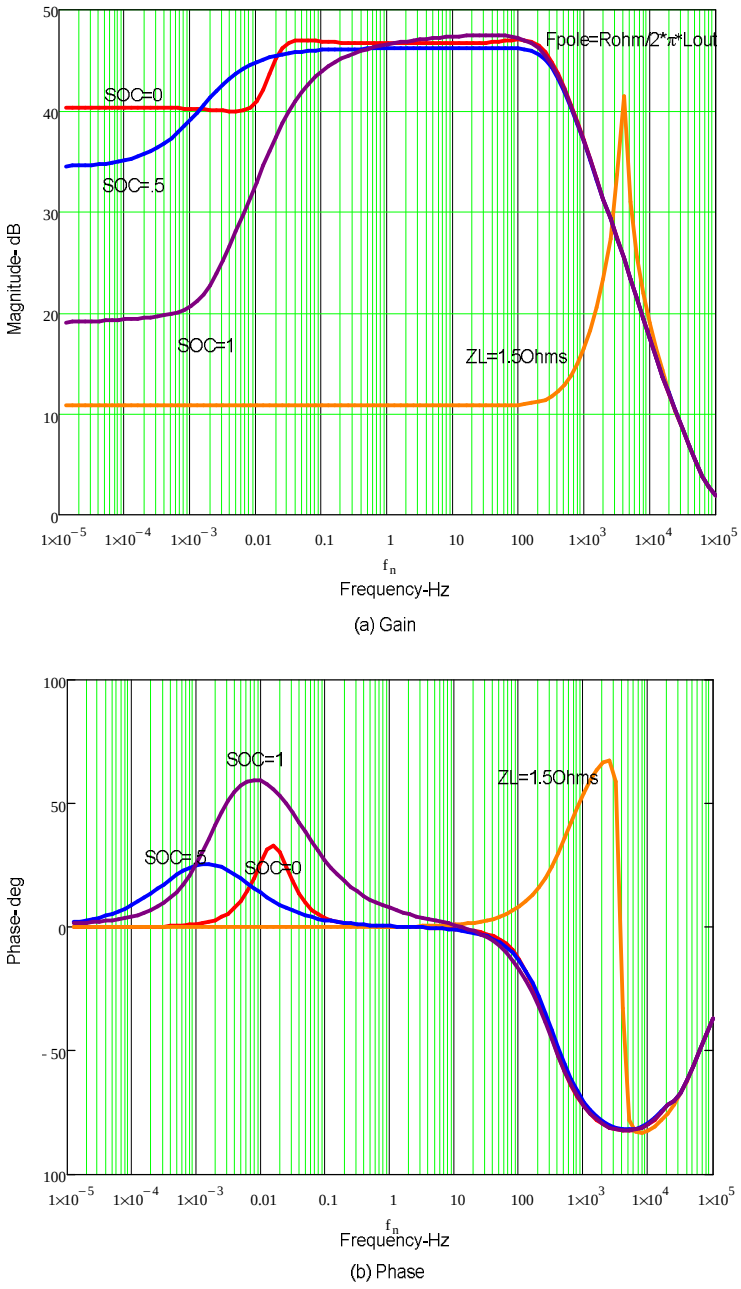


Figure 20 Control-to- Charge Current Transfer Function (a) Gain and (b) phase plots at SOC=1, SOC=.5, SOC=0 and ZL=1.5Ohms

3.4.2.6 Open Loop transfer function Discontinuous Conduction Mode (DCM)

The open loop transfer function for the discontinuous conduction mode derived using small signal AC model, getting a linearized model of the converter during the discontinuous mode of operation is beyond the scope of this work and hence only the converter transfer function is assumed [12]. The transfer function for the control to output is what we are interested in because the inductor current becomes discontinuous during the constant voltage mode. During the constant voltage mode, the battery is like a huge capacitor whose impedance is increase with time. So the current drawn from the power voltage source tends to zero from the full charging current. The control to output transfer function $G_{vd}(s)$ is given in eq. (3.13) and shown in Figure 21:

$$G_{vd}(s) = \frac{\hat{v}_o}{\hat{d}} = \frac{G_{d0}}{1 + \frac{s}{w_p}} \qquad (3.13)$$

Where

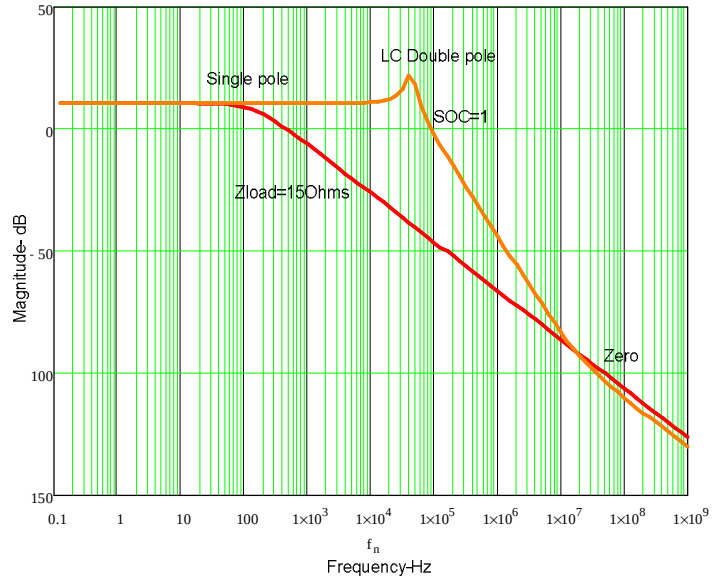
$$G_{d0} = \frac{2V_{in}}{D}\frac{1-M}{2-M} \qquad (3.14)$$

$$w_p = \frac{2-M}{(1-M)R_{bat}(s)C_{out}} \qquad (3.15)$$

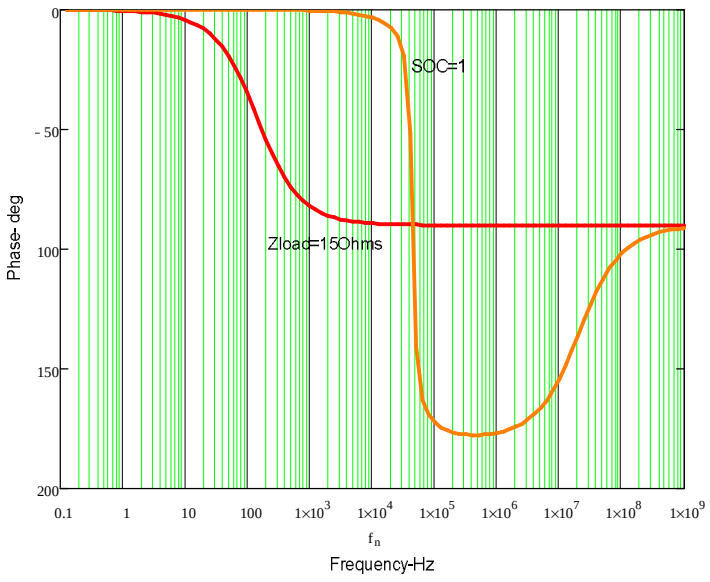
$$K = \frac{2L_{out}F_s}{\frac{V_{out}}{I_{out}}} \qquad (3.16)$$

$$M = \frac{2}{1+\sqrt{1+\frac{4K}{D^2}}} \qquad (3.17)$$

Where M is the duty cycle during discontinuous conduction mode and K determines if the converter will enter DCM mode or not.



(a) Gain



(b) Phase

Figure 21 Control-to-Output Voltage Transfer Function DCM (a) Gain and (b) phase plots

3.4.2.7 Discussion of open loop transfer functions

All the possible open loop transfer functions were discussed in the above sections. Figure 18 shows the control to output voltage transfer function of a voltage mode converter operating in CCM mode. The transfer function is analyzed with a normal resistive load and it is seen with a double pole that tapers the gain down. In Figure 19 the control to charge transfer function is analyzed for a resistive load and as well as battery load for different SOCs. We see that there is no double pole like that of a resistive load. Instead it has a single pole that is cause due to the battery parallel with the output capacitor [13]. The pole frequency is given in eq. (3.18):

$$w_p = \frac{R_{ohm}}{L_{out}} \qquad (3.18)$$

The control to charge current transfer function is used in the constant current mode. Figure 20 shows the control to input control transfer function which is analyzed since it is used during the maximum power point tracking mode. The transfer function has a single pole and the gain roles off at a 20dB per decade.

Figure 21 shows the control to output voltage transfer function during the DCM mode which is considered during the voltage mode when the battery is fully charged. As show the open loop transfer function has a double pole which is due to the stray inductance of the battery that is combining with the capacitor to form a double pole. The double pole frequency is given in eq. (3.19):

$$w_p = \frac{1}{\sqrt{(1-M)C_{out}L_{bat}}} \qquad (3.19)$$

If the L_{bat} is negligible then there is a single pole of frequency given in eq. (3.20):

$$w_p = \frac{1}{(1-M)C_{out}R_{ohm}} \qquad (3.20)$$

3.4.3 Compensation & Closed Loop Transfer Functions

For compensation even though we use digital compensation, we will consider the analog equivalent of it in this section. In the next chapter the conversion of the analog compensator to digital compensator is discussed. Since we are using a digital compensator the compensator is formed as a PID controller. The PID controller can either be complex or real. The complex PID is in the form given in eq. (3.21) [16]:

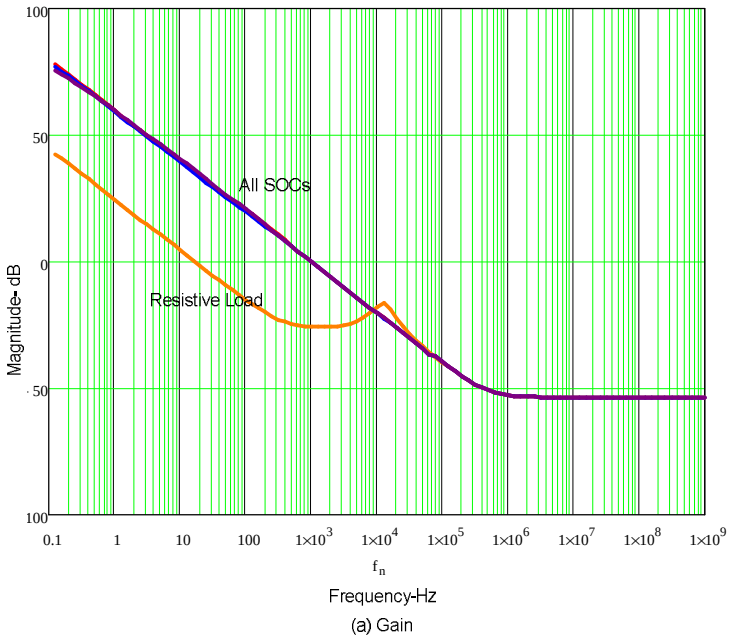
$$G_c = \frac{w_k}{s}\left(\frac{s^2}{w_z^{\,2}} + \frac{s}{Q_c w_z} + 1\right) \qquad (3.21)$$

The real PID is in the form given in eq. (3.22):

$$G_{cr} = \frac{w_k}{s}(s + w_{z1})(s + w_{z2}) \qquad (3.22)$$

Where w_z, Q_c, w_{z1}, w_{z2} are the complex zeros, the desired Q of the complex zeros and the real zeros respectively.

For the charge current and the input current transfer functions a real compensator is used the real zeros are places at the poles present in the transfer functions. For the voltage mode DCM transfer function we will be using a complex compensator since there is a LC double pole which is a result of the battery inductance and the output capacitor. All the loops are set to a bandwidth of 1 kHz. Figure 22-24 shows the closed loop gains for the charge current, input current and output voltage control loops.



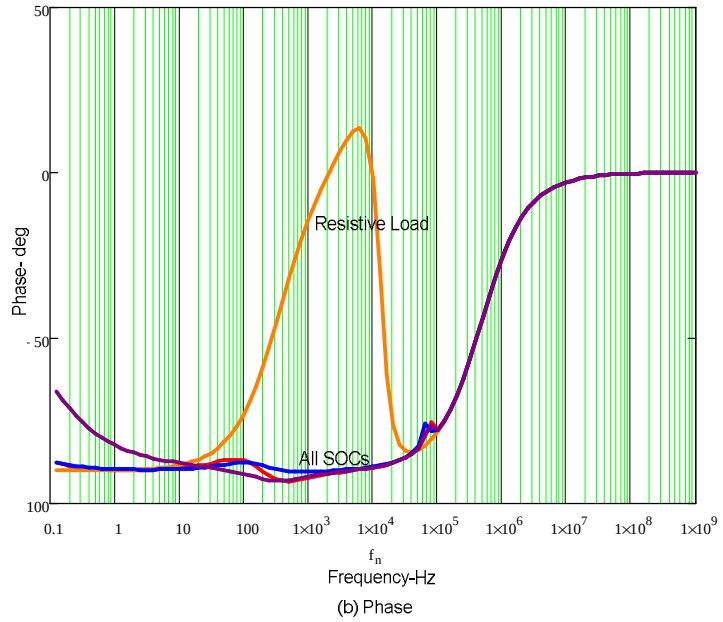
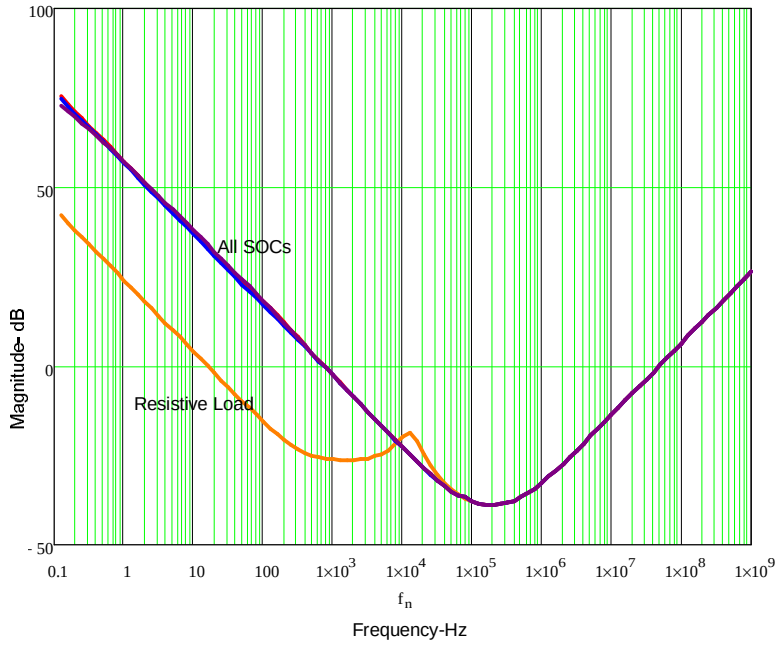
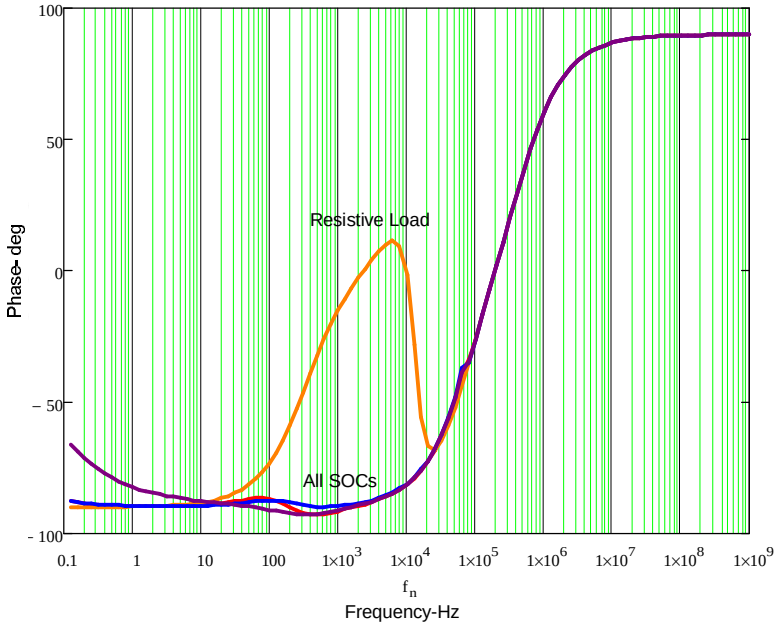


Figure 22 Charge Current Loop (a) Gain and (b) phase for All SOCs and resistive load



(a) Gain



(b) Phase

Figure 23 Input Current Loop (a) Gain and (b) phase for All SOCs and resistive load

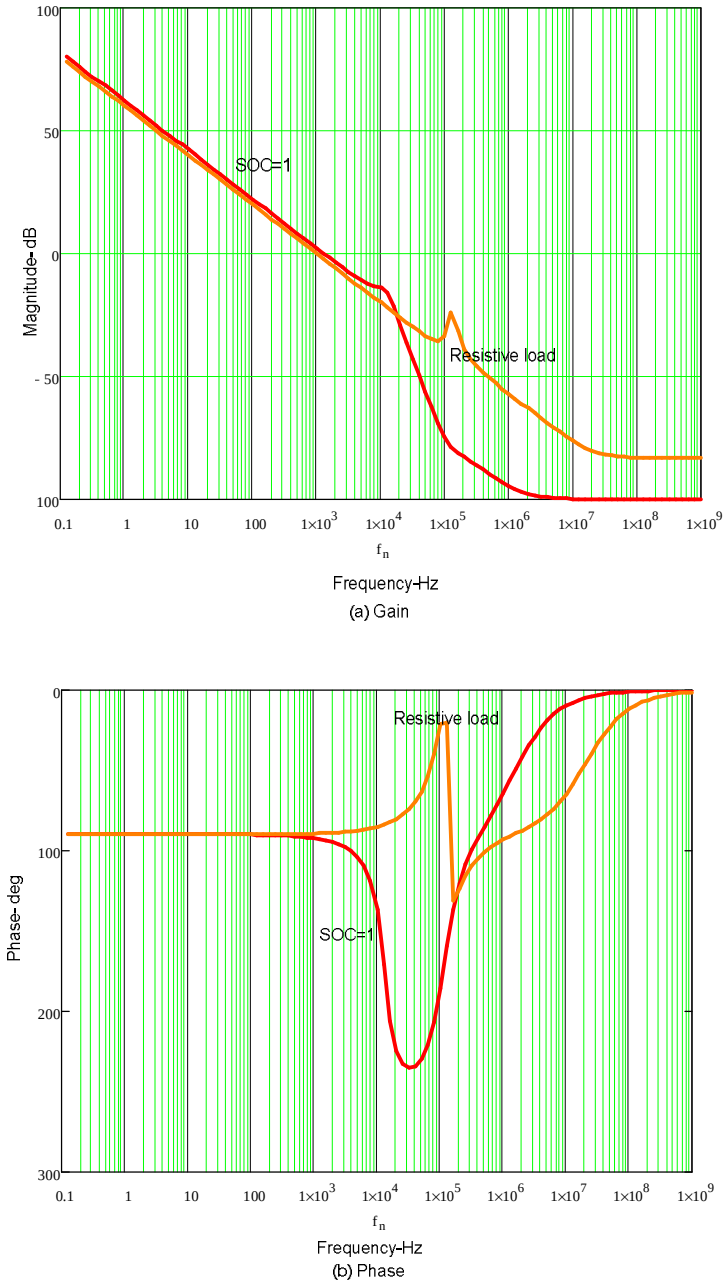


Figure 24 Output Voltage Loop (a) Gain and (b) phase for SOC=1 and resistive load

3.5 Modeling of FBCM Boost converter

3.5.1 Average AC Modeling- Continuous Conduction Mode (CCM)

Figure 25 shows the linear equivalent circuit models for different states of a synchronous boost converter. Figure 25 (a) shows the state 1 during which the voltage source charges the inductor. In Figure 25 (b) the discharging of the inductor is shown. For the DFBCM case, the load is a battery instead of a resistive load. The current in the resistive load is always linear but not in the case of the battery. It is shown in chapter 4 that the charge current and the charge resistance is a non linear quantity and it is described by the Butler-volmer Equation. But for the purpose of modeling, the battery load is considered to be linear for a very small duration of time. After considering the linear state equations, they are averaged by using duty cycle of the switch as a weighing factor. Then the dynamic quantities are perturbed and the DC terms are separated and the first order AC terms are considered and the non-linear AC terms are eliminated.

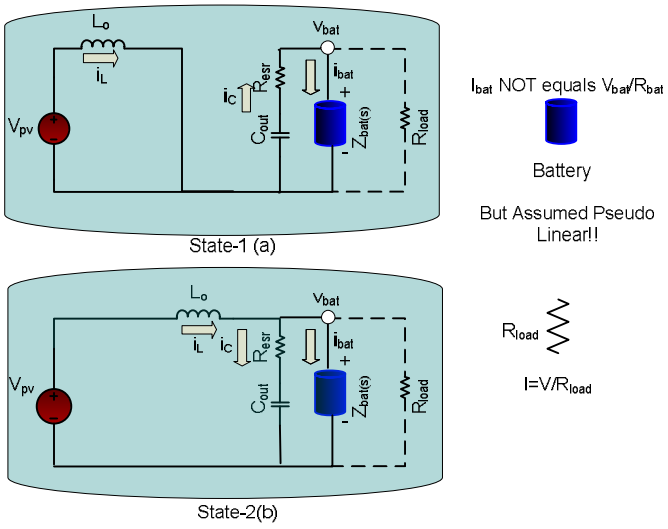


Figure 25 Linear equivalent circuit for each state of the boost converter in CCM

From the averaged and linearized AC terms from the averaged state equations that we get the control transfer functions for the dynamic current and the voltages.

3.5.2 Open loop transfer functions

3.5.2.1 Open loop transfer functions- Continuous Conduction Mode (CCM)

The boost converter operates in CCM only during the constant current charging state. The input current to control transfer function is same as the inductor current to control transfer function. During the constant voltage mode the inductor current is almost discontinuous.

The open-loop control to charge current transfer function [18] (FBCM Constant Current Mode) shown in Figure 27 and is given in eq. (3.23):

$$G_{iLd(s)} = \frac{\hat{i}_L}{\hat{d}} = \frac{G_{d0}(1+\frac{s}{w_{z1}})}{1+\frac{s}{w_p}+\frac{s^2}{w^2{}_0}} \qquad (3.23)$$

In which,

$$G_{d0} = \frac{2V_0}{R_{bat}D^{'2}} \qquad (3.24)$$

$$w_{z1} = \frac{1}{C_{out}R_{bat}} \qquad (3.25)$$

$$w_p = \frac{D^{'2}R_{ohm}}{L_{inp}} \qquad (3.26)$$

$$w_o = \frac{D^{'}}{\sqrt{L_{inp}C_{out}}} \qquad (3.27)$$

$$R_{bat}(s) = \frac{R_L Ls}{R_L + Ls} + R_{ohm} + \frac{R_1}{1 + R_1 C_1 s} + \frac{R_{ct}}{1 + R_{ct} Y_2 s^{n2}} \qquad (3.28)$$

Where,

$Z_{bat}(s)$ = The AC impedance of the battery

R_L = the parallel resistance to the inductance in the battery

R_{ohm} = Ohmic resistance of the battery

R_1 = the parallel resistance to C1

C_1= Capacitance of the constant phase element Q1

R_{ct} = Charge transfer resistance

Y_2 = Admittance of the constant phase element Q2

n_2 = power of the admittance of the constant phase element Q2

The equivalent circuit diagram of the battery is shown in figure 4.6.

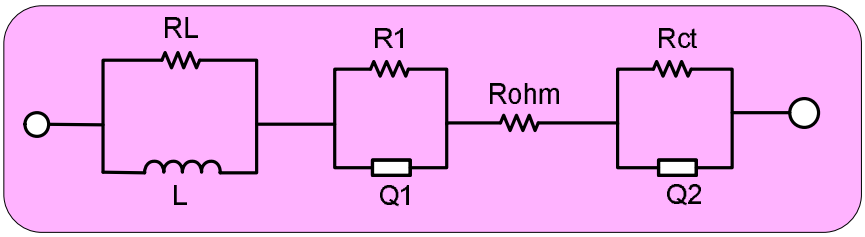


Figure 26 Equivalent circuit diagram of the battery

Control-to- Charge Current Transfer Function –Constant current mode

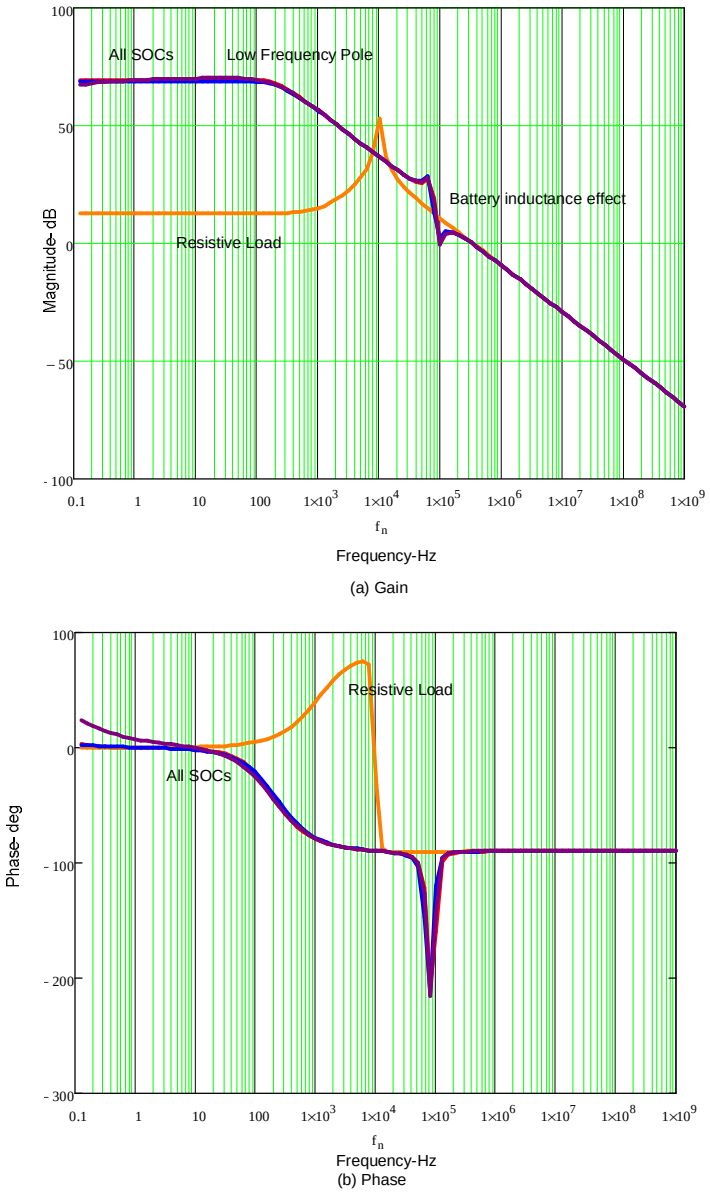


Figure 27 Control-to- Charge Current Transfer Function (a) Gain and (b) phase plots at all SOCs and ZL=15Ohms

3.5.2.3 Open Loop transfer function Discontinuous Conduction Mode (DCM)

The open loop transfer function for the discontinuous conduction mode derived using small signal AC model, getting a linearized model of the converter during the discontinuous mode of operation is beyond the scope of this work and hence only the converter transfer function is assumed [12]. The transfer function for the control to output is what we are interested in because the inductor current becomes discontinuous during the constant voltage mode. During the constant voltage mode, the battery is like a huge capacitor whose impedance is increase with time. So the current drawn from the power voltage source tends to zero from the full charging current.

The control to output transfer function $G_{vd}(s)$ is given in and shown in Figure 28:

$$G_{vd}(s) = \frac{\hat{v}_o}{\hat{d}} = \frac{G_{d0}}{1 + \frac{s}{w_p}} \qquad (3.29)$$

Where

$$G_{d0} = \frac{2V_{in}}{D}\frac{M-1}{2M-1} \qquad (3.30)$$

$$w_p = \frac{2M-1}{(M-1)R_{bat}(s)C_{out}} \qquad (3.31)$$

$$K = \frac{2L_{out}F_s}{\frac{V_{out}}{I_{out}}} \qquad (3.32)$$

$$M = \frac{1+\sqrt{1+\frac{4D^2}{K}}}{2} \qquad (3.33)$$

Where M is the duty cycle during discontinuous conduction mode and K determines if the converter will enter DCM mode or not.

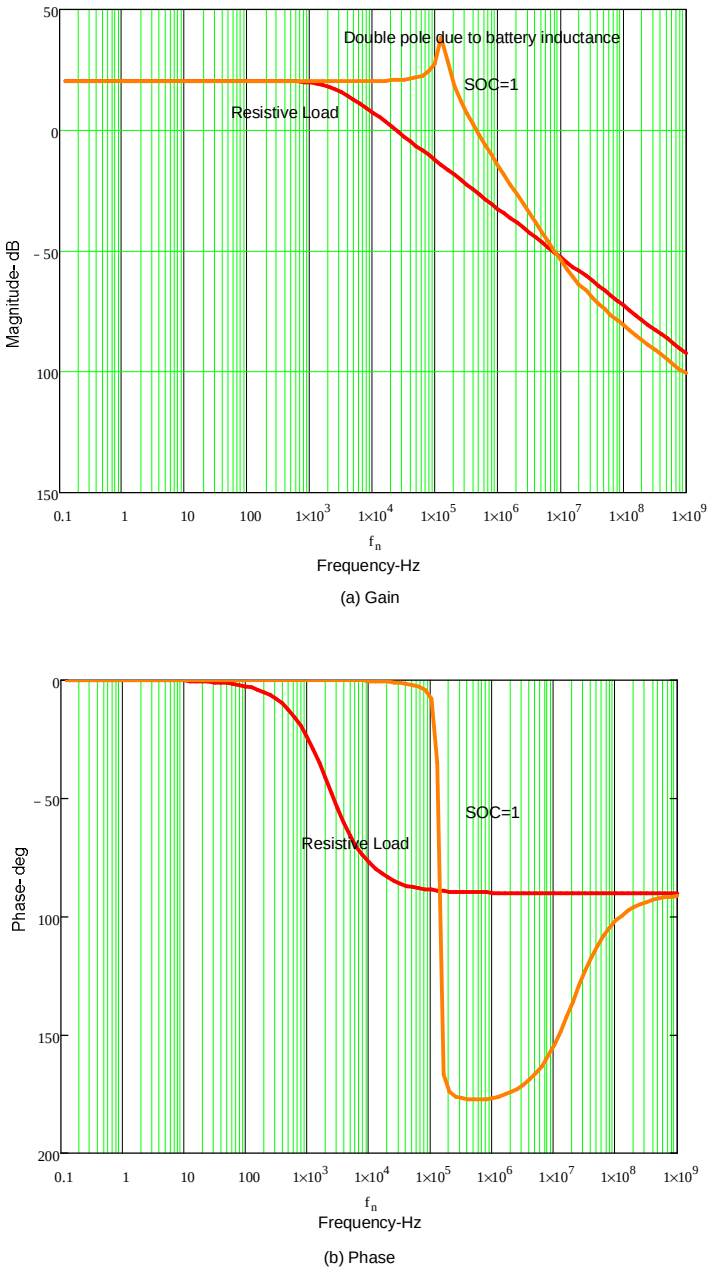


Figure 28 Control-to-Output Voltage Transfer Function DCM (a) Gain and (b) phase plots

3.5.2.4 Compensation and Closed loop gain plots

All the possible open loop transfer functions were discussed in the above sections. In Figure 27 the control to charge transfer function is analyzed for a resistive load and as well as battery load for different SOCs. We see that there is no double pole like that of a resistive load. Instead it has a single pole that is cause due to the battery parallel with the output capacitor. The gain roles off at a 20dB per decade. The single pole frequency is given by eq. (3.34):

$$w_p = \frac{R_{ohm} D^{'2}}{L_{out}} \qquad (3.34)$$

The control to charge current transfer function is used in the constant current mode. The control to input current transfer function is same as the control to charge current transfer function. The control to input current transfer function is used during the maximum power point tracking mode.

Figure 28 shows the control to output voltage transfer function during the DCM mode which is considered during the voltage mode when the battery is fully charged. As show the open loop transfer function has a double pole which is due to the stray inductance of the battery that is combining with the capacitor to form a double pole. The double pole frequency is given by eq. (3.35):

$$w_p = \frac{1}{\sqrt{(M-1) C_{out} L_{bat}}} \qquad (3.35)$$

If the L_{bat} is negligible then there is a single pole of frequency given in eq. (3.36):

$$w_p = \frac{1}{(M-1) C_{out} R_{ohm}} \qquad (3.36)$$

For compensation even though we use digital compensation, we will consider the analog equivalent of it in this section. In the next chapter the conversion of the analog compensator to digital compensator is discussed. Since we are using a digital compensator the compensator is formed as a PID controller. The PID controller can either be complex or real. The complex PID is given in eq. (3.37) of [16]:

$$G_c = \frac{w_k}{s}\left(\frac{s^2}{w_z^{\ 2}} + \frac{s}{Q_c w_z} + 1\right) \qquad (3.37)$$

The real PID is in eq. (3.38):

$$G_{cr} = \frac{w_k}{s}(s + w_{z1})(s + w_{z2}) \qquad (3.38)$$

Where w_z, Q_c, w_{z1}, w_{z2} are the complex zeros, the desired Q of the complex zeros and the real zeros respectively.

For the charge current and the input current transfer functions a real compensator is used the real zeros are places at the poles present in the transfer functions. For the voltage mode DCM transfer function we will be using a complex compensator since there is a LC double pole which is a result of the battery inductance and the output capacitor. All the loops are set to a bandwidth of 1 kHz. Figures 29-30 shows the closed loop gains for the charge current and output voltage control loops.

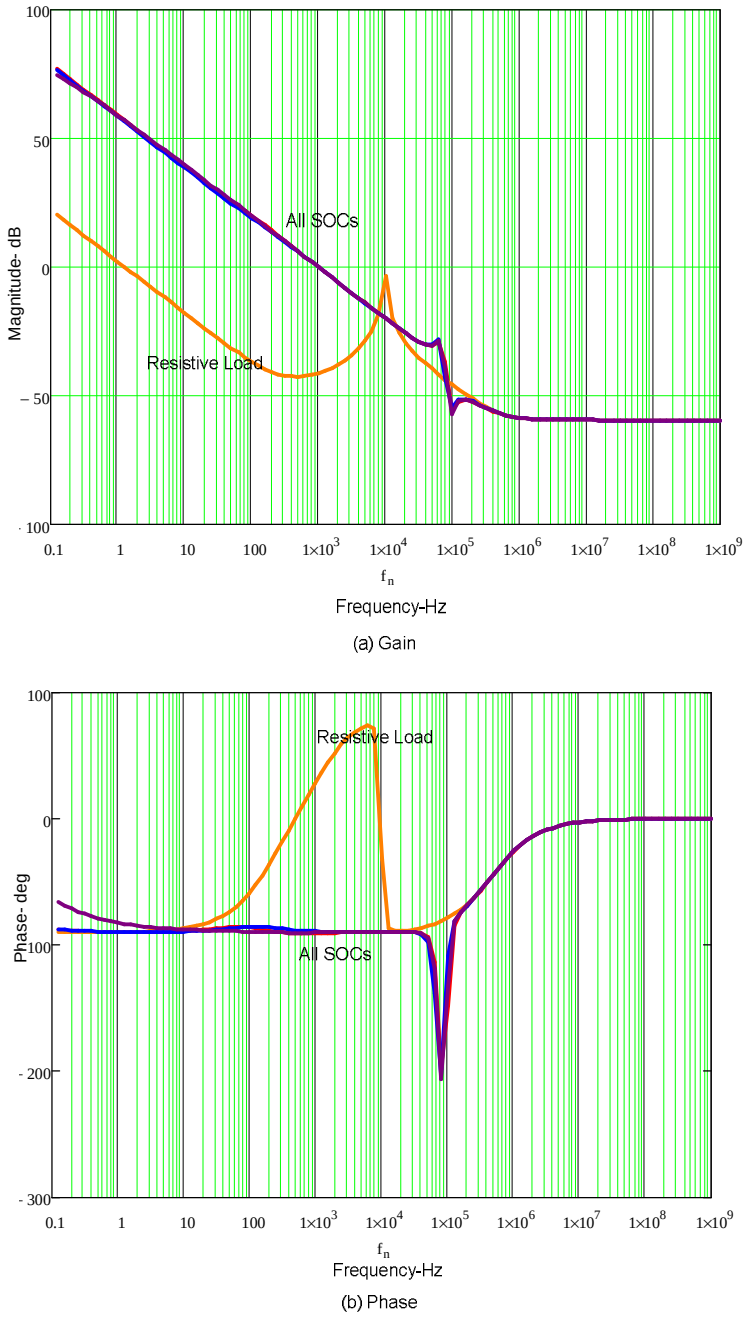
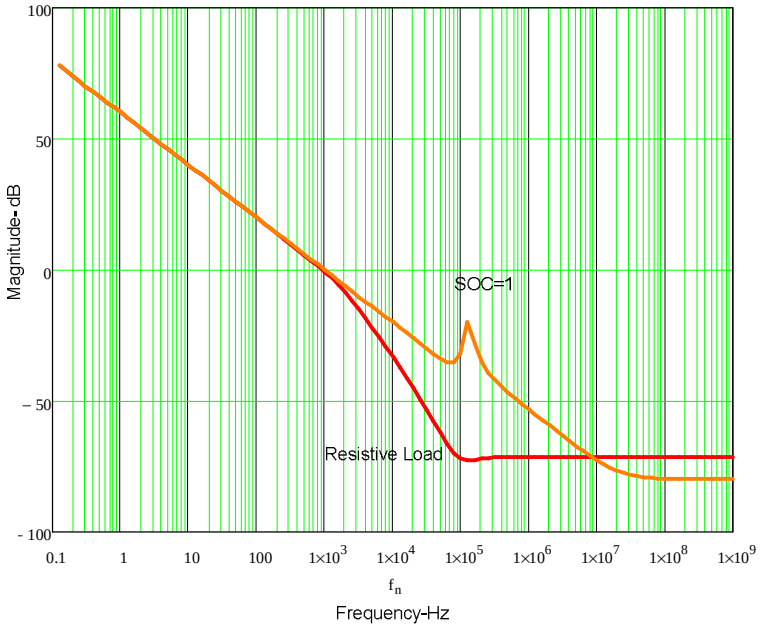
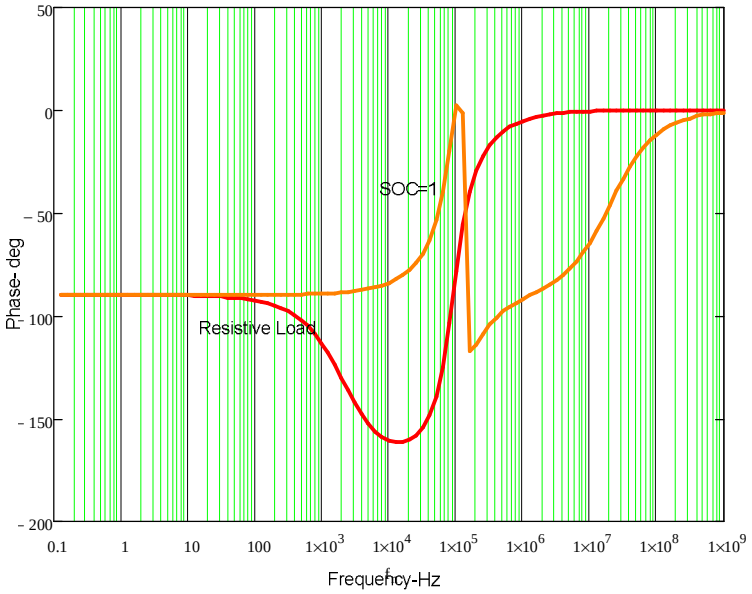


Figure 29 Charge Current Loop CCM (a) Gain and (b) phase for All SOCs and resistive load



(a) Gain



(b) Phase

Figure 30 Output Voltage Loop DCM (a) Gain and (b) phase for All SOCs and resistive load

Chapter 4

4. Energy Storage Device Modeling

4.1 Introduction

In this chapter, we characterize the energy storage device which plays a major role in the power system. For the satellite power system, Lithium Ion based batteries are highly recommended because both the volumetric and gravimetric energy densities are at least twice the value when compared to lead-acid/nickel cadmium batteries [4]. The characteristic impedance of the battery systems gives us an idea of the battery's state and it varies with cycle life, temperature, charging and discharging current. Thus a perfect characterization of the battery impedance over various operating conditions is the best option to make sure that the over all system control is under control. Electro chemical impedance spectroscopy, EIS, is a powerful way to gain information about electro chemical systems especially of those of batteries. Since most of the batteries are sealed, we do not have the option of checking the impedance of each of the electrodes and electrolytes separately, EIS gives us a way to measure the lumped impedance of the battery and use curve fitting to model the battery impedances. In the next chapter, the effect of the impedance on the control loop design is analyzed further.

4.2 Electro Chemistry of Lithium Based Batteries

In a sealed lithium based batteries, both the anode (negative plate) and cathode (positive plate) is made of intercalation materials with lattice structures into which guest

species are intercalated. The electrodes are extracted across a lithium Ion electrolyte of an aprotic solvent, without much structural modification of the host. The negative and the positive electrodes of a Li-ion cell are generally made of lithiated graphite and Lithium metal oxide respectively, and the electrolyte is a Li salt dissolved in an aprotic solvent. Figure 31 shows the general construction of a Lithium Ion battery.

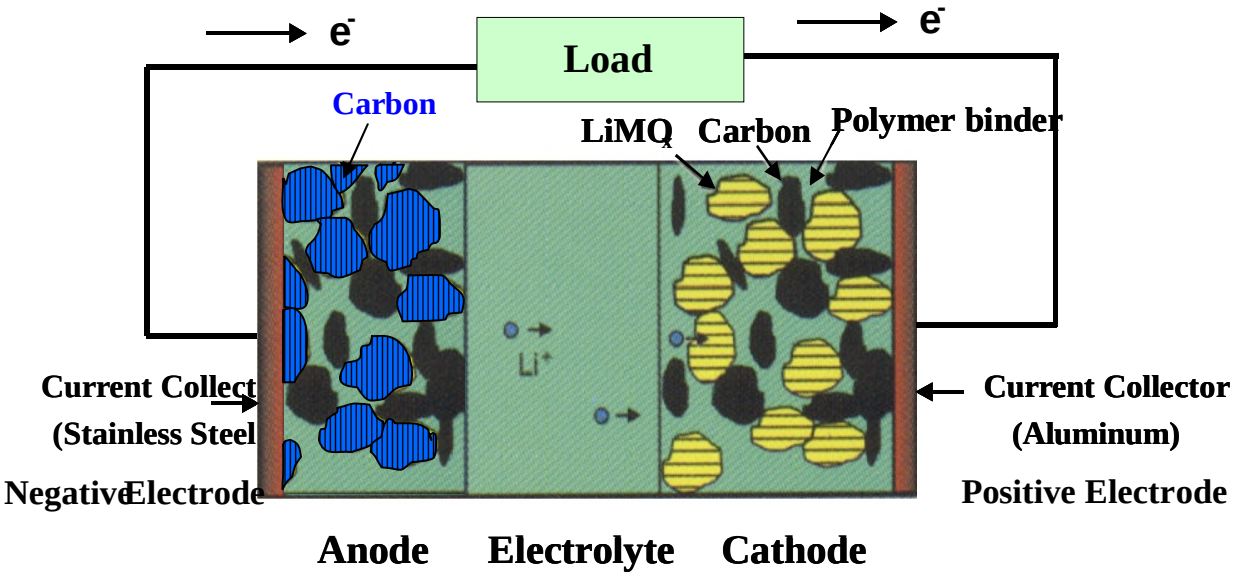


Figure 31 Active positive and negative materials in a Lithium Ion Cell

The respective electrode reactions are given in eq. (4.1) and eq. (4.2):

$$LiC \underset{charge}{\overset{discharge}{\rightleftharpoons}} Li_{1-x} + xLi^{+} + xe^{-} \quad E=-3.0V \qquad (4.1)$$

$$Li_{1-x}MO_x + xLi^{+} + xe^{-} \underset{charge}{\overset{discharge}{\rightleftharpoons}} LiMO_x \quad E=.6V \qquad (4.2)$$

The overall reaction is given by eq. (4.3)

$$LiC + Li_{1-x}MO_x \underset{charge}{\overset{discharge}{\rightleftharpoons}} Li_{1-x}C + LiMO_x \quad Ecell=3.6V \qquad (4.3)$$

The terminal voltage of the cell depends upon the concentration of the electrolyte and the electrodes [4][5]. EMF of the cells begins to drop down with current drawn from it. Figure 32 shows the discharge characteristics of a Lithium Ion Cell (ANR26650) from A123 systems. The nominal capacity and voltage of the battery is 2.3Ah, 3.3V respectively with an operating temperature of -30˚C to +60˚C. Figure 33 shows the discharge characteristics of the Lithium Ion battery that is used for the research study which varies with the discharge

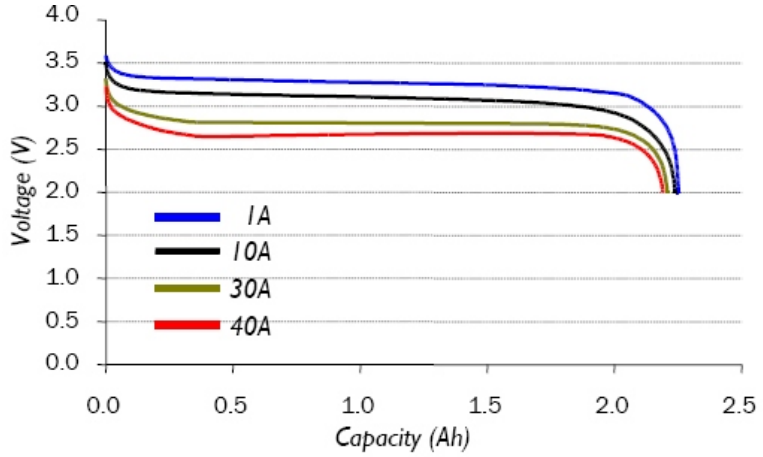


Figure 32 Discharge Characteristics of ANR26650 Li-ion battery from A123

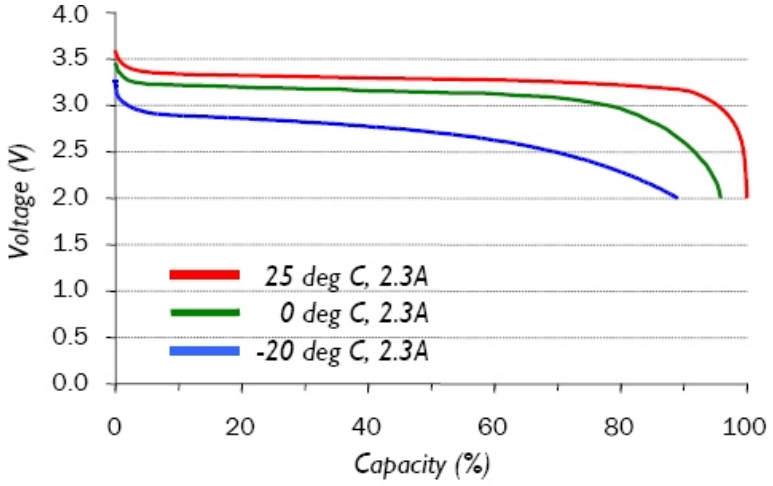


Figure 33 Low temperature discharge performance

Current. Figure 33 shows the low temperature discharge performance of the battery system. The discharge performance and the capacity are eventually affected by temperature. The battery is at its 90% capacity at -30˚C and also it is a fact that the capacity will increase when you increase the temperature beyond room temperature. The poor performance of Li-ion cell at low temperatures is due to poor kinetics which will be further substantiated by the ac impedance characteristics study.

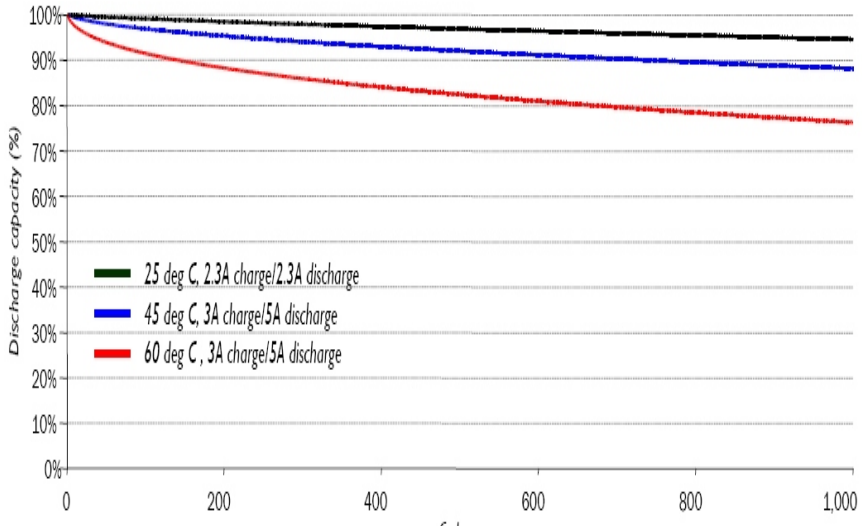


Figure 34 Cycle Life performance, 100% DOD, various temperatures

Figure 34 shows the cycle life performance and its effect on capacity shown for different operating temperatures. It is shown here that battery characteristics change with the age of the battery which is primarily the number of charge and discharge cycles. The battery capacity and hence the discharge characteristics change with number of cycles of charge and discharge the battery has gone through. The overall battery impedance changes with battery life which is further substantiated by studying the ac impedance spectrum of the battery [6].

4.3 Electrochemical Impedance Spectroscopy (EIS)

Electrochemical Impedance Spectroscopy (EIS) is an electrochemical technique with applications in corrosion, battery development, fuel cell development, paint characterization, sensor development, and physical electrochemistry. An EIS measurement technique involves the application of a sinusoidal electrochemical perturbation (potential or current) to the sample that covers a wide range of frequencies. This multi-frequency excitation allows (1) the measurement of several electrochemical reactions that take place at different rates and (2) the measurement of the capacitance of the electrode.

Electrochemical impedance is usually measured by applying an AC current through an electrochemical cell and measuring the potential across the cell. Assume that we apply a sinusoidal current excitation. The response to this current is an AC potential signal across it. This potential signal can be analyzed as a sum of sinusoidal functions (a Fourier series). Electrochemical Impedance is normally measured using a small excitation signal. This is done so that the cell's response is pseudo-linear. In a linear (or pseudo linear) system, the current response to a sinusoidal potential will be a sinusoid at the same frequency but shifted in phase as shown in Figure 35.

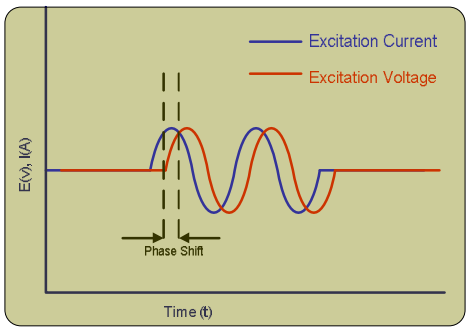


Figure 35 Sinusoidal Current Response in a Linear System

The excitation signal, expressed as a function of time, has the form $I_t = I_0 \text{ Sin } (\omega t + \varphi)$, where I_t is the current at time t, I_0 is the amplitude of the signal, and ω is the radial frequency. In a linear system, the response signal, is shifted in phase (φ) and has different amplitude, E_0 and expression $E_t = E_0 \text{ Sin } (\omega t)$. An expression analogous to Ohm's Law allows us to calculate the impedance of the system as: $Z = E_t/I_t = Z_0 (\text{Cos } \varphi + \text{Sin } \varphi)$. The impedance is therefore expressed in terms of a magnitude, Z_0 and a phase shift, φ. The complex impedance of the electrochemical cells over a wide range of AC frequencies is recorded by the EIS instrument. Typically, several cell elements and cell characteristics contribute to the system's EIS spectrum. Some of the possible elements include electrode double layer capacitance, electrode kinetics, diffusion layer, solution resistance and so on. The system's impedance at any given frequency usually depends upon more than one cell element. This greatly complicates the analysis of EIS spectra [7].

The most common method used to analyze EIS spectra is equivalent circuit modeling. We can simulate the cell using the equivalent circuit incorporating electrical components (resistors, capacitors, inductors) plus a few specialized electrochemical elements such as Warburg impedance. The key to analyzing the EIS spectra is good fitting of the data and proper assignment of the equivalent circuit model. A non-linear least square fitting program is used to fit the model to the experimental data. This program attempts to minimize the deviation between the spectrum of the model and the experimental data spectrum. The Levenberg- Marquardt algorithm and the simplex algorithm are two fitting algorithms that are used in this research study. Both of these algorithms automatically adjust the parameter values of the elements in the model to find the best fit [8].

One of the more difficult tasks in equivalent circuit modeling is determining the initial values for the model's parameters. The either optimization algorithm needs to start with values for all parameters (resistor, capacitor, inductances). If the initial values are far from the optimal values, the optimization program may be unable to find the best fit. Hence this process needs at least a rough idea of the parameter value to start with. This process is considered very tedious and expensive than the other methods for determining the equivalent circuit model and henceforth very few scientists prefer this method.

4.4 Equivalent Circuit Modeling

4.4.1. Introduction

Electro chemical and mathematical models are the two main types of models that are used for modeling batteries. Out of which electrochemical modeling methods are very accurate and highly reliable because they make use of high precision measurement techniques and also take care of the microscopic electrochemical information etc. Mathematical models are too abstract to embody any practical meaning but it is still useful to system designers. This chapter mainly focuses on electrochemical impedance based models but for the purpose of clarity the other commonly used models are also discussed here in short.

4.4.2. Thevenin and runtime based electrical models

In its most basic form, a Thevenin model, shown in Figure 36 uses a series resistor and RC parallel network to predict battery response to transient load events at a particular state of charge, by assuming the open circuit voltage is constant. Unfortunately this

assumption prevents it from capturing steady state battery voltage variations as well as runtime information. A more accurate model will be that will predict the runtime as well as transient data of the battery. This model is shown in Figure 37 in which on the left a capacitor and a current controlled current source which represents the runtime model and the RC capacitance and resistance that describes the transient behavior of the system. The transient behavior is also seen as a short time and long time effect causing elements [9].

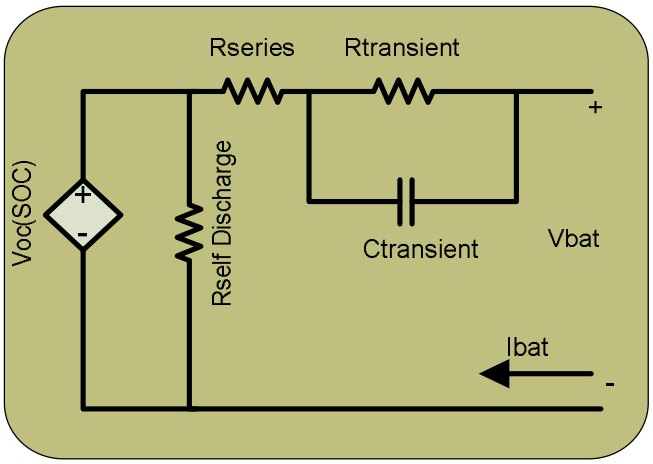


Figure 36 Thevenin based Mathematical Model

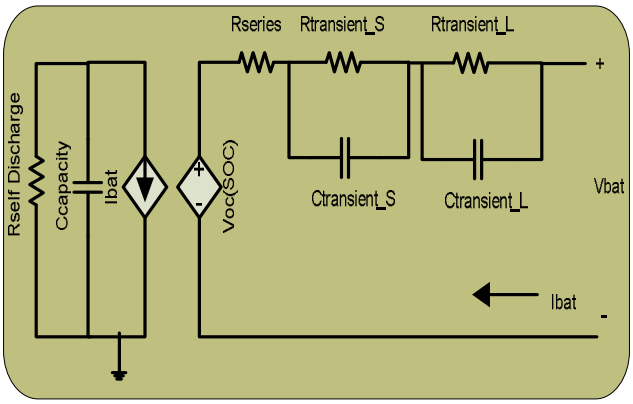


Figure 37 Run time based Model

4.4.3. Electrochemical Equivalent Circuit

The electrochemical equivalent circuit of a battery comprises the electrochemical processes occurring at the anode, the cathode and the electrolyte. Figure 38 shows the complete electrochemical equivalent circuit .The battery electrodes are usually porous and the porosity of the electrodes leads to the impedance becoming inductive at high frequency. Therefore La, Lc refers to the inductors associated with the anode and the cathode, respectively. Rohm refers to the ohmic resistance of the cell, which includes the resistance of the electrolyte, electrode base metal, electrode leads, terminals etc. The charge transfer resistance (Ra and Rc), the double layer capacitances (Ca and Cc) and the Warburg impedances (Wa and Wc) of the respective anode and cathode are included in the circuit following Randles' equivalent circuit model for energy storage devices [6].

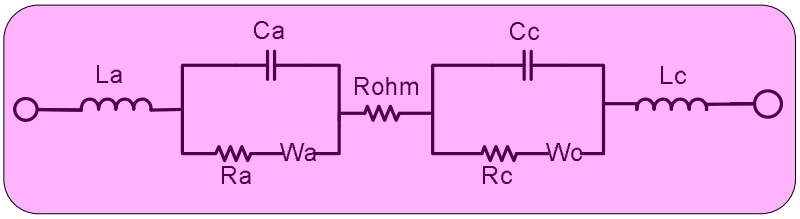


Figure 38 Electrochemical Equivalent Model

4.4.3.1. Charge Transfer Resistance (Ra and Rb)

The charge transfer resistance (Ra and Rb) of an electrochemical process is related to the exchange current. This resistance is formed where ever there is a kinetically controlled electrochemical reaction [7].

When a metal substrate in contact with an electrolyte, it can electrolytically dissolve into the electrolyte, according to eq. (4.4):

$$LiC \underset{charge}{\overset{discharge}{\rightleftharpoons}} Li_{1-x} + xLi^{+} + xe^{-} \qquad (4.4)$$

In the forward reaction, electrons enter the metal and metal ions diffuse into the electrolyte and charge is being transferred. In back ward reaction the electrons combine with the metal ions to form the metal. This charge transfer which is occurring in both ways has a certain speed and it depends on the kind of reaction, the temperature, the concentration of the reaction products and the potential.

The general relation between the potential and the current (which is directly related with the amount of electrons and so the charge transfer via faraday's law) is given by the Butler-Volmer equation given in eq. (4.5):

$$I=I_0 (\exp(\alpha n F\eta/RT) - \exp(-(1-\alpha) nF\eta/RT)) \qquad (4.5)$$

Where,

I_0=Exchange current density

η =Over potential (Eapp-Eoc)

F = Faraday's constant

T = temperature

R =gas constant

α = reaction order

n = number of electrons involved.

Thus the relationship between dc current and the charge transfer resistance (Rct) is non-linear. Thus the battery can no longer be considered as a linear load in a large signal way. The non linear charge transfer can be calculated in eq. (4.6)

$$R_{ct}(I)=\delta \eta/\delta I \qquad (4.6)$$

4.4.3.2. Warburg Impedance

The diffusion characteristics also can create impedance called Warburg impedance. The impedance depends upon the frequency of the potential perturbation [7]. At high frequencies the Warburg impedance is small since diffusing reactants don't have to move very far. At low frequencies the reactants have to diffuse farther, increasing the Warburg impedance.

The equation for the "infinite" Warburg impedance is given in eq. (4.7):

$$Zw = \sigma (\omega)^{-1/2}(1-j) \qquad (4.7)$$

On a Nyquist plot the Warburg impedance appears as a diagonal line with a slope of 45˚, On a Bode plot, the Warburg impedance exhibits a phase shift of 45˚.

In the Warburg impedance equation, σ is the Warburg co-efficient defined in eq. (4.8):

$$s = \frac{RT}{n^2F^2A\sqrt{2}}\left(\frac{1}{C^o\sqrt{D_o}} + \frac{1}{C^R\sqrt{D_R}}\right) \qquad (4.8)$$

In which,

D_o=diffusion coefficient of the oxidant

D_R=diffusion coefficient of the reductant

A= surface area of the electrode

n= number of electrons

4.4.3.3. Constant Phase Element

Capacitors in EIS experiments often do not behave ideally. Instead, they act like constant phase element as defined below [7].

The impedance of a capacitor can be expressed in eq. (4.9):

$$Z = (1/Y_0)\,(j\,\omega)^{-\alpha} \qquad (4.9)$$

Where,

Y_0 = C = the capacitance

α = an exponent which may vary for different behavior of the constant phase element. For capacitor it is 1.

4.5 EIS Measurements and Discussion

4.5.1 EIS spectra of a Fully Charged (SOC=1) Lithium ion battery.

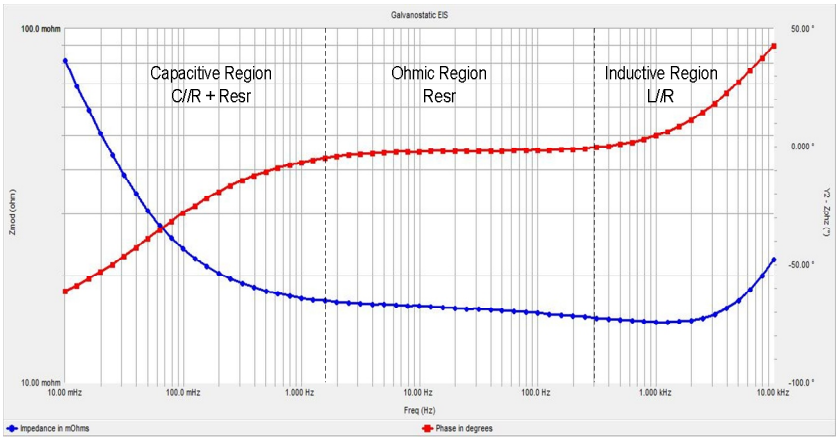


Figure 39 Galvonostatic EIS measurement Bode plot for Li-ion battery at SOC=1 at 0mA dc

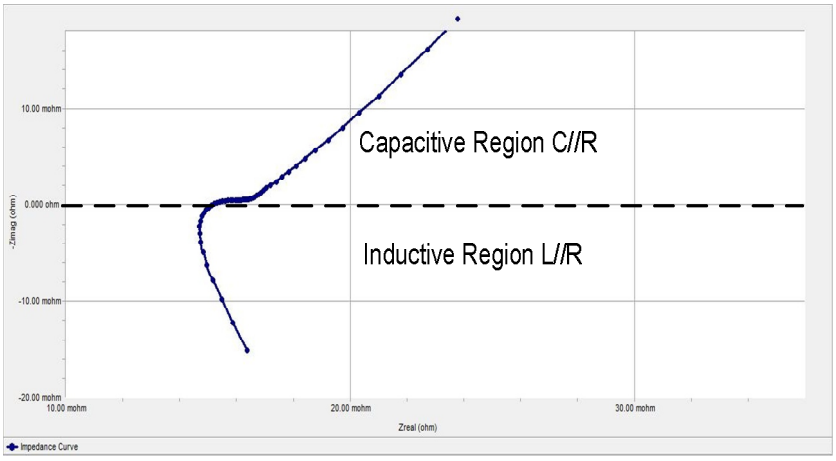


Figure 40 Galvonostatic EIS measurement Nyquist plot for Li-ion battery at SOC=1 at 0mA dc

The impedance spectrum of the lithium ion battery at SOC=1 is shown as Nyquist and Bode plot in Figure 39 and Figure 40 respectively. A semicircle on a complex plane diagram indicates the presence of a parallel combination of a resistor and a capacitor if Z imaginary is negative or a parallel combination of a resistor and an inductor if Z imaginary is positive. The Nyquist plot shown in Figure 40 shows a inductive behavior with frequencies >200Hz and shows a capacitive behavior at frequencies below<200Hz and >10mHz. The phase angle versus AC frequency plot suggests the value of Φ to be positive at high frequencies, corresponding to the inductive behavior of the battery. The phase angle gradually becomes negative and reaches a negative peak at -50˚, reflecting the capacitive behavior of the battery.

The impedance parameters of the lithium-ion battery were evaluated from the experimental impedance spectrum by an equivalent circuit non-linear least squares (NLLS) fitting procedure. The high frequency impedance data are inductive; therefore the inductance L and a resistance R_L are taken in parallel. The capacitive semicircles are depressed more so in the case of the high frequency small semicircle. Hence, a constant phase element CPE

denoted as Q1 is taken in parallel to a resistance R1 corresponding to the high frequency semicircle. The CPE arises due to distribution of microscopic material properties [4]. The interface between the electrode/electrolyte of the Li-ion cell is not smooth and uniform, as electrodes are made of fine particles of the active materials. The intercalation and deintercalation of lithium processes are not uniform throughout the surface of the electrodes. The admittance representation of CPE is given in eq. (4.10):

$$Y = Y_0 (j\,\omega)^n \qquad (4.10)$$

Where Y_0 is an adjustable parameter and $\omega=2\pi f$. For n=0, CPE represents a resistance, for n=1, a capacitance and for n=.5, a Warburg impedance. The NLLS-fit technique was employed using the equivalent circuit shown in figure 41 with the circuit description code: (RL) R (RQ) (RQ).

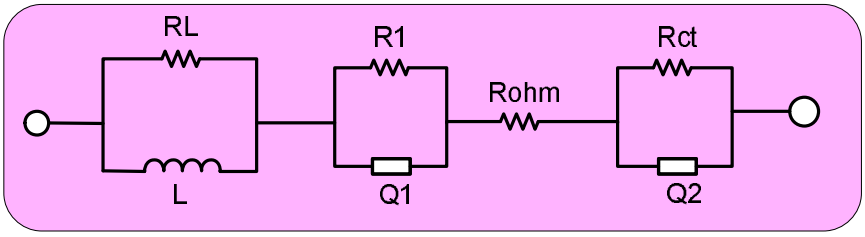


Figure 41 the equivalent circuit model used for NLLS fitting curve

4.5.2 EIS spectra of Lithium ion batteries at different SOCs and charge transfer current.

The electrochemical impedance is a function of state of charge, charge transfer current and temperature. The impedance variance due to temperature is quite significant but its study is out of scope of this thesis. The impedance data of the battery at different SOCs are important for us because it will affect the frequency response of the system. Since the EIS

data is a frequency characterization data, it accurately predicts the impedance for a range of frequencies and that of our interest for optimizing the frequency response of the system as a whole.

The EIS data is primarily used for studying the frequency response of the power system and its impact on the stability of the system. As a part of this research the impedance data at very critical stages of the battery charging stage is taken. This data will help us model the battery closed loop performance at these critical stages of the battery. The three impedance characteristics data are taken for the following states

1) Battery SOC=1 and DC current =10mA. (Constant Voltage Stage)
2) Battery SOC=.5 and DC current =500mA (Constant Current Stage-Charging)
3) Battery SOC=0 and DC current = 500mA. (Constant Current Stage-Charging)

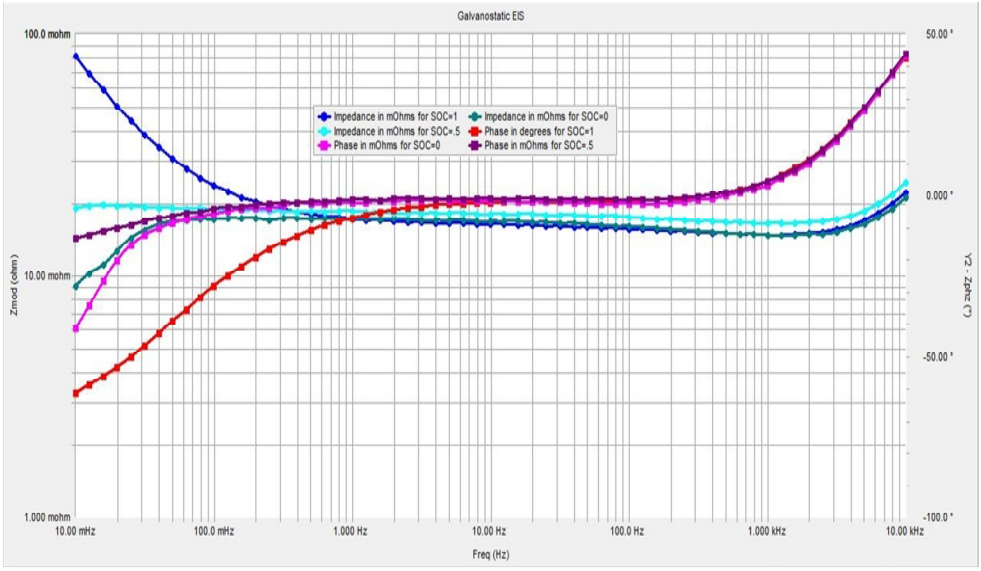


Figure 42 Galvonostatic EIS measurement Bode plot for Li-ion battery for 1) SOC=1 at 10mA 2) SOC=.5 at 500mA and 3) SOC=0 at 500mA

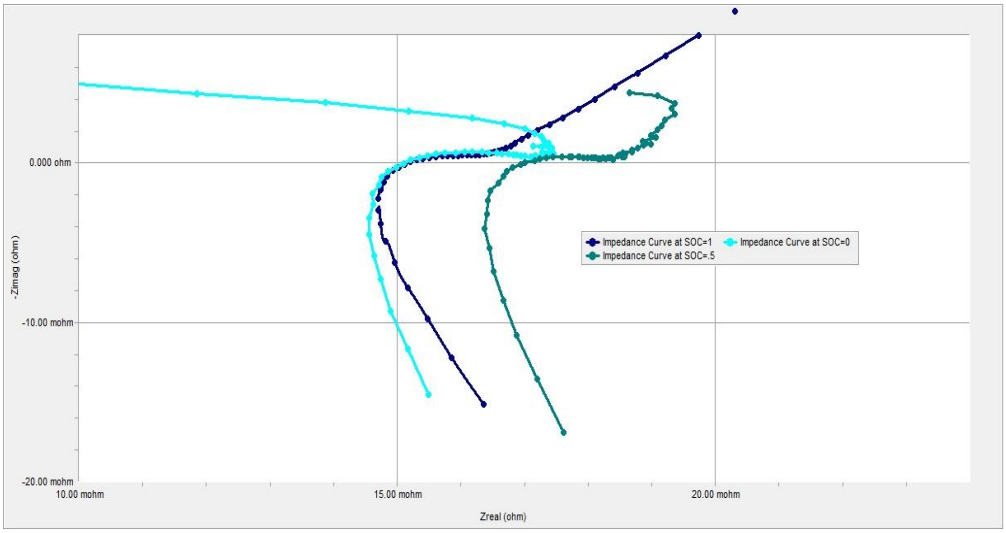


Figure 43 Galvonostatic EIS measurement Nyquist plot for Li-ion battery for

1) SOC=1 at 10mA 2) SOC=.5 at 500mA and 3) SOC=0 at 500mA

Table 1 Equivalent Circuit Parameters for different SOCs and charge currents

	SOC=1(I_{dc}=10mA)	***SOC=.5(I_{dc}=500mA)***	***SOC=0 (I_{dc}=500mA)***
Voltage(V)	3.666	3.318	**2.718**
R_L(Ohms)	31.39	6.859	**5.520**
L(nH)	243.5	271.5	**232.1**
R_{ohm}(Ohms)	15.21	15.77	**14.83**
R1(mOhms)	370.4	1.524	**2.52**
C1(F)(n=-1)	243.4	.756	**.6051**
R_{ct}(mOhms)	94.09	53.82	**18.77**
Y(Ohm^{-1})	158	1434	**1599**
n	.444	.776	**1.298**
R_{tot}(mohms)	**479.7**	**71.11**	**36.12**

4.5.3 Discussion of Equivalent circuit parameters.

The equivalent circuit parameter values are listed in Table 1 which is derived by fitting the data with the model shown in Figure 43. The inductance behavior was attributed to the geometric nature of the conductors and electrodes, and not to the faradic processes in the battery, and hence forth the chance in inductances across the various SOCs is not important to our study. The ohmic resistance (R_{ohm}) includes the resistance of the electrolyte, current collectors, and battery terminals, inter cell connectors etc. There is not much significant change in this value except when the SOC=0 the value becomes least. A summation of all the resistances (R_{ohm}+R1+ R_{ct}) will give you the DC resistance of the battery. Potentiostatic measurement methods use small signal voltage excitation which results in the small signal resistance of the battery, but since we have used a galvanostatic method to determine the DC resistance, the method ultimately gives us the large signal DC resistance of the battery. We see that the total resistance of the cell increases at SOC=0 and decreases with increase in SOC value. The resistances R1 and R_{ct} are most significantly affected by both the SOC and the dc current passed through the battery used for charging. We notice that R_{ct}+ R1 increases with increase in SOC mostly due to the effect of dc charge transfer current. We can say that the dc charge current and the resistance are pseudo linear. The Warburg CPE admittance and the double layer capacitance also changes with SOC which can largely affect the small signal frequency response of the battery.

Chapter 5

5. Maximum Power Point Tracking & Solar Cell Modeling

5.1 Introduction

Satellites which are launched to the low earth orbits (LEO) can have a range of power requirements from as little as watt or two to a few kilo watts. Most of them will have fixed solar arrays that encounter varying solar illumination characteristics across a typical orbit. Most will also experience frequent eclipse periods. For spacecraft within this category, there is a definitive need to have a flexible solar array interface that can adapt to the changing solar array characteristics while at the same time providing the ability to provide power to charge the batteries [2].

A Maximum Power Point Tracker (MPPT) is used for keeping the solar array at its maximum power point voltage and hence extracting the maximum power from it. The efficiency of this converter is about 90-95%, and introduces the main inefficiency in the power system. The benefits of this MPPT system are only realized in situations where the maximum power point (MPP) of the array is changing significantly whilst the spacecraft is in sunlight. This is the case in low earth orbit (LEO) where the array temperature, and hence MPP, changes considerably over the sunlight period of the orbit. In an orbit such as geostationary orbit, where there are extended periods of sunlight and solar arrays at equilibrium temperature, the inefficiency of the MPPT would make the use of this topology impractical [2].

Three popular tracking methods based on power feedback are widely adopted in PV power systems. They are the perturbation and observation method, the incremental conductance method and the hill climbing method. Of these, the perturbation and observation method (P&O), which moves the operating point toward the maximum power point by periodically increasing or decreasing the array voltage, is often used in photovoltaic systems. It has been shown that the P&O method works well when the irradiance does not vary quickly with time; however, the P&O method fails to quickly track the maximum power points unless the sampling time and the duty cycle steps are properly chosen [23].

5.2 Modified Perturb and Observe Method

For a rapidly changing **irradiance** conditions like in space applications the sampling interval should be set higher than a threshold in order to avoid instability and reduce the oscillations during steady state. Lowering the step change in duty cycle reduces the oscillations but makes the algorithm inefficient when the irradiance conditions changes rapidly. Figure 44 shows the successful tracking of the MPP with the irradiance level changing constantly.

An adaptive P&O method is adopted where the change in power due to rapidly varying irradiance is detected and the duty cycle step change is made in the direction of the change in power. Figure 45 shows the flowchart for the modified P&O algorithm. The automatic tuning is according to the equation a (k) =M.|ΔP|/a (k-1). Where a is the incremental change in duty cycle, ΔP is the change in power and M is a constant. If the value |ΔP|/a (k-1) is greater than the threshold e, the effect of the power variation is reflected on

the duty cycle change. The modified P&O algorithm was found to be most accurate, fast and simple to implement.

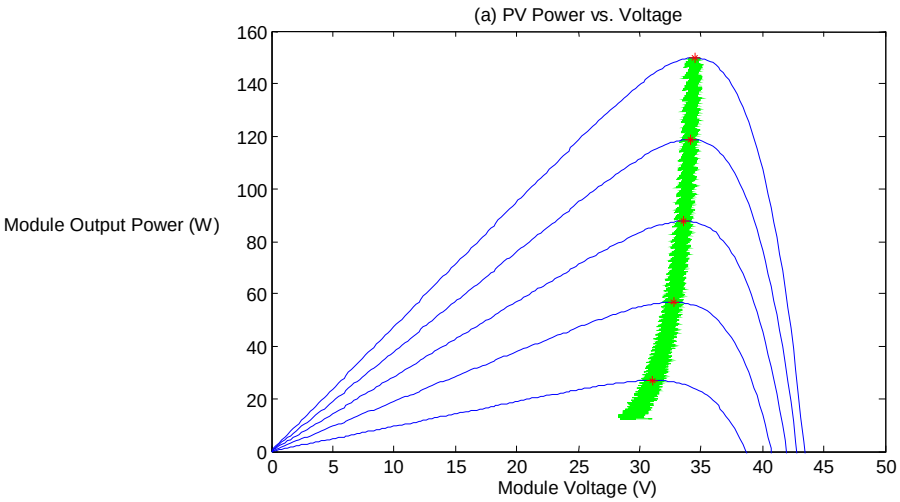


Figure 44 Maximum Power Point Tracking with variable irradiance level

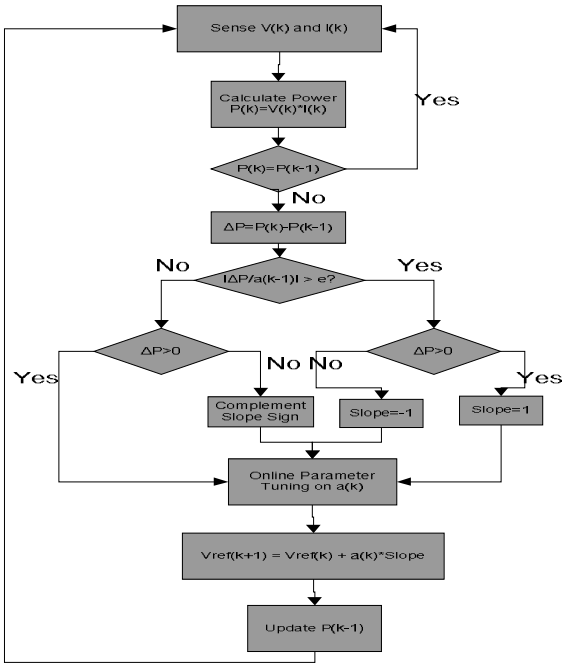


Figure 45 Adaptive P&O methodology flow chart

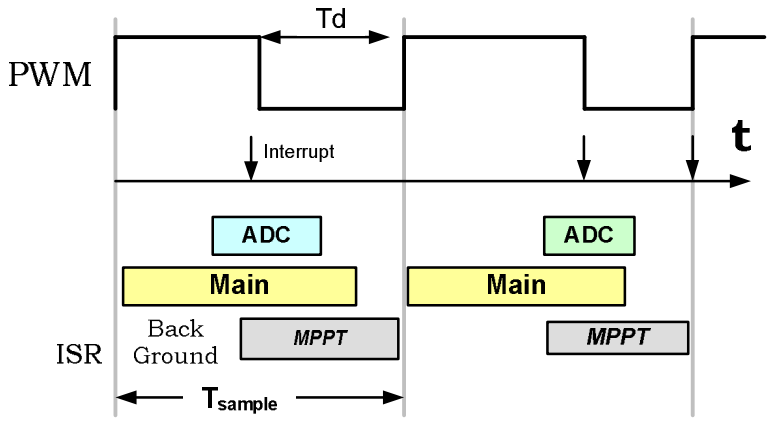


Figure 46 Sampling Loop Implementation

The sampling time determines the various interrupt service schemes and other factors in the case of having an optimized MPPT for varying irradiance conditions and temperature. The AD conversion is triggered using a timer based PWM with an interrupt service routine at the rising edge of the PWM. The AD conversion can also be triggered using the AD module at a constant sampling rate. After the conversion another interrupt service routine is triggered for the Maximum Power Point Tracking algorithm. At the end of executing this algorithm the duty cycle is updated. The time delay between the AD conversion and the triggering of the interrupt for the MPPT is Td as shown in Figure 46. The time delay includes the AD conversion time and the interrupt latency and this must be below the sampling time or the buck converter switching interval.

A disadvantage of the P&O algorithm is a tracking error which might occur during rapid changes of the solar irradiance. The error occurs when the change in irradiance during one sampling interval is larger and in the opposite direction of the power change due to the duty cycle modulation. This will confuse the MPPT, and it will adjust the duty cycle in the opposite direction. In order to reduce the risk of confusing the MPPT during these changes,

the sampling interval of the P&O algorithm should be set as low as possible without causing instability. In [26] it is stated that the system sampling interval should be set according to the converter's dynamics, so that after each duty - cycle perturbation the system is allowed to reach the steady state operation before the next perturbation. If the sampling is set lower than this, the MPPT might become confused by the PV array and the converter transient behavior. In order to find the time at which the system has reached steady state one has to look at the system model. It is shown in [27] that the array power is proportional to the PV voltage squared, as shown in the below equation. Therefore by finding a model for the control to PV - array voltage, one can calculate the time before the transients caused by the control perturbation has reached a certain value. When the system has reached this value, the MPPT can safely run without being confused by the system dynamics.

$$p(t) = -V^2_{PV}(t)/R_{MPP} \qquad (5.1)$$

$$R_{MPP}=V_{MPP}/I_{MPP} \qquad (5.2)$$

Where R_{MPP} is the steady state equivalent resistance of the PV load at the quiescent operating point, where it is assumed that the operating point is in the vicinity of the MPP. The sampling interval can now be found by defining a region around the steady state value of which must be reached before a new sampling is allowed.

5.3 Modeling Photovoltaic Cells

The PV module was modeled in SIMULINK by considering the equivalent circuit of a solar cell as a current source in parallel with a diode. The output of the current source is directly proportional to the light falling on the cell. The diode determines the I-V

characteristics of the cell. For modeling the PV array the temperature dependence of the photo current IL and the saturation current of the diode Io is considered. A series resistance RS to the current source is included. A single shunt diode was used with the diode quality factor set to achieve the best curve match. The equations that led to the modeling of the PV from [28] are worth mentioning.

The relationship between the cells terminal voltage and current is given by the Shockley equation when the cell is not illuminated. The current generated is offset from I_L the photo generated current given by eq. (5.3)

$$I = I_L - I_o(e^{q(V+IRs)/nkT}-1) \qquad (5.3)$$

The relationship between the photo current and temperature is linear and is deduced by noting the change of photo current with the change of temperature.

$$I_L= I_{L\,(T1)} (1+K_o (T-T_1)) \qquad (5.4)$$

$$K_o = (I_{SC(T2)}- I_{SC(T1)})/(T_2-T_1) \qquad (5.5)$$

The terminal voltage of the solar cell depends on the temperature and is given by eq. (5.6)

$$Vt= A.k.T/q \qquad (5.6)$$

Where q is the electron charge, k is the Boltzmann constant; A is the diode quality factor. The series Resistance Rs is used from the manufacturers specifications from the solar cell's datasheet. Using the above equations the model was designed with temperature and irradiance as its input parameters.

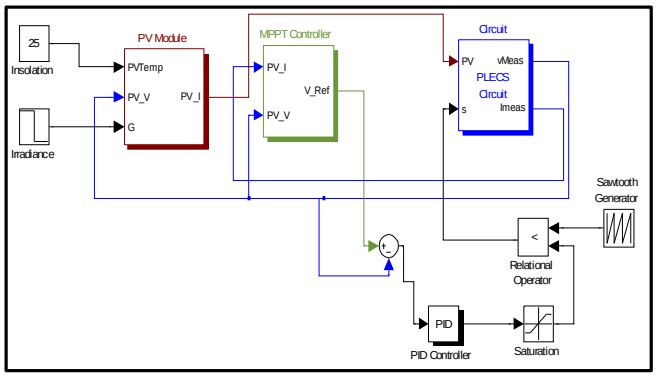


Figure 47 Simulation of MPPT algorithm implementation in MATLAB, Simulink

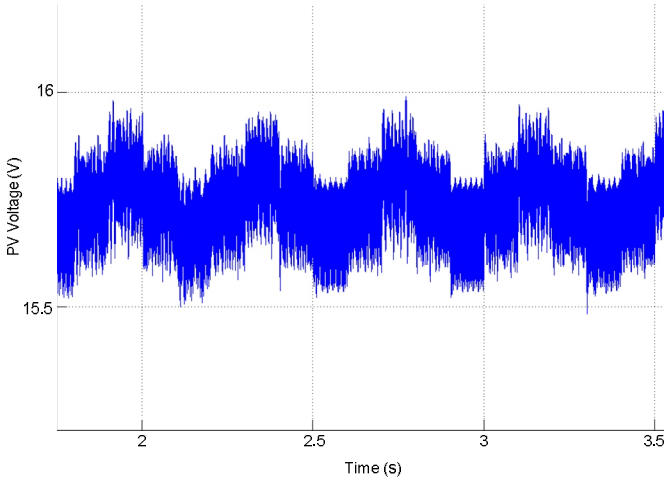


Figure 48 shows the PV voltage with sampling time T_s=.001 and ΔV_{ref}=.1

The complete setup was simulated using Simulink to test its performance in rapidly varying irradiance conditions. Figure 47 shows the complete simulation set up using MATLAB; the power stage was implemented using PLECs toolbox. Figure 48 shows the PV voltage with sampling time T_s=.001 and ΔV_{ref}=.1.

Chapter 6

Digital Power Control Modeling

6.1 Introduction

The heart of the satellite power system is the central controller that controls the FBCM, FDPOL modules and does other housekeeping services like monitoring the health of the power system and communicating the command and data handing subsystem. The central controller used in this power system is itself a powerful digital signal controller that can multi task with very high performance. The control algorithms and methods for the FBCM and the FDPOL modules are discussed here in this chapter.

6.2 Central Controller Engine

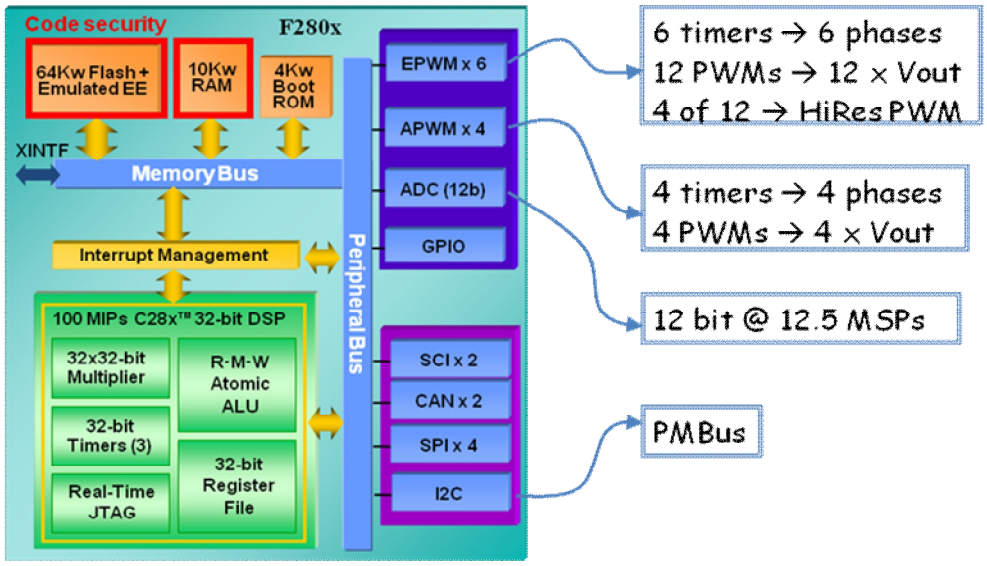


Figure 49 Central controller engine architecture

Figure 50 Central controller control card used for the FBCM and FDPOL

Modern 32-bit DSP controllers, such as Texas Instruments, TMS320F280x [19], with processor speed up to 100MHz and enhanced peripherals such as, high resolution PWM module, 12-bit A/D converter with conversion speed up to 160nSec, 32x32-bit multiplier, 32-bit timers and real-time code debugging capability, gives the power supply designers all the benefits of digital control and allows implementation of high bandwidth, high frequency power supplies without sacrificing performance. Figure 49 shows the micro controller engine architecture and Figure 50 shows the picture of the controller card used in FDPOL and FBCM. The extra computing power of such processors also allows implementation of sophisticated nonlinear control algorithms, integrate multiple converter control into the same processor and optimize the total system cost. We will take a closer look at the enhanced peripherals suited for digital power control in more detail.

6.3 Controller Power Control Peripherals

6.3.1 Analog to Digital Converter (ADC)

The ADC module in the 280x has been enhanced to provide flexible interface to ePWM peripherals. The ADC interface is built around a fast, 12-bit ADC module with a fast conversion rate of up to 80 ns at 25-MHz ADC clock. The ADC module has 16 channels, configurable as two independent 8-channel modules. The two independent 8-channel

modules can be cascaded to form a 16-channel module [20]. Although there are multiple input channels and two sequencers, there is only one converter in the ADC module.
The full scale input voltage to the ADC is 3V. There fore the gain provided by the ADC is given by the expression in eq. (6.1).

$$K_{eadc} = \frac{2^{noofbits}}{V_{fullscale}} \qquad (6.1)$$

6.3.2 Normal PWM and High Resolution PWM

The ePWM peripheral is used to perform a function that is mathematically equivalent to a digital-to-analog converter (DAC). The effective resolution for conventionally generated PWM is a function of PWM frequency (or period) and system clock frequency [21]. The gain due to the PWM module is given in eq. (6.2) and (6.3) [17].

$$PWMresolutioninbits(N_{PWM}) = Log_2 \frac{T_{PWM}}{T_{SYSCLOCK}} \qquad (6.2)$$

$$K_{ePWM} = \frac{1}{2^{N_{PWM}} - 1} \qquad (6.3)$$

If the required PWM operating frequency does not offer sufficient resolution in PWM mode, we can consider HRPWM. The HRPWM is based on micro edge positioner (MEP) technology. MEP logic is capable of positioning an edge very finely by sub-dividing one coarse system clock of a conventional PWM generator. The time step accuracy is on the order of 150 ps. A normal PWM modulation technique is shown in Figure 51; the PWM module has its own time base that is used for the increments of the period of the PWM. The PWM time base clock is pre-scaled from the system clock. The PWM period will be

(TBPRD+1) times the TBCLK. Duty modulation for EPWMxA is set by CMPA, and is active low (that is, the low time duty is proportional to CMPA). Duty modulation for EPWMxB is set by CMPB and is active low (that is, the low time duty is proportional to CMPB).

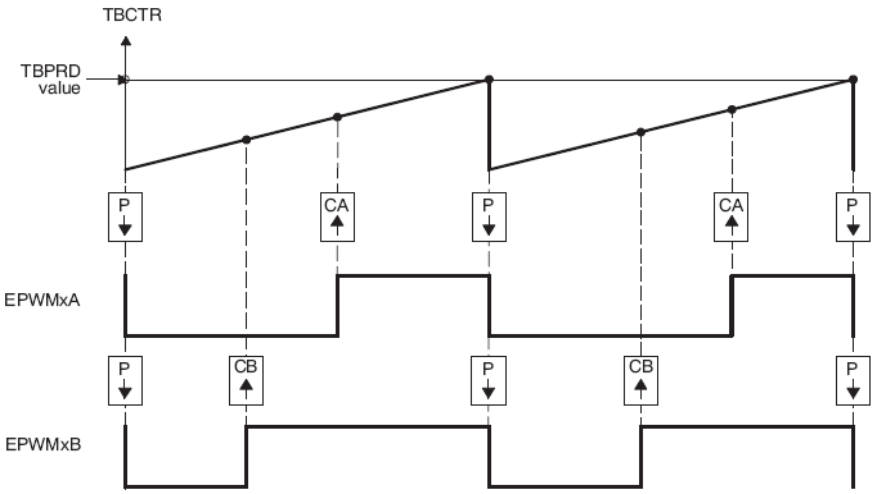


Figure 51 PWM Modulation Technique

In a typical power control loop, the duty cycle generated will be a fractional quantity, the PWM resolution provided with only CMPA register can cover the integer part of the duty cycle but the fractional part is almost always lost. The CMPAHR register is used to extend the resolution by 8 more bits using the CMPAHR register and thus achieving a very high resolution PWM.

6.4 Modeling the control loop

Switch mode power supplies have always had digital component; they have a control effort with a discrete update interval. That interval is the switching period. The net result is

that there can be latency in the response to disturbance in the control effect. When we analyze a DC/DC system, this latency shows up as a rotation in the phase of the open loop system. When we introduce digital components into the system, here are additional phenomena that must be taken into account. These things are:

1) Feedback quantization
2) Control effort quantization
3) Delay needed to sample the feedback and calculate the control effort.

The key to implementing a digitally controlled power supply is to understand these effects.

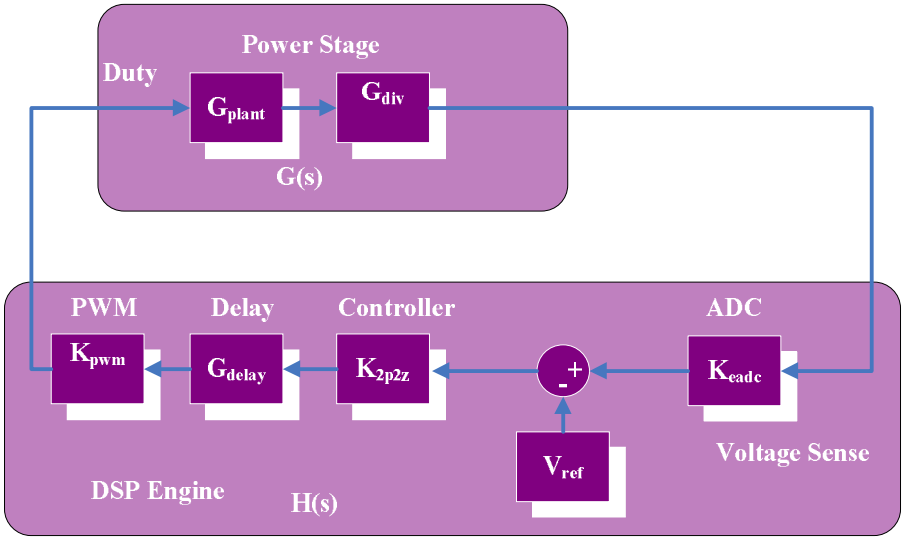


Figure 52 Digital Closed Loop control elements

Figure 52 shows the closed loop block diagram for a digitally controlled DC/DC converter that first senses the feedback voltage with the ADC and then compared it with a digital reference and then the controller calculated the digital effort and then the command is fed back to the plant. For this system the total open- loop gain is given in eq. (6.4)

$$T(s) = G(s)H(s) \qquad (6.4)$$

Then the closed loop gain, from the PWM control effect to the sensed output voltage is

$$\frac{\text{Vsense}}{duty} = \frac{G(s)}{\left[1+G(s)H(s)\right]} \qquad (6.5)$$

The contributors to the closed loop system are itemized in Table 6.1. To determine the frequency response of the power supply, and from that, determine the stability margin of the system, we need to define the dynamic gain for each block. Once we have the transfer function for each block, the standard measure of stability can be applied:

- Gain Margin- The inverse of the magnitude of the open-loop gain, expressed in dB, at the frequency where the phase of the closed-loop gain is 180 degrees.
- Phase Margin- The phase of the open-loop gain, expressed in degrees, where the magnitude of the closed loop gain is 1.

Table 2 Closed Loop system contributors

K_{AFE}	Analog front-end gain in V/V
K_{EADC}	Gain of the enhanced ADC in LSB/volt
G_{2z2p}	Digital compensator gain
G_{delay}	Total sampling and compensation delay
K_{PWM}	PWM gain in duty/LSB
G_{plant}	Transfer function of the power stage.
G_{div}	Divider network transfer function

6.5 FBCM Control Loop

The connection between the physical system and the software control algorithm which is implemented on a TMS320F2808 signal processor is the feedback signals and the PWM outputs. The quantities sensed include the PV current/voltage and the battery charging current/voltage. The sensed quantities are scaled appropriately, and then connected to the ADC (analog to digital converter) pins. The ADC samples these quantities and turns them into a numerical representation. A block diagram of the software is shown in Figure 53.

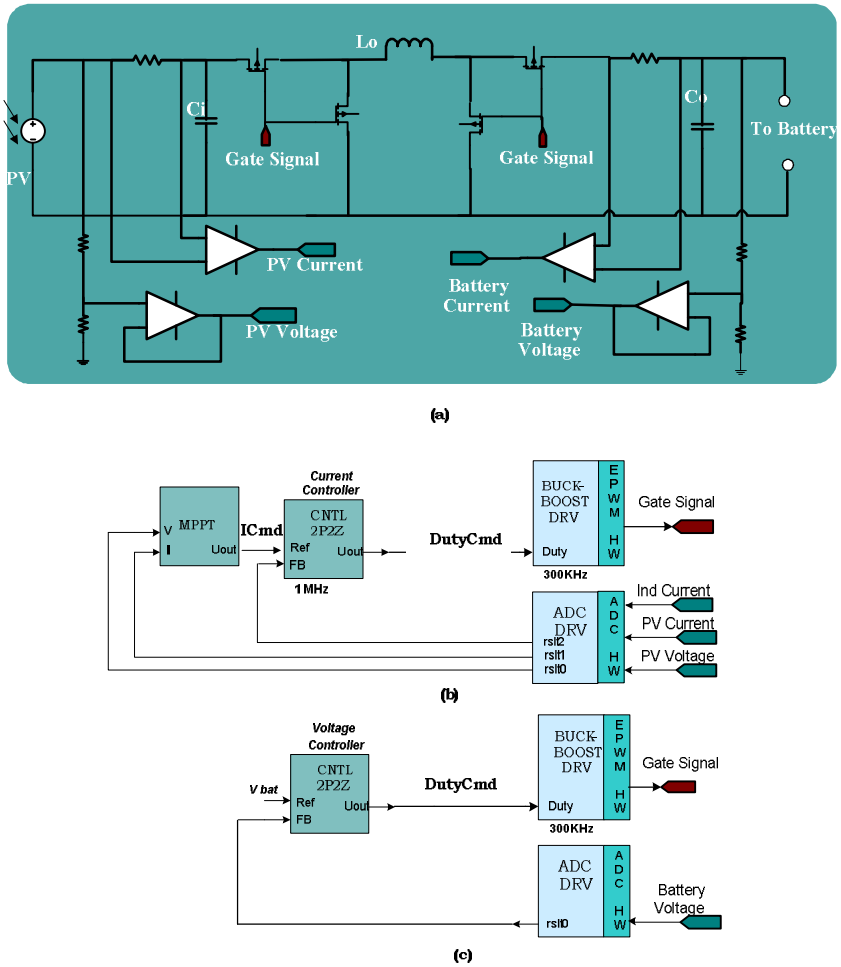


Figure 53 FBCM a) power stage b)MPPT/Current Loop c) Voltage Loop Implementation using Digital Controller

For the BCM there are two modes of operation, during the MPPT/Current mode the PV current and voltage are sensed. The MPPT algorithm generates the current command for the 2pole 2zero controller to generate the duty command for the power stage. During the MPPT/Current mode the inductor current is regulated to the current command which is essentially the maximum power point current of the solar panel. During this mode the battery is essentially charged with a constant current, and when the battery is fully charged the MPPT mode is stopped and the voltage control mode takes over. Here the battery voltage is fed back to the controller and is compared to a fixed voltage reference.

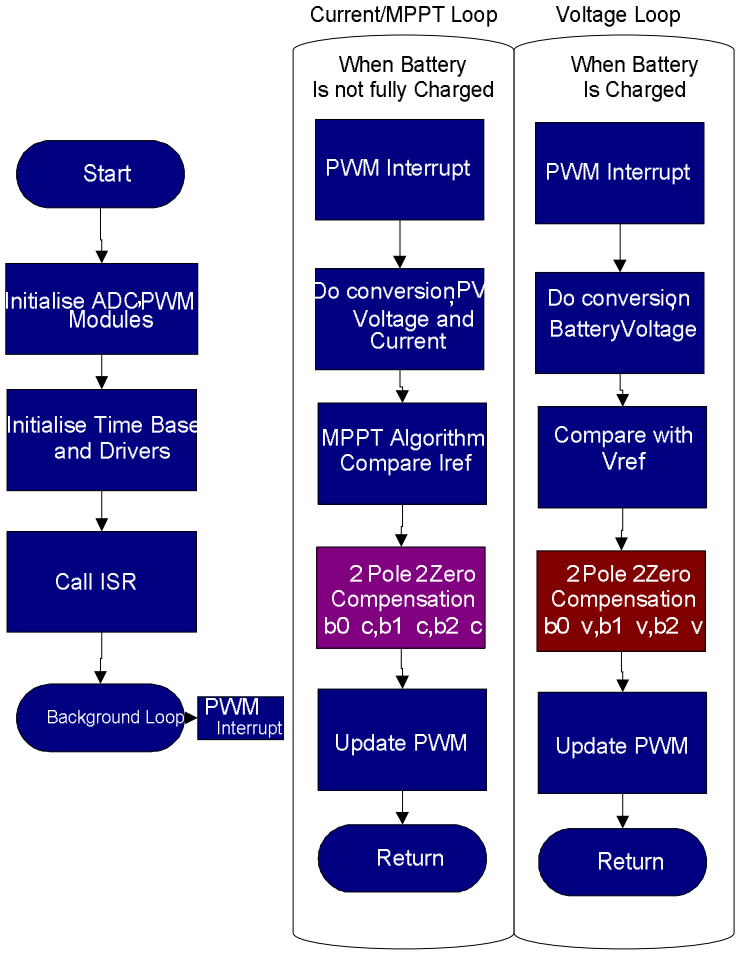


Figure 54 Software Algorithm for Current/MPPT loop

Figure 54 shows the software algorithm for the FBCM loop. The software algorithm is implemented in C and assembly language code in the TI C2000 compiler. The software is also modular in structure, and separated into the background loop module, compensator and PWM driver and the main module. The main module contains code for initialization and for features of enabling and starting the program, modifying the voltage and control parameters. The background module has the main interrupt loop that enables a chain of events in a fixed interval of time. Usually the interrupt is triggered by the PWM timer at the rising edge of the train of PWM signals. The interrupts triggers the AtoD conversion and the MPPT algorithm is ran to generate the Iref to compare it with in the case of current mode or it is compared to a fixed Vref in the case of voltage mode. Then the error voltage is passed through the 2 pole 2 zero compensator with the fixed coefficients for each mode. The output of the compensator is the input for the PWM driver that updated the duty cycle of the PWM module.

6.6 Novel Dynamic Multi-state Compensator for Battery Charging.

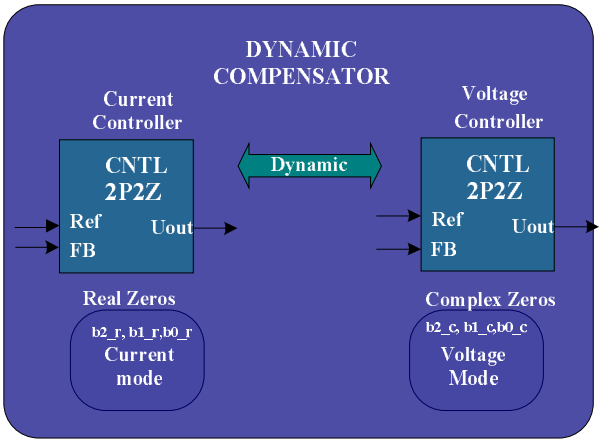


Figure 55 Dynamic compensator model for battery charging algorithm.

A dynamic compensator model (Figure 55) is proposed in this work. The stability models seen is the previous chapters for the charging control loop and voltage control loop suggest that a single compensator may not yield a optimum closed loop control. Let us take the example of the buck boost power stage compensation. The charging control loop is rather simple to stabilize due to the two poles in the system are spread out. For stabilizing the system we can use two real zeros and an integrator pole to adjust the gain and to get the desired crossover frequency. When the charging loop is discontinued and the voltage loop has begun, the power stage transfer function has a double pole. The digital controller platform allows us to adjust the FIR coefficients of the compensator to get a pair of complex zeros which can be used to compensate the double pole in the system.

6.7 FDPOL Control Loop

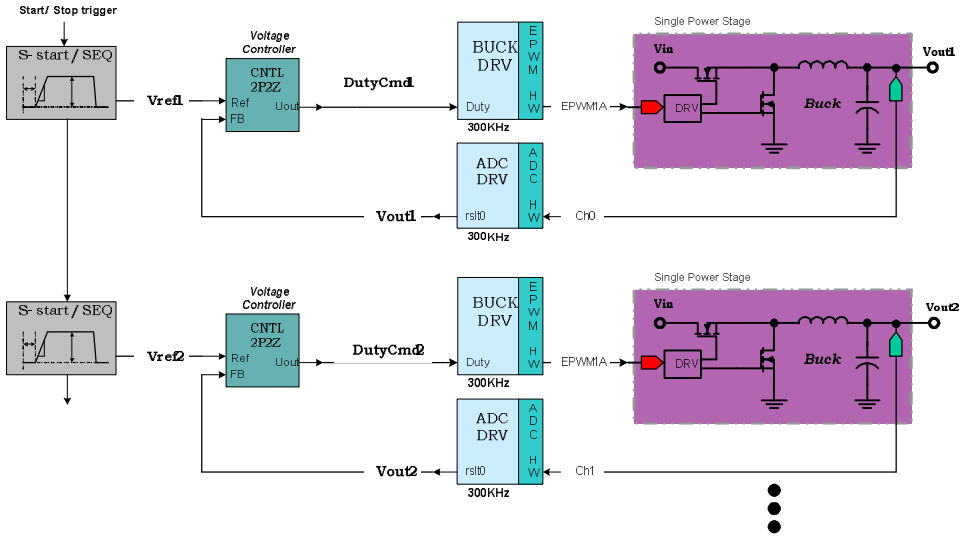


Figure 56 FDPOL Control Loop Model

The connection between the physical system and the software control algorithm which is implemented on a TMS320F2808 signal processor is the feedback signals and the

PWM outputs. The quantities sensed are the output voltages of the power stages. The sensed quantities are scaled appropriately, and then connected to the ADC (analog to digital converter) pins. The ADC samples these quantities and turns them into a numerical representation. A block diagram of the software is shown in Figure 56. The FDPOL control loop consists of only one voltage loop. The ADC results are digitally compared to a fixed voltage reference and it passed through a second order FIR filter which adds two zeros and one integrator pole to the system. The voltage loop generally has a double pole in the system that might either need a complex pole or a real pole to compensate the system and get a good phase margin and desired bandwidth. The Flexi-sat Digital Power Designer Software can help the user program the controller according to the power stage to get the desired stability and output voltage.

Figure 57 shows the software algorithm for the FBCM loop. The software algorithm is implemented in C and assembly language code in the TI C2000 compiler. The software is also modular in structure, and separated into the background loop module, compensator and PWM driver and the main module. The main module contains code for initialization and for features of enabling and starting the program, modifying the voltage and control parameters. The background module has the main interrupt loop that enables a chain of events in a fixed interval of time. Usually the interrupt is triggered by the PWM timer at the rising edge of the train of PWM signals. The interrupts triggers the AtoD conversion it is compared to a fixed Vref for a voltage mode. Then the error voltage is passed through the 2 pole 2 zero compensator with the fixed coefficients for each mode. The output of the compensator is the input for the PWM driver that updated the duty cycle of the PWM module.

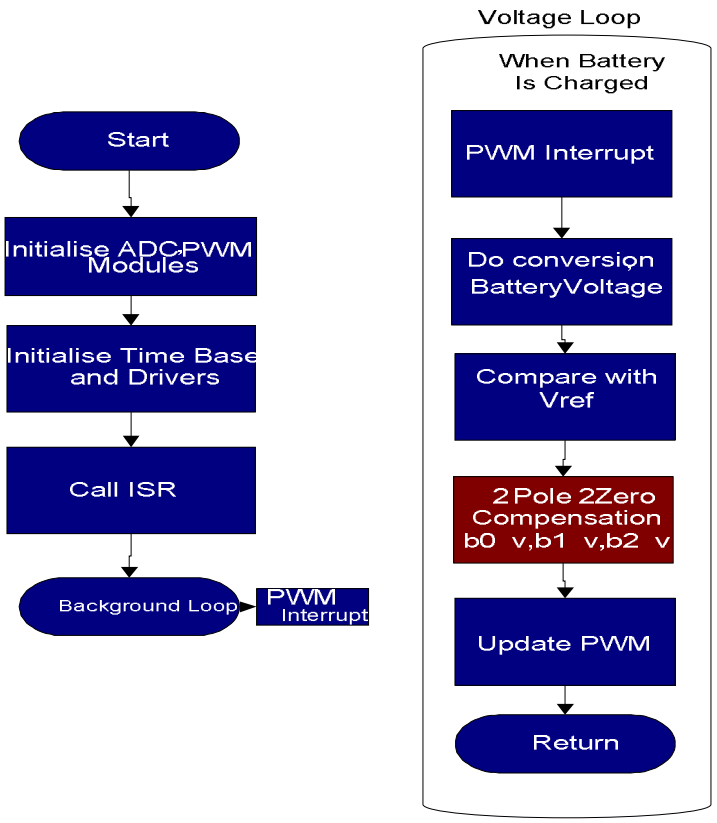


Figure 57 FDPOL software algorithm

6.8 PWM Drive for Discontinuous Conduction Mode

In the battery charging application, the synchronous switch converters have to be operated with a lot of caution because, improper switching can lead to reverse current from the battery to the source or ground. This may lead to damage of the MOSFET switches and the components in the path of the reverse current. For avoiding this synchronous switching pattern during continuous current mode is discontinued and changed to non synchronous switching method as shown in Figure 58.

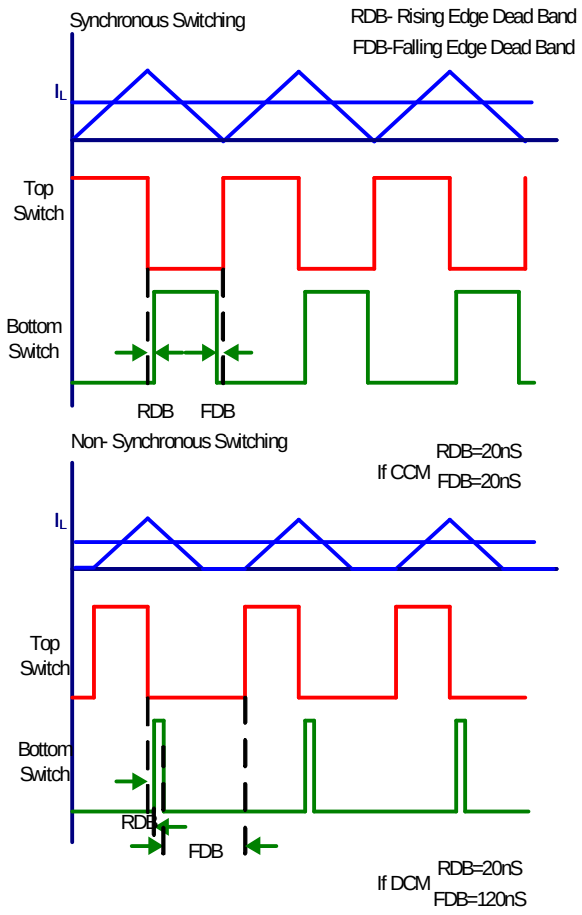


Figure 58 Synchronous Switching and Non-Synchronous switching

The change of the synchronous mode to non-synchronous mode is done using the features in the PWM peripheral of the DSP. For a synchronous mode switching, the dead band is set to minimum to avoid losses during the dead time. During the non-synchronous switching mode, the falling edge dead band is increased significantly with respect to the raising edge dead band, hence achieving a single shot pulse like bottom switch pulse. This would not allow the bottom switch to conduct when the inductor current tends to become negative. This non-synchronous type of operation will prevent the battery from discharging into the converter.

Chapter 7

7. Flex-Sat Digital Power Designer Software and Hardware Implementation

7.1 Introduction

The flexi-Sat software is a tool used to configure the compensation parameters of the FBCM and the FDPOL module. The software gives the designers the ability to reprogram the firmware in the controllers so that it fits the specifications required for the design. Digital power control is becoming more and more common in the low power DC-DC converter design since it gives the desired flexibility at a very low cost margin over analog controllers. In this chapter the working the Flexi-sat Digital Power Designer Software and the hardware implementation of the FBCM and FDPOL is discussed.

7.2 Flexi-Sat Digital Power Designer Software

Figure 59 shows the purpose of the software to provide user interface to the FBCM and FDPOL to configure, re-program the FBCM and FDPOL modules. Figure 60 shows the front panel of the Flexi-Sat Power Designer Software. The software was designed using National Instruments, Labview program, but the application can be run as a standalone software using

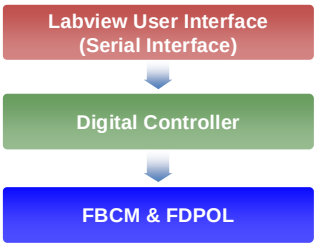


Figure 59 User control to the FBCM and FDPO

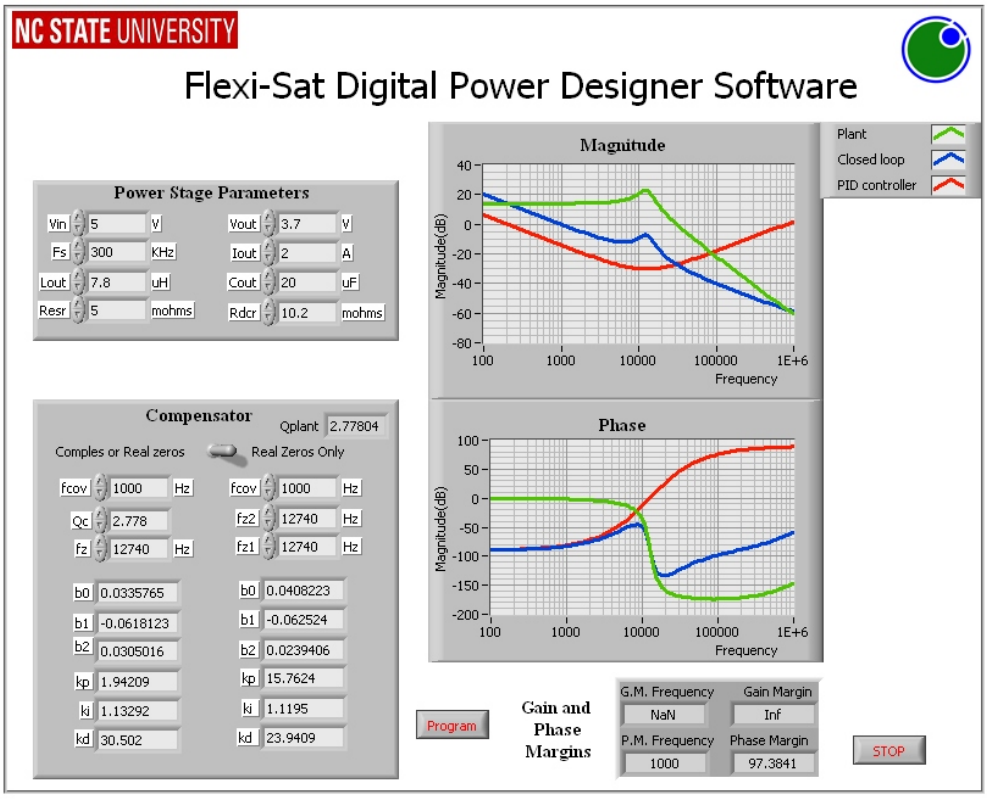


Figure 60 Flexi-Sat Digital Power Designer Software-showing design with real compensator

Labview Runtime Engine version 8.2.1. The software takes user inputs about the power stage parameters like the input voltage, switching frequency, output voltage, inductor and output capacitor, and the load current values. Then the software allows the user to design the compensation for the system.

Figure 61 shows the two types of continuous time compensators, one has real zeros and one has complex zeros. There are three gain and phase plots shown in the right hand side of the front panel. One is the bode plot of the plant open loop transfer function, and the other two are the compensator and the closed loop systems respectively. From the bode plot of the plant transfer function, the Q of the system is already calculated and is shown in the front

panel. If Q is high enough (Q>.5) then the plant need a complex zeros in the compensator, if Q<.5 then it need real zeros [16].

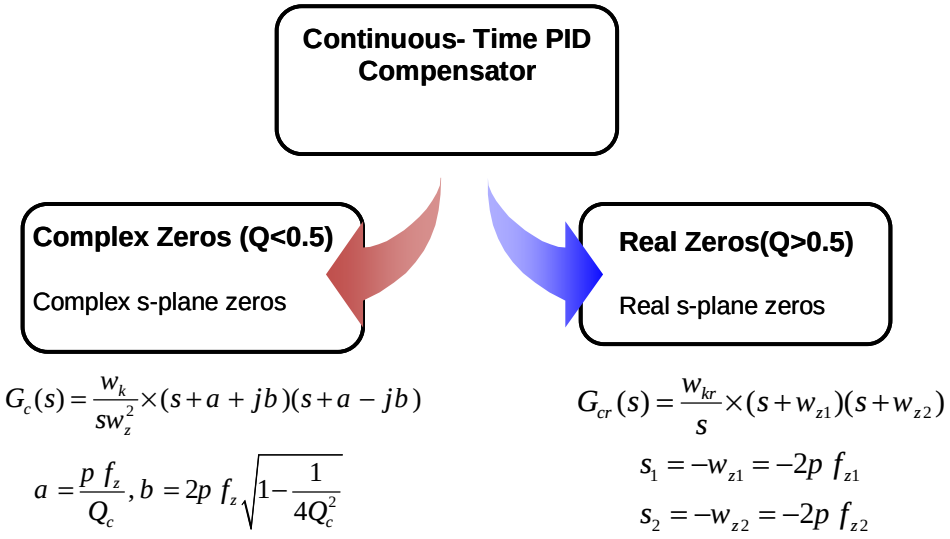


Figure 61 shows the two types of continuous time compensators which are real and complex

The user enters the desired cross over frequency (Fcov) and the Q of the desired double zero for the compensator and also the zero frequency. The software either chooses the complex compensator or the real compensator. Only one of them will be applied to the plant and the loop gain will be shown. If a real compensator is chosen, then the cross over frequency along with the two zero frequencies are taken as input from the user. The closed loop gain calculation is done when the run button is activated. Figure 60 shows an example with real zeros and Figure 62 shows an example with complex zeros.

The compensator block has 2 poles and 2 zeros and is based on the general IIR filter structure. The transfer function is given by eq. (7.1) :

$$\frac{U(z)}{E(z)}=\frac{b_0+b_1z^{-1}+b_2z^{-1}}{1+a_1z^{-1}+a_2z^{-1}} \qquad (7.1)$$

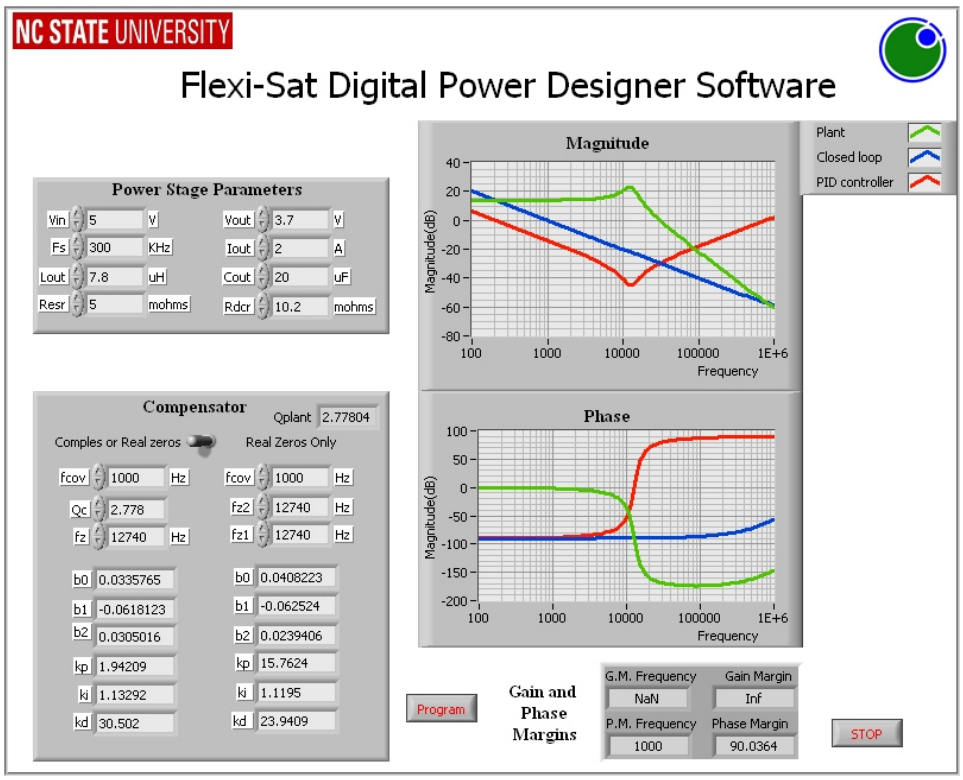


Figure 62 Flexi-Sat Digital Power Designer Software-showing design with complex compensator

The 2 pole 2 zero compensator is further simplified to a PID form where a_1=-1 and a_2=0 and now the numerator coefficients becomes eq. (7.2, 7.3, 7.4).

$$b_0 = K_p + K_I + K_D$$
$$b_1 = -K_p + K_I - 2K_D \quad (7.2,7.3,7.4)$$
$$b_2 = K_D$$

The continuous compensator is made discrete using bilinear transformation and the coefficients b0, b1, b2 are calculated and displayed in the compensator panel. The PID discrete equivalents are also displayed. Note that the PID coefficients are not continuous. The compensator coefficients can be programmed to the controller using the program option. The labview interface is set for a serial UART communication interface with the controller.

7.3 Hardware Implementation and experimental results.

7.3.1 Hardware Test bench platform- Charger with TMS320F2808 ezdsp kit

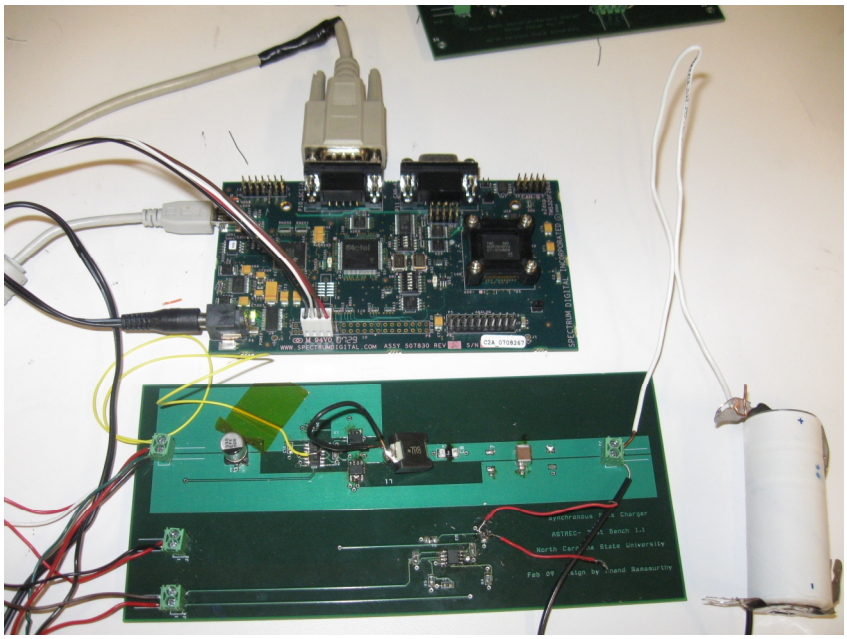


Figure 63 Synchronous Buck Based Battery Charger

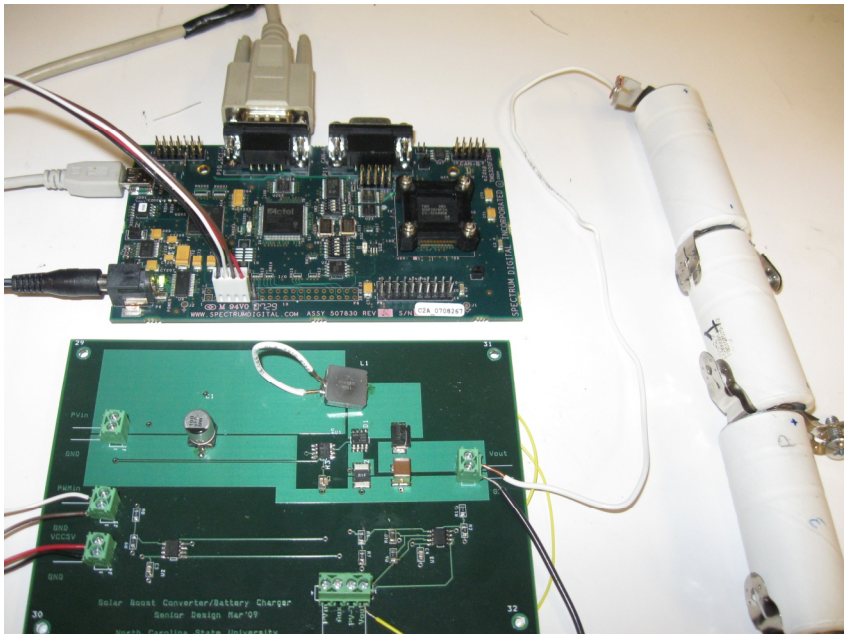


Figure 64 Non-Synchronous Boost Based Battery Charger

7.3.2 Synchronous Buck Charger Waveforms

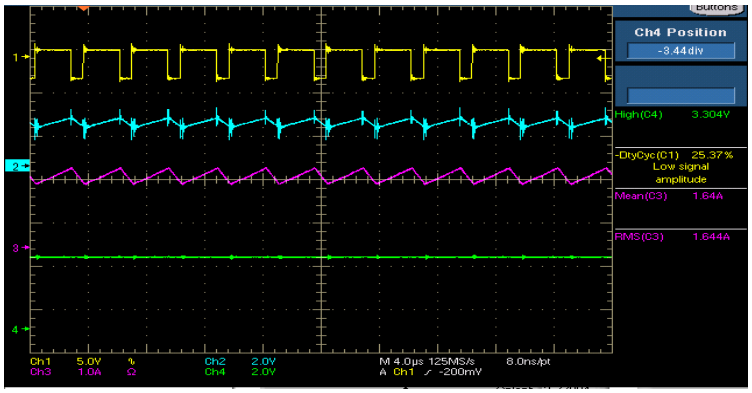


Figure 65 Voltage Regulation for Buck Converter Vin=5V, Vout=3.3V, Iout=2A

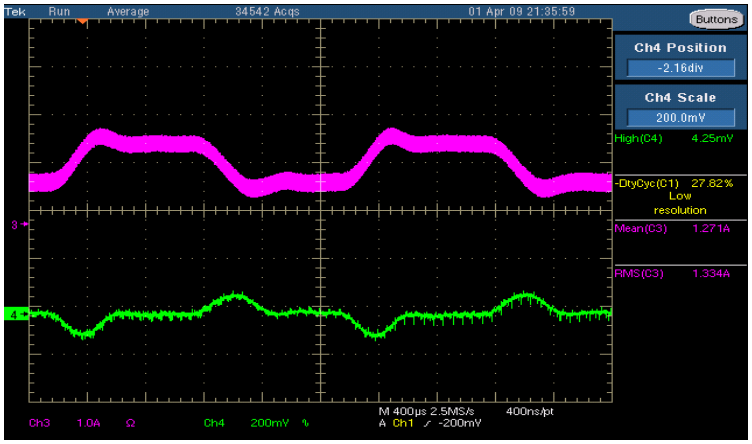


Figure 66 Transient performance of Buck regulator: 1A-2A step, 100mA/uSec slew rate

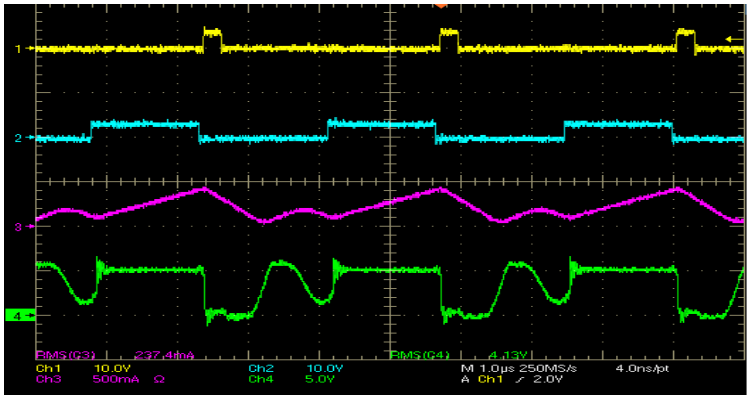


Figure 67 Non Synchronous Buck operation during light load operation

7.3.3 Non- Synchronous Boost Charger Waveforms

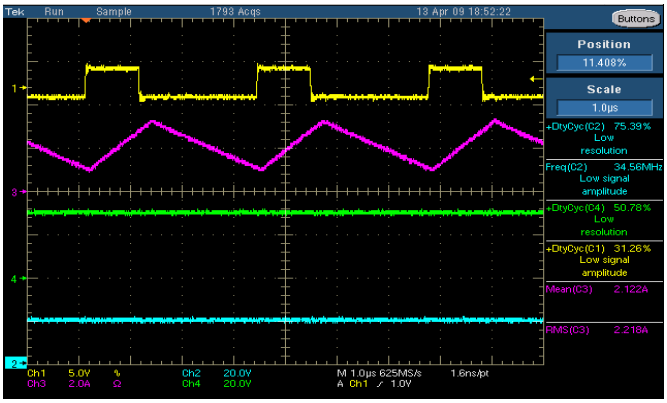


Figure 68 Voltage Mode Boost Converter Vin=14V Vout=28V Iout=2A

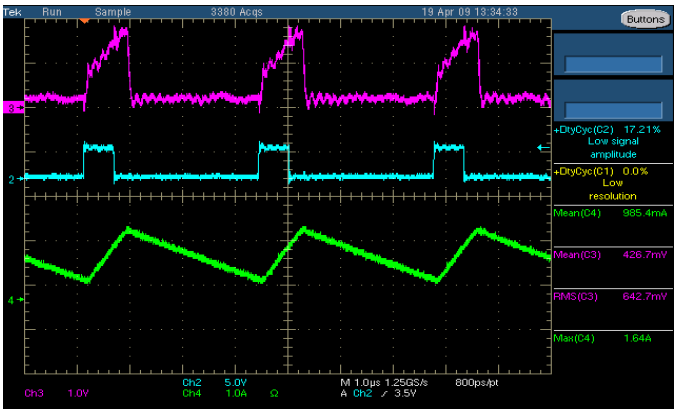


Figure 69 Current Mode Boost Converter Iout=2A

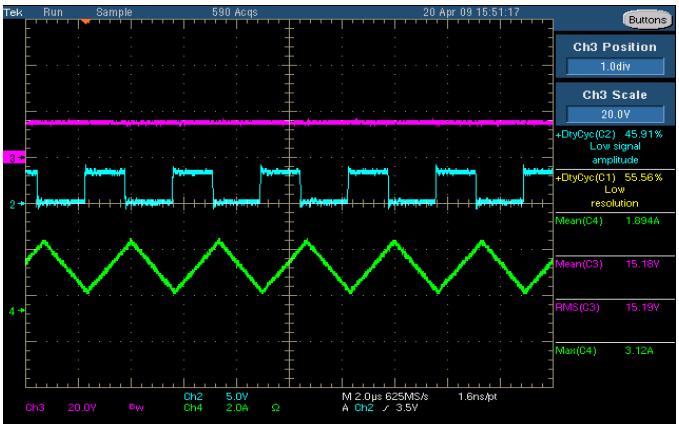


Figure 70 MPPT/Current Mode Boost Converter Vpv=16V, Ipv=1.8A

Chapter 8

8. Conclusions and future work

8.1 Conclusions

In this thesis we have focused on an optimum design of a small satellite power system which is flexible and scalable. Centralized power system control architecture was proposed for the satellite power system. The basic idea behind the architecture is to digitally control multiple power stages with a single high performance controller. A wide input synchronous buck-boost converter based flexible battery charging module (FBCM) was proposed which efficiently integrates the solar panels to the batteries. The FBCM is followed by a digitally programmable flexible point of load module which essentially provides the regulated DC bus for the satellite sub systems.

For the modeling aspect of the power system, a commercially available lithium based battery was modeled using EIS techniques. The battery model was included in the control loop of a buck and a boost power supply loop. The battery impedance changes with SOC of the battery and its effect on the control loop was observed. Based on the battery impedance based control loop performance, a dynamic compensation technique was proposed to optimally stabilize different control loops in the battery charging cycle. We have successfully verified the system model using a synchronous buck based charging system and a non synchronous boost based charger. A labview based user interface was also presented for the power modules to enable the user to re-program, optimize and design the power system.

8.2 Future Work

The FBCM has a wide operating voltage range but this work focused more on its operation during only its buck and boost mode. The work can be extended to the buck-boost mode too. The impedance of the battery is a function of temperature, SOC and the charge transfer current and hence for AC modeling a unified model of the battery is not yet know. The modeling aspect of this work can be extended to a good extent to make the AC EIS data of the batteries helpful for the AC modeling of the power supplies. Only the battery charging aspects of the system where discussed, battery fuel gauging and state of charge monitoring techniques were not explored. Also the health monitoring aspects of the power system needs to be explored.

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