ABSTRACT

KUMAR, MISHA. Control Implementations for High Bandwidth Shunt Active Filter. (Under the direction of Dr Subhashish Bhattacharya).

The presence of multiple harmonics in the power line due to various nonlinear consumer loads like adjustable speed drives, computers, etc incites the need for a high frequency active filter inverter so as to reduce the harmonic content at the point of common coupling (PCC) to be typically lower than 5% (for SCR<20) and 12%(for SCR=50-100) as specified by IEEE 519 harmonic standards. The objective of this thesis is to implement and compare three different active filter control techniques. These control techniques are based on Load Current, Supply Current and V_f (Voltage at Point of Common Coupling) harmonic extraction methods. Based on the analysis done in this work, it has been found that the V_f harmonic extraction method provides better compensation (THD=3.34%) as compared to the Load current (THD=3.82%) and Supply Current (THD=6.24%) harmonic extraction methods. A hardware board for harmonic extraction has also been built in the lab and its operation has been verified using three different types of nonlinear loads.

To provide the compensation for multiple harmonics in the power line, there is a need for the current controller which provides multiple frequency current tracking. Therefore, in this work, a Predictive current controller has been implemented on an analog board as a part of active filter control for providing current regulation. In the predictive current regulator, dead time compensation (3μsec) has also been performed in order to remove the effect of sampling and inverter dead time delay on PWM pulses and hence on the inverter output.

An Active Filter inverter has been driven in open loop using RL load at a switching frequency of 20 kHz by the six pulses from predictive current controller generating the compensating current. It has been verified that the compensating current exactly matches with the reference harmonic current.

For switching the active filter inverter at high frequencies for fast tracking of the reference current, there is a need to reduce the controller implementation delays. The Field Programmable Analog Array (FPAA) based analog controller has been used to implement a Synchronous Reference Frame (SRF)

controller algorithm for harmonic current extraction and the results are compared with the conventional digital implementation on Field Programmable Gate Array (FPGA). The FPAA based analog controller implementation(17.4μsec) proves to be faster than the digital FPGA implementation(30μsec) and can be a potential controller for SiC based active filter inverters with high switching frequencies of 50-100 kHz (10-20us).

Control Implementations for High Bandwidth Shunt Active Filter

by
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DEDICATION

To my parents and my brother.

BIOGRAPHY

Misha Kumar was born November 10,1987 in New Delhi, Delhi, India to Vineeta Kumar and Rakesh Kumar. She lived in New Delhi where she completed her high school from Hansraj Model School, Punjabi Bagh, New Delhi in May, 2005.She then pursued her undergraduate studies receiving Bachelor of Technology (Power-Electrical Engineering) from National Power Training Institute (Guru Gobind Singh Indraprastha University) in June, 2009.Since then she has been pursuing graduate studies at North Carolina State University, while working as a Teaching Assistant for Power Electronics course at North Carolina State University and Summer Research Assistant at FREEDM system center under the guidance of Dr Subhashish Bhattacharya. Her Primary research interests include Power Quality improvement, Power Electronics and Renewable Energy Systems.

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CHAPTER 1. INTRODUCTION

1.1 Background

With the advancement in Power Electronic technology, these days various consumer and industrial loads in the power system are nonlinear loads such as Adjustable Speed Drives with diode rectifier front end, Computers, Fax Machines, PLC's, High Power diode Rectifiers, Cycloconverters etc. These Nonlinear loads draw nonsinusoidal currents from utilities due to their operation thereby causing a poor power quality at the utility side. The harmonics are generated when nonlinear equipment draws current in short pulses. These harmonics in load current can sometimes result in overheated transformers, overheated neutrals, blown fuses ,tripped circuit breakers ,increased losses in the lines, decreased power factor, and can cause resonance with the capacitors connected in parallel with the system[2,3]. Harmonic distortion also causes inaccuracies in many devices which rely on the line voltage for timing.

1.1.a IEEE 519 Harmonic Standards

With the increased use of static power converter that require harmonic currents from power system, the Static Power Converter Committee of Industry Applications Society recognized the potential problem and started work on a standard that would give guidelines to users and engineer-architects in the applications of static power converter drives and other uses on electric power systems that contained capacitors. The result was IEEE 519-1981, *IEEE Guide for harmonic control and Reactive Compensation of Static Power converters [4]*. The IEEE 519 harmonic standard sets the limit on the Total Harmonic Distortion (THD) caused by the Non Linear Load at the Point of Common Coupling (PCC).Table I shows the harmonic current limits for Non Linear Loads at the Point of Common Coupling with other loads.

Table I: The Harmonic Current Limits for Non Linear Loads at the PCC [4]

Maximum Harmonic Current Distortion in % of Fundamental						
Harmonic Order (Odd Harmonics)						
I_{sc}/I_L*(SCR)*	<11	11⩽h⩽17	17⩽h⩽23	23⩽h⩽35	h⩽35	THD
<20	4	2	1.5	0.6	0.3	5
20-50	7	3.5	2.5	1	0.5	8
50-100	10	4.5	4	1.5	0.7	12
100-1000	12	5.5	5	2	1	15
>1000	15	7	6	2.5	1.4	20

Where I_{sc}=Maximum Short Circuit current at the Point of Common Coupling,

IL = Maximum Load current (Fundamental Frequency) at the Point of Common Coupling.

Table I suggests that the limitation on the harmonic current is based on the size of the consumer who is injecting the harmonic current and also on the size of the power system to which he is connected. If the size of consumer load is low with respect to power system, the larger is the percentage of harmonic current the consumer is allowed to inject into the power system.

1.1.b Control of Harmonics and their Impacts

Commonly employed solutions for harmonic problems are:

1. Modify the System Frequency response to avoid the adverse interaction with harmonic currents. This can be done by adding or removing capacitor banks, changing their sizes, adding shunt filters, inductors to detune the system away from harmful resonances.[5]
2. By employing shunt filters to remove harmonic currents from the system. Two types of Filter can be used for this:

a. Passive Filters: A Passive filter consists of a Series/Parallel combination of an inductor, a capacitor and a resistor specially tuned to filter a particular frequency current. The impedance of L-C tuned filter is lower than the source impedance at a particular harmonic frequency in order to absorb that harmonic current. Passive filter have an advantage of low cost, are less complicated and have high efficiency. However, they suffer from a serious limitation that their performance gets affected significantly due to the variation in the filter component values, filter component tolerance, source impedance, and frequency of ac source [6, 8]. Also, they may cause series and load resonances in the system. In this scenario, harmonic currents can get amplified on the source side and cause serious distortion in the voltage[6].The passive filters also tend to get overloaded in case the load harmonics increase[8]. A stiff utility system poses greater difficulty for design of passive filter because sharp tuning and high quality factor are required to sink harmonic current [7]. A typical passive filter tuned for 5^{th} and 7^{th} harmonic applied to power system is as shown in figure1.

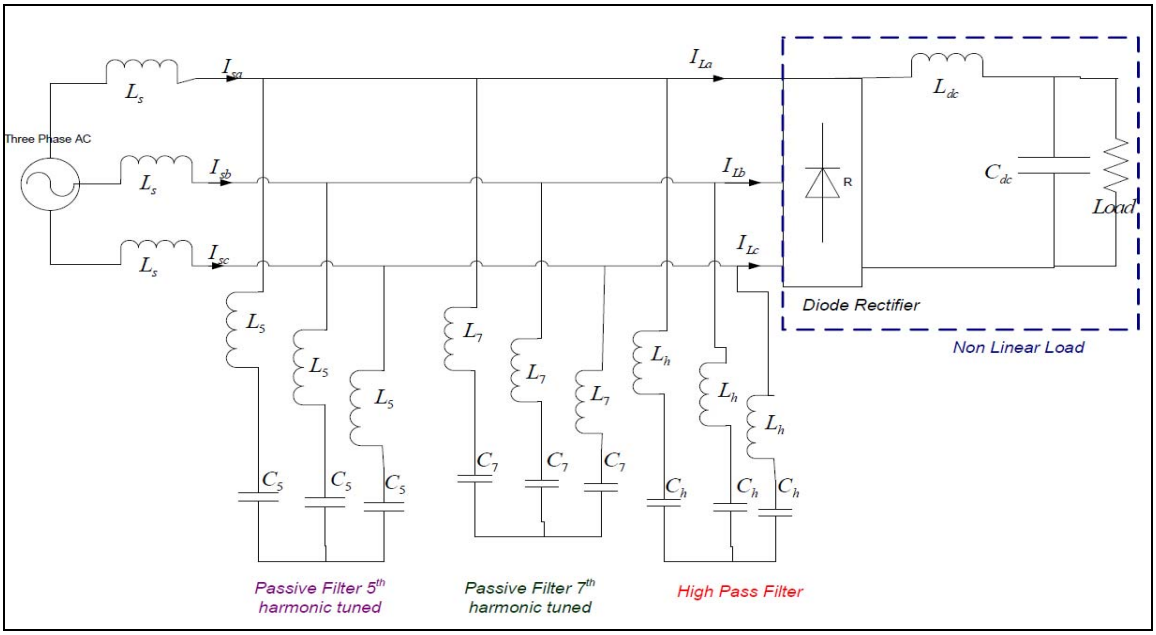

Figure 1.A Passive Filter System

b. Active Filter: An Active Filter involves the use of one or more active components such as a Voltage Source Inverter which can be controlled in such a way so as to provide the compensating current or voltage to the nonlinear load. In this way, the nonlinear load does not draw the nonsinusoidal components from the source and thus the source becomes free of harmonics. Figure 2 shows a shunt active filter system used for providing the harmonic compensation so as to meet IEEE 519 Standard at the point of common coupling.

The concept of shunt active filtering was first introduced by Gyugyi and Strycula in 1976[10].Since then several Active Filter topologies have been proposed, some of them are:

i) Shunt Active Filters

ii) Series Active Filters

iii) Hybrid Parallel Active Filters

These topologies have been discussed in detail in the following chapters.

Major Advantage of Active Filter over Passive Filter is that it can be controlled to compensate for harmonics in such a way that THD lower than 5% at the Point of Common Coupling can effectively be achieved. The shunt Active Filter can also be made to act as a damping device in a parallel resonance circuit formed by the passive filter and the power supply system by adopting a lead function in its controller [9].Thus it can prevent harmonic propagation resulting from harmonic resonances. Briefly, Active Filters can be designed to achieve following three goals:

- Harmonic Compensation
- Harmonic Damping
- Harmonic Isolation

1.2 Thesis Objective

The main objective of this thesis is to develop a controller for 5 KVA Shunt Active Filter system. The shunt active filter system consists of a 5KVA Active Filter inverter, a harmonic extractor and a current regulator. The harmonic extractor is implemented using three different algorithms for harmonic current extraction for comparison. These are based on Load current, Supply current and Vf (Voltage at the Point of Common Coupling) harmonic extraction.

The current regulator is implemented using predictive current control method.

An Active filter inverter is required to be switched at higher switching frequencies (50-100Khz) so as to reduce the harmonic content at the point of common coupling to be typically lower than 5% as specified by IEEE 519 harmonic standard. An attempt has been made in this thesis to implement the harmonic extraction algorithm on an Analog Board, by using Field Programmable Analog Array (FPAA) and Field Programmable Gate Array (FPGA) and then comparing the delays in the implementation on each of them. Various advantages and disadvantages of each of the methods are also analyzed.

1.3 Outline

Chapter 2 gives a review of different active filter topologies like shunt active filter, series active filter, hybrid parallel active filter. All of these topologies are compared with each other based on the type of loads they can be applied for, required active filter rating and their control technique.

Chapter 3 discusses about three different types of harmonic extraction methods and their comparison based on their application and their performance to reduce Total Harmonic Distortion (THD).This chapter also covers the predictive current control technique and its implementation issues. Three harmonic extraction methods running in closed loop have been presented along with their simulation results.

Chapter 4 discusses the implementation of Synchronous Reference Frame Controller using Field Programmable Analog Array (FPAA) and Field Programmable Gate Array(FPGA). It has been found that FPAA provide lower implementation delay as compared to FPGA and hence can prove a potential method for driving SiC based inverters at higher switching frequencies.

Chapter 5 discusses the hardware implementation of Shunt Active Filter System. Three types of loads have been used to validate the three harmonic extraction methods. This chapter also includes the experimental results from the predictive current controller board which receives its reference signal from the harmonic extraction board.

Chapter 6 gives the summary and the conclusion of the whole thesis work.

1.4 Glossary of Terms

- PCC-Point of Common Coupling
- THD-Total Harmonic Distortion
- FPAA-Field Programmable Analog Array
- FPGA-Field Programmable Gate Array
- SRF-Synchronous Reference Frame
- VSI-Voltage Source Inverter
- PWM-Pulse Width Modulation
- LPF-Low Pass Filter
- HPF-High Pass Filter
- IRP-Instantaneous Reactive Power
- S/H-Sample and Hold

CHAPTER 2. ACTIVE FILTERS

2.1 Review of Active Filter Topologies

2.1.a Shunt Active Filter

A Shunt Active Filter consists of a controlled Voltage Source Inverter (VSI) connected in parallel to the nonlinear load. A Shunt Active Filter compensates for the harmonic current required by the load so that the load only draws a fundamental current from the grid.

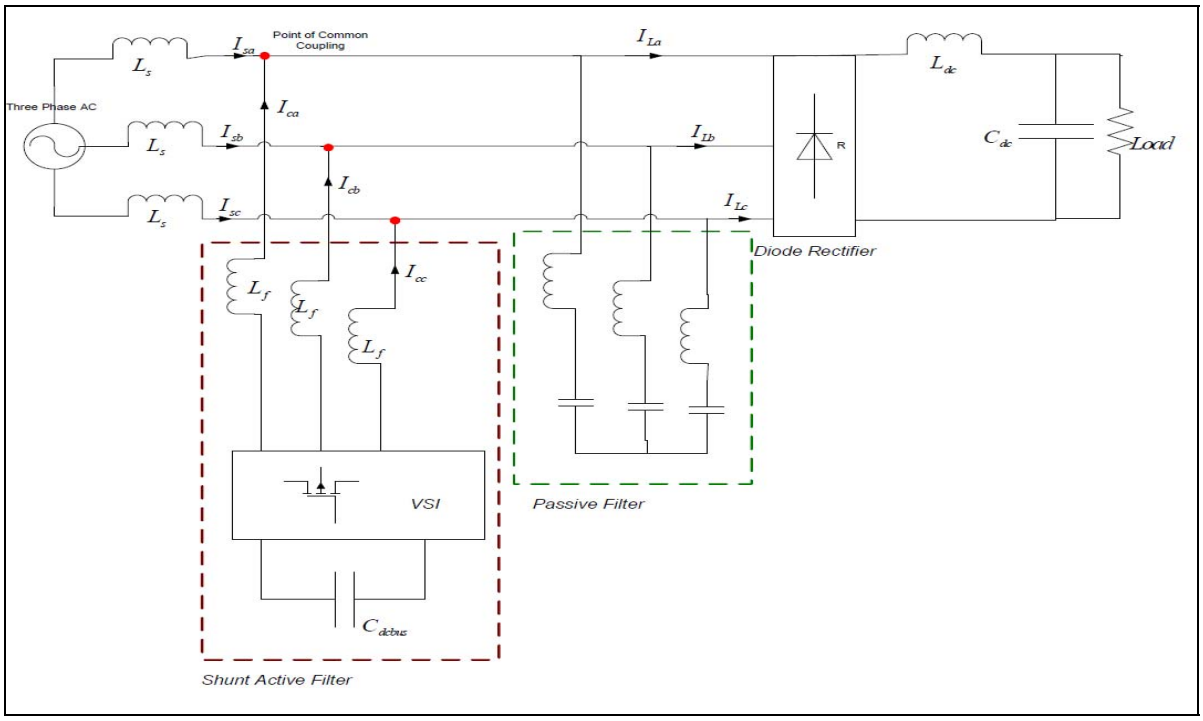

Figure 2.A Shunt Active Filter System

Therefore, for a Shunt Active Filter, according to the Kirchhoff's current law at PCC, we can write the following equation:

$$I_s + I_c = I_L \tag{1}$$

Where I_s is the supply current, I_c is the compensation current and I_L is the load current as shown in Figure 2.The Load current, I_L, is comprised of a fundamental component, I_f, and the harmonic

component, I_h .If the harmonic component is made equal to the compensation current, I_c ,then only the fundamental current required by the load will come from the supply.

The compensating current is supplied by the Active Filter Inverter which has a DC link capacitor. The capacitor voltage is held constant with the help of fundamental current from the grid.

In a practical implementation, a shunt active filter is always installed in parallel with a passive filter. The shunt passive filter, as shown in Figure 2, helps to absorb higher order harmonics and switching ripple. This helps the active filter to function with relatively smaller capacity [9].

A Shunt Active Filter Controller, whose design is discussed in detail in the following chapter, comprises of:

- Harmonic Extractor-A Harmonic Extractor is required to generate a reference for the compensation current. A Harmonic Extractor tells us what harmonics we need to compensate for.
- Current Regulator-A Current regulator compares the measured compensation current with the reference and produces the desired pulses for the Active Filter Inverter.

A Shunt Active Filter is suited for inductive or current source type load such as thyristor rectifier. If a Shunt Active Filter is used for voltage source type load then the injected current may be diverted to load causing its overloading [13].

2.1.b Series Active Filter

A series Active filter compensates for the voltage harmonics required at the load terminals due to the nature of nonlinear load. Therefore, the voltage at the source terminals becomes free of harmonics and supplies only the fundamental current required by the load. Figure 3 shows a series active filter system.

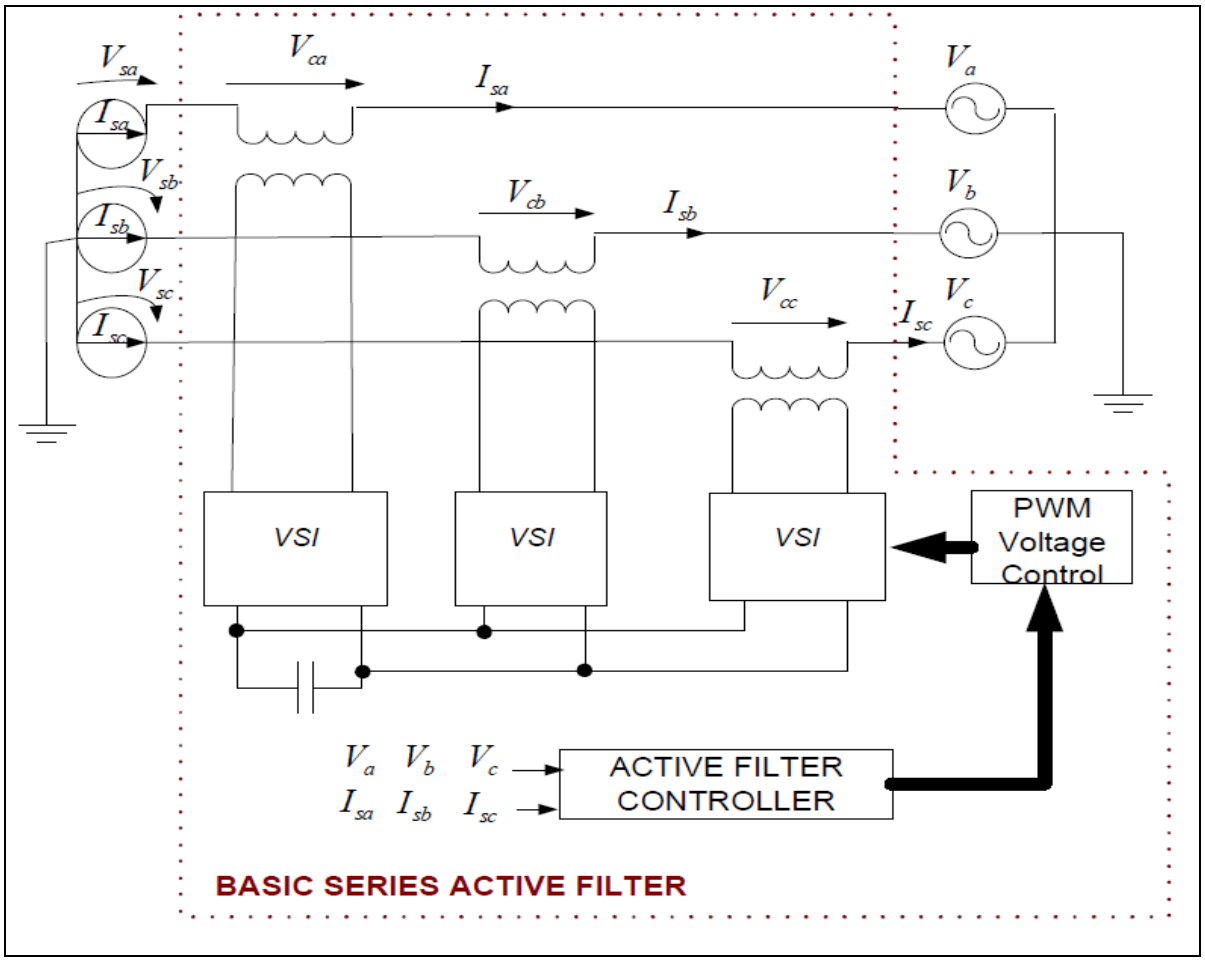

Figure 3. Series Active Filter System [10]

The voltages on the current sources are $V_{sa,}$ $V_{sb,}$ V_{sc}. The relation between the source voltage, the load voltage and the active filter voltage is given by:

$$\begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} = \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} - \begin{bmatrix} V_{ca} \\ V_{cb} \\ V_{cc} \end{bmatrix} \tag{2}$$

The basic series active filter voltages are synthesized by three single phase converters with a common dc capacitor. The reference voltage for these converters is calculated by the "active filter controller" which has input signals as load voltages and currents using dual p-q theory (as mentioned in [10]).

A Series Active Filter is suitable only for Capacitive or Voltage source type load such as condenser input type diode rectifier capacitive load [13].In case of series active filter, it is required to install a low impedance equipment such as LC filter or shunt condenser in parallel to the load is the load is of current source type or inductive [13].

2.1.c Hybrid Parallel Active Filter

Hybrid parallel active has an active filter in series with a particular frequency harmonic tuned passive filter .The main advantage of this Hybrid filter is that it reduces the VA rating of the active filter that needs to be installed in series with the passive filter. A practical active filter should have a VA rating lower than 5% of the load VA rating [11]. Hybrid Active filters improve compensation characteristics of the passive filters, making possible reduction in the active filter rating [11].This is done by making the active filter controller to implement a dynamically varying-either negative or positive 'active inductance'. The controller produces the reference active filter inverter voltage which is then compared with the sine triangle to generate desired PWM pulses. The 'active inductor' inverter reference voltage, V_{Lcmdn} is given by [12]:

$$V_{Lcmdn} = L_{cmdn} \left. \frac{di_{inv}}{dt} \right|_{n^{th} harmonic} \tag{3}$$

Where L_{cmdn} is the positive or negative 'active inductance' to be synthesized at n^{th} harmonic frequency. It is the inductance which tunes L_n-C_n passive filter at n^{th} harmonic frequency. Figure 4 shows the Parallel hybrid active filter diagram.

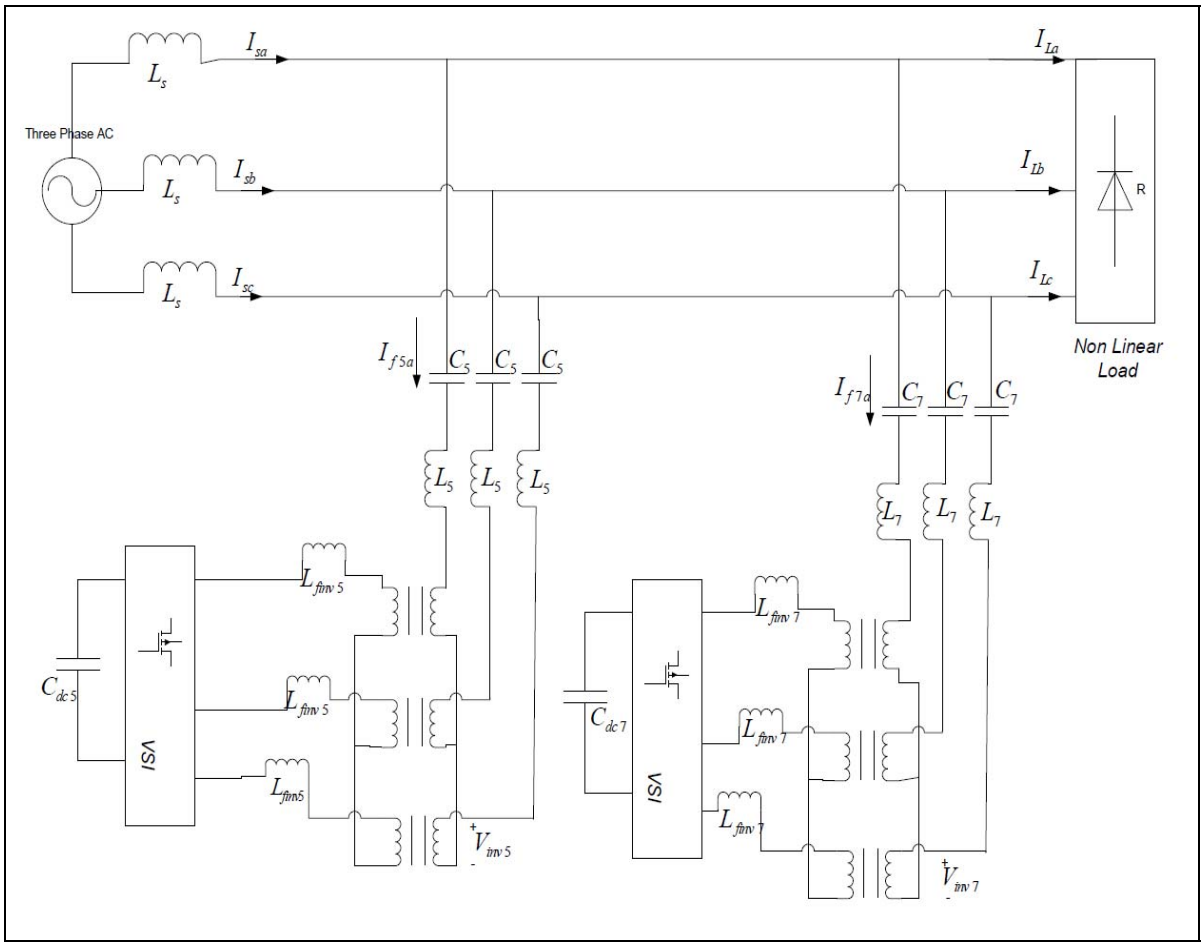

Figure 4.Hybrid Parallel Active Filter System

The desired value of L_{cmdn} is determined by taking an error between the measured value of the n^{th} frequency component of filter current, i_{fn}, and its reference i_{fn}* and passing it through a PI controller[as mentioned in [12].

The variable inductance controller based parallel hybrid active filter system with fifth and seventh passive filters can effectively provide harmonic compensation of the load and can be made to prevent passive filter overloading by 'current limiting' in presence of ambient harmonic loads and supply voltage harmonics[12]**.**

CHAPTER 3.SHUNT ACTIVE FILTER CONTROLLER

The Active Filter controller consists of a harmonic extractor and a current regulator. In this chapter different methods of harmonic extraction have been discussed. Each method has its own advantages and is application based. Predictive current control technique has also been discussed in this chapter along with its implementation issues and the dead time compensation.

3.1 Harmonic Extraction

The harmonic extraction involves the process of determining all the multiple frequency components present in the current or voltage. The harmonics thus extracted become the reference for the current regulator. The current regulator thus produces pulses in order to drive the active filter inverter in such a way so as to generate the compensating current which is same as the reference.

The most common method used for harmonic extraction is Synchronous Reference (SRF) Frame method.

3.1.a Synchronous Reference Frame Harmonic Extraction

The Synchronous Reference Frame harmonic extraction method involves park transformation to convert three phase current or voltages into synchronously rotating d-q reference frame. The Park Transformation can be performed as follows:

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \frac{2}{3}\begin{bmatrix} Cos\theta & Cos(\theta - \frac{2\Pi}{3}) & Cos(\theta + \frac{2\Pi}{3}) \\ Sin\theta & Sin(\theta - \frac{2\Pi}{3}) & Sin(\theta + \frac{2\Pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (4)$$

The motivation of changing to synchronous reference frame is that in synchronous reference frame the fundamental component becomes a constant which can then be low pass filtered to leave behind the high frequency components which can easily be extracted. Also, Low pass filtering of a DC

component does not cause any phase error in the signal which might be an issue if a High Pass filter was used [14].

The Synchronous Reference Frame method of harmonic extraction can further be applied for load current, supply current and Vf (Voltage at PCC) harmonic extraction. All of these methods have been represented in the form of block diagram in Figure 5.

Load Current Harmonic Extraction-Load current Harmonic Extraction method as shown in Figure 5 is the most straightforward method. The harmonics extracted from the load current are provided as the reference to the current regulator which drives the inverter to compensate for these harmonics. In this way, load current harmonics are supplied by the active filter inverter and the fundamental current comes from the source. In this method, the load current is first converted from three phase to the d-q synchronous reference frame. The d-q components so obtained are low pass filtered to obtain the DC component (or the fundamental component in three phase system).This is then subtracted from the original d-q components to perform 1-LPF (or HPF) operation to obtain the high frequency components. Inverse park transformation is then performed to obtain three phase harmonic signals [14].

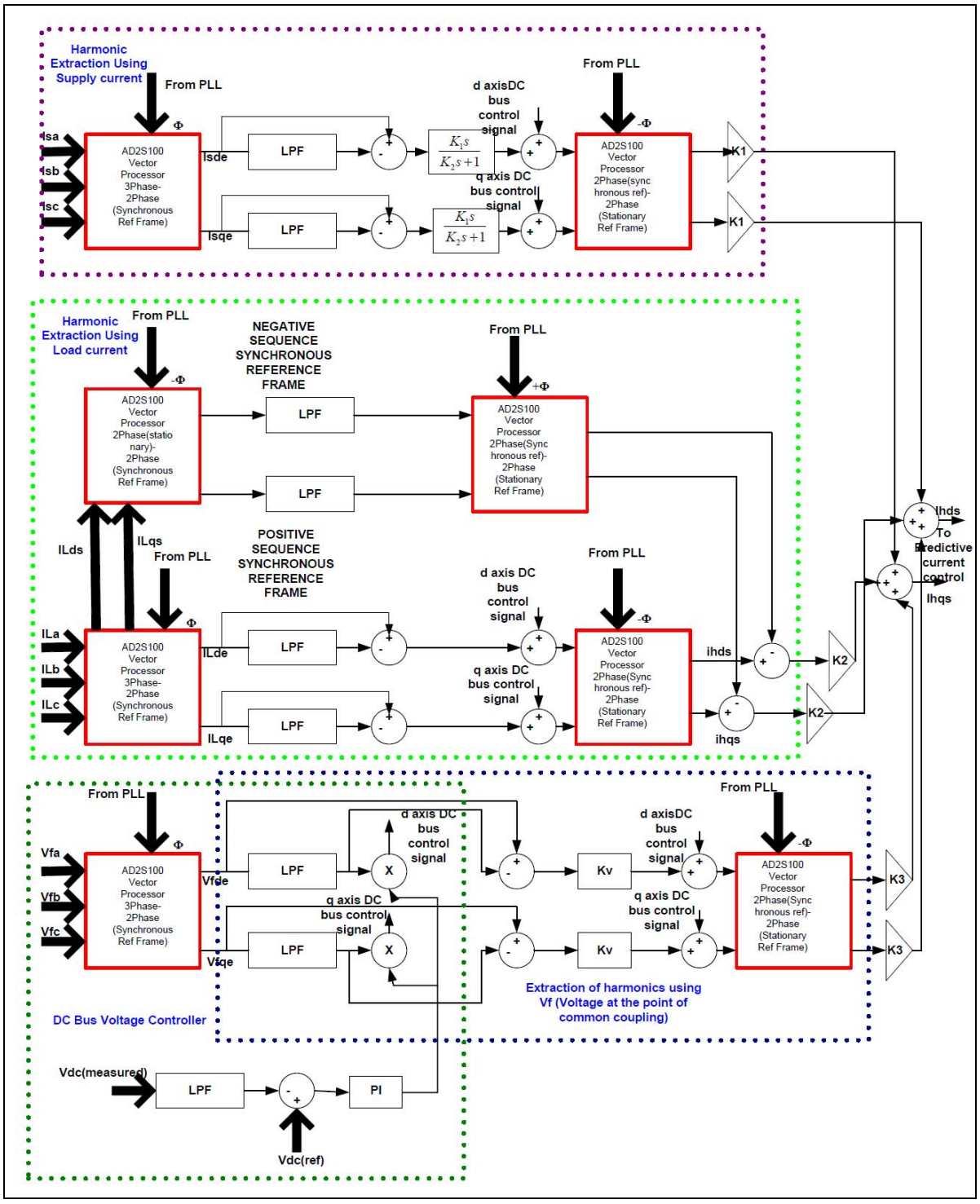

Figure 5.Block Diagram representation of Supply Current, Load Current and V_f harmonic extraction method

The Load current harmonic extraction method is the feedforward method of compensation. In a load current harmonic extraction method, the THD cannot be improved beyond a certain extent as there is no controller gain which can be varied to improve the THD.

Supply Current Harmonic Extraction- Figure 6 shows the equivalent circuit of an active filter. The three phase supply side currents are first converted from three phase to d-q components in synchronous reference frame. They are then High Pass Filtered as discussed above to obtain high frequency components. As derived in [9],

$$I_c = G(s) * I_{sh} \quad (5)$$

Where I_c=Compensating Current, I_{sh}=Harmonics present in Supply Current, G(s)=Active Filter Control Function.

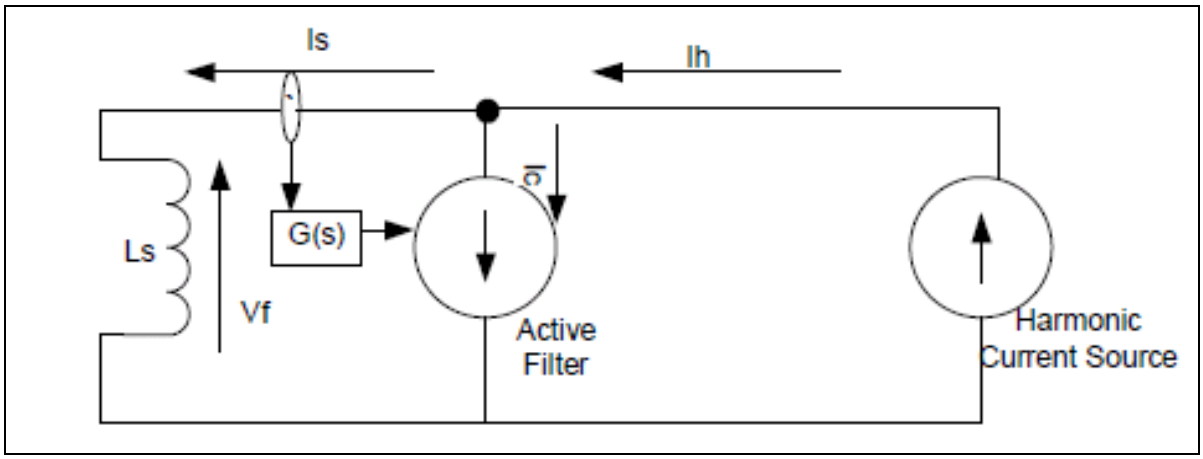

Figure 6.Harmonic Equivalent Circuit of Active Filter

As mentioned in[9],a good absorption of harmonic currents as well as suppression of amplification of harmonic currents due to the anti-parallel resonance are obtained if active filter controller has a lead plus proportional characteristics.

$$G(s) = \frac{(KT)s}{(T)s+1} \tag{6}$$

$$I_c = \frac{(KT)s}{(T)s+1} * I_{sh} \tag{7}$$

Also, $$V_f = s(L_s) * I_{sh} \tag{8}$$

Substituting (8) in (7),we get

$$I_c = \frac{1}{\frac{L_s}{KT} + \frac{L_s}{K}s} * V \tag{9}$$

Where L_s= Supply Side Inductance, T=Time constant of Lead Function, K=Gain Constant of Active Filter Control Function, s=Laplacian Operator

Equation (9) shows that an active filter behaves as a series circuit of a resistance of L_s/KT and an inductor with inductance of L_s/K equivalently. Figure 7 shows the lead plus proportional characteristics of an active filter controller. This figure helps us to choose the value of K=5.

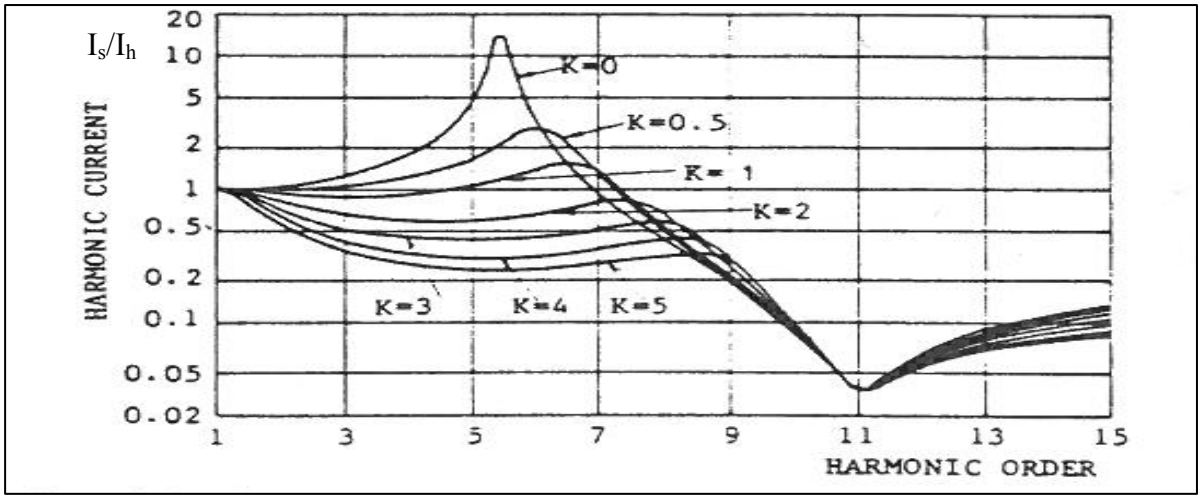

Figure 7.Lead plus Proportional Characteristic of Active Filter Controller (Reproduced from [9])

The supply current harmonic extraction method is a feedback method of compensation and implements a gain which can be varied to improve the THD. The supply current harmonic extraction method provides the source to load harmonic isolation.

V_f Harmonic Extraction Method-Harmonic propagation is a serious phenomenon in power distribution systems. This occurs due to the harmonic resonance between line inductors and capacitors which are installed for power factor correction. Also, it has been pointed out by actual measurements that fifth harmonic voltage at the end bus is magnified by 3.5 times as large as that at the beginning bus in a 6.6kV, 17 km long power distribution feeder having capacitors with a total capacity of 245kVA [10].Therefore, installing active filter on the last bus makes it possible for active filter to damp out harmonic propagation [10]. In the Vf harmonic extraction method, G(s) =(KT)s. This provides lead characteristics to the active filter controller [9]. Thus,

$$I_c=(KT)s*I_{sh} \tag{10}$$

Substituting (8) in (10), we get

$$I_c = \frac{V_f}{\frac{L_s}{KT}} = K_v * V_f \tag{11}$$

Equation (11) means that active filter acts as a pure resistor of L_s/KT. In this way, an active filter can be made to act as a harmonic damper by providing low impedance path to the harmonic frequencies. V_f method also provides the harmonic isolation between the source and the load. V_f method is the feedback method of harmonic compensation. It has a gain K_v which can be varied to improve the compensation and make the harmonic voltage at the PCC to go to zero. The limitation of the V_f method comes into picture when the supply voltage contains the harmonics. In this case the V_f harmonic extraction method cannot provide the harmonic compensation for the supply voltage

harmonics. Also, by making the harmonics at the point of common coupling zero, the V_f method causes harmonic current to flow from source to the load.

P-Q Theory (IRP Theory) Method-The P-Q Theory or Instantaneous Reactive Power Theory was first introduced in 1983 by Akagi, et al. In this method, A shunt active filter controller senses the three phase voltage at the point of common coupling ;V_{fa}, V_{fb}, V_{fc} and the three phase load currents; i_{La}, i_{Lb}, $i_{Lc.}$ P-Q Theory first transforms sensed three phase voltages and currents into two phase orthogonal axes, αβ system according to the following equations.

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \frac{2}{3}\begin{pmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{pmatrix}\begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \tag{12}$$

$$\begin{bmatrix} V_{f\alpha} \\ V_{f\beta} \end{bmatrix} = \frac{2}{3}\begin{pmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{pmatrix}\begin{bmatrix} V_{fa} \\ V_{fb} \\ V_{fc} \end{bmatrix} \tag{13}$$

P-Q theory is based on the instantaneous power calculation in αβ coordinate system [10]. The instantaneous power is further divided into instantaneous real power, P and instantaneous imaginary power, Q. Both of these can be further divided into their ac and dc components as follows:

$$P = P_{ac} + P_{dc} \tag{14}$$

$$Q = Q_{ac} + Q_{dc} \tag{15}$$

P_{dc} and Q_{dc} are referred to as the average components of real and imaginary powers and generally represent the active and the reactive power consumed by the load respectively. P_{ac} and Q_{ac} represent the oscillating components of real and imaginary power (explained in [10]) which are produced

because of the presence of harmonics in the system. They represent an additional power flow in the system without effective contribution to the energy transfer from source to load or from load to source [10]. The instantaneous value of P,Q can therefore be calculated as follows[10],[15]:

$$\begin{bmatrix} P \\ Q \end{bmatrix} = \begin{pmatrix} V_{f\alpha} & V_{f\beta} \\ -V_{f\beta} & V_{f\alpha} \end{pmatrix} \begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \end{bmatrix} \tag{16}$$

$$\begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \end{bmatrix} = \frac{1}{V_{f\alpha}^2 + V_{f\beta}^2} \begin{pmatrix} V_{f\alpha} & V_{f\beta} \\ V_{f\beta} & -V_{f\alpha} \end{pmatrix} \begin{bmatrix} P \\ Q \end{bmatrix} \tag{17}$$

Similarly, we get [from 15]:

$$\begin{bmatrix} i_{c\alpha} \\ i_{c\beta} \end{bmatrix} = \frac{1}{V_{f\alpha}^2 + V_{f\beta}^2} \begin{pmatrix} V_{f\alpha} & V_{f\beta} \\ V_{f\beta} & -V_{f\alpha} \end{pmatrix} \begin{bmatrix} P_c \\ Q_c \end{bmatrix} \tag{18}$$

Where P_c and Q_c are the instantaneous real and reactive power consumed by the compensator (the active filter inverter). For the compensator to act as purely a harmonic compensator $P_c = -P_{ac}$, $Q_c = -Q_{ac}$. It is found for the system having diode rectifier front ends that Pac ≈ 0[15].Thus, the equation for the harmonic compensator becomes:

$$\begin{bmatrix} i_{c\alpha} \\ i_{c\beta} \end{bmatrix} = \frac{1}{V_{f\alpha}^2 + V_{f\beta}^2} \begin{pmatrix} V_{f\alpha} & V_{f\beta} \\ V_{f\beta} & -V_{f\alpha} \end{pmatrix} \begin{bmatrix} 0 \\ -Q_c \end{bmatrix} \tag{19}$$

Where $i_{c\alpha}$,$i_{c\beta}$ are the α-β components of the compensating current.

3.2 DC Bus Voltage Control

The Block Diagram representation DC Bus Voltage controller implemented for an active filter inverter is shown in Figure 5.The DC bus voltage is measured and its error with the reference DC bus voltage is passed through a PI controller to get the desired current command. This current command is then multiplied with the fundamental component of the Voltage at PCC, V_f. This is done in order to ensure that the DC Bus gets charged through the real power. The fundamental current command is then added to the extracted harmonic current in d-q synchronous reference frame in order to get the

reference compensating current, I_c*.The measured DC bus voltage has to be low pass filtered to attenuate ac components present in V_{dc}. The dominant components of DC Bus voltage are at multiples of 360 Hz. These are present on the DC side because of the presence of 5^{th} and 7^{th} harmonic components on the ac side of the inverter [14]. If these harmonics in V_{dc} are not attenuated, they might generate harmonic reference in order to eliminate these harmonics from V_{dc} and in the process they will affect the actual harmonic reference current. Further, in the presence of supply voltage distortion active filter terminal voltage harmonics will interact with the DC bus voltage controller generated reference harmonic currents. This will result in a real power transfer between supply and dc bus. Thus, filtering ensures that the power transfer between the supply and dc bus only takes place at the fundamental frequencies [14].

3.3 Current Controller

3.3.a Predictive Current Controller with charge error control

Predictive Current controller with charge error control has been used for non-sinusoidal current tracking. The Current controller should be designed for a multiple frequency current tracking as opposed to a single frequency current tracking as may be in the case of motor drives. It should have an ability to operate with lower active filter inductance, L_f. A lower value of L_f allows better di/dt tracking and higher current bandwidth. It should have lower sensitivity to L_f and V_f estimation error. It should provide a simple and a cost effective implementation in analog domain [20].

In case of multiple frequency current tracking, the higher order harmonics incur a significant phase delay over half a switching period for a typical 20 kHz switching frequency. In other words, the higher frequency reference changes significantly over half a switching period. In addition to this, sample and hold delays and the inverter dead time delays represent a significant percent of the switching period and therefore result in even large percentage changes in high frequency reference current [20].

A predictive current controller has been proposed in [14] to address these issues. While designing predictive current controller, it has been assumed that the reference current remains constant over the complete switching period. Also, to eliminate low frequency errors, high frequency averaging has been performed per switching period such that the charge error over one switching period is equal to zero.

It has been shown that by using Space Vector PWM method, this high frequency averaging can be applied. In this method, the active space vectors are centered and hence the zero vectors are implicitly defined. This placement of the space vector minimizes the harmonics per switching period [14].

The schematic diagram of the implementation of predictive current control in analog domain has been shown in Figure 8.As can be seen from this figure, the predictive current controller with charge error control has been implemented in Stationary reference frame (or d^s-q^s frame).This achieves decoupling of phases and alleviates the concerns of phase interactions and limit cycles in the active filter current, i_f. Decoupling of phases also ensures predictable peak to peak current ripple for a given dc bus voltage, V_{dcbus}, active filter terminal voltage ,V_f, and filter inductor, L_f [14].

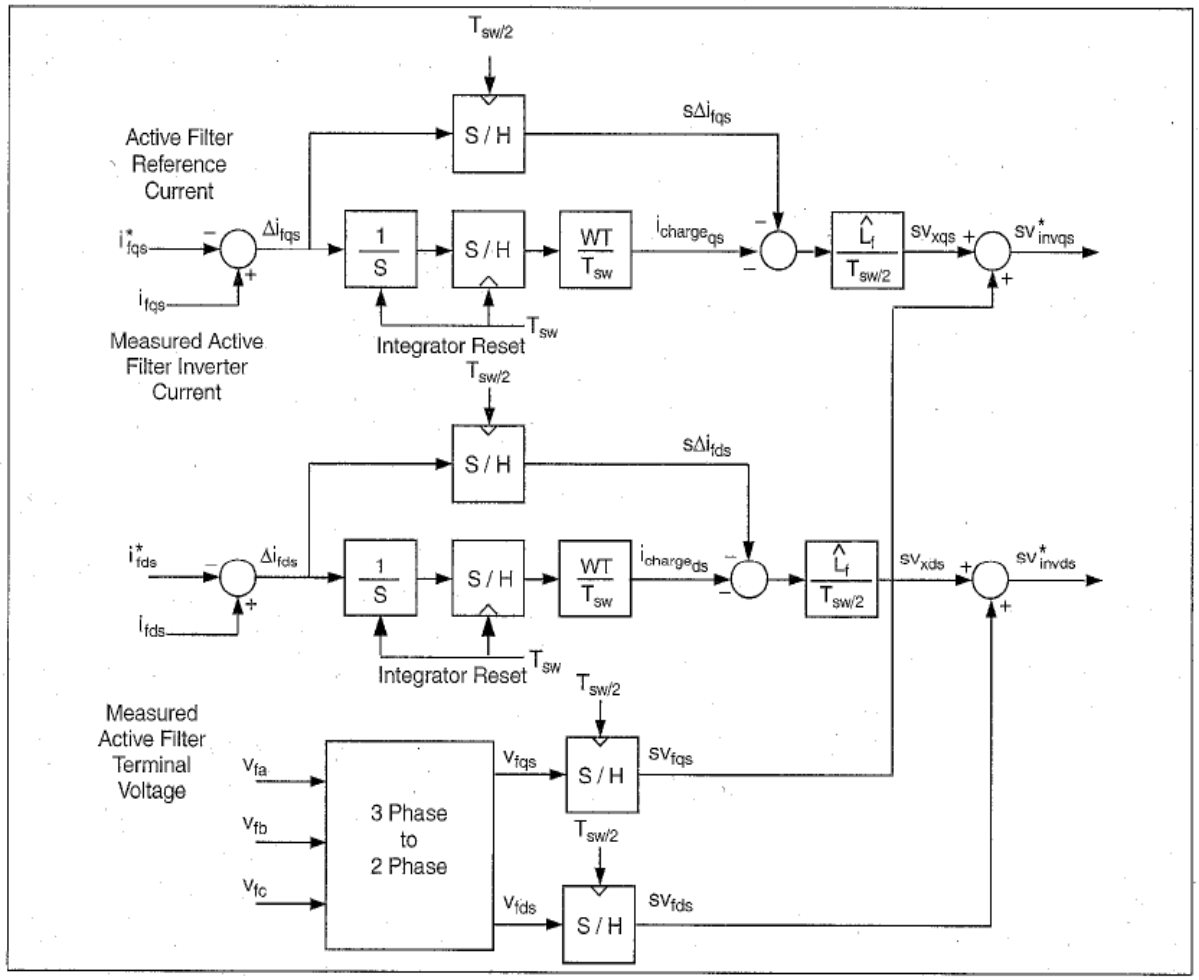

Figure 8.Predictive Current Controller with charge error control (Reproduced from [14])

The equations that describe current controller operation are:

$$\Delta i_{fqs} = i_{fqs} - i^*_{fqs} \tag{20}$$

$$\Delta i_{fds} = i_{fds} - i^*_{fds} \tag{21}$$

$$V_{xqds} = -\frac{L_f}{\frac{T_{sw}}{2}}(\Delta i_{fqds} + \frac{WT}{T_{sw}}\int_0^{T_{sw}} \Delta i_{fqds}\, dt) \tag{22}$$

$$V^*_{invqds} = V_{xqds} + V_{fqds} \tag{23}$$

Where, i_{fqs} and i^*_{fqs} are the q components of active filter compensating current and its reference current respectively; V^*_{invqds} is the reference inverter voltage in stationary reference frame; V_{fqds} is the active filter terminal voltage(or the voltage at PCC) in stationary reference frame. As can be seen from Figure 8, the inverter reference voltage is produced by the sum of two parallel paths. In the first path the current error, ΔI_{fqds}, is sampled every half switching period to improve tracking of higher order harmonic current due to their reference change within one switching period. This sampled current is then multiplied by $L_f/(T_{sw}/2)$ and then added to the back emf V_{fqds} to generate the reference active filter inverter voltage as in a conventional predictive current controller.

In the second parallel path, the integral of the current error or the charge error is determined and reset every switching period T_{sw}. This is achieved by an integrator reset and a sample and hold circuit. If an integrator is allowed to run free, it might accumulate low frequency errors and may cause integrator saturation problems. The weighting factor or WT as shown in the figure is to make the high frequency current averaging over a window greater or lesser than one switching period. A WT=2 means the current averaging over half a switching period [20].

The charge error is converted back to an equivalent $\Delta i_{chargeqds}$ by dividing it by T_{sw}. This is then added to the sampled value of Δi_{fqds} and their sum is multiplied by $L_f/(T_{sw}/2)$ to produce the reference voltage across the inductor L_f. This is then added to the back emf V_{fdqs} to produce the inverter reference voltage, V^*_{invqds} [20].

3.3.b Space Vector PWM and its implementation in Analog Domain

The Space Vector PWM generation method is a method in which the reference voltage which is mapped in stationary α-β reference frame is decomposed in the form of voltage switching vectors which are realizable on the 6 pulse inverter [15]. A space vector PWM method computes the duty cycle of the switching state vectors which are in proximity to the reference voltage. Choosing the

consecutive switching vectors in proximity to the reference helps to reduce the number of switching operations required and thereby helps in the reduction of switching losses. The space vector PWM generation method is regarded as the "superior" PWM generation technique [15] as compared to Sine-PWM technique which is implemented by comparison of reference with a sine triangle. Figure 9 shows the block diagram of the analog implementation of the space vector PWM technique.

It has been shown that on injecting triplens to the reference waveform and then comparing it with the triangular waveform produces the same switching pattern as is does by space vector PWM technique. Therefore, the inverter reference voltage in stationary α-β reference frame is transformed into the three phase inverter reference voltages; $V^*_{invan}, V^*_{invbn}, V^*_{invcn}$ .The extraction of triplens is achieved by passing three phase inverter reference voltages through a diode bridge circuit. This circuit extracts the maximum of the three during positive cycle and minimum of the three during negative cycle thereby resulting in the triplen extraction. The triplens are then added to the reference voltages. This resulting space vector modulating waveform; V_{moda}, V_{modb}, V_{modc} is regularly sampled and synchronized to the peak of the triangular waveform. This is then compared with the carrier triangular waveform to produce the desired space vector PWM pulses.

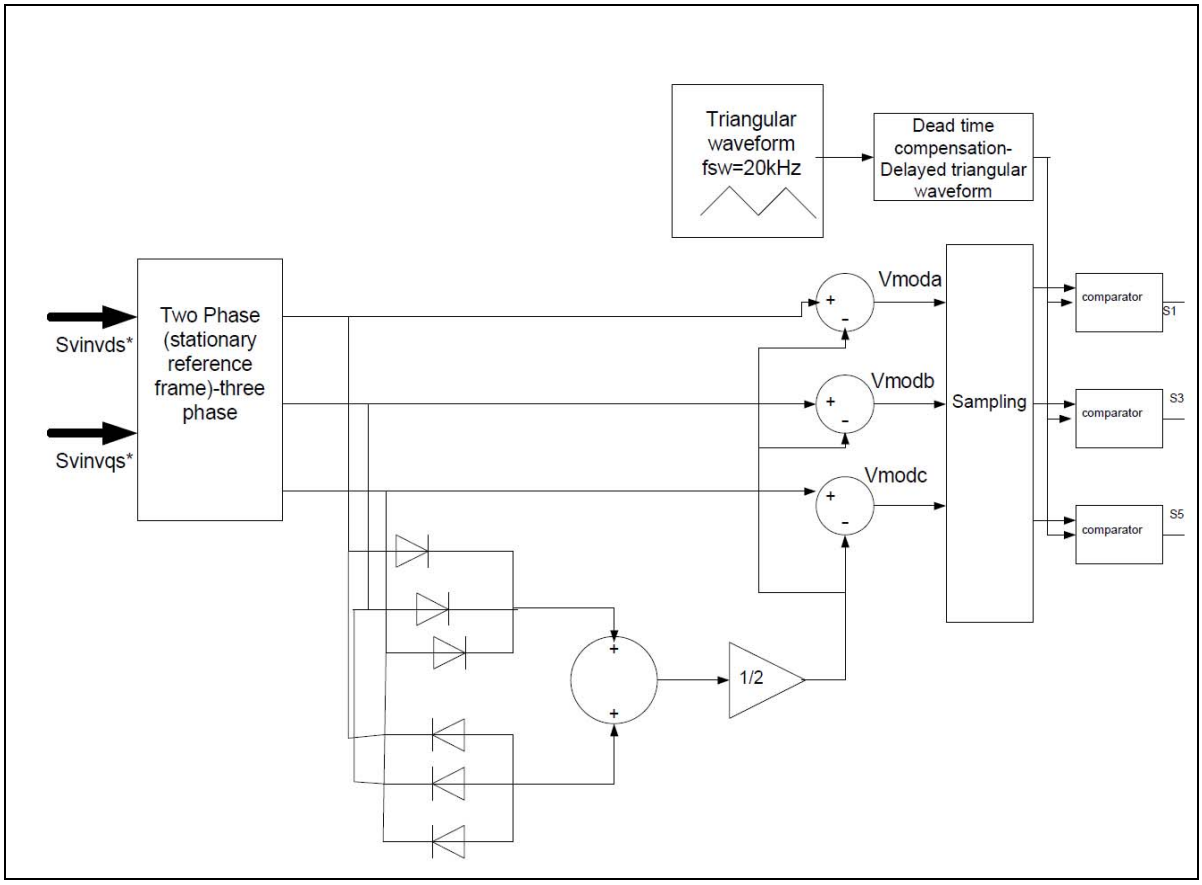

Figure 9. Block diagram of the Analog Implementation of the Space Vector PWM Technique

3.3.c Implementation issues and Dead Time Compensation

In a parallel active filter system, considering the switching frequency of 20kHz, there is an implementation delay typically of around 3µsec of which sample and hold causes a delay of around 1.5µsec and rest is caused by inverter dead time of 1.5µsec.This delay is quite significant since it constitutes 10-15% of the 50µsec (20kHz) switching period[20]. If this delay is not compensated for, it might cause wrong PWM signals to be produced or PWM signals might be shifted in time which can affect the harmonic compensation. Therefore, the dead time compensation technique is adopted in which the triangular carrier waveform is delayed by t_{delay}=Sampling delay+ Inverter dead time with

respect to the sampling pulse, such that both the sampling and the switching take place at the same instant. This method has been implemented in this work.

The other method for the dead time compensation is the feed forward method in which the compensation is provided by adding/subtracting the feed forward voltage depending upon the sign of the measured inverter current [20].

3.4 Bandwidth of Active Filter Inverter

The bandwidth of an active filter inverter is the range of frequencies which an inverter can produce at its terminals. It is decided by the frequency at which the inverter is switched and the inverter DC bus voltage. An active filter is required to compensate for multiple harmonics to achieve a THD which is typically lower than 5% (for SCR<20).Not only this, the remnant high frequency/high slew rate component in the supply current which is present even after compensation can lead to a very high voltage induced across the inductor. Therefore, in order to compensate for these higher order harmonics, there is a need to switch active filter inverters at a very high frequency. In this work, the switching frequency, f_{sw}=20Khz.

3.5 Active Filter System Specifications

The Active Filter System Specifications taken for the purpose of designing the Simulink Model are:

V_s= Line to Line Supply Voltage = 460 V rms

L_s= Supply Side Inductance=22µH

L_{dc}=DC Load side inductance =340µH

C_{dc}=DC Load side Capacitance=30mF

L_f=Filter Inductance=75µH

C_{dcbus}=DC Bus Capacitance=12.5mF

$V_{dcbus(ref)}$=Reference DC Bus Voltage =650-750V

Parallel Passive Filter Specifications (for20khz switching frequency) (taken from [14])

Parallel Passive Filter circuit used in the simulation is as shown in Figure 10.

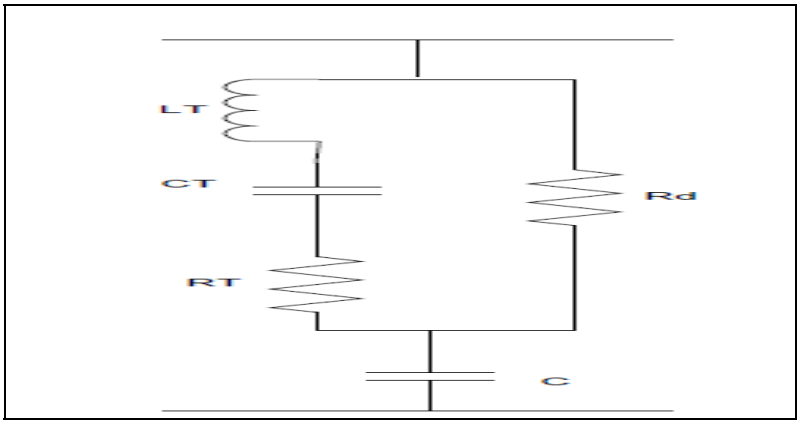

Figure 10.Parallel Passive Filter system used in Simulation

L_T=21µH

C_T=3µF

R_T=50mΩ

C=50µF

R_d=1.7Ω

3.6 Simulink/MATLAB Model and Simulation Results

3.6.a Simulation Results of System without Active Filter

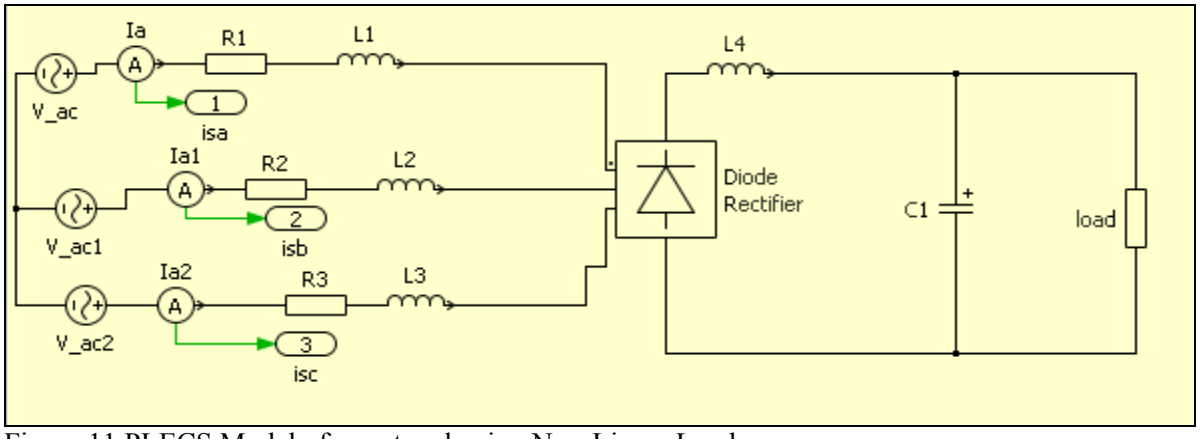

Figure 11.PLECS Model of a system having Non-Linear Load

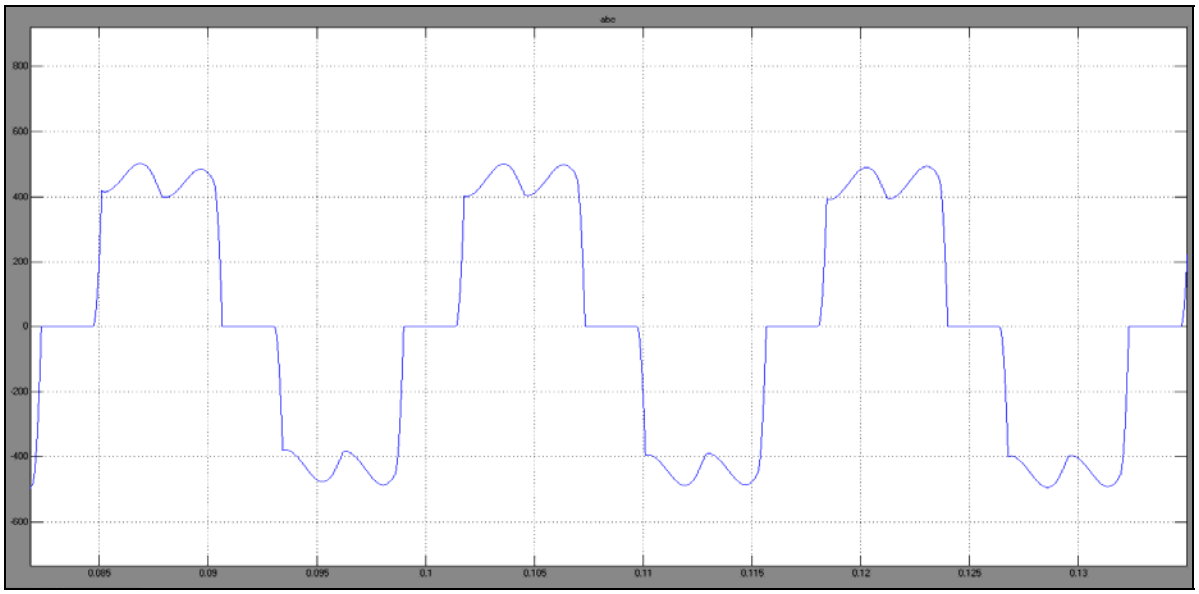

Figure 12.Supply Current waveform for the system without active filter

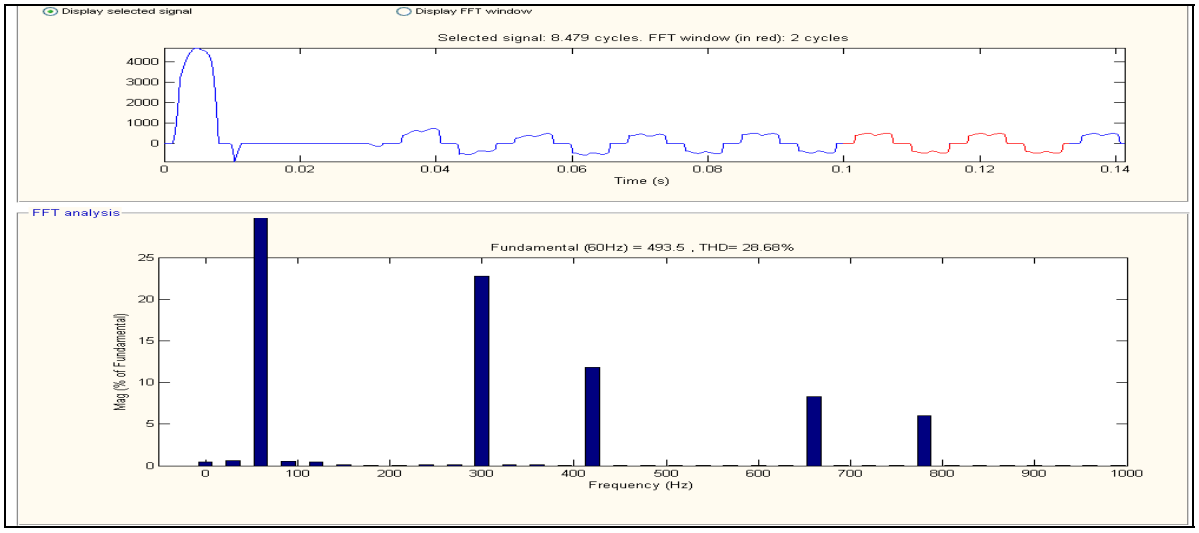

Figure 13.FFT Analysis of the Supply Current Waveform for the system without Active Filter

From the simulation results it can be seen that the System having Non-Linear load has :

- Total Harmonic Distortion=28.68%
- 5^{th} Harmonic Content=22.74%
- 7^{th} Harmonic Content =11.82%

- 11^{th} Harmonic Content=8.29%
- 13^{th} Harmonic Content =6.01%

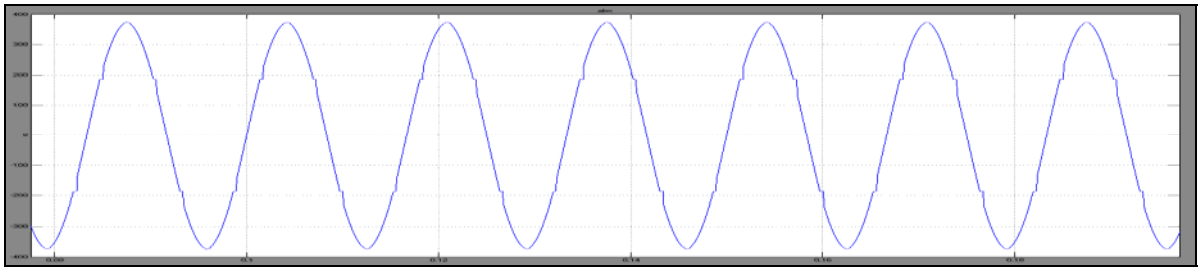

Figure14. V_{fa}(l-n Voltage at PCC) of the system without active filter

3.6.b Active Filter Compensation using Supply Current Harmonic Extraction Method

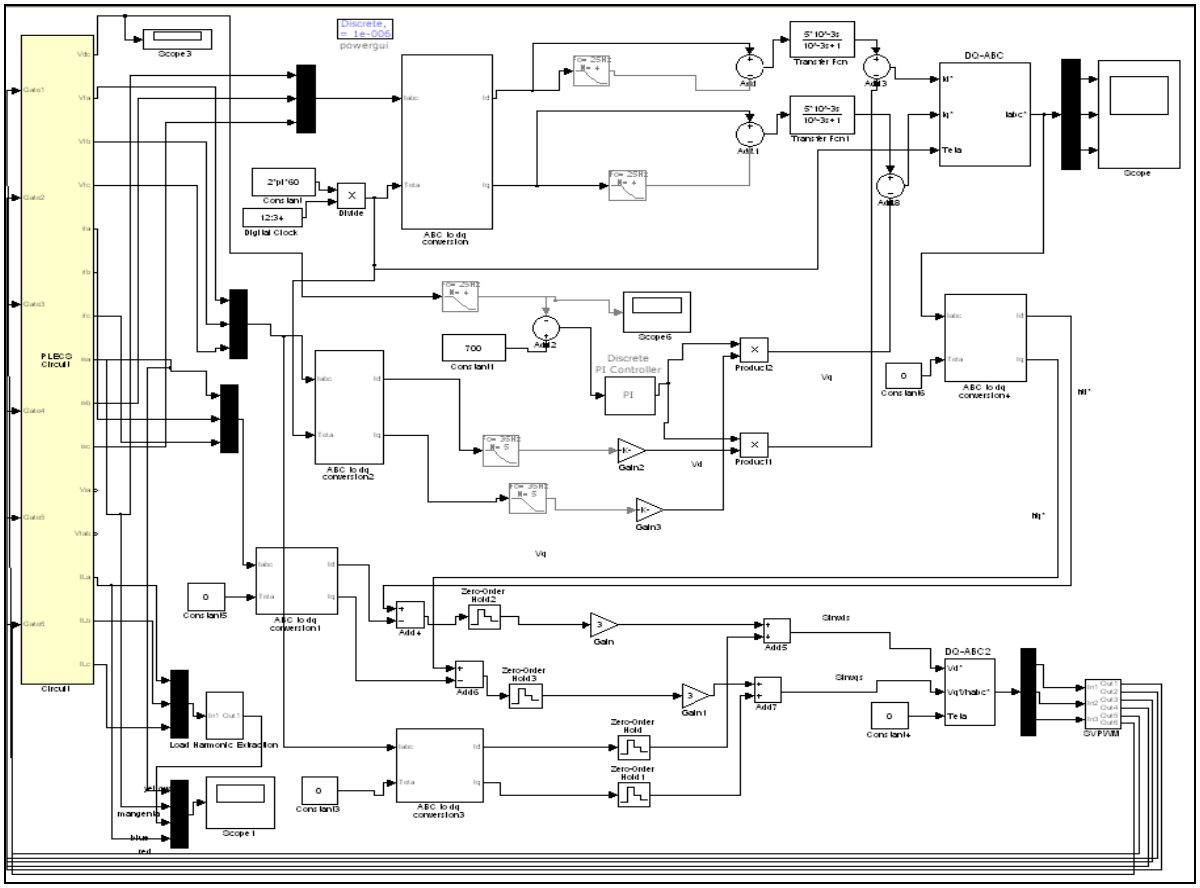

Figure 15.Simulink Model of an Active Filter Controller using Supply Current Harmonic Extraction method

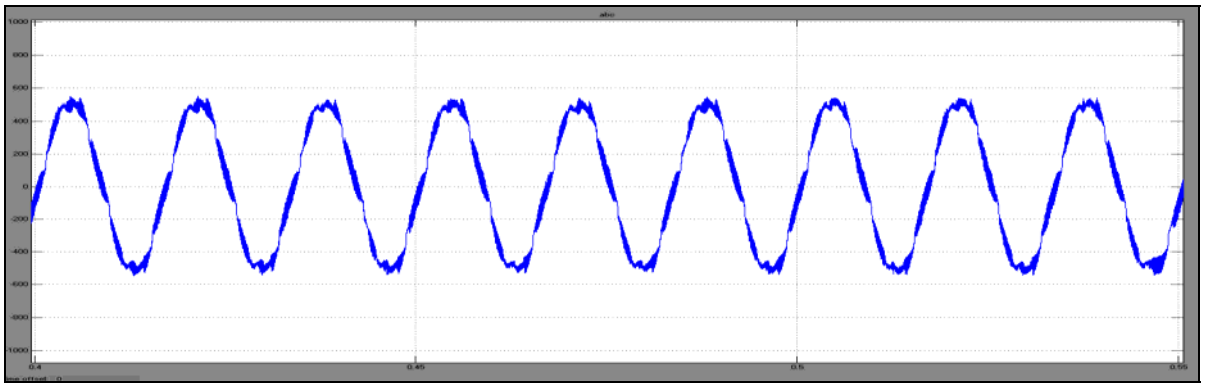

Figure 16.Supply Current waveform after the active filter compensation using supply current harmonic extraction method

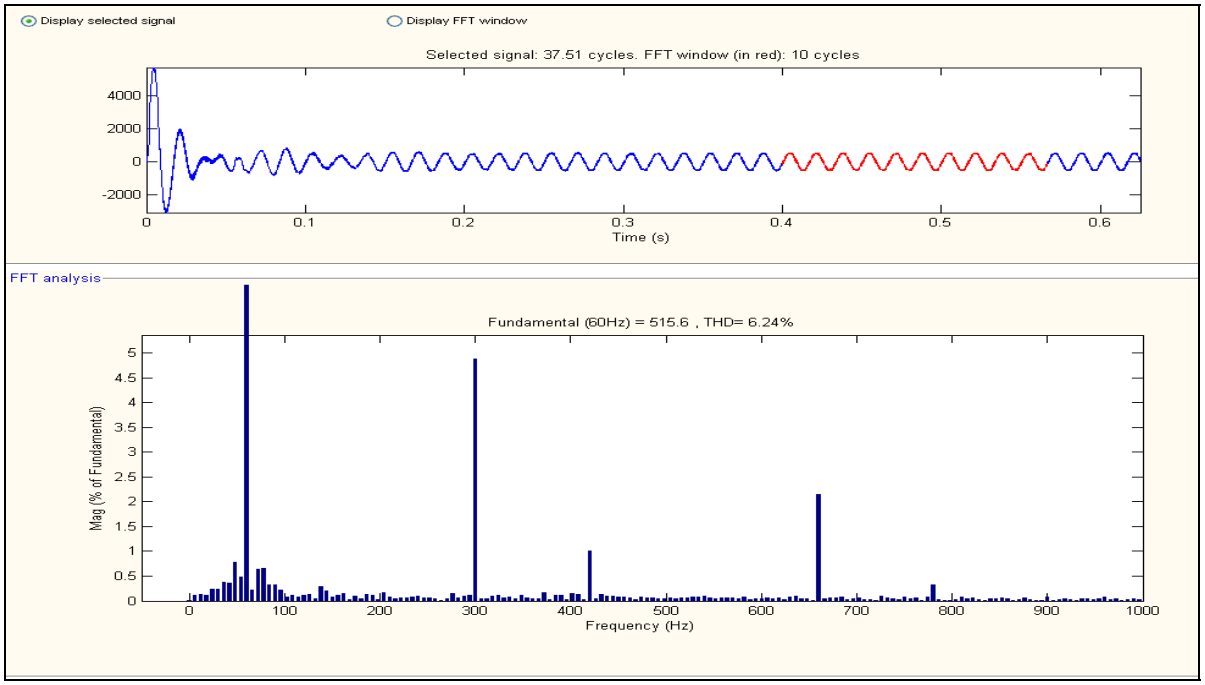

Figure 17.FFT Analysis of Supply Current Waveform after compensation

The FFT Analysis of supply Current waveform after the active filter compensation shows that:

- Total Harmonic Distortion=6.24%

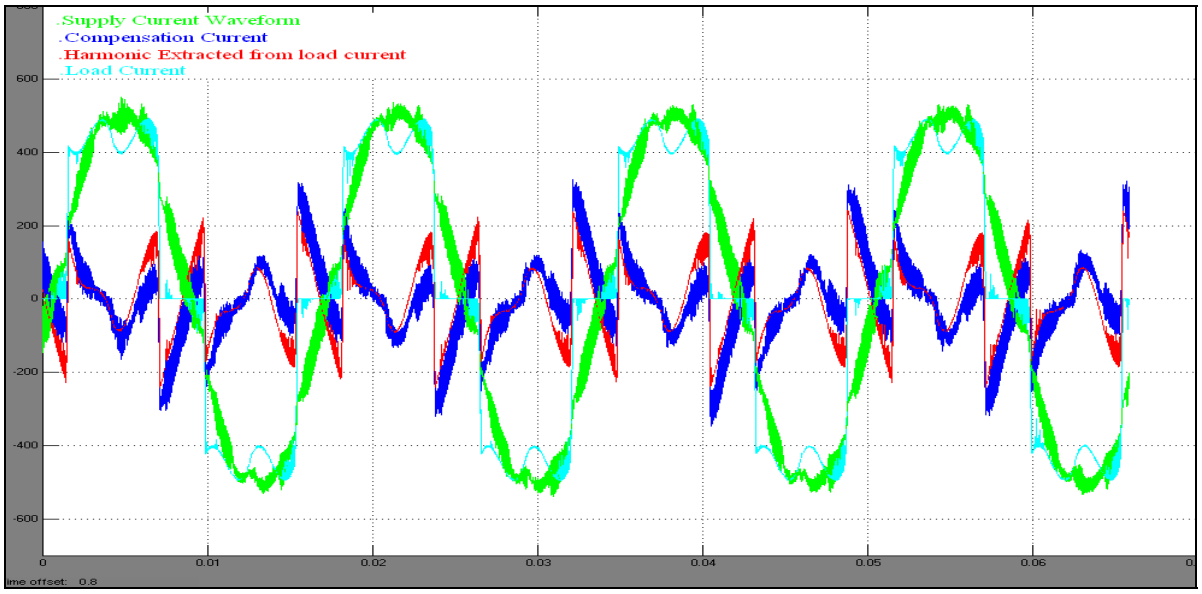

Figure 18.Compensation current matching with the Load Current Extracted Harmonics

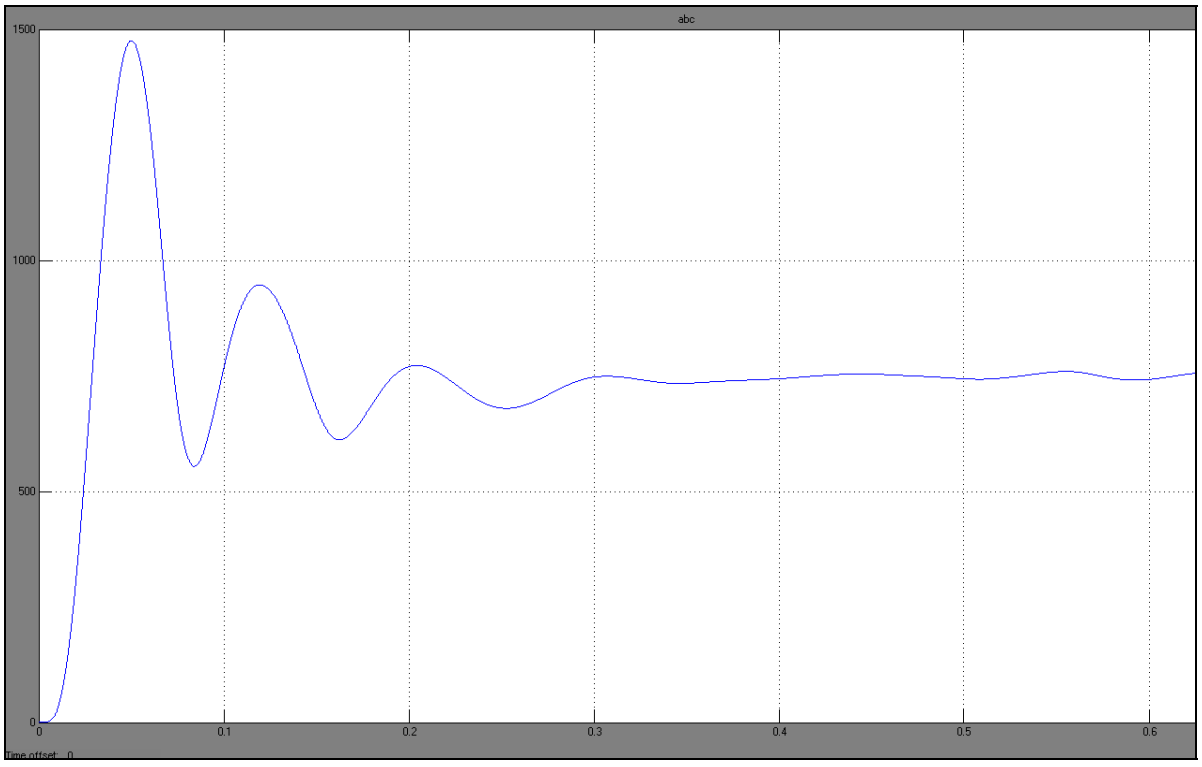

Figure 19.DC Bus Voltage controlled at 750V.

3.6.c Active Filter Compensation using Load Current Harmonic Extraction method

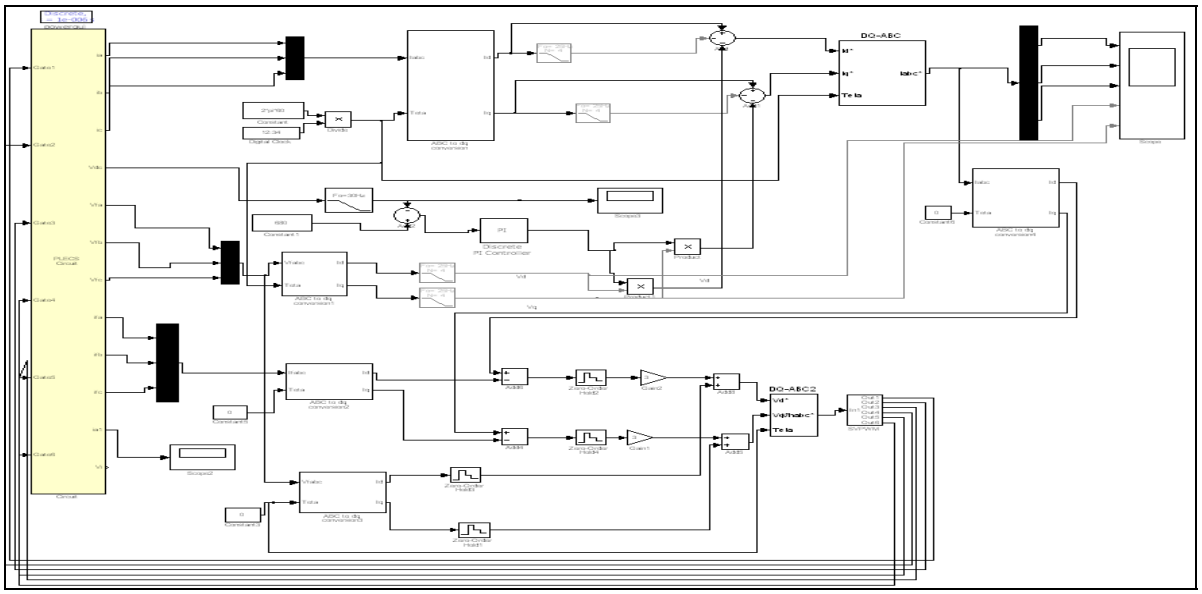

Figure 20.Simulink Model of the Active Filter Controller using Load Current Harmonic Extraction Method

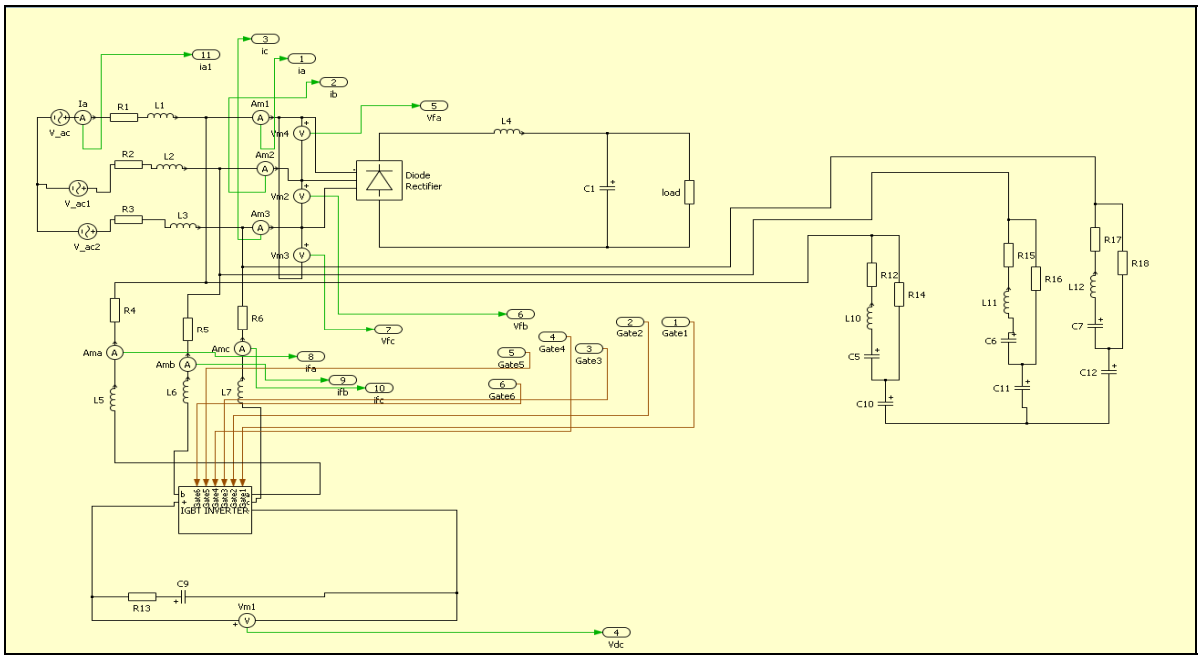

Figure 21.PLECS Model of the System with Active Filter

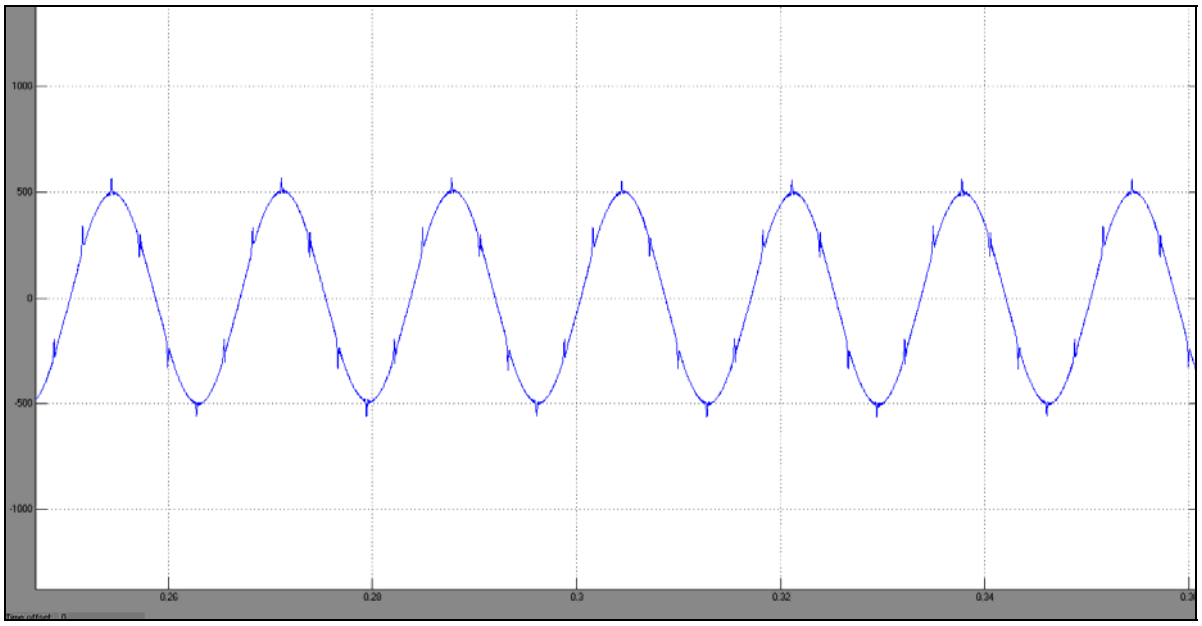

Figure 22.Supply Current Waveform after the active filter compensation using load current harmonic extraction method

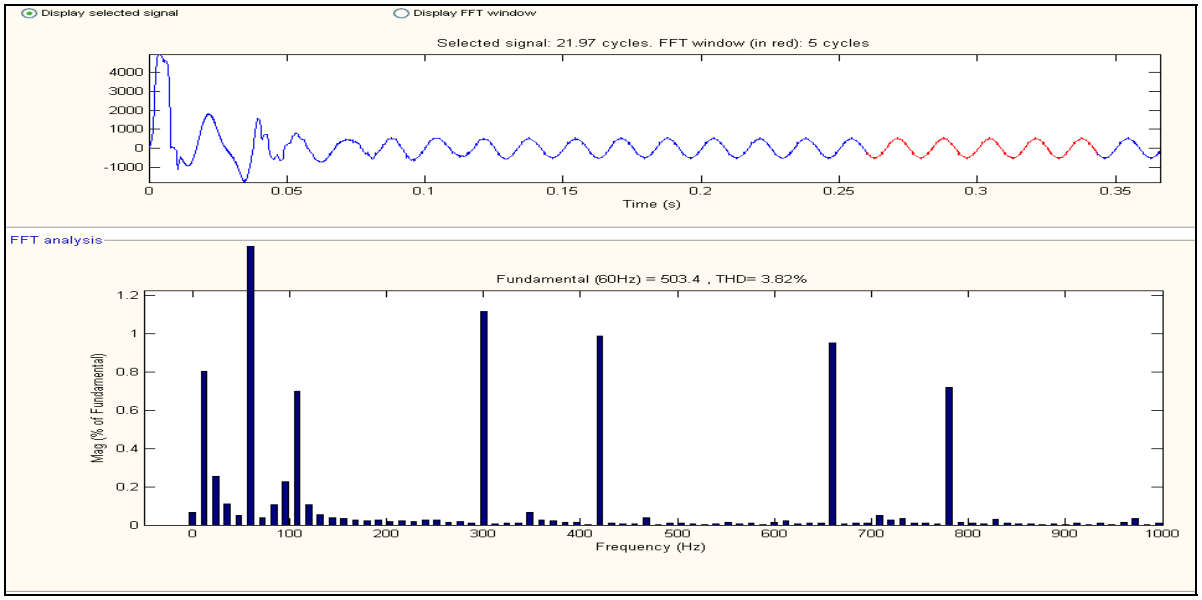

Figure 23.FFT Analysis of Supply Current Waveform after compensation

The FFT Analysis of supply Current waveform after the active filter compensation using load current harmonic extraction method shows that:

- Total Harmonic Distortion=3.82%

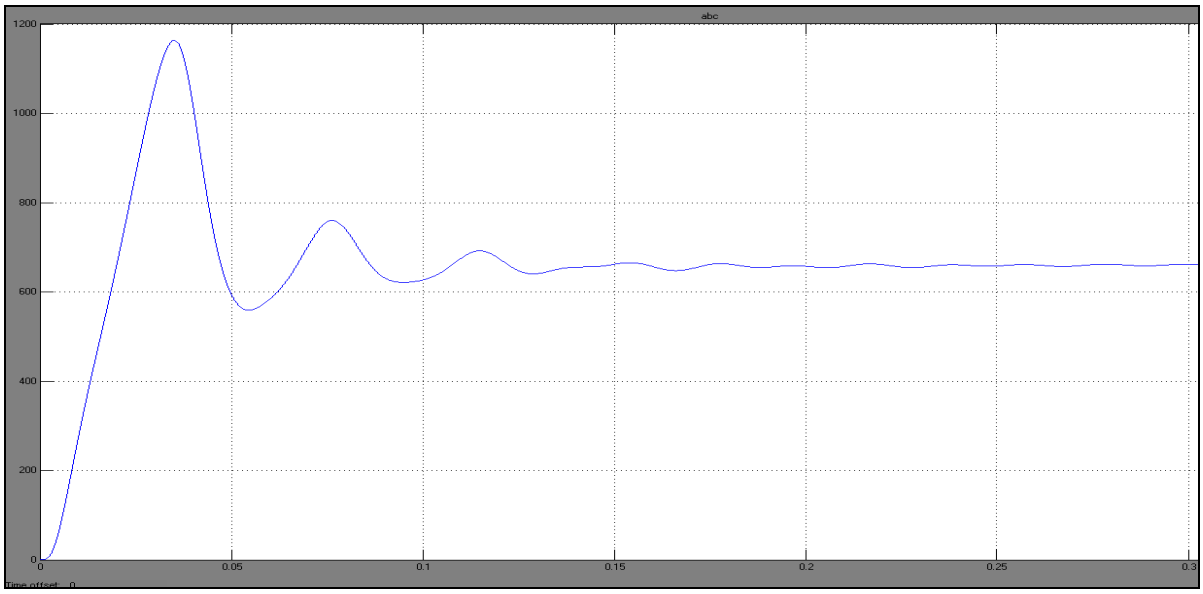

Figure 24.DC Bus Voltage Controlled at 680V

3.6.d Active Filter Compensation using V_f (Voltage at PCC) Harmonic Extraction method

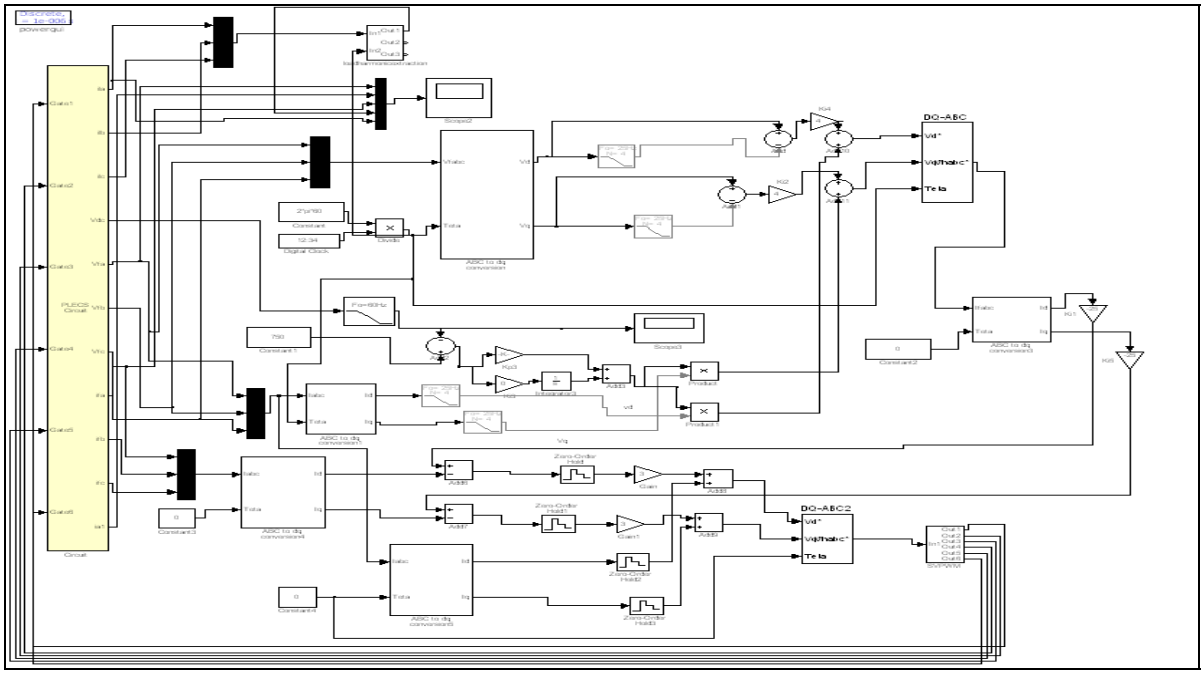

Figure 25. Simulink Model of the system with active filter controller using V_f harmonic extraction method

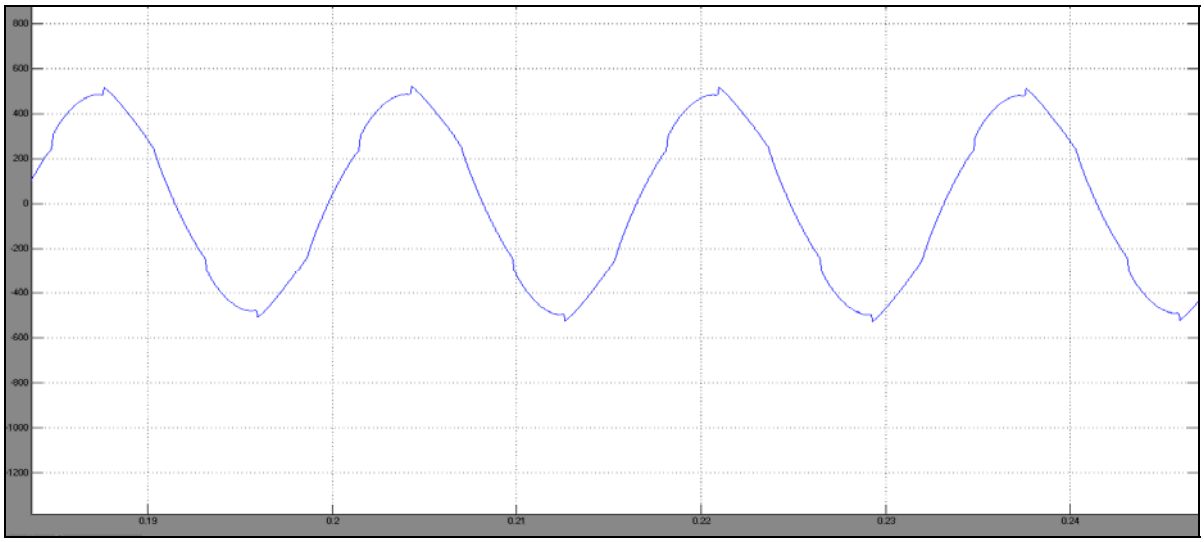

Figure 26.Supply Current Waveform after compensation using Vf harmonic extraction method

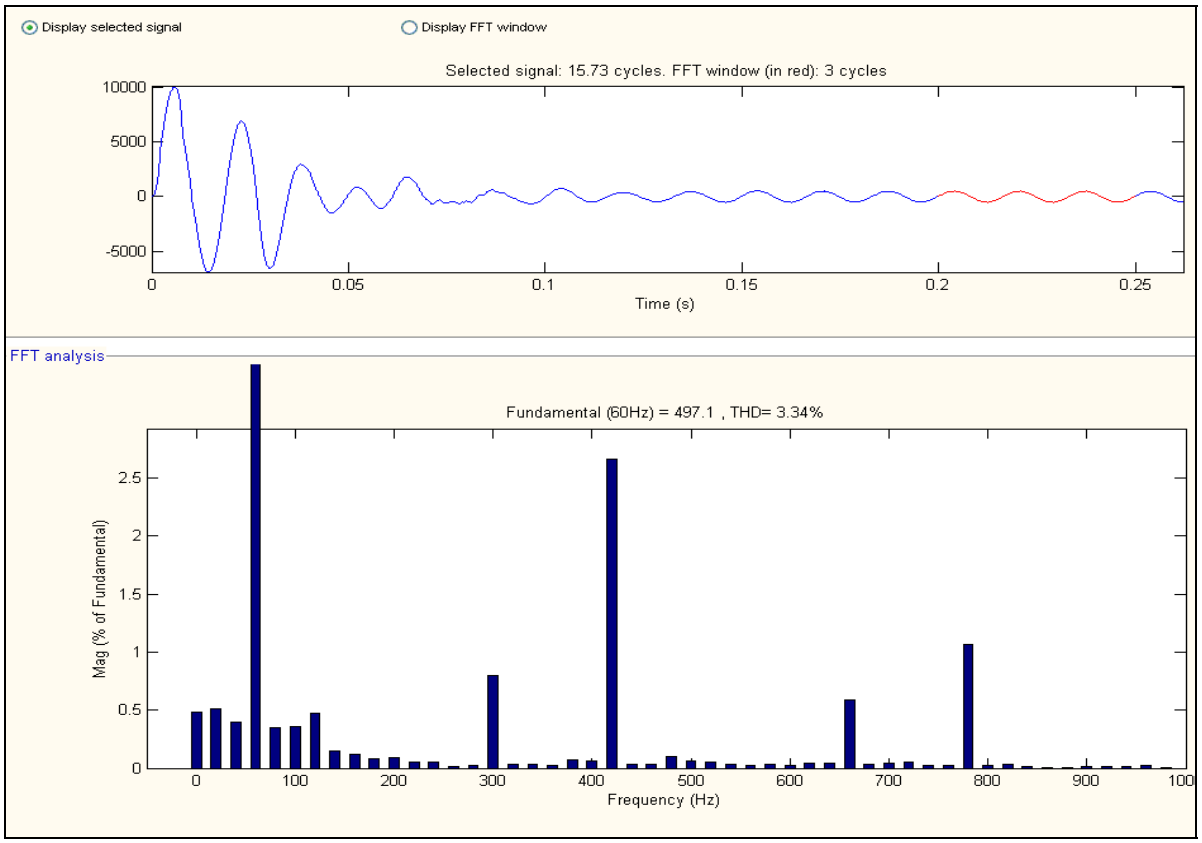

Figure 27.FFT Analysis of Supply current waveform after harmonic compensation using V_f harmonic extraction method

The FFT Analysis of supply Current waveform after the active filter compensation using V_f (Voltage at PCC) harmonic extraction method shows that:

Total Harmonic Distortion=3.34%

The value of Kv chosen for this simulation =140.

The Table below shows the total harmonic distortion (THD) that we get from the FFT Analysis of supply current waveform for different values of K_v. It is clear from this table that on increasing the value of K_v, we achieve better THD. This is due to the fact that on increasing the value of K_v, the resistance implemented by active filter reduces and hence it offers a low impedance path to the harmonic frequencies thereby resulting in better THD.

Table II. Effect of Change in K_v on Total Harmonic Distortion (THD) of supply current waveform

	K_v	**Total Harmonic Distortion(THD)**
1.	20	18.03%
2.	40	10.70%
3.	60	7.24%
4.	80	5.38%
5.	100	4.30%
6.	120	3.67%
7.	140	3.34%

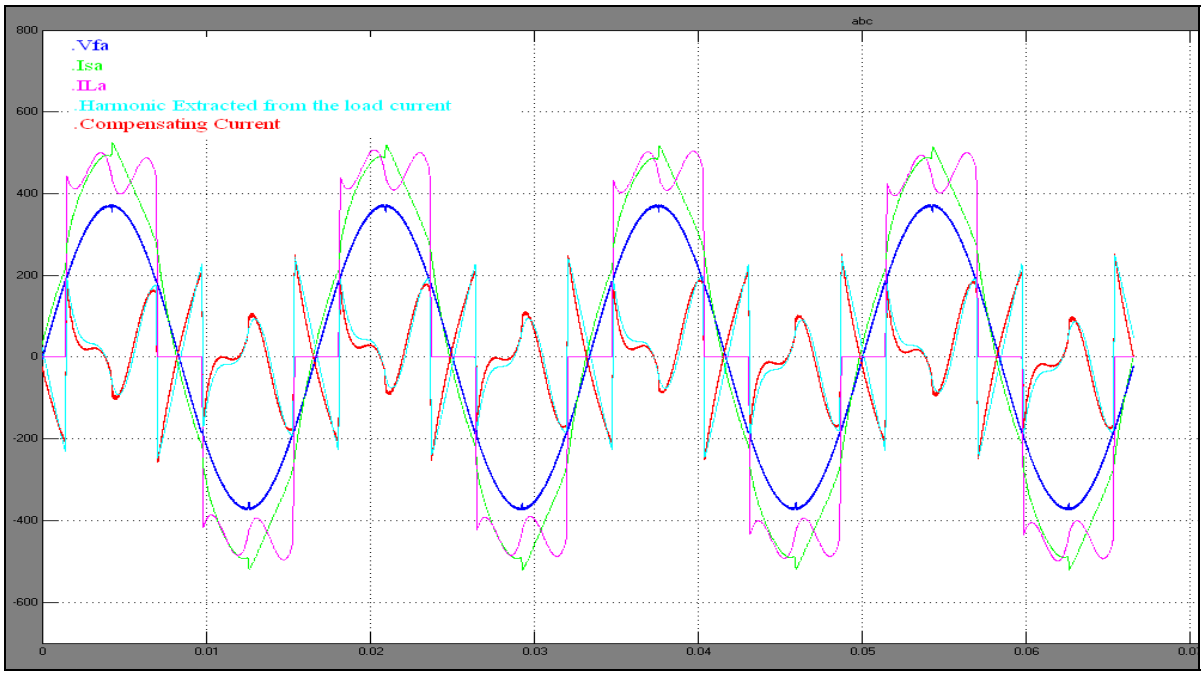

Figure 28. Compensating current, the harmonic current extracted from load current and V_{fa}

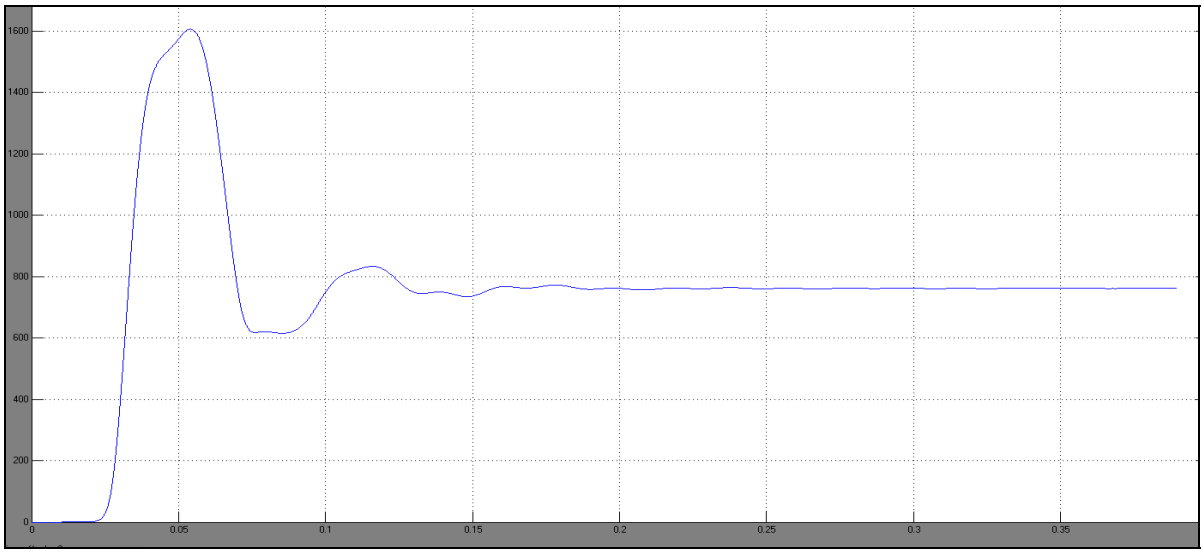

Figure 29. DC Bus Voltage Controlled at 750 V

3.7 Comparison between the three different harmonic extraction methods

The supply current harmonic extraction method is the feedback method of compensation which provides lead plus proportional characteristics to the active filter controller. The value of equivalent

inductance and resistance realized by the supply current harmonic extraction method can be varied to get low THD. The supply current harmonic extraction method is especially important when the source voltage has harmonics as this method directly aims to reduce the supply current harmonics to zero. Also, the supply current harmonic extraction method can provide a good suppression of amplification of harmonic currents due to anti parallel resonance.

The V_f harmonic extraction method is a feedback method of compensation which provides proportional characteristics to the active filter controller. The equivalent resistance realized by the active filter controller makes the active filter to act as harmonic damper along with the harmonic compensator. This method is aimed at reducing the harmonic voltage at the point of common coupling to zero so that only the fundamental current is drawn from the supply. The main drawback of this method is in case when the supply voltage has harmonics. In such a case, reducing the harmonic voltage at the point of common coupling to zero can lead to an increase in the supply side harmonic current.

The load current harmonic extraction method is a feed forward method of compensation. It is the most simple and straightforward method of harmonic compensation. Though, in this method, the THD cannot be improved beyond a certain point as there is no controller gain which can be varied to improve THD. The load current harmonic extraction method can only make an active filter act as a harmonic compensator but not as a harmonic damper. It can also not provide any compensation in case the supply voltage has harmonics.

From the comparison between three methods, it has been found that each method has its own specific use. All the methods can provide a good harmonic compensation but it depends upon the need of the system (in terms of requirement of harmonic damping or compensation of harmonics present due to supply voltage) to be able to choose which method to use.

3.8 Summary

This chapter discusses in detail about the three harmonic extraction algorithms and the predictive current control technique. The simulation results have been presented to verify the control algorithms and to make comparisons between them. All the three harmonic extraction method have been shown to give a THD <12% (for L_s=22μH,SCR=50-100) thereby conforming with IEEE 519 harmonic standards. From the simulation results, in terms of achieving low THD, it can be inferred that V_f (Voltage at PCC) harmonic extraction method gives a better harmonic compensation (THD=3.34%) as compared to the supply current (THD=6.24%) and load current (THD=3.82%) harmonic extraction method. From the comparison between three methods, it has been found that each method has its own specific use. All the methods can provide a good harmonic compensation, in terms of conforming to IEEE 519 harmonic standards, but it depends upon the need of the system (in terms of requirement of harmonic damping or compensation of harmonics present due to supply voltage) to be able to choose which method to use.

This chapter also discusses in detail about the analog implementation of the predictive current controller, Space Vector PWM technique, the implementation issues and the dead time compensation (3μsec) of the predictive current regulator.

CHAPTER 4. FPAA AND FPGA IMPLEMENTATION OF SRF CONTROLLER

The presence of multiple harmonics in the power line due to various non-linear loads like adjustable speed drives, computers, fax machine, PLC's, etc. requires high frequency switching of an active filter inverter so as to reduce the harmonic content at the point of common coupling (PCC) to be typically lower than 5%(for SCR<20) as specified by IEEE 519 harmonic standards. In this work, the Field Programmable Analog Array (FPAA) based analog controller has been used to implement the SRF Controller algorithm for harmonic current extraction for Shunt Active Filter controller and the results are compared with the conventional digital implementation on Field Programmable Gate Array (FPGA). The FPAA based analog controller implementation proves to be faster than the digital FPGA implementation and can be a potential controller for SiC based active filter inverters with high switching frequencies of 50-100 kHz (10-20us).

4.1 Field Programmable Analog Arrays

Field Programmable Analog Arrays (FPAA) are integrated circuits that can implement various analog operations. FPAAs are composed of Configurable Analog Blocks (CABs) and an interconnecting routing network. Each CAB can implement analog processing functions including amplification, integration, differentiation, addition, subtraction, multiplication, and division to name a few. The interconnection network routes the signal between CABs and I/O blocks. Figure 30 shows the overall configuration diagram of FPAA.

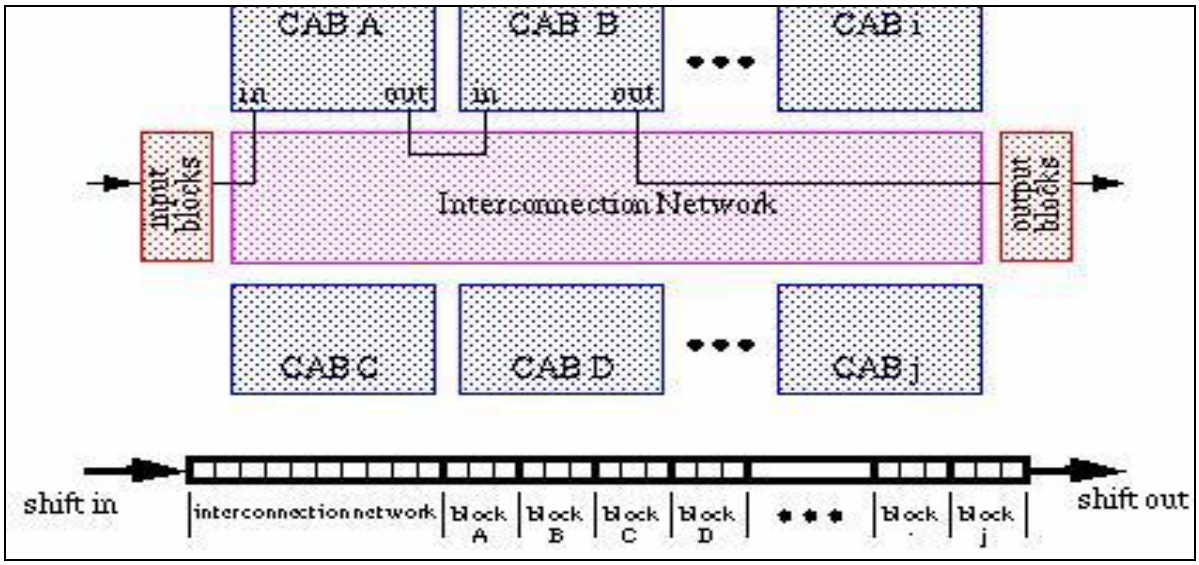

Figure 30. FPAA Configuration Diagram [16], [17]

FPAA's are reconfigurable and easy to design and can simulate complex analog circuits as compared to Analog Boards. They are also much faster than Field Programmable Gate Array (FPGA) in terms of speed while delivering the results with same accuracy. In FPGA's the additional delay can be attributed to Analog to Digital and Digital to Analog conversion steps. Thus, FPAA's provides not only the ease of reconfigurability of complex analog circuits but also proves to be the best solution when it comes to high speed switching applications.

The FPAA's used in this work are Anadigm third generation AN231E04 board. It is a discrete time FPAA chip which is designed with the switched capacitor technology [16]. This allows for easier programmability of FPAA. Figure 31 shows the FPAA AN231E04 evaluation board.

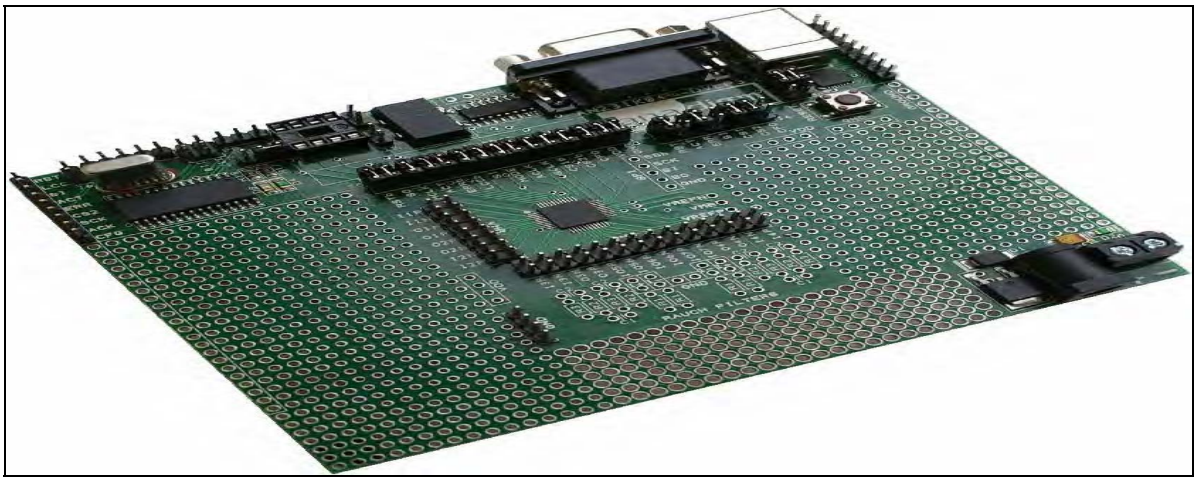

Figure 31. Anadigm's AN231E04 FPAA Evaluation Board

4.2 Simulation Results of Positive Sequence SRF Controller Using Simulink/MATLAB

The simulation of Positive sequence SRF controller with square wave input as the harmonic current waveform has been performed and the results are shown below.

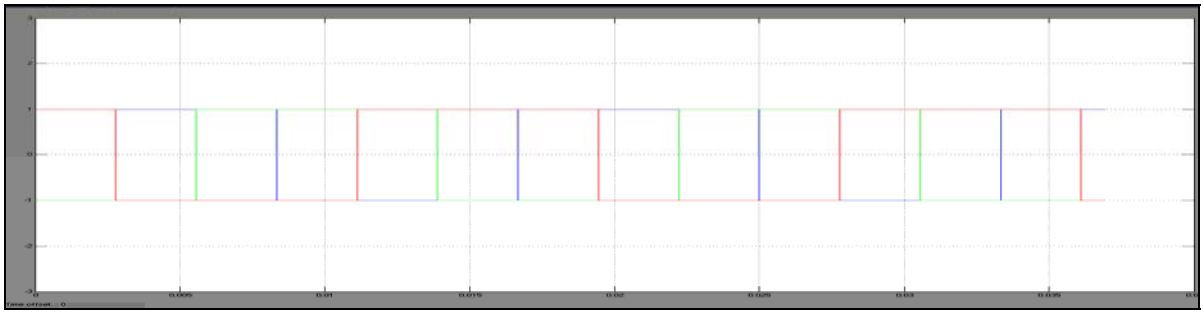

Figure 32. I_{La},I_{Lb},I_{Lc} waveform input to the SRF Controller

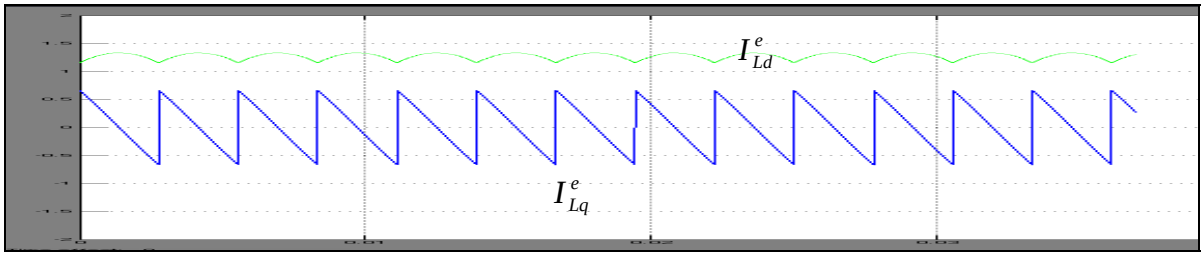

Figure 33. I^e_{Ld} , I^e_{Lq} waveform obtained after the Park Transformation

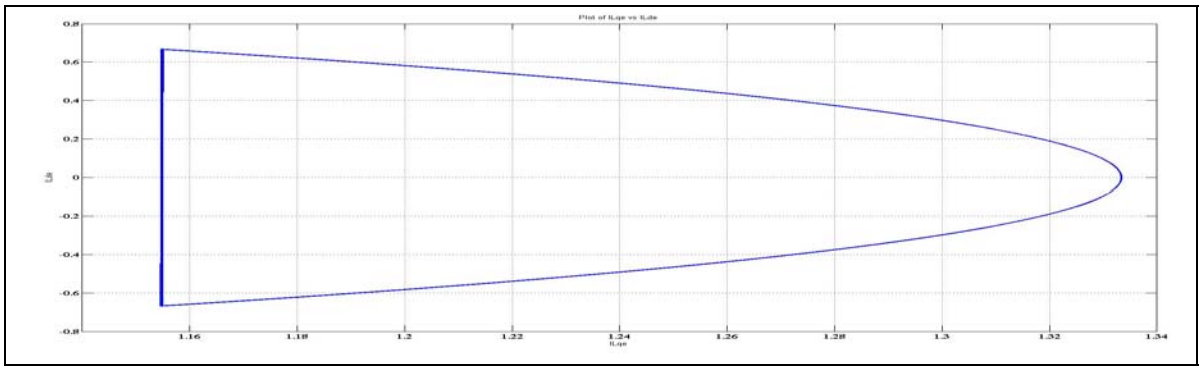

Fig34. I^e_{Lq} vs I^e_{Ld}

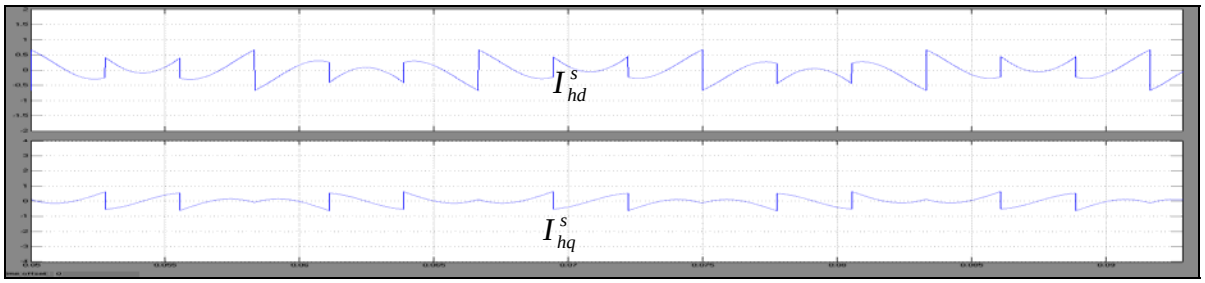

Figure 35. I^s_{hd}, I^s_{hq} waveforms

Ideally, I^s_{hd} should coincide with I_{La} at each zero crossing as shown in the Figure 36 below.

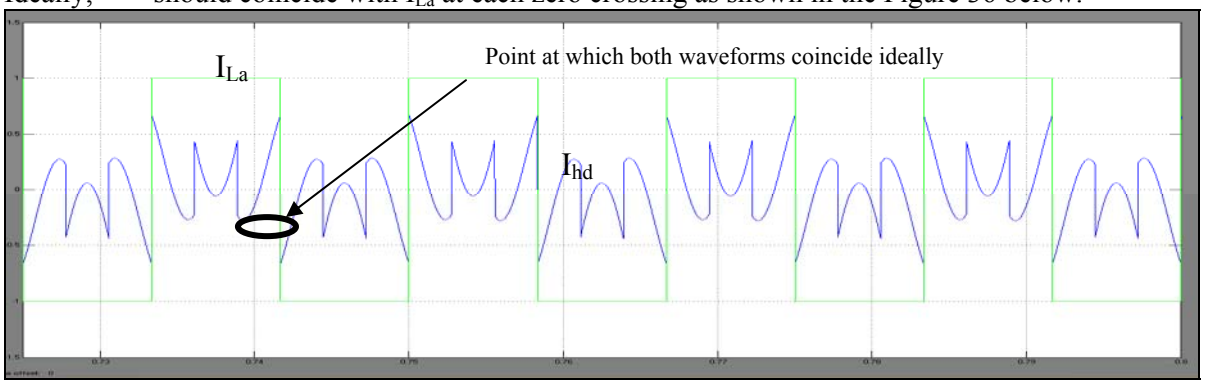

Figure 36. I_{hd} and I_{La} waveform

4.3 Implementation of SRF Controller on FPAA

The Positive sequence SRF Controller has been implemented using seven AN231E04 boards. The FPAA chips are configured using Anadigm Designer 2 software. Figure 37 shows the implementation of SRF Controller on seven FPAA boards using Anadigm Designer 2

software. The corresponding experimental setup is shown in Figure 38.A 3rd order Butterworth filter with a cutoff frequency of 10Hz has been implemented to perform a low pass filter operation on FPAA.

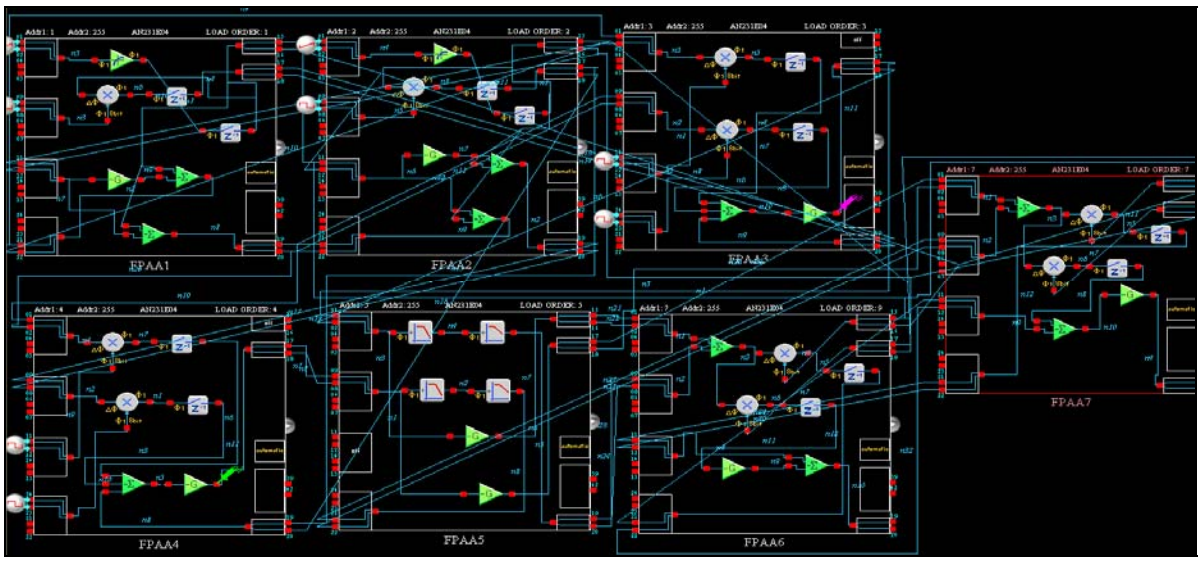

Figure 37. Implementation of Positive Sequence SRF Controller using Anadigm Designer 2 software

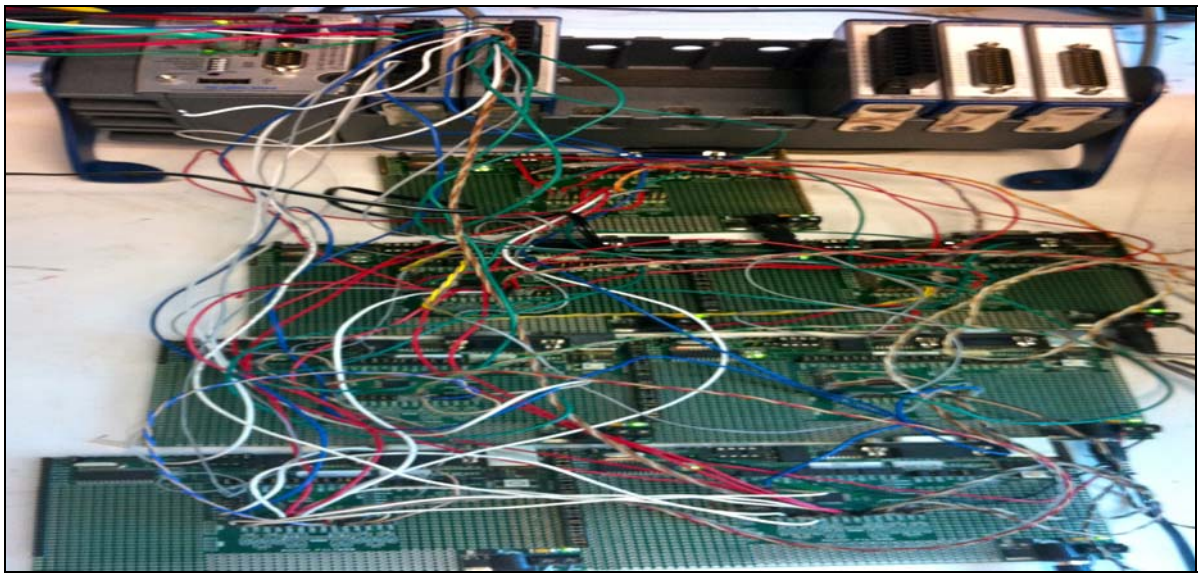

Figure 38. Laboratory Setup of seven FPAA boards to implement Positive Sequence SRF Controller algorithm

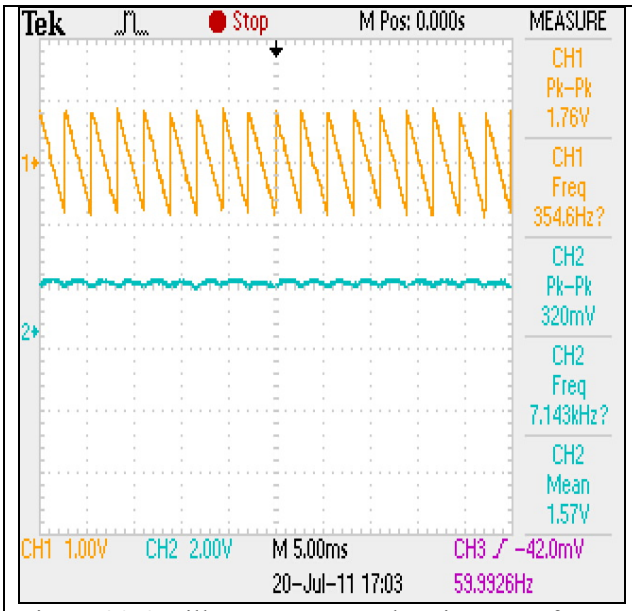

Figure 39.Oscilloscope output showing waveforms for $I_{Ld}^{e}(bottom), I_{Lq}^{e}(top)$

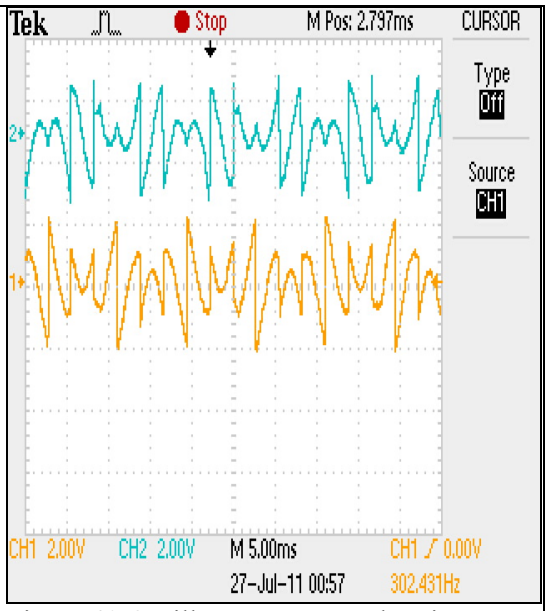

Figure 40.Oscilloscope output showing waveforms for $I_{hq}^{s}(top), I_{hd}^{s}(bottom)$

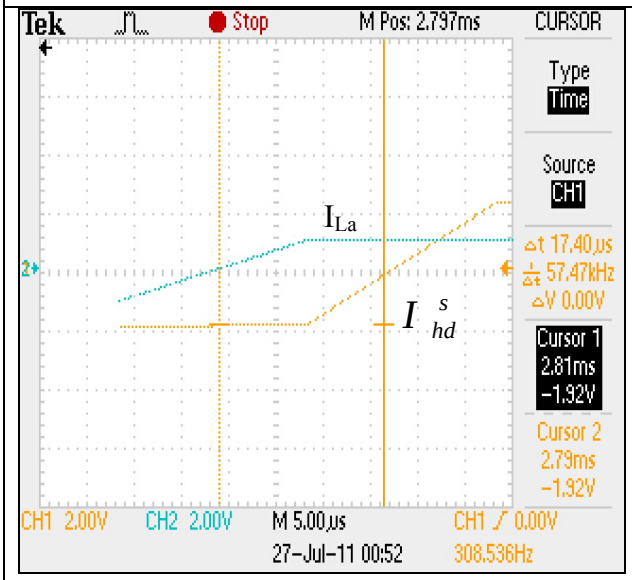

Figure 41.Delay in Implementation on FPAA(17.4µsec)

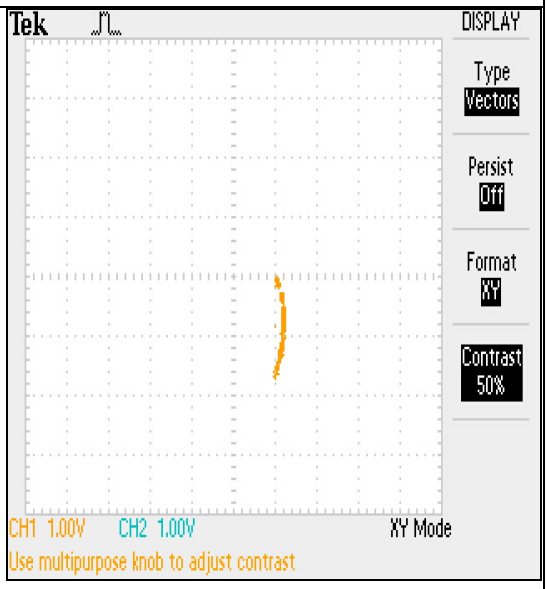

Figure 42.Plot of I_{Lq}^{e} vs I_{Ld}^{e}

From these results, it can be seen that the delay in implementation of the complete positive sequence SRF controller algorithm is 17.4 µsec.

4.4 Implementation of SRF Controller on FPGA

The National Instrument Compact-RIO (NI-C-RIO) digital controller system consists of a reconfigurable chassis that contains the user programmable FPGA, hot swappable I/O modules and a real time controller. LABVIEW software is used to program the FPGA and the digital NI-CRIO controller system. The square-wave (worst case for harmonic current extraction) load currents i_{La}, i_{Lb}, i_{Lc} were generated by the C-RIO controller internally and then provided as inputs to the programmed SRF Controller. A 4th order Butterworth filter with a cutoff frequency of 10 Hz has been used to perform a low pass filter operation. The outputs of the FPGA (C-RIO) controller which are I_{ha}, I_{hb}, I_{hc} compensating harmonic currents extraction are shown in Figure 44. It is verified that the digital FPGA based C-RIO controller can also be used to implement the SRF Controller – albeit with larger computational delays compared to an analog based FPAA controller implementation.

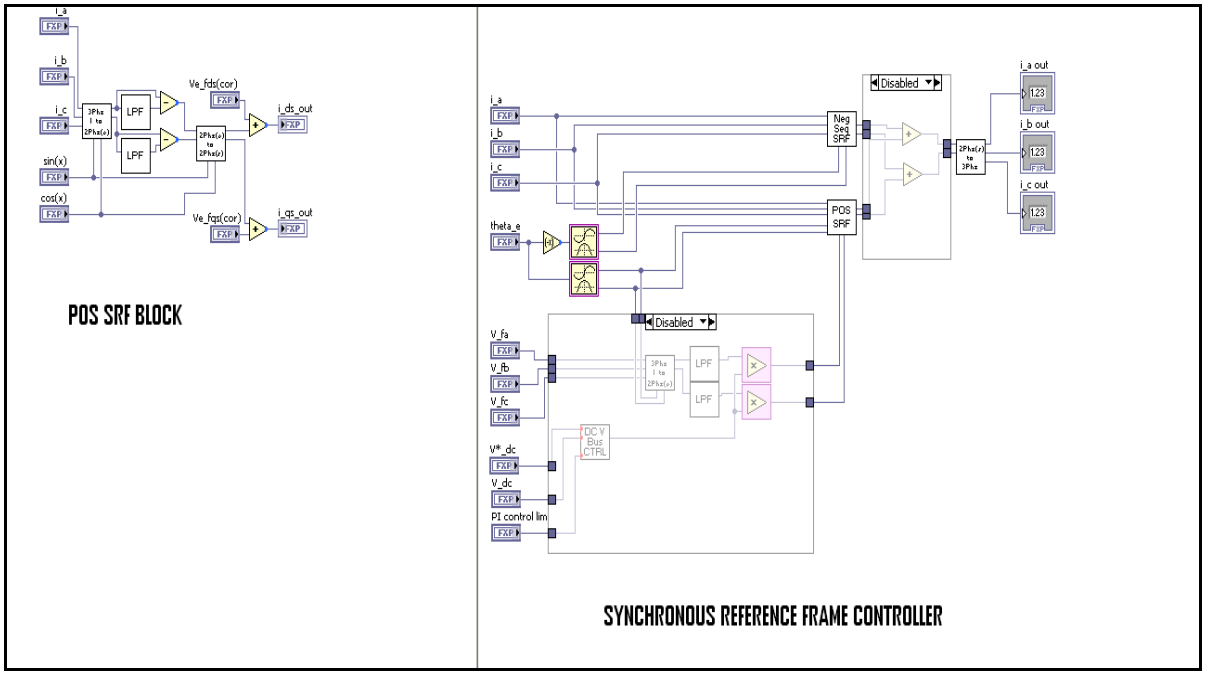

Figure 43. Positive Sequence SRF Controller Implementation on NI C-RIO(FPGA) using LABVIEW software

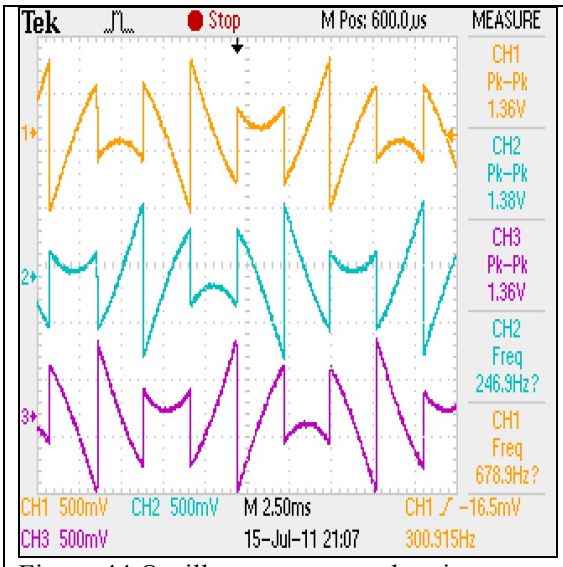

Figure 44.Oscilloscope output showing waveforms for I_{ha}, I_{hb}, I_{hc}

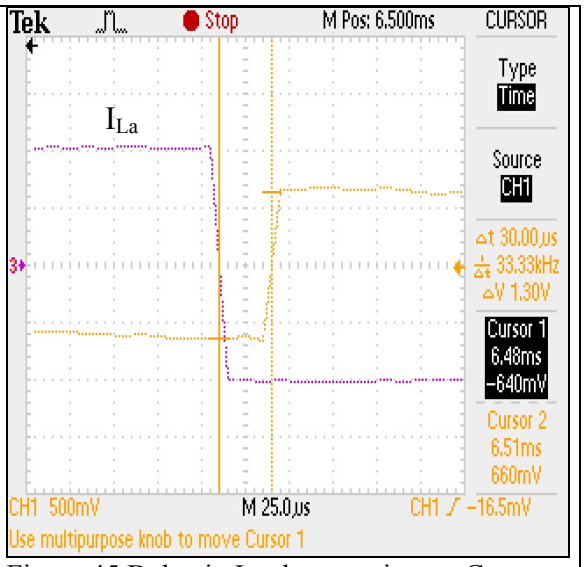

Figure 45.Delay in Implementation on C-RIO(30µsec)

4.5 Comparison of Analog FPAA and Digital FPGA Controller Outputs

The comparison of the analog FPAA and digital FPGA based controllers were based on the implementation delay for the same SRF Controller based compensator for harmonic current extraction with exactly the same square-wave (worst case for harmonic current extraction) load currents i_{La}, i_{Lb}, i_{Lc} generated by the C-RIO controller for both analog (FPAA) and digital (FPGA) controllers. The delays were measured by calculating the time difference between the zero crossings of two points (one point on the input signal, i_{La} and the other point on output signal, I_{hd}^{s}). These points of the two signals were chosen because the zero crossings of the input current signal, i_{La} and the output current signal, I_{hd}^{s} are ideally supposed to coincide. Figure 41 shows a time delay of 17.4µs for the implementation on analog FPAA based controller. Figure 45 shows a time delay of 30µs for the implementation on digital FPGA based controller. Thus, it can be seen from the results obtained from both the implementations that the FPAA analog controller is much faster than the

FPGA digital controller, and therefore it can be used as a viable controller for very high switching frequency converter applications – such as Silicon Carbide power semiconductor device based converters with 50 kHz switching frequency.

CHAPTER 5.HARDWARE IMPLEMENTATION OF SHUNT ACTIVE FILTER SYSTEM

The hardware implementation of shunt active filter system has been performed by first building a nonlinear load (for lower power rating as compared to the simulations shown in Chapter3) in the laboratory. The current and the voltage measurements from the nonlinear load were then given to the harmonic extraction board and the current controller board to drive the active filter inverter.

Figure 46 shows the hardware setup of the shunt active filter system in laboratory.

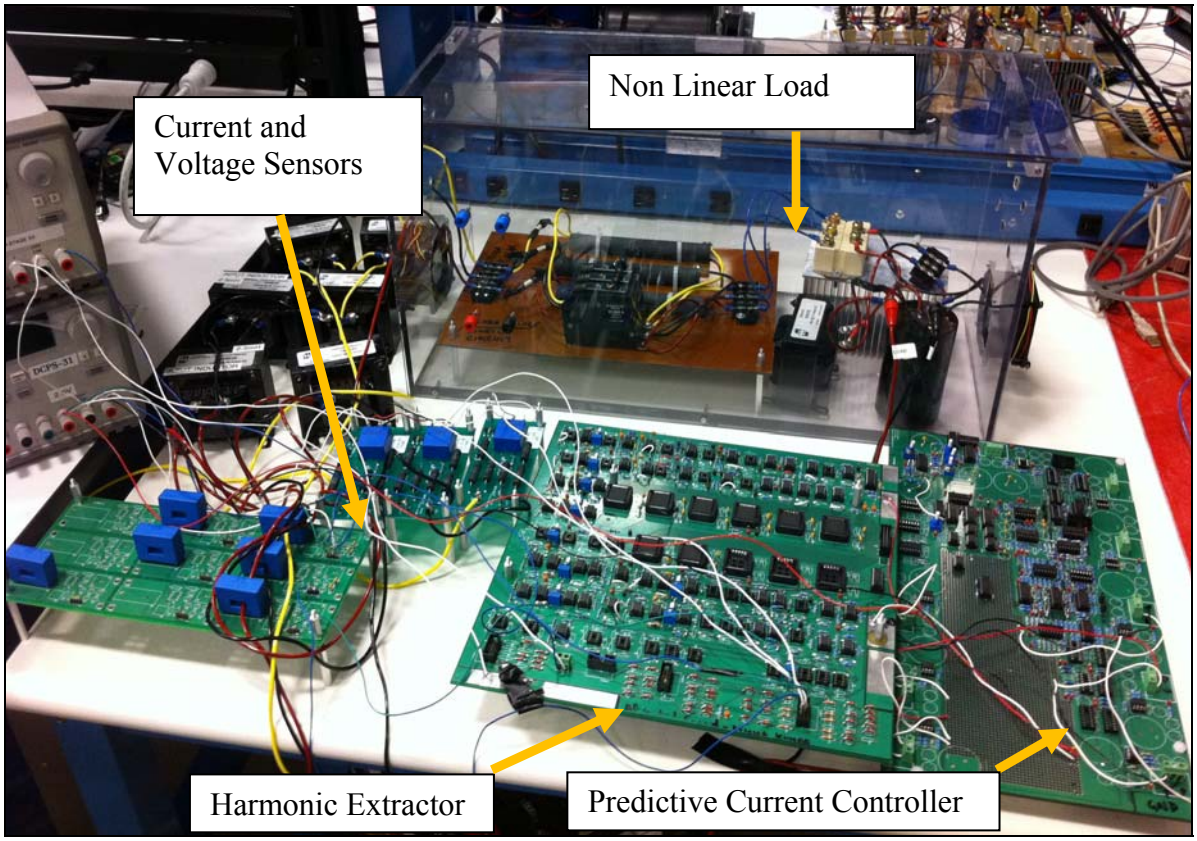

Figure 46.Hardware Setup of Shunt Active Filter Controller and the Nonlinear Load

5.1 Nonlinear Load Specifications

- Vs(rms line to line)=208V
- Ls=Supply Side Inductance=2.5mH

- Lac=Smoothing Reactor =2.5mH
- Ldc=DC side Inductance=5mH
- Cdc=DC side Capacitance=50µF
- Rdc=DC Load=72Ω
- Pdc=Load Rating=944.67W
- Rstartup=Startup Resistance=5Ω,100W

5.1.a Diode Rectifier with DC side Inductor, and DC side Capacitor system

This type of nonlinear load has a higher value of di/dt for the supply current waveform. The dc side inductor has the effect of increasing the di/dt of the supply current waveform but reducing the supply current amplitude ripple. The amplitude of the ripple depends on the value of L_{dc} chosen. Particularly, for the specifications of this system, the value of L_{dc} is such that it gives a discontinuous supply current waveform.

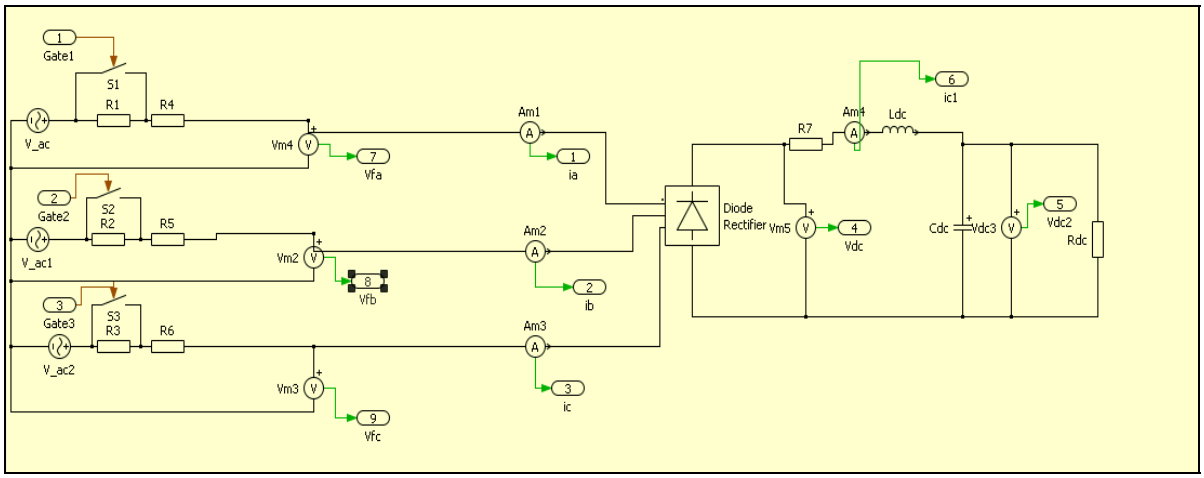

Figure 47. Diode Rectifier with DC side Inductor, and DC side Capacitor system

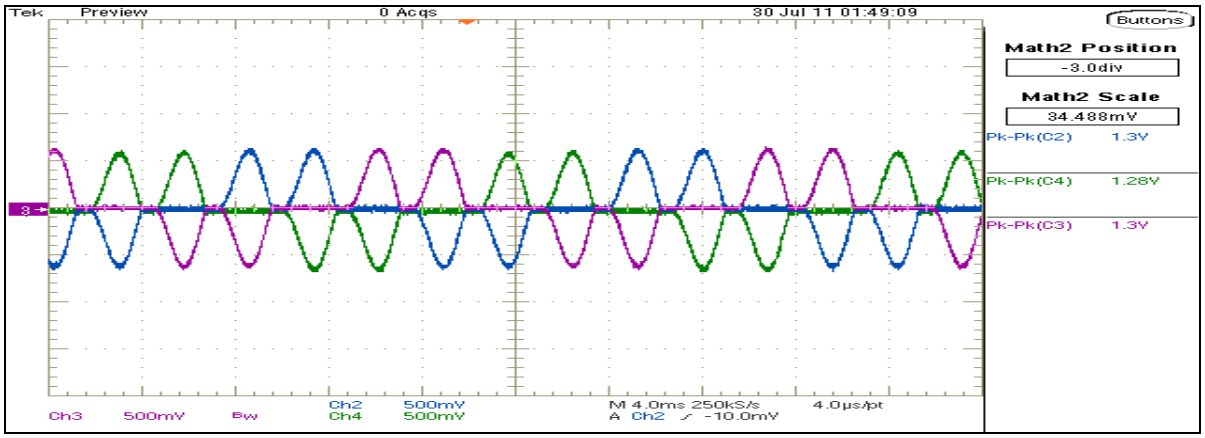

Figure 48. Oscilloscope waveform for Scaled I_{sa},I_{sb},I_{sc}

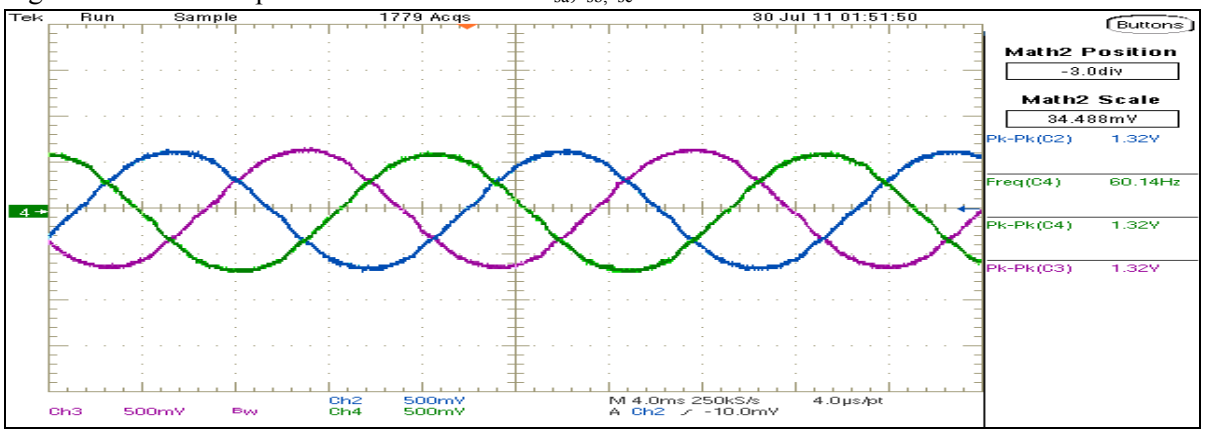

Figure 49. Oscilloscope Waveform for Scaled Three phase voltage V_{fa},V_{fb},V_{fc}

5.1.b AC Supply Side Line Inductor and Diode Rectifier with DC side Capacitor system

The AC Supply Side Line Inductor helps in reducing di/dt and the peak supply current and hence the THD value (typically limited to 40%) [18]. It helps in making the supply current more continuous.

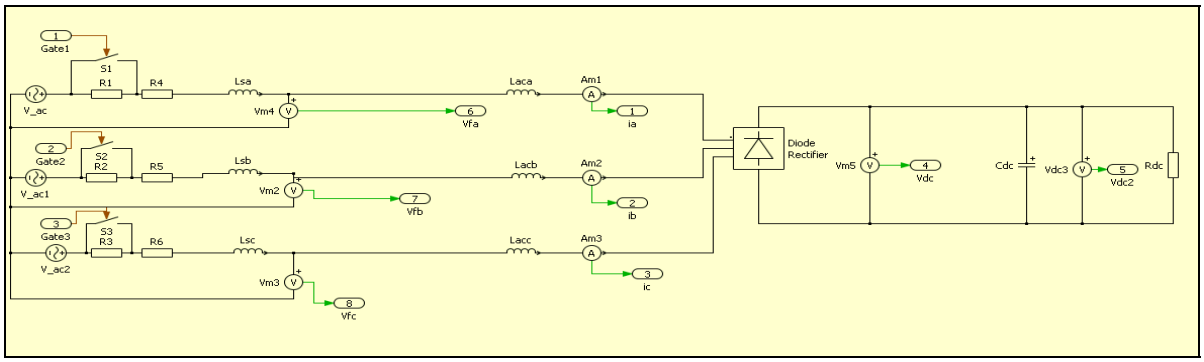

Figure 50. Diode Rectifier with AC supply side Inductor and DC side Capacitor system

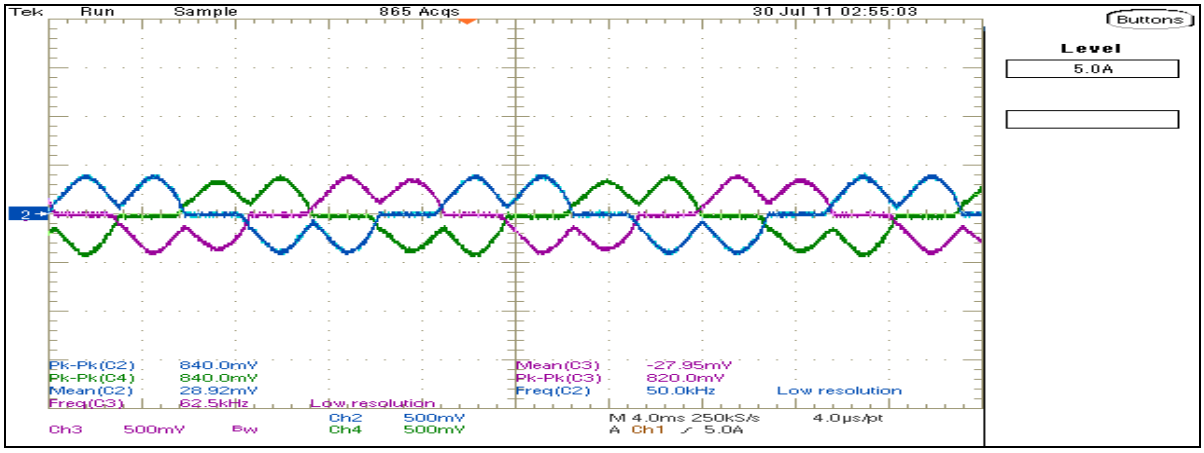

Figure 51. Oscilloscope waveform for Scaled I_{sa},I_{sb},I_{sc}

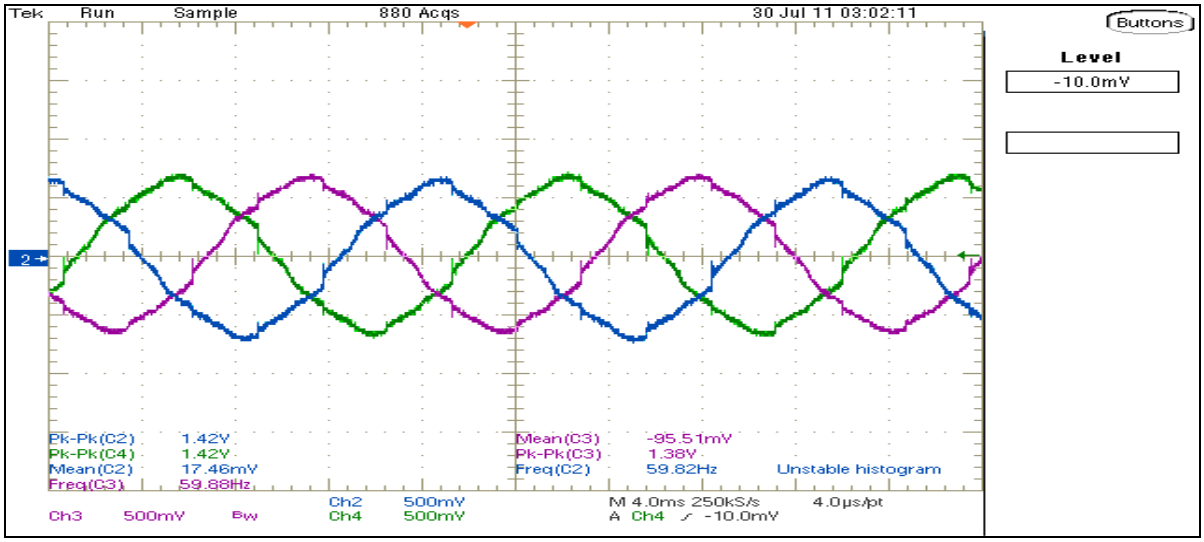

Figure 52. Oscilloscope Waveform for Scaled Three phase voltage V_{fa},V_{fb},V_{fc}

5.1.c AC Supply Side Line Inductor, Diode Rectifier with DC side Inductor, and DC side Capacitor system

The Nonlinear Load schematic for AC Supply Side Line Inductor, Diode Rectifier with DC side Inductor, and DC side Capacitor system is shown in Figure 53.This is the most desirable utility interface topology for ASD's and other loads like DC power supplies. The supply side AC line inductors reduce the THD and the di/dt of the supply current waveform [18]. Also, L_{dc} helps in getting a continuous supply current and helps reduce supply voltage unbalance effects on supply side [18].

The Diode Bridge startup circuit is required to limit the inrush current due to the charging of DC side capacitor during start up. For this purpose, a startup resistance is used in this circuit and all the other nonlinear load circuits shown above for initial few seconds and then it is taken out of the circuit using a switch as shown in the figure.

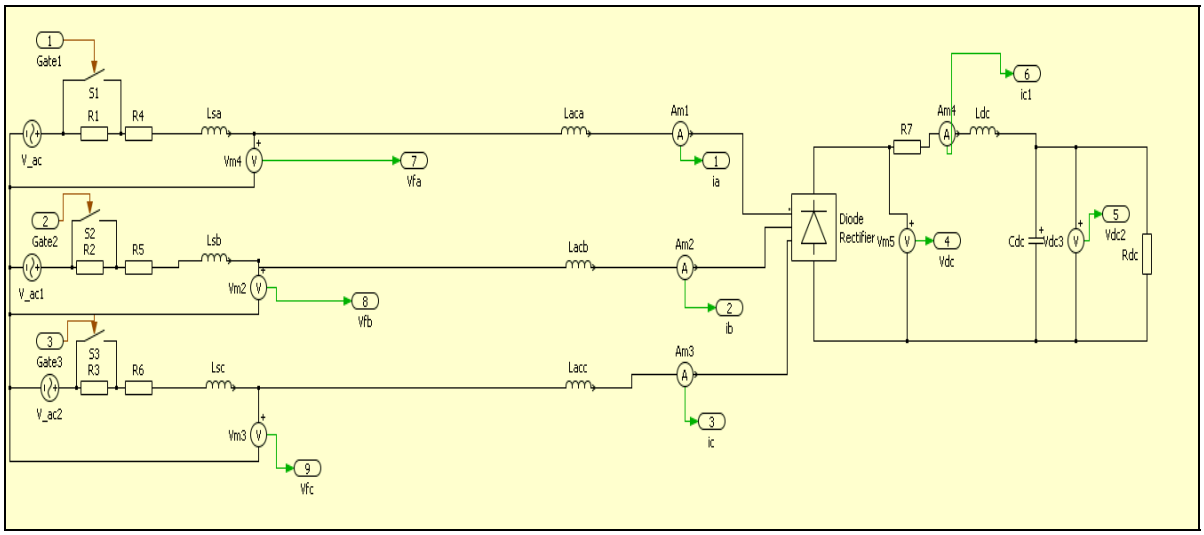

Figure 53. AC Supply Side Line Inductor, Diode Rectifier with DC side Inductor, and DC side Capacitor system.

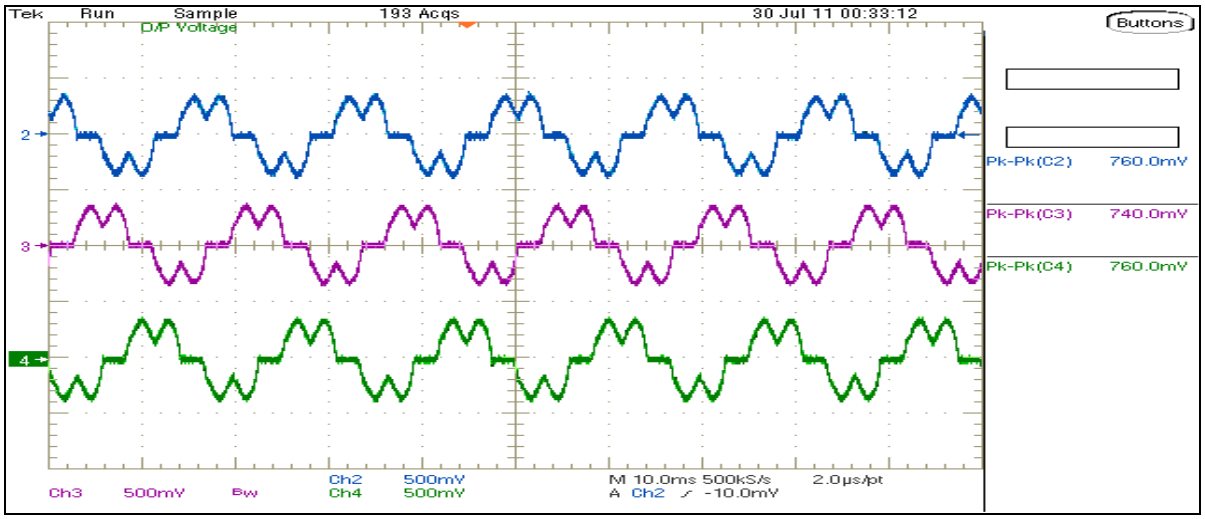

Figure 54.Oscilloscope waveform for Scaled I_{sa},$I_{sb,}$$I_{sc}$

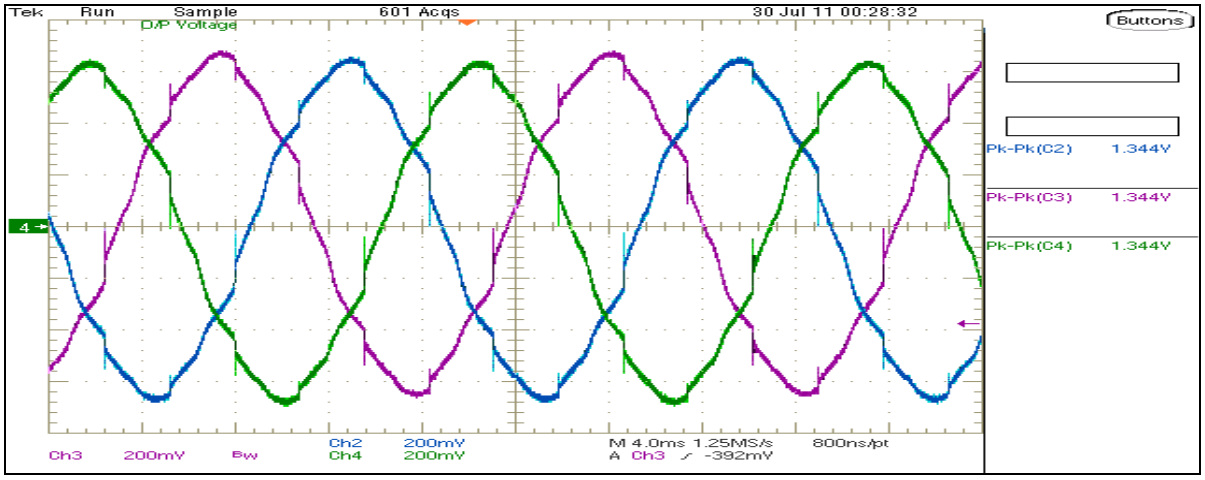

Figure 55.Oscilloscope Waveform for Scaled Three phase voltage V_{fa},V_{fb},V_{fc}

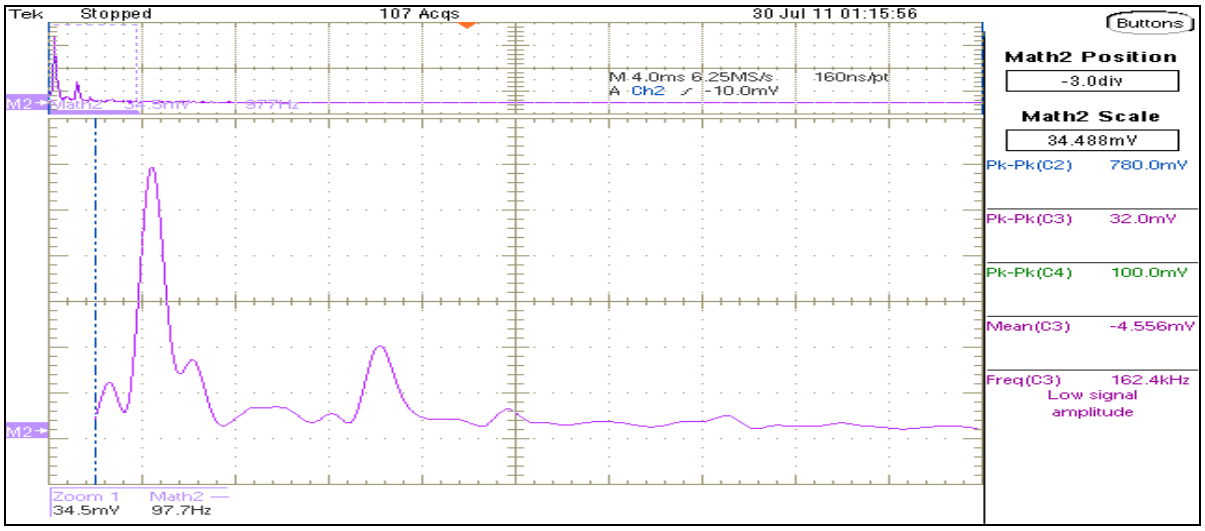

Figure 56.Fast Fourier Transform (FFT) of the I_{sa} waveform on oscilloscope

5.2 Harmonic Extraction on an Analog Board

The harmonic extraction board has been implemented on an analog board using integrated circuits. Three different harmonic extraction algorithms have been implemented namely V_f, Load Current and Supply current harmonic extraction method as discussed in chapter 3.The board receives the voltage and current signals measured from the nonlinear load system and gives out the extracted harmonics in αβ stationary reference frame and the three phase. These extracted harmonics become the reference for the current controller board. The schematic of the harmonic extraction board laid out using ORCAD Capture has been attached in Appendix A. Analog Device's AD2S100 chip has been used for the vector rotation from three phase to two phase synchronous reference frame. The Low Pass Filter used is MAX280 which is a 5^{th} order Butterworth filter. It has been set for a cutoff frequency of 9.14 Hz by choosing appropriate value of Resistance and Capacitance in the circuit. The Butterworth filters have a slower roll off towards the stop band and hence they require a higher order for a particular stop band specification [19].

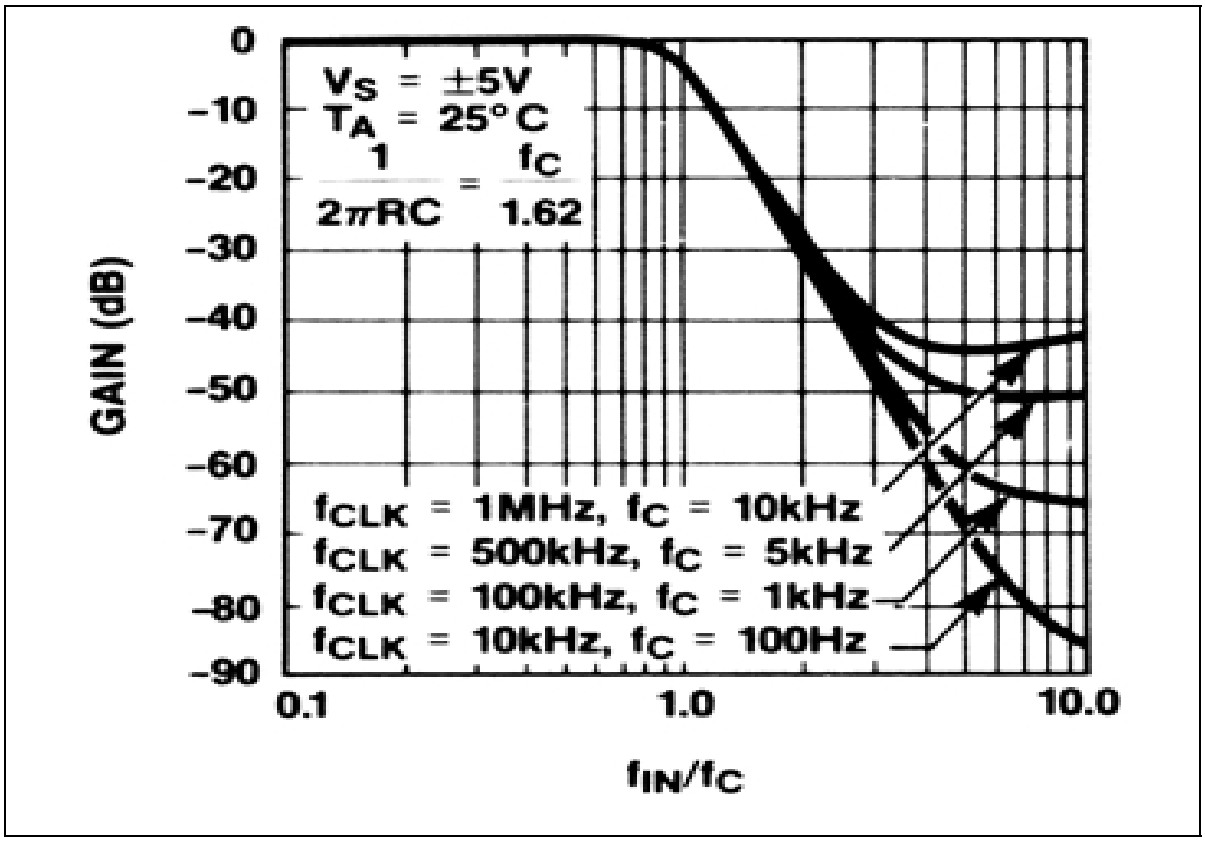

Figure 57.Magnitude Bode Plot of the 5th order Butterworth Filter (Gain Normalized to the Cut off Frequency) (Reproduced from MAX280 Datasheet)

5.2.a Implementation delay of Analog harmonic extractor

The analog harmonic extractor board has an implementation delay of 4.8µsec.The delay is measured by using the input currents I_{La} , I_{Lb}, I_{Lc} as the currents of 7th harmonic frequency. The extracted harmonic current should also be a 7th harmonic current of the same amplitude. The zero crossing of the output I_{hds} should ideally coincide with the zero crossing of the input current I_{La}.

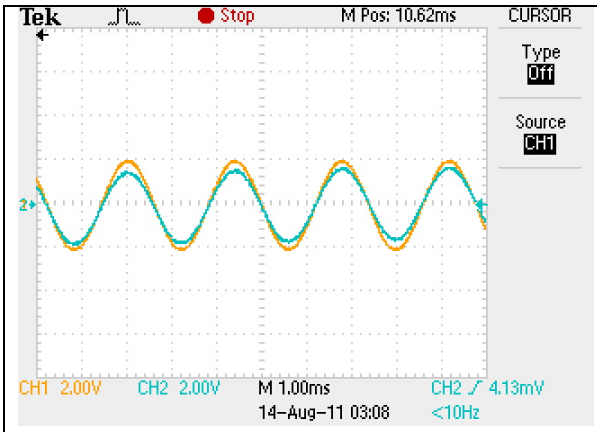

Figure 58.Oscilloscope waveform for I_{La}(yellow),I_{hds}(blue)

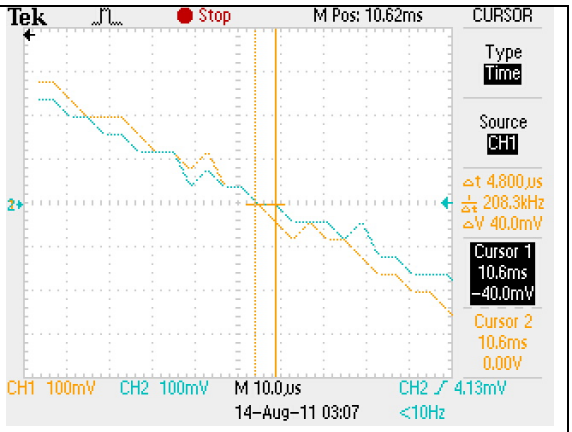

Figure 59.Zoomed Oscilloscope waveform for I_{La} (yellow),I_{hds}(blue) showing a delay of 4.8µsec

Clearly, the analog implementation of harmonic extractor is much faster than FPAA and FPGA implementations. Though, FPAA have an advantage of reconfigurability and ease of implementation.

5.2.b.i Load Current Harmonic Extraction Results

The Load current harmonic extraction method has been verified using all three types of loads discussed in section 5.1.

1. For Load type: AC Supply Side Line Inductor, Diode Rectifier with DC side Inductor, and DC side Capacitor system

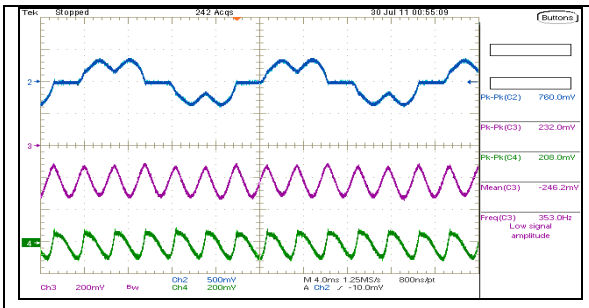

Figure 60.Oscilloscope waveform for i_{La}(blue), $i_d^e(pink)$, $i_q^e(green)$ for load type explained in section 5.1.c

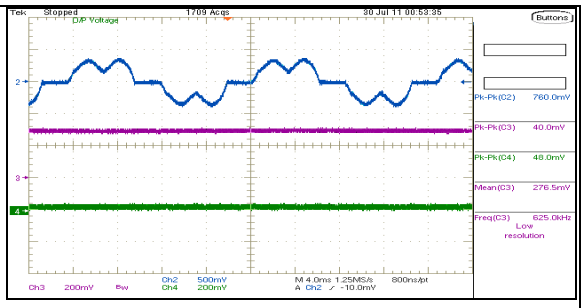

Figure 61. Oscilloscope waveform for i_{La} (blue), inverted low pass filtered i_d^e (pink), inverted low pass filtered i_q^e (green)

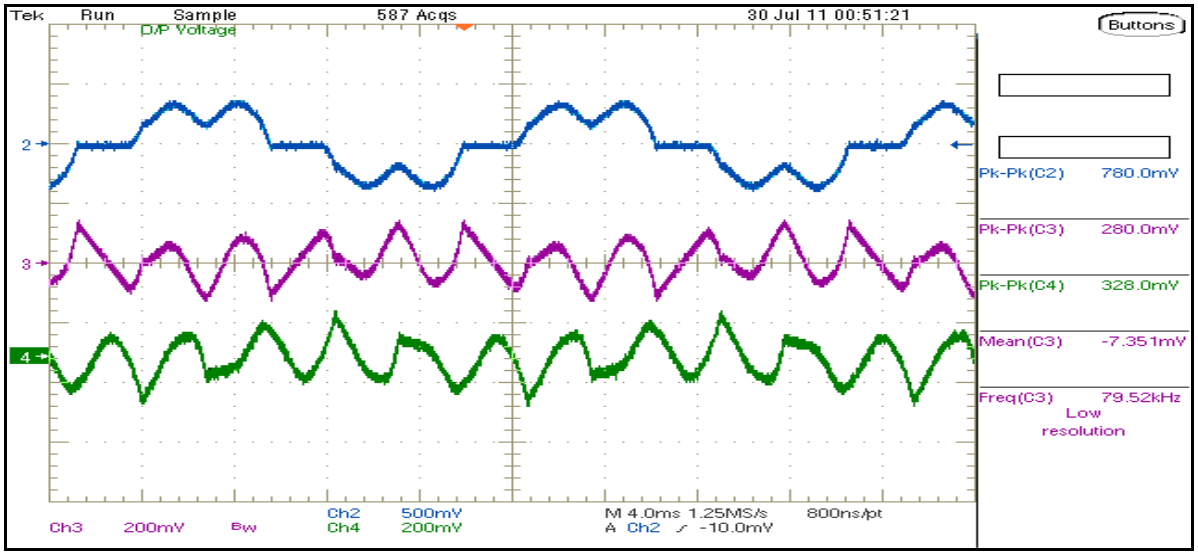

Figure 62.Oscilloscope waveform of i_{hd}^{s} (pink), i_{hq}^{s} (green) for load type explained in section 5.1.c

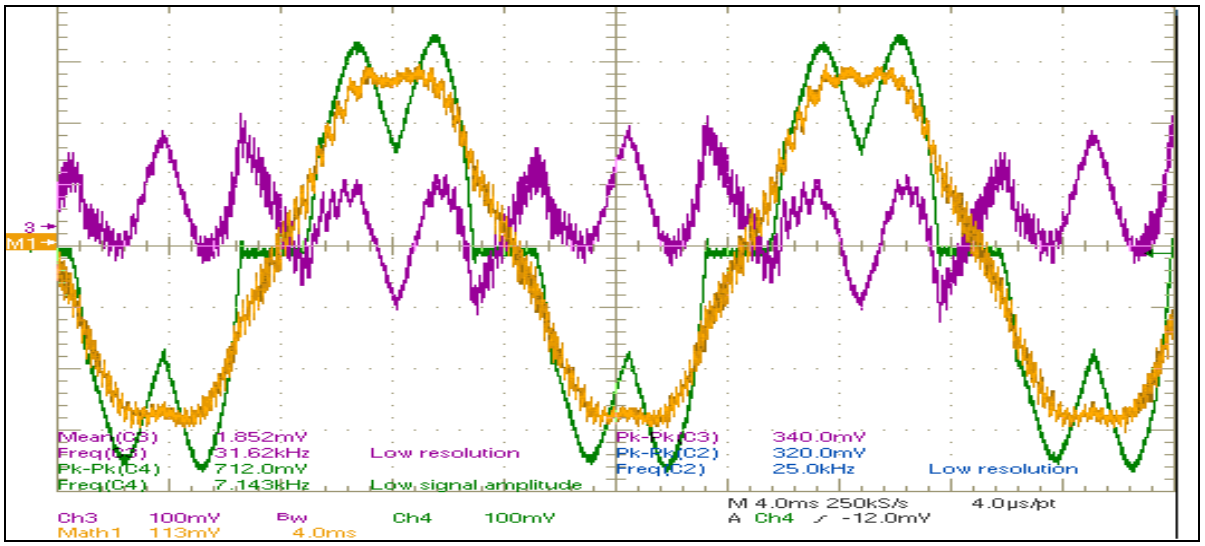

Figure 63. i_{hd}^{s} (pink),i_{fa}(green),i_{fa}-i_{hd}^{s} (yellow)

Figure 63 verifies that the harmonic extraction is taking place perfectly such that when the extracted harmonic is subtracted from the load current, it gives a sinusoidal current.

2. For Load type: AC Supply Side Line Inductor, Diode Rectifier with DC side Capacitor system

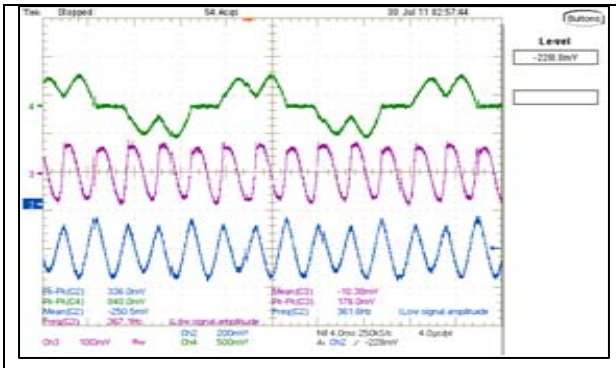

Figure 64.Oscilloscope waveform for i_{La} (green), i_d^e (blue), i_q^e (pink)for load type explained in section 5.1.b

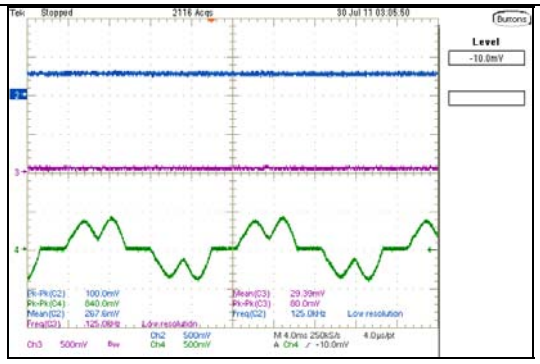

Figure 65.Oscilloscope waveform for i_{La} (green), inverted low pass filtered i_d^e (blue), inverted low pass filtered i_q^e (pink)

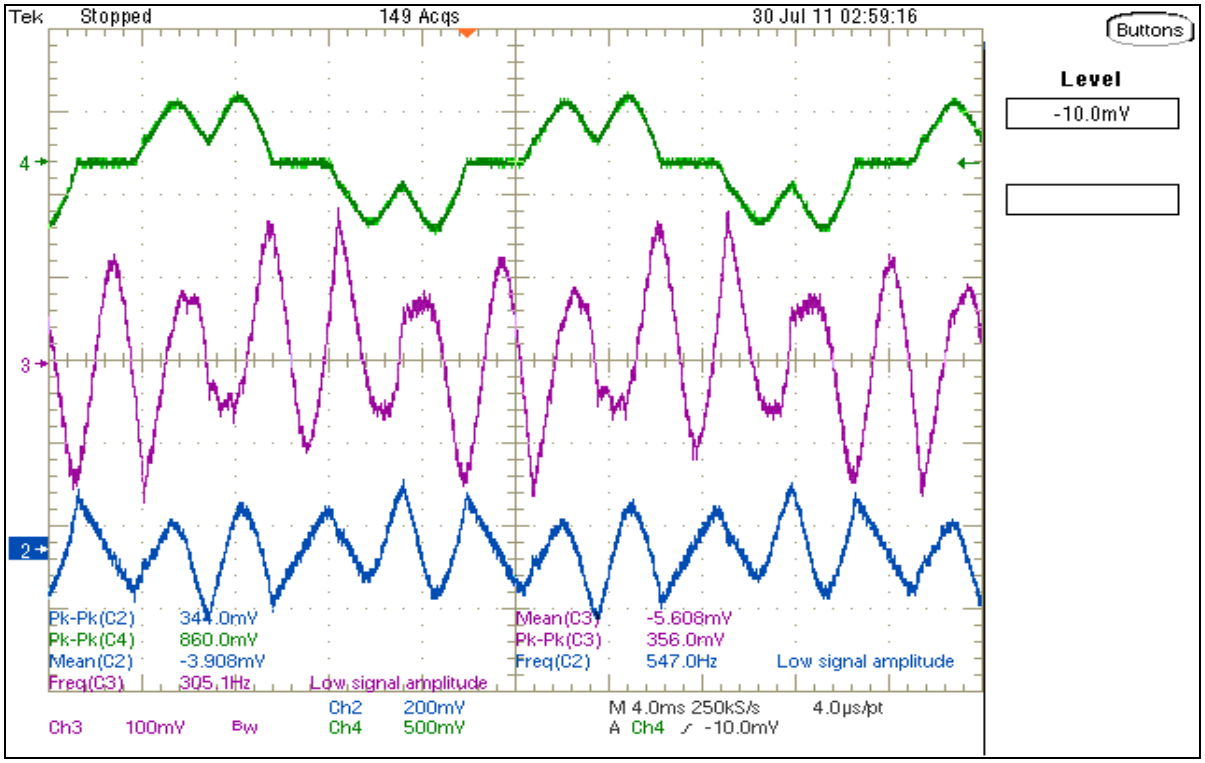

Figure 66. Oscilloscope waveform of i_{hd}^s (blue), i_{hq}^s (pink) for load type explained in section 5.1.b

3. For Load type: Diode Rectifier with DC side inductor and DC side Capacitor system

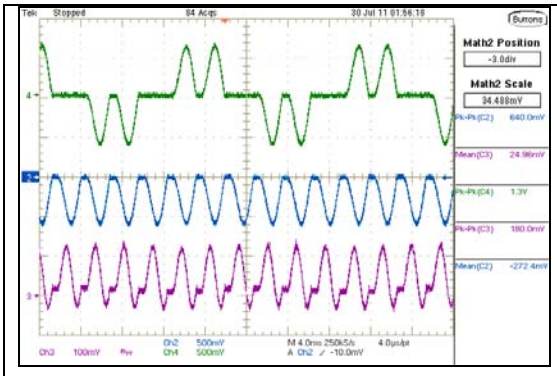

Figure 67. Oscilloscope waveform for i_{La} (green), i_d^e (blue), i_q^e (pink)for load type explained in section 5.1.a

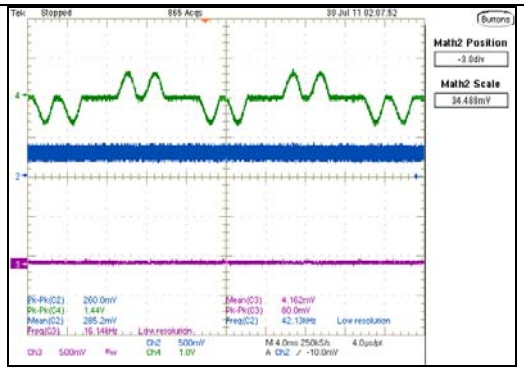

Figure 68. Oscilloscope waveform for i_{La} (green), inverted low pass filtered i_d^e (blue), inverted low pass filtered i_q^e (pink)

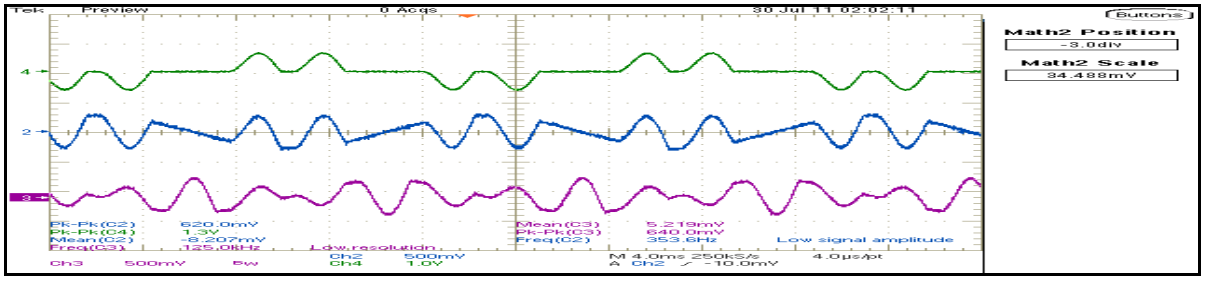

Figure 69. Oscilloscope waveform of i_{hd}^s (blue), i_{hq}^s (pink) for load type explained in section 5.1.a

5.2.b.ii Vf (Voltage at PCC) Harmonic Extraction Results

The Vf harmonic extraction method has been verified for the load type explained in section 5.1.c.

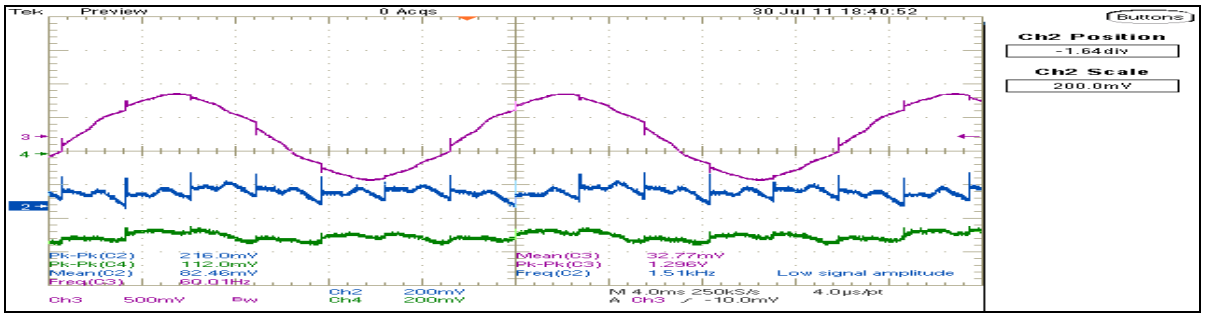

Figure 70.Oscilloscope waveform for V_{fa} (pink), V_d^e (green), V_q^e (blue)

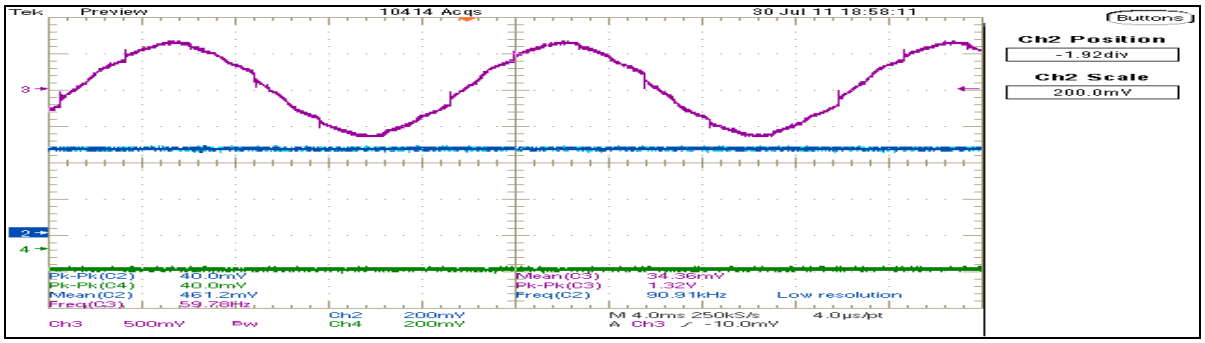

Figure 71. Oscilloscope waveform for V_{fa} (pink), inverted and filtered V_d^e (blue), V_q^e (green)

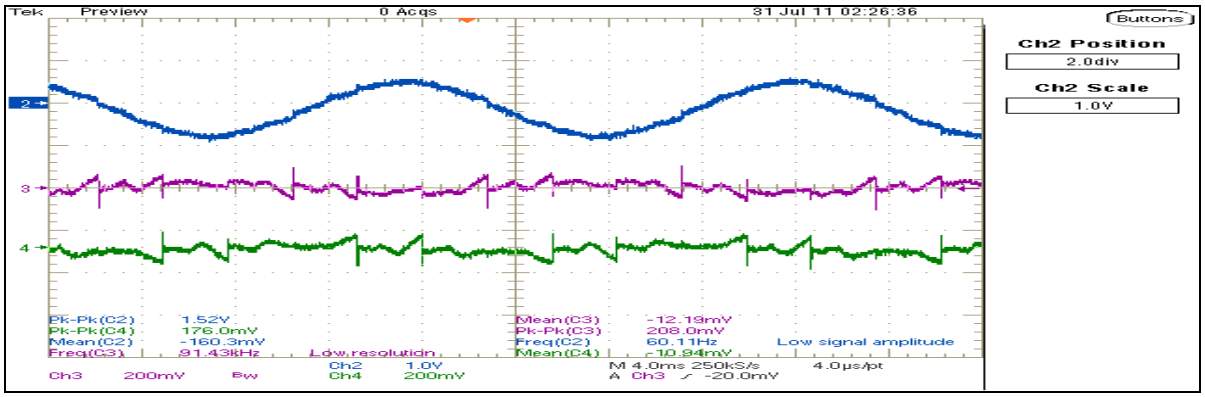

Figure 72. Oscilloscope waveform for V_{fa} (blue), V_d^s (pink), V_q^s (green)

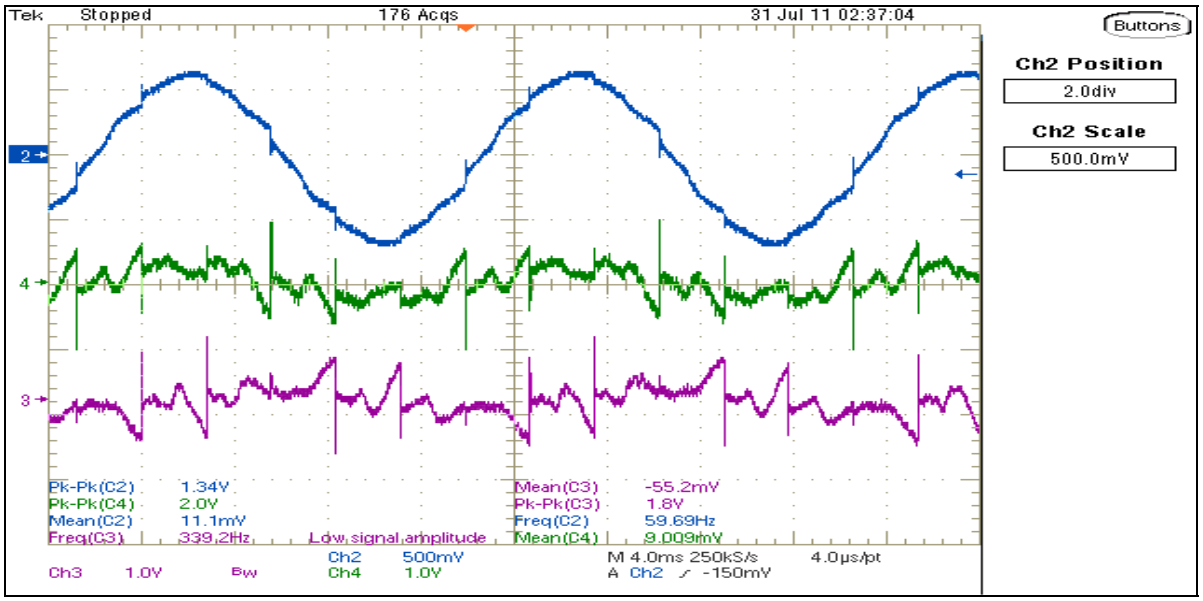

Figure 73. Oscilloscope waveform for V_{fa} (blue), i_{hd}^s (green), i_{hq}^s (pink)(for K_v=10)

5.2.b.iii Supply Current Harmonic Extraction Method Results

The Supply Current Harmonic Extraction method has been verified on the Analog Board for the load of type discussed in section 5.1.c

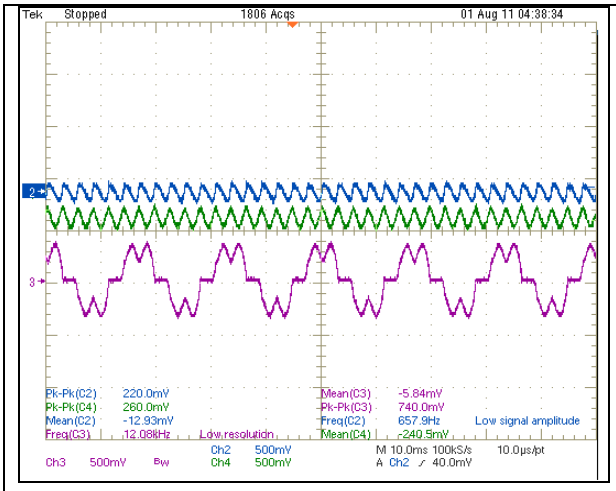

Figure 74. Oscilloscope waveform for i_{sa} (pink), $i_{sd}^{e}(green), i_{sq}^{e}(blue)$

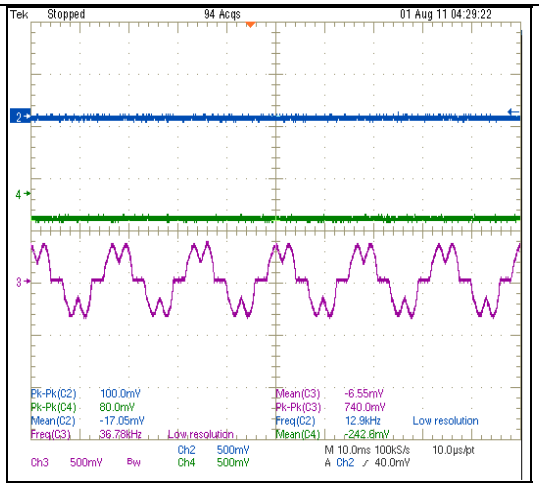

Figure 75. Oscilloscope waveform for i_{sa} (pink), inverted low pass filtered i_{sd}^{e} (green), inverted low pass filtered i_{sq}^{e} (blue)

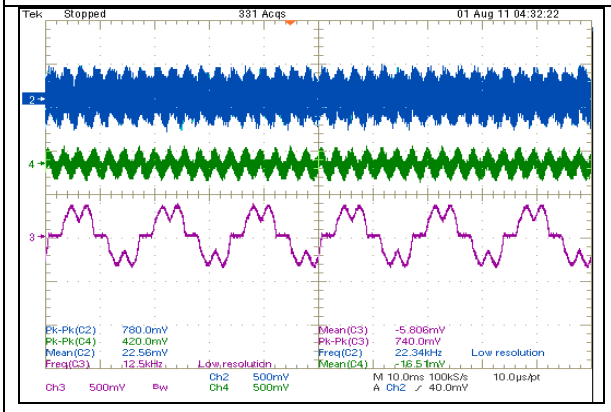

Figure 76.Oscilloscope waveform for i_{sa} (pink) , i_{sd}^{e} (green) after gain $G(s)=\frac{(KT)s}{1+(KT)s}$, i_{sq}^{e} (blue) after gain $G(s)=\frac{(KT)s}{1+(KT)s}$,K=5,T=$10^{-3}$

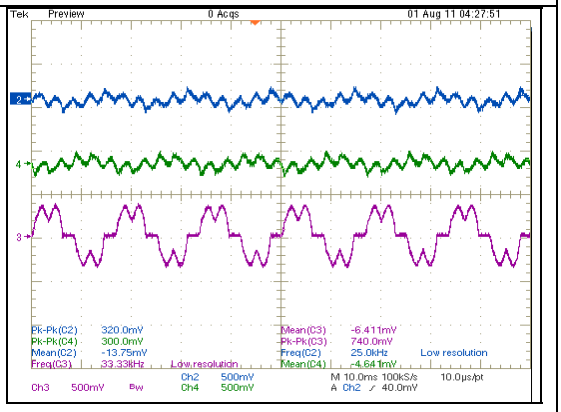

Figure 77.Oscilloscope waveform for i_{sa}(pink), i_{hd}^{s} (green), i_{hq}^{s} (blue)

5.3 Predictive Current Controller Implementation on Analog Board

The Predictive current controller logic has been tested by using harmonic extraction from load current harmonic extraction method as the reference. Currently, for testing the predictive current controller logic, the measured active filter inverter currents, i_{fqs} and i_{fds} are made zero. V_{fd}^{s} and V_{fq}^{s} (V_f in αβ reference frame) are also supplied from harmonic extractor board. The Switching frequency for this implementation is 20kHz.The Active Filter Inductance, L_f is designed for 150μH, so that the gain:

$$\frac{L_f}{\frac{T_{sw}}{2}} = 6$$

In this implementation, compensation has been provided for sampling and inverter dead time delays. For this reason, the triangular waveform has been delayed by a time=3μsec (sampling delay+ dead time delay) from the time at which the sampling starts. For the purpose of implementing the current tracking at every half of switching period ($T_{sw}/2$), two sample and hold pulses are produced, one being delayed by $T_{sw}/2$ from the other as shown in Figure 82. They are then multiplexed every $T_{sw}/2$ for implementing current tracking every $T_{sw}/2$.The sample and hold pulses are produced from the comparator output in the triangular wave generation circuit as shown in Appendix B. This is done such that sample and hold pulses are synchronized with the triangular waveform.

Following oscilloscope waveforms validate the correctness of the logic.

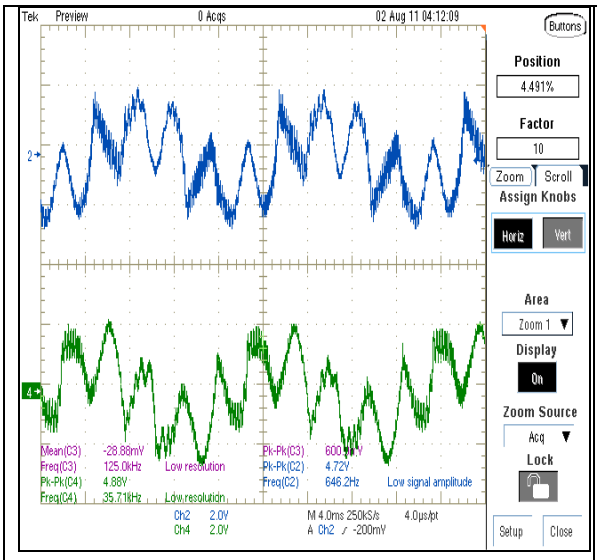

Figure 78. SV^{*}_{invds} (blue), SV^{*}_{invqs} (green)(Active Filter inverter reference voltages for SVPWM)

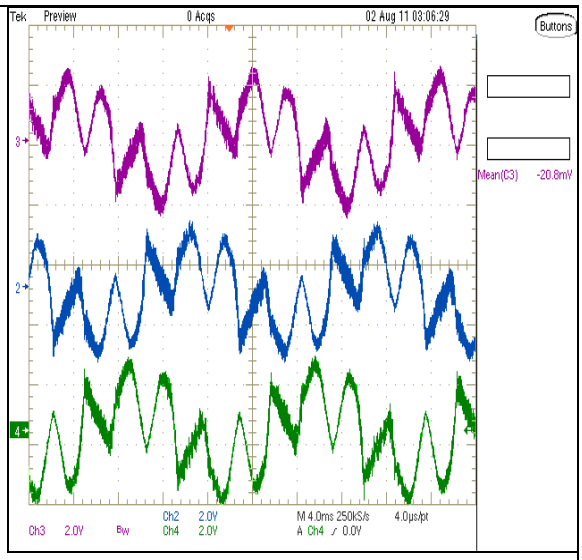

Figure 79. V^{*}_{invan} , V^{*}_{invbn} , V^{*}_{invcn} (Three phase active filter inverter reference voltage for SVPWM)

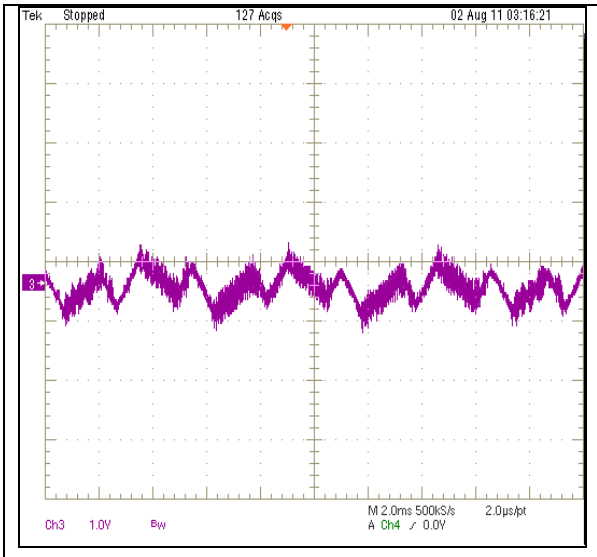

Figure 80.Triplen extraction for the SVPWM technique

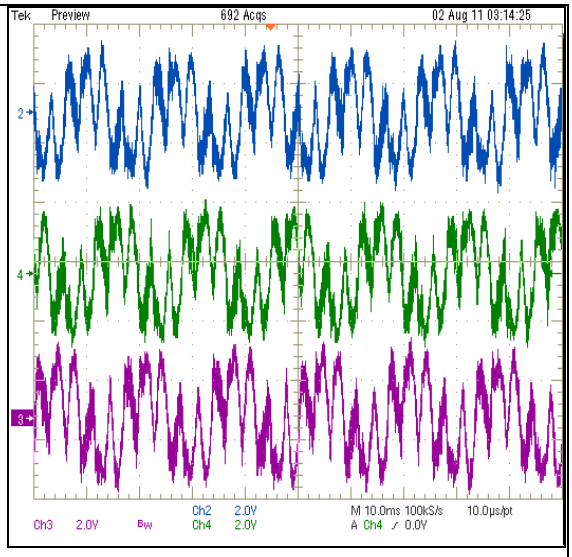

Figure 81.V_{amod},V_{bmod} , V_{cmod} (Three phase modulating voltages for comparing with triangular waveform)

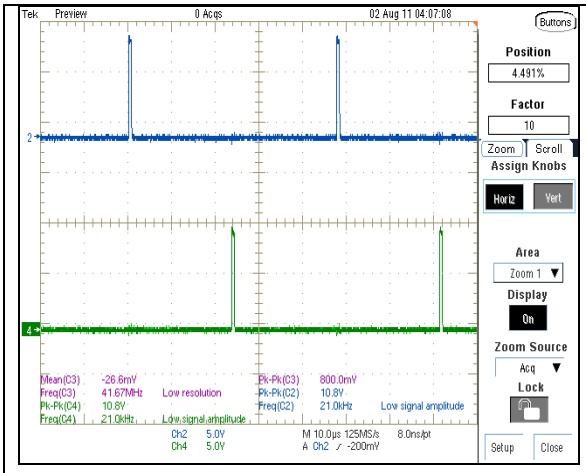

Figure 82.Sample and Hold(S/H) Pulses; S/H at T_{sw}(blue),S/H at T_{sw}/2(green)

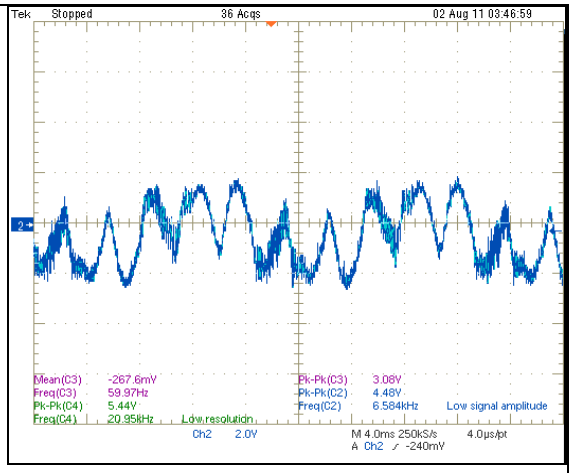

Figure 83.V_{amod} after sample and hold operation

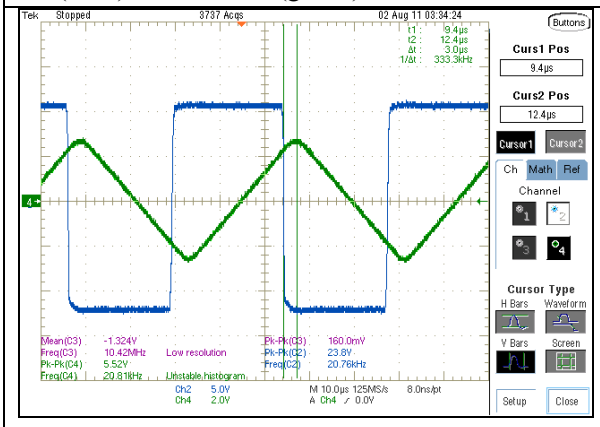

Figure 84.Delayed triangular waveform(delayed by 3µsec from the sampling pulse for inverter dead time compensation)

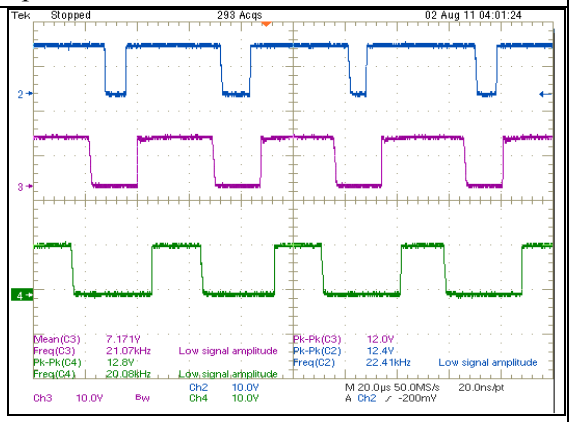

Figure 85.Inverter pulses for switches S1(blue),S3(pink) and S5(green)

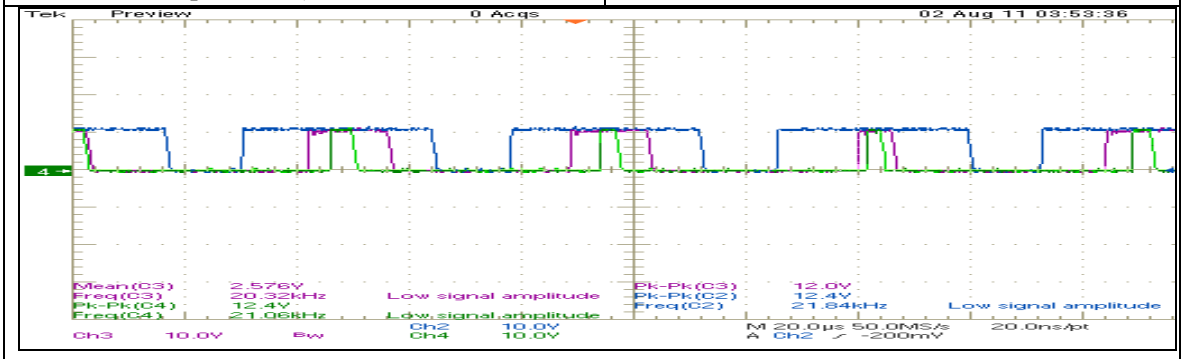

Figure 86.Inverter pulses S1,S3,S5 enclosed in one another in 0127-7210 order and showing the SVPWM operation

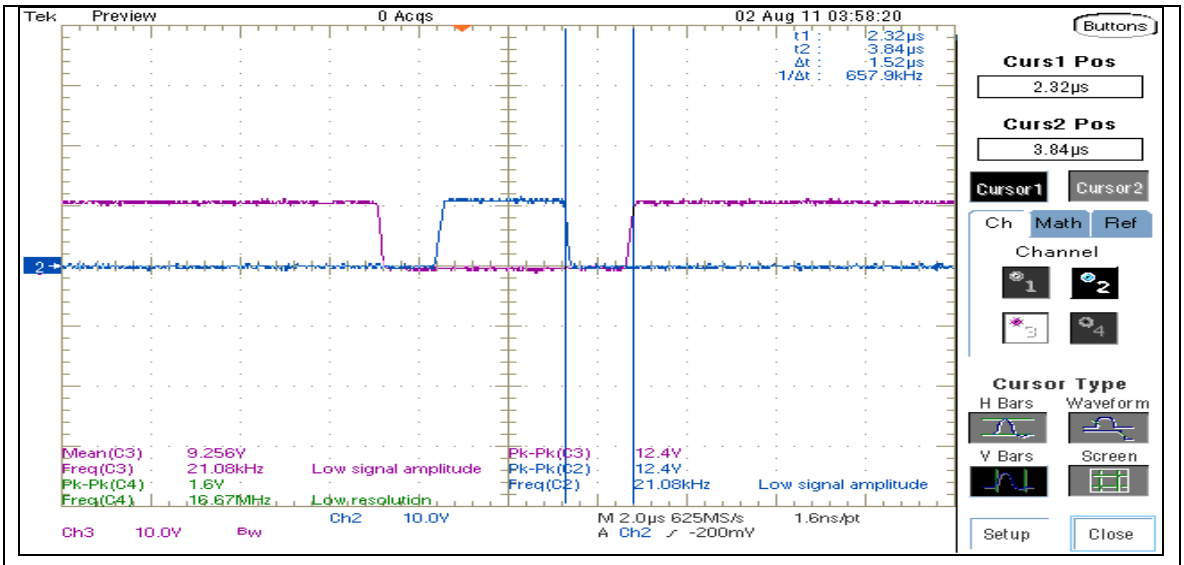

Figure 87.Inverter dead band given to S1 and S2 pulses

5.4 Active Filter Inverter System

In this work, the active filter inverter has been driven using six pulses from predictive current controller in open loop. For driving the active filter inverter in open loop RL load has been used. The specifications of each component of this system are:

L_f =150µH

C_f =50µF

R_{load} =50Ω

Figure 88 shows the schematic of the active filter inverter system implemented in lab. Figure 89 shows the experimental setup of the active filter inverter system.

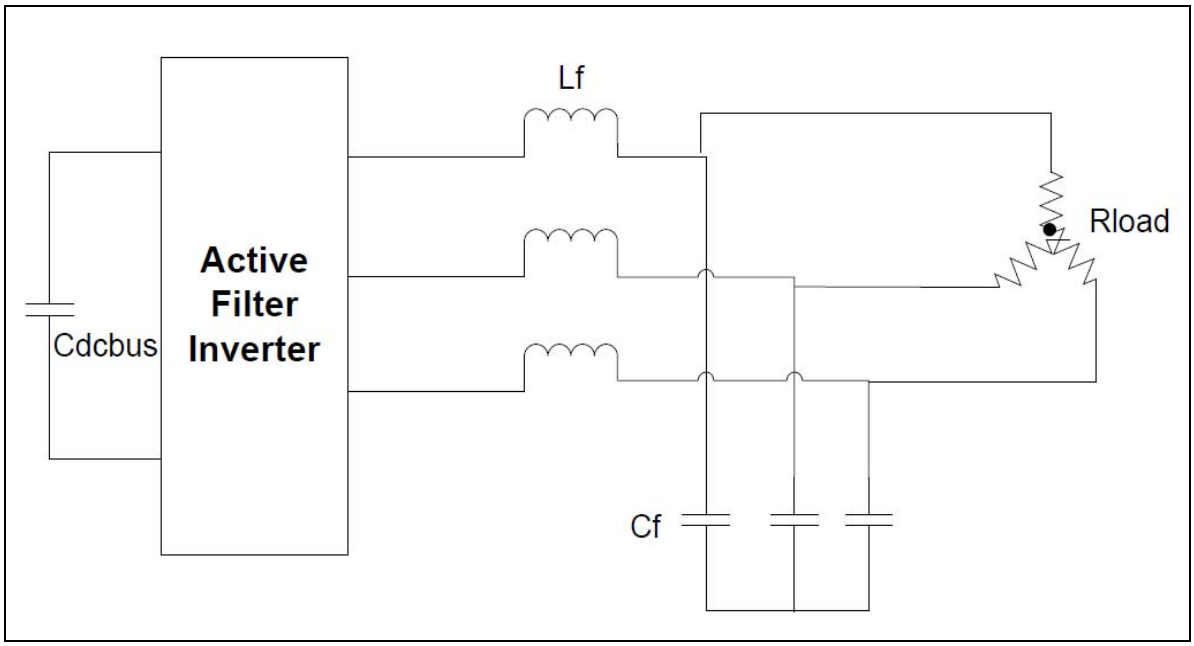

Figure 88. Schematic of the active filter inverter system implemented in lab.

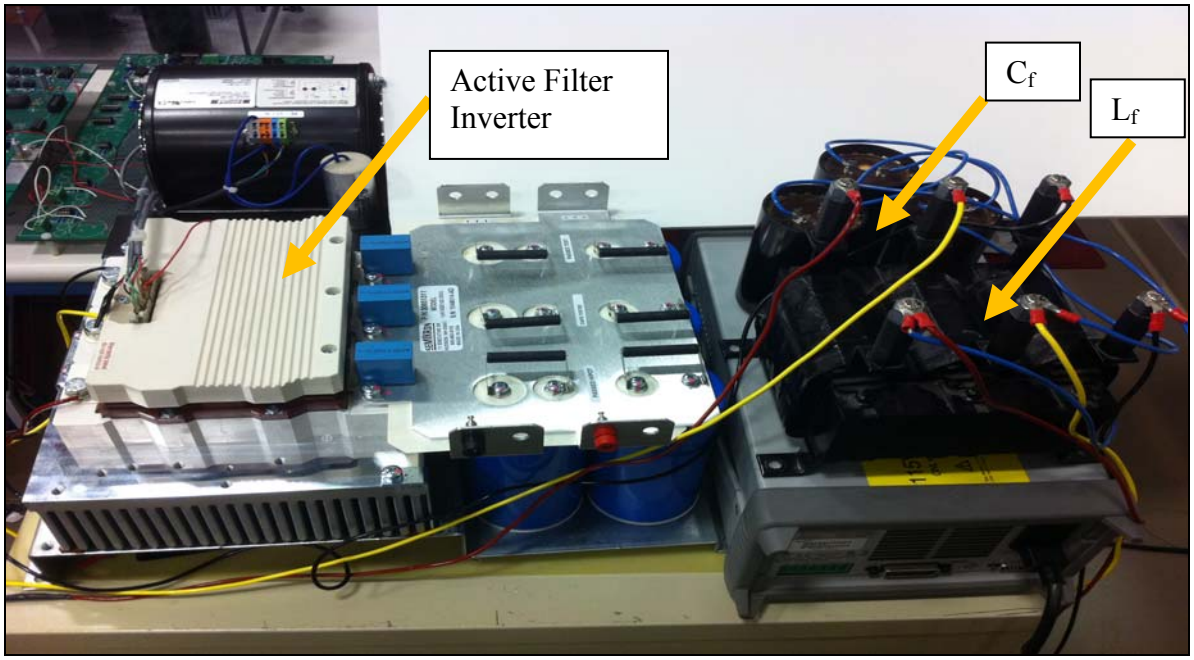

Figure 89. The experimental setup of the active filter inverter system

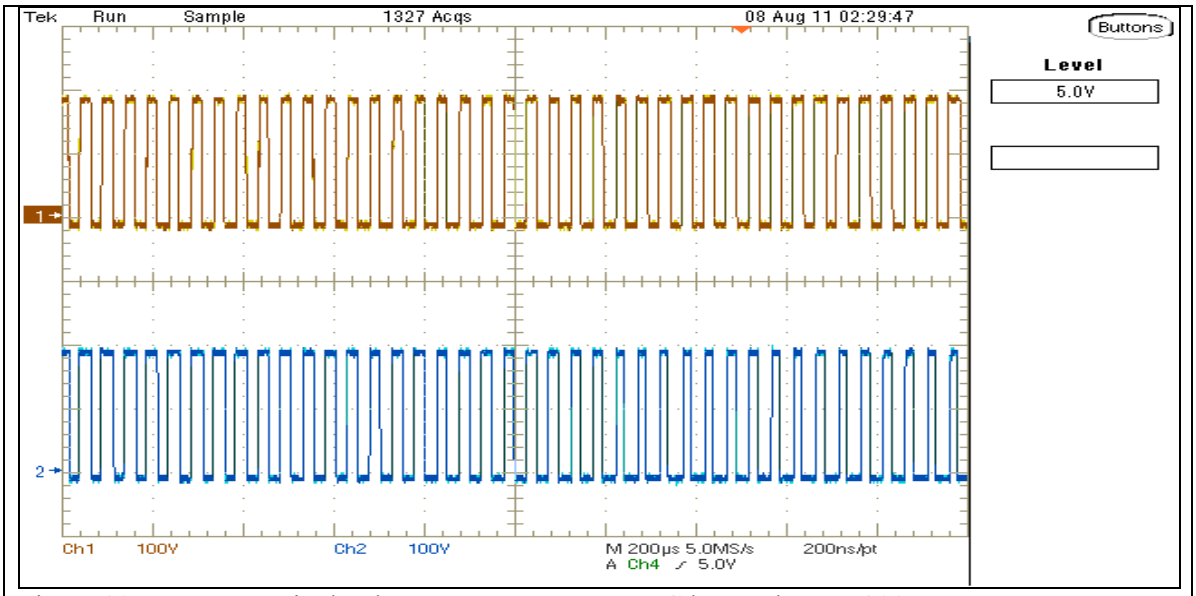

Figure 90.Inverter terminal voltages; V_{invan} , V_{invbn} at DC bus Voltage = 200V

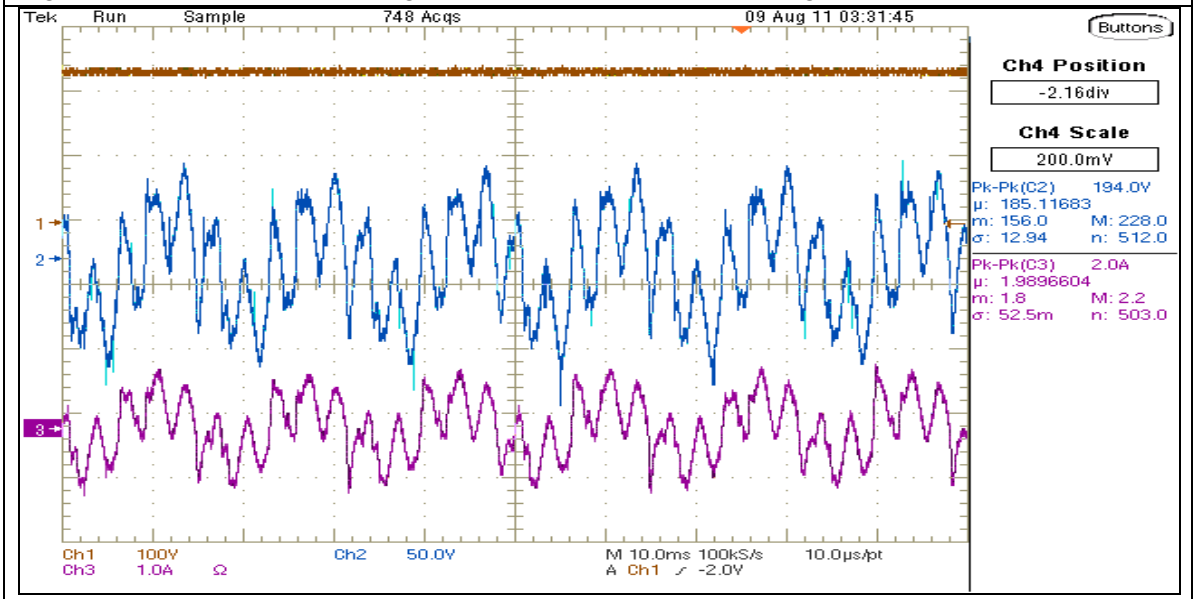

Figure 91.DC bus Voltage(at 250V)(brown),Voltage across load(l-l)(blue),Ifa(pink)

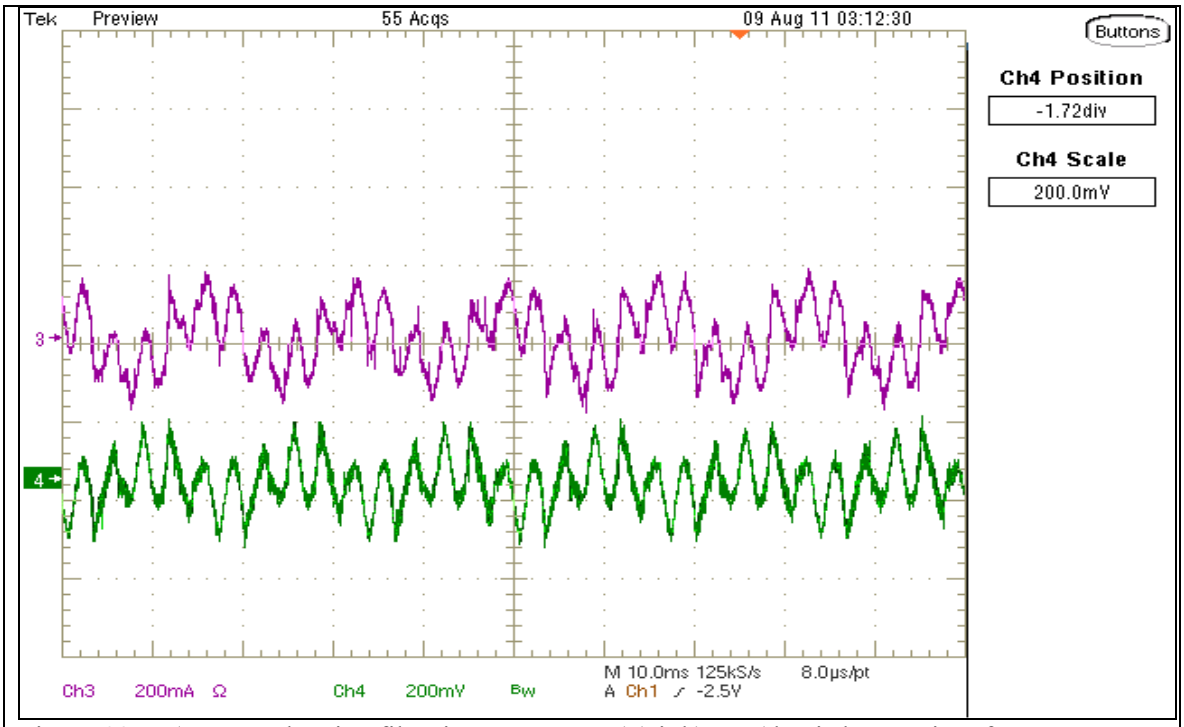

Figure 92.I_{fa} (measured active filter inverter current)(pink),I_{hds} (d axis harmonic reference current)(green)

From figure 92, it is clear that the compensating current produced at the active filter inverter terminals exactly matches with the reference current which proves that the predictive current controller works perfectly.

5.4 Summary

In this chapter three types of nonlinear loads have been considered and analyzed based on their current and voltage wave shapes. These nonlinear loads are used for testing three different harmonic extraction methods namely V_f (Voltage at PCC), Load current and Supply Current harmonic extraction method. All the methods have been verified to work correctly. The harmonics extracted from the load current harmonic extraction method have been used as reference for the predictive current controller which is verified to give the desired pulses to drive the active filter inverter at a

switching frequency of 20 kHz. Also, the compensation for sampling and inverter dead time delays has been provided in the analog implementation of predictive current regulator.

An Active Filter inverter has been driven in open loop using RL load at a switching frequency of 20 kHz by the six pulses from predictive current controller generating the compensating current. It has been verified that the compensating current exactly matches with the reference harmonic current.

CHAPTER 6.CONCLUSION

This thesis work has been aimed at comparing different harmonic extraction algorithms for active filter controller implementation. Three harmonic extraction methods have been verified using simulation results. All the three harmonic extraction methods have been shown to reduce THD below 12% (Ls=22µH, SCR=50-100) and hence they conform to the IEEE 519 harmonic standards. From the simulation results, in terms of achieving lower THD, V_f harmonic extraction method (THD=3.34%) proves to be better than the load current harmonic extraction (THD=3.82%) and supply current harmonic extraction (THD=6.24%) method.

Though, from the comparison between the three methods, it has been found that each method has its own specific use. All the methods can provide a good harmonic compensation but it depends upon the need of the system (in terms of requirement of harmonic damping or compensation of harmonics present due to supply voltage) to be able to choose which method to use.

The harmonic extractor board developed in the laboratory has been verified to extract harmonics using all three harmonic extraction algorithms. It has been verified that the subtraction of extracted harmonic from the load current will result in a fundamental current. These harmonics so extracted were then sent as the reference signals to the current controller board.

This thesis work also shows the analog implementation of the predictive current controller. The experimental results prove the correctness of the logic and produces desired pulses using Space Vector PWM technique. In the predictive current regulator, dead time compensation (3µsec) has also been performed in order to remove the effect of sampling and inverter dead time delay on PWM pulses and hence on the inverter output.

An Active Filter inverter has been driven in open loop using RL load at a switching frequency of 20 kHz by the six pulses from predictive current controller generating the compensating current. It has been verified that the compensating current exactly matches with the reference harmonic current.

As the active inverter has a high bandwidth, therefore there is a need to switch these inverters at a very high frequency. Therefore, there is a need to reduce the delay in the controller implementation.

The positive sequence Synchronous Reference Frame controller has been implemented on both Field Programmable Analog Array (FPAA) and Field Programmable Gate Array (FPGA).Seven Anadigm's AN231E04 development boards have been used for the implementation on FPAA. For the implementation on FPGA, NI-CRIO has been used. The FPAA implementation proves to be faster with a delay of 17.4μsec as compared to the FPGA implementation which has a delay of 30μsec.

Though, the analog board implementation of harmonic extractor has an implementation delay of 4.8μsec, still they are complicated to implement and are not reconfigurable.

Thus, FPAA implementation can prove to be a potential method for switching SiC inverters at a very high frequency 50-100kHz along with being reconfigurable and easy to implement.

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