ABSTRACT

ASOKAN, PRIYADARSHINI. Field Programmable Analog Array Implementation of Active Filter Controller. (Under the direction of Subhashish Bhattacharya).

There is a need for Active Filter inverters to be switched at very high frequencies in order to match the harmonic requirement of the load. The next generation of Active Filters using Silicon Carbide (SiC) can achieve switching frequencies as high as 50-100KHz. For such devices, there is a need for a high speed controller which can be used to switch the inverter at these high speeds.

Current methods of designing Active Filter controllers include design of analog chips of using FPGAs and DSP. These methods involve much time in processing the signals.

In this research, FPAAs were considered for the controller, because of their simple method of design and flexibility. It was expected that the FPAA would be faster than conventional methods of designing the Active Filter Controller.

The PQ theory, one type of Active Filter Controller, was implemented on four FPAA chips and compared to the implementation on FPGA chips. The FPAAs were indeed faster than the FPGA implementation by 97.7%. Thus, FPAAs could potentially be an alternative to current methods.

Field Programmable Analog Array Implementation of Active Filter Controller

by
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APPROVED BY:

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Subhashish Bhattacharya
Committee Chair

DEDICATION

To my parents and my brother.

BIOGRAPHY

Priyadarshini Asokan was born on November 3, 1989 in Tamil Nadu, India. She moved to the United States with her parents at the age of 3. Her family spent the first few months in Boston, Massachusetts, before making the move to Cary, North Carolina.

After graduating from Enloe High School in 2006, Priya attended North Carolina State University (NCSU) for her undergraduate degree. At the end of her sophomore year, Priya was inducted into the Phi Kappa Phi and Eta Kappa Nu Honor Societies. Also during her time at N. C. State, Priya co-founded NCSU's first service sorority, Omega Phi Alpha. In May 2010, she graduated from NCSU as a Valedictorian with a Bachelor's Degree in Electrical Engineering.

Priya continued her graduate studies at North Carolina State University as a part of the Accelerated Bachelor's/Master's (ABM) Program. She joined the NSF funded Future Renewable Electric Energy Delivery and Management (FREEDM) Center in June, 2010. There she is performing research under the advising of Dr. Subhashish Bhattacharya.

ACKNOWLEDGEMENTS

First and foremost, I would like to thank my advisor, Dr. Bhattacharya, for his guidance and endless support throughout this research. I would also like to thank the other committee members Dr. Griff Bilbro and Dr. W. Rhett Davis for their suggestions and willingness to help.

I would like to acknowledge and thank my fellow graduate students, Misha Kumar and Eric Green for their valuable help. Misha, thank you for your support throughout the course of this research. Eric, without your help with the C-RIO, I could not have achieved my goals for this research.

Last, but not least, I would like to thank my parents for their love and for supporting me every step of the way.

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1 INTRODUCTION

When multiple harmonics are present in the supply current, the bandwidth requirement of an active filter increases. These harmonics occur because of the presence of power electronic loads like adjustable speed drive with diode bridge front ends. Hence, there is a need for the Active Filter inverter to be switched at very high frequencies in order to match the harmonic requirement of the load.

The next generation of Active Filters which make use of Silicon Carbide (SiC) can achieve switching frequencies as high as 50-100KHz. For such devices, there is a need for a high speed controller which can be used to switch the inverter at these high speeds. Hence, the motivation for this research was to achieve a faster controller than current methods.

The controller can be designed using analog chips. However, this method is highly design intensive and lacks flexibility. Alternatively, the controller can be designed in the digital domain, which would involve the use of Field Programmable Gate Arrays (FPGAs) and Digital Signal Processing (DSP). The disadvantage of this method is that it involves a long processing time. In order to receive, process, and transmit signals, Analog to Digital and Digital to Analog converters are required.

In this research, the high speed controller has been attempted using Field Programmable Analog Array (FPAA) chips. FPAAs are very simple to design and very flexible. FPAAs can be configure and reconfigured in a matter of seconds. Also, the use of FPAAs requires minimum hardware, requires lower power, and is highly reliable compared to the previously discussed digital option. (Dong, 2006)

1.1 THESIS ORGANIZATION

Chapter 1 is the introduction and provides the motivation behind the research. Chapter 2 described the background and theory of Active Filters and PQ theory. Chapter 3 provides an overview of FPAAs. The implementation of the PQ theory using FPAA chips is described in detail in Chapter 4. In Chapter 5, the implementation on the Compact-RIO is explained. Chapter 6 compares the implementation using FPAA chips with the implementation on the Compact-RIO. Lastly, Chapter 7 states the conclusions drawn from the research and suggests directions for future work.

2 BACKGROUND

This chapter describes the theory of Active Filters and PQ Theory.

2.1 SHUNT ACTIVE FILTER

The shunt Active Filter generates currents to compensate for the un-desirable current components in the load current. For various non-linear loads in the power system, the input current quality can be polluted with harmonics. The Active Filters are used to supply the compensating harmonic requirements of the load allowing the supply current to be free of harmonics. (Akagi, Watanabe, & Aredes, 2007) The overview of the shunt Active Filter is shown in **Figure 2.1**.

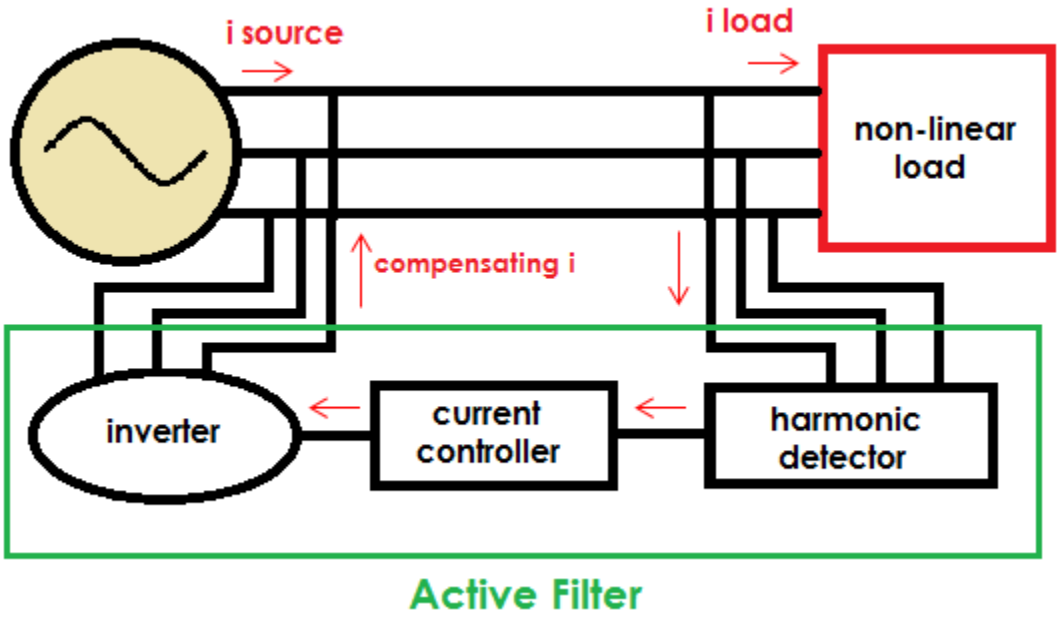

FIGURE 2.1 SHUNT ACTIVE FILTER

The shunt active filter consists of a harmonic detector, current controller and an inverter. The inverter operates in a current regulated Pulse Width Modulated (PWM) mode. The harmonic detector is extracting the harmonics from the load current and shows what the compensator current should look like. The current controller produces the pulses for the inverter. And finally, the pulses fire the gates of the switches in the inverter to produce the compensating current.

An open loop circuit is shown below in **Figure 2.2**. The waveform of the source current for this circuit is shown in **Figure 2.3**. The figure shows that the source current contains harmonics because of the load.

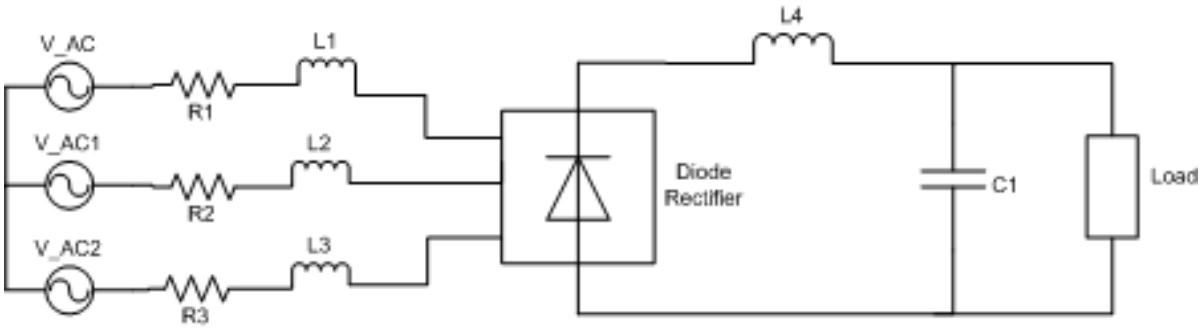

FIGURE 2.2 OPEN LOOP CIRCUIT (NO ACTIVE FILTER)

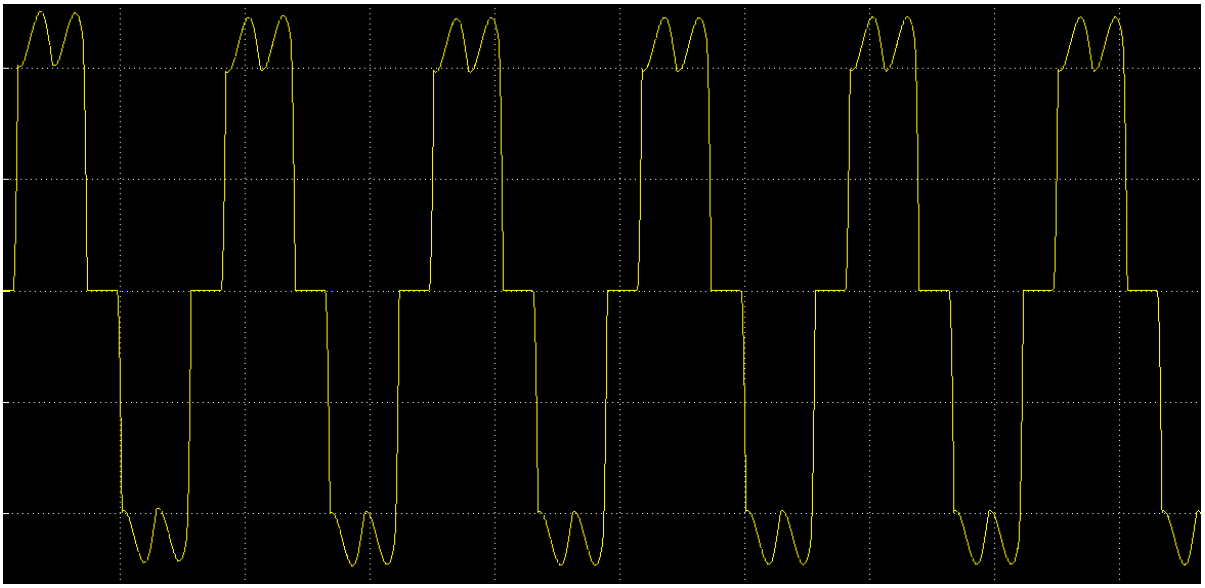

FIGURE 2.3 SOURCE CURRENT OF OPEN LOOP CIRCUIT

The harmonic spectrum of the source current for the open loop circuit is shown in **Figure 2.4**. IEEE 519 standard states that total harmonic distortion should be less than 5%. In the spectra above, the total harmonic distortion is much greater than 5%, at 28.71%.

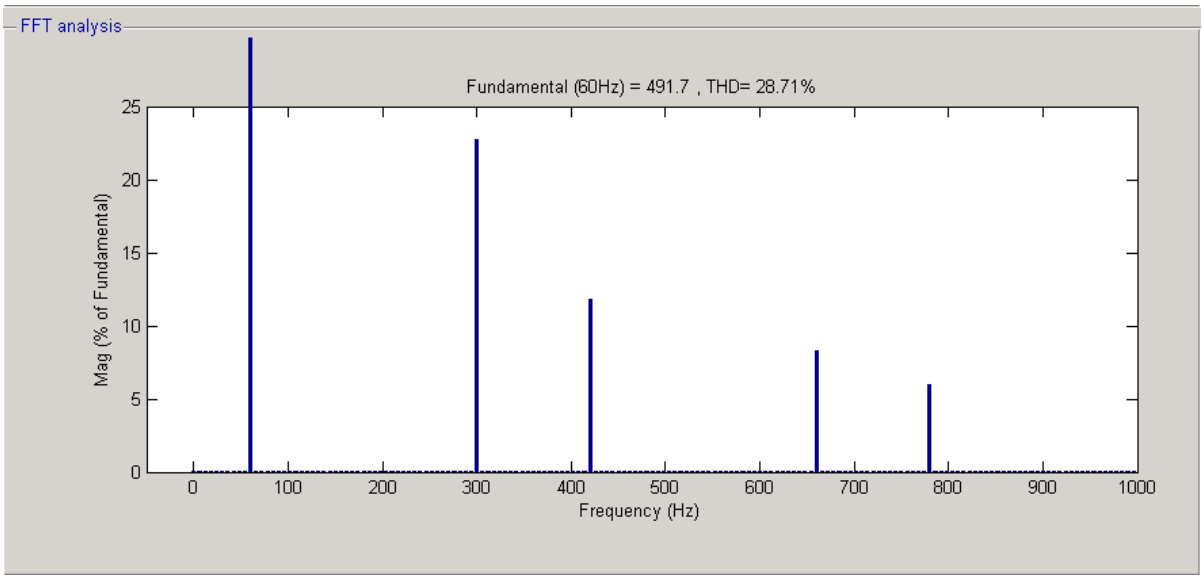

FIGURE 2.4 HARMONIC SCPECTRUM OF SOURCE CURRENT IN OPEN LOOP CIRCUIT

In order to precisely compensate for the high frequency harmonics, the bandwidth requirement of the inverter increases. To better compensate for these harmonics, the inverter requires a high switching speed.

Now, an active filter has been added to the circuit from **Figure 2.2**. The closed loop circuit is shown in **Figure 2.5**.

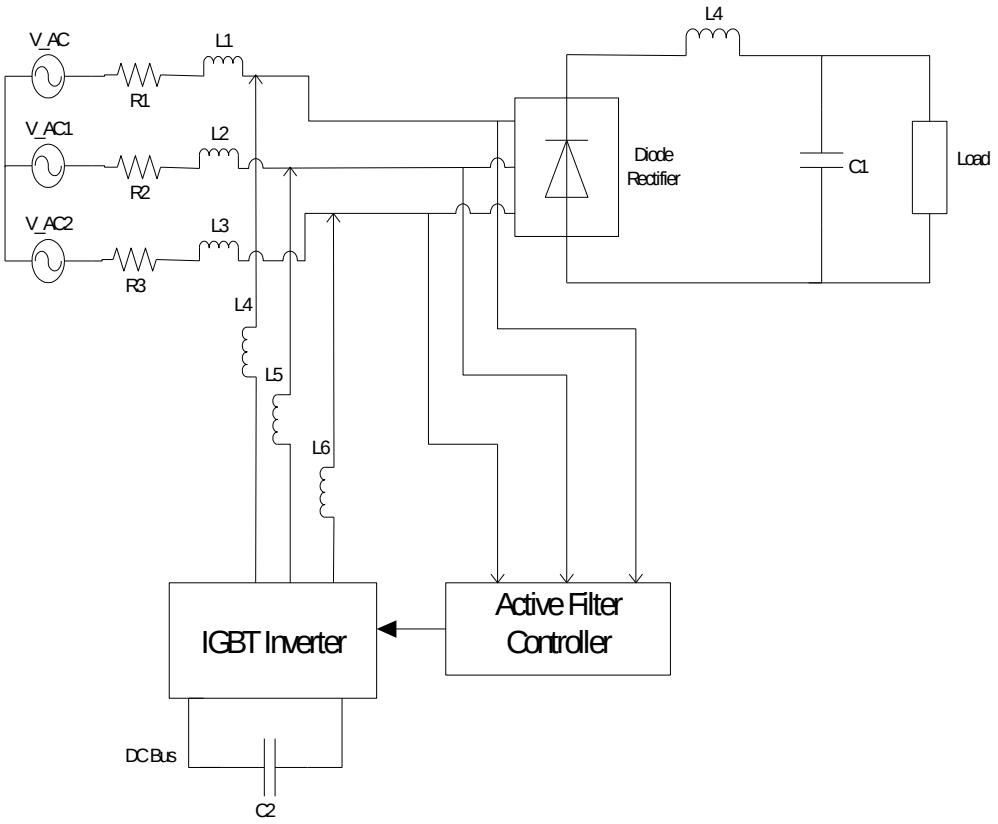

FIGURE 2.5 CLOSED LOOP CIRCUIT (ACTIVE FILTER)

The waveform of the source current in the closed loop circuit is shown in **Figure 2.6**. Compared to **Figure 2.3**, the source current now contains much less harmonics with the presence of the Active Filter.

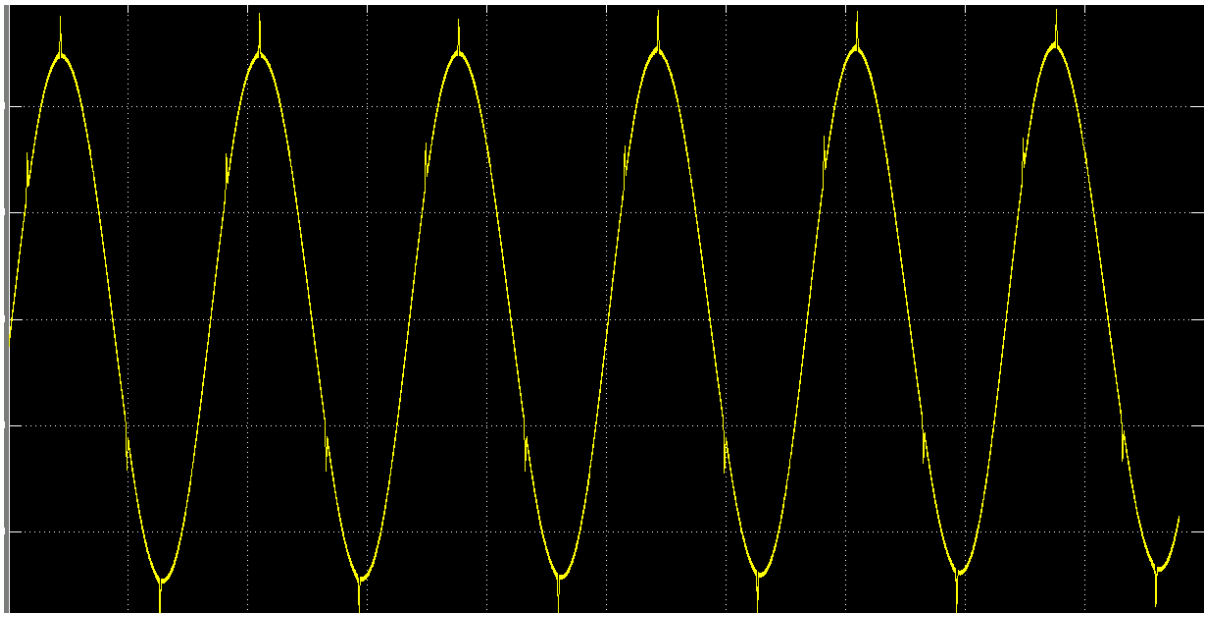

FIGURE 2.6 SOURCE CURRENT OF CLOSED LOOP CIRCUIT

The Harmonic Spectrum of this new source current is shown in **Figure 2.7**. The total harmonic distribution is now 2.64%. This complies with the IEEE 519 standard mentioned above. The compensating current produced by the Active Filter is shown in **Figure 2.8**. This compensating current is what must be produced by the active filter in order for the source current to contain fewer harmonics.

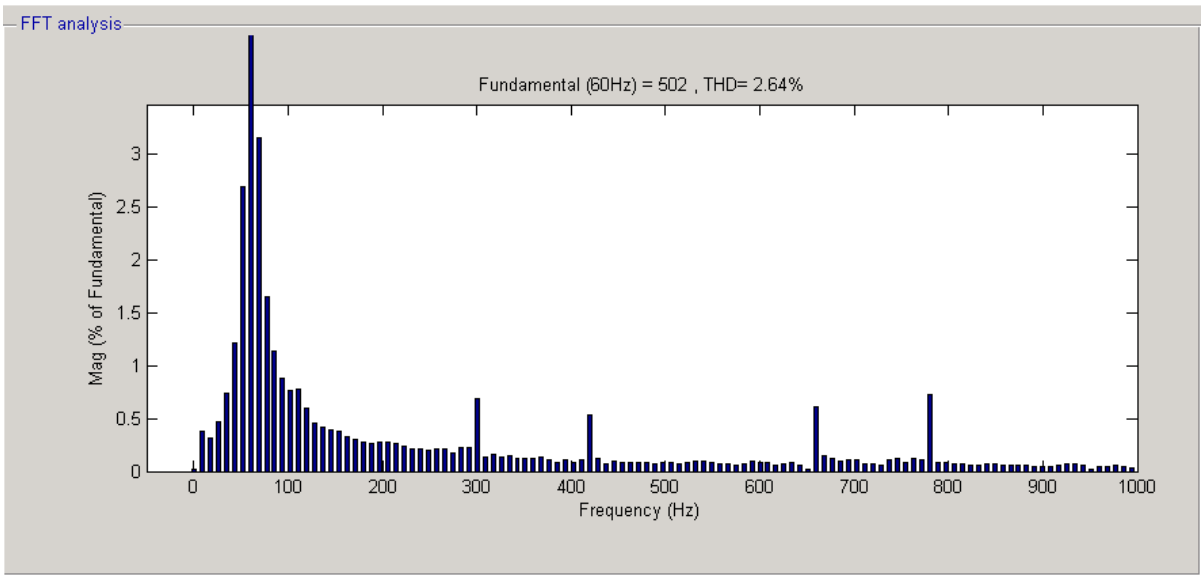

FIGURE 2.7 HARMONIC SPECTRUM OF SOURCE CURRENT IN CLOSED LOOP CIRCUIT

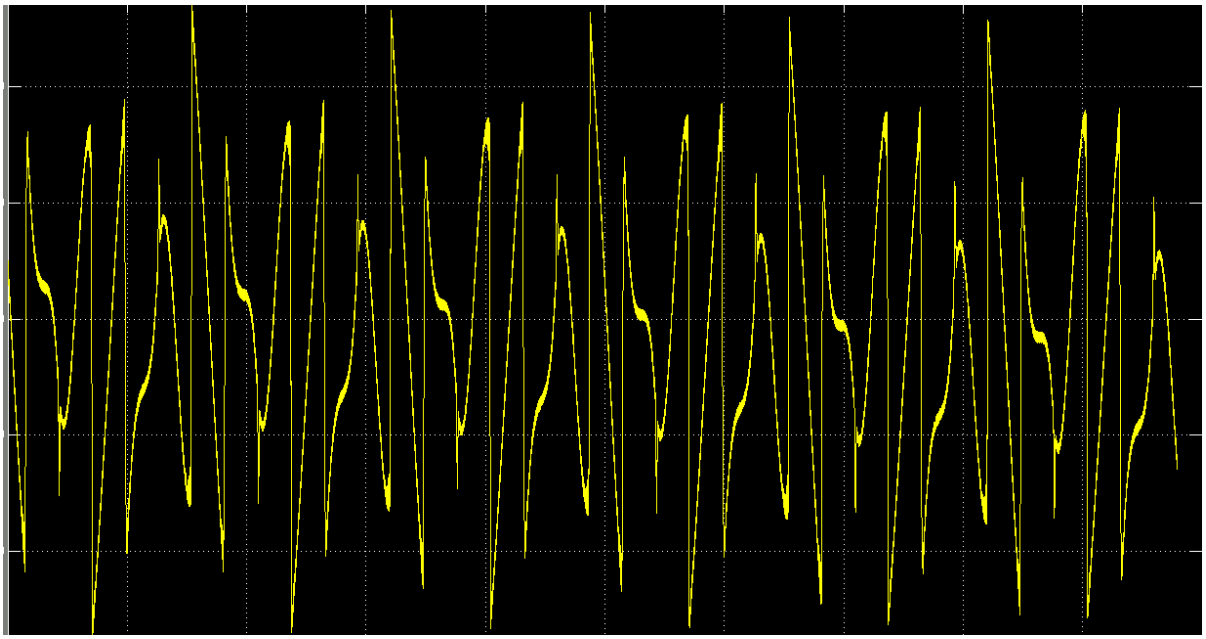

FIGURE 2.8 COMPENSATING CURRENT FROM ACTIVE FILTER

The total distortion in the source decreased from 28.71% to 2.64% by the addition of the Active Filter to the Circuit. Thus, it can be seen that the Active Filter compensates for the harmonics from the load that would otherwise be polluting the source.

2.2 PQ THEORY

P-Q Theory is a well-known controller structure. In this section, the P-Q theory will be implemented on shunt active filters. P-Q Theory uses the measure values of the three phase voltages (e_a, e_b, e_c) and three phase load currents (i_a, i_b, i_c) to calculate the reference currents. There reference currents are used by the inverter to create the compensation currents. (Acharya) **Figure 2.9** shows the diagram of a basic Active Filter compensator.

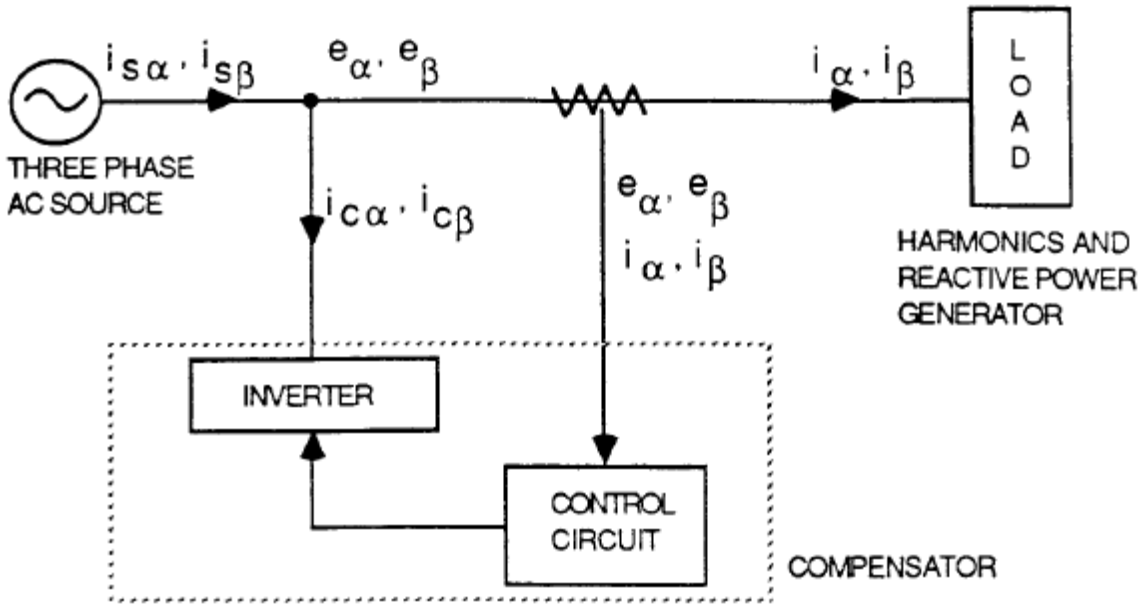

FIGURE 2.9 BASIC ACTIVE FILTER COMPENSATOR (ACHARYA)

P-Q theory, or instantaneous power theory, was first proposed in 1983 by Akagi, et al. It is based on the transformation from three phases, abc, to a two phase

orthogonal axes, αβ, system. After voltages and currents are transformed from abc to αβ, the instantaneous powers are defined on these coordinates. (Akagi, Watanabe, & Aredes, 2007)

The transformation from abc to αβ0 is done using the C matrix as shown below.

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}$$

$$\begin{bmatrix} e_\alpha \\ e_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix}$$

The abc axis shift to orthogonal αβ axes are shown below in **Figure 2.10**.

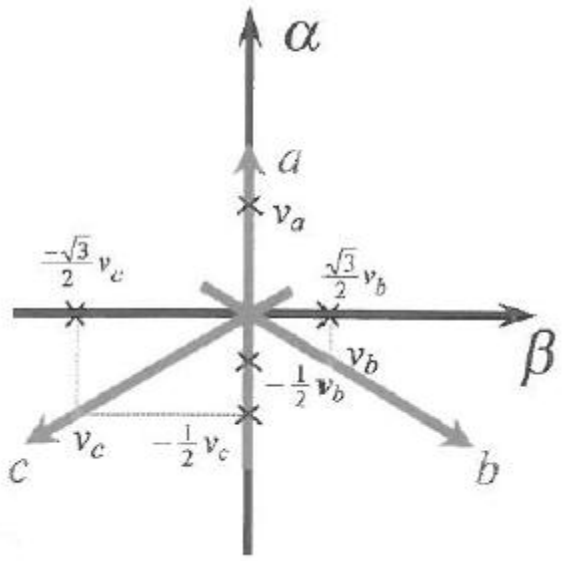

FIGURE 2.10 THREE PHASE TO TWO PHASE TRANSFORMATION (AKAGI, WATANABE, & AREDES, 2007)

Figure 2.2.1 shows the two-phase currents of the source ($i_{S\alpha}$, $i_{S\beta}$), load (i_α, i_β), and compensator ($i_{C\alpha}$, $i_{C\beta}$). The two-phase voltage (e_α, e_β), which is same for source and load, are also shown. From the diagram, it can be seen that:

$$i_{S\alpha} = i_{C\alpha} + i_\alpha$$
$$i_{S\beta} = i_{C\beta} + i_\beta$$

Now, the instantaneous power components of the circuit will be examined on the αβ coordinates. The instantaneous real power **P** and the instantaneous imaginary power **Q** have dc and ac components:

$$P = P_{dc} + P_{ac}$$
$$Q = Q_{dc} + Q_{ac}$$

P_{dc} is the average real active power consumed by the resistive nature of the load. P_{ac} is the oscillating real active power produced by the harmonics. Q_{dc} is the average reactive power consumed by the inductive, capacitive nature of the load. Q_{ac} is the oscillating reactive power from the harmonics. (Acharya)

P and **Q** written in terms of the currents and voltages are given as:

$$\begin{bmatrix} P \\ Q \end{bmatrix} = \begin{bmatrix} e_\alpha & e_\beta \\ -e_\beta & e_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix}$$

So, from the previous equations, the following can be written:

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} e_\alpha & e_\beta \\ -e_\beta & e_\alpha \end{bmatrix}^{-1} \begin{bmatrix} P \\ Q \end{bmatrix}$$
$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \frac{1}{e_\alpha^2 + e_\beta^2} \begin{bmatrix} e_\alpha & e_\beta \\ e_\beta & -e_\alpha \end{bmatrix} \begin{bmatrix} P \\ Q \end{bmatrix}$$

The previous equation shows the load currents, (i_α, i_β), in terms of P and Q, the powers consumed by the load. Similarly, the same can be written for the source currents and the compensating currents in terms of their respective power consumption.

Source Currents:

$$\begin{bmatrix} i_{S\alpha} \\ i_{S\beta} \end{bmatrix} = \frac{1}{e_\alpha^2 + e_\beta^2} \begin{bmatrix} e_\alpha & e_\beta \\ e_\beta & -e_\alpha \end{bmatrix} \begin{bmatrix} P_S \\ Q_S \end{bmatrix}$$

where P_S and Q_S are the powers consumed by the source.

Active Filter Compensating Currents:

$$\begin{bmatrix} i_{C\alpha} \\ i_{C\beta} \end{bmatrix} = \frac{1}{e_\alpha^2 + e_\beta^2} \begin{bmatrix} e_\alpha & e_\beta \\ e_\beta & -e_\alpha \end{bmatrix} \begin{bmatrix} P_C \\ Q_C \end{bmatrix}$$

where P_C and Q_C are the powers consumed by the Active Filter.

In order for the active filter to serve as a harmonic compensator, the compensator must supply the oscillating active and reactive powers of the harmonics. So, P_c=-P_{ac} and Q_c=-Q_{ac}.

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \frac{1}{e_\alpha^2 + e_\beta^2} \begin{bmatrix} e_\alpha & e_\beta \\ e_\beta & -e_\alpha \end{bmatrix} \begin{bmatrix} P \\ Q \end{bmatrix}$$

$$\begin{bmatrix} i_{S\alpha} - i_{C\alpha} \\ i_{S\beta} - i_{C\beta} \end{bmatrix} = \frac{1}{e_\alpha^2 + e_\beta^2} \begin{bmatrix} e_\alpha & e_\beta \\ e_\beta & -e_\alpha \end{bmatrix} \begin{bmatrix} P_{dc} + P_{ac} \\ Q_{dc} + Q_{ac} \end{bmatrix}$$

$$\begin{bmatrix} i_{S\alpha} - i_{C\alpha} \\ i_{S\beta} - i_{C\beta} \end{bmatrix} = \frac{1}{e_\alpha^2 + e_\beta^2} \begin{bmatrix} e_\alpha & e_\beta \\ e_\beta & -e_\alpha \end{bmatrix} \begin{bmatrix} P_S - P_C \\ Q_S - Q_C \end{bmatrix}$$

$$P_S - P_C = P_{dc} + P_{ac}$$

$$Q_S - Q_C = Q_{dc} + Q_{ac}$$

Since, P_c=-P_{ac} and Q_c=-Q_{ac}, then:

$$\therefore P_S = P_{dc}$$

$$\therefore Q_S = Q_{dc}$$

The source is only required to produce the DC components of the power, and the Active Filter will compensate for the harmonics present as shown above.

Now, the compensating currents to implement this harmonic compensator will be considered. (Acharya)

$$\begin{bmatrix} i_{C\alpha} \\ i_{C\beta} \end{bmatrix} = \frac{1}{e_\alpha^2 + e_\beta^2} \begin{bmatrix} e_\alpha & e_\beta \\ e_\beta & -e_\alpha \end{bmatrix} \begin{bmatrix} P_C \\ Q_C \end{bmatrix} = \frac{1}{e_\alpha^2 + e_\beta^2} \begin{bmatrix} e_\alpha & e_\beta \\ e_\beta & -e_\alpha \end{bmatrix} \begin{bmatrix} -P_{ac} \\ -Q_{ac} \end{bmatrix}$$

However, most common loads include a rectifier front-end (or diode bridge). For a diode bridge load, P_{ac} is negligible in comparison to Q_{ac} as shown in **Figure 2.11**.

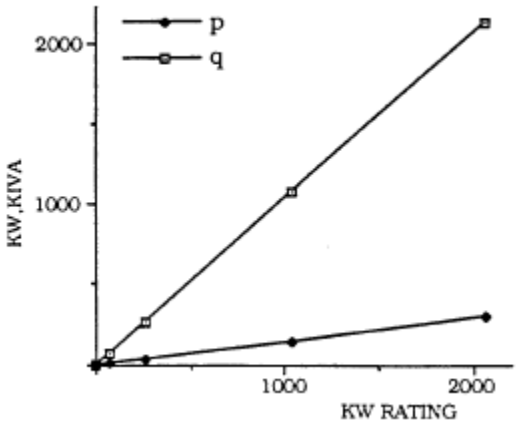

FIGURE 2.11 AC COMPONENTS OF P AND Q (ACHARYA)

So, if P_{ac} is negligible, then the compensating currents are now:

$$\begin{bmatrix} i_{C\alpha} \\ i_{C\beta} \end{bmatrix} = \frac{1}{e_\alpha^2 + e_\beta^2} \begin{bmatrix} e_\alpha & e_\beta \\ e_\beta & -e_\alpha \end{bmatrix} \begin{bmatrix} P_C \\ Q_C \end{bmatrix} = \frac{1}{e_\alpha^2 + e_\beta^2} \begin{bmatrix} e_\alpha & e_\beta \\ e_\beta & -e_\alpha \end{bmatrix} \begin{bmatrix} 0 \\ -Q_{ac} \end{bmatrix}$$

These currents will now compensate for the harmonics in the load. The two-phase currents will then be converted back to three phase as the last step in the PQ theory.

$$\begin{bmatrix} i_{Ca} \\ i_{Cb} \\ i_{Cc} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_{C\alpha} \\ i_{C\beta} \end{bmatrix}$$

This implementation of this PQ theory method is shown in its entirety in **Figure 2.12**.

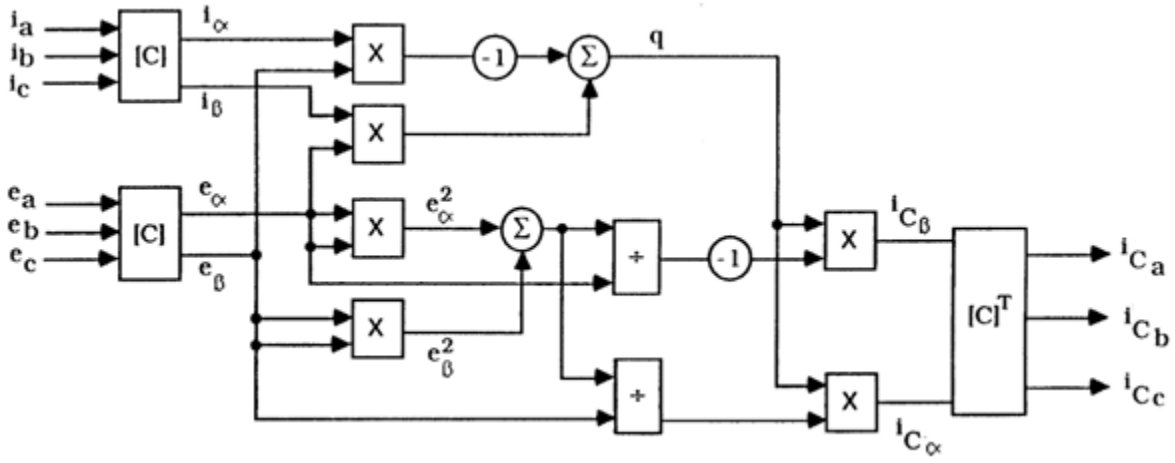

FIGURE 2.12 PQ THEORY BLOCK DIAGRAM (ACHARYA)

2.2.1 MATLAB SIMULATIONS OF PQ THEORY

The PQ theory implementation shown above in **Figure 2.12** was implemented in Matlab. In this section, the simulations of various signals in the implementation are shown.

The simulations of the three-phase to two-phase conversion for current is shown in **Figure 2.13** and **Figure 2.14**. The same conversion for voltage is shown in **Figure 2.15** and **Figure 2.16**.

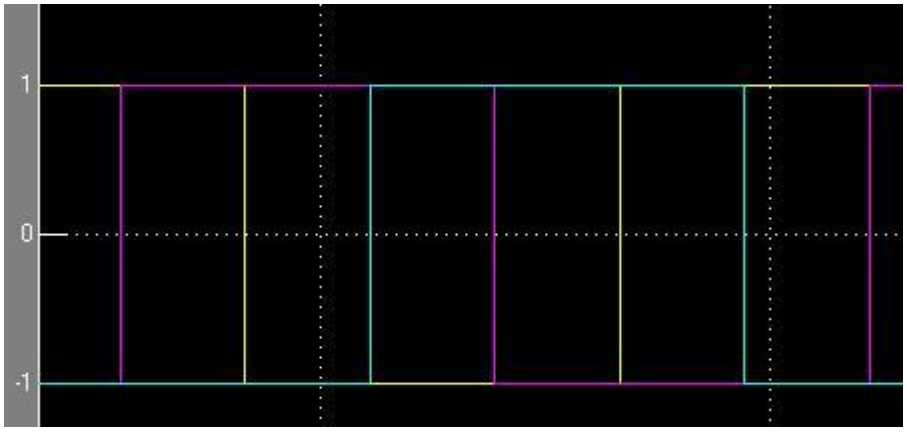

FIGURE 2.13 THREE PHASE CURRENT

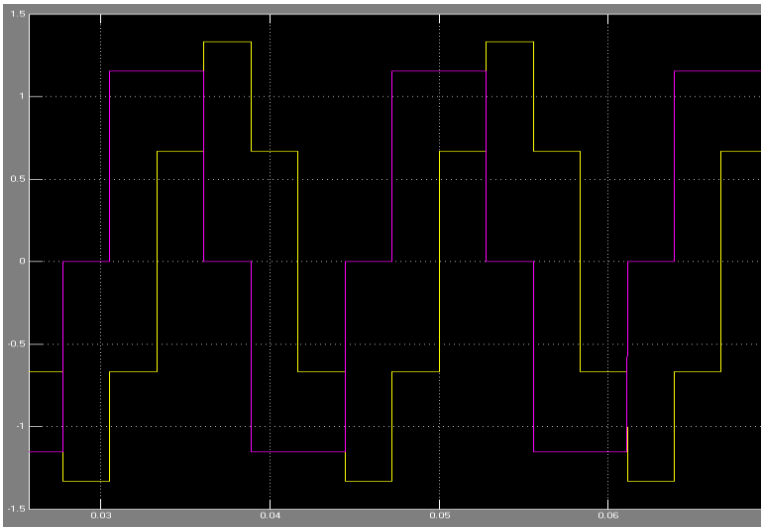

FIGURE 2.14 TWO PHASE CONVERSION FOR CURRENT

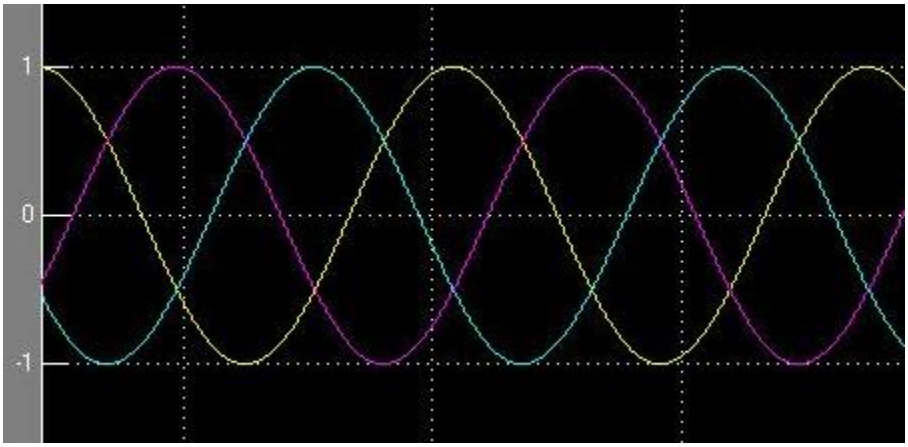

FIGURE 2.15 THREE PHASE VOLTAGE

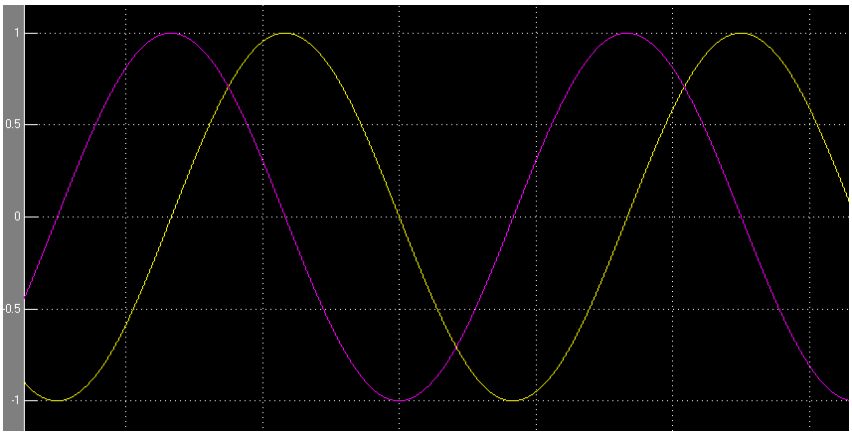

FIGURE 2.16 TWO PHASE CONVERSION FOR VOLTAGE

Figure 2.17 shows the value of q, which we derived in the previous section.

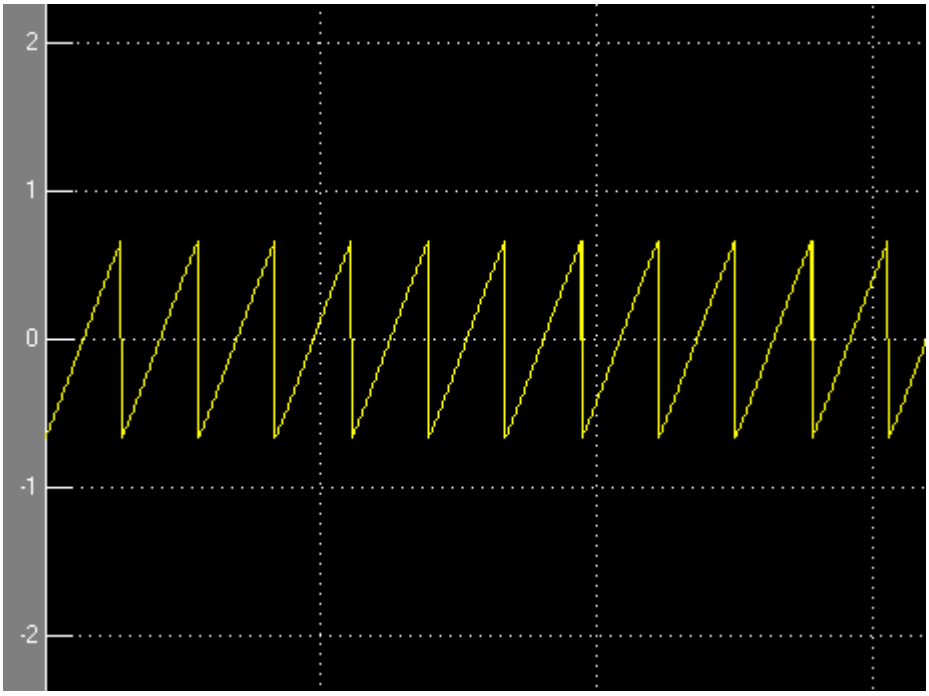

FIGURE 2.17 SIGNAL Q

Figure 2.18 and **Figure 2.19** show the two phase compensating currents, $i_{C\alpha}$ and $i_{C\beta}$ signal that is calculated by the Active Filter.

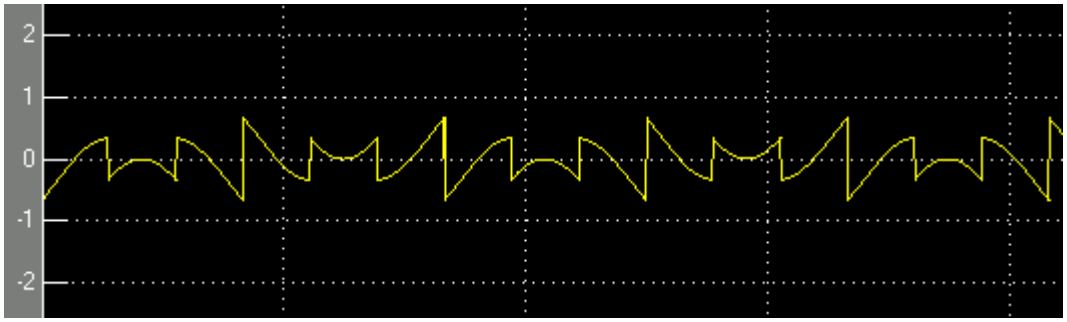

FIGURE 2.18 $i_{C\alpha}$ SIGNAL

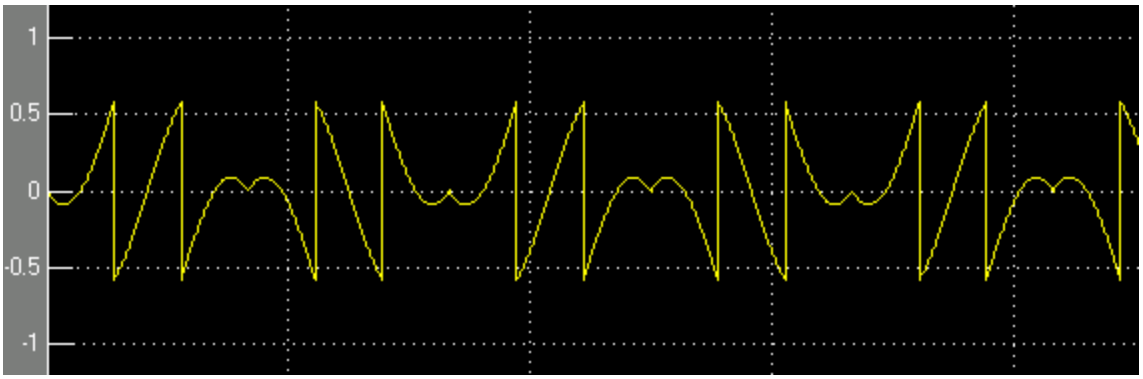

FIGURE 2.19 $i_{C\beta}$ SIGNAL

2.3 SERIES ACTIVE FILTER

In contrast to the Shunt Active Filter, which generates harmonic currents to cancel the load's harmonic currents, the Series Active Filter generates harmonic voltages to cancel the load harmonic voltages. In the Shunt Active Filter, the source voltage equals the load voltage. However, in the Series Active Filter, it is the source current that is equal to the load current. (Akagi, Watanabe, & Aredes, 2007) The diagram of the Series Active Filter is shown in **Figure 2.20**.

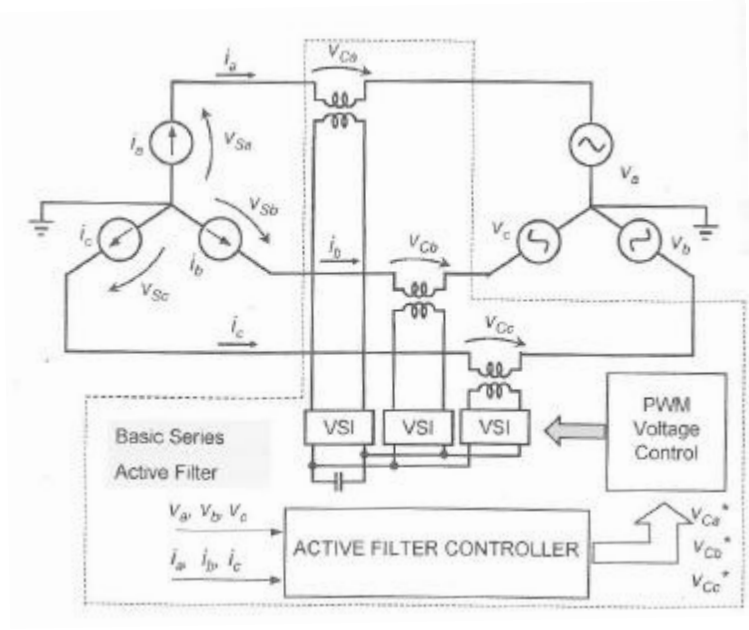

FIGURE 2.20 BASIC SERIES FILTER (AKAGI, WATANABE, & AREDES, 2007)

The voltages on the current sources are V_{Sa}, V_{Sb}, and V_{Sc}. The load voltages are V_a, V_b, and V_c. And the compensating voltages are given as V_{Ca}, V_{Cb}, and V_{Cc}. The relationship between these voltages is given as follows:

$$\begin{bmatrix} V_{Sa} \\ V_{Sb} \\ V_{Sc} \end{bmatrix} = \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} - \begin{bmatrix} V_{Ca} \\ V_{Cb} \\ V_{Cc} \end{bmatrix}$$

The compensating voltages from the Active Filter are synthesized by 3 single-phase Voltage Source Inverters (VSIs). The reference voltages for these inverters are produced by the Active Filter Controller using the load voltages and currents. This calculation can be done using the P-Q theory implementation.

The real and imaginary powers, P and Q, are defined as follows:

$$\begin{bmatrix} P \\ Q \end{bmatrix} = \begin{bmatrix} i_\alpha & i_\beta \\ -i_\beta & i_\alpha \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix}$$

Again, in order for the active filter to serve as a harmonic compensator, the compensator must supply the oscillating active and reactive powers of the harmonics (P_c=-P_{ac} and Q_c=-Q_{ac}). Thus,

$$\begin{bmatrix} V_{C\alpha} \\ V_{C\beta} \end{bmatrix} = \frac{1}{i_\alpha^2 + i_\beta^2} \begin{bmatrix} i_\alpha & i_\beta \\ i_\beta & -i_\alpha \end{bmatrix} \begin{bmatrix} P_C \\ Q_C \end{bmatrix} = \frac{1}{i_\alpha^2 + i_\beta^2} \begin{bmatrix} i_\alpha & i_\beta \\ i_\beta & -i_\alpha \end{bmatrix} \begin{bmatrix} -P_{ac} \\ -Q_{ac} \end{bmatrix}$$

The two phase compensating voltages are converted back into three phase:

$$\begin{bmatrix} V_{Ca} \\ V_{Cb} \\ V_{Cc} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{C\alpha} \\ V_{C\beta} \end{bmatrix}$$

As show, series active filters uses voltages to compensate for the harmonics in the load as opposed to using current, the method used by shunt active filters.

2.4 SYNCHRONOUS REFERENCE FRAME CONTROLLER

Synchronous Reference Frame (SRF) controller is another type of Active Filter Controller. The SRF controller extracts the load harmonic currents and also regulates the voltage for the inverter DC bus. The block diagram of the SRF controller is shown in **Figure 2.21**.

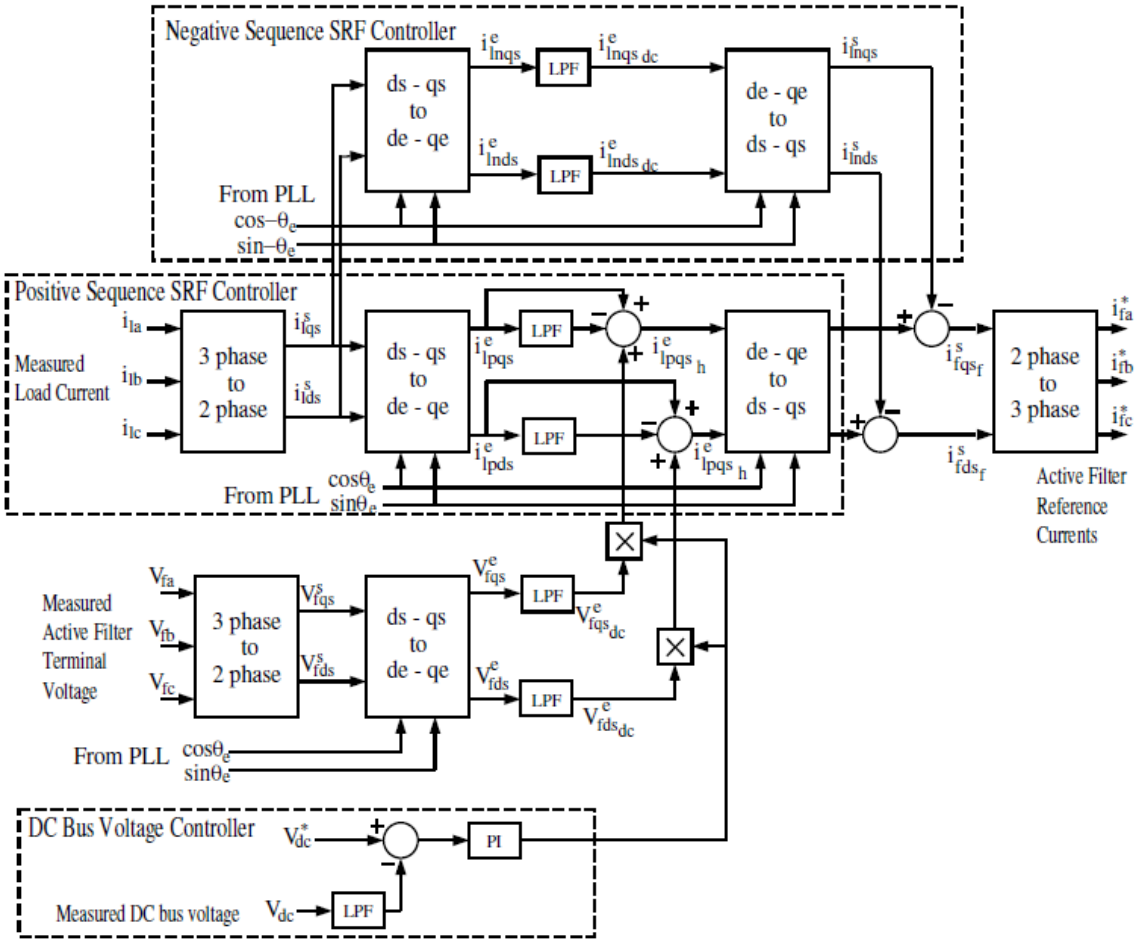

FIGURE 2.21 SYNCHRONOUS REFERENCE FRAME (SRF) CONTROLLER (BHATTACHARYA, FRANK, DIVAN, & BANERJEE, 1998)

The three phase load currents are i_{la}, i_{lb}, and i_{lc}. V_{fa}, V_{fb}, and V_{fc} are the Active Filter terminal voltages. The SRF controller consists of 3 sub-controllers: Positive Sequence SRF controller, Negative Sequence SRF controller, and DC Bus Voltage Controller. The Positive Sequence SRF controller extracts the harmonics in the synchronous d-q (direct-quadrature) reference frame. The Negative Sequence SRF controller extracts the fundamental negative sequence The SRF controller does not compensate for this fundamental negative sequence. In addition, the SRF controls the voltage for the

inverter DC bus. The fundamental frequency we are considering is 60Hz. (Bhattacharya, Frank, Divan, & Banerjee, 1998)

Positive sequence SRF

The Positive sequence SRF controller takes the three phase load currents and converts them into two phase load currents in terms of a stationary reference frame, d_s-q_s. This stationary reference frame is then converted to a synchronous reference frame, d_e-q_e, using angle $+\theta_e$. The currents in the synchronous reference frame are: i^e_{lpds} and i^e_{lpqs}.

In the d_e-q_e reference frame, the fundamental **positive** sequence components are DC quantities, whereas all the harmonic components (mainly 5th and 7th harmonics) are AC quantities. By passing i^e_{lpds} and i^e_{lpqs} through a low-pass filter with a cutoff around 200Hz, the dc component (fundamental **positive** sequence) can be isolated. Then, by subtracting this dc components from i^e_{lpds} and i^e_{lpqs}, the ac components, $i^e_{lpds_h}$ and $i^e_{lpqs_h}$, are separated. The signals $i^e_{lpds_h}$ and $i^e_{lpqs_h}$ are converted back to the stationary reference frame producing the harmonic components of the load current.

If a fundamental negative sequence is present, then the Positive sequence SRF controller treats this as a harmonic because in the synchronous reference frame, this sequence will appear as an AC component (120Hz). The Negative sequence SRF controller will remove this sequence from the harmonic components found in the Positive sequence SRF. (Bhattacharya, Frank, Divan, & Banerjee, 1998)

Negative sequence SRF

The signals in the stationary reference frame, d_s-q_s, are then converted to a synchronous reference frame, d_e-q_e, using angle $-\theta_e$. The currents in the synchronous reference frame are now: i^e_{lnds} and i^e_{lnqs}.

In the d_e-q_e reference frame, the fundamental **negative** sequence components are DC quantities, whereas all the harmonic components (mainly 5th and 7th harmonics) and fundamental **positive** sequence are AC quantities. By passing i^e_{lpds} and i^e_{lpqs} through a low-pass filter with a cutoff around 200Hz, the fundamental negative sequence can be isolated. The extracted dc quantities are transformed back into the stationary reference frame. Then the fundamental negative sequence is subtracted from the output of the Positive sequence SRF controller.

Thus, this leaves just the harmonics signals in two phase (stationary reference frame). These signals are converted back to three phase as the final step. These reference currents, i_{fa}, i_{fb}, and i_{fc}, do not contain the fundamental negative sequence component. This ensures that the active filter only compensates for the harmonics, and not the negative sequence current. (Bhattacharya, Frank, Divan, & Banerjee, 1998)

DC bus Voltage Controller

The DC bus Voltage controller regulates the voltage across the DC bus to a particular reference value by compensating for the inverter losses. The controller produces a fundamental reference current to provide the real power transfer for regulation of DC bus voltage and compensation of inverter losses. (Bhattacharya, Frank, Divan, & Banerjee, 1998)

3 FIELD PROGRAMMABLE ANALOG ARRAY

Field Programmable Analog Arrays (FPAA) are the analog counterpart of Field Programmable Gate Arrays (FPGA). Similar to FPGAs, FPAAs are reconfigurable and easy to design and simulate. This chapter gives background on FPAA and AnadigmDesigner2 configuration tool.

3.1 OVERVIEW OF FPAA

Field Programmable Analog Arrays are integrated circuits that can implement various analog circuits. FPAAs are composed of Configurable Analog Blocks (CAB) and an interconnecting routing network. Each CAB can implement analog signal processing functions including, amplification, integration, differentiation, addition, subtraction, multiplication, and division to name a few. The interconnection network routes the signals between CABs and I/O blocks. **Figure 3.1** shows the overall diagram of the FPAA.

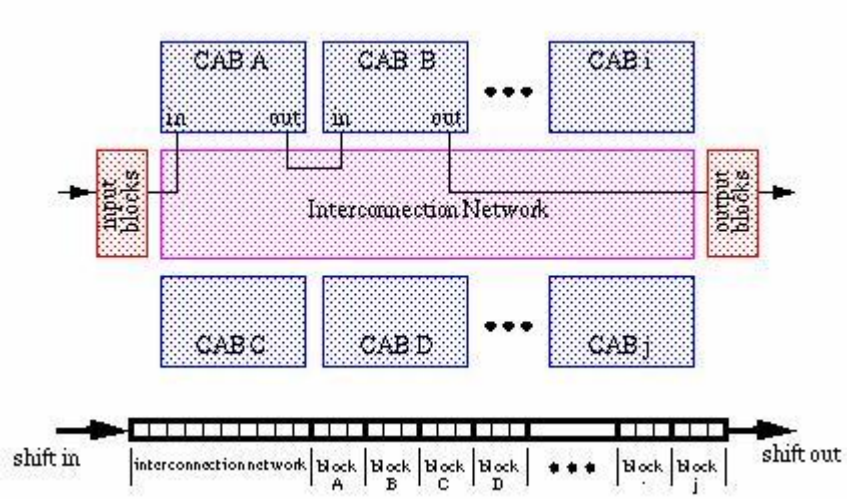

FIGURE 3.1 FPAA DIAGRAM (ILA, BATTLE, CUFI, & GARCIA, 2002) (CIOC, LITA, VISAN, & BOSTAN, 2009)

There are two types of FPAAs: Discrete-time and Continuous-time. The internal structure of the CABs depends on the type of FPAA. Discrete-time FPAA is designed with switched capacitor technology, which is explained further in the next section. This allows for easier programmability of FPAA. Continuous-time FPAA is designed with transconductor technology. This is advantageous in terms of bandwidth, but it is limited in programmability.

Only Discrete-time FPAA technology is considered in detail here since the FPAA chip used, Anadigm's AN231E04, for the sake of this research is of that type. The next section focuses on the switched capacitor technology of Discrete-time FPAAs. (Ila, Battle, Cufi, & Garcia, 2002)

3.2 SWITCHING CAPACITOR TECHNOLOGY

Switched capacitor technology is utilized by Anadigm in its discrete-time FPAA chips. This technique is based on the fact that a capacitor switching between two circuit nodes at a certain frequency is equivalent to a resistor connecting these same nodes. This is shown in **Figure 3.2**. The resistance of this resistor depends on the capacitance and the switching frequency. (Cioc, Lita, Visan, & Bostan, 2009)

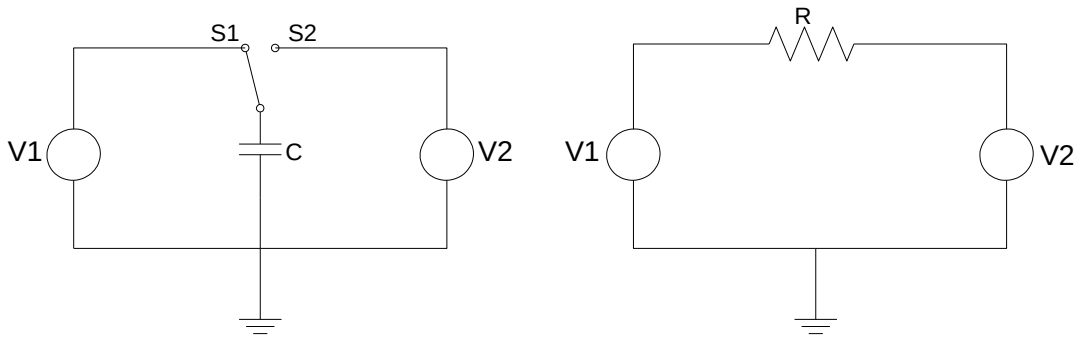

FIGURE 3.2 EQUIVALENCE OF SWITCHED CAPACITOR TO RESISTOR

When the switch is set to position S1, the capacitor is charged to the voltage V1, input voltage. The total charge on capacitor C is

$$Q_1 = C \cdot V_1 \ .$$

When switch position is set to S2, the capacitor is now charged to voltage V2, output voltage. The total charge on capacitor C is now

$$Q_2 = C \cdot V_2 \ .$$

The change in charge on capacitor C is given as

$$\Delta Q = Q_2 - Q_1 = C \cdot (V_2 - V_1) \quad .$$

So, the current flowing from the input to output is

$$I = \frac{\Delta Q}{T} = \frac{C \cdot (V_2 - V_1)}{T} \quad ,$$

where T is the time between switching as shown in **Figure 3.3**.

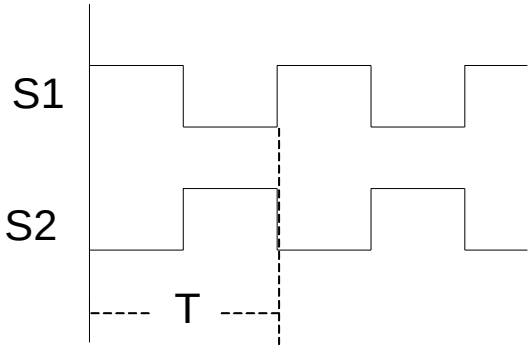

FIGURE 3.3 TIMING DIAGRAM OF SWITCH POSITIONS

The frequency of switching can be found using T, where

$$f_S = \frac{1}{T} \quad .$$

The current flowing from input to output is the same for the equivalent resistor circuit. The voltage across the resistor is $V_2 - V_1$. Then, the resistance is

$$R = \frac{V}{I} = \frac{(V_2 - V_1)}{\frac{C \cdot (V_2 - V_1)}{T}} = \frac{T}{C} = \frac{1}{f_S \cdot C} \quad .$$

Therefore, as mentioned earlier, the resistance, R, depends on the capacitance, C, and the switching frequency, f_S. (Dong, 2006)

By using switched-capacitors in place of resistors, the behavior of a resistor can be imitated except with higher accuracy, lower power consumption, and smaller area. Also, the value of the resistance can be changed by changing the switching frequency. Thus, using the switched-capacitor technology in the FPAA is beneficial technique.

3.3 FPAA ARCHITECTURE

For this research, Anadigm's third generation FPAA chip, AN231e04, was used. The chip and corresponding evaluation board are shown in **Figure 3.4**. In this section, the architecture of the FPAA chip will be described in detail.

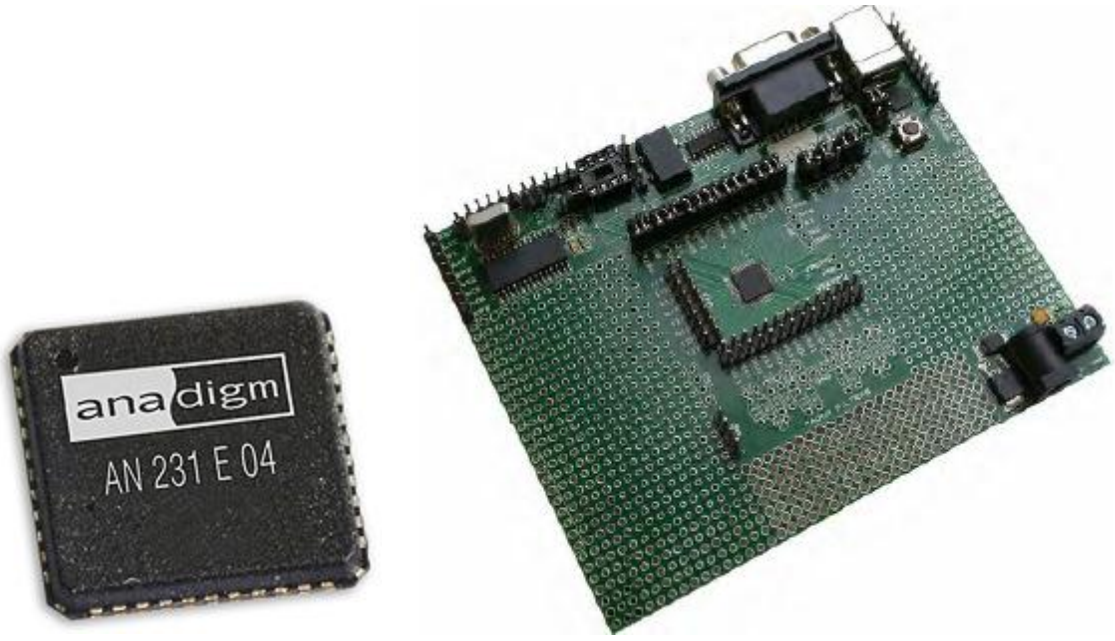

FIGURE 3.4 AN231E04 CHIP AND EVALUATION BOARD (ANADIGMAPEX DPASP FAMILY USER MANUAL, AN 23X SERIES, 2005)

Anadigm's AN231E04 chip belongs to the family of Anadigmvortex, Anadigm's third generation FPAA family. The chip contains four CABs and seven analog I/O cells. The 2x2 matrix of CABs allows for the CABs to be interconnected. The analog signal processing occurs almost entirely in the CABs. (AN231E04 DataSheet, 2008) Each of the CABs had access to a single Look Up Table (LUT), which can be used to implement arbitrary transfer functions. A Voltage Reference Generator is also found on the chip and its purpose is to supply reference voltages to the CABs. (AnadigmApex dpASP Family User Manual, AN 23x series, 2005) The architecture overview of the chip is shown in **Figure 3.5**.

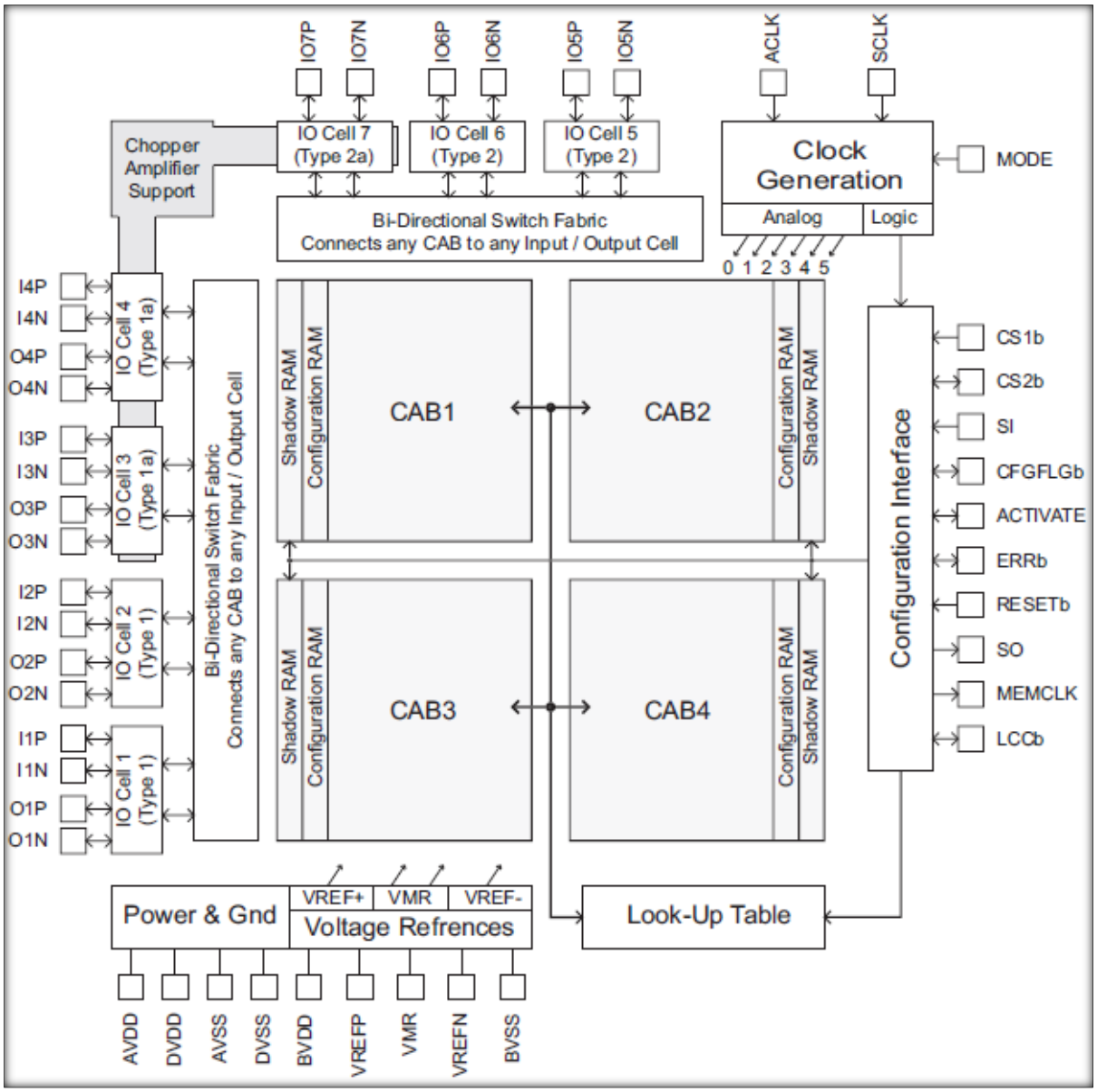

FIGURE 3.5 ARCHITECTURE OF AN231E04 CHIP (AN231E04 DATASHEET, 2008)

3.4 CONFIGURATION WITH ANADIGM DESIGNER TOOL

Anadigm's FPAA boards can be configured and reconfigured using AnadigmDesigner2 Tool. This software tool allows for a quick and easy way to construct simple or complex analog circuit using a simple graphical interface. Design of the circuits in AnadigmDesigner 2 Tool is simple by selecting, placing, and wiring together built-in Configurable Analog Modules (CAM). CAMs are essentially small building blocks of a circuit including gains, filters, summations, multipliers, dividers, and rectifiers to name a few. (Priyadarshini, 2006)

Circuits constructed on AnadigmDesigner 2 Tool can be downloaded to the dynamically programmable Analog Signal Processor (dpASP) using an USB or RS232 cable. The dpASP can be modified as needed while operating. Once the new circuit data is loaded onto the dpASP completely, the configuration of the FPAA chip occurs in a single clock cycle. The FPAA chip can be reconfigured as many times as needed because the memory is SRAM based. (AnadigmApex dpASP Family User Manual, AN 23x series, 2005)

There are three regions of volatile SRAM within the dpASP device. These include Shadow SRAM, Configuration SRAM, and a Look-Up Table (LUT). The Shadow SRAM gets written to during configuration and reconfiguration. It holds the configuration data prior to the transfer of the data to the Configuration SRAM. Then, the Configuration SRAM controls the behavior of the analog signal processing circuitry. This transfer from the Shadow SRAM to the Configuration SRAM occurs in one clock cycle. The LUT memory is used to create arbitrary waveforms and table based functions. (AnadigmApex dpASP Family User Manual, AN 23x series, 2005)

AnadigmDesigner 2 also includes a time domain functional simulator which shows the circuit's behavior without an oscilloscope. **Figure 3.6**, **Figure 3.7**, and **Figure 3.8** show aspects of the software discussed for a simple circuit. **Figure 3.6** shows the circuit for implementing a sinusoidal function. The LUT for this function is shown in **Figure 3.7**. And **Figure 3.8** shows the simulation result for the circuit.

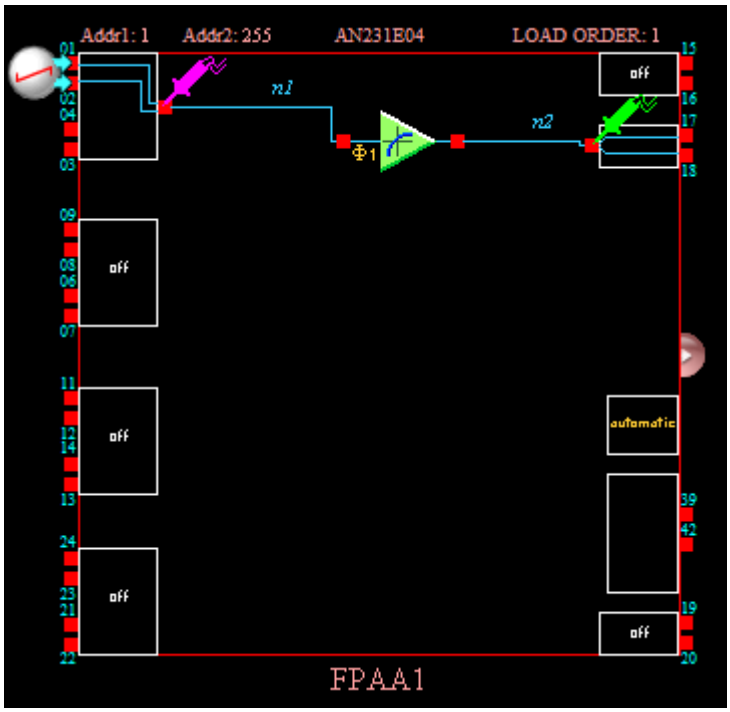

FIGURE 3.6 FPAA CIRCUIT OF SINUSOIDAL FUNCTION

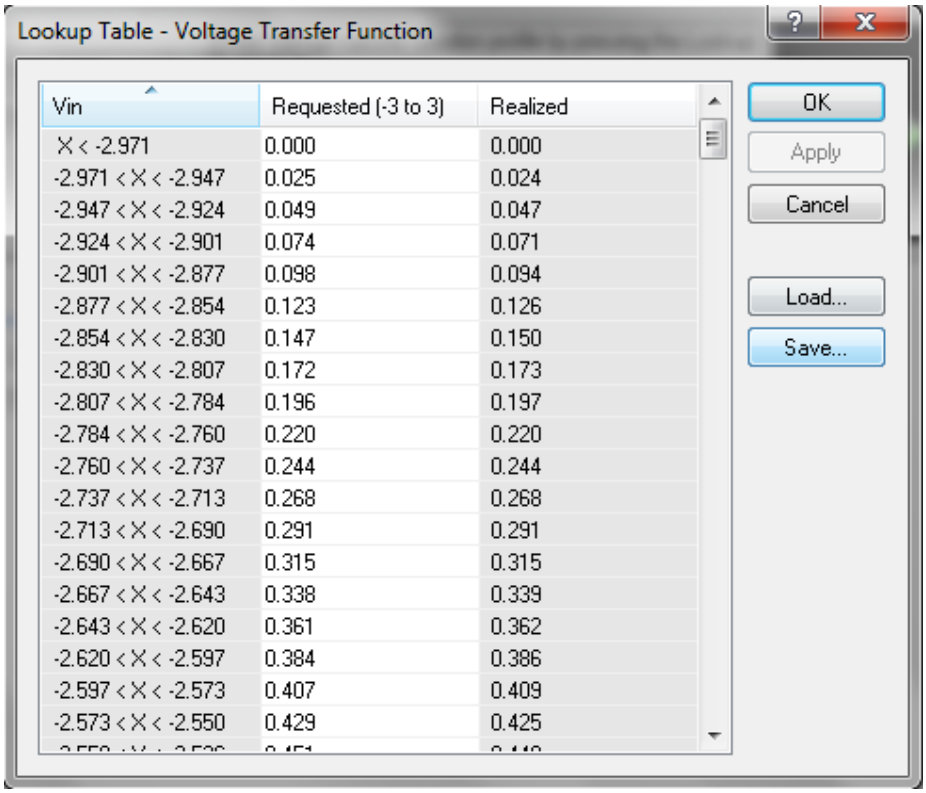

FIGURE 3.7 LOOK-UP TABLE FOR SINUSOIDAL FUNCTION

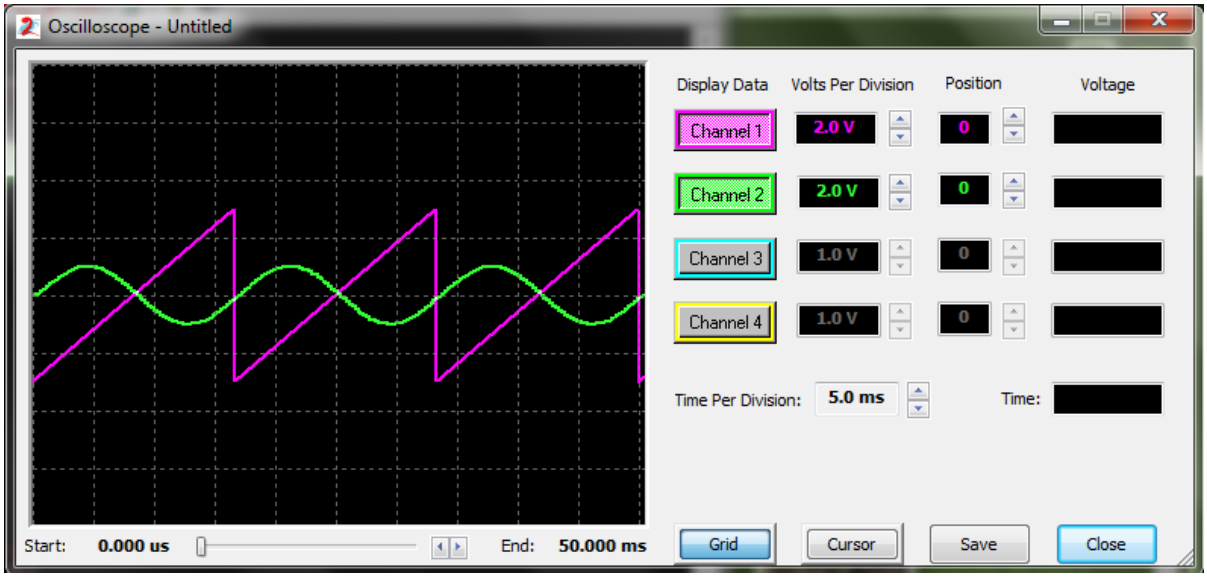

FIGURE 3.8 SIMULATION RESULT OF SINUSOIDAL FUNCTION

Overall, the AnadigmDesigner 2 Tool allows for improved speed and ease of circuit design on the FPAA.

3.5 ADVANTAGES OF FPAA

Real world signals are analog, not digital. The use of FPAAs allows for the manipulations of these signals directly without the need for A/D or D/A conversion. This is because the FPAAs receive, process, and transmit these signals entirely in the analog domain. Also, the speed of the FPAA is suited for real time applications because of the lack of conversion. (Dong, 2006)

Another advantage of the FPAA chip is the speed of the design. FPAA circuits design is much faster than the conventional analog circuit design (draw, simulate, breadboard, and test). Using the AnadigmDesigner 2 software, it is simple to design a circuit and then configure an FPAA. And in seconds, the FPAA chip can be reconfigured to another circuit, if desired. This allows for much flexibility in the design while reducing time, labor, and cost of conventional design technique.

4 FPAA IMPLEMENTATION OF PQ THEORY

The PQ theory was implemented using four FPAA chips. The entire design as designed in AnadigmDesigner 2 is shown in **Figure 4.1**. First, the input, intermediate, and output signals will be considered for each individual chip. Then, the final output of the implementation will be considered. The simulation results and experimental results will be compared for each of these signals to show that the experimental results are correct.

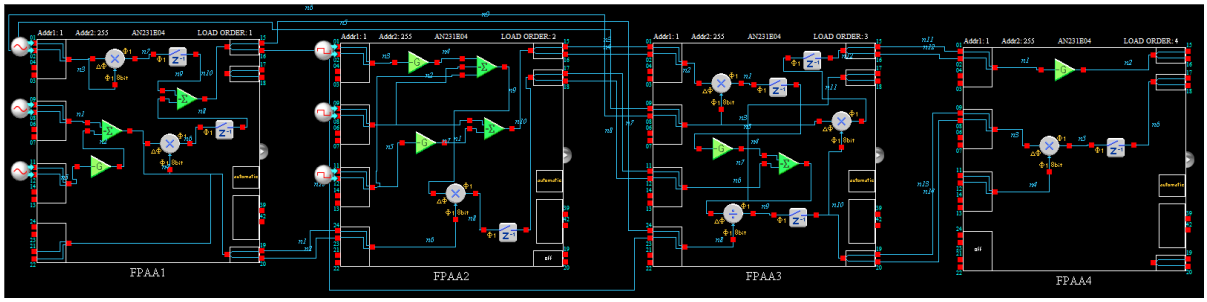

FIGURE 4.1 PQ THEORY DESIGN IN ANADIGMDESIGNER 2

4.1 INTERMEDIATE SIGNALS

In this section, the individual chips in the design are examined in detail. For each chip, the simulated signals on AnadigmDesigner 2 are compared with the actual outputs from the corresponding FPAA chip.

4.1.1 CHIP 1

Figure 4.2 shows the circuitry of Chip 1 in AnadigmDesigner 2.

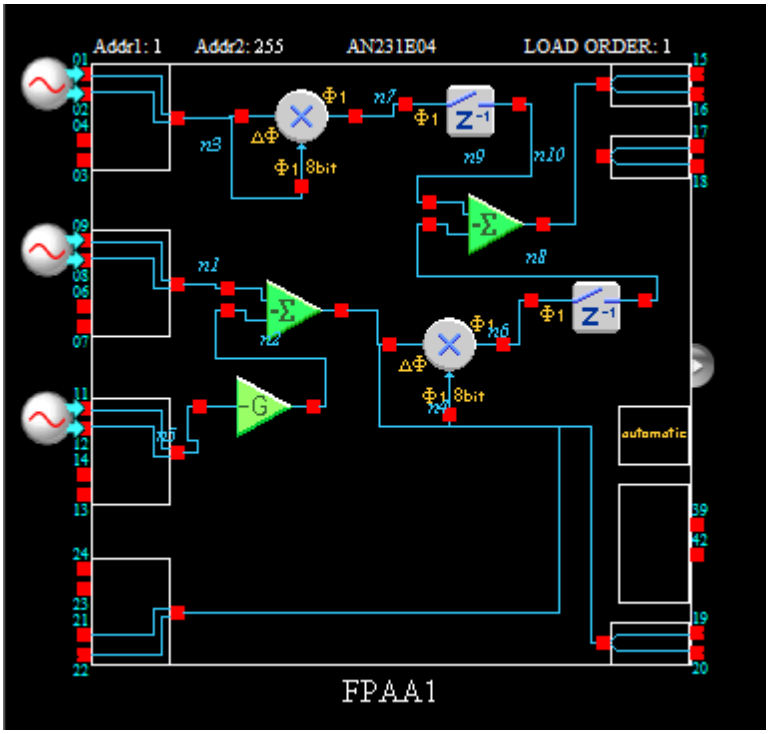

FIGURE 4.2 CHIP 1

Inputs: e_a, e_b, e_c

Outputs: e_β, $-(e_\alpha^2 + e_\beta^2)$

Inputs to Chip 1 are the three phase voltage sources: e_a, e_b, e_c. The simulation results are shown in **Figure 4.3**.

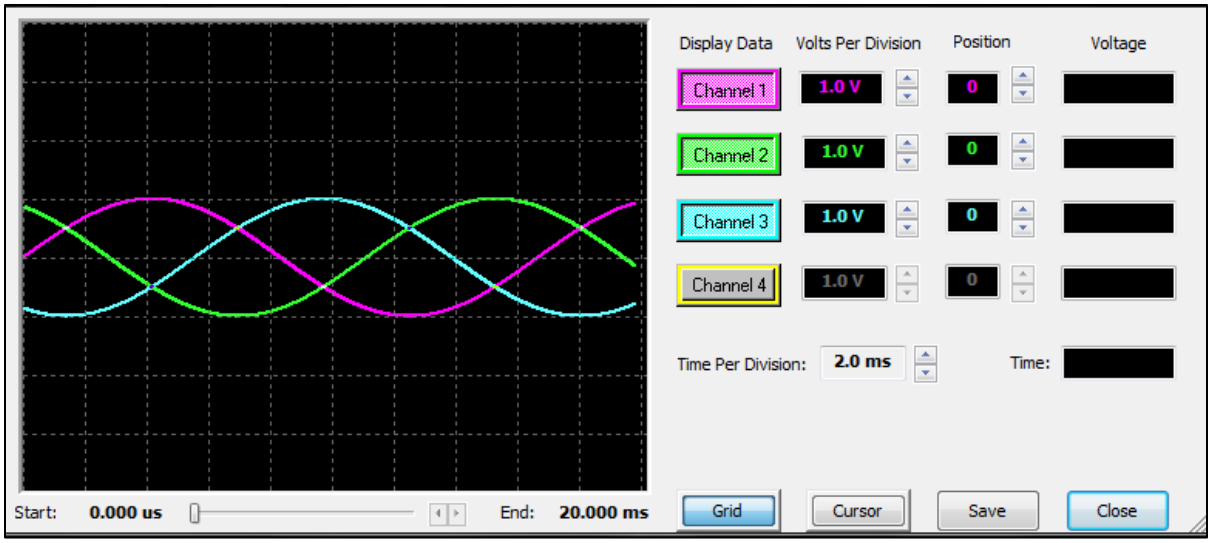

FIGURE 4.3 SIMULATION RESULTS OF $e_a,\ e_b,\ e_c$

Important signals from chip 1 include e_α and e_β. The simulation results and experimental results of e_α and e_β are shown in **Figure 4.4** and **Figure 4.5**. These two signals must be in quadrature as they are the two-phase conversions of the three-phase input. This characteristic does hold as can be seen in these figures.

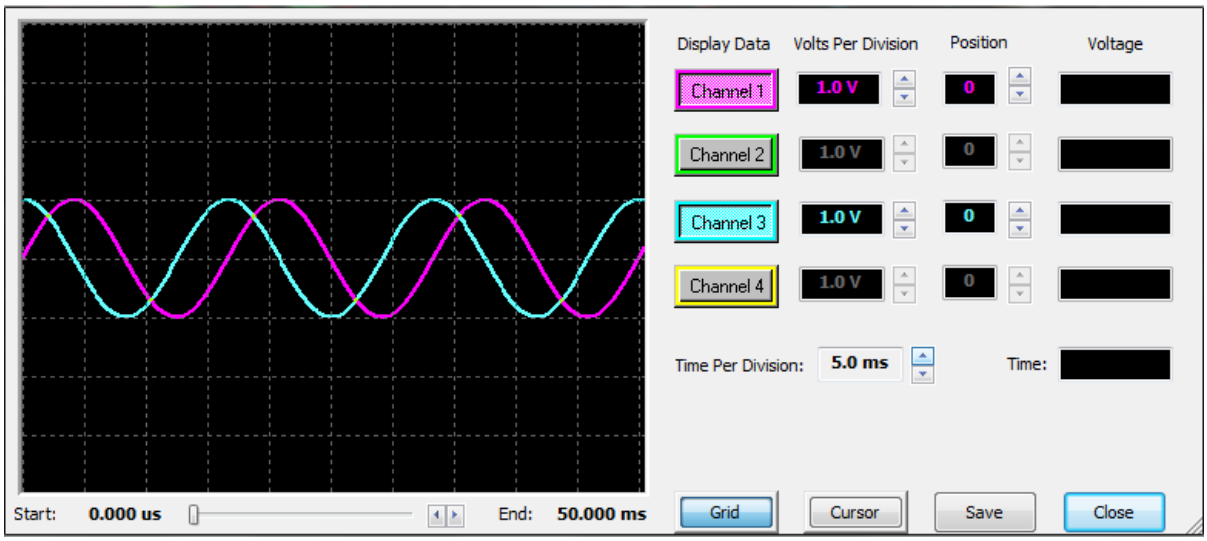

FIGURE 4.4 SIMULATION RESULTS OF e_α AND e_β

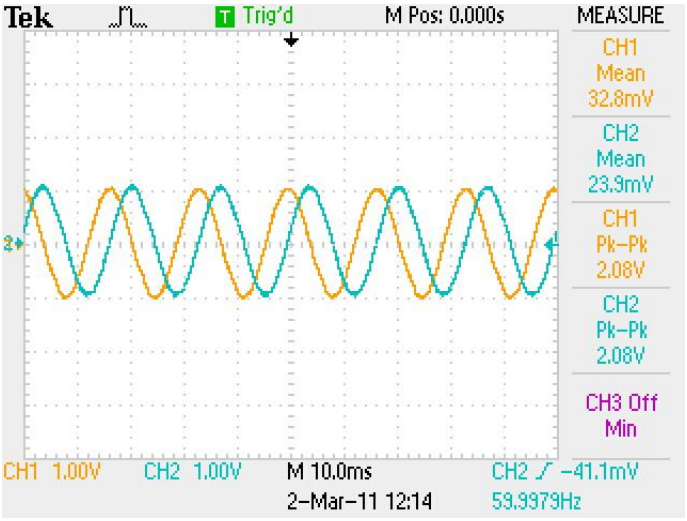

FIGURE 4.5 EXPERIMENTAL RESULTS OF e_α AND e_β

The simulation results and experimental results of the output $-(e_\alpha^2 + e_\beta^2)$ are shown in **Figure 4.6** and **Figure 4.7**. Both figures show that $-(e_\alpha^2 + e_\beta^2)$ is constant at the value of -1V.

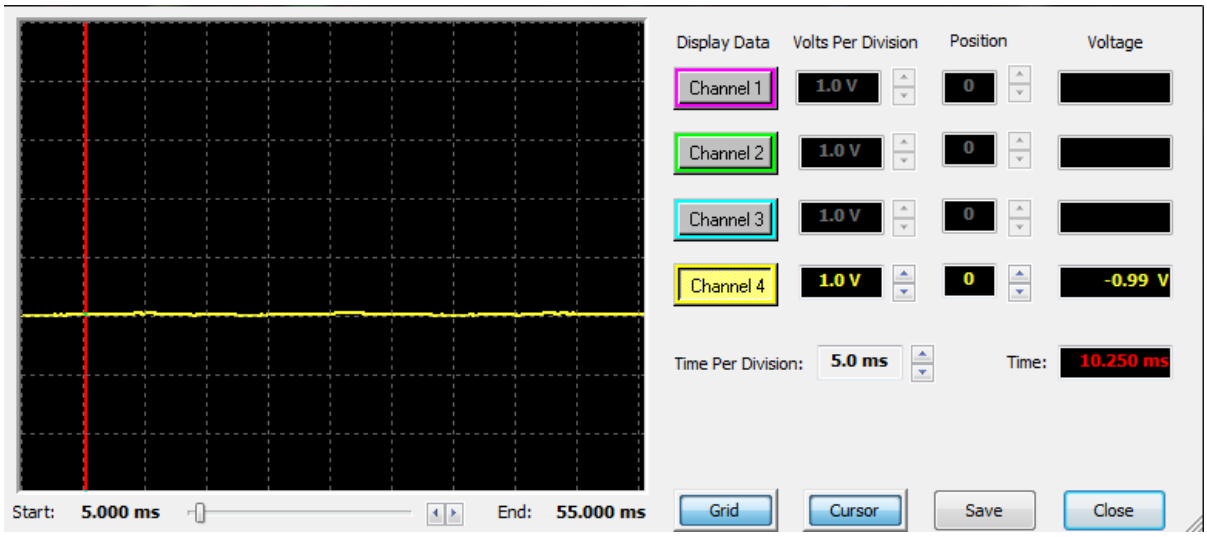

FIGURE 4.6 SIMULATION RESULTS OF $-(e_\alpha^2 + e_\beta^2)$

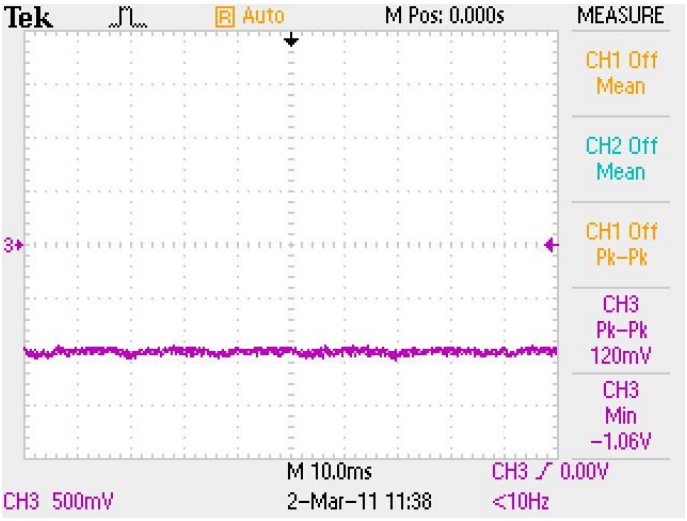

FIGURE 4.7 EXPERIMENTAL RESULTS OF $-(e_\alpha^2 + e_\beta^2)$

4.1.2 CHIP 2

Figure 4.8 shows the circuitry of Chip 2 in AnadigmDesigner 2.

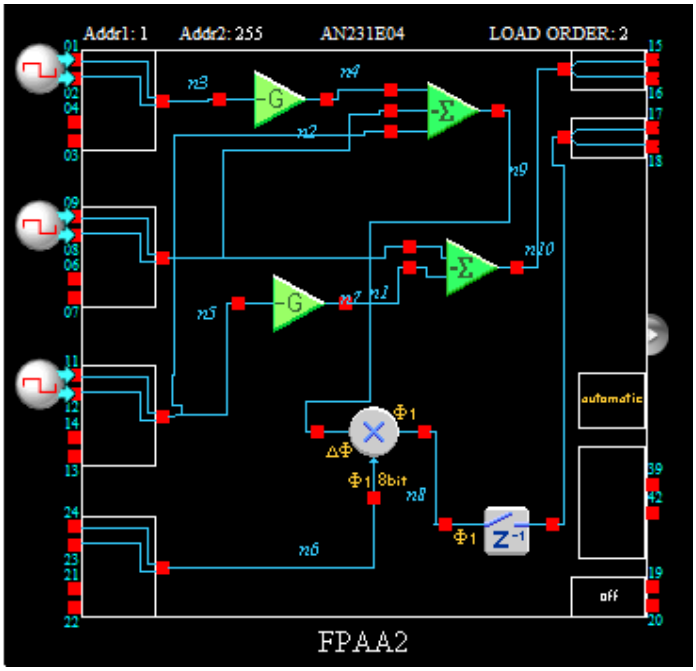

FIGURE 4.8 CHIP 2

Inputs: i_a, i_b, i_c

Outputs: $i_\alpha e_\beta$, i_β

Inputs to Chip 2 are the three phase current sources: i_a, i_b, i_c. The simulation results and experimental results of these inputs are shown in **Figure 4.9** and **Figure 4.10**. Also, e_β is another input to Chip 2. This signal is an output from Chip 1 and was described in the previous section.

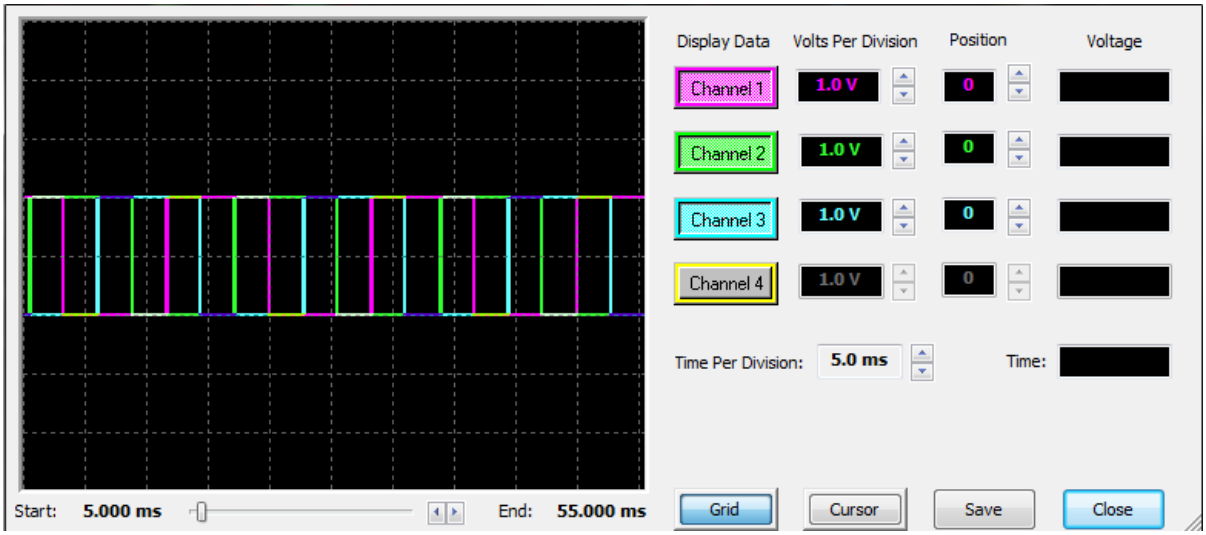

FIGURE 4.9 SIMULATION RESULTS OF INPUTS $i_a,\ i_b,\ i_c$

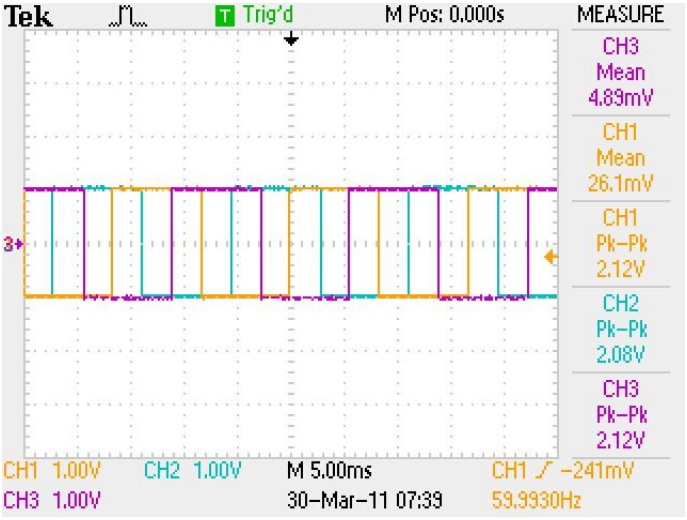

FIGURE 4.10 EXPERIMENTAL RESULTS OF INPUTS $i_a,\ i_b,\ i_c$

Other important signals produced by Chip 1 include are i_α and i_β. The simulation results and experimental results of i_α are shown in **Figure 4.11** and **Figure 4.12**. Similarly, the results for i_β are given in **Figure 4.13** and **Figure 4.14**. These two signals

are also in quadrature, but this cannot be seen directly from the figures because of their unique shapes. Therefore, the signals are considered individually here.

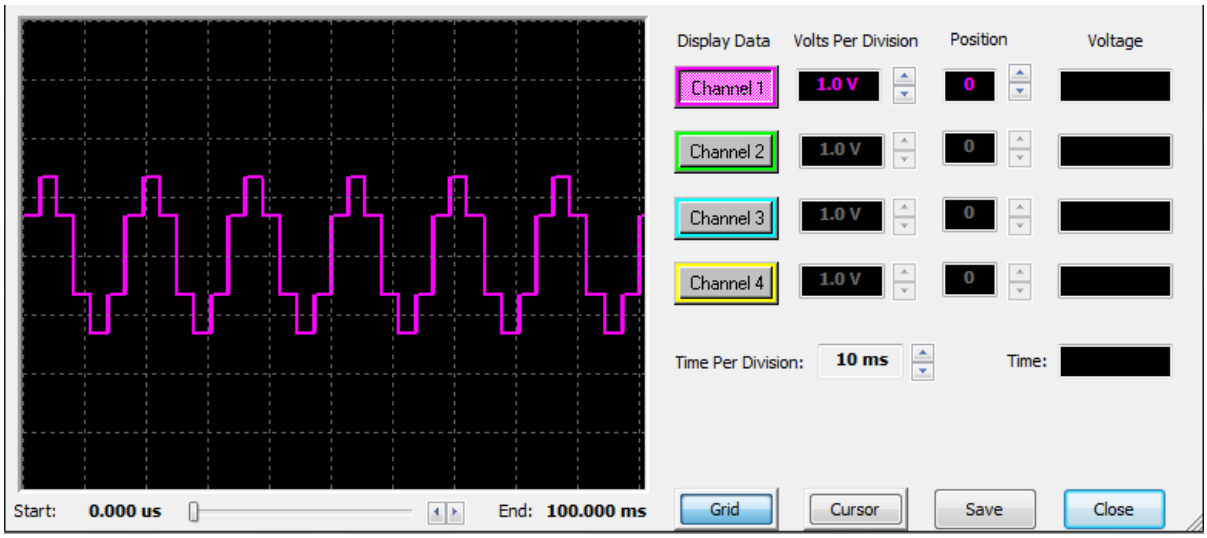

FIGURE 4.11 SIMULATION RESULTS OF i_α

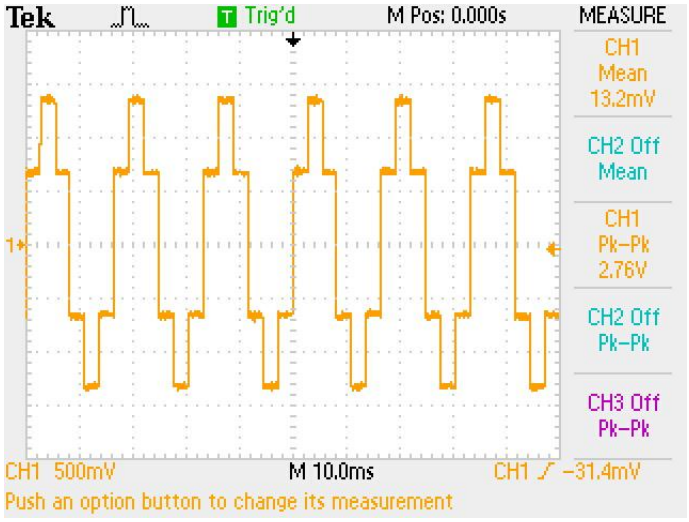

FIGURE 4.12 EXPERIMENTAL RESULTS OF i_α

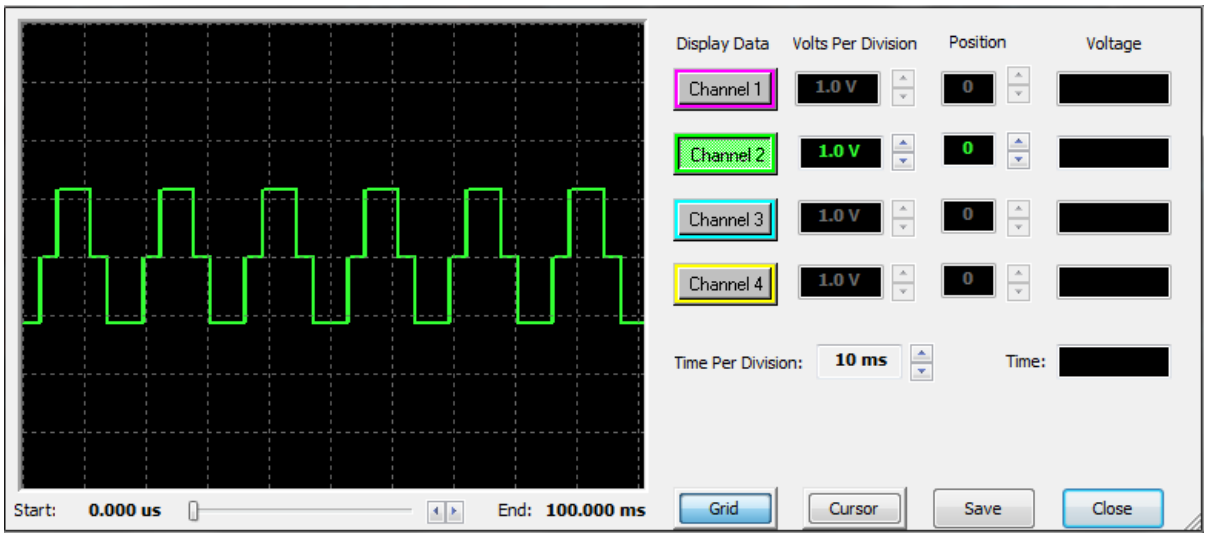

FIGURE 4.13 SIMULATION RESULTS OF i_β

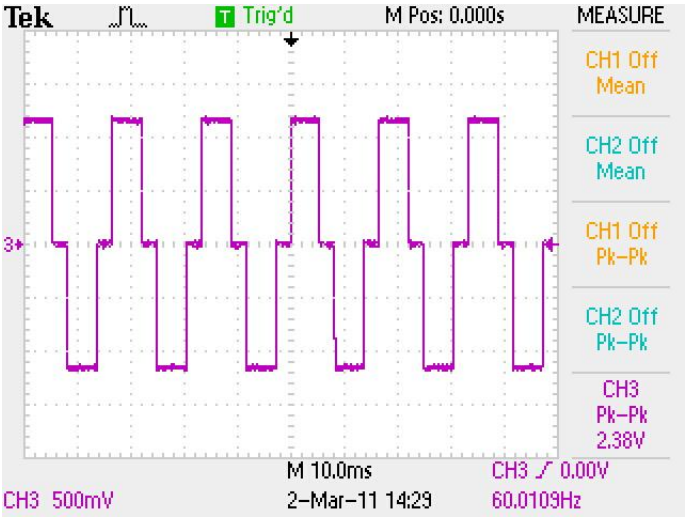

FIGURE 4.14 EXPERIMENTAL RESULTS OF i_β

The simulation results and experimental results of output $i_\alpha e_\beta$ are shown in **Figure 4.15** and **Figure 4.16**.

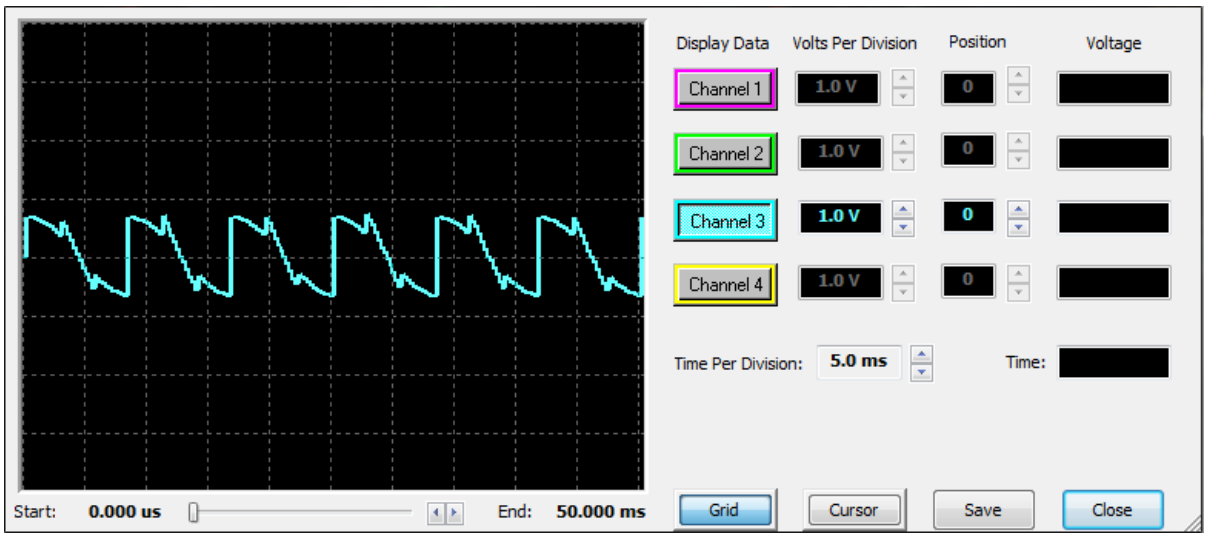

FIGURE 4.15 SIMULATION RESULTS OF $i_\alpha e_\beta$

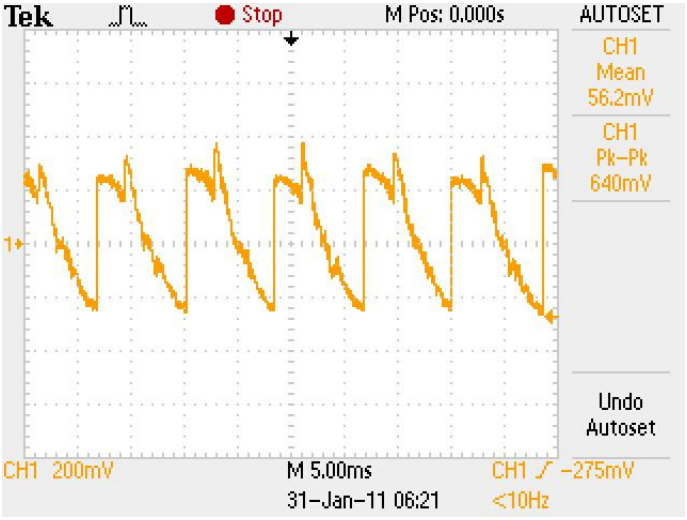

FIGURE 4.16 EXPERIMENTAL RESULTS OF $i_\alpha e_\beta$

4.1.3 CHIP 3

The design of Chip 3 is shown in **Figure 4.17**.

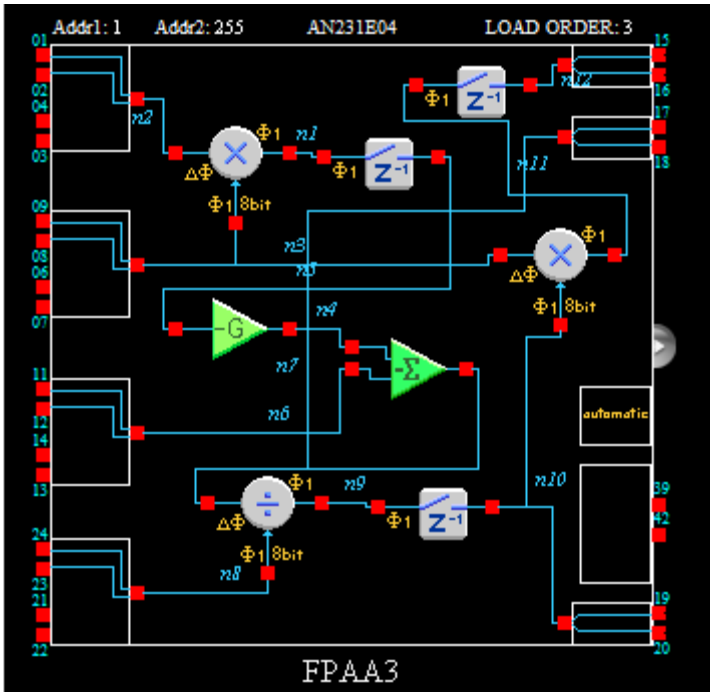

FIGURE 4.17 CHIP 3

Inputs: $-(e_\alpha^2 + e_\beta^2),\ e_\alpha,\ i_\alpha e_\beta,\ i_\beta$

Outputs: $-\frac{q}{(e_\alpha^2+e_\beta^2)},\ -\frac{e_\alpha q}{(e_\alpha^2+e_\beta^2)}$

Chip 3 produces the important signal q, the oscillating power as described in Chapter 2. The simulation results and experimental results of output q are shown in **Figure 4.18** and **Figure 4.19**.

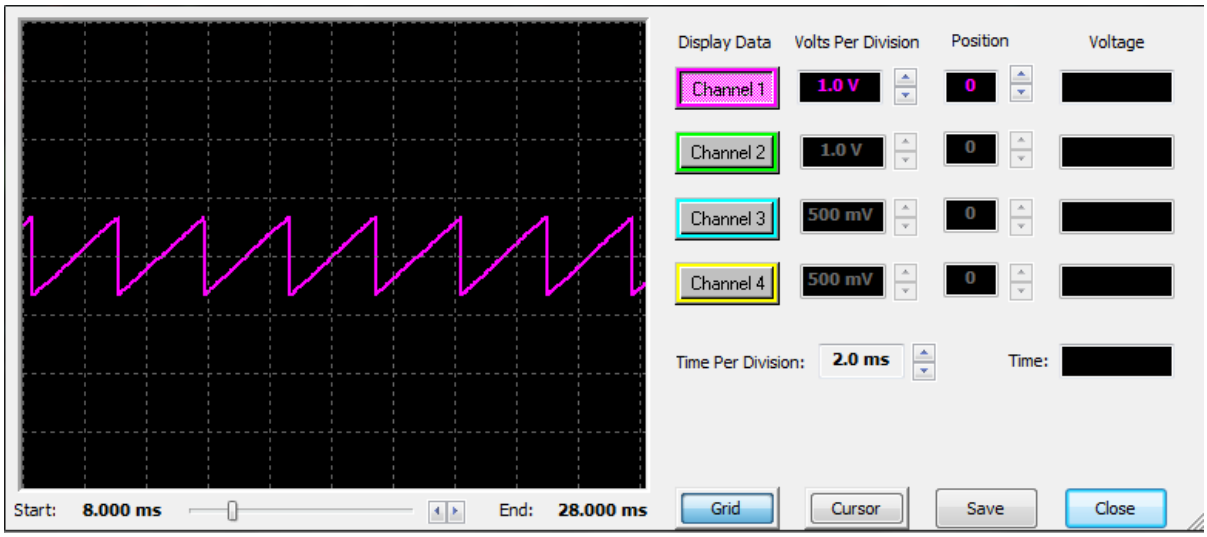

FIGURE 4.18 SIMULATION RESULTS OF Q

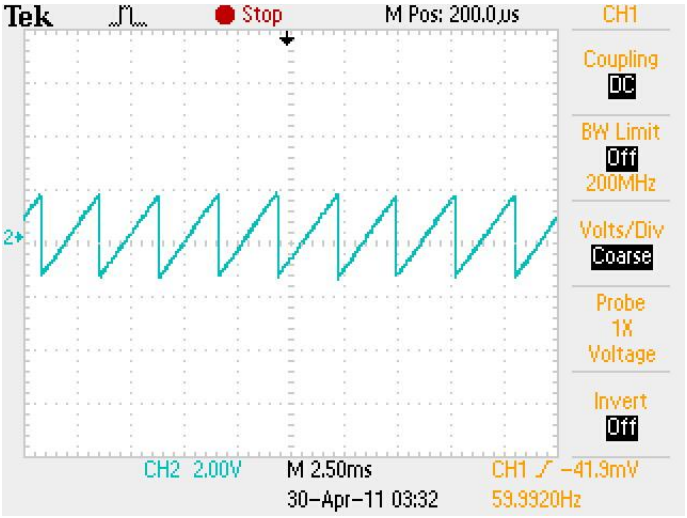

FIGURE 4.19 EXPERIMENTAL RESULTS OF Q

4.1.4 CHIP 4

The design of Chip 4 is shown in **Figure 4.20**.

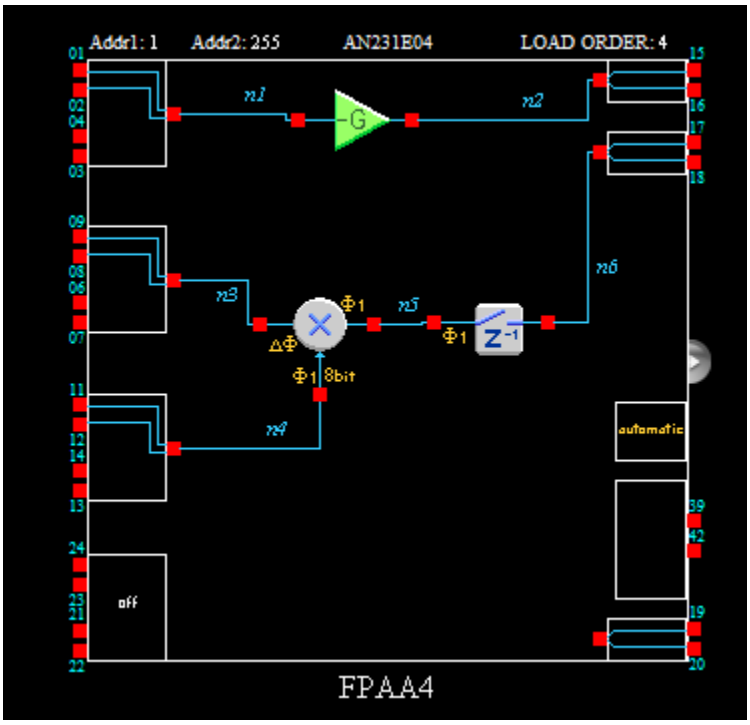

FIGURE 4.20 CHIP 4

Inputs: $-\frac{q}{(e_\alpha^2+e_\beta^2)}$, $-\frac{e_\alpha q}{(e_\alpha^2+e_\beta^2)}$, e_β

Outputs: $\frac{e_\alpha q}{(e_\alpha^2+e_\beta^2)}$, $-\frac{e_\beta q}{(e_\alpha^2+e_\beta^2)}$ (same as $i_{C\beta}$ and $i_{C\alpha}$ respectively)

The simulation and experimental results of the outputs $i_{C\beta}$ and $i_{C\alpha}$ are shown in **Figure 4.21**, **Figure 4.22**, **Figure 4.23**, and **Figure 4.24**.

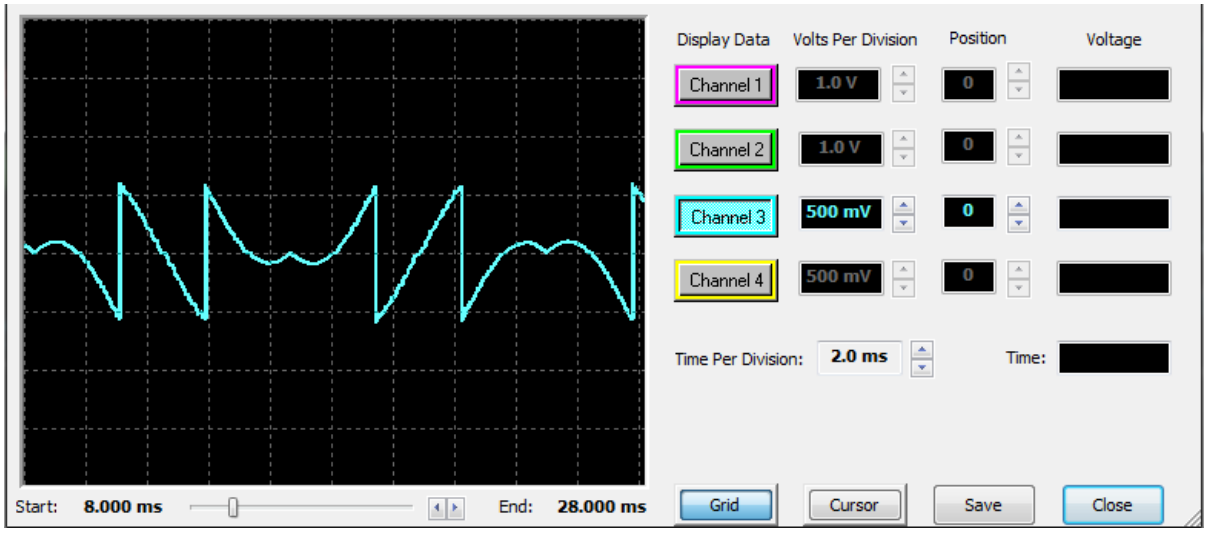

FIGURE 4.21 SIMULATION RESULTS OF $i_{c\beta}$

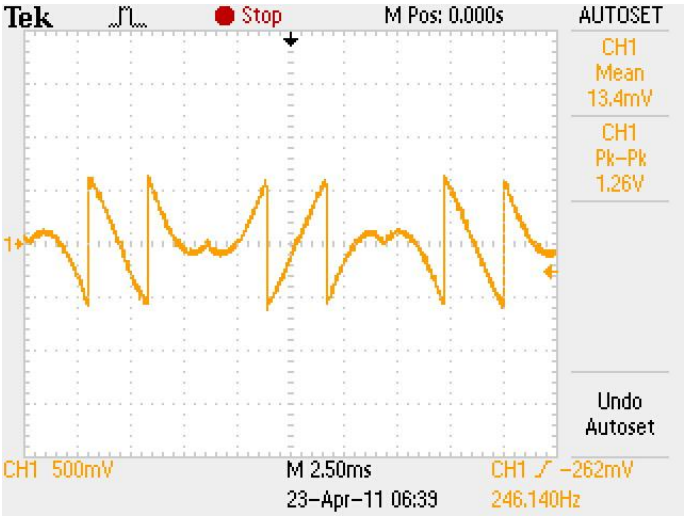

FIGURE 4.22 EXPERIMENTAL RESULTS OF $i_{c\beta}$

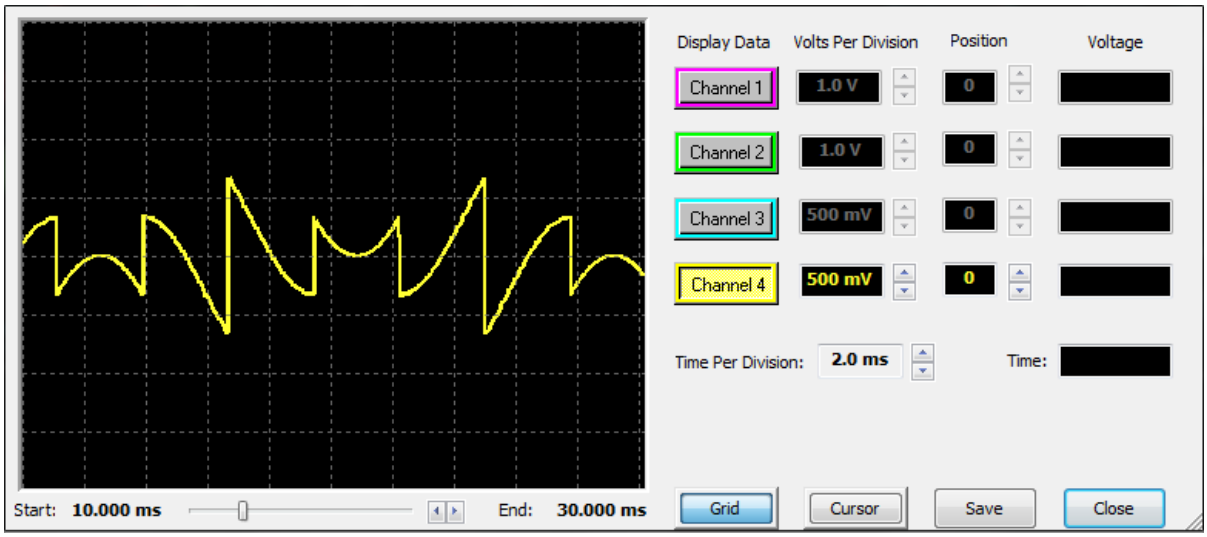

FIGURE 4.23 SIMULATION RESULTS OF $i_{C\alpha}$

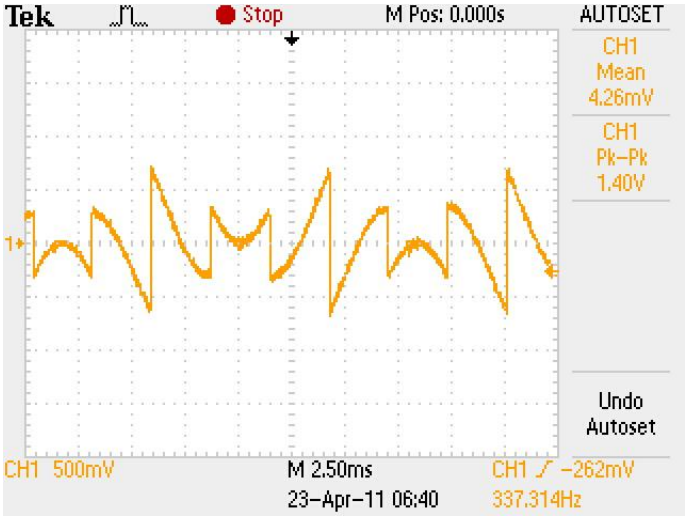

FIGURE 4.24 EXPERIMENTAL RESULTS OF $i_{C\alpha}$

4.2 FINAL OUTPUTS

This section reiterates the overall results of the PQ Theory implementation focusing on the inputs and outputs of the design in its entirety.
The inputs to the Active Filter Controller are the three phase currents and three phase voltages as shown in **Figure 4.25**.

The Active Filter Controller outputs the compensating reference currents, $i_{C\beta}$ and $i_{C\alpha}$. The compensating currents have been left in two-phase because the predictive current controller only requires the two-phase currents to generate the pulses for the inverter. The Experimental outputs are given in **Figure 4.26** and **Figure 4.27**.

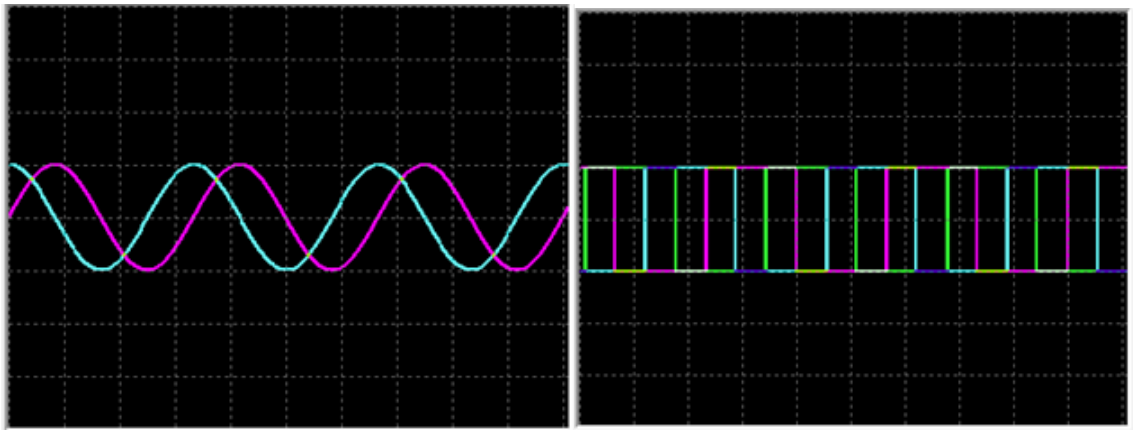

FIGURE 4.25 INPUTS TO ACTIVE FILTER CONTROLLER: 3 PHASE VOLTAGE, 3 PHASE CURRENT

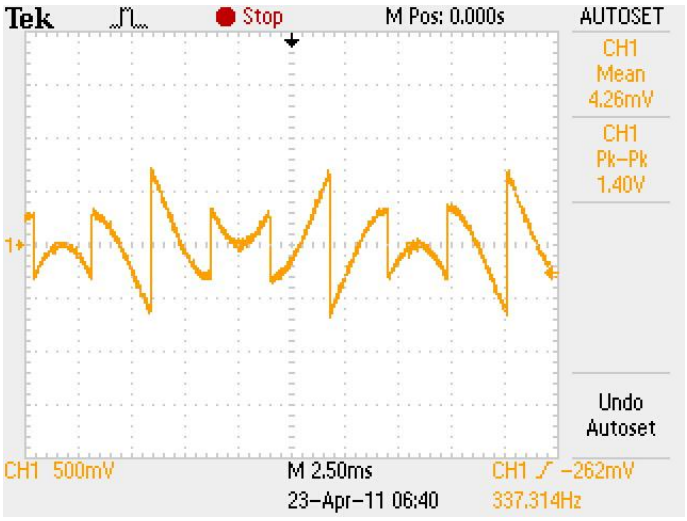

FIGURE 4.26 OUTPUT $i_{C\alpha}$ OF ACTIVE FILTER CONTROLLER

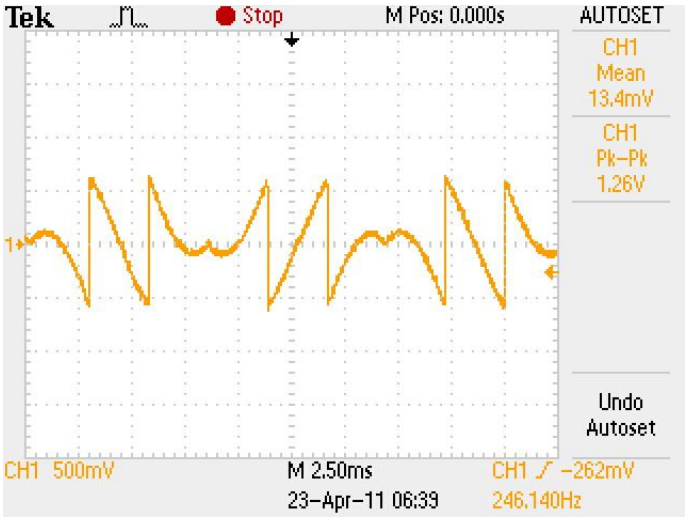

FIGURE 4.27 OUTPUT $i_{C\beta}$ OF ACTIVE FILTER CONTROLLER

5 C-RIO IMPLEMENTATION OF PQ THEORY

The National Instruments C-RIO is a programmable automation controller that contains swappable industrial I/O modules. The C-RIO is powered by reconfigurable I/O (RIO) FPGA technology.

The C-RIO system consists of a reconfigurable chassis that contains the user-programmable FPGA, hot swappable I/O modules, and a real time controller. The chassis connects the controller and the I/O modules. Graphical LabVIEW software is used to program the FPGA.

The PQ theory was also implemented[1] on the Compact-RIO (C-RIO). The LabVIEW diagram of the implementation is shown in **Figure 5.1** and **Figure 5.2**.

[1] The PQ Theory implementation on the C-RIO was done with the help of Eric Green.

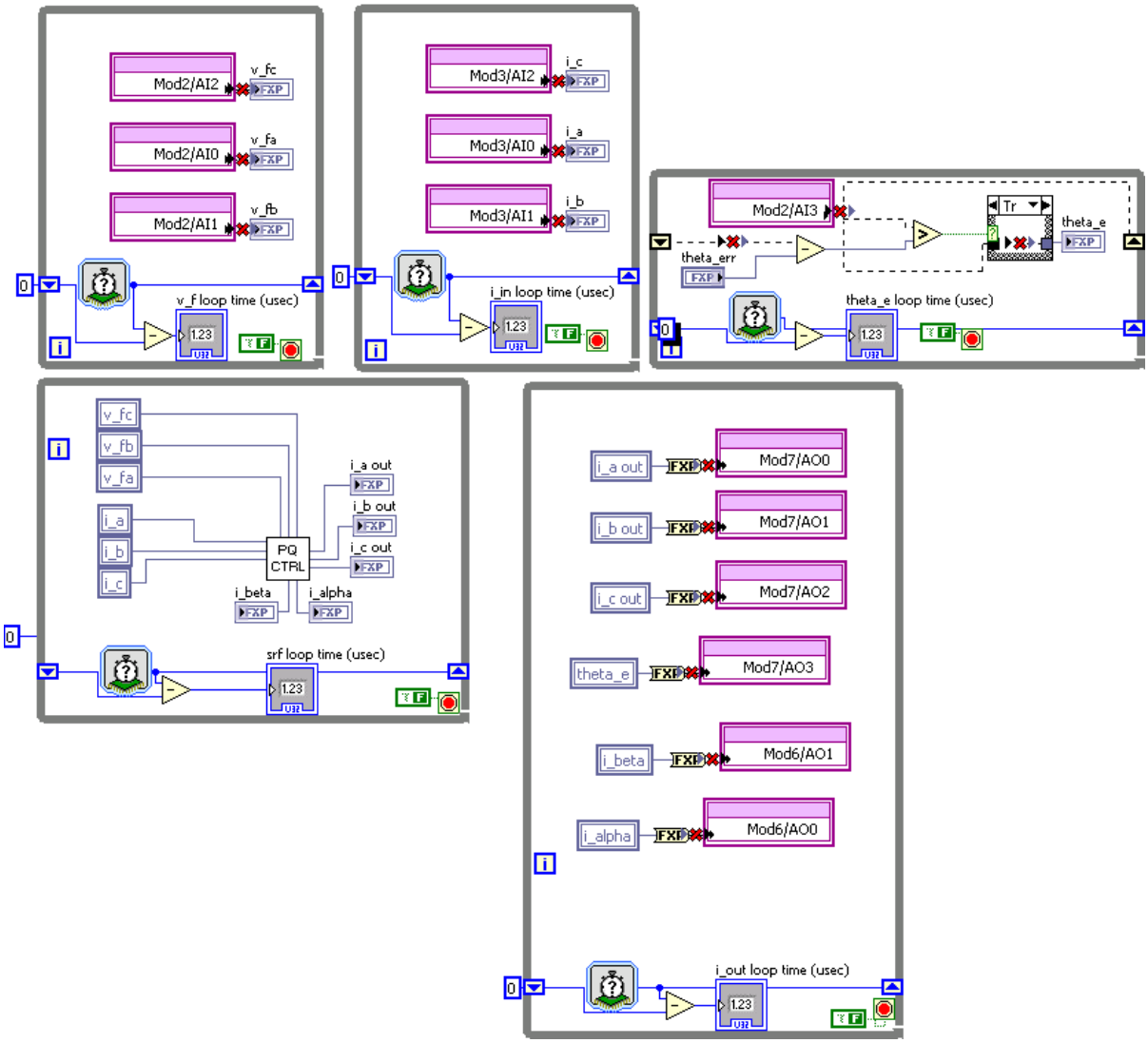

FIGURE 5.1 OVERALL DIAGRAM OF PQ THEORY IMPLEMENTATION ON C-RIO IN LABVIEW

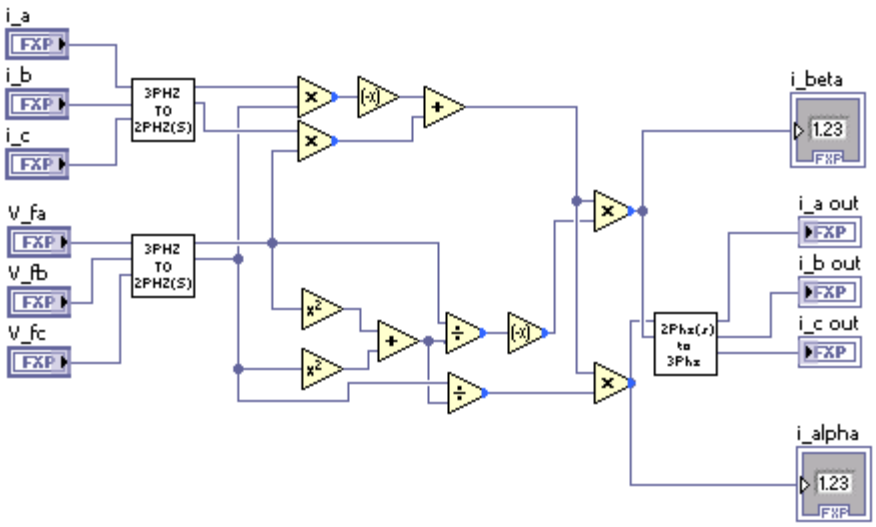

FIGURE 5.2 DIAGRAM OF PQ CONTROLLER IN LABVIEW

The outputs of $i_{C\beta}$ and $i_{C\alpha}$ from the C-RIO are shown in **Figure 5.3**. These results match with both the FPAA and Matlab Simulation Results. The delay of this implementation and the delay from the FPAA implementation will be compared in the following chapter.

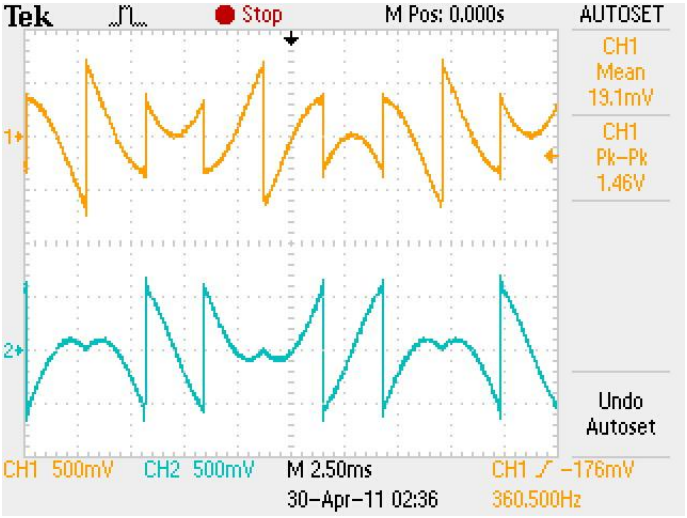

FIGURE 5.3 OUTPUT FROM C-RIO: $i_{C\alpha}$ (TOP) AND $i_{C\beta}$(BOTTOM)

6 COMPARISON OF IMPLEMENTATIONS

To determine whether the FPAA implementation was indeed faster than its digital counterparts, the delays produced by each implementation will be compared.

The delays were measured by calculating the time difference between the zero crossings of two points (one point on the input signal, e_a ,and the other on the output signal, $i_{C\beta}$). These points were chosen because the zero crossings are ideally supposed to coincide.

Figure 6.1 shows the delay in the implementation using C-RIO. **Figure 6.2** shows the delay for the FPAA implementation.

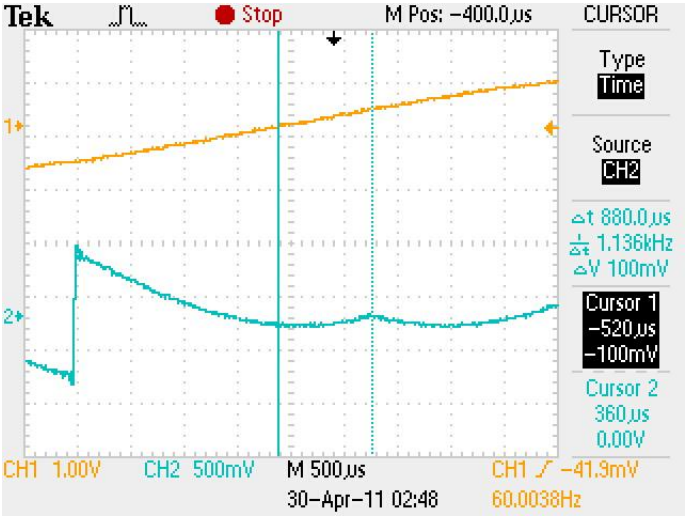

FIGURE 6.1 DELAY IN C-RIO IMPLEMENTATION

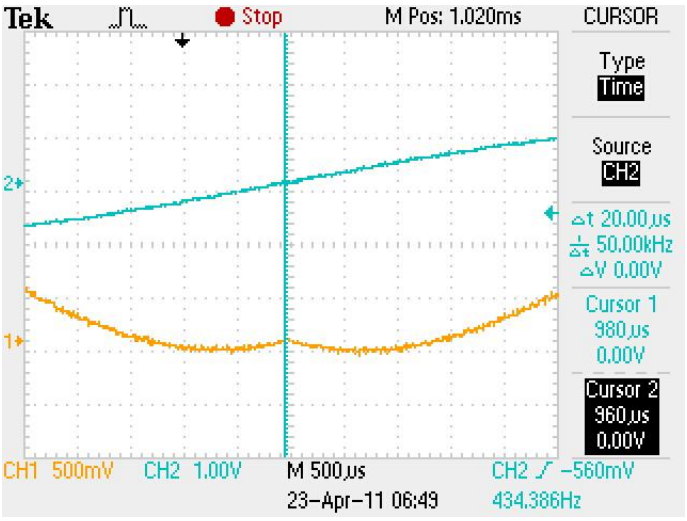

FIGURE 6.2 DELAY IN FPAA IMPLEMENTATION

The delay for the C-RIO Implementation is 880µs. The delay in the FPAA Implementation is 20µs. Therefore, the FPAA implementation of the PQ theory does reduce the delay compared to the digital implementation on the C-RIO. The FPAA implementation is 97.7% faster than the C-RIO implementation.

7 CONCLUSION

There is a need for Active Filter inverters to be switched at very high frequencies in order to match the harmonic requirement of the load. The next generation of Active Filters using Silicon Carbide (SiC) can achieve switching frequencies as high as 50-100KHz. For such devices, there is a need for a high speed controller which can be used to switch the inverter at these high speeds.

Current methods of designing Active Filter controllers include design of analog chips of using FPGAs and DSP. These methods involve much time in processing the signals.

In this research, FPAAs were considered for the controller, because of their simple method of design and flexibility. In implementing PQ theory, on specific type of Active Filter Controller, the FPAAs were indeed faster than the FPGA implementation by about 97.7%. Thus, FPAAs could potentially be an alternative to current methods of implementing Active Filter controllers.

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