ABSTRACT

SINGH, SHIKHAR. Development of Effective and Efficient Digital Control Architectures for a Scalable and Flexible Electrical Power System of Cube-Satellites and Small Satellites. (Under the direction of Dr. Subhashish Bhattacharya).

This thesis presents the hardware and software aspects of the development of digital control methodologies of configurable power systems. An electrical power system of a Cube-Satellite is developed and is used as a test bed for implementation of the various control algorithms necessary for such photovoltaic – battery based power management systems. The system consists of programmable battery charging modules and multi-domain voltage supplies along with path selection capability. The introduction of a digital controller to such power systems provide the system added flexibility and intelligence but also introduce controller design challenges with many control loops running simultaneously and being controlled by a single controller. This thesis reports the implementation of a control scheme that takes into account various parameters like load transients, control loop update rate and sampling intervals that have an effect on the system performance. Several design tradeoffs and their impact on the performance of the system are identified and a system which regulates the voltage or current within specified limits and at the same time capable of running multiple control loops is developed. The test bed behaves like a standalone photovoltaic battery charging system that harnesses solar energy to charge the battery banks. This entails the development of maximum power point tracking techniques as well as battery charging methods such as constant-current/constant-voltage charging. A dual loop control methodology with output current control is implemented to regulate the output current when charging the battery. A new CubeSat which uses Gallium Nitride MOSFETs as the primary switching devices is also developed. This new Electrical Power System - EPS aims to reduce power losses and also have all the capabilities of its silicon counterpart in a smaller form factor. This increases its portability and also makes it feasible to add more functionality with the same or even smaller dimensions.

Development of Effective and Efficient Digital Control Architectures for a Scalable and Flexible Electrical Power System of Cube-Satellite and Small Satellites

by
Shikhar Singh

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APPROVED BY:

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Dr. Subhashish Bhattacharya
Committee Chair

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Dr. Alexander G. Dean Dr. H Troy Nagle

DEDICATION

TO

MY PARENTS

SUNITA & SATYA PRAKASH

BIOGRAPHY

Shikhar Singh was born on September 8, 1990 in Delhi, India. He completed his schooling from BVB's Nand Vidya Niketan, Surat (Gujarat), India. He graduated from National Institute of Technology, Surat with a Bachelor of Technology degree in Electronics and Communication Engineering. He is currently pursuing a M.S in Computer Engineering from North Carolina State University. Since August 2012, he has been working at the FREEDM Systems Center as a Research Assistant. His research focusses on digital control of power converters, photovoltaic battery charging systems and GaN device based circuits.

Shikhar was a vocational intern at Infocom and Process Instrumentation departments at the Oil and Natural Gas Corporation Ltd. (ONGC), India. He worked with Hi-Rel Eletronics, India as an intern during the period of May – Aug 2011 where he developed automated debugging interface for UPS circuit boards. He was employed with IBM Emerging Technologies Institute as a Software Intern. He worked with the hardware acceleration group to develop hardware for Internet Scale Messaging.

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I thank Dr. Bhattacharya for trusting me and my abilities for this project. I have learned a lot under your guidance. Working with you for the last two years has been an enriching experience, academically and otherwise.

I thank Dr. Dean for his insightful suggestions and his constant support helped this project be directed towards useful and logical milestones. Your help with the embedded control design and software support has been critical to the successful execution of the project. Dr. Nagle, I express my gratitude for accepting to become a member of the committee.

I thank Mihir for introducing me to the project, for his constant guidance and help throughout the course of my work. Thank you Avik for bringing me up to date with the software of the project and helping me with the compensator designs. I thank my team mates Rohit, Udai, Dan, Si Li for the numerous discussions and suggestions regarding my work. Samir, Sachin, Ankan, Sumit, Awneesh and Arun, thank you for your valuable advice. Hulgize and Karen, it wouldn't have been possible to complete the project without your support with the lab equipment and orders. Swapnil, Bharat, Sushmit, Dhaval, Nidhi & Rita; thank you for making this journey a joyous and memorable affair. Thank you Daddy, Ma and Shireen for your constant belief in me. Your love gave me strength and conviction to complete the project.

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CHAPTER 1
Introduction

The most remarkable feature of space exploration and research in the past few decades has been the exciting rate at which space technologies have expanded their horizon. Gone are the days when such projects were either under the ambit of government or were funded by large corporate enterprises. The recent past saw an emergence of research centers, which are academic and involve many professors, students and hobbyists. Space technologies have become more accessible and this has enthused a lot of interest in academic institutions to contribute towards such research [1]. The noteworthy part of such a transformation is the fact that such centers are not only confined to the developed regions of the Americas and Europe; developing nations like China and India are channeling significant resources in developing these R&D centers. This phenomenon was seen in action when SRMSAT, a nano-satellite developed by students at SRM University, India was launched from the Indian Space Research Organization's Satish Dhawan Space Center [2].

CubeSat is a generic term for a miniature satellite which is designed using commercial off-the-shelf components for development of its electronics framework. A CubeSat fits perfectly in the scenario discussed in the previous paragraph as a majority of the development and launches come from the academia. The use of off-the-shelf components enables almost anyone to develop his/her own satellite. CubeSat provides a viable and cost effective way for universities and colleges to contribute towards space research.

This thesis discusses the design and development of an effective, cost effective, multi domain and scalable electrical power system of a CubeSat. This involves addressing issues like solar power harnessing, battery charging mechanism, DC-DC converter design and control, load characterization and analysis.

Shailesh Notani [3] in his thesis carried out the technical survey of the current CubeSat technology and trends. He discussed the merits of different systems available in the market and developed the first version of the EPS board which adheres to the proposed design specifications. He also published some preliminary results. Mihir Shah [4] followed the work of Notani and carried out an exhaustive testing of the circuit making enhancements and developing the second version of the EPS board. Shah also carried out experiments with implementing the CubeSat EPS as a testbed for testing the concept of dynamic voltage scaling in portable embedded systems. This work builds on the work carried out by Notani and Shah.

Chapter 2 introduces the concept of CubeSat with its technical specifications, characteristics and the various building blocks. It also introduces the Electrical Power Subsystem of the CubeSat.

Chapter 3 discusses in detail, the electrical power system of a CubeSat. The necessary and desirable features for such a system are discussed along with the proposed architecture. Some commercially available EPSs are also surveyed and their architectures are analyzed.

Chapter 4 discusses the hardware design of the EPS and its various sections – the solar power harnessing system, battery management circuitry, point of load converters, path selection and switching, power failure recovery and current/voltage sensing. It also discusses the enhancements made in the current version of the EPS board. Chapter 5 deals with the digital controller design of the system. This involves the control loop design of the various power converters on the system. The small signal modeling of DC-DC converters with the real time loads is developed to design compensators that adhere to the performance specifications. The photovoltaic or PV charging system design is developed which involves the development of maximum power point tracking or MPPT algorithms and the battery state machine for constant current and constant voltage CC-CV charging.

Chapter 6 delves into software design of the system and discusses the necessary features of the code layout that ensures reliable and efficient operation of intelligent power systems like the EPS of a CubeSat. A software model is developed for the power management system and its integration with the operating system.

Chapter 7 discusses the design of the hardware for the GaN device based CubeSat EPS. The advantages of using GaN devices over Silicon devices with respect to circuit performance and efficiency are discussed. The various building blocks of the EPS hardware are described.

Chapter 8 summarizes the observations and results of the project along with the merits and shortcomings of the proposed design. Chapter 9 lays out the future plan of work. This section also identifies key domains which demand more research and experimentation.

CHAPTER 2
CubeSat Fundamentals

2.1. Introduction

CubeSat is a generic term for a small satellite which has a volume of 1 liter, which translates into a cube having a 10 cm edge. A typical CubeSat weighs approximately 1 kilogram. The most remarkable feature of such satellites is the simplified development cycle; the use of off-the-shelf hardware and easy access to software resources had led to rapid rise in the numbers of the CubeSats deployed. The CubeSats, being highly modular, can be combined to form larger satellites.

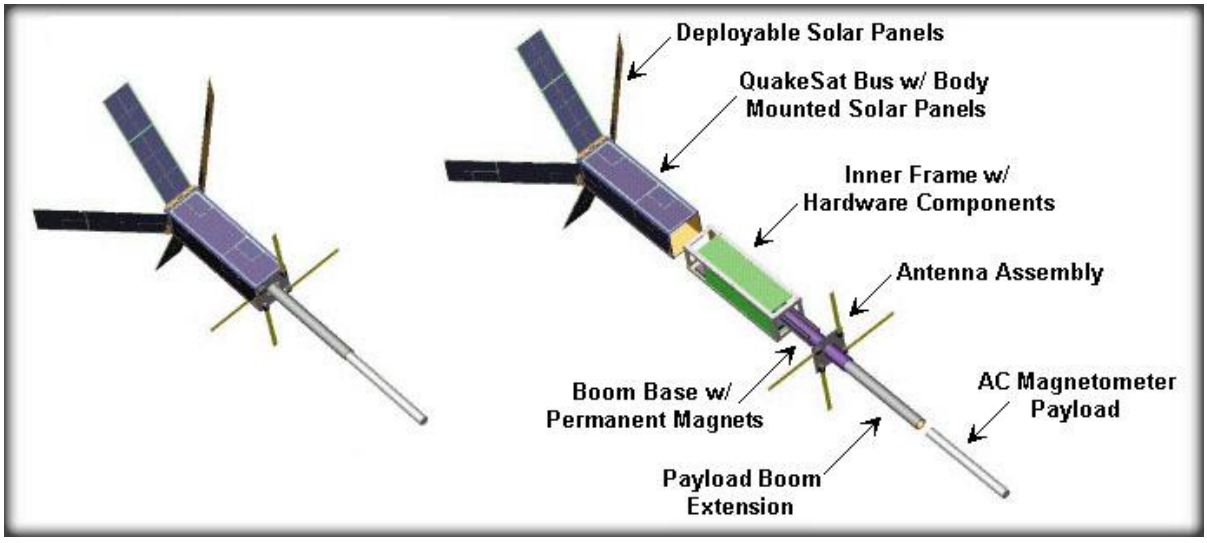

Figure 1. QuakeSat and its components

Figure 1 depicts a satellite called QuakeSat. It was one of the earliest small satellites launched for scientific research. It was in operation for more than 11 months and gathered important scientific data [5].

Since its conception in 1999 by professors Jordi Puig-Suari and Bob Twiggs from the California Polytechnic State University and Stanford University respectively [6] [7], more than 100 CubeSats have been launched. These satellites are used in a myriad of applications such as space imaging, communication, atmospheric research, biological experiments and test beds for future technologies.

The 10 x 10 x 10 cm standard dimension CubeSat is usually referred to as 1U or 1 unit CubeSat. As mentioned before, 1U CubeSats can be combined to form larger units. However, the dimensions can be increased only along a single axis and only by discrete increments of 1U. A 3U CubeSat would measure (30 x 10 x 10) cm while a 2U CubeSat would have the dimensions of (20 x 10 x 10) cm. Such scaled up models have been tested and launched.

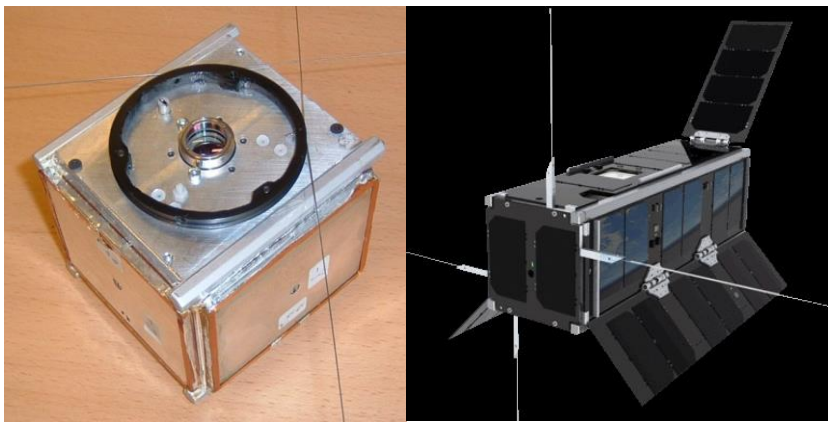

Figure 2. (a) AAU 1U CubeSat (b) UKube-1 3U CubeSat

Figure 2 shows the scalability which these CubesSats exhibit. Figure 2(a) shows the 1U AAU CubeSat developed by the students at Aalborg University with the objective of capturing images from space using a hi-resolution camera. Figure 2(b) shows UKube – 1, a 3U CubeSat developed by Clyde Space in collaboration with UK Space Agency. It will carry four payloads developed by both industry and academia.

These standardizations of CubeSat dimensions enable the use of a common deployment technology. CubeSats are deployed using an assembly called the Poly – Pico Satellite Orbital Deployer or P-POD which was developed at the California Polytechnic University. P-POD systems can have the same dimensions as every satellite adhering to the CubeSat specifications would measure 10 x 10 cm along a plane. These P-PODs are carried by a launch vehicle and once the required orbit is attained, the CubeSats are deployed. Since these P-PODs are only an add-on payload and each P-POD carries more than 1 CubeSat; the cost of deployment is reduced. Today, launching a CubeSat typically costs 100 thousand dollars which is much smaller compared to millions of dollars required to launch a commercial satellite [8].

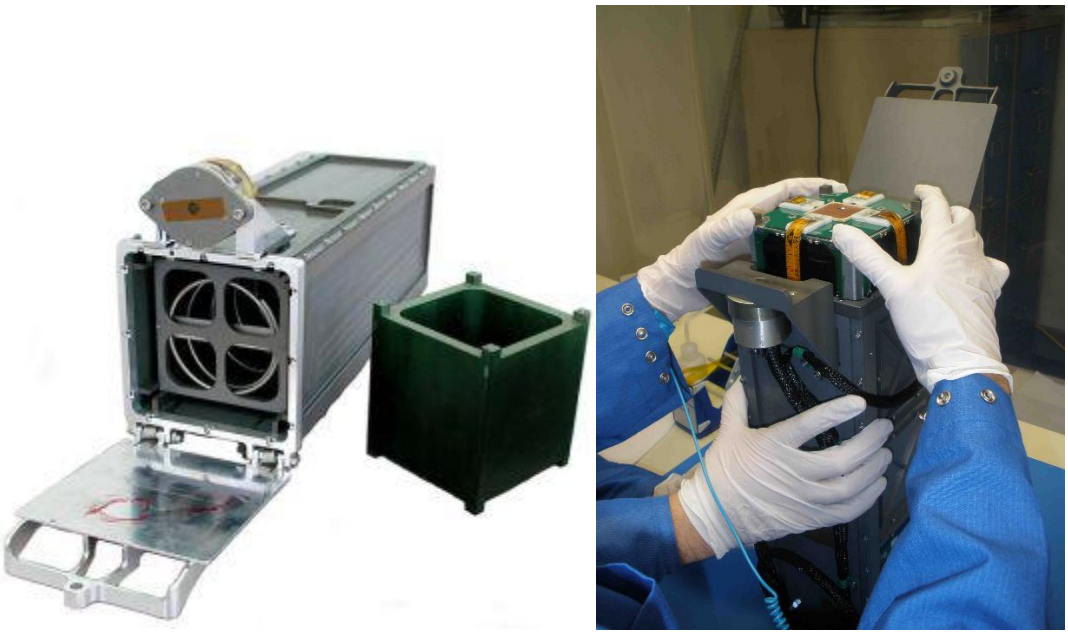

Figure 3. P-POD Assembly

Figure 3 shows the P-POD assemby. The picture on the left depicts the deployer while the figure on the rigth shows a 1U CubeSat being inserted into the deployer.

2.2 CubeSat Subsystems

A CubeSat is composed of several building blocks or subsystems that perform dedicated and specific functions. For proper functioning of the satellite, it is necessary for each subsystem to operate properly and co-ordinate with other subsystems. Figure 4 below shows the various subsystems of the generic CubeSat. These subsystems are briefly discussed in this section.

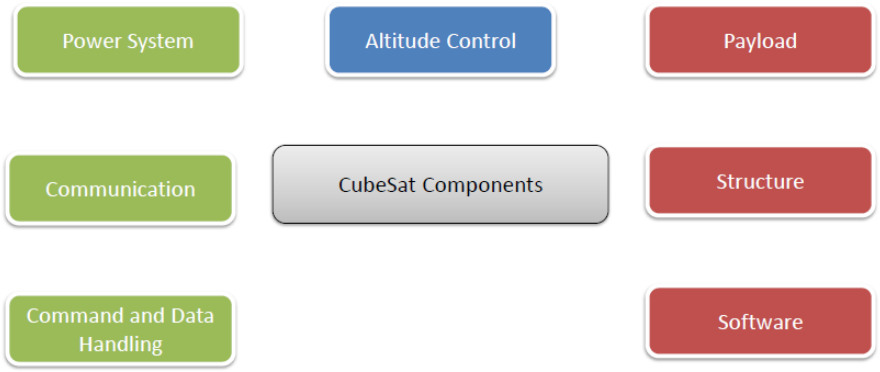

Figure 4. CubeSat Subsystems

Altitude Determination and Control

This subsystem is responsible for maintaining the satellite's orbit and orientation. Expensive and complex systems used in conventional satellites are of little utility for CubeSats which aims to use commercially available and simple building components. Therefore cost effective sensors like magnetometers, gyroscopes and flywheel assemblies form the core of the system [9]. This system maintains a proper orientation of the satellite so as to point the antennae in the direction of the ground station and hence interacts with the communication subsystem to obtain positional readings. The solar panels need to face the sun and also sensors like the camera need to be positioned so as to point to the appropriate ground location [10].

Communications

The communication system establishes the link between the ground station and the satellite. The satellite relays sensor and health data and receives commands from the ground station via a full duplex communication link managed by the communication subsystem. Limited budget prevents the development of specialized communication systems. Many of these CubeSats, especially those built by academic institutions, use commercial off-the-shelf (COTS) transceivers. These COTS transceivers are cheap but have a limited lifespan and reliability. Some scientific CubeSats use custom built transceivers. Such systems are composed of a terminal node controller (TNC) and an amplifier or an amplifier and an antenna [11]. Some companies like ISIS [12] and AstroDev [13] sell radios designed for CubeSats.

Structures

The structure comprises of the chassis and framework of the CubeSat and is responsible for supporting and holding various components like the circuit boards, sensors and batteries in place. Structures also provides protection to the CubeSat and its internal components against the harsh environments of space like temperature gradients and radiation.

Command and Data Handling

This subsystem is the central processing and management unit of the CubeSat. It coordinates and synchronizes the operation of all the other subsystems. Data processing and relay, fault management and central control are the main functions of the command and data handling subsystem.

Payload

Payload consists of the scientific and experimental apparatus carried by the CubeSat. Over the years, CubeSats have carried a wide range of payloads like cameras, weather monitoring equipment, magnetic and radiation sensors and proof of concept designs.

Software

Software subsystem provides the software infrastructure for the complete satellite system including the ground station and CubeSat control. The ground station software system is responsible for receiving and processing data from CubeSat and managing protocols for communication and sending the required commands. The CubeSat software controls the functionality of CubeSat systems. Certain algorithms that are essential to the functioning of the satellite like closed loop control, health monitoring, sensor interface and communication are run by the software system.

Electrical Power System

The EPS is the powerhouse of the CubeSat. It is responsible for powering the various components of the CubeSat which include the control unit, servo mechanisms, scientific equipment and communication modules. A CubeSat has limited battery storage given the size and weight restrictions and batteries need to be charged periodically using the energy harvested from the solar panels. Moreover, every component has different power requirements and the EPS is responsible for providing voltage supplies tailored to the needs of the components. A more detailed description of the EPS architecture is presented in the next chapter.

CHAPTER 3
Electrical Power System

This chapter deals with the architecture of the developed EPS system and a detailed description of its features. The work done by Notani and Shah who developed the previous versions of the EPS hardware is discussed. As mentioned in the previous sections, the EPS is responsible for power management in the CubeSat. It is responsible for harnessing power, battery management and power rail supply. Given these requirements, there are certain features and characteristics expected of an EPS.

3.1. EPS Features

- Scalability

  A CubeSat EPS should be able to power multiple peripherals with varying power requirements. This means that the EPS should be able to regulate multiple voltage rails with transients limited to the specifications. Hence the EPS should have multiple point of load converters producing different output voltages.
- Efficiency

  A CubeSat operates with a limited power budget. Batteries are the primary storage devices and the size and weight constraints limit its capacity. The EPS should be optimized for high efficiency so that all the available energy is utilized for useful purposes.
- Robustness

  The CubeSat operates in harsh environments of space with intense radiation and temperature gradients. As a result, there is a higher chance of system failure and the EPS needs to handle hardware faults and exceptions. The components used in construction of the EPS should be radiation resistant and should have wide temperature range of operation.

- Reliability

  An EPS should be reliable and able to withstand possible malfunctions. It should be able to redirect and route power in case one or more power processing modules fail. Features like path switching, shutdown recovery and battery failure conditions ensure reliable operation. Having multiple storage devices and power harnessing modules also helps towards making the system fault tolerant.
- Size

  A 1U CubeSat measures 10cm on each edge. This restricts the size of EPS to less than 10cm by 10cm. The design of an EPS with all of the aforementioned features given the size constraints poses significant PCB design and packaging challenges.

3.2. EPS Architecture

The features and capabilities of the EPS were described in the previous section. To summarize, a good power subsystem should be scalable, compact, robust and efficient [14]. Figure 6 is the block diagram of a generic EPS and the minimum desired modules which should be present in the EPS board. The solar panels are interfaced to the battery charging modules which is connected to the battery banks. An EPS usually has two lithium batteries so that when one is in operation the other can be charged. All the other subsystems like the Communications, Altitude Determination, etc., are powered by point of load converters which provide a regulated power bus. In case of battery failure, the solar panels can be directly interfaced to the point of load converters to keep the other systems operational. A controller sits at the heart of the system and controls the modules and runs the control loops and other protection algorithms. Notani, in his thesis, discussed the shortcomings of such an architecture with respect to efficiency, scalability and versatility.

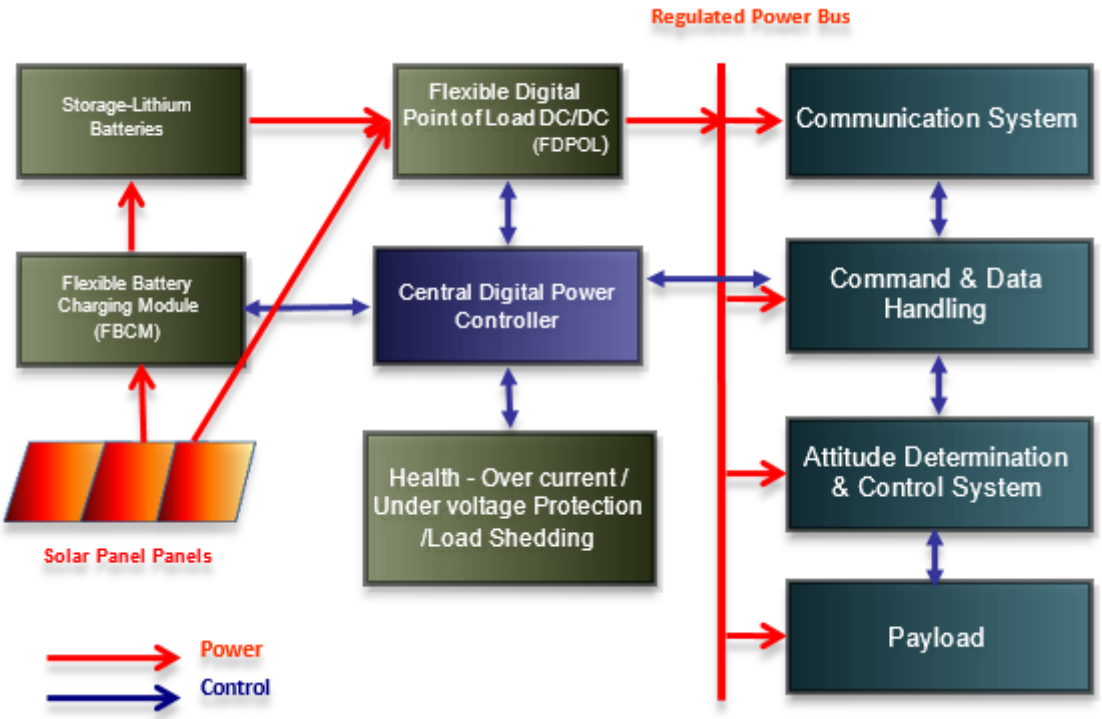

Figure 5. CubeSat EPS [3]

Figure 7 shows the proposed EPS architecture which is an upgrade to the generic CubeSat architecture shown above. The solar panels feed into the FBCM – flexible battery charging modules which are responsible for charging the lithium batteries. The FBCMs are DC-DC converters which perform a CC-CV charging of the battery. The switching circuitry directs the output of the FBCMs to the desired battery packs. The existing architecture has four FDPOL – flexible digital point of load converters which produce DC voltage rails from 3.3 V to 12V. There are two synchronous buck and two synchronous boost converters. The solar panels can directly be connected to the input of the FDPOLs in case of battery failure. The path selection circuitry connects the output of one of the battery packs to the FDPOL's input.

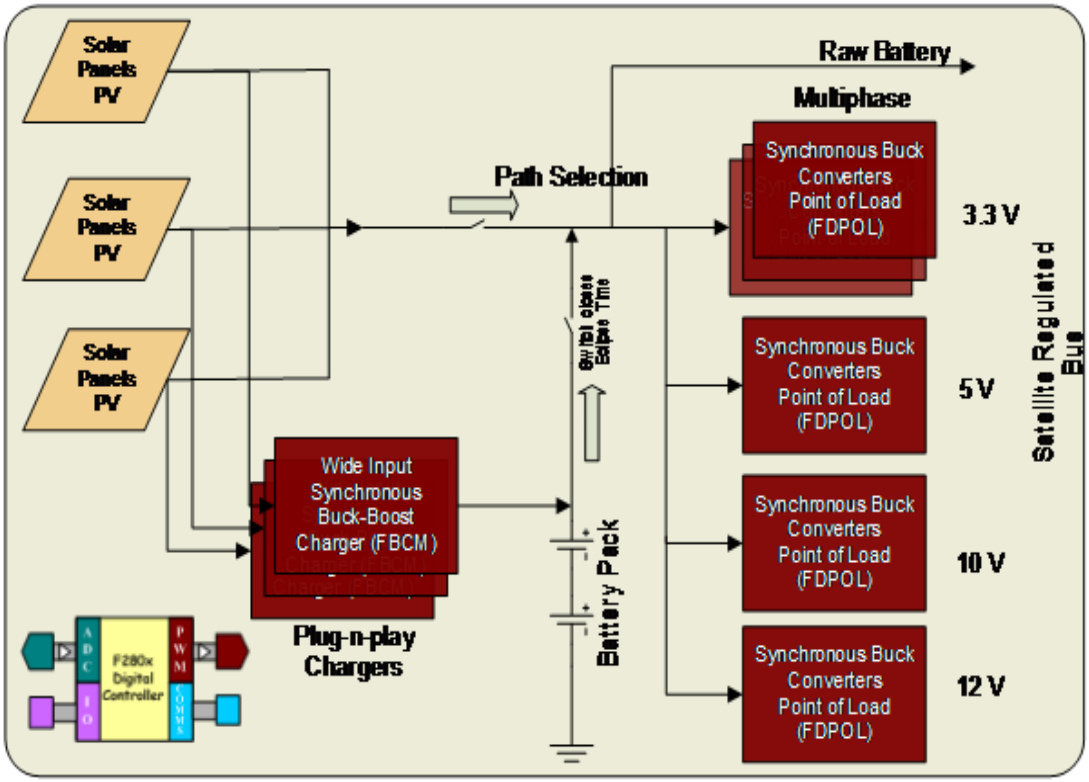

Figure 7. Proposed EPS Architecture [4]

3.3. Previous Work

The ever growing interest in CubeSats has led to the development and marketing of commercial EPSs by companies like Clyde Space [15] and CubeSat Kit [16]. These EPSs are tailored for different CubeSat sizes and hence provide customizability. Figure 8 below shows the block diagram of the Clyde Space EPS and the EPS circuit board. The BCR or battery charging regulators harness the solar energy from the solar panels positioned across the 3 axis of the CubeSat. The solar panels operate on peak efficiency using MPPT – maximum power point tracking algorithms. Each BCR interfaces to the solar arrays in a particular axis. The BCRs produce a regulated battery bus which charges the battery. There are two output regulators providing a rail voltage of 5V and 3.3V.

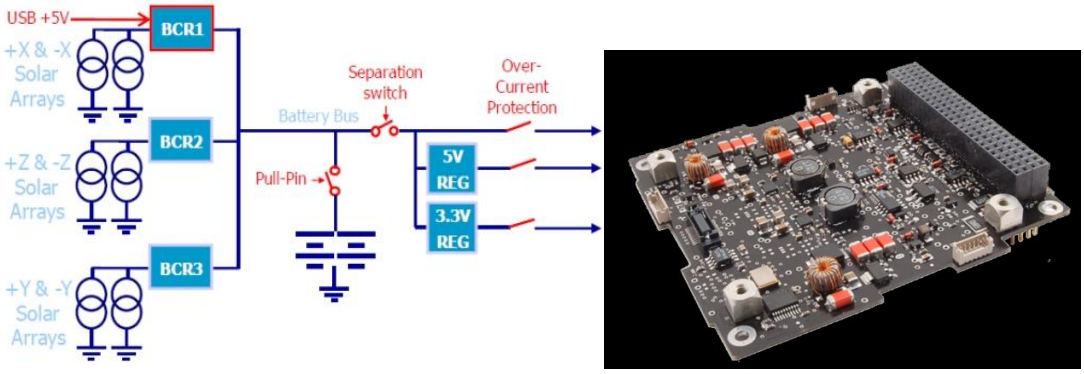

Figure 8. Clyde Space EPS

In his thesis [3], Notani proposed the basic hardware architecture of the EPS. He determined the desired features and worked towards designing the necessary hardware. He developed the software model of the various constituents of the EPS like the solar panel connections, the MPPT control loop and the FBCM and FDPOL control loop modeling. Notani developed a version of the CubeSat EPS and carried out some preliminary hardware testing. Figure 9 depicts the first EPS prototype board.

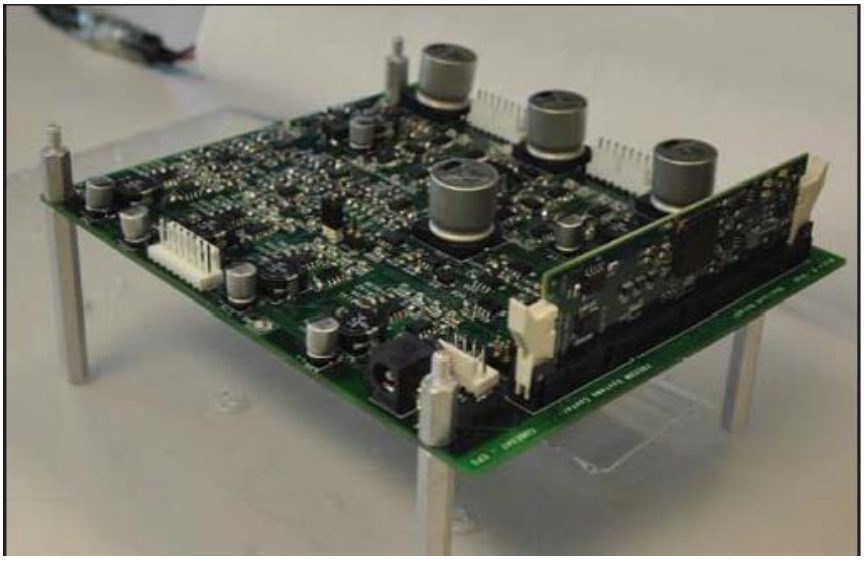

Figure 9. CubeSat EPS - Version 1

Shah [4] continued the work of Notani and developed the second revision of the EPS board. He carried out extensive hardware testing of the board and eliminated all the faults in the previous version. He also created a GUI based debugging interface to monitor real time parameters of the board. He also developed the current sensor card of the EPS which enabled the use of current control techniques. Figure 10 shows the second version of the EPS board along with the current sensor board.

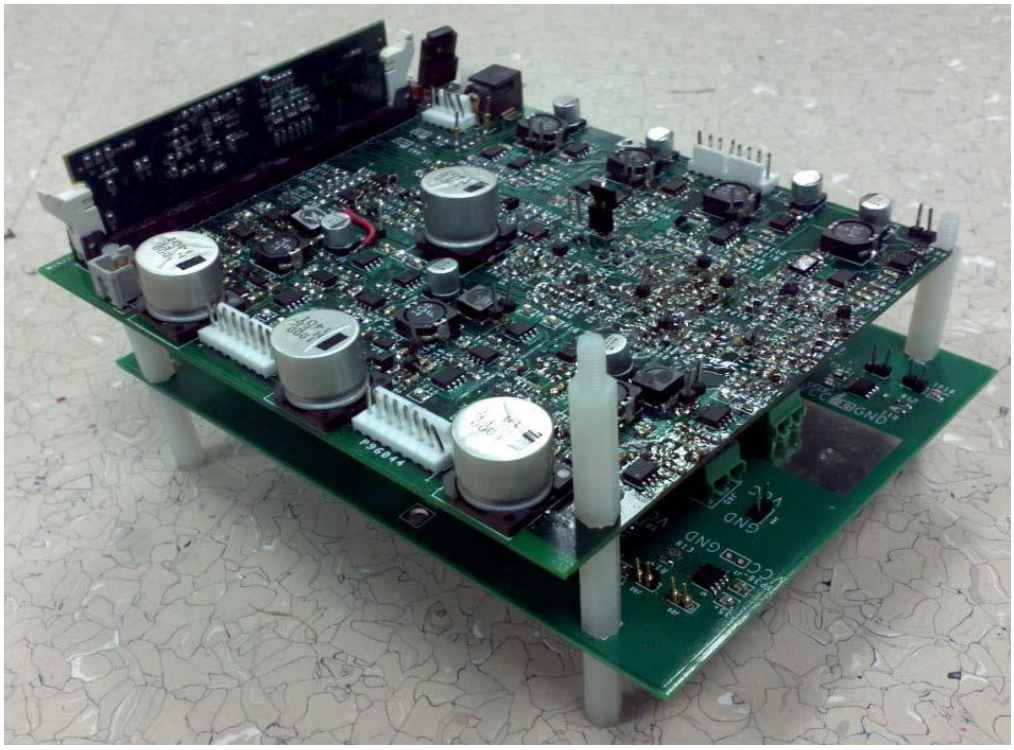

Figure 10. CubeSat EPS - Version 2

CHAPTER 4

Hardware Design

This chapter describes the hardware design of the board. The EPS circuit can be divided into modules that perform dedicated operations. A detailed analysis of these modules is undertaken with an emphasis on the hardware design aspect of the system. Figure 11 shows the test setup of the EPS. It is connected to two battery packs and it interfaces to six solar panels of the type seen in the background. Figure 12 is that of the top view of the EPS board that shows the various component modules. The board measures 5 x 4 inches.

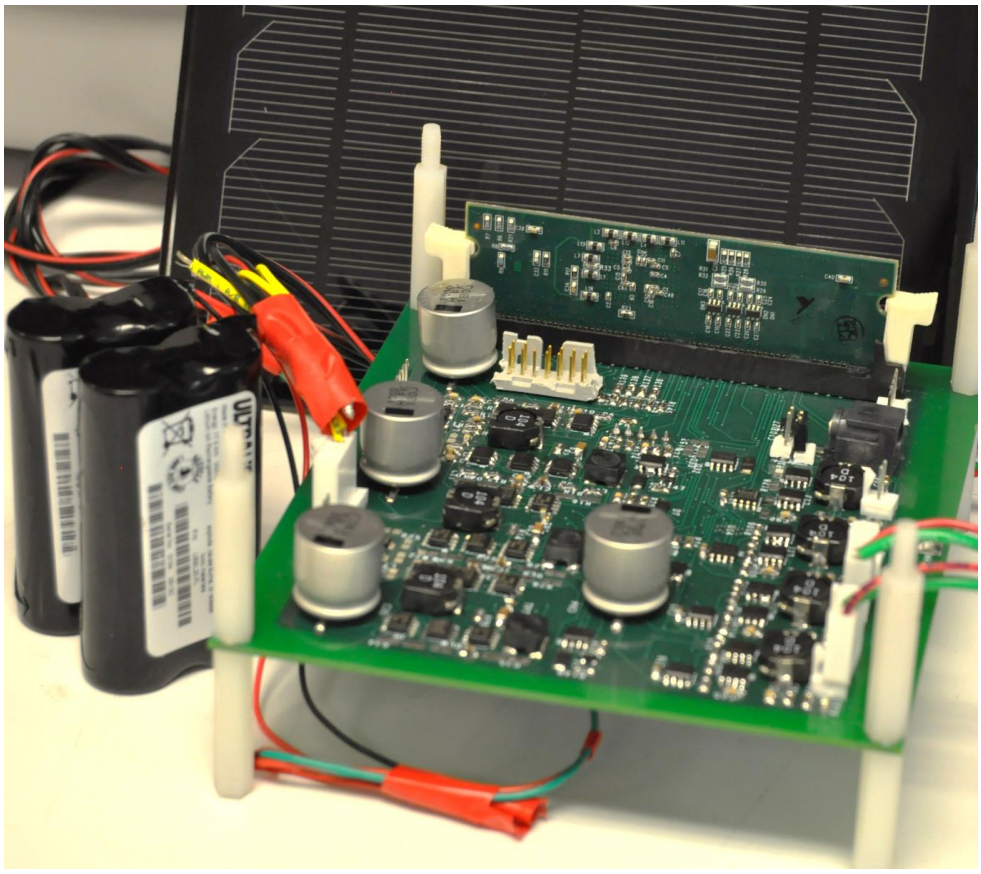

Figure 11. EPS Test Setup

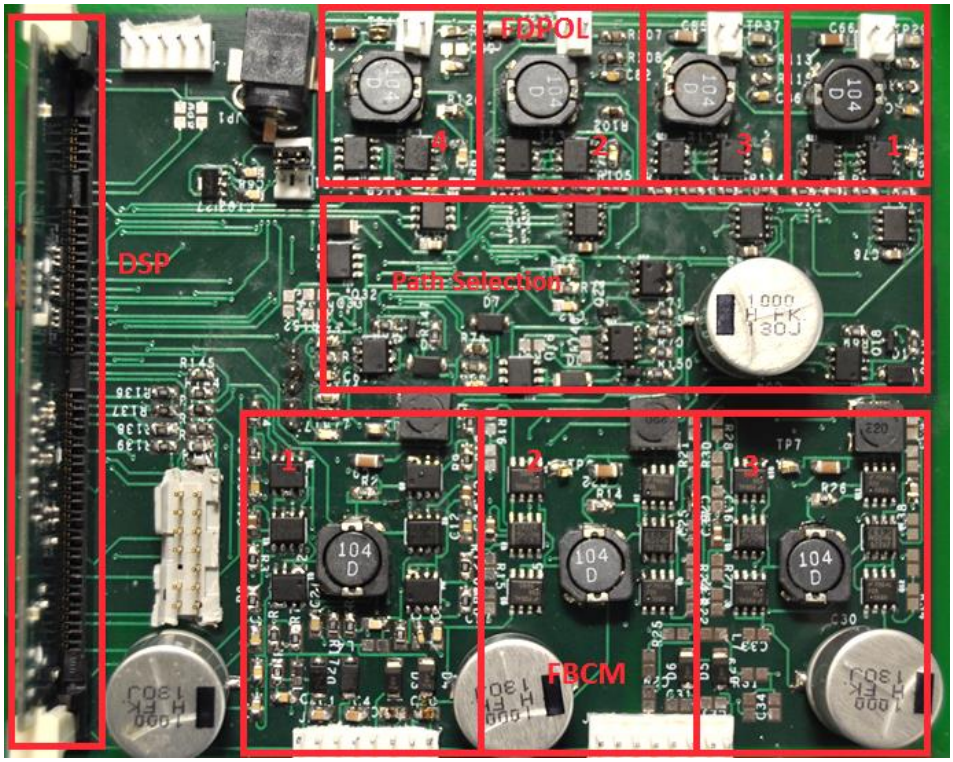

Figure 12. EPS Board Components

4.1. Flexible Battery Charging Modules

The FBCMs or flexible battery charging modules are responsible for harnessing solar power to keep the battery banks adequately charged. The structure of an FBCM module is a buck converter followed by a boost converter. The input voltage and current from the solar panel are measured to track the maximum power point. Depending on the input voltage, either the buck or boost part of the circuit is operational to output the required voltage. An inductor is placed after the output capacitor to provide a continuous output current when the boost mode is in operation. Figure 13 shows a FBCM module, transistors Q1 to Q4 are the switching components and inductor L2 acts as the common inductor for both the buck and boost configuration.

Sense resistors R1 and R2 are used for sensing the input and inductor current respectively. C9 is the output capacitor and L6 is small coil placed at the output of the module that makes the output current continuous. The outputs of the three FBCMs are combined and connected to the battery banks.

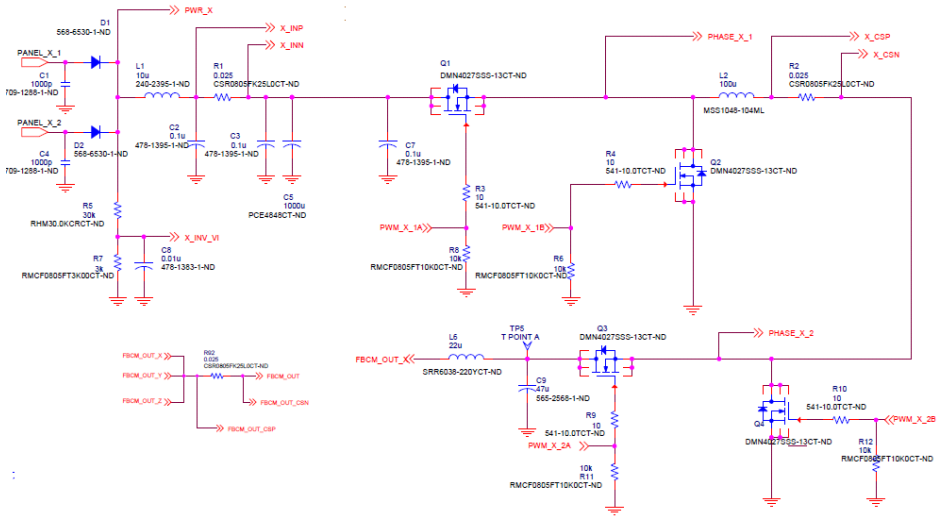

Figure 13. EPS - Flexible Battery Charging Modules

4.2. Flexible Digital Point of Load Converter

Flexible digital points of load converters or FDPOLs are buck and boost converters. An important aspect of the proposed CubeSat EPS architecture is its versatility. The ability to provide multiple output voltages enables the operation of multiple peripherals and scientific equipment. The EPS consists of four synchronous FDPOL's, two buck and two boost converters. These produce varying rail voltages from 3.3V to 15V. The converters are flexible is the sense that they can be programmed to produce any output voltage within specified parameters. The FDPOLs are powered by the batteries on-board the CubeSat. A buck converter is step down DC-DC converter that decreases or steps down the input DC voltage. The EPS consists of two buck converters that are programmed to output voltages of 3.3V and 5V.

The buck converter used in the EPS is shown in Figure 14**.** Q24 and Q25 are switching devices that, along with inductor L10 and capacitor C86, form a synchronous buck configuration.

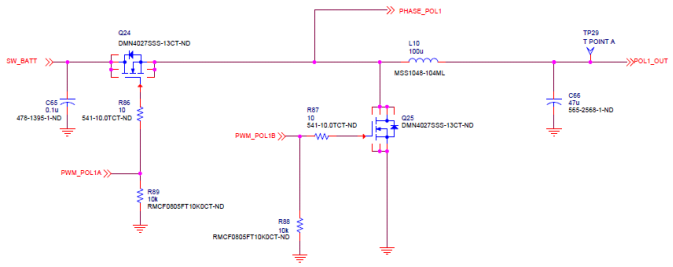

Figure 14. FDPOL - Buck Converter

Figure 15 shows synchronous boost converter. The EPS has two boost converters programmed to produce voltages of 12V and 15V. This is to power the high voltage systems on the satellite.

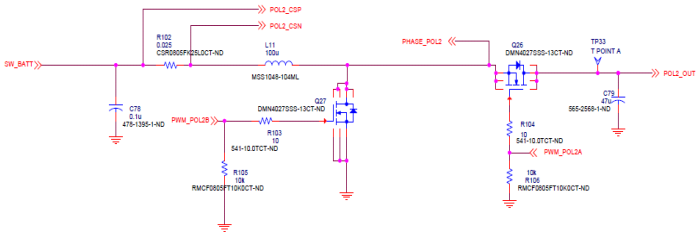

Figure 15. FDPOL Boost Converter

4.3. Driver Circuitry

The converters on the EPS board consist of n-channel MOSFETs. Texas instruments TPS28226 synchronous MOSFET drivers are used to generate the required gate voltage. These

drivers generate complementary gate signals for the high side and low side MOSFETs along with dead band provision. The ICs operate in the voltage range of 6.8V to 8.8V.

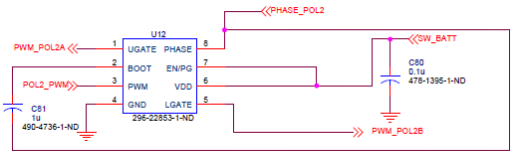

Figure 16. EPS - Driver Circuitry

4.4. Voltage Sensing

The proper operation of the EPS requires that voltages at critical junctions be continuously monitored. The voltages are fed into the ADC of the controller and since these voltages exceed the maximum limit for the ADC, the voltage being monitored is fed to controller via a resistor divider network. Since very high value resistors are used, minimal losses are incurred. These resistors also have a 1% tolerance for accurate measurement.

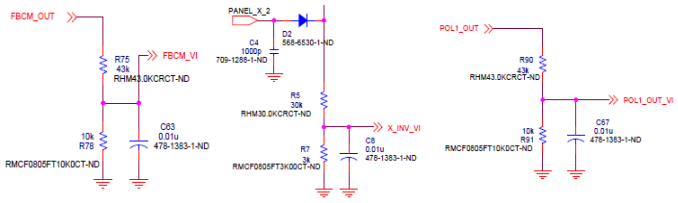

Figure 17. Voltage Sensing Circuitry

Figure 17 shows the voltage sensing circuitry. The left circuit shows the voltage sensing circuitry for sensing the FBCM voltages and similar divider networks are used for sensing the battery voltages and FDPOL output voltages shown on the right. The circuit in the center shows the sensing circuitry for panel voltages that are required for MPPT algorithms.

4.5. Current Sensing

Current sensing becomes an important aspect of EPS design as it plays a major role in battery charging systems which employ CC-CV charging and also measuring the current across the inductor is crucial to implementing closed loop control in power converters. The current is measured by measuring the potential difference across a low loss sense resistor measuring 0.025Ω; the difference is fed into a current sense amplifier shown in the Figure 18 below. Maxim's Max9920 current sense amplifiers are used and they are powered by the 5V supply.

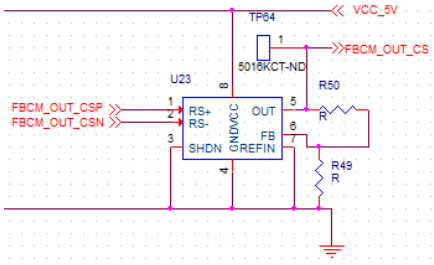

Figure 18. Current Sensing Circuitry

4.6. Controller

A digital controller sits at the heart of the EPS and is responsible for maintaining proper operation of the system. The system uses TI's TMS320F28335 DSP which runs at 150MHz. It has features like hardware floating point unit, 16 12 bit ADC channels which can be configured in several ways, 18 PWM outputs and 6 high resolution PWM channels, UART and JTAG support. The controller generates the PWM signals, triggers the pass transistors and monitors voltage and current for closed loop control. The present design employs TI's Delfino F28335 daughter card. The EPS has a pluggable microcontroller interface and which enables the use of any controller with minimal modifications.

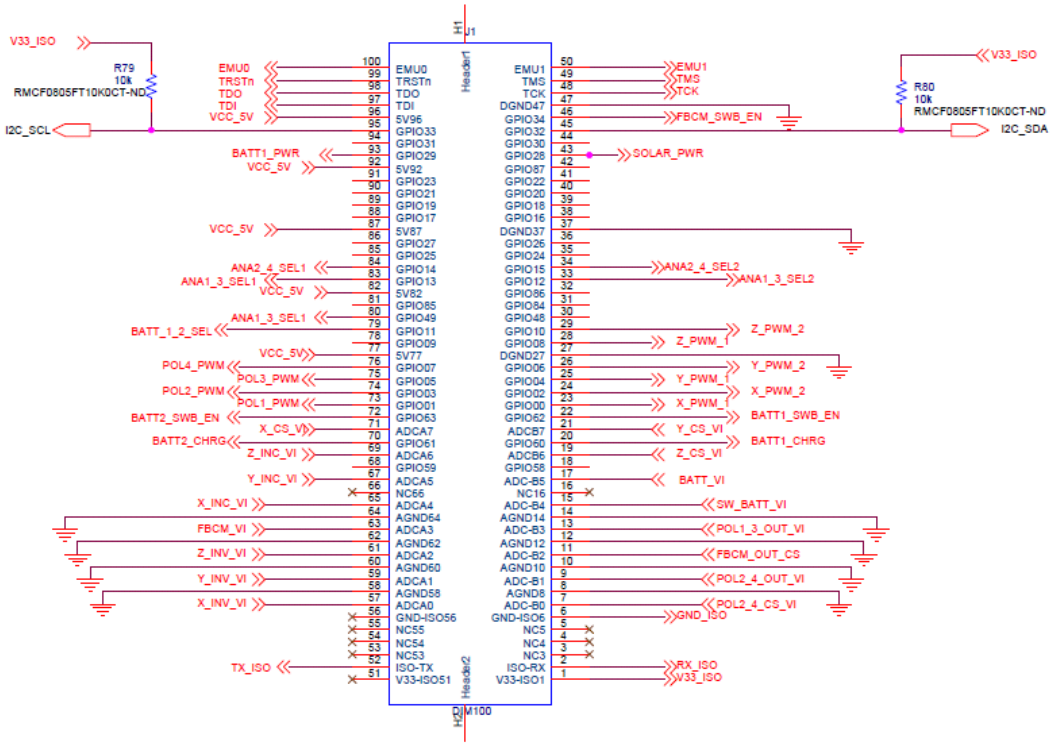

Figure 19. Controller Interface Circuitry

4.7. Path Selection

The EPS consists of an assembly of p-type MOSFETs switches which are responsible for routing the power to various modules on the board. The output of the FBCM – FBCM_OUT can be routed to either battery 1 – BATT1 or battery 2 – BATT2 or it can be directly used to power the FDPOLs. The input voltage bus of the FDPOL is the SW_BATT. The other pass transistors are used to route the power from either of the batteries to the SW_BATT. When one battery charges, the other is used to power the input bus. The inputs of the pass transistor have a diode to prevent the reverse flow of current. The gates of the pass transistors are connected to the drain of npn transistors which are operated by the contol signals generated by the onboard controller. This is done to invert the trigger logic and to turn off the pass transistor using the input voltage which ensures that the p-type MOSFETs are turned off.

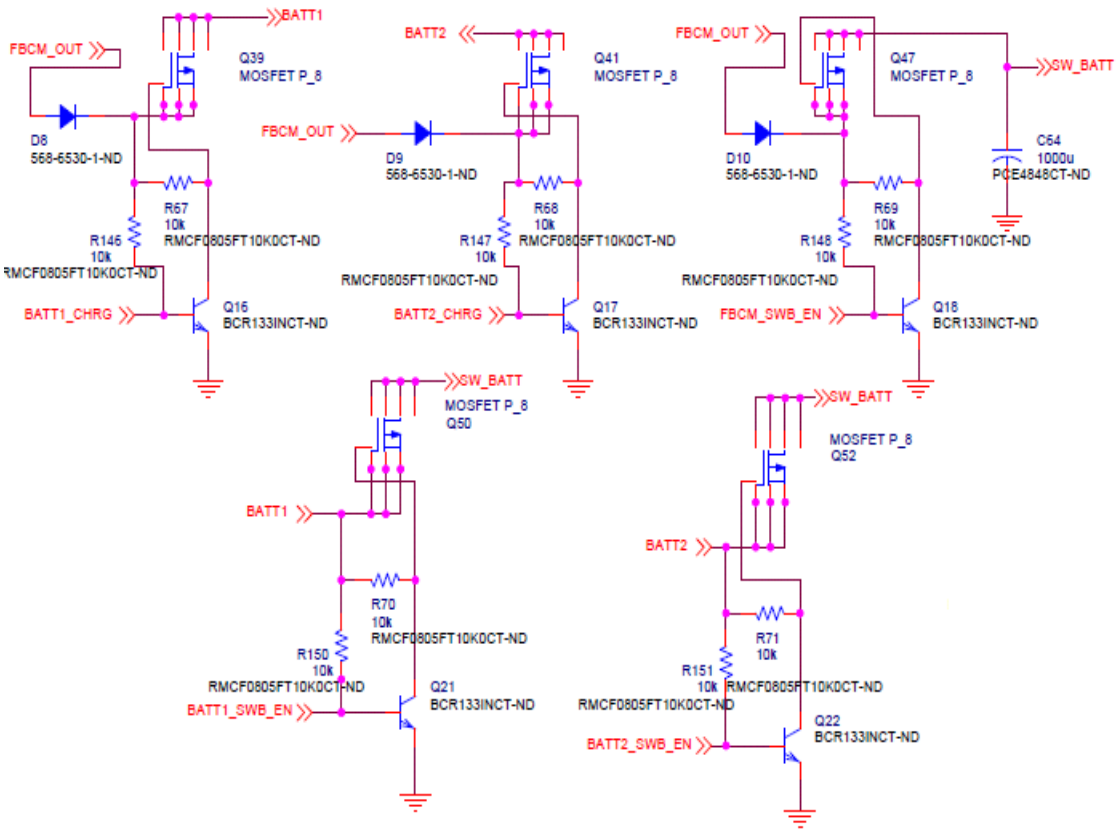

Figure 20. Path Selection Circuitry

4.8. Power Supply

The EPS board has two power buses of 7V and 5V. The MOSFET drivers in the switches require a 7V supply while the control and the current sensor ICs need 5V. Since the EPS is supplied by batteries that are 7.2V, a low drop-out linear regulator is used to step down the voltage to 5V. Figure 21 shows the circuit for the power supply connections. The linear regulator can be supplied by either of the batteries which can be selected by a pass transistor. The board has a provision for a separate 5V supply which can be connected through an onboard connector.

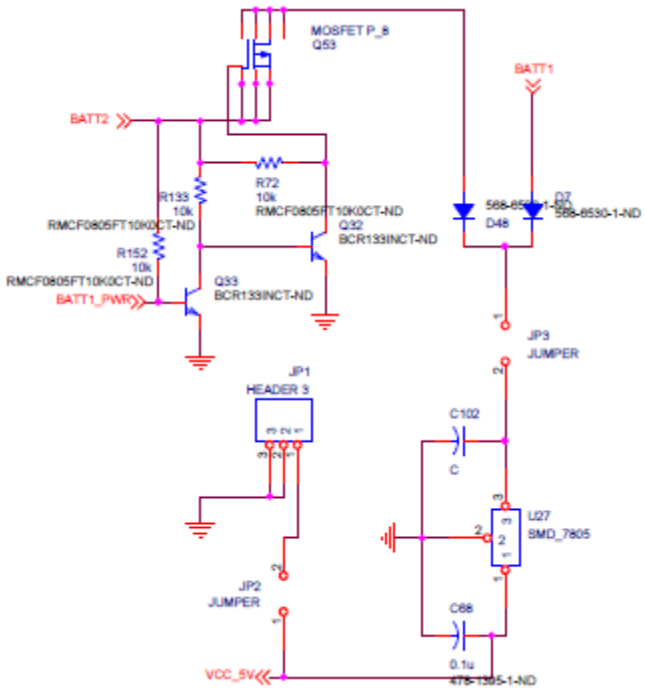

Figure 21. Power Supply Circuit

CHAPTER 5
Controller Design

The previous chapter dealt with the hardware design of the system emphasizing on the circuit construction, the choice of components, etc. A critical component of such power management systems is the controller scheme. Digital control based power systems have seen a gigantic growth in the last decade. Analog control brought with itself benefits such as ease of implementation, high bandwidth and cost effectiveness. As silicon technology improved and the cost of processors decreased, it ushered an era of low cost, high bandwidth digital signal processors [17]. A significant factor in the migration to digital control was the need to make power converter systems smart, configurable and the need for better integration with embedded systems which was not possible with traditional analog controllers. The electrical power system for a device such as a CubeSat should exhibit all of the aforementioned features like intelligence, plug and play capability and integration to a wide range of peripherals. This becomes extremely difficult to accomplish using analog control techniques.

5.1 Digital Control for DC-DC converters

The previous paragraph highlighted the advantages of digital control over analog control for CubeSats. This section will describe the digital control model fundamentals and how it would be extended to converter topologies being used in the EPS. While digital control offers a lot of benefits, it has its own set of challenges that need to be considered while designing such controllers [17]. There are two main approaches for designing digital systems – digital redesign and direct digital design. In the former method, a well-tested and well-known analog compensator is converted to a digital implementation. The latter deals with developing a discrete time model of the system and then a digital compensator is designed using conventional control design techniques. Direct digital design has advantages when it comes to achieving better phase margins and bandwidths [18].

The discrete time model of the plant is obtained by developing a continuous time model and then converting it into a sampled system using well known transformation techniques. Figure 22 below shows the closed loop control block diagram for voltage mode control of a generic DC-DC converter. The control loop diagram is divided into three sections – the controller, the plant and the power stage.

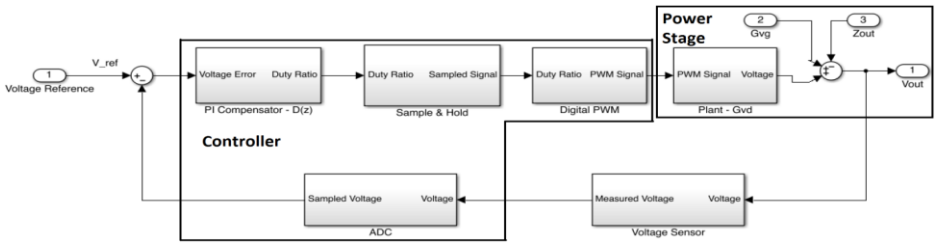

Figure 22. Closed Loop Control Block Diagram

5.1.1. Controller Section

The controller is responsible for sensing the output voltage at regular interval specified by the sampling frequency and then comparing it with the voltage reference Vref. The difference e[n] is then fed to the compensator D(z) represented by a difference equation [19]. The output of the compensator is given to the DPWM – dynamic PWM module which determines the duty ratio of the switching transistors that regulate the output voltage. The zero order hold represents the fact that the duty cycle is updated in discrete intervals. As mentioned before, the controller samples the output voltage and converts it into a 12 bit number represented by K_{adc} [20] while K_{pwm} is the value representing the duty ratio. Equation 1 represents the value of K_{adc} and K_{pwm}. $Vmax_{adc}$ is the maximum output voltage that the ADC can generate.

$$K_{pwm} = \frac{1}{2^{n_{pwm}}-1} \text{ and } K_{adc} = \frac{1-2^{-n_{adc}}}{V_{max_{adc}}} \quad (1)$$

The transfer functions of the ADC and the PWM modules are represented by equations 2 and 3.

$$G_{pwm}(s) = K_{pwm} * e^{-sT_{pwm}} \quad (2)$$

$$G_{adc}(s) = K_{adc} * e^{-sT_{adc}} \quad (3)$$

The exponential terms in the transfer function represents the ADC conversion delay and the DPWM delay.

5.1.2. Plant

A plant is defined as the system being controlled and is represented by a transfer function. In this system, the DC-DC converter represents the plant. A mathematical model of the converter that models all the dominant system characteristics needs to be derived [21]. Since the objective is to maintain a constant input voltage, a model is developed to depict the effects of variations in the duty cycle on the output voltage. The ac modeling approach involves removing the switching harmonics by averaging the inductor current and capacitor voltage waveforms over a switching cycle and then linearizing the system at a particular operating point. A small signal model is developed which assumes that the ac variations are negligible compared to the DC operating points or the quiescent values. $G_{vd}(s)$ represents the small signal duty cycle to output voltage transfer function. The plant comprises of G_{vd} along with a zero order hold. Equations 4 and 5 represent the plant transfer function in the s and z domains respectively.

$$G(s) = \left(\frac{1-e^{-sT}}{s}\right)_{ZOH} * Gvd(s) \quad (4)$$

$$G(z) = \frac{z-1}{z} Z^{T}\left\{\frac{Gvd(s)}{s}\right\} \quad (5)$$

5.1.3. Power Stage

The power stage represents the DC-DC converter dynamics. This incorporates everything that relates to converter parameters like input voltage, impedances and load that affect the converter operation. G_{vg} is the small signal input voltage to output voltage transfer function while Z_{out} is the output impedance as seen by the converter. These parameters are modeled as disturbances to the system and compensator should be able to maintain constant output voltage with variations in the input voltage and the load. The following sections will discuss the compensator design of the FBCM and FDPOL modules.

5.1.4 Compensator Modeling in Software

The manner in which a digital compensator is implemented in software is important. A generic first order compensator transfer function is represented by equation 6.

$$D(z) = \frac{a_2 + a_1 z^{-1}}{1 + b_1 z^{-1}} = \frac{d(z)}{E(z)} \quad (6)$$

All compensators in this project are proportional-integral or PI compensator. The given equation is converted to a discrete time difference equation of the form given in equation 7.

$$d[n] = a_2 e[n] + a_1 e[n-1] - b_1 d[n-1] \quad (7)$$

The term d[n] represents the new duty cycle while d[n-1] represents the duty cycle in the previous time step. Similarly, e[n] is the present error and e[n-1] is the error in the previous time step. The PI gains are represented by a_1 and a_2 and the compensator is designed using MATLAB's Control Systems Toolbox [22].

5.2. FDPOL Compensator Design

5.2.1. Buck Converter

The two synchronous buck converters are designed to output a voltage of 3.3V and 5V. Equation 8 represents the transfer function of the synchronous buck converter. G_{vd} is the small signal duty cycle to output voltage transfer function [23].

$$G_{vd}(s) = \frac{(V_g.R_o/(R_o+r_L))(1+sr_CC)}{1+\left[C\left(r_C+\frac{R_o.r_L}{R_o+r_L}\right)+\frac{L}{R_o+r_L}\right]s+[LC(R_o+r_C)/(R_o+r_L)]s^2} \quad (8)$$

Table 1 lists the buck converter specifications on which the small signal model is built. The converter supplies a resistive load of 330 mA for 3.3 V output and 0.5 mA for 5 V output.

Table 1. FDPOL Buck Converter Parameters

Parameter	Symbol	Value
Input Voltage	V_g	7 V - 8.4 V
Output Voltage	V	3.3 V/5V
Output Capacitor	C	47 µF
Capacitor ESR	r_C	200 mΩ
Inductor	L	100 µH
Inductor DCR	r_L	0.253 Ω
Resistance	R_o	10 Ω
Switching Frequency	fs	150 KHz
Sampling frequency	f_T	10kHz

The compensator was designed by converting the analog transfer function into discrete time transfer function using zero order hold and a sampling period of 100 µs.

A PI compensator was designed and the compensated system has a bandwidth of 4000 rad/sec. Figure 23 shows the margin plots of the analog system, digital system and the compensated system. Table 2 below compares the gain and phase margins of the uncompensated and compensated system.

Table 2. Gain and Phase margins of FDPOL Buck Model

System	Phase Margin (degree)	Gain Margin (dB)
Analog Uncompensated	31.6	Inf
Digital Uncompensated	Inf	-2.92
Digital Compensated	72.7	5.52

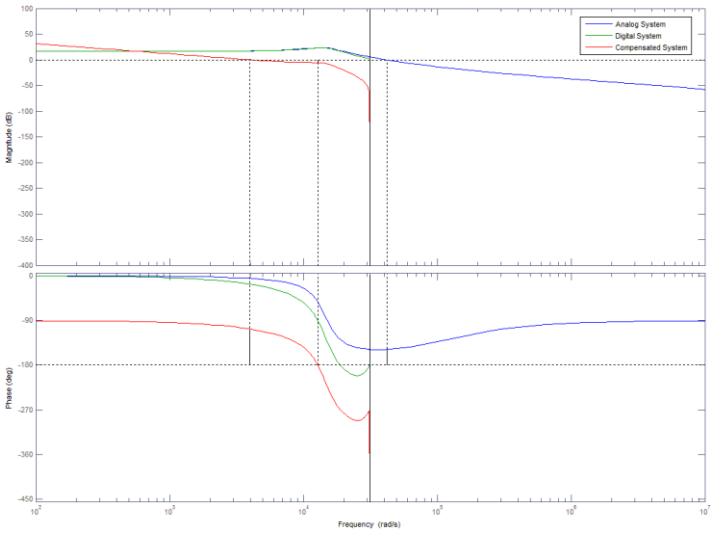

Figure 23. Margin plots of the buck converter models

The step responses of the buck converter are analyzed for various configurations. The yellow traces represent the output voltage of the converter while the blue traces represent the voltage across the load. Figure 24 is the open loop step response of the system; it is seen that the output voltage settles at a lower value and there is steady state error.

The traces in Figure 25 depict the step responses for a set output voltage of 3.3V and 5V respectively and an input voltage of 7V. As is evident from the step responses, the PI compensator removes the steady state error without significantly affecting the response times. The converter is supplying a step load of 10Ω in each of these figures.

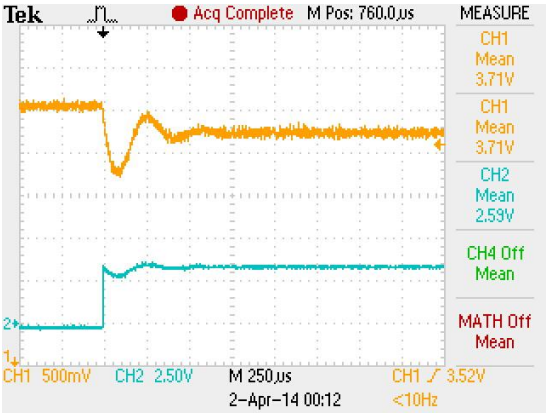

Figure 24. Open Loop Response - Buck Converter

Figure 25(a) is the step response for a 10Ω load and 3.3V output voltage which makes it a step change in current from 0A to 330mA. Figure 25(b) is a 5V converter and is a step change from 0A to 200mA.

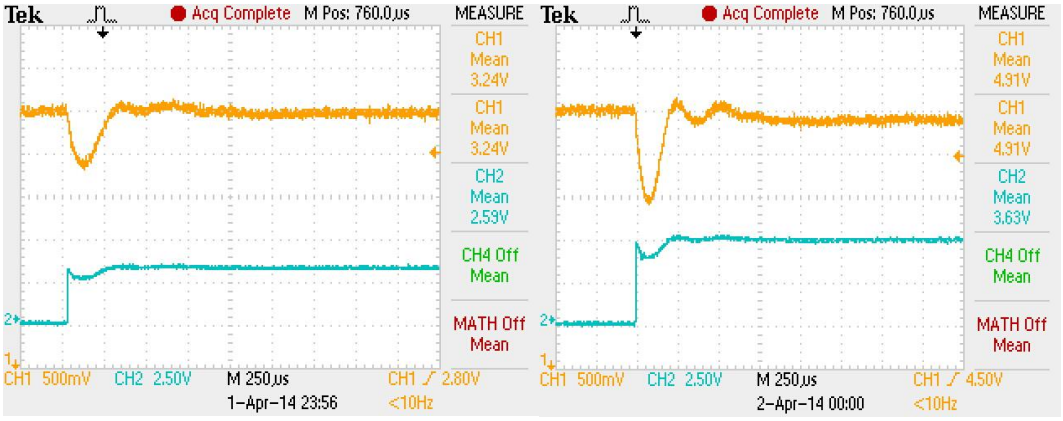

Figure 25. Closed Loop Response - Buck Converter (a) 3.3 Volts (b) 5 Volts

5.2.3. Boost Converter

The boost converters are designed to output a voltage of 10V and 12V. A boost converter operating in continuous conduction mode is more difficult to control due to the presence of a right hand plane (RHP)-zero which destabilizes the system. Also, the boost converter transfer function depends on both the input voltage and output voltage apart from the capacitance, inductance and load which further complicates the system [24]. This led to reluctance in the use of voltage mode control for boost converters and current mode control techniques are employed which simplify control of the system. The advent of very fast and cost effective processors for digital control applications have enabled the use of voltage mode control which is computationally less expensive and provides satisfactory transient responses. The small signal duty cycle to output voltage transfer function is given by equation 9**.**

$$G_{vd}(s) = \frac{(R_o + r_C)(sCr_C+1)\left[-(sL+ r_L)(R_o+r_C)+D'^2 R_o^2\right]}{P(s)[D' R_o(D' R_o + r_C)+ r_L(R_o+r_C)]}.R_o V_g \qquad (9)$$

$$P(s) = s^2LC(R_o + r_C)^2 + s[L(R_o + r_C) + r_LC(R_o + r_C)^2 + D'R_o r_C C(R_o + r_C)] + (R_o + r_C) + D' R_o(D' R_o + r_C) \qquad (10)$$

Table 3. FDPOL Boost Converter Parameters

Parameter	Symbol	Value
Input Voltage	V_g	7 V - 8.4 V
Output Voltage	V	10 V/12 V
Output Capacitor	C	47 µF
Capacitor ESR	r_C	200 mΩ
Inductor	L	100 µH
Inductor DCR	r_L	0.253 Ω
Resistance	R_o	20 Ω
Switching Frequency	fs	150 KHz
Sampling Frequency	f_T	10KHz

The boost compensator design procedure is similar to that of the buck converter. The analog plant is transformed into a digital plant and a PI compensator is designed to ensure system stability with satisfactory response times. The margins of the analog, digital and the compensated systems are compared in the margin plot shown in Figure 26. It is evident from the plots, a bandwidth of 3000 rad/sec is achieved. The gain and phase margins are compared in Table 4.

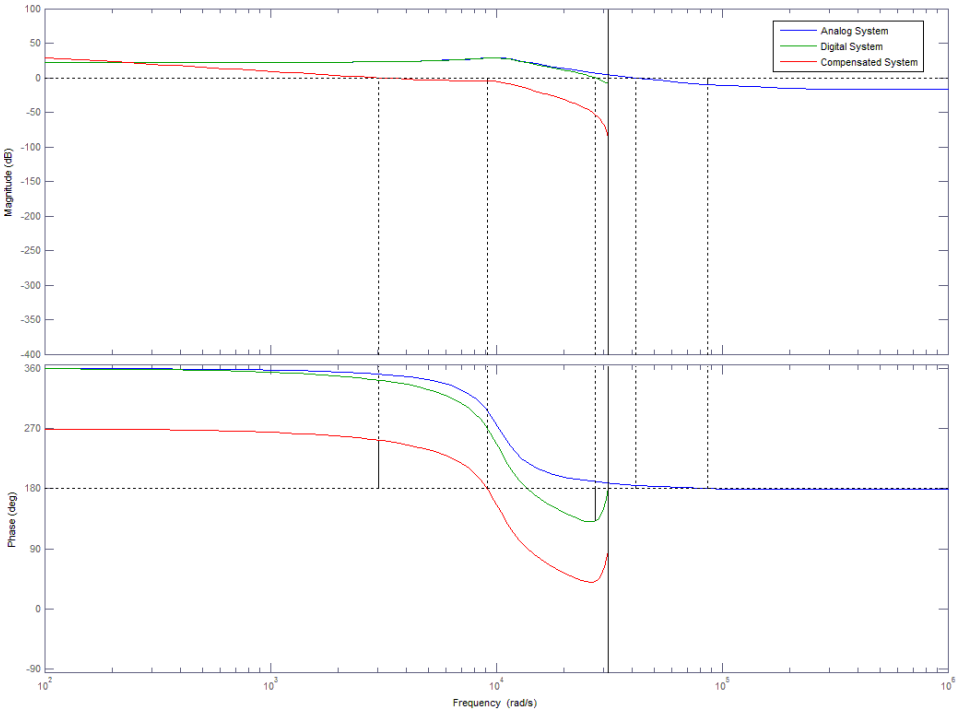

Figure 26. Margin Plots of the boost converter models

Table 4. Gain and Phase Margins of FDPOL Boost Model

System	Phase Margin (degree)	Gain Margin (dB)
Analog Uncompensated	4.91	9.7
Digital Uncompensated	-48.5	7.18
Digital Compensated	72.3	4.64

Figure 27 is the open loop step response of the boost converter supplying a 20Ω load. A significant steady state error is evident. The yellow trace represents the output voltage while the blue trace is the voltage across the load.

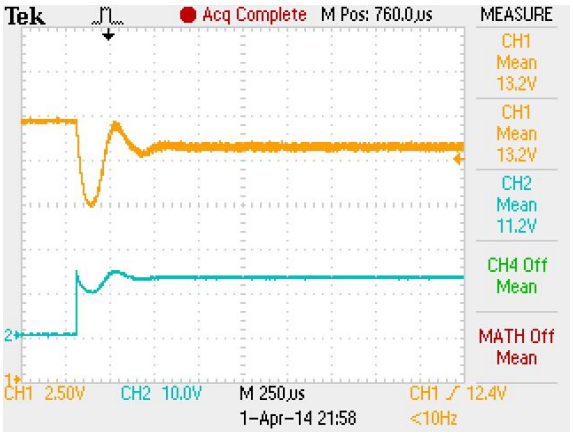

Figure 27. Open Loop Response - Boost Converter

Figure 28(a) is the step response of a boost converter with a 10V output and a load of 500mA making it a 5W system. The step response of Figure 28(b) is that of a 12V boost converter supplying a 600mA load. This makes it a 7.2W system. The PI compensator ensures zero steady state error.

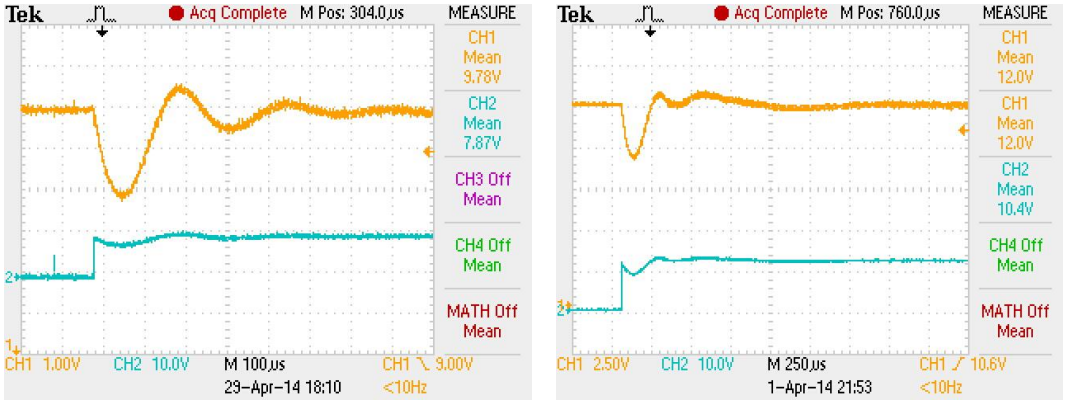

Figure 28. Closed Loop Response - Boost Converter (a) 10 Volts (b) 12 Volts

The FDPOLs are operated in parallel and can be regulated simultaneously. Figure 29 shows the two buck FDPOLs being regulated at 3.3V and 5V and a boost FDPOL regulated at 12V. The input voltage being 7V. The green trace is the input, the blue and purple traces show the outputs of the buck converters and the yellow trace is that of the boost output.

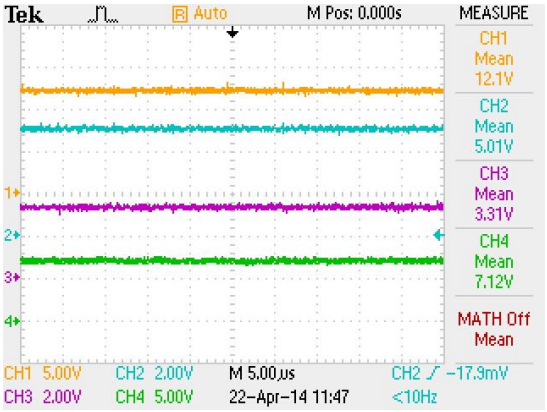

Figure 29: FDPOL - Parallel Operation

5.3. FBCM Compensator Design

The purpose of a flexible battery charging module, as discussed before, is to provide an interface between the solar panel and the battery. The compensator design procedure for an FBCM is different from that of an FDPOL as the FBCMs modules act as a photovoltaic battery charging system. The small signal models of buck and boost converters developed for FDPOLs can be extended for FBCM regulation. The batteries are charged using constant current - constant voltage (CC-CV) technique. To accomplish this, a dual loop control scheme is employed.

Constant Voltage Mode – The methodology for constant voltage remains same as that of the FDPOL. Figure 30(a) shows the step response of a boost converter powering a battery load in constant voltage mode.

The blue trace is that of the battery voltage while the yellow trace represents the converter output voltage. Figure 30(b) shows the plot of the battery voltage and the output current in constant voltage mode. A volt in the current trace corresponds to 0.63A current. The input voltage is 5V and the output is 8V.

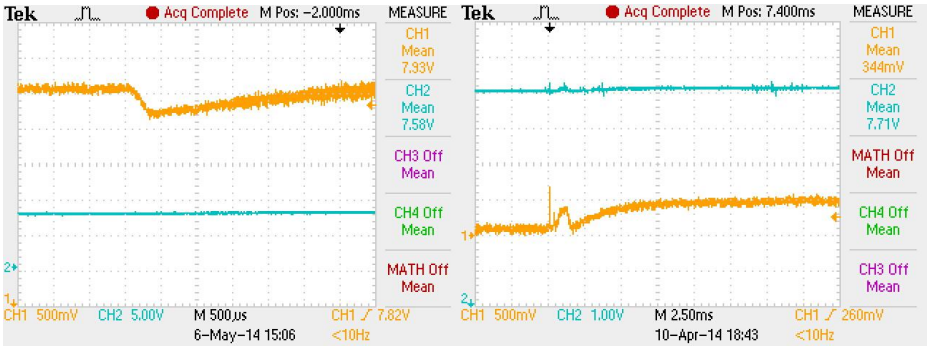

Figure 30. FBCM Boost Constant Voltage Mode (a) Converter Output Voltage (b) Converter Output Current

Figure 31 show the FBCM in the buck mode. The plot on the left shows the battery and the converter output voltages. As in the previous case, the blue trace is the battery voltage while the yellow trace is the converter output voltage. The plot on the right is that of battery voltage and output current. The blue and yellow traces represent battery voltage and output current respectively. The input is 12V while the output is 8V.

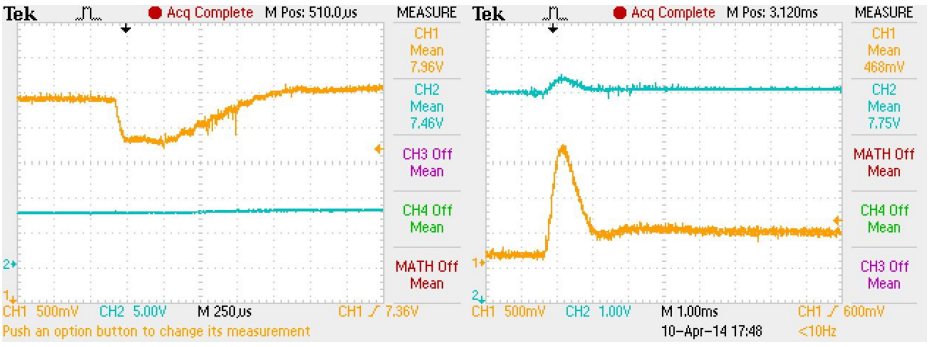

Figure 31. FBCM Buck Constant Voltage Mode (a) Converter Output Voltage (b) Converter Output Current

Constant Current Mode – Charging the battery with constant current poses challenge for buck and boost converter topologies as the control loop runs in voltage mode control. The regulation of output current requires sensing it, which in turn requires a high bandwidth current sensor. This is difficult to accomplish for digital systems employing a low sampling rate. Hence, a tradeoff is established which regulates current within acceptable range. Some implementations have used inductor current control for regulating output current [25] while others control algorithms are based on battery current control [26]. However, a direct control scheme for the output current was found to perform better for the CubeSat application.

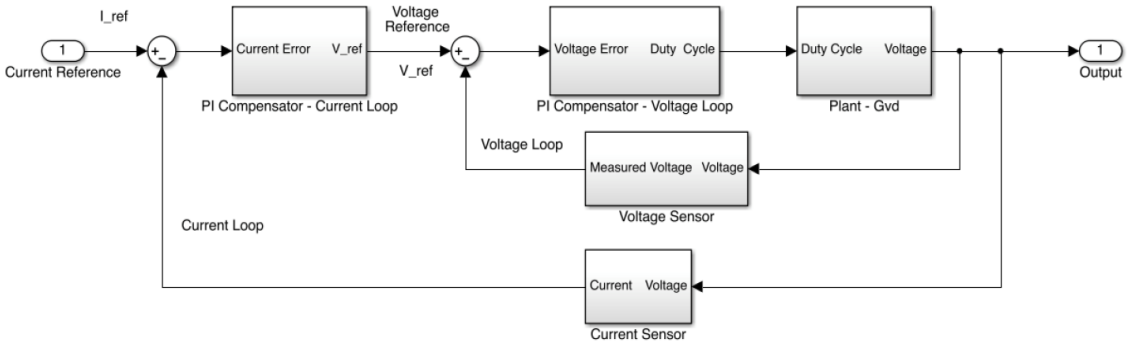

Figure 32. FBCM Constant Current Mode Control Loop Block Diagram

Figure 32 shows the control loop diagram of FBCM running in constant current mode. This scheme employs two control loops –outer current loop and inner voltage loop. The voltage loop is similar to the voltage control loop employed in constant voltage control. The outer current loop measures the output current and compares it to the desired current reference. The error term is fed to a PI compensator which generates the voltage reference. The voltage loop runs around 10 times faster than the current loop. Figure 33(a) shows the FBCM boost converter running in constant current mode and Figure 33(b) shows the FBCM buck converter running in constant current mode. The blue traces depict the battery voltage while the yellow traces show the current. The current reference is set at 0.45A. The yellow trace shows the current while the blue trace shows the terminal voltage.

The current measurement scale is 1V to 0.63A. It is evident from the traces below that the current is regulated at 0.45A with negligible ripples.

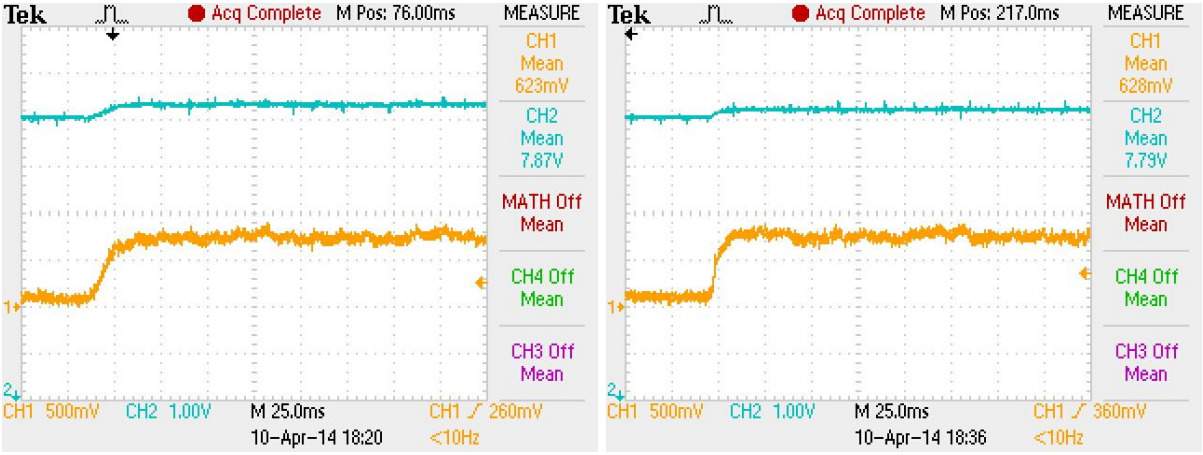

Figure 33. FBCM Constant Current Operation (a) Boost Mode (b) Buck Mode

5.4. Maximum Power Point Tracking

The FBCM modules derive their power from solar panels. The output from the solar panel depends of a variety of factors such as light intensity, ambient temperature changes, load changes and partial shading conditions. The operating point of the solar panel changes with changes in these conditions and maximum power output is not always guaranteed and a lot of available power is wasted. As a result a technique which ensures that the panel operates at or closer to its maximum power point becomes essential for battery charging systems because the panel always has to provide more power than what the battery can absorb.

Figure 34 shows the voltage-current and voltage-power characteristics of a generic solar panel. As is seen from the curves, the maximum power point is different for different levels of radiation.

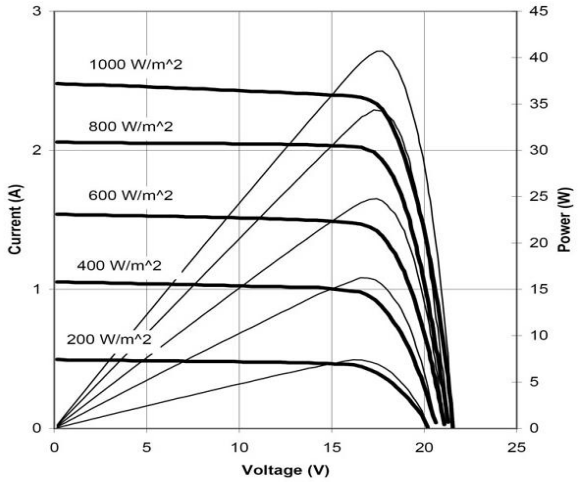

Figure 34. Typical Solar Panel Characteristics

The basic idea behind maximum power point tracking algorithms is that of impedance matching. A DC/DC converter represents variable impedance that changes with the duty ratio of the converter. The algorithm continuously tracks the maximum power point and steers the panel's voltage to that particular operating point [27]. There are several MPPT algorithms which usually trade-off between the implementation complexity and performance. Two of the most prevalent ones are discussed in brief.

Perturb and Observe P&O – This is the most commonly used algorithm because of its inherent simplicity and cost of implementation. The solar panel voltage is perturbed by a fixed or variable amount [27] by modifying the duty cycle of the converter. The voltage and the current from the solar panel are measured and the power is calculated. This power is compared to the power measured before the perturbation; it there is an increase in power, the direction of the next perturbation remains the same and it is reversed if the power has decreased. Once the maximum power point - MPP is reached, the system oscillates around this value.

Incremental Conductance – The basis of the incremental conductance algorithm is the fact that the slope of the power vs. voltage curve will be zero at the maximum power point - MPP. At each iteration, the incremental conductance ($\Delta I/\Delta V$) is compared to the instantaneous conductance. Based on the result, the panel voltage is increased or decreased until the MPP is reached. There is no oscillation around the MPP like the P&O algorithm.

The present implementation uses the P&O algorithm because of its simplicity and satisfactory performance for low to medium power systems. The flow diagram of the algorithm is given in Figure 35. On the right portion of the flow chart, increasing panel voltage will increase power and on the left portion, decreasing panel voltage will decrease power.

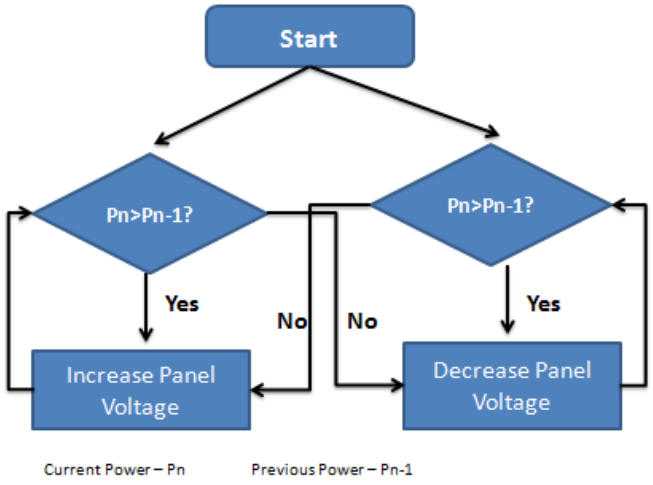

Figure 35. Perturb and Observe (P&O) MPPT Control Flow Diagram

The solar panels used are 5.2W mono-crystalline type with 9.55V open circuit voltage and 550mA short circuit current. Since, each FBCM interfaces with a pair of these panels, the characteristic curves were plotted for two units connected in parallel. Figure 36 shows these solar panel characteristics.

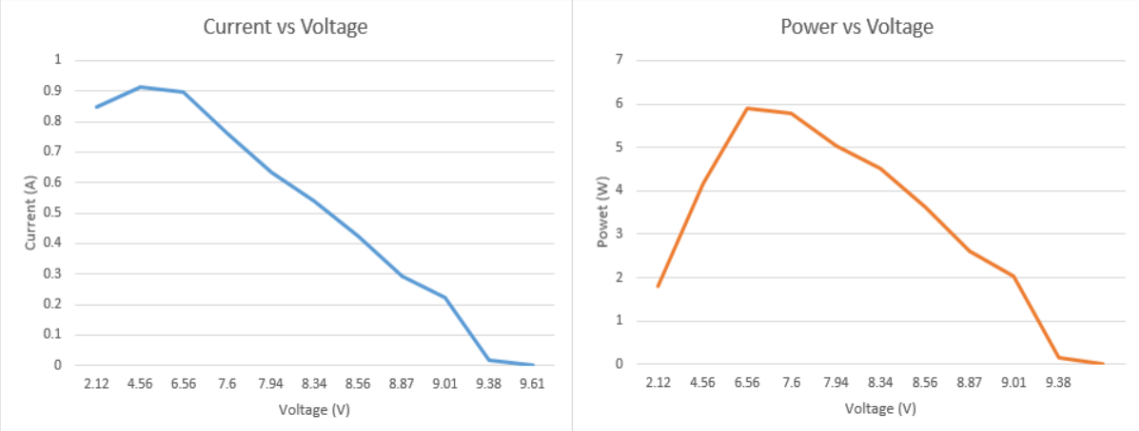

Figure 36. Solar Panel Characteristics

A PI compensator was implemented to regulate the panel's voltage. Figure 37 shows the P&O MPPT control response. The blue trace is the solar panel voltage, the yellow trace is the panel current and the red trace shows the instantaneous power. As seen in the trace, the operating point settles near the peak power rating of the panel. The plot on the right is the zoomed in view of the response. A volt on the trace representing current corresponds to 0.63A. As is seen in the figure below, around 4.5W are extracted from the panels.

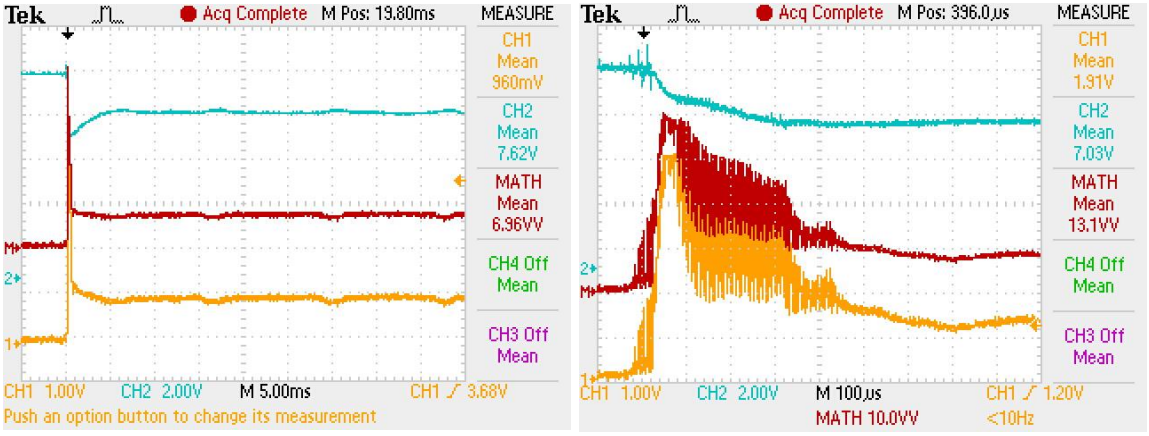

Figure 37. P&O MPPT Operation

5.5. Path Selection

The path selection feature of the EPS provides enhanced configurability and scalability. The power from the solar panels can be routed to either of the battery banks. The FDPOLs can be powered using either of the battery banks depending on the state of charge. The path switching feature ensures that the FDPOLs get necessary input power and remain in operation. Assuming that initially battery 1 is powering the FDPOLs and battery 2 is on standby; if battery 1gets discharged, battery 2 is connected to the FDPOL input while battery 1 is connected to the FBCM output for charging. The traces in Figure 38 demonstrates the path selection feature and it also shows the effect of changing FDPOL input on the FDPOL output voltage. The yellow trace shows the output of FDPOL buck converter operating at 3.3V. The purple and green traces show voltages of battery 1 and 2 respectively. The blue trace shows the FDPOL input. Initially, battery 1 is connected to input of FDPOL. When the voltage of battery 1 starts to decrease, the FDPOL input voltage decreases along with it (the blue trace follows the purple trace). If the voltage goes below a certain threshold, the path is switched and battery 2 is connected to the FDPOL input (the blue trace now follows the green trace).

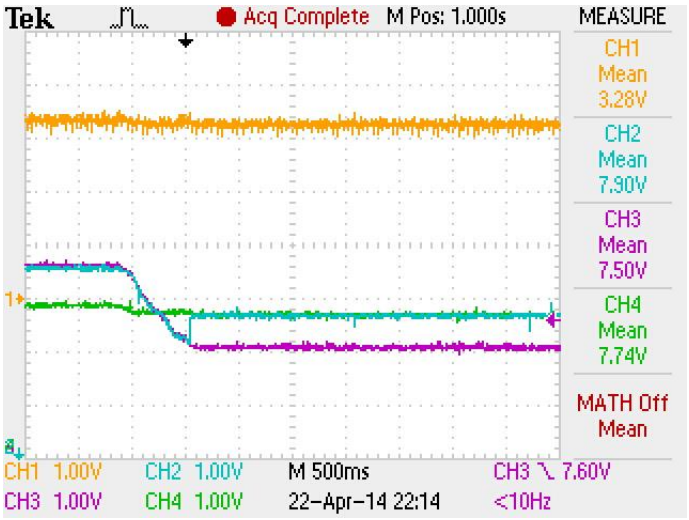

Figure 38. Path Selection Feature

CHAPTER 6
Software Design

The software architecture becomes significant for systems like EPS which are scalable, programmable and intelligent. A system that runs simultaneous control loops needs a well-planned software layout so that all the critical functions are completed before the next sampling interval arrives. Issues like control loop update rate, sampling frequency and ADC conversion time need to be considered while laying out the software for the system. This chapter discusses the features of the software design of the system. This includes the main control loop implementation, the photovoltaic battery charging scheme and the digital compensator code implementation. The code is profiled and the time spent on different modules is calculated and the results are discussed.

6.1 Central Control Loop

The EPS code has a main control loop that runs the compensator, the path switching circuitry and the battery charging code. Figure 39 shows the control flow diagram of the central control loop. The control loop update rate is 100µs which means that the duty cycle is updated every 100µs. A timer triggers the execution of the central control loop. The voltages and current are sensed synchronously every fourth duty period and all the samples before the next update period are averaged to remove sensing aberrations. The central control loop carries out three functions viz. Path Selection, FDPOL Control and FBCM Control.

Path Selection – The EPS consists of pass transistors which act as an assembly of switches that route power from different power sources to the FDPOL input rail. The switching paths can be configured to have the following paths of power flow.

- Battery 1 powers the FDPOLs
- Battery 2 powers the FDPOLs
- FBCM's output is connected to battery 1

- FBCM's output is connected to battery 2
- FBCM directly powers the FDPOL's

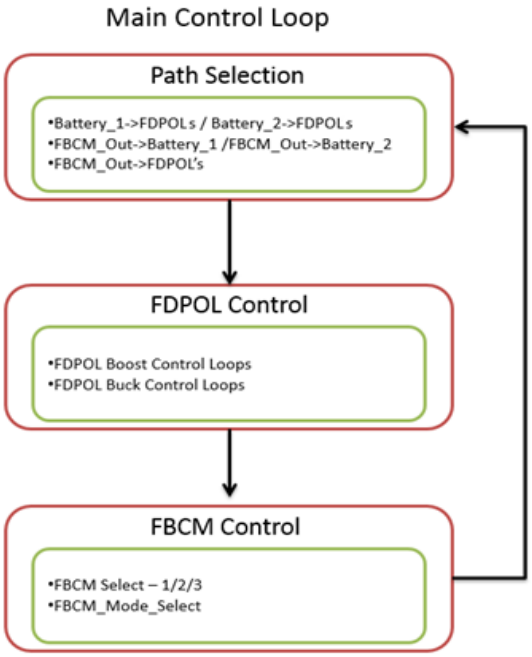

Figure 39. Main Control Loop

FDPOL Control – The closed loop control of the point of load converters is run as a part of the central control loop. These converters can be enabled or disabled depending on the application.

FBCM Control – There are three FBCM modules in the EPS board. The FBCM that runs is determined by the orientation of the satellite and the panel that receives maximum solar radiation. Also, the FBCM can run in either battery charging modes or MPPT mode depending on the solar power level at the input. Furthermore, in the battery charging mode a FBCM can run in either CC or CV mode depending on the battery charge level.

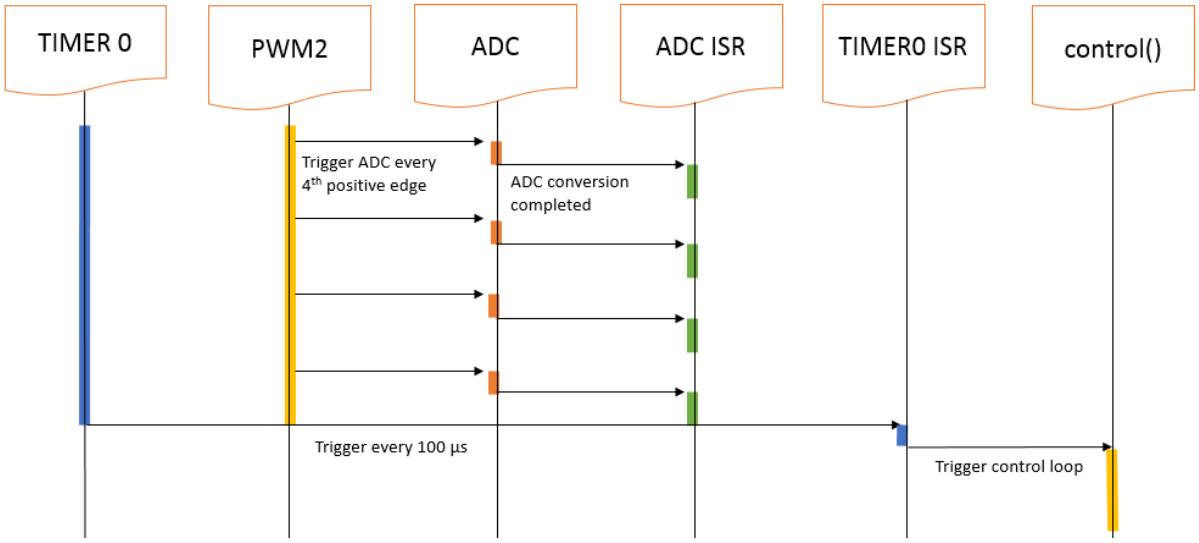

Figure 40. Sequence Diagram for the EPS software

Figure 40 shows the sequence diagram for the software scheme. The PWM channel triggers ADC start of conversion every 4th positive edge. The voltage and current are recorded and averaged four times every duty cycle. The duty cycle is updates every 100µs by means of timer zero whose ISR triggers the control loop which is responsible for FBCM and FDPOL control.

6.2. FBCM Control

The control of FBCM modules need special consideration and provisions because it provides an interface between solar panels and the battery. Instead of just the conventional voltage mode control, it also operated in constant current mode for the purposes of charging the battery. Apart from the output voltage or current control, the input voltage is also altered for the purposes of tracking the maximum power point (MPP). Additional complexity arises from the fact that the control loop can either regulate output or input voltage and hence the control needs to switch between the MPPT and output voltage/current regulation depending upon the solar power level [28]. The Figure 41 below shows the FBCM control mechanism.

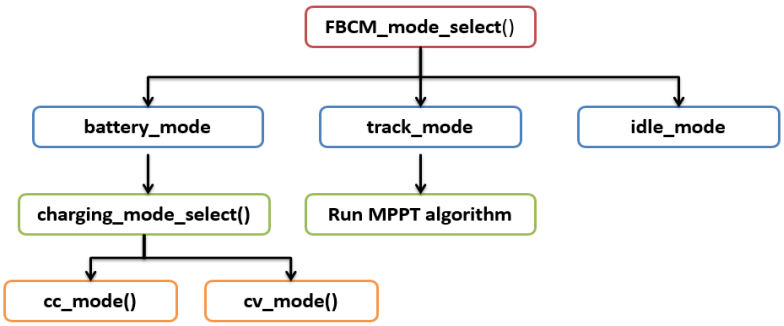

Figure 41. FBCM mode select function

The function FBCM_mode_select determines the mode in which the FBCM runs. The FBCM can either run in battery mode, track mode or be in idle mode. In battery mode, the FBCM is carrying out CC/CV charging; in track mode, the FBCM runs maximum power point tracking algorithms and the output is unregulated. If the batteries are charged or that particular FBCM is disabled, it is in idle mode. When in battery mode, the FBCM can either regulate the output current or the output voltage. This is determined by the charging_mode_select function. Figure 42 describes the state machine diagram for the FBCM_mode_select functionality. The FBCM module can exist in three states as explained in the previous paragraph. The state diagram describes the conditions which result in transition from one state to another. Certain battery parameters are represented as constants in the code. MIN_VOLTAGE is the minimum allowable battery voltage for safe operation; however, it is usually kept above the minimum voltage to allow a safe margin of operation. SET_VOLTAGE is the maximum voltage to which the battery is charged while SET_CURRENT represents the minimum current below which the battery charging is terminated. The CC/CV charging starts with battery being charged in CC mode. Once the battery voltage reaches the SET_VOLTAGE, the mode changes to CV mode and the output voltage is held at SET_VOLTAGE until the current being absorbed by the battery drops below a certain limit represented by SET_CURRENT [29]. These two parameters depend on the battery chemistry and the capacity. The present implementation uses a 7.2V, 2.2Ah Li-Ion battery pack for which the aforementioned constants are listed out in the table below.

Table 5. Battery Parameters

Parameter	Value
MIN_VOLTAGE	6.5 V
SET_VOLTAGE	8.4 V
SET_CURRENT	50 mA

The MPPT algorithm ensures that the solar panels operate at or near the peak efficiency. However, while charging the battery, it might happen that the panels' power decreases and the MPPT algorithm needs to run again. There are many ways to determine when the solar panel is unable to supply adequate power to the load. The most straightforward way is to keep track of the duty cycle attained after the MPPT algorithm completes, this is stored in MPPT_DUTY_RATIO. During the course of charging the battery, if the duty ratio increases beyond the MPPT_DUTY_RATIO, this indicates that the solar panel is not able to supply the required power and the mode changes to track_mode. It switches back to battery_mode once the MPPT ensures that the solar panel is able to provide the necessary power.

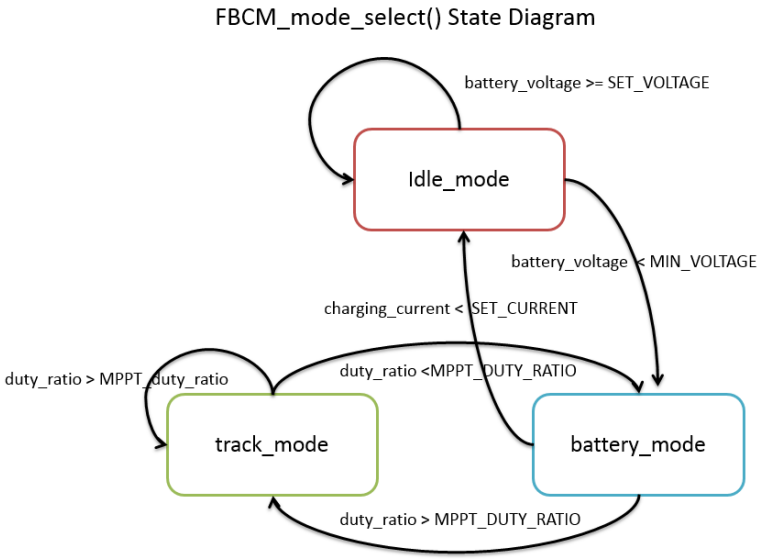

Figure 42. FBCM Mode Select State Diagram

Table 6. FBCM Mode Select State Transition table

Initial State	Next State	Conditions
idle_mode	idle_mode	The battery is charged and is above or equal to the SET_VOLTAGE
idle_mode	battery_mode	The battery voltage drops below the MIN_VOLTAGE and the battery needs charging, so the state changes to battery_mode
battery_mode	idle_mode	The charging current drops below SET_CURRENT and the charging is complete; the state changes to idle
battery_mode	track_mode	The panels can't supply the desired power and needs to run the MPPT code
track_mode	battery_mode	The panels can supply the desired power and can revert to the battery charging mode
track_mode	track_mode	The MPPT code is still and trying to reach the required power level

Table 6 lists out the state transitions and the conditions which cause them. Once the FBCM state machine enters the battery mode, the charging mode is determined by the state transition diagram shown in Figure 43. The transitions and the conditions are explained in Table 7.

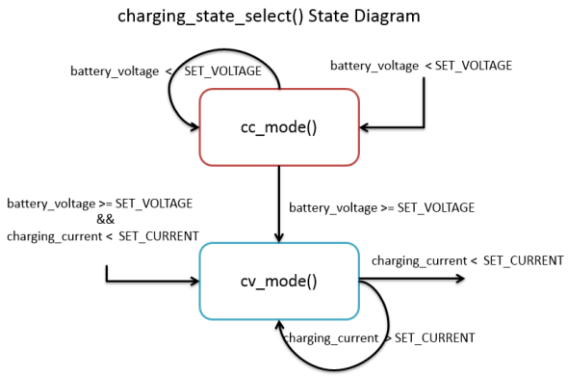

Figure 43. Charging State Diagram

Table 7. Charging Mode Select State Transition table

Initial State	Next State	Conditions
none	cc_mode	The cc_mode can be entered either from the idle state when the battery just starts to charge or else from MPPT mode if required power during course of charging is not available
cc_mode	cc_mode	The battery is charged in cc_mode until the voltage equals or exceeds the SET_VOLTAGE
cc_mode	cv_mode	The battery is transitions to cv_mode once the voltage equals or exceeds the SET_VOLTAGE
cv_mode	cv_mode	The battery is charged in cv_mode until the current becomes less than the SET_CURRENT
cv_mode	none	The cv_mode exits when the charging current drops to below the SET_CURRENT
none	cv_mode	The cv_mode charging resumes once the MMPT algorithm is done tracking the maximum power point

6.3. Compensator Implementation in Software

The chapter on controller design discussed the methodology of implementing a digital controller from a control systems perspective. The manner in which the compensator is implemented in code becomes important from a performance and feasibility perspective. The controller implemented as a discrete time difference equation makes the software implementation easy and straightforward. Figure 44 shows the PI compensator flow chart for the voltage mode control while Figure 45 shows the code snippet for the same. Since PI is a first order compensator, only the error and duty cycle values of the previous time step need to be stored. As seen in the block diagram, the error is calculated first followed by the calculation of duty cycle for the next update. The present values of the duty cycle and error terms are updated in the variables storing the previous values. This is because these present values will become the past values in the next cycle.

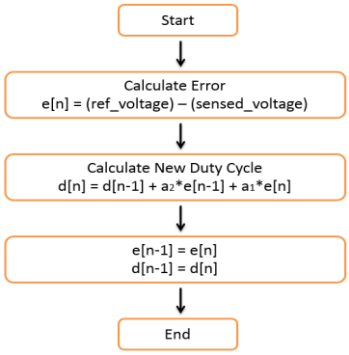

Figure 44. PI Compensator Flow Chart - Voltage Mode Control

The paramters for the PI compensator are references by a structure object. The structure variables error and voltage hold the present error and duty values while the variables error_1 and duty_1 store the previous values.

```
typedef struct
{
    float32 error, error_1;
    float32 duty, duty_1;
}pi_compensator_voltage_mode;

void pid_control_buck1(void)
{
    pid_FDPOL1_Vout.error =   (float32)SetOutputVoltage_POL1 - (float32)SensedVoltage_POL_1 ;

    pid_FDPOL1_Vout.duty =  (pid_FDPOL1_Vout.duty_1) + 0.027789*(pid_FDPOL1_Vout.error + pid_FDPOL1_Vout.error_1);

    if(pid_FDPOL1_Vout.duty<0.1)
        pid_FDPOL1_Vout.duty=0.1;
    if(pid_FDPOL1_Vout.duty>0.98)
        pid_FDPOL1_Vout.duty = 0.98;

    POL1_EPwmOnTime = pid_FDPOL1_Vout.duty*1000;

    pid_FDPOL1_Vout.duty_1 = pid_FDPOL1_Vout.duty;
    pid_FDPOL1_Vout.error_1 = pid_FDPOL1_Vout.error;
}
```

Figure 45. Software Implementation - PI Compensator

The FBCM constant current control uses an extension of the PI controller code discussed above. The flow chart of dual loop control is shown in Figure 46. The structures of outer current loop and inner voltage loop are separate. The result of the outer loop decides the voltage reference for the inner loop. Figure 47 shows the code for dual loop control.

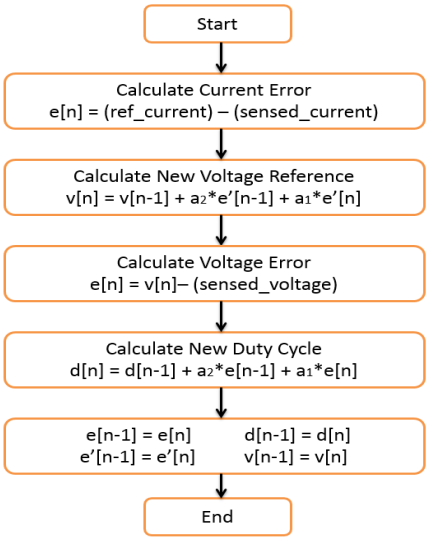

Figure 46. PI Compensator Flow Chart - Dual Loop Control

```
//Buck Converter is bypassed
FBCM1_Buck_EPwmOnTime = 1000;

//outer current loop
pid_FBCM_boost_o.error = SetOutputCurrent_FBCM - current;
pid_FBCM_boost_o.voltage = (pid_FBCM_boost_o.voltage_1) + 0.0045312*(pid_FBCM_boost_o.error + pid_FBCM_boost_o.error_1);

//voltage reference determined by the outer loop
voltage_ref = pid_FBCM_boost_o.voltage;

//inner voltage loop
pid_FBCM_boost.error = pid_FBCM_boost_o.voltage - SensedVoltage_FBCM_Out;
pid_FBCM_boost.duty = (pid_FBCM_boost.duty_1) + 0.010865*(pid_FBCM_boost.error + pid_FBCM_boost.error_1);

if(pid_FBCM_boost.duty<0.01)
    pid_FBCM_boost.duty=0.01;
if(pid_FBCM_boost.duty>0.80)
    pid_FBCM_boost.duty = 0.80;

FBCM1_Boost_EPwmOnTime = 1000 - pid_FBCM_boost.duty*1000;
pid_FBCM_boost_o.voltage_1 = pid_FBCM_boost_o.voltage;
pid_FBCM_boost_o.error_1 = pid_FBCM_boost_o.error;
pid_FBCM_boost.duty_1 = pid_FBCM_boost.duty;
pid_FBCM_boost.error_1 = pid_FBCM_boost.error;
```

Figure 47. Software Implementation – PI Compensator Dual Loop Control

The MPPT controller is responsible for steering the panel voltage to a value that would maximize the harnessed power. The compensator design of the MPPT controller was discussed in the chapter on controller designs.

The input voltage of the FBCM modules, which is similar to the output voltage of the panels, is regulated by a PI compensator. The code structure for output voltage control can be used for input voltage control as well. The code snippet in Figure 48 has the MPPT code for perturb and observe method. The mppt_fbcm_x() subroutine sets the voltage reference while the input_control_fbcm_x() subroutine is a PI loop which steers the panel voltage to the voltage reference. The negative sign in the compensator indicates the fact that increasing the duty cycle will decrease the panel voltage and vice versa.

```
typedef enum {
    UP,
    DOWN
}mppt_direction;

mppt_direction updown = UP;

void mppt_fbcm_x(void)  {
    x_voltage = SensedCurrent_X_In;
    x_current = SensedVoltage_X_In;
    x_power = x_voltage * x_current;

    if(x_power < x_prev_power) {
        if(updown == UP)
            updown = DOWN;
        else
            updown = UP;
    }

    if(updown == DOWN)
        x_panel_voltage_ref -= MPPT_STEP;
    else
        x_panel_voltage_ref += MPPT_STEP;

    x_prev_power = x_power;
    x_panel_voltage = 0;
    x_panel_current = 0;
}
void input_control_fbcm_x() {

    fbcm_x.error =   (float32)x_panel_voltage_ref - (float32)SensedVoltage_X_In;

    fbcm_x.duty = (fbcm_x.duty_1) - 0.079*(fbcm_x.error + fbcm_x.error_1);
    if(fbcm_x.duty<0.20)
            fbcm_x.duty=0.20;
        if(fbcm_x.duty>0.8)
            fbcm_x.duty = 0.8;
    FBCM1_Boost_EPwmOnTime = 1000 - fbcm_x.duty*1000;

    fbcm_x.duty_1 = fbcm_x.duty;
    fbcm_x.error_1 = fbcm_x.error;
}
```

Figure 48. Software Implementation - MPPT P&O Algorithm

6.4. Code Analysis and Profiling

The previous sections discussed about the software structure of the system. The different modules of the code designed to perform dedicated operations were described. The control loop operations like FDPOL voltage control, FBCM battery charge control, and MPPT control and path selection were described. As is evident from the past discussions, intelligent power processing systems like CubeSat EPS pose a significant challenge when it comes to the software design. Hence, it is important that the code be profiled and optimized for speed and memory usage. A code that executes faster will result in an increase in the sampling frequency which enhances the transient performance. Also, a faster code would help in increasing the functionality as more functions can be integrated without compromising the system performance. The main control loop runs every 100µs which means that the voltage/current loops are and run and the duty cycle is updated every 100 µs. In every cycle, the voltage and currents are sampled four times and the values are averaged before being used to calculate the error. Figure 49 shows the relationship between the various intervals. The pink trace shows the switching frequency while the yellow and blue traces show the sampling and update frequencies respectively.

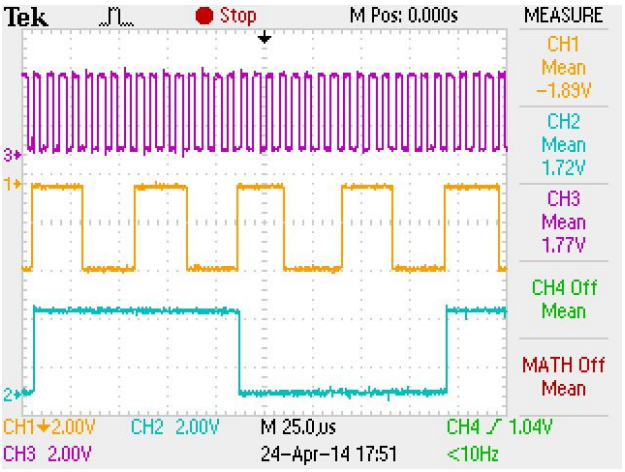

Figure 49: Switching, Sampling and Update Frequencies

The primary step towards designing an efficient software is to determine the time taken by the different code blocks. This can be done by reading the number of ticks taken for the code block to execute.

Table 8 lists the time taken by the various code modules. As mentioned before, the control loop runs every 100µs during which the ADC is run four times. Each sweep of the ADC ISR which involves the calculation of current and voltages from ADC values and calculating average and other such functions take around 20µs to execute resulting in a total of around 80µs. The time taken by the control loop is 4.5µs. The update loop runs the FDPOL PI loops, the battery state machine and the path selection features. The time taken by the battery state machine code and the various PI loops is also listed out in the table. In every timer period, the ADC ISR is run four times and the control is run once. This amounts to a total of around 85µs which is less than the timer period with a safety margin of 15µs.

Table 8. Time taken by various code blocks

Code Segment	**Clock Ticks**	**Time (µs)**
Timer Interrupt Period	15256	101.7
ADC ISR	3000	20
Control Loop	680	4.5
Battery State Machine	250	1.67
FBCM Constant Current PI Loop	150	1
FBCM Constant Voltage PI Loop	120	0.8
MPPT Loop	84	0.56
FDPOL PI Loop	67	0.45
Update Duty Cycle	40	0.27

Figure 50 and Figure 51 depict, graphically, the time consumed by the various code blocks. It is worthwhile to mention that MPPT control, FBCM control, battery state machine and the FDPOL control are a part of the main control loop and get executed depending on the

conditions of the batteries and the solar panel. The time consumed by the control loop is hence an average of the times taken by the control loop for all possible conditions.

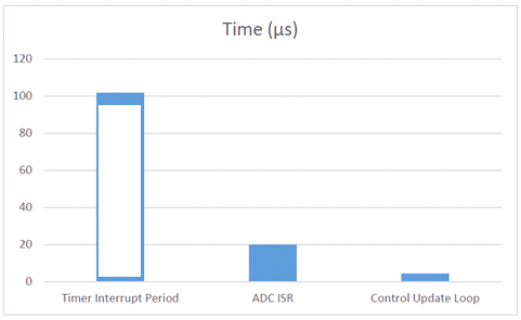

Figure 50: Time taken by the various code blocks

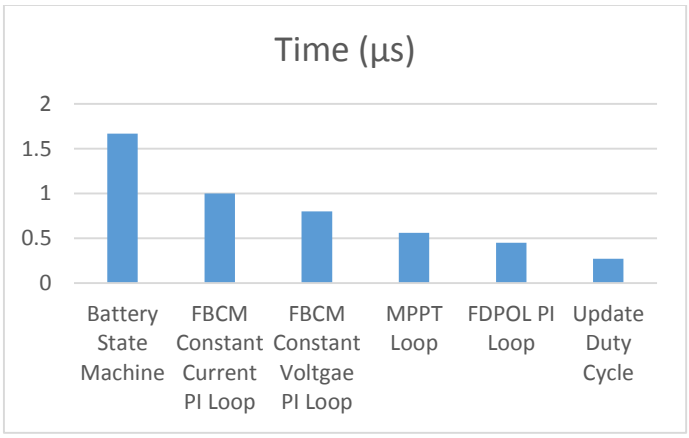

Figure 51. Time taken by the various functions of the control loop

This chapter provides valuable insights into the software structure of the system. The design methodology discussed can be used as a generic blueprint to design control software for power management and processing systems like the CubeSat EPS. The information of the execution time of various code blocks help the programmer to devise effective code optimization schemes.

CHAPTER 7
GaN Device based EPS

The present implementation for the EPS uses silicon MOSFETs. GaN based devices have become prevalent in the past decade and have shown promise of superior performance in the low to mid power domain and a suitable replacement for power MOSFETs. The small size, lower on resistance and less capacitance make then an exciting avenue for use in portable, power and efficient power processing system like the CubeSat EPS [30]. Operation at frequencies in the MHz [31] range permits the use of smaller magnetics. GaN based converter circuits have gained significant attention from the industry as well as the research community. The strive to make efficient portable systems which handle kilo-watts of power has led to the development and analysis of GaN based circuits in variety of topologies.

Hardware Design

A prototype of the CubeSat EPS that uses the EPS2016 [32] in synchronous buck and boost topologies is developed. These devices are capable of operating up to 100V and 11A amperes with an exceptionally low on resistance of 16mΩ. Figure 52 shows the EPC2016 module. It is supplied only in passivated die form with solder bars.

Figure 52. EPC 2016

Figure 53 shows the GaN based EPS board. It is a scaled down version of its silicon counterpart with one FBCM and two FDPOL modules. The two FDPOL modules are 3.3V and 5V buck converters. This makes it easier to test the performance of these devices in solar battery charging systems with multi domain output. The various modules of the board remain similar to the previous board. The devices are triggered using the TI's LM5113 half bridge gate driver and the circuit is designed to switch at 500KHz. This use low loss GaN devices will make the system more efficient and result in maximum utilization of the solar power to charge the batteries and power the FDPOLs.

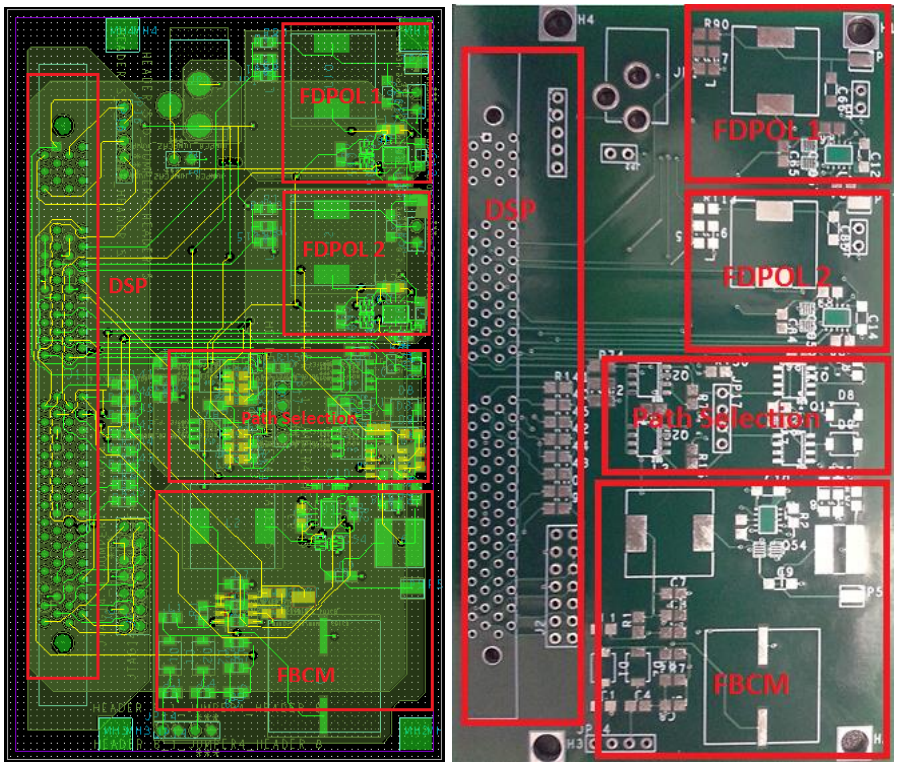

Figure 53. GaN CubeSat EPS

CHAPTER 8
Conclusions

The development of an intelligent and configurable power system for CubeSats and small satellites has provided meaningful insights into the feasibility of such power systems which involve digital control and regulation. With embedded and computing devices scaling down in size and the ever increasing need for extra features, it is imperative that the power delivery and management schemes for such devices become smarter and match up the versatile demands of the product.

The use of solar energy for power generation has been on the rise and this trend is likely to continue for the coming decades. The use of solar energy to power mid power devices like computers and cell phones has attracted significant attention from industry and academia. Efficiency and cost remain the limiting factors. However, with the controllers becoming more powerful and cheaper and the decreasing cost of panels has made it possible to construct intelligent solar power systems tailored to provide power to embedded systems.

The digital control of such multi domain power management and distribution systems poses new challenges as the central controller has to regulate power at multiple points. Along with a thorough knowledge of converter topologies, it entails a deeper understanding of embedded code and its working. The central controller apart from running the control loops, also has to take care other tasks necessary for the correct operation of the system. As a result, the controller part of the code should be optimized to occupy minimal amount of processor time. The development of efficient and optimized control system is crucial for the feasibility of such systems. This requires an in-depth analysis of the load transients and identifying tradeoffs between control loop update rate and response times. A system with lower sampling rate would occupy less processor time but at the same time will exhibits slower response time.

The EPS board implements all of the aforementioned concepts. A multi-domain output voltage regulation control is achieved using a single controller. The sampling periods are set so that the code takes up minimum possible processor time and maintaining decent response times. An intelligent power routing technique is implemented which ensures configurability and fault tolerance. A digital control scheme for battery charging is implemented which directly regulates output current. A digital P&O MPPT controller is designed which ensures that the panels operate at peak efficiency. A battery state machine is implemented which keeps a track of the battery parameters and switches between the constant current and constant voltage charging modes. The state machine also detects when the solar panels are not able to supply the necessary power and runs MPPT algorithm as and when required. A compact and well-structured code that encapsulates all the necessary functions is designed. The code is profiled and the time taken by the various code segments is recorded and discussed so as to come up with the best possible combination of sampling frequency and control loop update rate.

This project also explored the use of gallium nitride (GaN) MOSFETs in such low to middle range power management systems. The properties of these devices enable them to switch at high frequencies which results in a reduction in the size of the magnetic components. This paves the way for smaller and compact circuits with higher power processing capacity. With smaller size and high frequencies, comes the challenge of board design and heat management. However, these devices are bound to play an incremental role towards developing more efficient and compact power management systems.

CHAPTER 9
Future Work

The CubeSat EPS is an excellent test bed for implementing digital photovoltaic power systems. The control structure for output voltage regulation, battery charging system, MPPT and path selection features were implemented. The use of GaN devices was explored as well. The next step towards improving system performance would be to further study control loop performance over a wide range of sampling frequencies and loads. The battery charging system can be improved be implementing advanced battery models including state of charge and health algorithms. The use of fixed point math instead of floating point math should be investigated to reduce the execution time and migrate of low power and simple controllers. The present code can be converted to RTOS implementation for better integration with other functions in the system and easier cross platform compatibility.

The present GaN based CubeSat EPS has a single FBCM and two FDPOL modules. This can be increased to increase the number of modules in the board that can provide additional voltage domains and interface to more number of solar panels. Also, thorough studies on identifying an optimum switching frequency range need to be carried out to help in minimizing loses and selecting the appropriate magnetic components.

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