ABSTRACT

BABAEI, SAMAN. Control Structures for VSC-based FACTS Devices under Normal and Faulted AC-systems. (Under the direction of Dr. Subhashish Bhattacharya.)

This thesis is concerned with improving the Flexible AC Transmission Systems (FACTS) devices performance under the normal and fault AC-system conditions by proposing new control structures and also converter topologies. The combination of the increasing electricity demand and restrictions in expanding the power system infrastructures has urged the utility owners to deploy the utility-scaled power electronics in the power system. Basically, FACTS is referred to the application of the power electronics in the power systems. Voltage Source Converter (VSC) is the preferred building block of the FACTS devices and many other utility-scale power electronics applications. Despite of advances in the semiconductor technology and ultra-fast microprocessor based controllers, there are still many issues to address and room to improve[25]. An attempt is made in this thesis to address these important issues of the VSC-based FACTS devices and provide solutions to improve them.

Control Structures for VSC-based FACTS Devices under Normal and Faulted AC-systems

by
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DEDICATION

To my mother

Nahid Chaparchi

BIOGRAPHY

The author, Saman Babaei, was born in Tehran, Iran. He received the B.Sc. and M.Sc. degrees in electrical engineering from Iran University of Science and Technology, Tehran Iran, and Chalmers University of Technology, Gothenburg, Sweden respectively. He had four years of working experience in the area of power system operation and protection.

In 2010, he started to peruse his PhD in Electrical Engineering at North Carolina State University. He was a member of the NSF Engineering Research Center for Future Renewable Electric Energy Delivery and Management (FREEDM) Systems Center. During his PhD study, he worked for the Quanta Technology Company as a graduate intern. His research interests include FACTS and HVDC, utility applications of power electronics, Power electronics converter design and control, application of power electronics in renewable energy integration to the grid, and smart grid.

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Chapter 1: Introduction

1.1 Background

At the present time, by daily increasing the electricity demand, power systems are forced to operate at their full capacity which puts too much stress on the system. Moreover, generation patterns frequently result in overloading of the transmission systems that tend to incur greater losses as well as decrease in the system stability margin and security level [1]. Therefore, the power system needs to be reinforced to increase its capacity and become smarter, aware, more fault-tolerant, self-healing and statically and dynamically controllable.

The traditional alternative to reinforce the power system is to build up new power infrastructures such as transmission lines, electrical substations, and associated equipment. However, due to the environmental issues and also high cost of the reinforcing power system through the addition of the new infrastructures, the power system expansions are often restricted [1],[2].

Besides the traditional alternative, the other solution in response to the mentioned challenges is optimizing the utilization of the existing power system through the application of the advanced power electronics technology. Flexible AC Transmission System (FACTS) is referred to the application of the power electronics in the power systems. FACTS technology provides technical solutions to increase the utilization capacity of the existing power systems assets and also address the new operating challenges being presented today. Devices, such as a Static Synchronous Compensator (STATCOM), Static Var Compensator (SVC), Static Synchronous Series Compensator (SSSC), and Unified Power Flow Controller

(UPFC), can be connected in series or shunt (or a combination of the two) to achieve numerous control functions including voltage regulation, power flow control, and system damping [2]-[24]. In this way, the system performance can be considerably improved. Following are few examples of the long list of the benefits that FACTS devices offer:

- Utilizing the power system infrastructures up to their thermal limits without sacrificing the system stability and security.
- Continuous control over the system voltage profile.
-Reactive power support functionality to improve the system voltage profile, decreasing the system losses and also improving the system voltage stability
-Power flow controllability
-Power system oscillation damping

1.2 Relevance

This thesis is concerned with improving the FACTS devices performance by proposing new control structures and also converter topologies. As mentioned in the preceding section, the combination of the increasing electricity demand and restrictions in expanding the power system has urged the utility owners to use the FACTS devices.

Voltage Source Converter (VSC) is the preferred building block of the FACTS devices and many other utility-scale power electronics applications. Despite of advances in the semiconductor technology and ultra-fast microprocessor based controllers, there are still many issues to address and room to improve[25]. VSC-based STATCOMs for example are very sensitive to the voltage disturbances especially unbalanced condition and system faults. To protect the semiconductor switches from the huge fault current flow, the STATCOM is

tripped under utility system faults or severe unbalanced conditions when its reactive power support functionality is really needed.

Basically, the inverter power components and switches must be designed for the peak continuous operating current and for the peak continuous operating voltage. Generally there is a designed margin beyond this point to accommodate some percentage overload as well as specified abnormal operating condition particularly unbalanced condition and grid faults. The MVA rating of the equipment and hence the cost is derived from the product of peak voltage and current (considering the fault and unbalanced condition), regardless of whether they occur at the same time or not [26]. Hence, the appropriate controller which is capable of limiting the fault current and consequently decrease the converter design margin will significantly reduce the converter equipment rating and cost.

The other example of the challenges regarding the VSC-based FACTS devices is the controllability range of the specific type of the UPFC in which the DC-link voltage is not fixed and is regulated over the range of the values. Many of the UPFC installations around the world are of this kind. In this type of the UPFCs, the controllability range is varied with shunt inverter operating point.

An attempt is made in this thesis to address these important issues of the VSC-based FACTS devices and provide solutions to improve them.

1.3 Contributions

The key contributions of this thesis are enumerated as follows:

1. Design a new control structure (Dual Angle Controller) to improve the line-frequency-switched (angle-controlled) STATCOM performance under unbalanced conditions and system faults. *(Chapter 3)*
2. Application of the DC-side active power filters to improve the line-frequency-switched (angle-controlled) STATCOM performance under unbalanced conditions and system faults. *(Chapter 4)*
3. An alternative control structure to improve the PWM-controlled VSC-based STATCOMs under AC-system faults. *(Chapter 5)*
4. Designing an alternative controller for the PWM-controlled VSC which is capable of instantaneous limiting the negative sequence current under fault conditions. When the line voltage is distorted by the specific harmonics, this controller can also be used to eliminate those harmonics in the current spectrum. *(Chapter 6)*
5. Design a controller to improve the controllability range of specific type of the UPFC in which the DC-link voltage is not fixed but regulated over the range of the values. Most of the existing transmission level UPFC installations around the world are of this kind. This controller increases the UPFC controllability range when its DC-link voltage is at minimum level. *(Chapter 7)*

1.4 Organization

Followed by the introduction, chapter 2 provides a literature survey on essential topics of this research. It starts with calculating a mathematical model for generally a VSC and particularly a STATCOM connected to the grid. That is followed by introduction of the existing control structures for the STATCOM (PWM-based vector controller, and angle-controller) and discussing the pros and cons of each of them for the transmission level application. For the literature review part of this chapter which provides the basic dynamic and static equations of the STATCOM that will be used afterward in the thesis, a close look has been taken to the Dr. Colin Schauder paper [19].This paper has been referred wherever possible through this chapter.

Chapter 3 addresses the issues regarding the angle-controlled STATCOM performance under AC-system faults. It starts with calculation of the DC, and AC-sides waveforms of the STATCOM under unbalanced condition and afterward these equations are particularly used to develop the Dual angle controller (DAC). DAC limits the STATCOM fault currents and removes the DC-link voltage 2^{nd} harmonic oscillation under severe unbalanced conditions and AC-system faults. The proposed DAC performance has been validated by the simulation and experimental results.

Chapter 4 addresses the same issue of the Angle-controller STATCOM performance under unbalanced condition and AC-system faults that was discussed in the preceding chapter but proposes an alternative solution to resolve it. A new converter topology along with appropriate control structure is presented in this chapter that limits the negative

sequence currents under system faults. The proposed solution is validated by the simulation results.

Chapter 5 uses the basic idea of the chapter 3 to develop an alternative control structure that improves the PWM-controlled VSC-based STATCOM performance under AC-system fault conditions. The theoretical results of this chapter are supported by the simulation and Hardware-In-the- Loop-test results.

Chapter 6 proposes a control structure that improves the grid-connected PWM-controlled VSC currents Total Harmonic Distortion (THD) and removes the DC-link voltage oscillations when the input voltage is distorted by the low/high order harmonics. The input voltage harmonic can range from (-1) which corresponds to the unbalanced AC-system conditions to any high order harmonic (providing that the switching frequency is high enough). In particular, when the input voltage is unbalanced due to the fault condition, the proposed controller instantly limits the negative sequence current and removes the DC-link voltage oscillations. The proposed controller performance is validated by the precise simulation and Hardware-In-the- Loop-test results.

Chapter 7 starts with deriving the mathematical model of the UPFC series inverter. Based on this model, existing power flow controller are discussed and analyzed with appropriate simulation results. A close attention has been taken into the specific type of the UPFC in which the DC-link voltage is not fixed but regulated over the range of the values. This type of the UPFC has been discussed in detail through this chapter. Finally this chapter ends up with proposing a controller that increases the controllability range of this type of the UPFC when the DC-link voltage is at its minimum value.

Chapter 2: Review of different control structure for the STATCOM

2. 1 Introduction

VSC-based STATCOMs are used for voltage regulation in transmission and distribution systems. The VSC-based STATCOM operation is based on the principle that a VSC inverter can be connected between the three phase AC-system and an energy storage device such as a capacitor and controlled to exchange mainly reactive current with AC-system[19]. Basically from the power system point of view the STATCOM is seen as a controllable current source that injects (almost) 90 degrees leading or lagging current to the AC-system. This provides the capability to act as either sink or source of the reactive power to the grid. And finally this reactive power support functionality is used to regulate the AC-bus voltage at the point of connection.

In this chapter the dynamic behavior of the STATCOM has been studied in depth. First, the mathematical model of the STATCOM is derived. Then, this model is used to develop the existing controllers i.e. vector controller (PWM Controller), and angle controller. The pros and cons of each control method are discussed in detail for transmission level applications. The more emphasize has been given to the angle controller. In this chapter besides the PSCAD, and Real Time Digital Simulation (RTDS) results, experimental results based on a scaled analog model of a real 100 MVA STATCOM has been presented.

2. 2 Derivation of the STATCOM Mathematical Model

2.2.1 Stationary (αβ) and synchronous (dq) coordinate systems

The main function of the STATCOM is to regulate the AC-bus voltage at the point of connection by acting as a source or sink of the reactive power. From the power system point of view the STATCOM is seen as a controllable reactive current source. Reactive current is part of the current associated with reactive power and does not have any effect on the active power.

The reactive power and current are well known, however, for designing a controller with response time as fast as a fraction of a cycle a broader definition of the reactive power (current) is required which is valid on an instantaneous basis. The instantaneous active power at a point on the line is given by [19]:

$$P = v_a i_a + v_b i_b + v_c i_c \tag{2-1}$$

The instantaneous reactive current can be defined as that part of the three phases current that can be eliminated at any instance without altering the real power [19]. To obtain the algebraic equation of the active and reactive instantaneous current, it is needed to transfer all the variables into a domain in which the instantaneous calculation is possible.

Based on the Park transformation theory [27], A set of three instantaneous phase variable that sum to zero can be uniquely represented by a single point in a plane. By definition the vector drawn from origin to this point has vertical projection onto each of three symmetrically disposed phase axes which corresponds to the instantaneous value of the associated phase variable. The vector contains all the information on the three phase set including steady-state unbalance, harmonics and transient components [19].

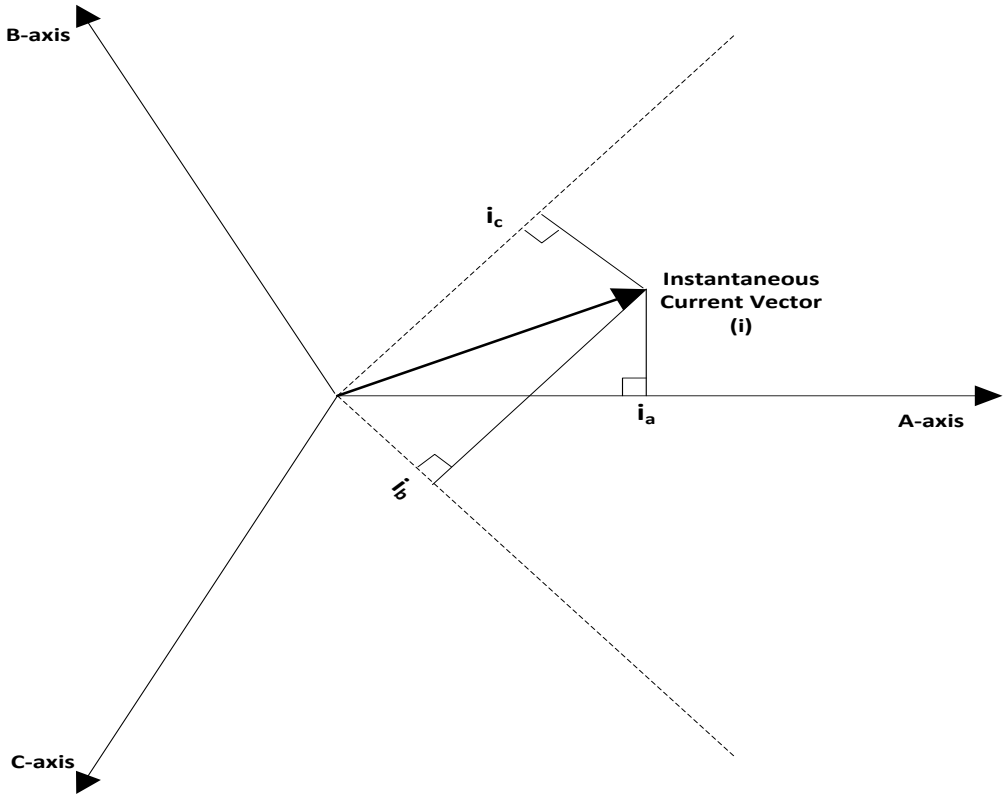


Figure 2-1. Instantaneous current vector

Based on instantaneous vector theory, a coordinate system is introduced in which the α-axis is coincident to the phase A-axis and β-axis is perpendicular to the α-axis. The transformation from abc domain to the αβ domain is defined as in:

$$\begin{bmatrix} i_\alpha \\ i_\beta \\ 0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{2-2}$$

Figure 2-2 indicates the current and voltage instantaneous vectors in the αβ coordinate system. Equation (2-1) can be rewritten in the αβ-coordinate system as in:

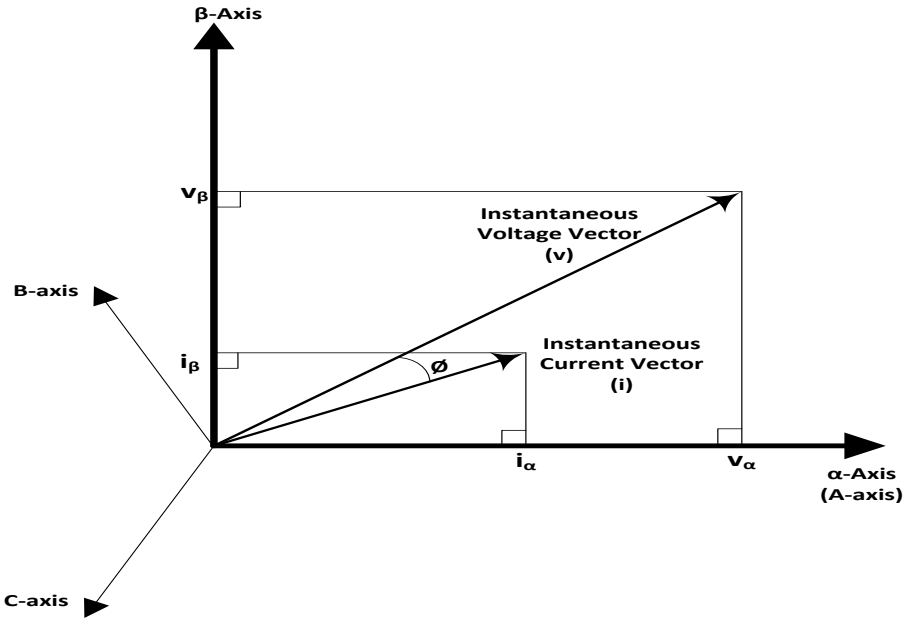


Figure 2-2. Instantaneous vectors in αβ coordinate system

$$P = \frac{3}{2}\left(v_\alpha i_\alpha + V_\beta\, I_\beta\right) \tag{2-3}$$

Inspection of (2-3) indicates that the instantaneous active power is the dot (scalar) product of the instantaneous voltage and current vectors in the stationary αβ-coordinate system. Therefore (2-3) can be rewritten as in:

$$P = \frac{3}{2}|V||I|\,cos(\emptyset) \tag{2-4}$$

where ϕ is the angle between the instantaneous current and voltage vector. Therefore, the part of the current which is aligned with the instantaneous voltage vector ($|\mathrm{I}|\cos(\emptyset)$) contributes to the active power and the remaining part ($|\mathrm{I}|\sin(\emptyset)$) has no part in the active power construction and therefore is the reactive current. The instantaneous reactive power is

defined as the cross product of the instantaneous voltage vector by the instantaneous current vector:

$$Q = \frac{3}{2}|V||I|\,sin(\emptyset) \tag{2-5}$$

Equation (2-5) can be rewritten as in (2-6):

$$Q = \frac{3}{2}(V_\alpha I_\beta - V_\beta I_\alpha) \tag{2-6}$$

Inspection of Figure 2-2, and considering (2-4), and (2-5) indicates that defining a rotatory co-ordinate system in which one of the axes is always coincident with instantaneous voltage vector, leads to useful separation of the variables for the active and reactive power control. Therefore, the synchronous frame (dq coordinate system) is designed in a way that d-axis is always coincident with instantaneous voltage vector and q-axis is perpendicular to the d-axis. Note should be taken that synchronous frame is not a stationary frame and d and q-axis rotate with instantaneous voltage vector. The equation (2-5), and (2-6) can be simply rewritten in the synchronous frame as in:

$$P = \frac{3}{2}|V|i_d = \frac{3}{2}v_d i_d \tag{2-7}$$

$$Q = \frac{3}{2}|V|i_q = \frac{3}{2}v_d i_q \tag{2-8}$$

The instantaneous voltage and current vectors in the synchronous reference frame are illustrated in Figure 2-3.

Equation (2-7), and (2-8) clearly show that in the synchronous frame the instantaneous active and reactive current are separated. i_d is always aligned with instantaneous voltage

vector and only contributes to the active power while i_q is always perpendicular to the instantaneous voltage vector and only contributes to the reactive power.

Transformation from abc to the synchronous frame is defined as: [19],[28].

$$f_{dq} = T(\omega t) f_{abc} \tag{2-9}$$

$$f_{abc} = T(\omega t)^{-1} f_{dq} \tag{2-10}$$

Where:

$$T(\omega t) = \frac{2}{3}\begin{bmatrix} \cos(\omega t) & \cos(\omega t - \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \\ -\sin(\omega t) & -\sin(\omega t - \frac{2\pi}{3}) & -\sin(\omega t + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \tag{2-11}$$

and ωt is the ac-bus phase locked loop output.

Writing the abc domain variables in terms of dq variables based on (2-10) and substitute them in (2-1), then the active and reactive powers in terms of dq variables are obtained as in:

$$P = \frac{3}{2}(v_d i_d + v_q i_q) \tag{2-12}$$

$$Q = \frac{3}{2}(v_d i_q - v_q i_d) \tag{2-13}$$

(2-12), and (2-13) are the general equations of the active and reactive power in the synchronous frame. When the d-axis is coincident with instantaneous voltage vector (which is usually the case in dealing with power electronics converters) then $v_q = 0$, and $v_d = |V|$ and therefore, equation (2-12), and (2-13) simplified to (2-7), and (2-8) respectively.

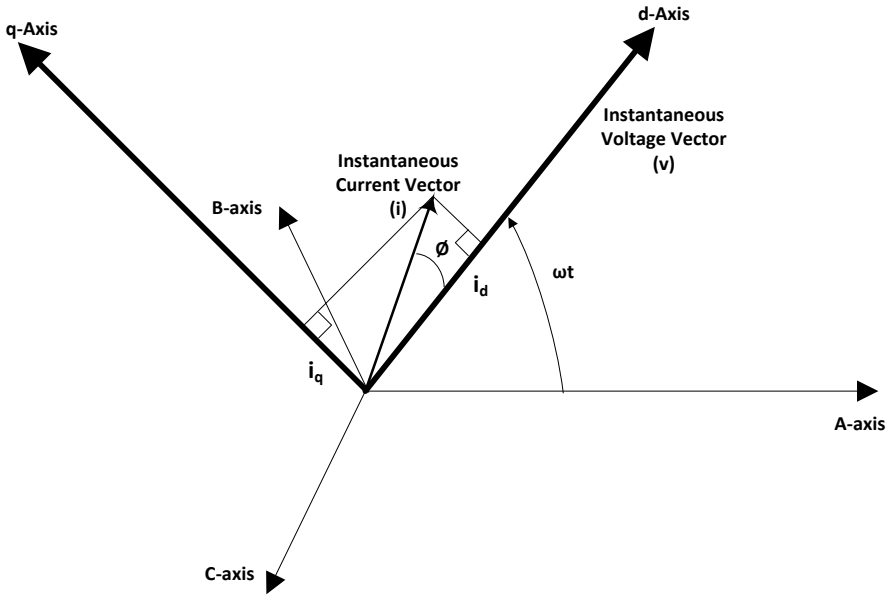


Figure 2-3. Instantaneous vectors in synchronous frame (dq)

2.2.2 STATCOM equations and controllers

Figure 2-4 indicates the equivalent circuit of the STATCOM connected to the AC-system. The derivative of the STATCOM tie line currents with respect to the time can be written as in:

$$\frac{d}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} \frac{-R}{L} & 0 & 0 \\ 0 & \frac{-R}{L} & 0 \\ 0 & 0 & \frac{-R}{L} \end{bmatrix}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \frac{1}{L}\begin{bmatrix} e_a - v_a \\ e_b - v_b \\ e_c - v_c \end{bmatrix} \tag{2-14}$$

For controller design, it is always easier to work with per-unit value. The per-unit system can be obtained according the following equations [19]:

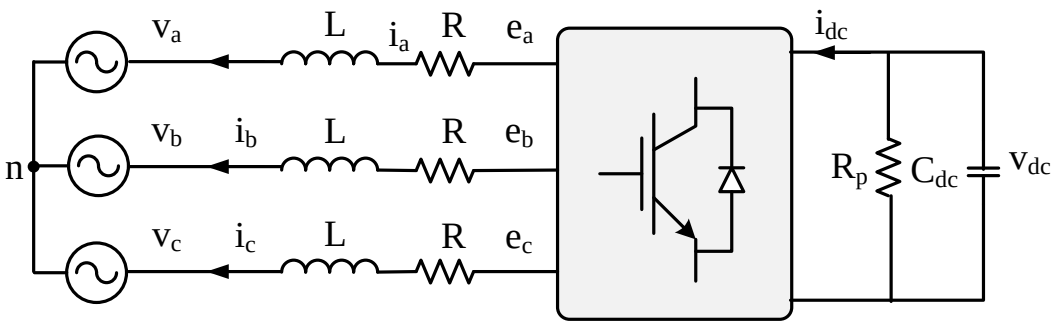


Figure 2-4. STATCOM connected to the AC-system

$$L_{pu} = \frac{\omega_b L}{Z_{base}} \tag{2-15}$$

$$C_{pu} = \frac{1}{\omega_b C Z_{base}} \tag{2-16}$$

$$R_{pu} = \frac{R}{Z_{base}} \tag{2-17}$$

$$i_{pu} = \frac{i}{i_{base}} \tag{2-18}$$

$$v_{pu} = \frac{v}{v_{base}} \tag{2-19}$$

$$Z_{pu} = \frac{v_{base}}{i_{base}} \tag{2-20}$$

Per-unitizing (2-14) based on (2-15)-(12-20), we obtain:

$$\frac{d}{dt}\begin{bmatrix} i_{apu} \\ i_{bpu} \\ i_{cpu} \end{bmatrix} = \begin{bmatrix} \frac{-R_{pu}\omega_b}{L_{pu}} & 0 & 0 \\ 0 & \frac{-R_{pu}\omega_b}{L_{pu}} & 0 \\ 0 & 0 & \frac{-R_{pu}\omega_b}{L_{pu}} \end{bmatrix} \begin{bmatrix} i_{apu} \\ i_{bpu} \\ i_{cpu} \end{bmatrix} + \frac{\omega_b}{L_{pu}} \begin{bmatrix} e_{apu} - v_{apu} \\ e_{bpu} - v_{bpu} \\ e_{cpu} - v_{cpu} \end{bmatrix} \tag{2-21}$$

Transferring (2-21) from abc domain to the synchronous frame based on (2-11) yields:

$$\frac{d}{dt}\begin{bmatrix} i_{dpu} \\ i_{qpu} \end{bmatrix} = \begin{bmatrix} \frac{-R_{pu}\omega_b}{L_{pu}} & \omega \\ -\omega & \frac{-R_{pu}\omega_b}{L_{pu}} \end{bmatrix} \begin{bmatrix} i_{dpu} \\ i_{qpu} \end{bmatrix} + \frac{\omega_b}{L_{pu}} \begin{bmatrix} e_{dpu} - |v|_{pu} \\ e_{qpu} \end{bmatrix} \quad (2\text{-}22)$$

Rearranging (2-22) we obtain:

$$\begin{bmatrix} e_{dpu} \\ e_{qpu} \end{bmatrix} = \begin{bmatrix} \frac{L_{pu}}{\omega_b}\frac{d}{dt} i_{dpu} + R_{pu} i_{dpu} - \frac{L_{pu}\omega}{\omega_b} i_{qpu} + |v|_{pu} \\ \frac{L_{pu}}{\omega_b}\frac{d}{dt} i_{qpu} + R_{pu} i_{qpu} + \frac{L_{pu}\omega}{\omega_b} i_{dpu} \end{bmatrix} \quad (2\text{-}23)$$

Inspection of equation (2-23) clearly indicates that i_{dpu} and i_{qpu} can easily be controlled using e_{dpu} and e_{qpu} respectively. The coupling between the d and q components can be removed by adding proper terms to the controller output. Feed-forwarding the $|v|_{pu}$ to the d-axis controller output also improves the converter dynamic performance. Therefore, the control structure of the vector controlled (PWM-controlled) STATCOM can be illustrated as in Figure 2-5.

From the control point of view a converter can be considered as an ideal power transformer with a time delay. The output voltage of the converter is assumed to follow a voltage reference signal with an average time delay due to the PWM switching. Let's assume that the switching frequency is high enough such that the average time delay is negligible. Therefore, we will have:

$$\begin{bmatrix} e_{dpu\,ref} \\ e_{qpu\,ref} \end{bmatrix} = \begin{bmatrix} e_{dpu} \\ e_{qpu} \end{bmatrix} \quad (2\text{-}24)$$

Considering the control structure of Figure 2-5 and equation (2-24), thene_{dpu}, and e_{qpu} in the Laplace domain are calculated as in:

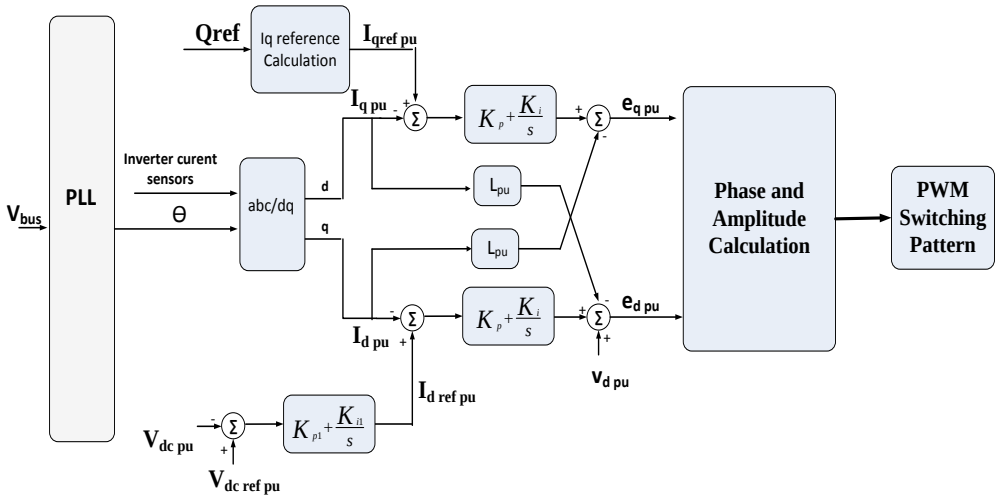


Figure 2-5. Vector controlled STATCOM control structure

$$e_{dpu} = \left(i_{drefpu} - i_{dpu}\right)\left(k_p + \frac{k_i}{s}\right) - L_{pu} i_{qpu} + |v|_{pu} \tag{2-25}$$

$$e_{qpu} = \left(i_{qrefpu} - i_{qpu}\right)\left(k_p + \frac{k_i}{s}\right) + L_{pu} i_{dpu} \tag{2-26}$$

These two equations show that the reference voltage of the inverter can be split into two components. One of them is obtained from the PI controller and the other one is feed-forward term to remove the coupling between d and q axis and also improve the transient response. The reference for the q component of the STATCOM current is calculated based on the required capacitive or inductive reactive power at the point of the connection. The d component reference value is calculated by a PI controller that regulates the DC-link voltage at a fixed value.

The PWM-controlled STATCOM may be uneconomical for many transmission level FACTS devices due to the high switching losses of the PWM VSCs. Apart from the PWM-controlled STATCOM; there is another STATCOM controller which is based on controlling

only the angle of the output voltage. It has been shown in [19] that by a slight change of the inverter output voltage angle (α) for a controlled time; the inverter is able to provide inductive/capacitive reactive power. Basically, by controlling the α toward the positive/negative direction , for a controlled time, the DC-link voltage is driven lower/higher and therefore the VSC output voltage decreases/increases accordingly[29].In this type of inverter, the ratio between AC and DC voltages is kept constant and the VSC output voltage magnitude is varied indirectly by changing the DC-bus voltage. Since angle α is the only control input in this control strategy, it is called angle control.

Since in the angle-controlled STATCOM the inverter output voltage is controlled by changing the DC-link voltage level, it is necessary to include the DC-side equation in the STATCOM model. The instantaneous active power at the AC and DC-side of the inverter are identical. Therefore we have:

$$v_{dcpu} i_{dcpu} = \frac{3}{2}\left(e_{dpu} i_{dpu} + e_{qpu} i_{qpu}\right) \tag{2-27}$$

And the DC-side circuit equation is:

$$\frac{d}{dt} v_{dcpu} = -\omega_b C_{pu}\left(i_{dcpu} + \frac{v_{dcpu}}{R_{ppu}}\right) \tag{2-28}$$

R_p is a shunt resistance at DC-side that models the converter losses. In all the converters the absolute value of the fundamental inverter output voltage is proportional with DC link voltage.

$$e = kV_{dc} \tag{2-29}$$

And therefore:

$$e_d = kV_{dc}cos\alpha \tag{2-30}$$

$$e_q = kV_{dc}sin\alpha \tag{2-31}$$

k is the factor for inverter which relates the DC-side voltage to the amplitude of the phase to neutral voltage at the inverter AC-side terminals.

Combining equations (2-22), (2-27), (2-28), (2-30), and (2-31), yields:

$$\frac{d}{dt}\begin{bmatrix} i_{dpu} \\ i_{qpu} \\ v_{dcpu} \end{bmatrix} \tag{2-32}$$

$$= \begin{bmatrix} \frac{-R_{pu}\omega_b}{L_{pu}} & \omega & \frac{k\omega_b\cos(\alpha)}{L_{pu}} \\ -\omega & \frac{-R_{pu}\omega_b}{L_{pu}} & \frac{k\omega_b\sin(\alpha)}{L_{pu}} \\ \frac{-3}{2}kC_{pu}\omega_b\cos(\alpha) & -\frac{3}{2}kC_{pu}\omega_b\sin(\alpha) & \frac{-C_{pu}\omega_b}{R_{ppu}} \end{bmatrix} \begin{bmatrix} i_{dpu} \\ i_{qpu} \\ v_{dcpu} \end{bmatrix}$$

$$-\frac{\omega_b}{L_{pu}}\begin{bmatrix} |v|_{pu} \\ 0 \\ 0 \end{bmatrix}$$

Rearranging (2-32), we will have:

$$\frac{d}{dt}\begin{bmatrix} i_{dpu} \\ i_{qpu} \\ v_{dcpu} \end{bmatrix} \tag{2-33}$$

$$= \begin{bmatrix} \frac{-R_{pu}\omega_b}{L_{pu}}i_{dpu} + \frac{\omega_b(kv_{dcpu}cos\alpha - |v|_{pu})}{L_{pu}} + \omega i_{qpu} = f1 \\ \frac{-R_{pu}\omega_b}{L_{pu}}i_{qpu} + \frac{k\omega_b sin(\alpha)}{L_{pu}}v_{dcpu} - \omega i_{dpu} = f2 \\ \frac{-C_{pu}\omega_b}{R_{ppu}}v_{dcpu} - \frac{3}{2}kC_{pu}\omega_b\cos(\alpha)\, i_{dpu} - \frac{3}{2}kC_{pu}\omega_b\sin(\alpha)\, i_{qpu} = f3 \end{bmatrix}$$

State space equations in (2-32) are nonlinear if α is considered as one of the system input. However, by linearizing equation (2-32) around an equilibrium point, it is possible to analyze the perturbation of the d and q component of the current and also DC-link voltage about a chosen steady state point. f1, f2, and f3 are nonlinear differential equations defined in (2-33). The linearization process is carried out based on (2-34):

$$\frac{d}{dt}\begin{bmatrix}\Delta i_{dpu}\\ \Delta i_{qpu}\\ \Delta v_{dcpu}\end{bmatrix}=\begin{bmatrix}\frac{\partial f1}{\partial i_{dpu}} & \frac{\partial f1}{\partial i_{qpu}} & \frac{\partial f1}{\partial v_{dcpu}}\\ \frac{\partial f2}{\partial i_{dpu}} & \frac{\partial f2}{\partial i_{qpu}} & \frac{\partial f2}{\partial v_{dcpu}}\\ \frac{\partial f3}{\partial i_{dpu}} & \frac{\partial f3}{\partial i_{qpu}} & \frac{\partial f3}{\partial v_{dcpu}}\end{bmatrix}\begin{bmatrix}\Delta i_{dpu}\\ \Delta i_{qpu}\\ \Delta v_{DCpu}\end{bmatrix}+\begin{bmatrix}\frac{\partial f1}{\partial |v|_{pu}} & \frac{\partial f1}{\partial \alpha}\\ \frac{\partial f2}{\partial |v|_{pu}} & \frac{\partial f2}{\partial \alpha}\\ \frac{\partial f3}{\partial |v|_{pu}} & \frac{\partial f3}{\partial \alpha}\end{bmatrix}\begin{bmatrix}\Delta|v|_{pu}\\ \Delta\alpha\end{bmatrix} \tag{2-34}$$

and therefore linearizing (2-33) based on (2-34) yields:

$$\frac{d}{dt}\begin{bmatrix}\Delta i_{dpu}\\ \Delta i_{qpu}\\ \Delta v_{dcpu}\end{bmatrix} \tag{2-35}$$

$$=\begin{bmatrix}\frac{-R_{pu}\omega_b}{L_{pu}} & \omega_b & \frac{k\omega_b cos(\alpha_0)}{L_{pu}}\\ -\omega_b & \frac{-R_{pu}\omega_b}{L_{pu}} & \frac{k\omega_b sin(\alpha_0)}{L_{pu}}\\ \frac{-3}{2}kC_{pu}\omega_b cos(\alpha_0) & -\frac{3}{2}kC_{pu}\omega_b sin(\alpha_0) & \frac{-C_{pu}\omega_b}{R_{ppu}}\end{bmatrix}\begin{bmatrix}\Delta i_{dpu}\\ \Delta i_{qpu}\\ \Delta v_{dcpu}\end{bmatrix}$$

$$+\begin{bmatrix}\frac{-\omega_b}{L_{pu}} & \frac{-k\omega_b v_{dcpu0} sin(\alpha_0)}{L_{pu}}\\ 0 & \frac{k\omega_b v_{dcpu0} cos(\alpha_0)}{L_{pu}}\\ 0 & \frac{3}{2}kC_{pu}\omega_b(sin(\alpha_0)\, i_{dpu0} - cos(\alpha_0)\, i_{qpu0})\end{bmatrix}\begin{bmatrix}\Delta|v|_{pu}\\ \Delta\alpha\end{bmatrix}$$

Equation (2-35) indicates the dynamic behavior of the STATCOM controlled by the angel controller. Subscript 0 denotes that the signal is at its equilibrium point. Using the state space

equations of (2-35), the transfer function between the i_{qpu} perturbations (Δi_{qpu}) and $\Delta\alpha$ is calculated as in [19]:

$$\frac{\Delta i_{qpu}(s)}{\Delta\alpha(s)} = \frac{v_{dcpu0}\left(s^2 + C^{"}L^{"}\right)L^{"} + C^{"}L^{"}\omega_b i_{qpu0}}{s(s^2 + C^{"}L^{"} + {\omega_b}^2)} \tag{2-36}$$

Where [19]:

$$L^{"} = \frac{kw_b}{L_{pu}} \tag{2-37}$$

$$C^{"} = \frac{3kw_b C_{pu}}{2} \tag{2-38}$$

Note should be taken that to obtain this transfer function the AC-system cupper losses and also converter switching losses are ignored ($R_{pu} = 0,\ R_{ppu} = \infty$, and$\alpha_0 = 0$). Having obtained the transfer function between the Δi_{qpu} and $\Delta\alpha(s)$ and using the well-known control rules it is possible to design an appropriate controller. Figure 2-6 illustrates the control structure of the STATCOM working with angle controller.

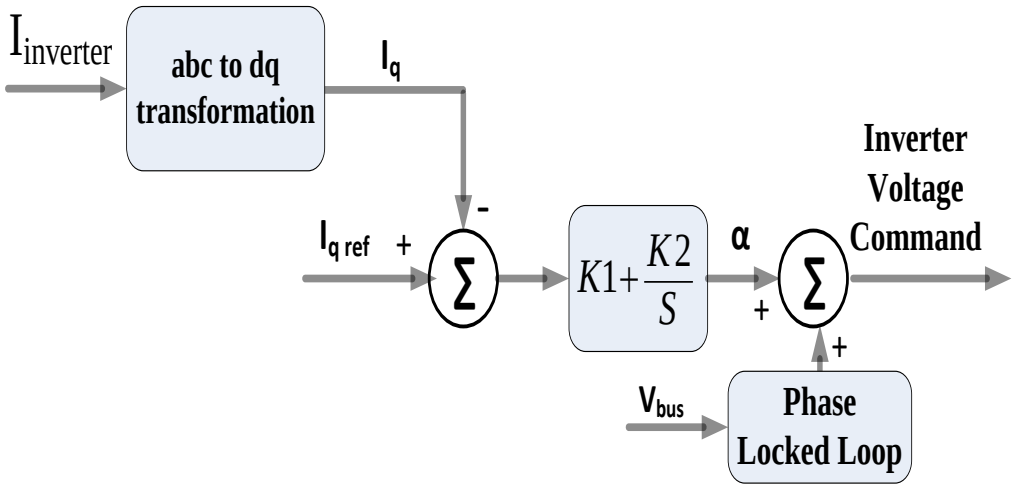


Figure 2-6. Angle controller

2. 3 Comparison between the PWM-controlled and angle-controlled STATCOM performances

In the previous sections, the STATCOM mathematical model was obtained and two possible control structure i.e. PWM-based Vector controller and angle controller were discussed in detail. In this part of the thesis, first the converter topology of the PWM-controlled VSC-based STATCOM along with simulation results is presented. This is followed by comprehensive analysis of the line-frequency-switched pulse inverters used for the voltage construction of the angle-controlled STATCOMs. PSCAD/EMTDC , Real Time Digital Simulation (RTDS), and experimental results of the angle-controlled STATCOM performance under different control commands are also presented in this section. The experiments were conducted on a Transient Network Analyzer (TNA), a unique hardware based FACTS system simulator which was designed to study system faults and transients for a 2×100 MVA STATCOM field installation.

2.3.1 PWM-controlled VSC-based STATCOM

Figure 2-7 indicates a simple 2-level VSC-based inverter. This inverter is controlled using the PWM technique. The DC-link is connected to the series connection of two DC-voltage sources. In this inverter the DC-link voltage is being chopped with the PWM pulses to any arbitrary voltage vector with desired amplitude and angle.

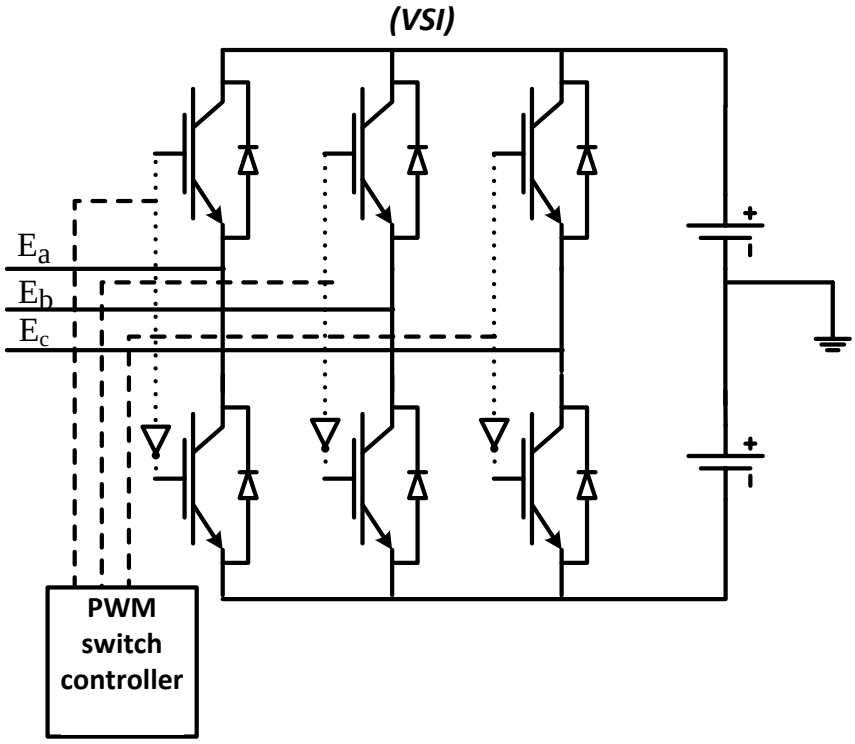


Figure 2-7. 2-level VSC-based PWM controlled inverter

Figure 2-8 indicates the voltage spectrum of this inverter with different modulation index. The switching frequency is set to 21 times of the line frequency (21×60=1260). As can be seen in this figure the harmonics value around the switching frequency and its multiple is

very large. Usually the switching frequency is set to a large number to push the harmonics far from the line frequency. The inductor that connects the inverter to the grid is seen as the open circuit for the high order harmonics and prevents them to reach to the grid (providing that the switching frequency is large enough). However, the larger the switching frequency the more converter losses we will have. Therefore, for transmission level applications the PWM-controlled inverter is uneconomical.

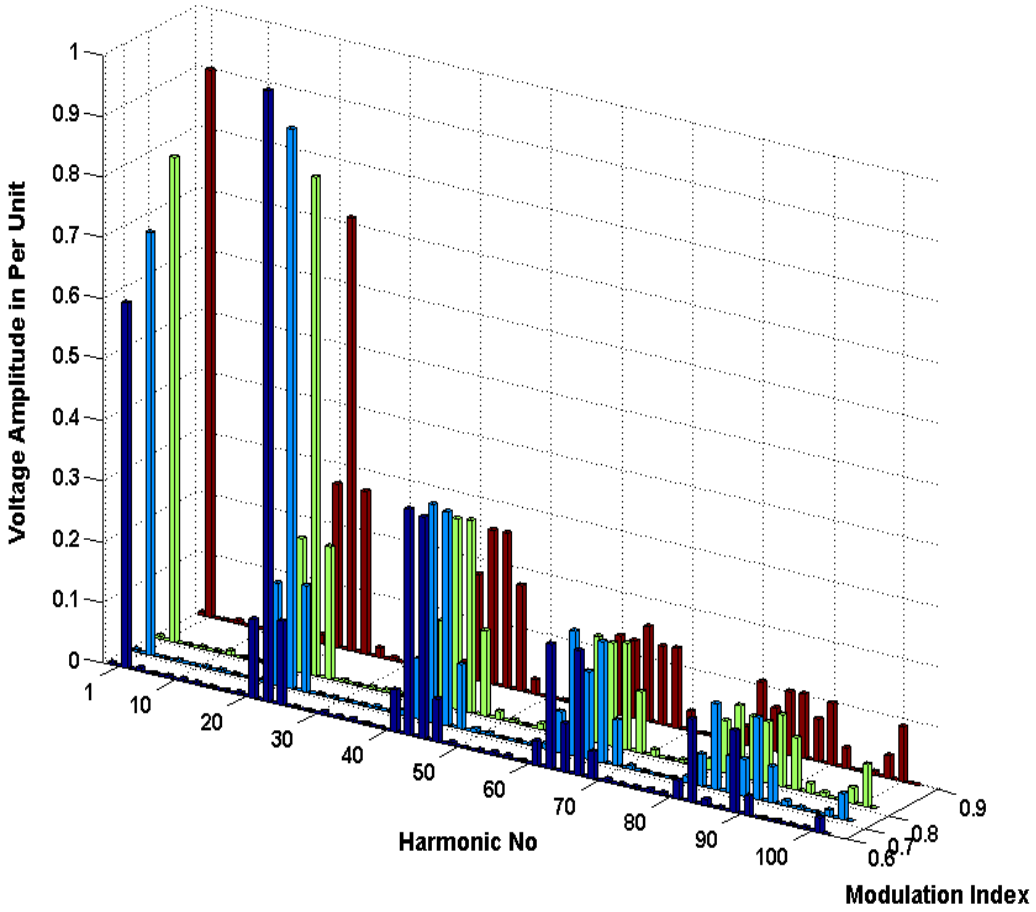


Figure 2-8. 2-level VSC-based PWM controlled inverter voltage spectrum with different modulation index

2.3.2 Line-frequency-switched pulse inverter

It was mentioned in the previous section that the PWM-controlled inverters are uneconomical for the transmission level application due to the high converter losses. The type of the inverter that suits for the transmission level application must have two basic following characteristics:

1- Low switching frequency (low converter losses)

2- High quality voltage at Point of Common Coupling (PCC) (low Total Harmonic Distortion(THD))

With PWM-controlled inverters we could not have both of the mentioned characteristics at the same time. To decrease the voltage THD at PCC we had to increase the switching frequency that lead to high converter loses. There is another type of the inverter that perfectly meets the mentioned transmission level requirements. The line –frequency-switched pulse inverters synthesize a very high quality voltage at their output terminals with switching frequency as low as the line frequency.24, and 48-pulse inverters are commonly used in the FACTS devices. A group of Neutral Point Clamped (NPC) inverters are electromagnetically coupled using transformers to synthetize the high quality output voltage. The inverter output voltage magnitude is changed indirectly by changing the DC-link voltage level.

This part of the thesis precisely analyses a 48-pulse inverter model which is developed based on the New York Power Authority (NYPA) Convertible Static Synchronous

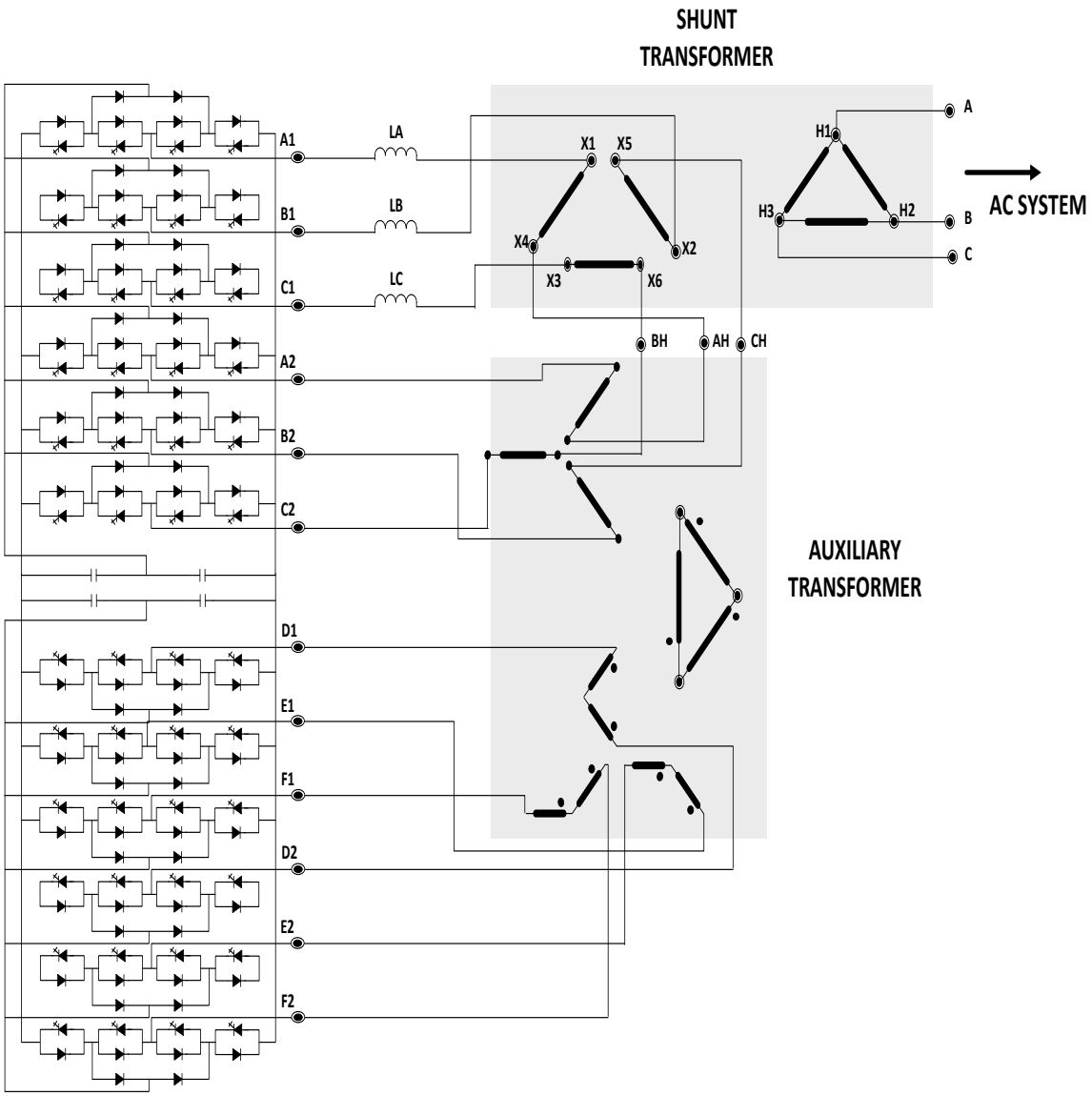


Figure 2-9. Power circuit of the NYPA three-level NPC 48-pulse inverter[30].

Compensator (CSC) at the Marcy substation. This inverter has been used in different chapter of the thesis. The entire angle controlled STATCOM simulation and experimental results throughout the thesis are based on this 48-pulse inverter. The UPFC model used in the last chapter of the thesis is also based on this inverter.

Figure 2-9 indicates the power circuit of the 48-pulse inverter. The VSC consists of 4 three level Neutral Point Clamped (NPC) three phase inverters (A1, B1, C1), (A2, B2, C2), (D1, E1, F1), and (D2, E2, F2). Their square wave outputs are combined electromagnetically to generate a 48-pulse output voltage waveform and their DC sides are connected to a common DC-bus. The output voltages of the three level NPC poles are combined through auxiliary and shunt transformers. The primary winding of the auxiliary transformer is doubly fed open wye winding with 11.9 kV rated voltage across the winding. The secondary winding is doubly fed open zigzag winding with the same voltage rating as the primary winding i.e. 11.9 kV. The voltage across the secondary leads the primary by 30 degree. The shunt transformer aids in voltage waveform construction and serves to couple the synthesized voltage to the 345 kV transmission system. The shunt transformer has standard delta connected primary windings rated 345 kV, and open delta secondary windings rated 21.4 kV across the winding [30].The AC-system zero-sequence current, in case of ground faults in the AC-system, is filtered out by the primary winding delta connection. Therefore, the AC-system zero-sequence current does not flow on the STATCOM tie line. The detailed voltage harmonic analysis of this inverter is presented in appendix 2-A of this chapter. Figure 2-10 presents the line to line output voltage of the 48-pulse inverter simulated in the PSCAD /EMTDC. To obtain this results, the DC-side of the inverter is connected into two series connected 6 kV DC-voltage sources and the AC-side is left open circuit.

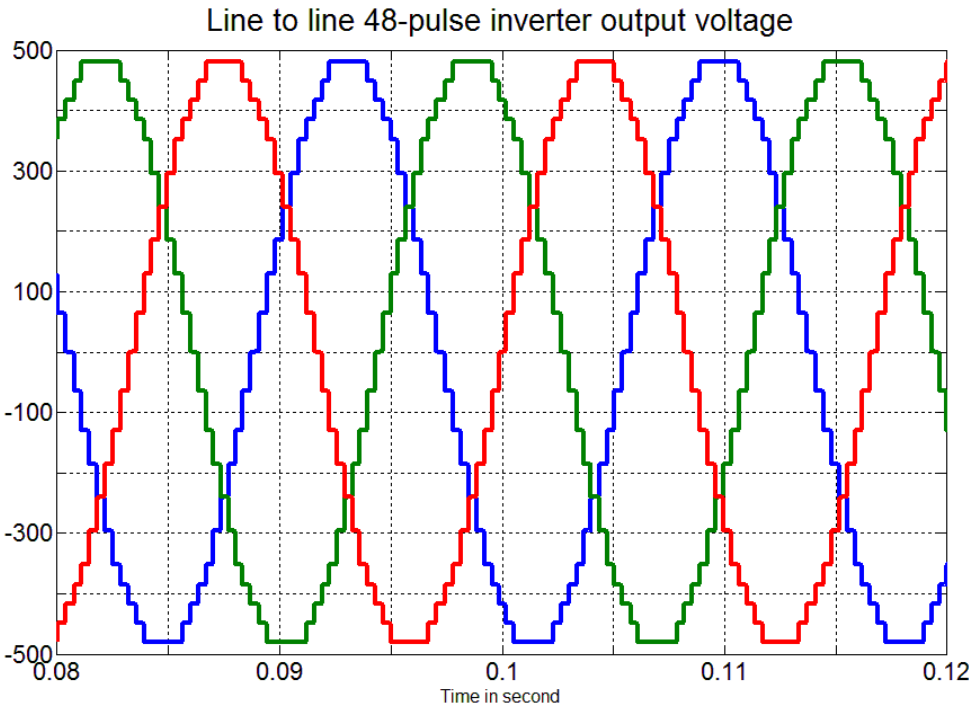


Figure 2-10. 48-pulse inverter line to line output voltages

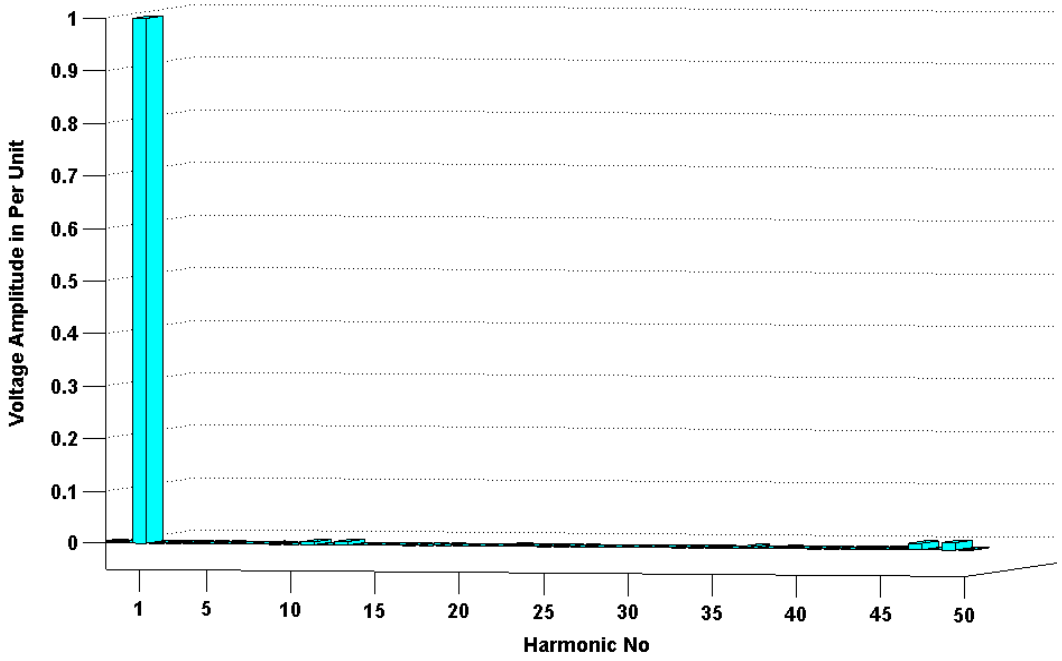


Figure 2-11. 48-pulse inverter output voltage harmonic content

Figure 2-11 indicates the harmonic content of the 48-pulse inverter output voltage. As it can be seen in this figure the quality of the output voltage is very high and there is not any considerable high or low order harmonics rather than the fundamental frequency. The output voltage THD is 3%.

2.3.2.1 PSCAD/ EMTDC simulation results of the angle-controlled STATCOM

In this part of the thesis the 48-pulse inverter has been modeled in the PSCAD/EMTDC platform and has been controlled with angle control structure to have the STATCOM functionality. This STATCOM has been connected to the reduced order 3-bus AC-system model of the NYPA power system as shown in Figure 2-12. All the per unit values are based on 100 MVA, and 345 kV base system.

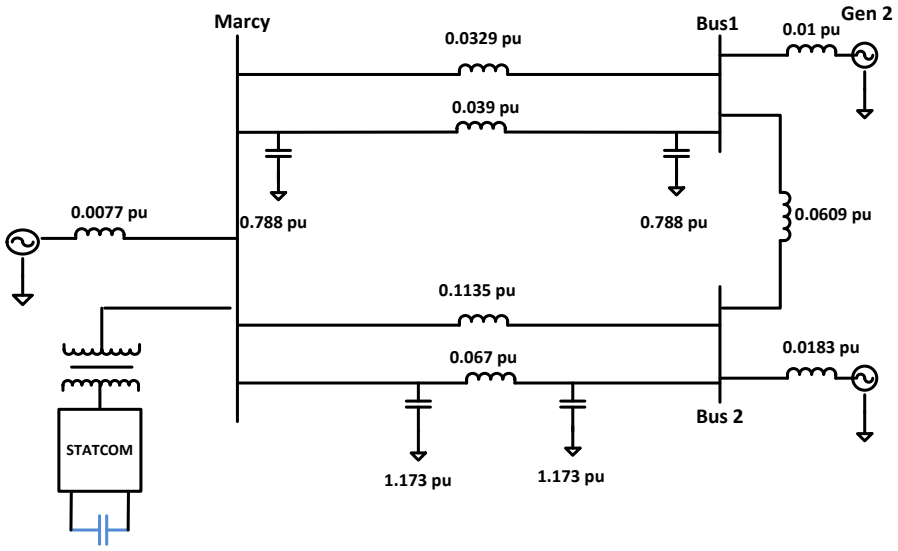


Figure 2-12. The angle-controlled STATCOM connected to the NYPA 3-bus AC system. Per unit values are based on 345kV, and 100 MVA.

Results in Figure 2-13 illustrate the STATCOM performance under different control command. Initially STATCOM works in the inductive mode of operation and absorbs 1 pu (167.347 A equivalent to 100 MVA reactive power) of inductive current form the grid. The reference of iq is set to be zero at around t=0.21 seconds and finally at around t=0.32 seconds it starts to work in capacitive mode of operation and injects 1 pu of capacitive current to the grid. As can be seen in this figure the reactive current follows its reference value quickly and smoothly. It is also important to note that the DC-link voltage value is not fixed and changes over the range of the values. That is due to the reason that the angle controller changes the inverter output voltage indirectly by changing the DC-link voltage level.

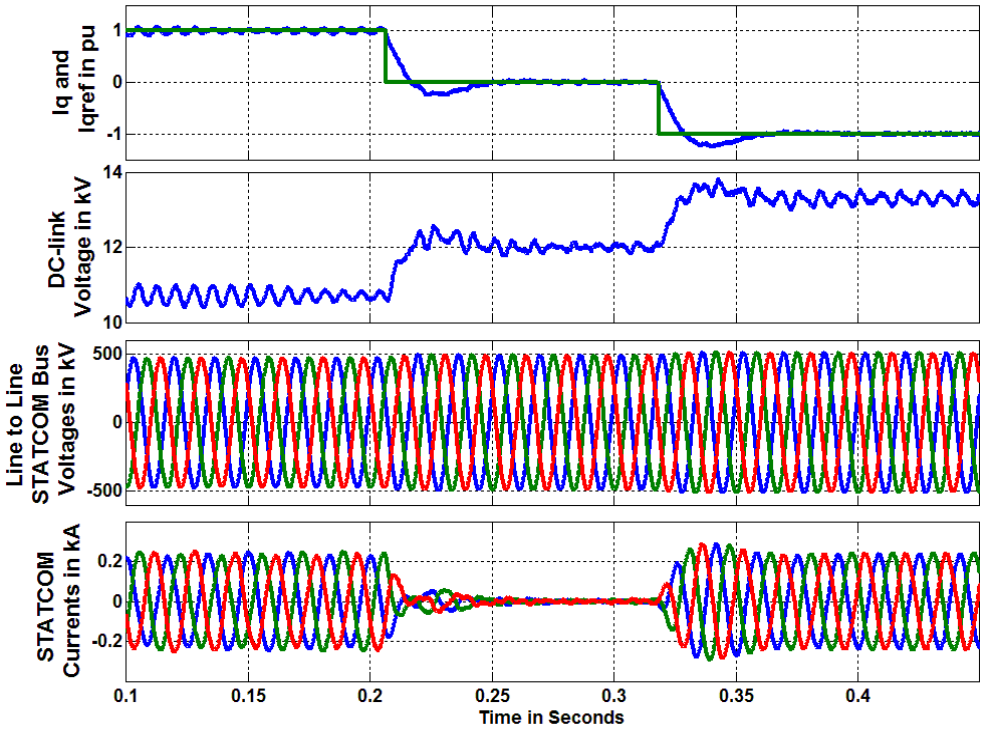


Figure 2-13. 48-pulse angle-controlled STATCOM performance with different current references. Per unit values are based on 345kV, and 100 MVA.

2.3.2.2 Real Time Digital Simulation (RTDS) results of the angle-controlled STATCOM

The 48-pulse inverter along with the angle controller has been implements in the RTDS platform. Four GPC processor cards plus two PB5 cards have been used to simulate the entire angle-controlled STATCOM along with the 3-bus AC-system. 48 GTO valves are distributed between two small time step bridge boxes. Small time step bridge box is designed for the power electronics simulations and all the components inside the bridge boxes are ran with small time step (very fast). The number of the small time component that can be placed inside a bridge box cannot exceed a specific number (this number varies depending on the processor usage of each component). In our case for simulation of the 4 NPC inverters and auxiliary and shunt transformers 3 bridge boxes have been used. The 3-bus AC system has been simulated in the large time step. Bridge boxes must be connected to each other using the transmission line or transformer model. The small time step part of the simulation is also being connected to the large time step part using a transmission line. These transmission lines do not exist in the real model and although their impedance have been set to the minimum possible value, but they affect the simulation results. The other constraint in our RTDS simulation was that using too many small time step components dramatically increases the minimum possible time step. In our case it was not possible to lower the time step below the 70 μs.

Figure 2-14 shows the RTDS racks at North Carolina State University. The processor usage of the rack 1 and 2 are shown in Figure 2-15.

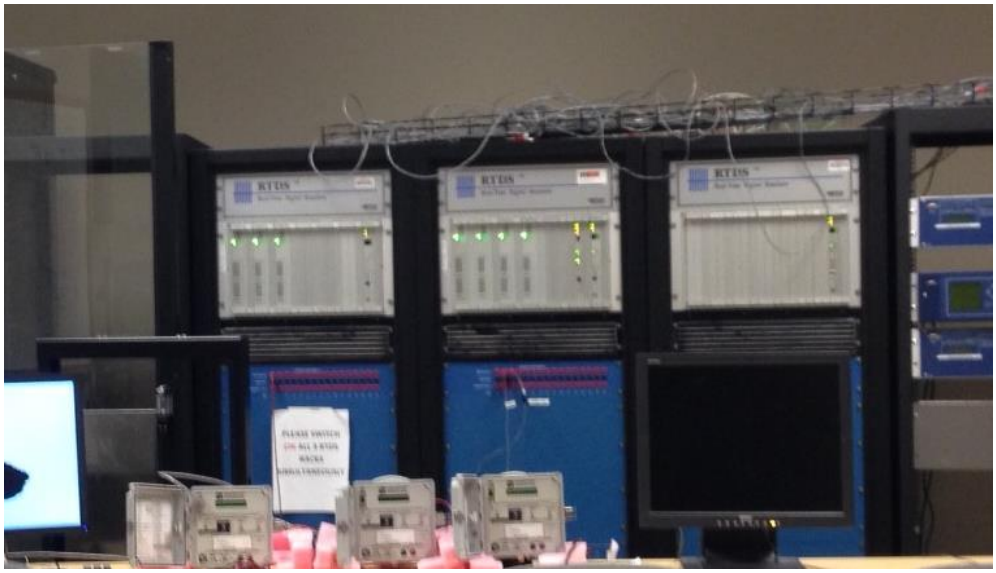


Figure 2-14. RTDS Racks at NCSU

(a) (b)

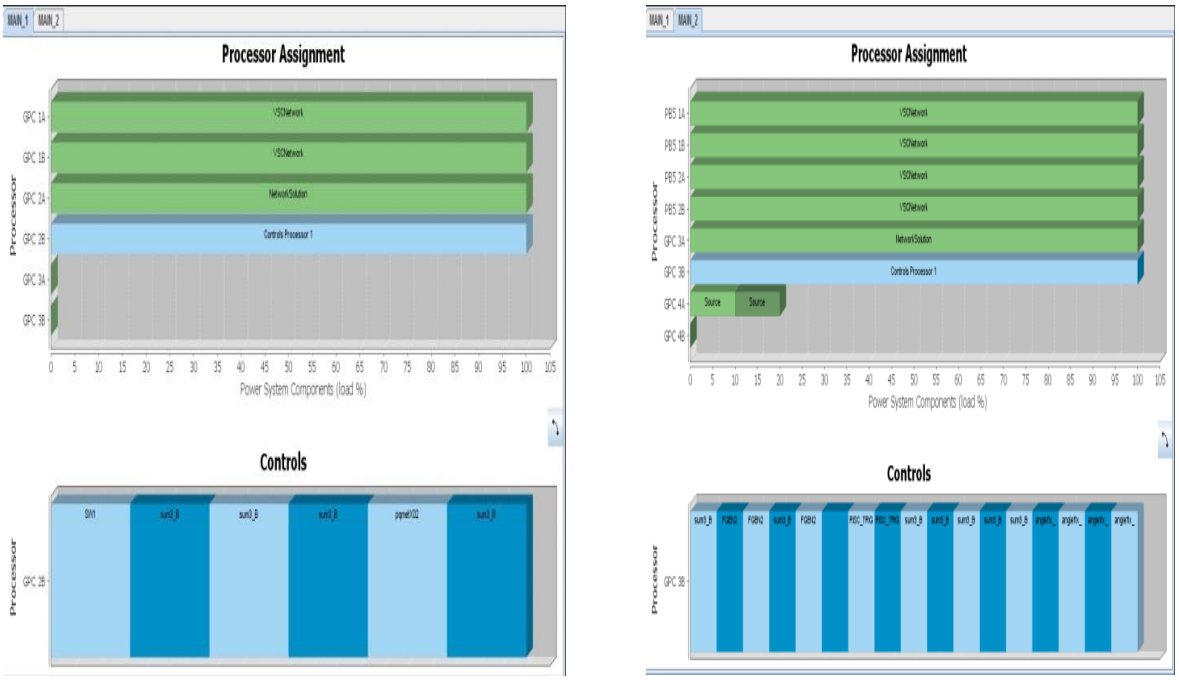


Figure 2-15. Rack 1 (column (a)), and 2 (column (b)) processor usage for the angle-controlled STATCOM simulation

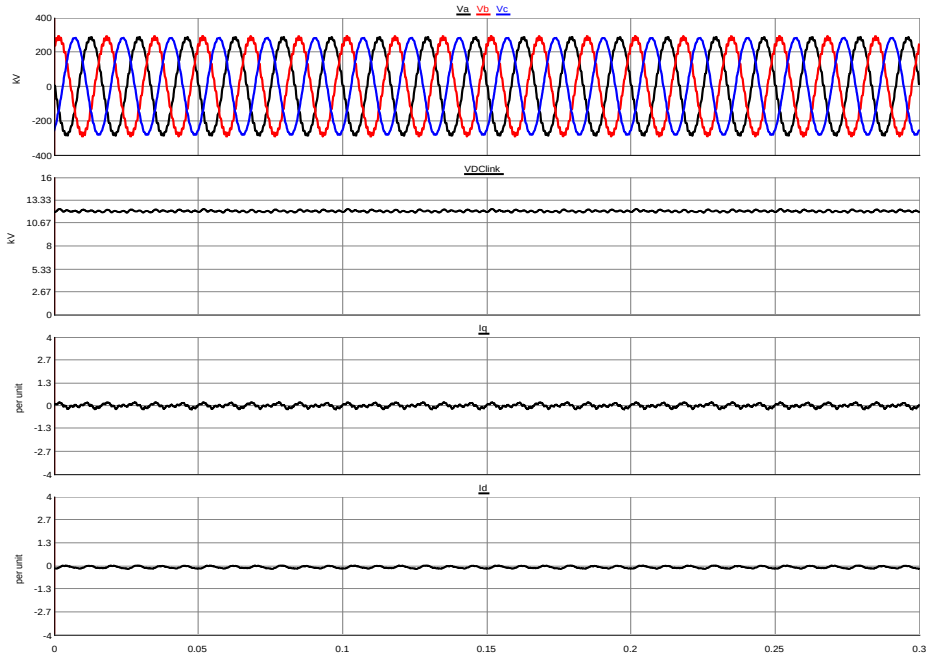


Figure 2-16. Angle-controlled STATCOM performance with iq=0

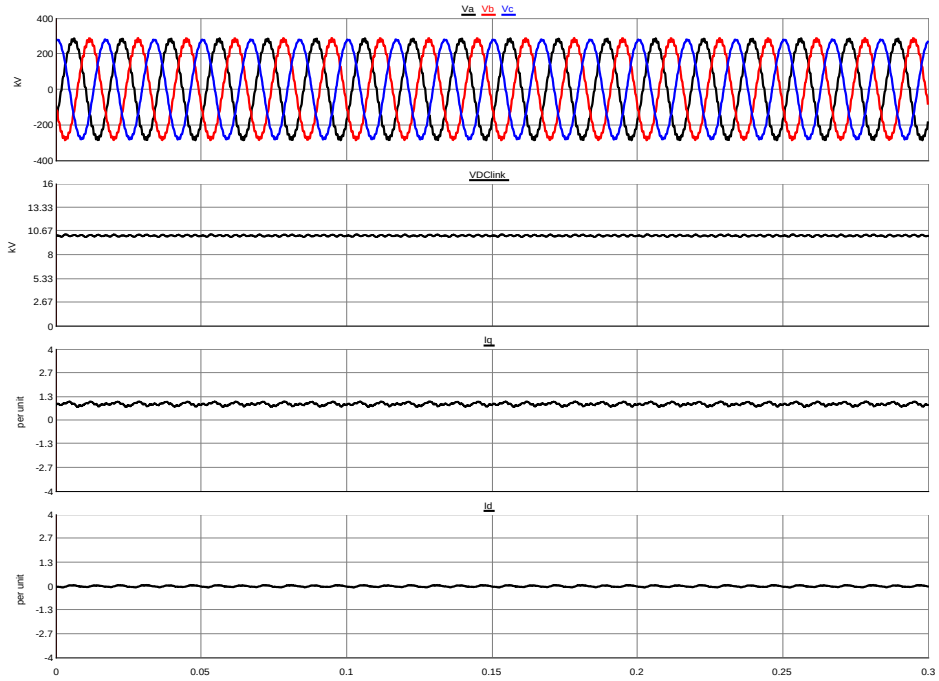


Figure 2-17. Angle-controlled STATCOM performance with iq=1 pu inductive

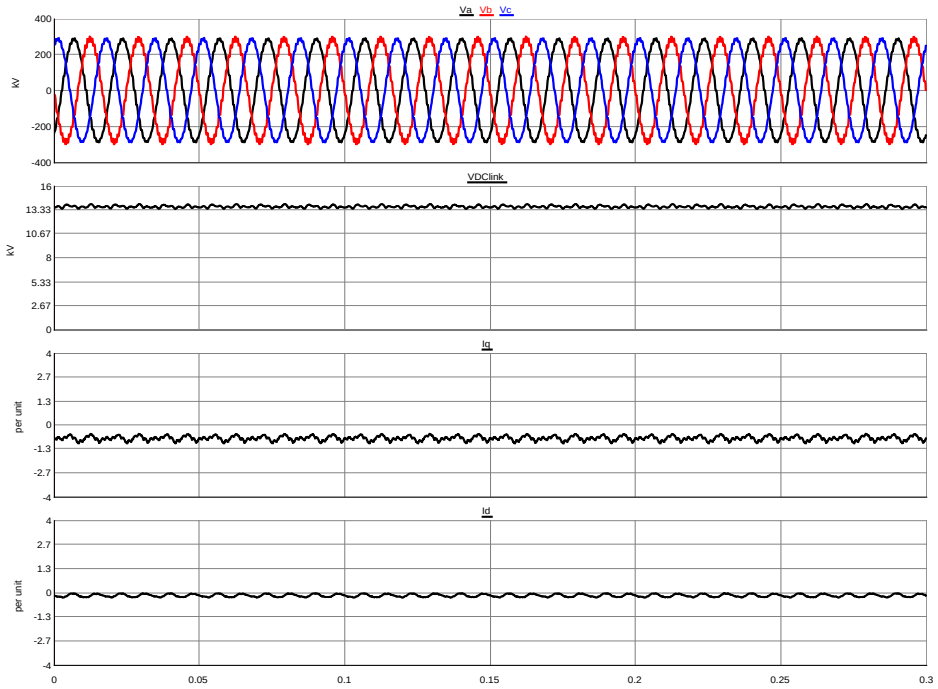


Figure 2-18. Angle-controlled STATCOM performance with iq=-1 pu capacitive

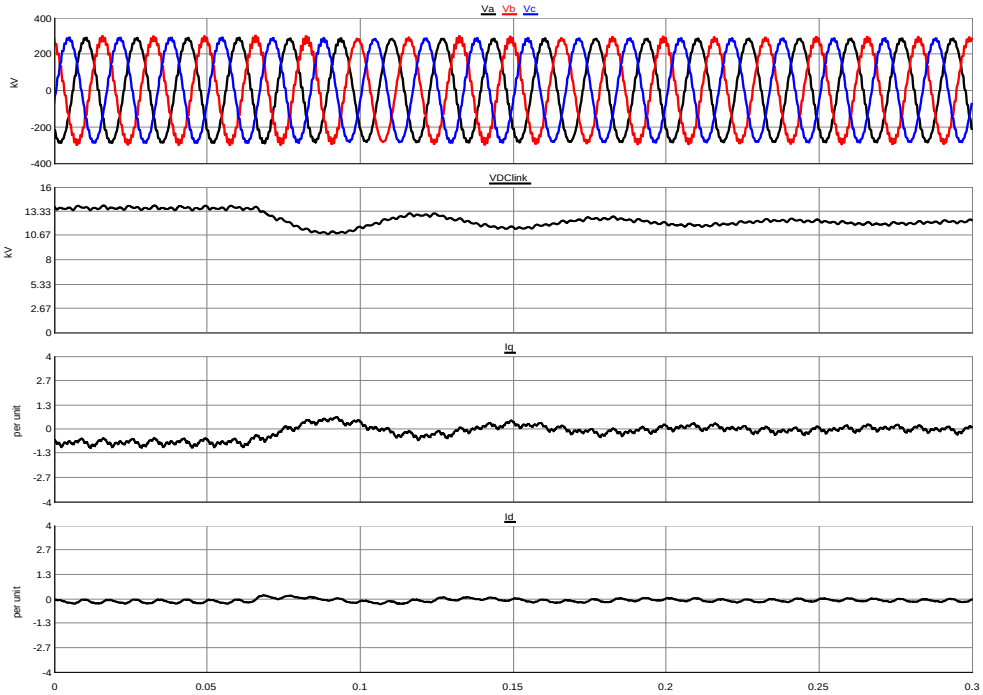


Figure 2-19. Angle-controller performance in transition from capacitive (iq=-1 pu) to zero current

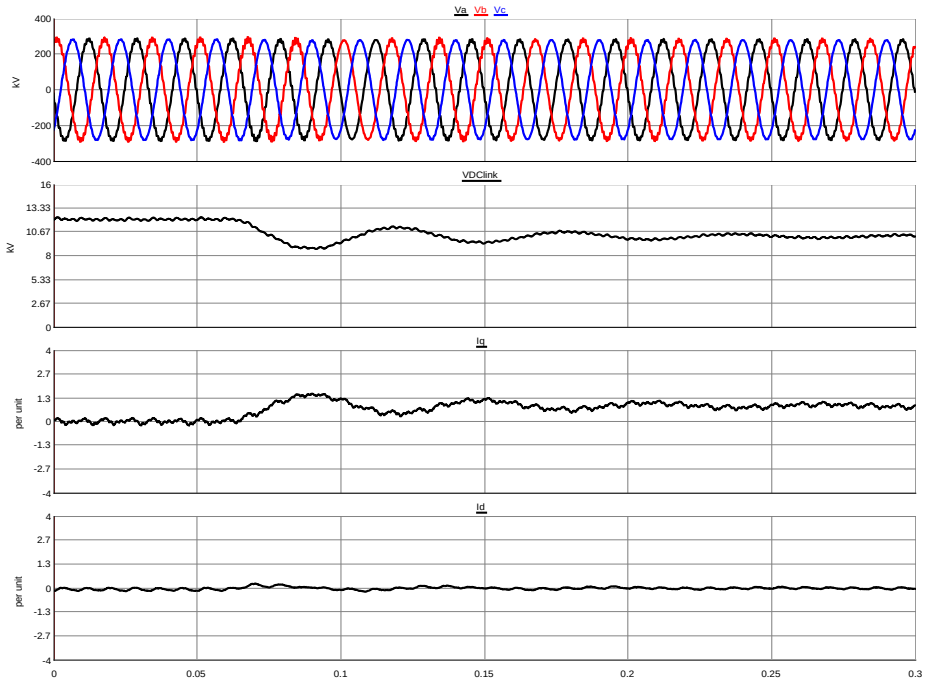


Figure 2-20. Angle-controlled STATCOM performance in transition from zero current to fully inductive (iq=1pu)

Results in Figure 2-16, Figure 2-17, and Figure 2-18 indicate the steady-state STATCOM performance under different control commands i.e. different iq reference values. Waveforms of Figure 2-16 are associated with STATCOM performance when the iq is set to zero. The results in Figure 2-17, and Figure 2-18 illustrate the STATCOM performance in fully inductive (iq=1 pu), and fully capacitive (iq=-1pu) respectively. Results in Figure 2-19, and Figure 2-20 show the STATCOM transition from fully capacitive to zero current and from zero current to fully inductive respectively. As can be seen in these figures the STATCOM response time is longer that the PSCAD simulation. This is due the mentioned constraints in the RTDS.

2.3.2.3 Transient Network Analyzer (TNA) Results of the Angle-Controlled STATCOM

TNA is a scaled analogue equivalent model of the actual transformers, switches and inverter equipment connected to the Convertible Static Compensator (CSC) at Marcy substation in the state of the New York. Two VSCs are connected to the AC-system through shunt and series transformers. This arrangement of the converters allows STATCOM, SSSC, UPFC, or Interline Power Flow Controller (IPFC) deployment at the bus and two of the lines exiting the substation. The operation of the STATCOMs and shunt converter in the UPFC mode is based on angle-controller strategy [30]. The TNA control system is exactly the same as the controller that is installed at the Marcy substation. To provide an overall view of the testing system, the interface of the inverters to the controllers and its connection to the AC-system is shown conceptually in Figure 2-21. Figure 2-22 shows the AC-system panels that in fact is a scaled down equivalent model of the NYPA 3-bus AC system. The capacitors and inductors value are also shown in this figure. The entire power circuit of the Marcy CSC has been scaled down and replicated in the TNA system. The nominal inverter rating of 100 MVA is scaled to 12 VA and the nominal system voltage of 345 kV is scaled to 100 V RMS (L-L). The magnetics, the substation bus structure, and transmission line impedances at the Marcy substation have also been similarly replicated using scaled down hardware components.

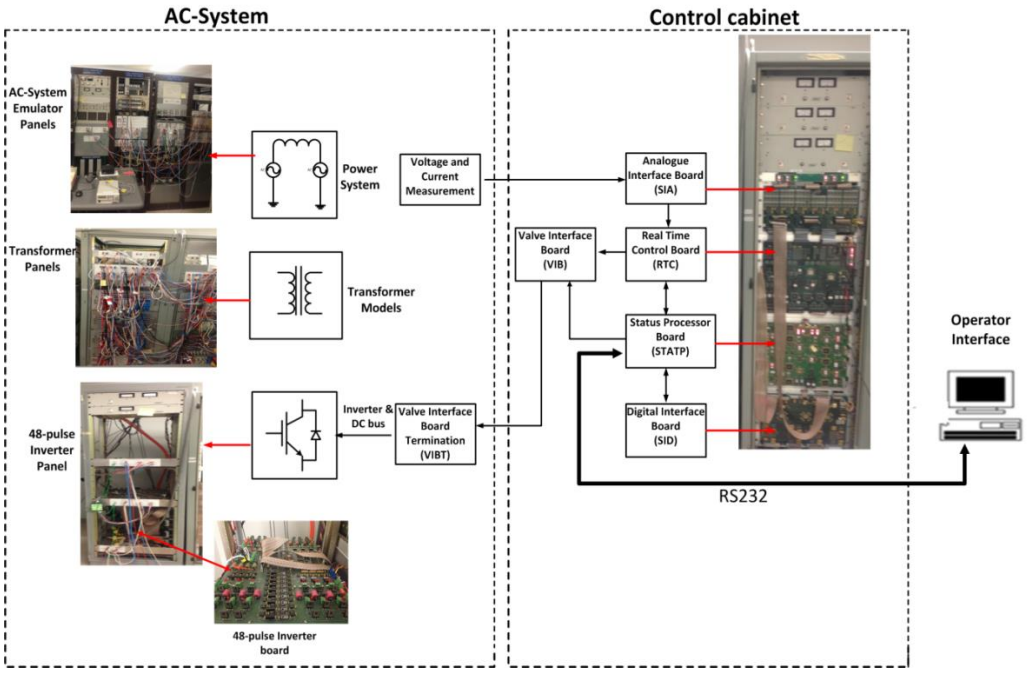
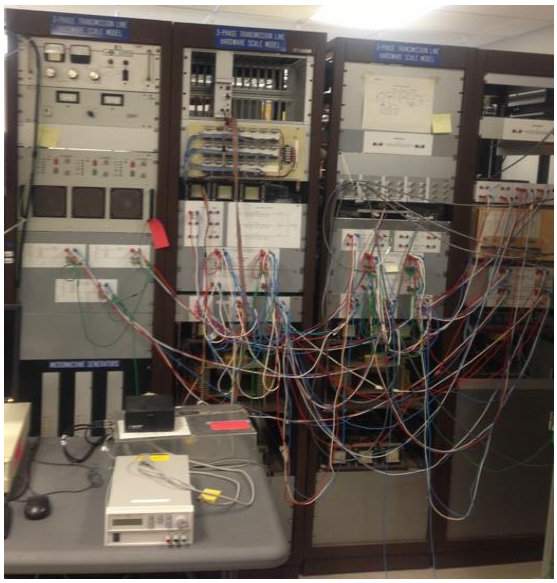
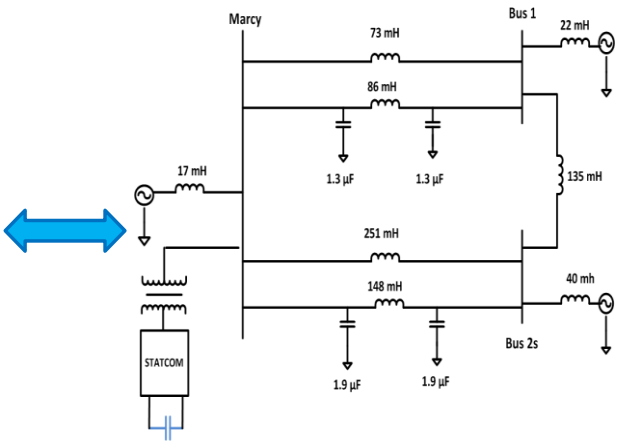


Figure 2-21. Interface of Control equipment to TNA

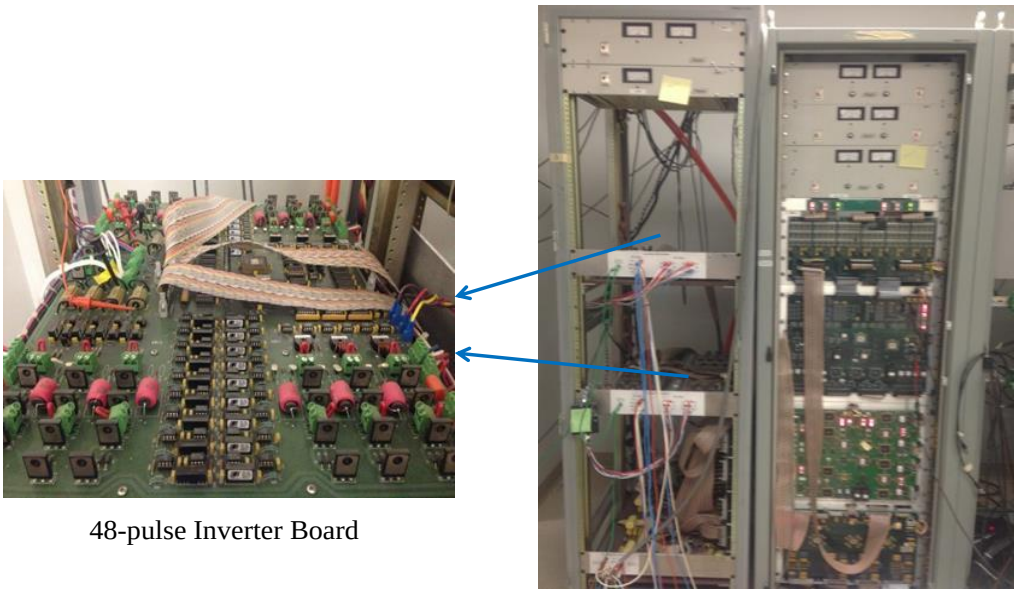


AC-system panels



Scaled-down NYPA 3-bus AC-system model

Figure 2-22. Scaled down model of the NYPA 3-bus AC system used for experimental verification



48-pulse Inverter Board

Inverter and Control Panel

Figure 2-23. Inverter and control panels

Figure 2-23 shows the inverter and control panels of the TNA. Inverter panel consists of two 48-pulse inverters. The 48-pulse inverter board shown in Figure 2-23 is the scaled model of the inverter used in the RSCAD, and PSCAD simulation which was built based on the NYPA 48-pulse inverter.

The TNA is controlled by a software package called Genesis made by Iconics, which features a specialized database and custom designed graphical displays to convey the equipment status and receive operator input. Through these displays the operator may start and stop the equipment, change equipment configuration, change equipment operating mode or set points, and access both summary and detailed status and diagnostic information.

The operator would use the One Line Diagram Screen to verify the AC-system switch position prior to start up. The One-Line Diagram screen shown in Figure 2-24 is a single line

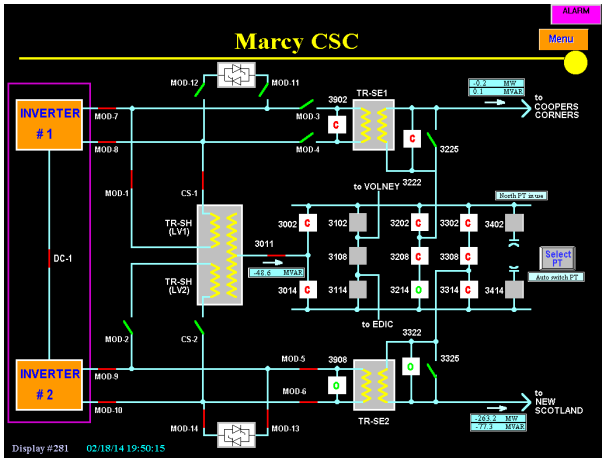


Figure 2-24. One-Line Diagram Screen

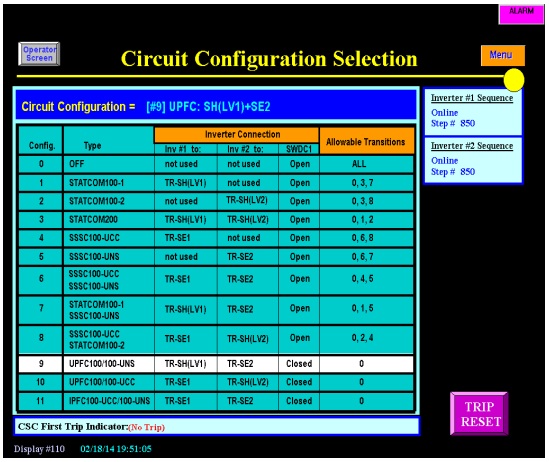


Figure 2-25. Circuit Configuration Selection

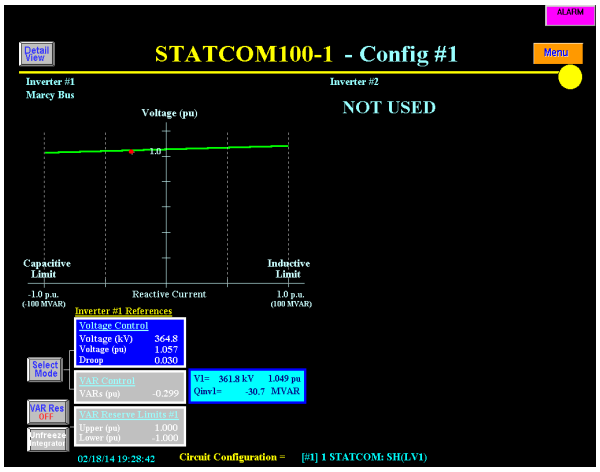


Figure 2-26. Operator Control Screen for STATCOM

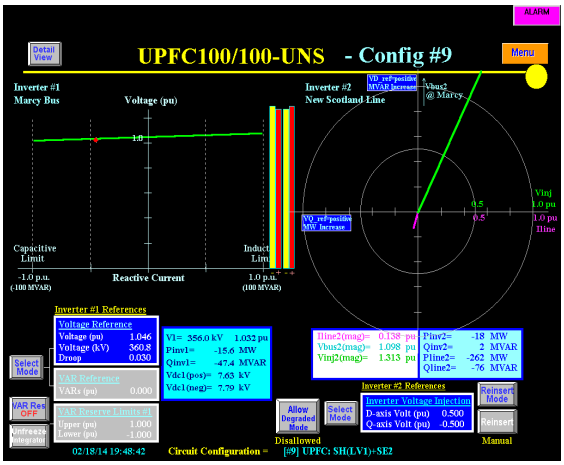


Figure 2-27. Operator Control Screen for UPFC

diagram of the CSC connections to the 3-bus AC-system. From this display, an operator can visually ascertain the status of the breakers and switches. The Circuit Configuration Selection screen shown in Figure 2-25 allows the operator to select a new circuit configuration, which causes the control system to start up or shut down one or both inverters as needed. Figure 2-26 and Figure 2-27 show the operation screen in STATCOM and UPFC mode respectively.

The STATCOM mode operation of the TNA has been analyzed here. The emphasize has been given to the STATCOM mode because later in this thesis a new control structure has been proposed to improve the angle-controlled STATCOM performance under AC-system faults and the TNA has been used to verify the controller performance. The TNA inverter 1 is set to work in the STATCOM mode and the inverter 2 is left idle. Figure 2-28 indicates the STATCOM transition from inductive mode to the capacitive mode. Initially it works in the inductive mode and absorbs Iq=0.6 inductive current from the grid. The STATCOM is commended to work in the capacitive mode and inject Iq=-0.7 pu to the grid then. As cane be seen in this figure, the DC-link voltage increases and the STATCOM smoothly and quickly reaches to the steady state capacitive mode. Results in Figure 2-29, and Figure 2-30 illustrate the STATCOM transition from inductive to the zero current and zero current to the capacitive mode respectively.

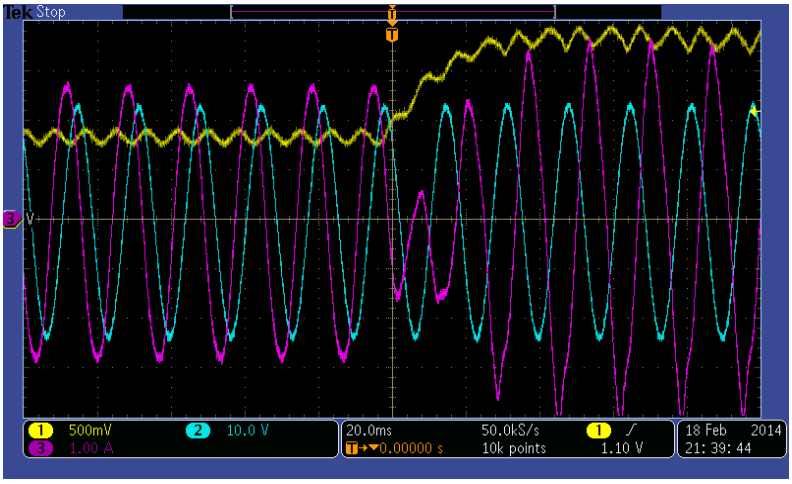


Figure 2-28. STATCOM transition from inductive mode Iq=0.6 pu to capacitive mode Iq=-0.7 pu

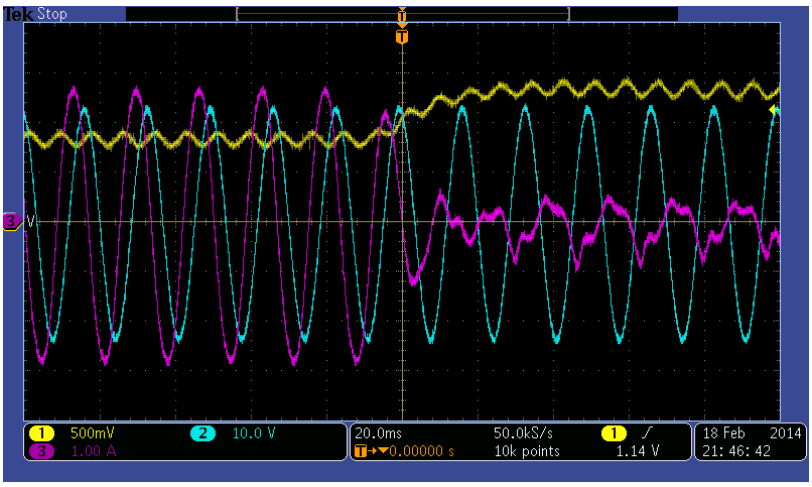


Figure 2-29. The STATCOM transition from inductive mode Iq=0.6 pu to zeroe current Iq=0

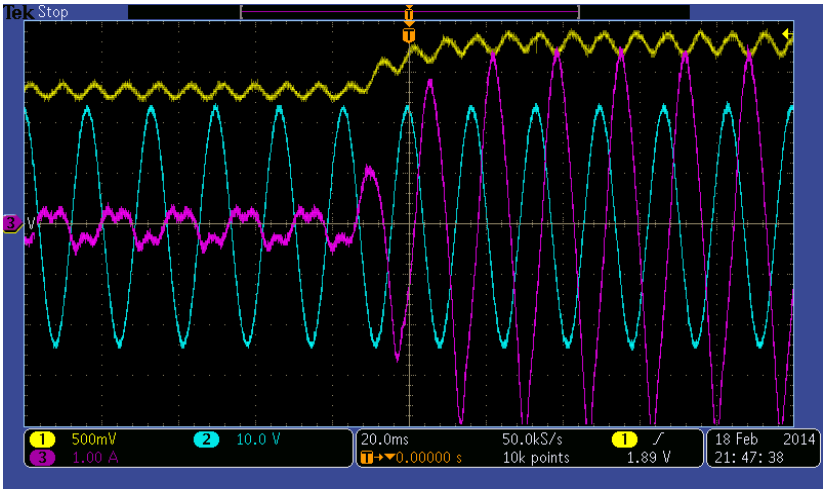


Figure 2-30. The STATCOM transition from zero current Iq=0 pu to capacitive mode Iq=-0.7

APPENDIX

2. 4 Appendix (2-A)

The voltage spectrum of the three-level NPC inverter output voltage of Figure 2-31 is calculated as:

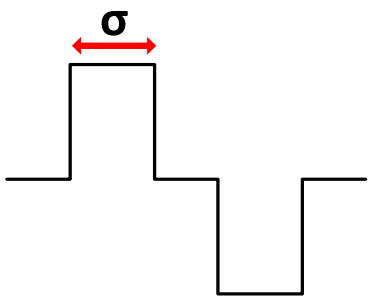


Figure 2-31. NPC converter output voltage

$$v_{an} = \frac{2Vdc}{n \times \pi} \cos\left(\frac{n(\pi - \sigma)}{2}\right) = \pm \frac{2Vdc}{n \times \pi} \sin(\frac{n(\sigma)}{2}) \quad (2\text{-}39)$$

In this equation n denotes the number of the harmonic. The (+) sign applies when $n = 4k + 1$ while negative (-) applies when $n = 4k + 3$. Note should be taken that in the voltage spectrum those harmonics that $n = 3k + 1$ are positive sequence and those that $n = 3k + 2$ are negative sequence.

Expanding (2-39) yields:

$$v_{an} = \frac{2Vdc}{\pi}[\sin\left(\frac{\sigma}{2}\right)\ \sin wt - \frac{1}{3}\sin\left(\frac{3\sigma}{2}\right)\ \sin 3wt + \frac{1}{5}\sin\left(\frac{5\sigma}{2}\right)\ \sin 5wt - \frac{1}{7}\sin\left(\frac{7\sigma}{2}\right)\ \sin 7wt + \frac{1}{9}\sin\left(\frac{9\sigma}{2}\right)\ \sin 9wt - \frac{1}{11}\sin\left(\frac{11\sigma}{2}\right)\ \sin 11wt + \frac{1}{13}\sin\left(\frac{13\sigma}{2}\right)\ \sin 13wt\ - \frac{1}{15}\sin\left(\frac{15\sigma}{2}\right)\ \sin 15wt + \frac{1}{17}\sin\left(\frac{17\sigma}{2}\right)\ \sin 17wt - \cdots] \quad (2\text{-}40)$$

Therefore, the line to line voltage will be:

$$\frac{2Vdc\sqrt{3}}{\pi}[\sin\left(\frac{\sigma}{2}\right)\ \sin(wt+30) + \frac{1}{5}\sin\left(\frac{5\sigma}{2}\right)\ \sin(5wt+150) + \frac{1}{7}\sin\left(\frac{7\sigma}{2}\right)\ \sin(7wt+30) + + \frac{1}{11}\sin\left(\frac{11\sigma}{2}\right)\ \sin(11wt+150) + \frac{1}{13}\sin\left(\frac{13\sigma}{2}\right)\ \sin(13wt+30)\ + \frac{1}{17}\sin\left(\frac{17\sigma}{2}\right)\ \sin(17wt+150) + \frac{1}{19}\sin\left(\frac{19\sigma}{2}\right)\ \sin(19wt+30) + \frac{1}{23}\sin\left(\frac{23\sigma}{2}\right)\ \sin(23wt+150) + \frac{1}{25}\sin\left(\frac{25\sigma}{2}\right)\ \sin(25wt+30) + \frac{1}{29}\sin\left(\frac{29\sigma}{2}\right)\ \sin(29wtl+150) + \frac{1}{31}\sin\left(\frac{31\sigma}{2}\right)\ \sin(31wt+30) + \frac{1}{35}\sin\left(\frac{35\sigma}{2}\right)\ \sin(35wt+150) + \frac{1}{37}\sin\left(\frac{37\sigma}{2}\right)\ \sin(37wt+30) + \frac{1}{41}\sin\left(\frac{41\sigma}{2}\right)\ \sin(41wt+150) + \frac{1}{43}\sin\left(\frac{43\sigma}{2}\right)\ \sin(43wt+30) + \frac{1}{47}\sin\left(\frac{47\sigma}{2}\right)\ \sin(47wt+150) + \frac{1}{49}\sin\left(\frac{49\sigma}{2}\right)\ \sin(49wt+30) + \cdots] \quad (2\text{-}41)$$

Table 2-1 to 2-4 indicate how the initial angle of every single harmonic of all four NPC converters of the 48-pulse inverter are being shifted by the gate driver and also auxiliary and shunt transformers. Figure 2-32 illustrates the summation of the all the harmonics of 4 NPC output voltages. It is shown that most of the harmonics are being eliminated. The harmonics 23rd, and 25th are being eliminated by setting the zero angle of the NPC converters to 3.75˚.

Table 2-1. Converter 1 output voltage phase shifting

Harmonic No	Initial Angle	Leading 7.5˚ by gate driver
1	30	37.5
5	150	187.5
7	30	82.5
11	150	232.5
13	30	127.5
17	150	277.5
19	30	172.5
23	150	322.5
25	30	217.5
29	150	7.5
31	30	262.5
35	150	52.5
37	30	307.5
41	150	97.5
43	30	352.5
47	150	142.5
49	30	37.5

Table 2-2. Converter 2 output voltage phase shifting

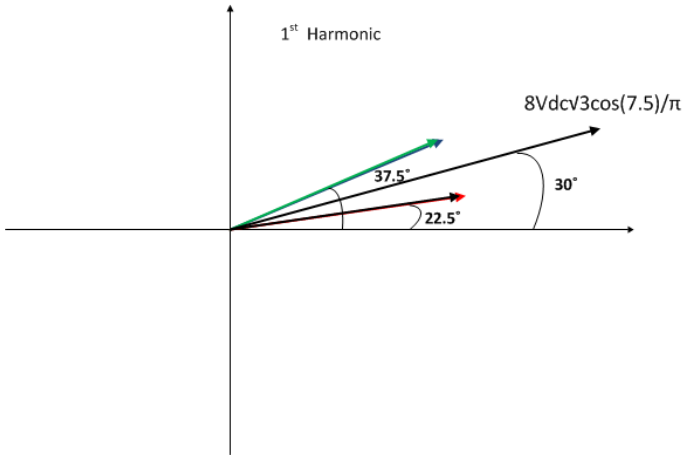
Harmonic No	Initial Angle	Leading 172.5˚ by gate driver	Shift 180˚ using transformer
1	30	202.5	22.5
5	150	1012.5	112.5
7	30	1237.5	337.5
11	150	2047.5	67.5
13	30	2272.5	292.5
17	150	3082.5	22.5
19	30	3307.5	247.5
23	150	4117.5	337.5
25	30	4342.5	202.5
29	150	5152.5	292.5
31	30	5377.5	157.5
35	150	6187.5	247.5
37	30	6412.5	112.5
41	150	7222.5	202.5
43	30	7447.5	67.5
47	150	8257.5	157.5
49	30	8482.5	22.5

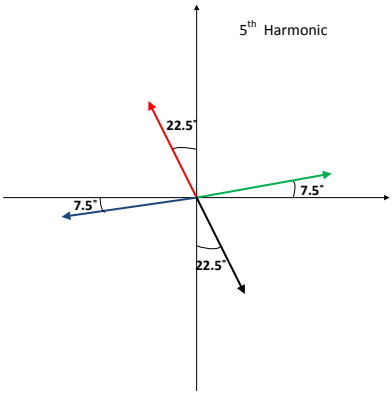
Table 2-3. Converter 3 output voltage phase shifting

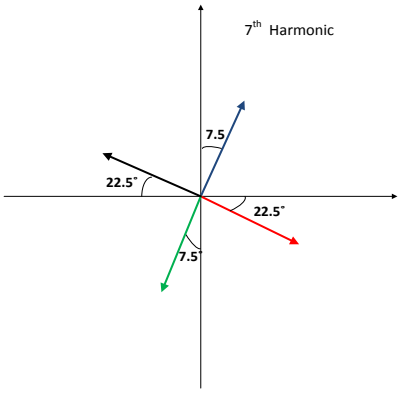
Harmonic No	Initial Angle	Leading 37.5˚ by gate driver	Lagging 30˚ using Aux. transformer
1	30	67.5	37.5
5	150	337.5	7.5
7	30	292.5	262.5
11	150	562.5	232.5
13	30	517.5	127.5
17	150	787.5	97.5
19	30	742.5	352.5
23	150	1012.5	322.5
25	30	967.5	217.5
29	150	1237.5	187.5
31	30	1192.5	82.5
35	150	1462.5	52.5
37	30	1417.5	307.5
41	150	1687.5	277.5
43	30	1642.5	172.5
47	150	1912.5	142.5
49	30	1867.5	37.5

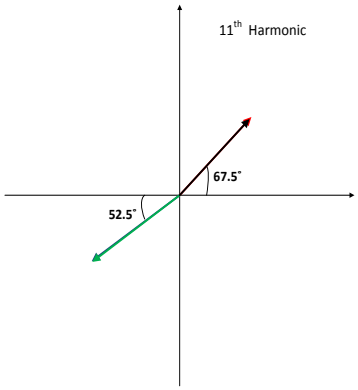
Table 2-4. Converter 4 output voltage phase shifting

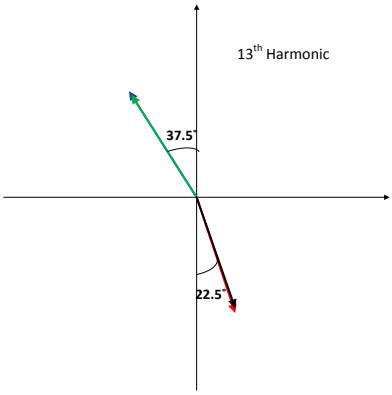
Harmonic No	Initial Angle	Leading 202.5˚ by gate driver	shifting 180˚ using Aux. transformer	Lagging 30˚ using Aux. transformer
1	30	232.5	412.5	22.5
5	150	1162.5	1342.5	292.5
7	30	1447.5	1627.5	157.5
11	150	2377.5	2557.5	67.5
13	30	2662.5	2842.5	292.5
17	150	3592.5	3772.5	202.5
19	30	3877.5	4057.5	67.5
23	150	4807.5	4987.5	337.5
25	30	5092.5	5272.5	202.5
29	150	6022.5	6202.5	112.5
31	30	6307.5	6487.5	337.5
35	150	7237.5	7417.5	247.5
37	30	7522.5	7702.5	112.5
41	150	8452.5	8632.5	22.5
43	30	8737.5	8917.5	247.5
47	150	9667.5	9847.5	157.5
49	30	9952.5	10132.5	22.5

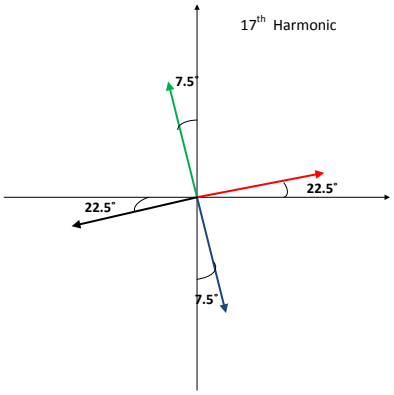

1st Harmonic
8Vdc√3cos(7.5)/π
37.5˚
30˚
22.5˚

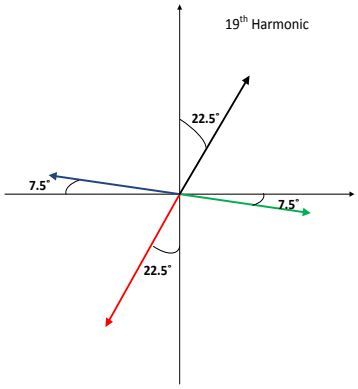

5th Harmonic
22.5˚
7.5˚
7.5˚
22.5˚


7th Harmonic
7.5
22.5˚
22.5˚
7.5˚


11th Harmonic
67.5˚
52.5˚


13th Harmonic
37.5˚
22.5˚


17th Harmonic
7.5˚
22.5˚
22.5˚
7.5˚


19th Harmonic
22.5˚
7.5˚
7.5˚
22.5˚

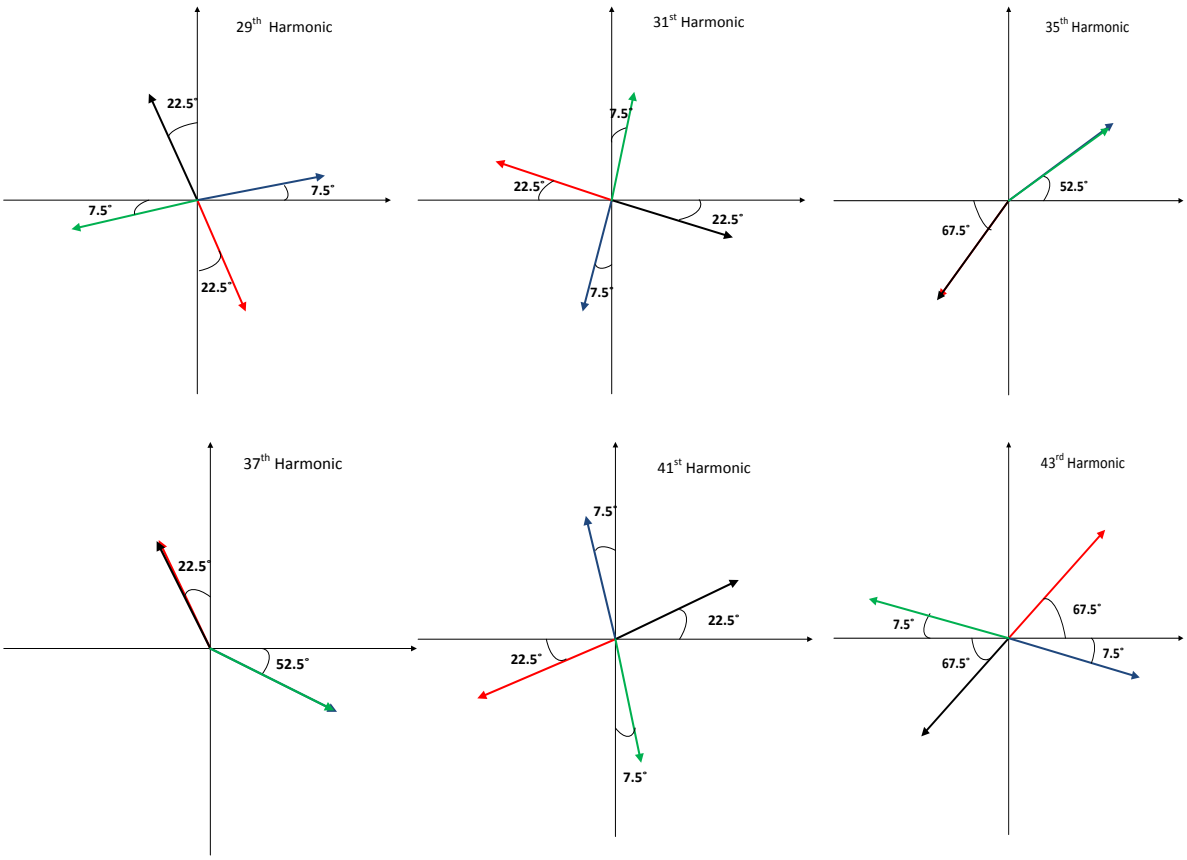


Figure 2-32. illustrative harmonic elimination of the 48-pulse inverter using the gate drive phase shift and also auxiliary and shunt transformers phase shifting. All the harmonics up to the 49th are illustrated. Blue, red, green, and black represent the NPC converter 1, 2, 3, and 4 respectively.

Chapter3: Dual Angle Control for Line-Frequency-Switched Static Synchronous Compensators under System Faults

3. 1 Introduction

The possibility of generating or absorbing controllable reactive power with various power electronics switching converters has long been recognized [19]-[30] . The VSC-based STATCOM is used for voltage regulation in transmission and distribution systems. Unlike the PWM-controlled STATCOMs, *Angle-controlled* STATCOMs are switched at line frequency to achieve lower system losses. In recent years, *angle-controlled* STATCOMs have been deployed by utility owners for the purpose of voltage regulation, voltage stability improvement and increasing operational functionality. The first such installation was ±100 MVAr STATCOM at TVA Sullivan substation [34]. This was followed by the New York Power Authority (NYPA) installation of a FACTS controller, known as the Convertible Static Compensator (CSC), at the Marcy 345 kV substation in New York State. Two 100 MVA VSCs are connected to the system through shunt and series transformers. This arrangement of the converters allows STATCOM, SSSC, UPFC, or IPFC deployment at the bus and two of the lines exiting the substation. The operation of the STATCOMs and shunt converter in the UPFC mode is based on *angle-controller* strategy [30], [35]. 150 MVA STATCOM at Laredo and Brownsville substation at Texas, 160 MVA STATCOM at Inez substation in Eastern Kentucky, 43 MVA PG&E Santa Cruz STATCOM, and 40 MVA KEPCO (Korea Electric Power Corporation) STATCOM at Kangjin substation in South Korea are few examples of the other *Angle-controlled* STATCOMs.

Despite the superior feature on voltage waveform quality and efficiency, the practical *angle-controlled* STATCOMs suffer from the over-current (and trips) and possible saturation of the interfacing transformers caused by negative sequence current during unbalanced conditions and faults, when the VAR support is needed the most. It is important to note that solutions proposed in the literature to improve the PWM based VSC performance under unbalanced conditions are not applicable to *angle-controlled* STATCOMs. *Angle-controlled* STATCOMs do not have the same degree of freedom as PWM-controlled STATCOM. The main motivation to use *Angle-controlled* STATCOM is to obtain higher waveform quality of voltage with lower losses compared to PWM VSC. This becomes especially important for utility application of large rated STATCOMs in the range of 100-150 MVA where standard PWM VSC for drives cannot be directly applied.

This chapter presents a new control structure for high power *angle-controlled* STATCOMs during normal and fault conditions. As discussed earlier, the only control input in the *angle-controlled* STATCOM is phase angle difference between VSC and AC bus instantaneous voltage vector (α) [19]. In the proposed controller, α is split into two parts, α_{dc} and α_{ac} .The DC part (α_{dc}) which is the conventional *angle-controller* output is in charge of controlling the positive sequence VSC output voltage. The oscillating part (α_{ac}) controls the DC-link voltage oscillations with twice the line frequency to generate required fundamental negative sequence voltages at the VSC output terminals to limit the negative sequence current. Since this control scheme uses two angles (α_{dc} and α_{ac}) as control inputs, it is called *Dual Angle Control (DAC)*. The Dual Angle Control stabilizes the STATCOM DC bus during power system faults, and therefore allows the STATCOM to continue operation

without tripping.

In this chapter, we address the issue of limiting the STATCOM negative sequence current, and thus the resulting DC-link voltage oscillations, in high-power *angle-controlled* STATCOMs, to enable the STATCOM to operate without tripping in the presence of power system faults and AC-system voltage unbalances. This is done by control action, which makes it unnecessary to constrain the design of STATCOM power components to achieve the same task. We give an analysis of STATCOM unbalanced operation, followed by a description of the proposed dual angle control method.

The analysis and performance of the STATCOM and the control method is supported by PSCAD/EMTDC simulation, and by experimental results. The experiments were done on a Transient Network Analyzer (TNA), which was used to study the STATCOM performance for the NYPA CSC 2×100 MVA installation at the Marcy substation. The description of the TNA was presented in the last chapter.

3. 2 Angle-controlled STATCOM under normal and system faults

3.2.1 Description of Conventional Angle-Controller Structure

The description of the angle-controlled STATCOM was presented in detail in the last chapter. To make this chapter self-sufficient a brief outline is also given in this chapter. All the VSCs, which are building block of FACTS devices, regardless of their topology can be divided into two types depending on their control methods. One type is vector controlled or PWM-based converter. The function of generating arbitrary voltage vector is already known for this type of inverters. This holds because the DC link voltage which is regulated to a constant reference value can be chopped with the PWM pulses to any arbitrary voltage vector with desired amplitude and angle. Figure 3-1indicates the control structure of a STATCOM working with vector controlled inverter. However, this type of inverter may be uneconomical for many transmission level FACTS devices due to the high switching losses of the PWM VSCs.

The other type of inverter is based on controlling only the angle of the output voltage. It has been shown in [19] that by a slight change of the inverter output voltage angle for a controlled time, the inverter is able to provide inductive/capacitive reactive power. Basically by controlling the α toward the positive/negative direction , for a controlled time, the DC-link voltage is driven lower/higher and therefore the VSC output voltage decreases/increases accordingly. In this type of inverter, the ratio between AC and DC voltages is kept constant and the VSC output voltage magnitude is varied indirectly by changing the DC bus voltage. Since angle α is the only control input in this control strategy, it is called *angle control*. Control architecture of the conventional *angle controller* STATCOM is illustrated in

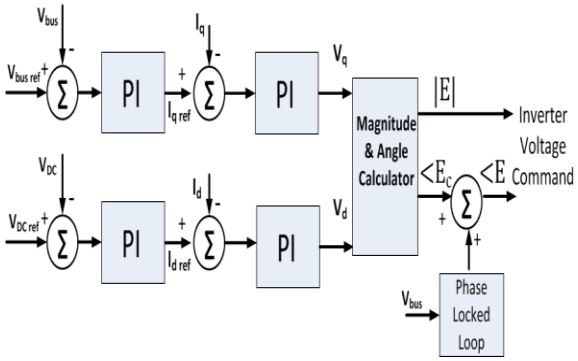


Figure 3-1. Control structure of a vector controlled (PWM) STATCOM.

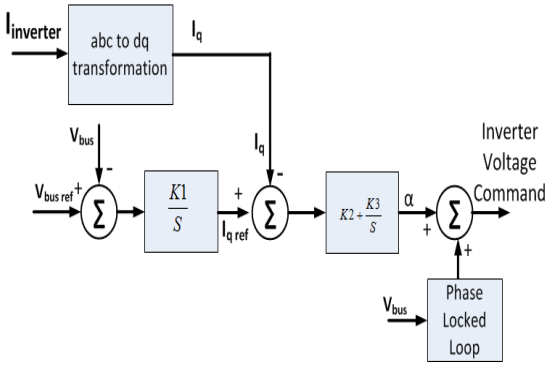


Figure 3-2. Control structure of an angle-controlled STATCOM.

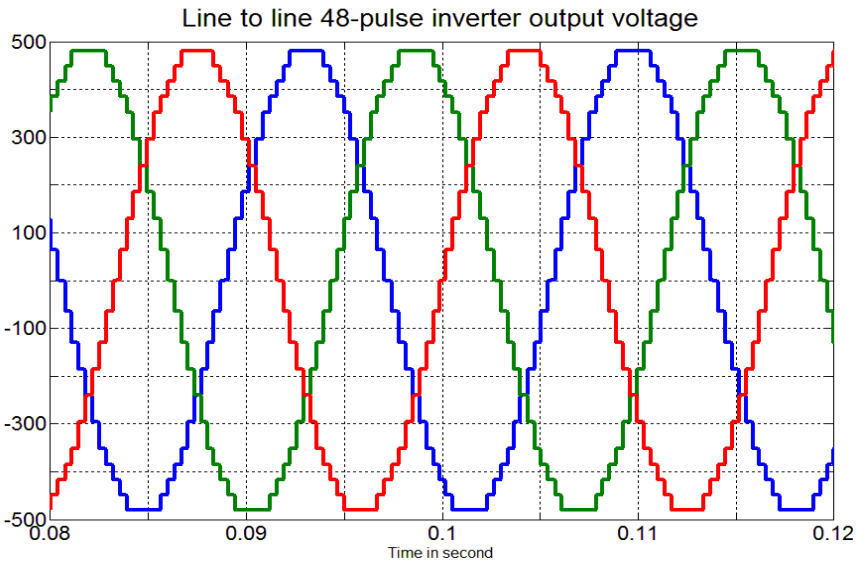


Figure 3-3. 48-pulse inverter line to line output voltages.

Figure 3-2. High-quality output voltage of the *angle-controlled* STACOM is provided by multi-pulse inverters. 24-pulse and 48-pulse inverters are commonly used for this kind of STATCOMs at the transmission level since the output voltage THD is 3-4% with low overall converter losses. The 100 MVA, 345 kV *angle-controlled* STATCOM model developed

based on the NYPA STATCOM (which was presented in the previous chapter) has been simulated in PSCAD/EMTDC. Voltage construction of this STACOM is carried out by a 48-pulse inverter as shown in Figure 3-3.Throughout this chapter, all the PSCAD/EMTDC simulation results, presented in different sections of this chapter are based on this STACOM simulation. The performance of this STATCOM under normal operating condition and variable instantaneous reactive current (iq) references is illustrated in Figure 3-4.

3.2.2 Angle-Controlled STATCOM under Unbalanced Conditions and System Faults

The VSC is the main building block of the STATCOM and many other converter-based FACTS devices. Therefore, the study on the methods to improve the VSC performance under unbalanced ac voltage condition is important and practical. Many different control structures have been proposed by the researchers to improve the VSC performance under fault conditions [36]- [54]. These are focused on mainly generating the current reference in both positive and negative synchronous frame to regulate the power or voltage at the point of common coupling (PCC). However, all these methods are based on controlling both the angle and magnitude of the VSC output voltage and are not applicable for *angle-controlled* STATCOMs with only one control input angle (α). There are very few studies that concentrate specifically on the *angle-controlled* STATCOM performance under AC-system fault conditions. Schauder *et al*.[19] have calculated the amount of the DC-link capacitor that minimizes the negative sequence current flow on the STATCOM tie line. They have shown that by choosing proposed amount of the DC-link capacitor, VSC along with tie line inductor becomes an open circuit for the fundamental negative sequence current, with the

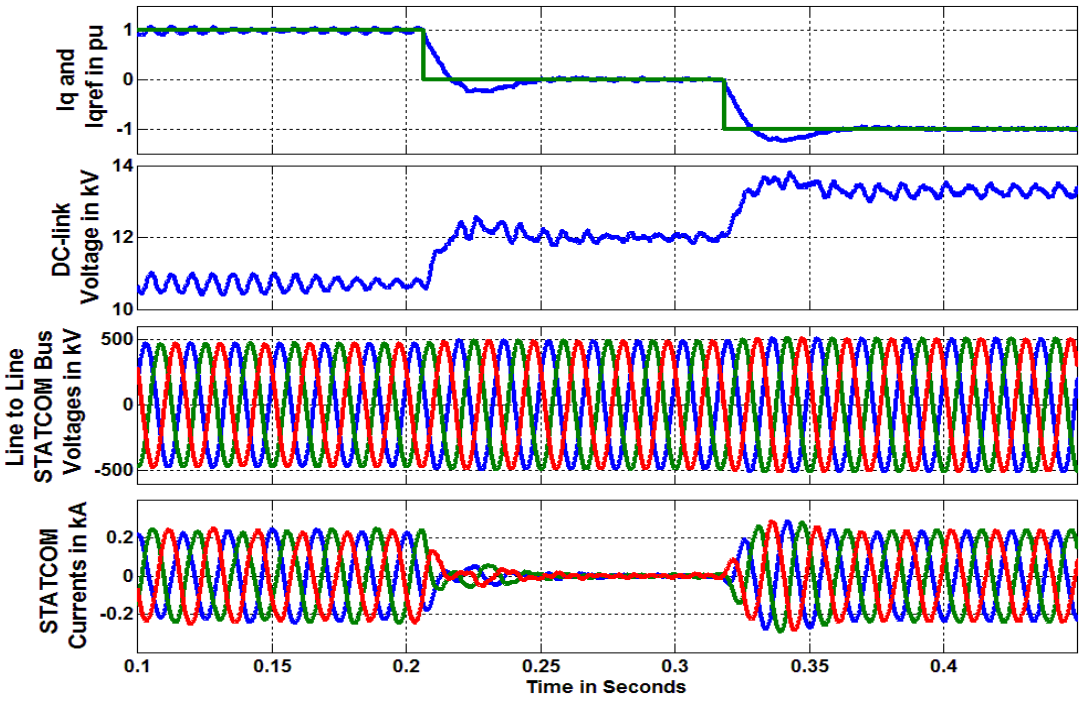


Figure 3-4. Angle-controlled STATCOM performance with two different instantaneous reactive current (Iq) references

implemented positive sequence angle (α) control. This solution although limits the negative sequence current dramatically, however, results in large DC-link voltage second harmonic oscillations. This high DC-link oscillation often trips the STATCOM due to DC-link over voltage. Authors in [55] have added a hysteresis current controller in addition to the conventional *angle controller*. In this current controller, the VSCs will individually detect and self-implement hysteresis switching to control their phase (VSC pole and device) currents within predetermined limits. Each VSC will ensure that its overcurrent limit determined in the controller is not reached during and after a system fault distortions. This solution protects the switches and limits the STATCOM current under fault condition; however, VSC currents and voltages and also DC-link voltage are much distorted. The DC-

link voltage oscillations seen by this method may also cause the STATCOM trip. On other hand, injecting poor quality voltage and current waveforms containing high harmonics into the faulted power system imposes undesirable stress on various power system components.

3. 3 Analysis of the VSC under unbalanced conditions

Symmetrical component are most commonly used for analysis of three-phase unbalanced electrical systems. In this method, a set of unbalanced three phase phasors is split into two symmetrical positive and negative sequences and one zero sequence component. Based on this theory, tie line currents of the STATCOM in Figure 3-5 under fault condition will be as:

$$i_a = i_a^+ + i_a^- + i_a^0 \tag{3-1}$$

$$i_a = i^+ \sin(\omega t + \theta_i^+) + i^- \sin(\omega t + \theta_i^-) + i^0 \sin(\omega t + \theta_i^0) \tag{3-2}$$

$$i_b = i^+ \sin\left(\omega t + \theta_i^+ - \frac{2\pi}{3}\right) + i^- \sin\left(\omega t + \theta_i^- + \frac{2\pi}{3}\right) + i^0 \sin(\omega t + \theta_i^0) \tag{3-3}$$

$$i_c = i^+ \sin\left(\omega t + \theta_i^+ + \frac{2\pi}{3}\right) + i^- \sin\left(\omega t + \theta_i^- - \frac{2\pi}{3}\right) + i^0 \sin(\omega t + \theta_i^0) \tag{3-4}$$

Since there is no path for neutral current to flow in three wire system, the zero sequence component is ignored throughout this paper. As it was mentioned earlier, in the *angle-controlled* STATCOM the only control input is angle α which is always applied identically to all three phases of the inverter. Therefore, the switching function for an *angle-controlled* STATCOM is always symmetric and by neglecting all the harmonics except the fundamental, (which is a fair assumption for a 24 and 48-pulse inverter due to output voltage THD typically around than 3%), the switching function for phase a, b, and c can be represented as:

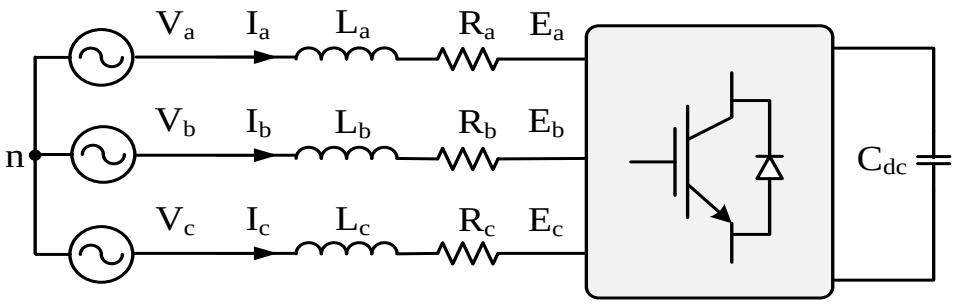


Figure 3-5. Equivalent circuit of a VSC connected to AC system.

$$s_a = K\sin(\omega t + \alpha) \tag{3-5}$$

$$s_b = K\sin\left(\omega t + \alpha - 2\frac{\pi}{3}\right) \tag{3-6}$$

$$s_c = K\sin\left(\omega t + \alpha + 2\frac{\pi}{3}\right) \tag{3-7}$$

where K is the factor for the inverter which relates the DC-side voltage to the amplitude of the phase to neutral voltage at the inverter AC-side terminals, and α is the angle by which the inverter voltage vector leads/lags the line voltage vector. Then the inverter terminal fundamental voltage is calculated as:

$$v_a = K\, v_{DC}\sin(\omega t + \alpha) \tag{3-8}$$

$$v_b = K\, v_{DC}\sin\left(\omega t + \alpha - 2\frac{\pi}{3}\right) \tag{3-9}$$

$$v_c = K\, v_{DC}\sin\left(\omega t + \alpha + 2\frac{\pi}{3}\right) \tag{3-10}$$

The interaction between the fundamental frequency inverter switching function and the negative sequence component of the current, produces 2nd harmonic oscillations on the DC-link voltage and current [39], [40]. Therefore general expression of DC-link voltage during unbalanced condition becomes: [37]

$$v_{DC} = V_{dc} + V_{dch2}\cos(2\omega t + \theta_v^{dc}) \quad (3\text{-}11)$$

where V_{dc} is the average value and V_{dch2} is the amplitude of the 2nd harmonic oscillations of DC-Link voltage.

Substituting (3-11) in (3-8)-(3-10), the inverter output voltages when the DC-link voltage is distorted by 2nd harmonic oscillations due to the unbalanced AC system are calculated as:

$$v_a = \mathrm{K}\,V_{dc}\sin(\omega t + \alpha) + \frac{KV_{dch2}}{2}\sin\left(3\omega t + \alpha + \theta_v^{dc}\right) + \frac{KV_{dch2}}{2}\sin(-\omega t + \alpha - \theta_v^{dc}) \quad (3\text{-}12)$$

$$v_b = \mathrm{K}\,V_{dc}\sin\left(\omega t + \alpha - 2\frac{\pi}{3}\right) + \frac{KV_{dch2}}{2}\sin\left(3\omega t + \alpha + \theta_v^{dc} - 2\frac{\pi}{3}\right) + \frac{KV_{dch2}}{2}\sin(-\omega t + \alpha - \theta_v^{dc} - 2\frac{\pi}{3}) \quad (3\text{-}13)$$

$$v_c = \mathrm{K}\,V_{dc}\sin\left(\omega t + \alpha + 2\frac{\pi}{3}\right) + \frac{KV_{dch2}}{2}\sin\left(3\omega t + \alpha + \theta_v^{dc} + 2\frac{\pi}{3}\right) + \frac{KV_{dch2}}{2}\sin(-\omega t + \alpha - \theta_v^{dc} + 2\frac{\pi}{3}) \quad (3\text{-}14)$$

Equations (3-12)-(3-14) show that the interaction between switching function and the DC-link voltage 2nd harmonic oscillations generates fundamental negative sequence voltage at the VSC output terminals. Basically, the unbalanced AC-system conditions can be emulated by postulating a set of negative sequence voltage source in series with STATCOM tie line [19]. The basic idea of the *Dual Angle Control* strategy is to generate required fundamental negative sequence voltage vector at the VSC output terminals to attenuate the effect of postulated negative sequence bus voltage. The generated negative sequence voltage, results in reduction of the negative sequence current seen by the STATCOM under fault conditions. It is important to note that interaction between switching function and the DC-link voltage

2^{nd} harmonic oscillations also generates 3^{rd} harmonic voltage at the VSC output terminals. This 3^{rd} harmonic voltage is positive sequence and phase a, b, and c are 120 degree apart. Basically, the negative sequence current flow due to unbalanced AC-system condition generates the 2^{nd} harmonic oscillations on the DC-link voltage which will be reflected as fundamental negative sequence voltage and 3^{rd} harmonic voltage at the VSC terminals. Similar to the fundamental negative sequence voltage, the amplitude of this 3^{rd} harmonic voltage is decided by the DC-link voltage 2^{nd} harmonic oscillations. This chapter will show that by controlling 2^{nd} harmonic oscillations on the DC-link voltage, the negative sequence current will reduce significantly. Decreased negative sequence current will inherently reduce the DC-link voltage 2^{nd} harmonic oscillations. Reduction in DC-link voltage 2^{nd} harmonic oscillations results in decreasing the 3^{rd} harmonic voltage and therefore current at STATCOM tie line.

The negative sequence voltage calculated in equation (3-12)-(3-14) was verified with PSCAD/ EMTDC simulation of a three-level Neutral Point Clamped (NPC) based 48-pulse inverter. The DC-side of the inverter is supplied from two series connected 6 kV DC voltage sources in series with two variable AC voltage sources as shown in Figure 3-6. The AC-side is left open circuit. Table 3-1 compares the theoretical value of the positive and negative sequence output voltage with simulation results. In the first row, for example, the inverter output negative sequence voltage according to equation (3-12) is $\frac{345}{12\times2} \times 1 = 14.37\ kV$ which perfectly matches with simulation results. Figure 3-7 indicates the harmonic content of the inverter output voltage with two different values of 2^{nd} harmonic oscillations added to the

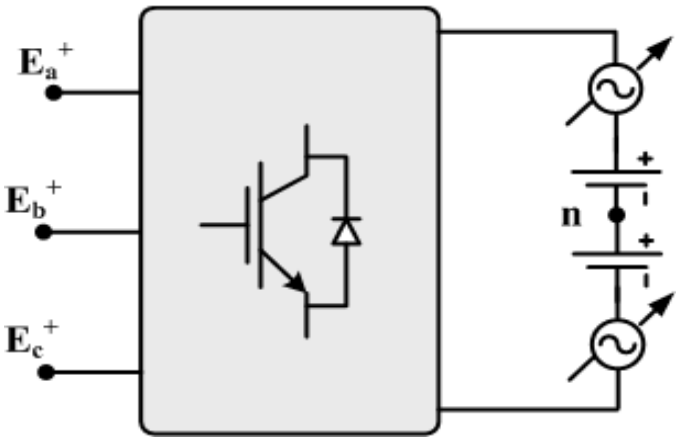


Figure 3-6. Equivalent circuit of the 3-Level NPC VSC used for calculation of the fundamental negative sequence voltage vector at VSC output terminals

Table 3-1: calculation and simulation results of one three level NPC 48-pulse inverter

DC Bus Voltage (kv)	Pos Seq Fundamental Theory (kV)	Neg Seq Fundamental Theory (kV)	Pos Seq Fundamental Simulation(kV)	Neg Seq Fundamental Simulation(kV)
v_{DC}=12+1sin(2wt)	345	14.37	342.5	14.23
v_{DC}=12+2sin(2wt)	345	28.75	342.5	28.46
v_{DC}=12+3sin(2wt)	345	43.12	342.5	42.78
v_{DC}=12+4sin(2wt)	345	57.50	342.5	56.9
v_{DC}=12+5sin(2wt)	345	71.87	342.5	70.25

DC-link and compares them with base case i.e. without any oscillations on the DC-link voltage. As can be observed in this figure, with different 2nd harmonic oscillation on the DC-bus, the fundamental voltage remains unchanged. The change in the other harmonics, excluding the 3rd harmonic and negative sequence voltage, is also negligible. This idea of generating desirable negative sequence voltage vector by controlling the DC-link voltage 2nd harmonic oscillations has been used in this chapter to develop the *Dual angle controller*.

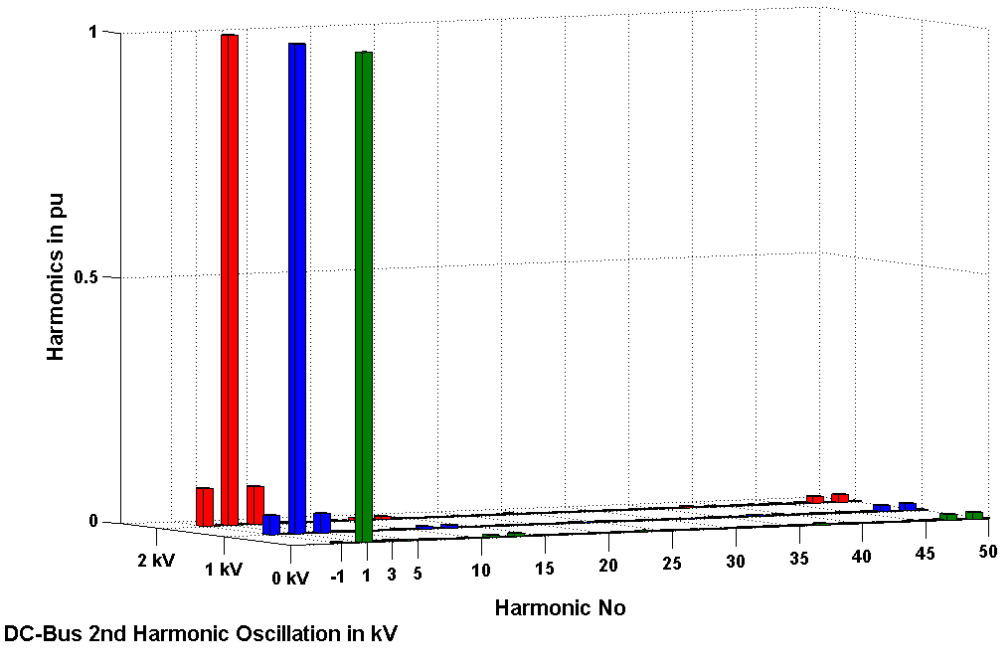


Figure 3-7. 48-pulse inverter output voltage harmonic content with different 2nd harmonic oscillations added to the DC-link voltage

3. 4 Proposed Control Structure

3.4.1 Derivation of STATCOM equations in the negative synchronous frame

As discussed in the previous section, STATCOM voltage and current during unbalanced conditions can be calculated by postulating a set of negative sequence voltage in series with STATCOM tie line as shown in Figure 3-8. As discussed earlier, negative sequence current at STATCOM tie line generates 2nd harmonic oscillations at the DC-link voltage. This 2nd harmonic oscillation will be reflected as negative sequence voltage at STATCOM terminals as calculated in (3-12)-(3-14).

Assuming 2nd harmonic oscillation at DC-link voltage as:

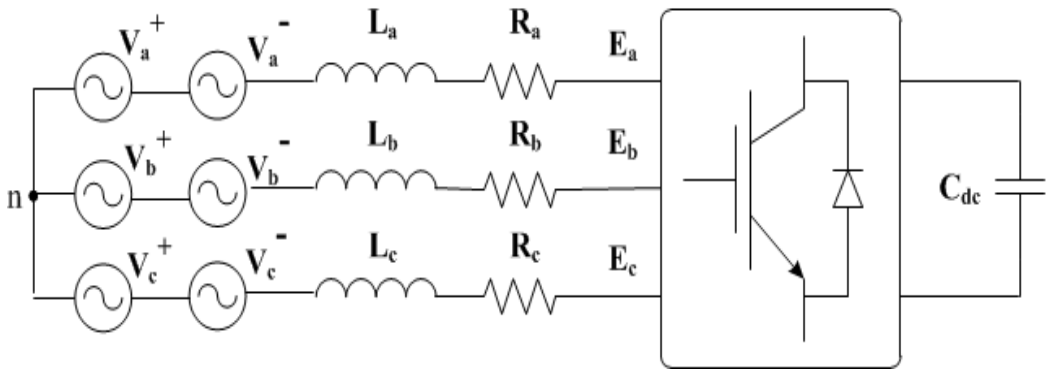


Figure 3-8. STATCOM equivalent circuit with series negative sequence voltage sources

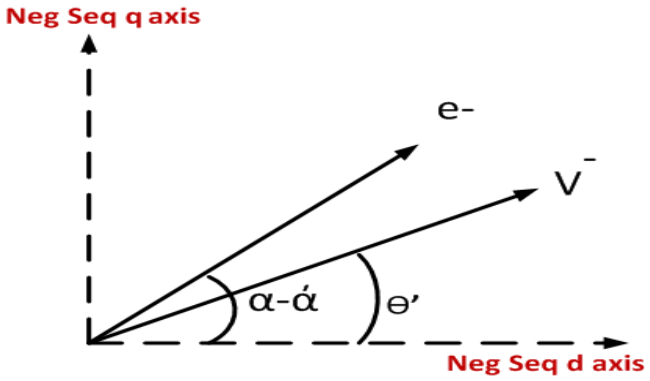


Figure 3-9. STATCOM instantaneous vectors in the negative synchronous frame

$$V_{dch2}\cos(2\omega t + \alpha') \tag{3-15}$$

then reflected negative sequence voltages at STATCOM terminal are calculated as in (3-16)-(3-18).

$$e_a^- = \frac{KV_{dch2}}{2}\, sin(-\omega t + \alpha - \alpha') \tag{3-16}$$

$$e_b^- = \frac{KV_{dch2}}{2}\, sin(-\omega t + \alpha - \alpha' - \frac{2\pi}{3}) \tag{3-17}$$

$$e_c^- = \frac{KV_{dch2}}{2}\, sin(-\omega t + \alpha - \alpha' + \frac{2\pi}{3}) \tag{3-18}$$

The derivative of STATCOM tie line negative sequence currents with respect to time are calculated as in (3-19)-(3-21).

$$\frac{di_a{}^-}{d_t} = \frac{-R}{L} i_a{}^- + \frac{(e_a{}^- - V_a{}^-)}{L} \tag{3-19}$$

$$\frac{di_b{}^-}{d_t} = \frac{-R}{L} i_b{}^- + \frac{(e_b{}^- - V_b{}^-)}{L} \tag{3-20}$$

$$\frac{di_c{}^-}{d_t} = \frac{-R}{L} i_c{}^- + \frac{(e_c{}^- - V_c{}^-)}{L} \tag{3-21}$$

Transformation from abc to negative synchronous frame is defined as: [28]

$$f_{dq}^- = T(-\omega t) f_{abc}^- \tag{3-22}$$

where:

$$T(-\omega t) = \frac{2}{3}\begin{bmatrix} \cos(-\omega t) & \cos(-\omega t - \frac{2\pi}{3}) & \cos(-\omega t + \frac{2\pi}{3}) \\ -\sin(-\omega t) & -\sin(-\omega t - \frac{2\pi}{3}) & -\sin(-\omega t + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \tag{3-23}$$

and ωt is the STATCOM ac-bus phase locked loop output.

Figure 3-9 illustrates the instantaneous negative sequence STATCOM bus (v^-) and inverter output voltage (e^-) in the negative synchronous frame. Vector v^- is assumed to have an arbitrary angle of Θ'. d and q components of these two vectors are calculated as:

$$e_d^- = |e^-| \cos(\alpha - \alpha') = \frac{KV_{dch2}}{2} \cos(\alpha - \alpha') \tag{3-24}$$

$$e_q^- = |e^-| \sin(\alpha - \alpha') = \frac{KV_{dch2}}{2} \sin(\alpha - \alpha') \tag{3-25}$$

$$v_d^- = |v^-| \cos(\theta') \tag{3-26}$$

$$v_q^- = |v^-| \sin(\theta') \tag{3-27}$$

Transforming equation (3-19)-(3-21) based on (3-23), we find:

$$\frac{d}{dt} i_d^- = \frac{-R}{L} i_d^- - \omega i_q^- + \frac{K}{2L} V_{dch2} \cos(\alpha - \alpha') - \frac{1}{L} v_d^- \tag{3-28}$$

$$\frac{d}{dt} i_q^- = \frac{-R}{L} i_q^- + \omega i_d^- + \frac{K}{2L} V_{dch2} \sin(\alpha - \alpha') - \frac{1}{L} v_q^- \tag{3-29}$$

Equation (3-28) and (3-29) describe the dynamics of the VSC AC-side negative sequence current, in terms of negative synchronous frame variables and 2nd harmonic oscillations of the DC-link voltage. These equations show that the dynamics of STATCOM tie line negative sequence current d and q components (i_d^- , i_q^-) are related to the phase and amplitude of the DC-link voltage 2nd harmonic oscillations.

3.4.2 Control input to control the negative sequence current

As discussed earlier, *Dual Angle Control* strategy is based on generating required fundamental negative sequence voltage vector at the VSC output terminals to attenuate the effect of postulated negative sequence bus voltage under fault conditions and to limit the negative sequence current. The required negative sequence voltage vector is obtained by controlling the 2nd harmonic DC-link voltage oscillations. This part shows that DC-link voltage 2nd harmonic oscillations are controlled by adding appropriate oscillations to the conventional *angle controller* output i.e. angle α. It was mentioned earlier that α is the only control input for the *angle-controlled* STATCOM. α is a control angle that has a pulse type characteristic in the normal operation. In steady state α is zero. Transiently it moves toward the positive or negative direction to decrease or increase the DC-link voltage and then goes

back to zero. Small variations of the DC-link voltage around a chosen steady state point when all the losses are ignored is related to angle α perturbation through a third order transfer function as calculated in (3-30).

$$\frac{\Delta V_{dcpu}}{\Delta \alpha(s)} = \frac{-C^{"} i_{q0} s^2 - V_{DCpu0} L^{"} C^{"} w_b - C^{"} i_{q0} {w_b}^2}{s(s^2 + C^{"} L^{"} + {w_b}^2)} \tag{3-30}$$

$C^{"}$ and $L^{"}$ were defined in the last chapter [19].

Where:

$$L^{"} = \frac{k w_b}{L'} \tag{3-31}$$

$$C^{"} = \frac{3 k w_b C'}{2} \tag{3-32}$$

C' and L' are the per-unit values of the DC-link capacitor and STATCOM tie line inductance as described in the last chapter:

$$L' = \frac{w_b L}{Z_{base}} \tag{3-33}$$

$$C' = \frac{1}{w_b C Z_{base}} \tag{3-34}$$

Numerical calculation for the 100 MVA, 345 kV *angle-controlled* STATCOM has been done for two operating points to illustrate the DC-link voltage behavior in response to changing α. Results for these two cases, one in inductive and the other one in capacitive mode, in a logarithm plot of gain and phase against frequency is presented in Figure 3-10. This figure shows that introducing 2nd harmonic oscillations to the α, results in 90° leading 2nd harmonic oscillations on the DC-link voltage in both capacitive and inductive mode of operations. This result has been verified by PSCAD/EMTDC simulation results.

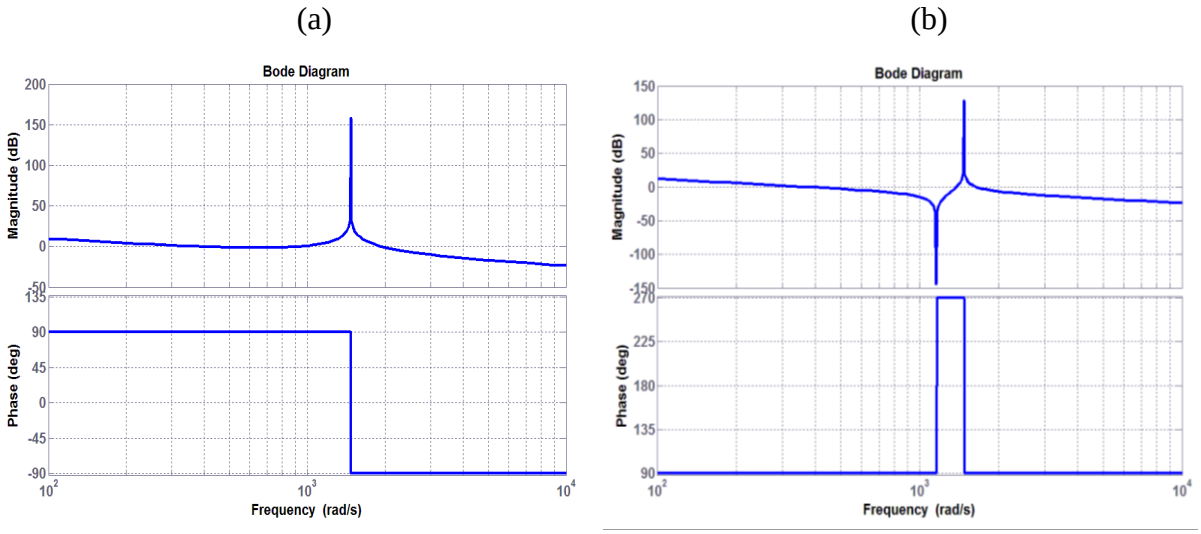


Figure 3-10. Bode plots of the DC-link voltage perturbation against α perturbation around a capacitive (a)/inductive (b) equilibrium point

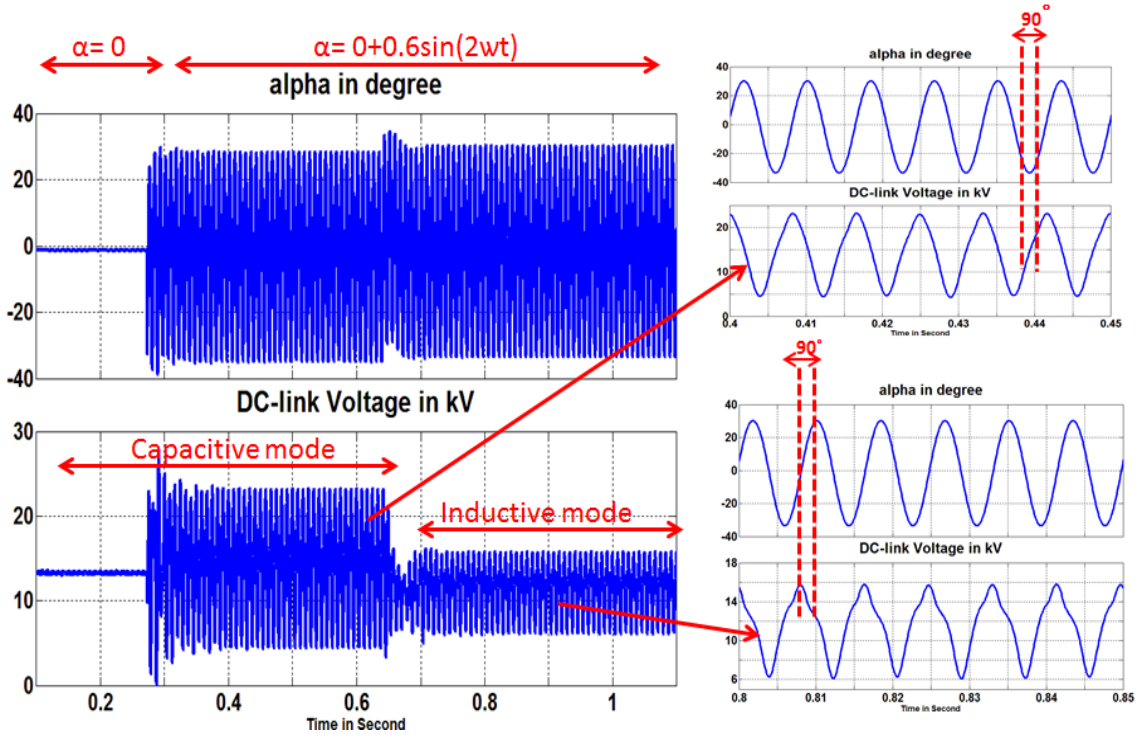


Figure 3-11. DC-link voltage 2nd harmonic oscillations generated by introducing 2nd harmonic oscillations to the α in both capacitive and inductive operation modes

Figure 3-11 illustrates the 2^{nd} harmonic DC-link voltage oscillations generated by introducing 2^{nd} harmonic oscillations to the α in both capacitive and inductive mode of operations. Initially the STATCOM is working in capacitive mode with steady state α of 0˚. At around t=0.3 second, 2^{nd} harmonic oscillation of 0.6sin (2ωt) radian is added to α. These oscillations generate 90˚ leading 2^{nd} harmonic oscillations on the DC-link voltage. At around t=0.7 second, STATCOM switched to inductive mode and as can be observed, DC-link voltage oscillations amplitude decreases but it is still leads the α oscillations by 90˚. This concept of 90˚ phase shift between DC-link voltage and α 2^{nd} harmonic oscillation has been used in the Dual Angle Controller. The application of this concept to develop the DAC has been discussed in details in the following part and appendix (3-A).

3.4.3 Control structure

In the proposed controller, angle α is split into two parts, α_{dc} and α_{ac}. The angle α_{dc} is the output of the positive sequence controller which is the same as conventional angle controller. Rejection notch filter at double the line frequency has been added to the measured current in synchronous frame to isolate the positive sequence controller from the negative sequence signals. The output of the negative sequence controller is α_{ac}. The angle α_{ac} is the 2^{nd} harmonic oscillations with appropriate phase and amplitude to generate the required negative sequence voltage vector at the VSC terminals to attenuate the effect of the postulated negative sequence bus voltage under fault conditions. The generated negative sequence voltage results in reduction of the negative sequence current seen by the STACOM. Like the positive sequence controller, sequence extraction is implemented using rejection notch filters.

The α_{ac} should be properly filtered such that it contents only 2nd harmonic oscillations otherwise it will generate higher order harmonics oscillations on the DC-link voltage which will be reflected as higher order harmonic voltage on the AC-side. It was discussed earlier that 2nd harmonic oscillations on the DC-link voltage does not affect the fundamental inverter output voltage and all the other harmonics (excluding the 3rd and fundamental negative sequence voltage) remain almost unchanged. The phase of the α_{ac} is coming from the 2nd harmonic oscillations of the q-axis component of the tie line current in the positive synchronous frame when system is unbalanced. The negative sequence current appears as 2nd harmonic oscillations in the q-axis component of the line current in positive synchronous frame as calculated in (3-35).

$$\frac{2}{3}\begin{bmatrix} i^{-}\sin(-\omega t+\theta_i^{-}) \\ i^{-}\sin\left(-\omega t+\theta_i^{-}-\frac{2\pi}{3}\right) \\ i^{-}\sin\left(-\omega t+\theta_i^{-}+\frac{2\pi}{3}\right) \end{bmatrix}\left[-\sin(\omega t) \quad -\sin(\omega t-\tfrac{2\pi}{3}) \quad -\sin(\omega t+\tfrac{2\pi}{3})\right]= \tag{3-35}$$

$$i^{-}\cos(-2\omega t+\theta_i^{-}+\pi)=i^{-}\cos(2\omega t-\theta_i^{-}+\pi)$$

It is shown in appendix (3-A) that injecting a 2nd harmonic oscillation in phase with the signal of equation (3-35) as α_{ac}, will generate negative sequence voltage in phase with v^{-} (STATCOM AC-bus negative sequence voltage due to unbalanced conditions and faults) at the STATCOM terminals. The amplitude of the α_{ac} is regulated by a PI controller. The proposed control structure is shown in Figure 3-12.

3. 5 PSCAD/EMTDC simulation results

The same 100 MVA, 345 kV STATCOM used to obtain the results in Figure 3-4, Figure 3-10, and Figure 3-11 (described in the preceding chapter) has been used to verify the *DAC*

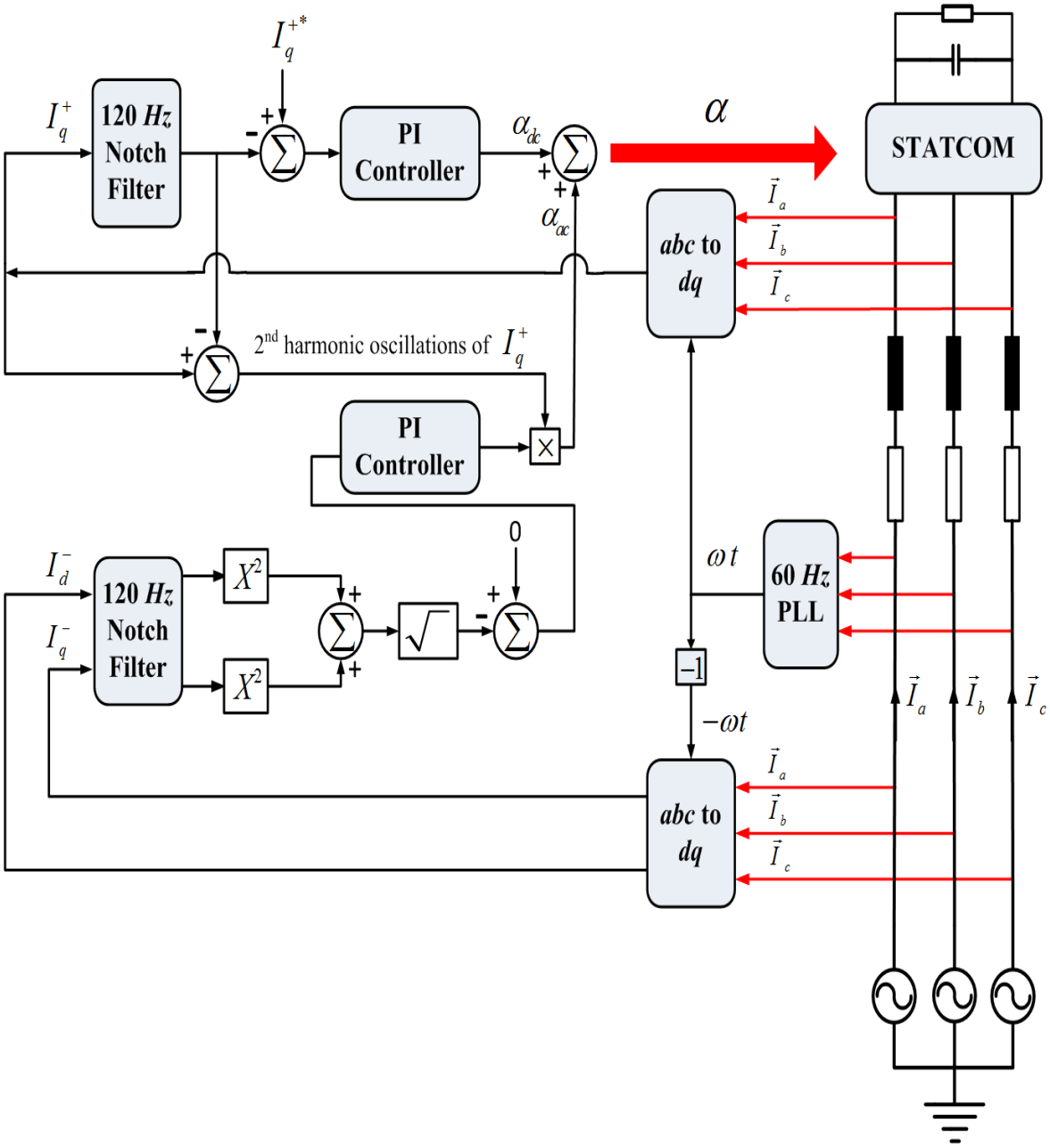


Figure 3-12. Proposed Control structure

performance under fault conditions. As mentioned earlier, the voltage construction of this STATCOM is carried out by a 48-pulse inverter topology[30]. This STATCOM has been

connected to a reduced order 3-bus AC system model of the NYPA as shown in Figure 3-13. AC system voltage is 345 kV. Figure 3-14 demonstrates the STATCOM performance with and without *DAC* under single line to ground (SLG) fault at phase c, right at STATCOM bus. The STATCOM is operating in the capacitive mode with reactive power injection of 100 MVAR (nominal rating of the system). I_{dneg} and I_{qneg} represent the negative sequence

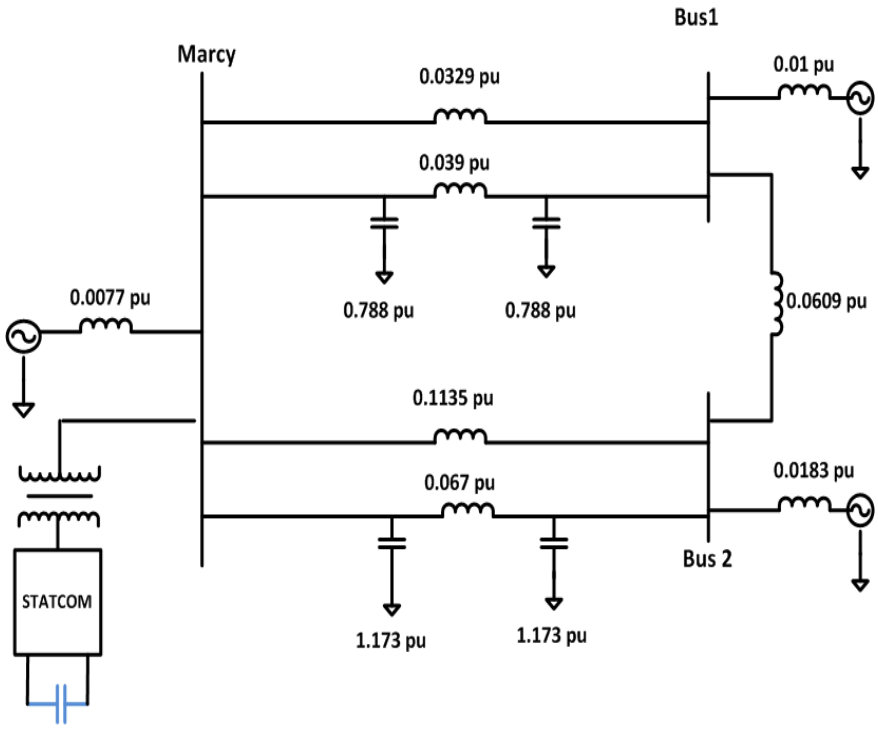


Figure 3-13. 3-bus AC system model. All the pu values are based on 345 kV and 100 MVA

STATCOM tie line current d and q axis components in negative synchronous frame respectively. After applying fault at t=0.2 second, in the case of STATCOM with conventional *angle controller*, I_{dneg} and I_{qneg} increase significantly. The RMS value of the

negative sequence current of STATCOM reaches to around 1.1 kA and DC-link voltage 2nd harmonic oscillations is very large. By contrast, with proposed *DAC* structure, the RMS value of the negative sequence tie line current reaches only to around 0.2 kA after fault applied. DC-link voltage 2nd harmonic oscillations are low and will not trigger the STATCOM DC-link over voltage protection. The same test has been applied to the STATCOM when it is working in inductive mode and absorbing 100 MVAR reactive power from the grid. As can be observed in Figure 3-15, similar to the capacitive mode of operation, the RMS value of the negative sequence STATCOM current in inductive mode is limited perfectly by *DAC* after fault. In contrast with conventional *angle controller*, DC-link voltage 2nd harmonic oscillations are reduced significantly by the proposed *DAC*. The proposed *DAC* performance has also been verified by applying AC-system faults at different locations of the 3-bus AC system model. Figure 3-16 indicates the STATCOM performance with and without proposed *DAC* when there is a SLG fault at phase C and STATCOM is working in the capacitive mode. In this case, SLG fault is applied in the middle of the Marcy-Bus1 345 kV outgoing transmission line in the 3-bus AC system model. In other test, SLG fault at phase C has been applied in the middle of the Marcy-Bus2 345 kV transmission line in the 3-bus AC system model when STATCOM is working in the capacitive mode. The STATCOM performance of this test with and without proposed *DAC* is shown in Figure 3-17. The simulation results illustrated in Figure 3-16, and Figure 3-17 validate the capability of the proposed *DAC* in limiting the STATCOM negative sequence current when there is an AC system fault at different locations of the 3-bus AC system.

3. 6 Experimental verification

3.6.1 Brief description of Transient Network Analyzer (TNA)

Experimental verification has been implemented on a very unique Transient Network Analyzer (TNA) hardware system. The TNA description was given in the last chapter. However, to make this chapter self-sufficient a brief outline is given here. The TNA is a scaled analogue equivalent model of the actual transformers, switches, and the exact 48-pulse inverter topology installed at 345 kV Marcy substation. The control system is exactly the same as the controller that is installed at the Marcy substation. To provide an overall view of

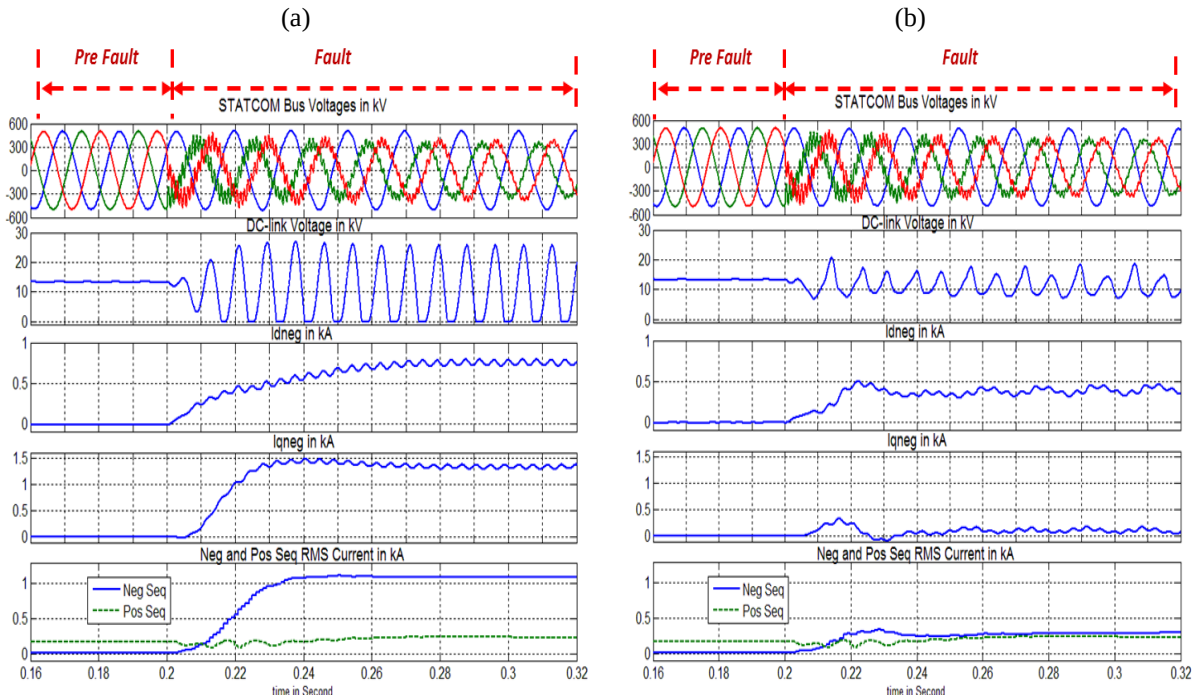


Figure 3-14. STATCOM performance with (b) and without (a) proposed DAC when STATCOM is working in capacitive mode and SLG fault at phase C is applied right at STATCOM bus. (PSCAD/EMTDC simulation results)

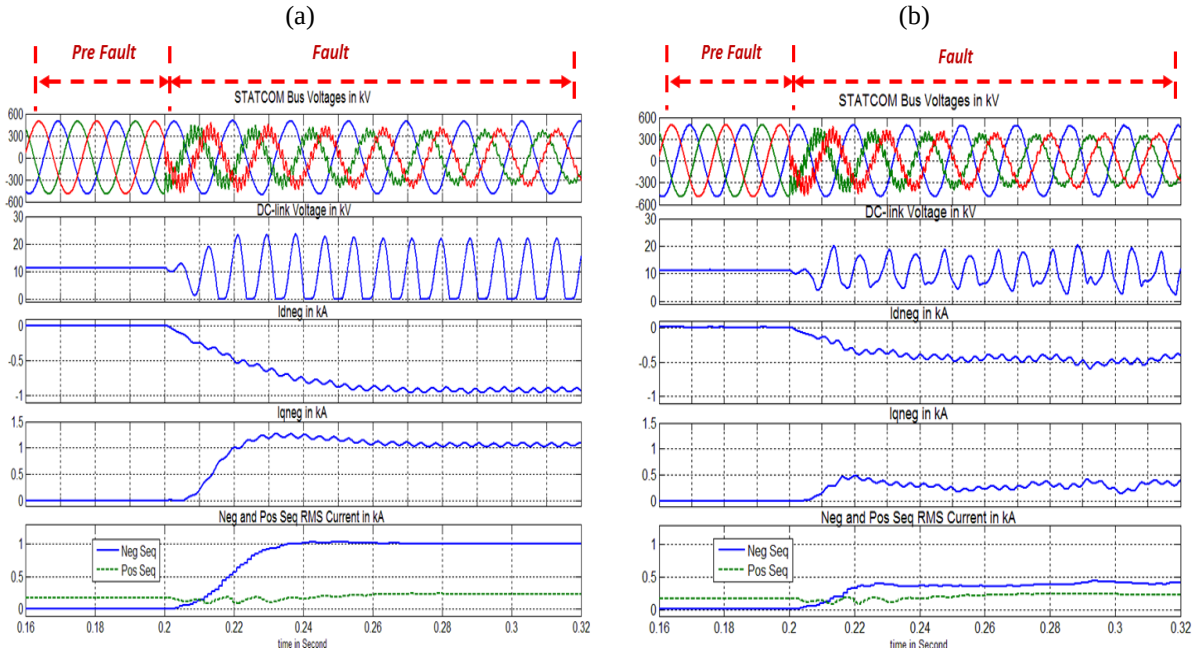


Figure 3-15. STATCOM performance with (b) and without (a) proposed DAC when STATCOM is working in inductive mode and SLG fault at phase C is applied right at STATCOM bus. (PSCAD/EMTDC simulation results)

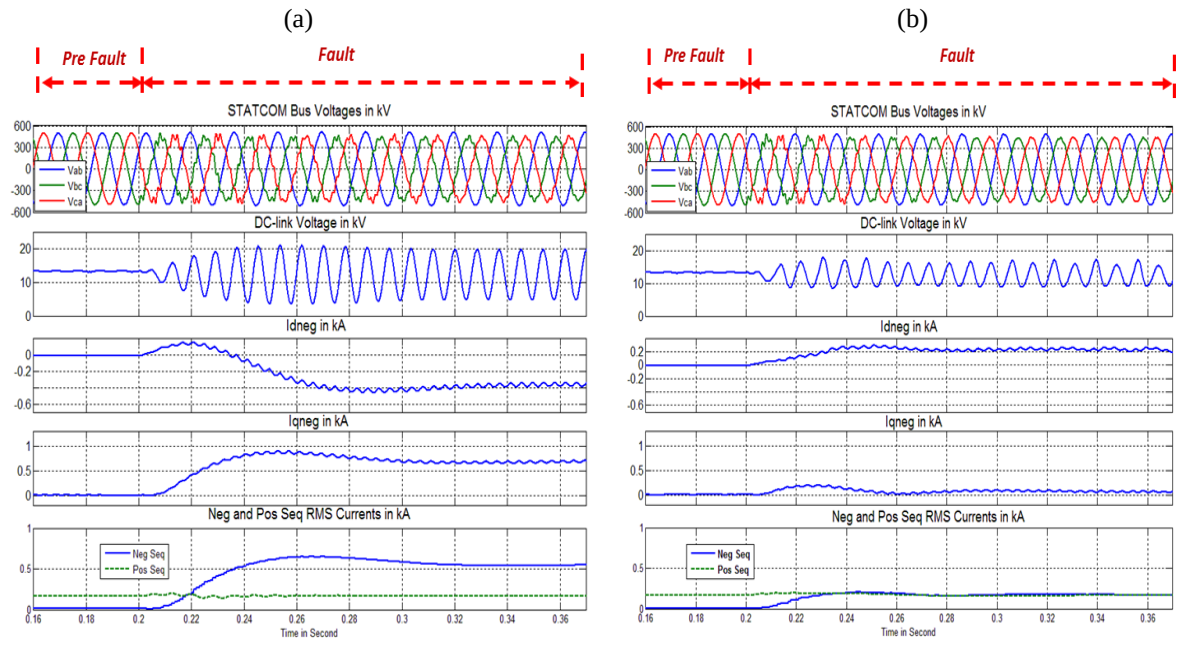


Figure 3-16. STATCOM performance with (b) and without (a) proposed DAC when STATCOM is working in capacitive mode and SLG fault at phase C is applied in the middle of the Marcy-Bus1 345 kV outgoing transmission line in the 3-bus AC system . (PSCAD/EMTDC simulation results)

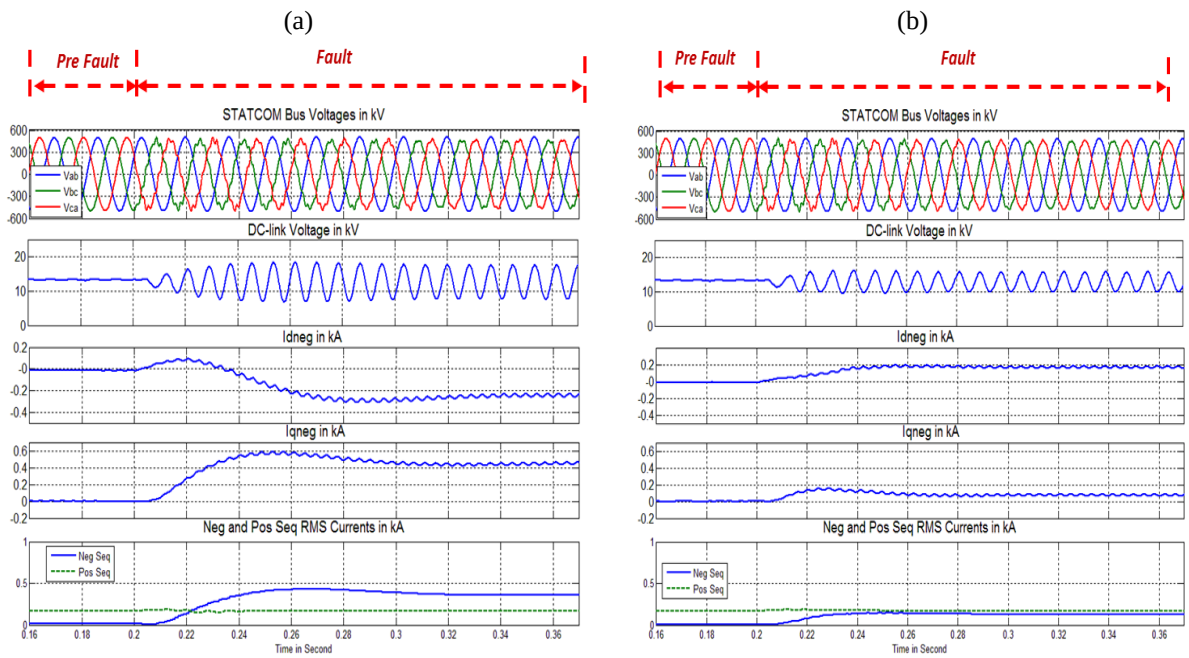


Figure 3-17. STATCOM performance with (b) and without (a) proposed DAC when STATCOM is working in capacitive mode and SLG fault at phase C is applied in the middle of the Marcy-Bus2 345 kV outgoing transmission line in the 3-bus AC system . (PSCAD/EMTDC simulation results)

testing system, the interface of the TNA to the controllers is shown conceptually in Figure 3-18. Figure 3-19 shows the 3-bus AC-system, inverter, control, and all the transformer magnetic panels. The AC system is a scaled down equivalent model of the NYPA 3-bus AC system that used for simulation verification as shown in Figure 3-20 . The entire power circuit of the actual 2×100MVA Marcy STATCOMs has been scaled down and replicated in the TNA system. The nominal inverter rating of 100 MVA is scaled to 12 VA and the nominal system voltage of 345 kV is scaled to 100 V RMS (L-L). The magnetics, the substation bus structure, and transmission line impedances at the Marcy substation have also been similarly replicated using scaled down hardware components. The power circuit

topology of the inverters along with auxiliary and shunt transformers that are used to construct the 48-pulse AC output voltage in the TNA are illustrated in Figure 3-21.

3.6.2 Experimental Results

The proposed controller performance under an unbalanced conditions has been verified by injecting 25% negative sequence voltage in series with STATCOM bus generator.Figure 3-22 illustrates the STATCOM performance under the unbalanced condition with and without *DAC* when it is operating in the capacitive mode of operation. I_{dneg} and I_{qneg} are representing the negative sequence STATCOM tie line current d and q components in negative synchronous frame respectively. The STATCOM is operating under nominal

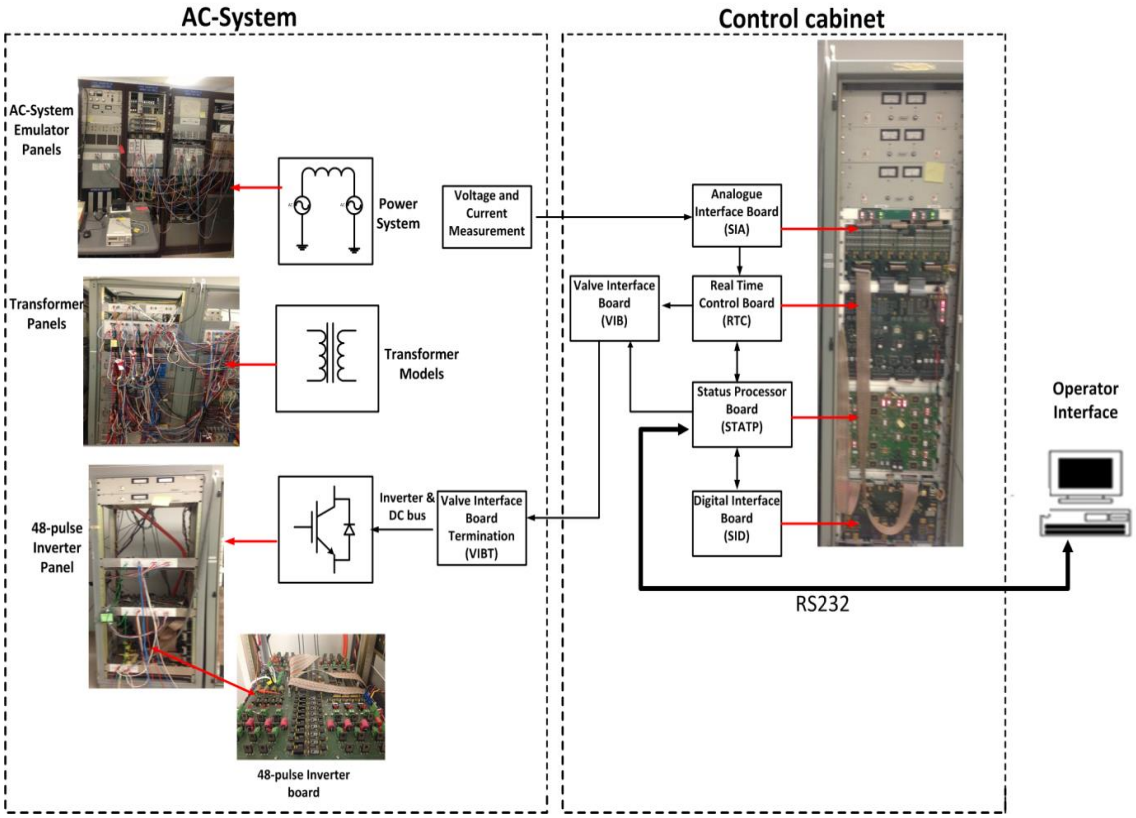


Figure 3-18. Interface of Control equipment to TNA

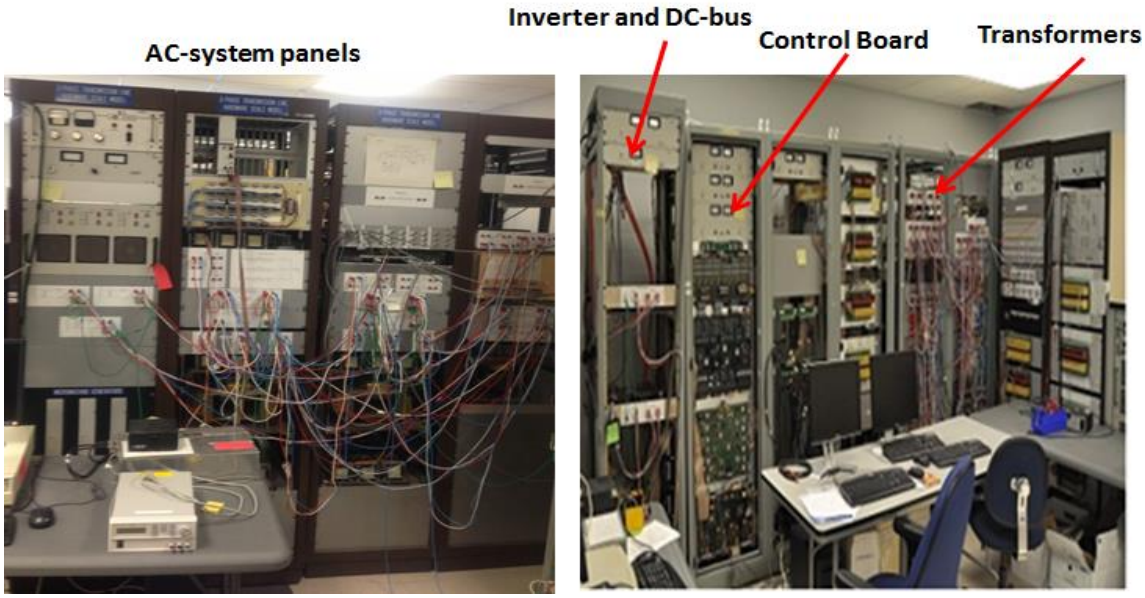


Figure 3-19. Control and magnetic panels

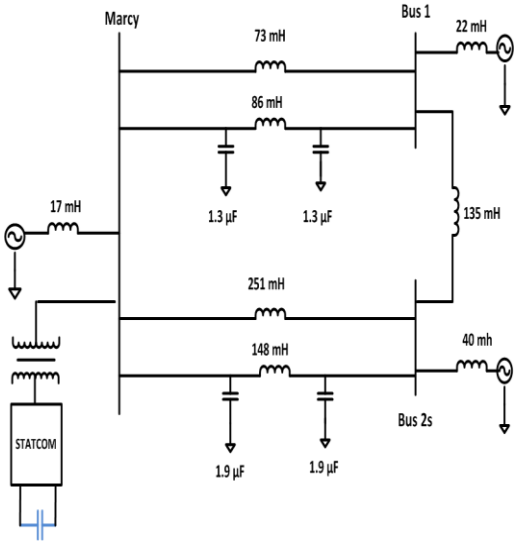


Figure 3-20. Scaled down model of the NYPA 3-bus AC system used for experimental verification

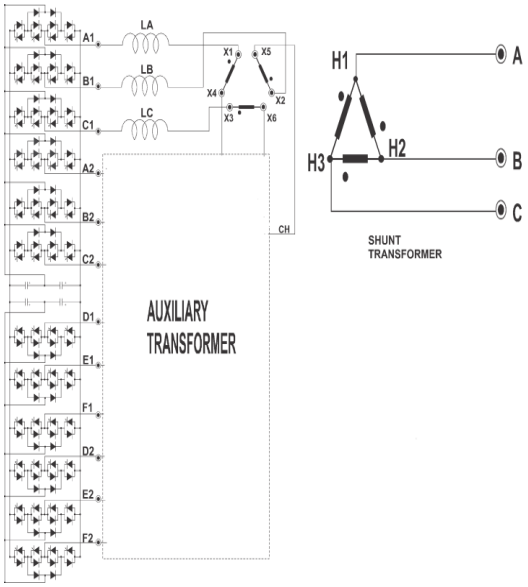


Figure 3-21. Power circuit topology of the inverters connected to auxiliary and shunt transformers to construct 48-pulse output voltage waveform

condition and injecting 1 pu of capacitive current to the AC-system. As can be observed in Figure 3-22 , DC-link voltage 2nd harmonic oscillations are very large when STATCOM is controlled by the conventional *angle controller*. The amplitude of the negative sequence current is also very high. However, when the STATCOM controller switches to the proposed DAC, the DC-link voltage oscillations decrease dramatically and the negative sequence current reaches close to zero. The decreased DC-link voltage 2nd harmonic oscillations reduce the 3rd harmonic VSC output voltage and consequently the 3rd harmonic current of STATCOM tie line. Reduction in negative sequence current decreases the fault peak current from around 1.8 pu to around 1 pu. This reduction in fault peak current prevents the protection system from over current tripping while the safe operation of the switches and other STATCOM power components is provided. The unbalanced current THD decreases from 5.6%, in case of STATCOM with conventional angle controller, to 1.1% in case of STATCOM with DAC.

The performance of the proposed controller under severe fault condition has also been verified by experimental results. Attention is taken to SLG fault, right at STATCOM bus when the STATCOM is operating under nominal condition. Plots in Figure 3-23 indicate the STATCOM performance with and without the DAC under SLG fault at the STATCOM bus phase C when STATCOM is operating in capacitive mode. As can be seen in this figure, the DAC decreases the negative sequence current and consequently the fault peak current dramatically. The significant reduction in DC-link voltage 2nd harmonic oscillations reduces the STATCOM tie line 3rd harmonic current. The STATCOM fault current THD reaches from 3.8%, in case of STATCOM with conventional controller, to the 2.2% in case of

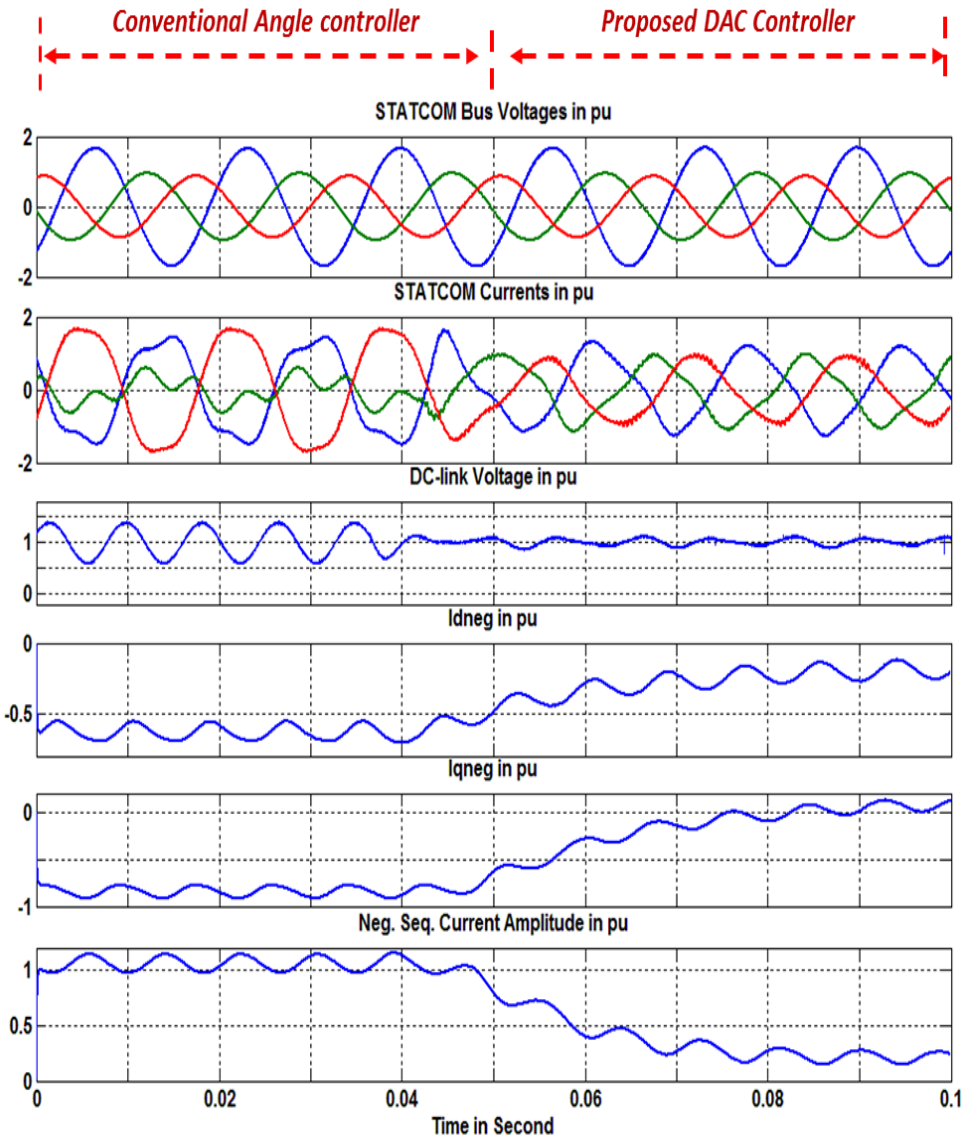
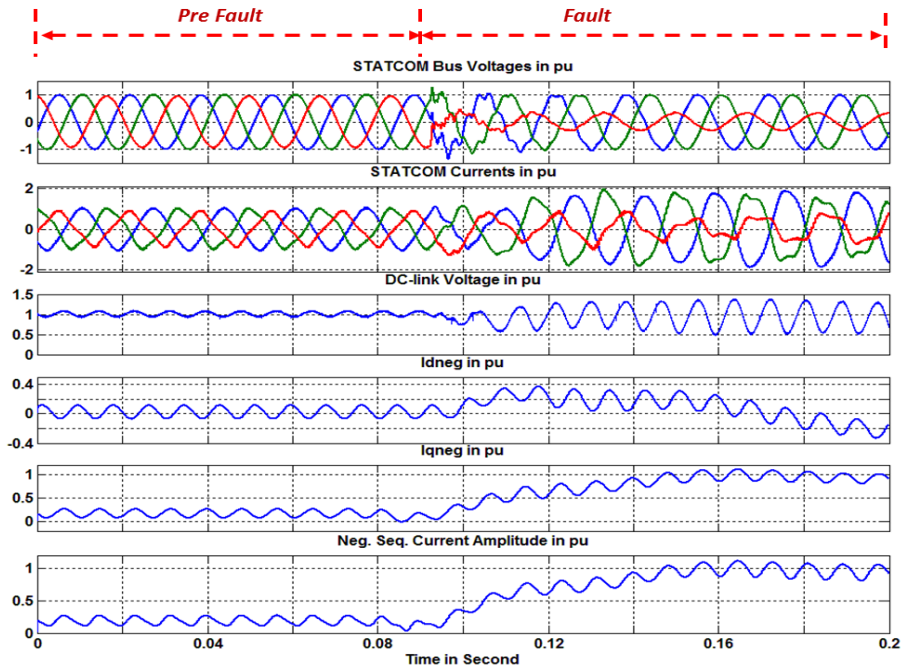


Figure 3-22. STATCOM performance with and without DAC in capacitive operation mode when there is 25% of negative sequence voltage injection at STATCOM bus. All pu values are based on 12 VA and 100 V RMS (L-L) ac system. (Experimental results)

(a)



(b)

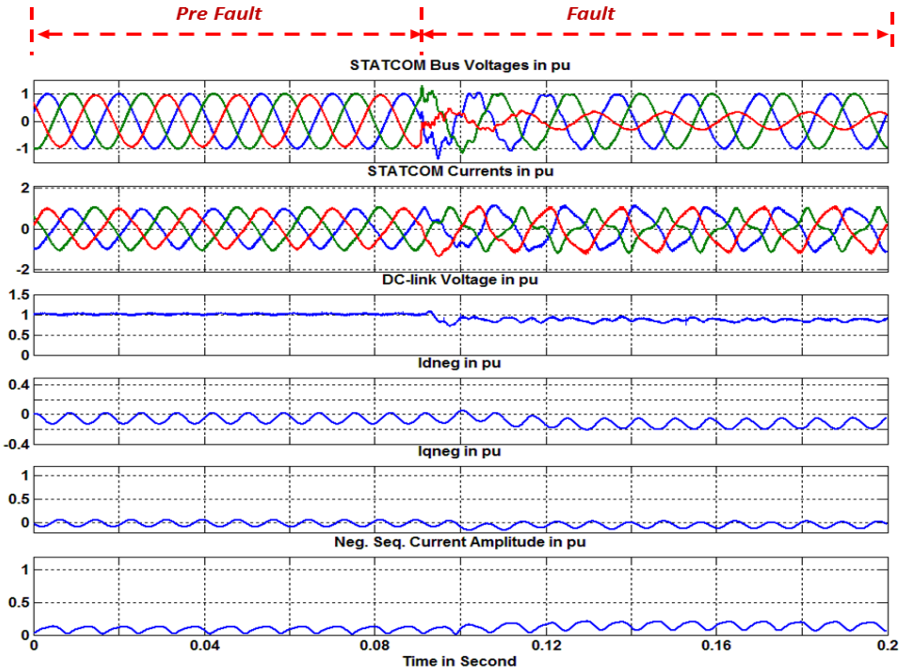
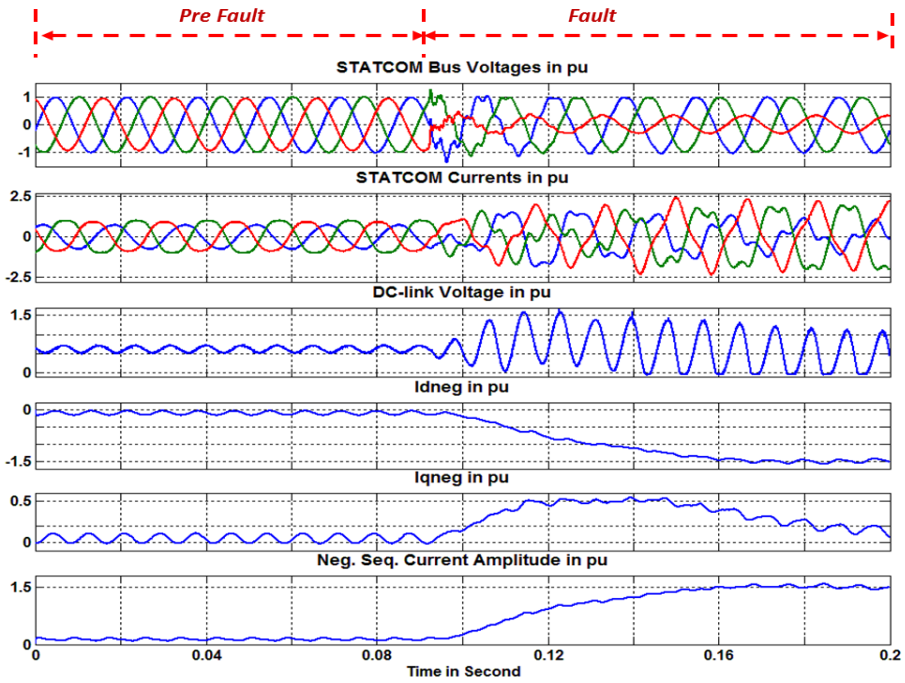


Figure 3-23. Capacitive mode performance of STATCOM under single line to ground fault with (b) and without (a) DAC. All pu values are based on 12 VA and 100 V RMS (L-L) ac system. (Experimental results)

(a)



(b)

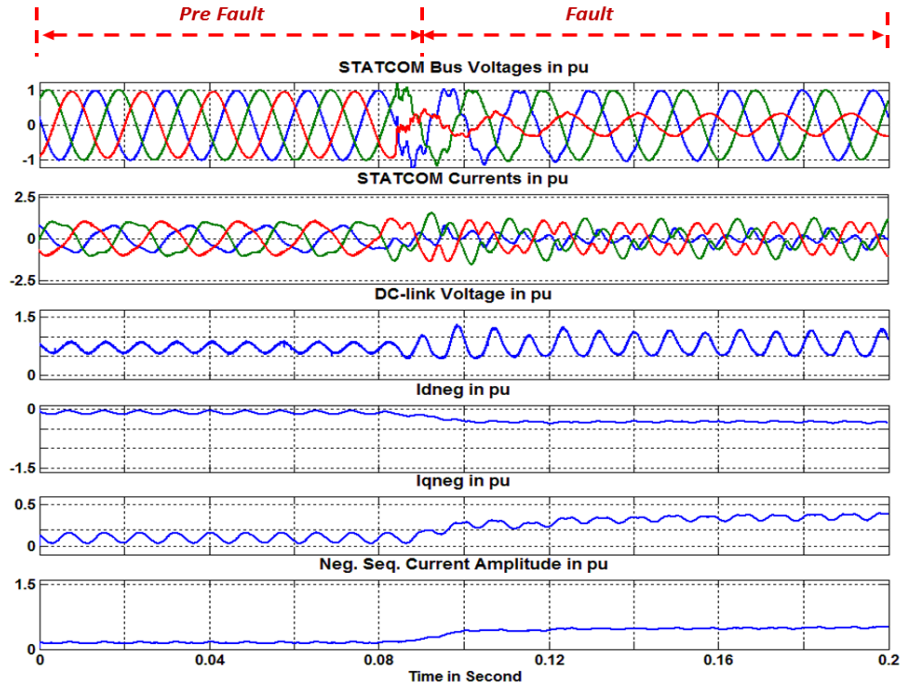


Figure 3-24. Inductive mode performance of STATCOM under single line to ground fault with (b) and without (a) DAC. All pu values are based on 12 VA and 100 V RMS (L-L) ac system. (Experimental results)

STATCOM with proposed controller. The STATCOM performance under fault conditions in inductive mode with and without the DAC is shown in Figure 3-24. As can be observed in this figure, the negative sequence current is well limited by the proposed controller and reaches form 1.5 pu to around 0.2 pu. This reduction in negative sequence current results in dramatic fault peak current reduction from around 2.5 pu to around 1pu. The DC-link voltage 2^{nd} harmonic oscillations are well limited as well and STATCOM fault current THD changes from 15% to 11%.

Note that the structure of the DAC is based on multiplying the amplitude of the 2^{nd} harmonic oscillations of the q-axis component of the tie line current in the positive synchronous frame (Iq+) by the output of the negative sequence PI controller and injecting the obtained signal as α_{ac} to generate required fundamental negative sequence voltage vector at the VSC output terminals to limit the negative sequence current. This 2^{nd} harmonic oscillation of Iq+ only exists when there is negative sequence current flow on the STATCOM tie line (equation (3-35)). In other word, the DAC uses the 2^{nd} harmonic signals in the positive synchronous frame, made by the fault condition, to make its output (α_{ac}) to limit the negative sequence current. At steady state, finally the system reaches to an equilibrium point at which the negative sequence current is reduced to a low steady-state value. This negative sequence current reduction is because of the steady-state negative sequence voltage at VSC output terminals which is generated by the non-zero steady-state α_{ac}.

3. 7 Summary

This chapter proposed a control structure to improve the *angle-controlled* STATCOM performance under utility unbalanced conditions and system faults. The main improvement is to significantly decrease the negative sequence current and DC-link voltage oscillations under power system faults through control. This makes it unnecessary to constrain the choice of power component to achieve this desired reduction. The proposed structure is designed based on adding an appropriate oscillation (α_{ac}) to the conventional *Angle-controller* output (angle α). The angle α is the angle by which the inverter voltage vector leads/lags the line voltage vector. The angle α_{ac} is controlling the DC-link voltage oscillations with twice the line frequency to generate the required negative sequence voltages at VSC output terminals to attenuate the effects of the postulated negative sequence bus voltage. This generated negative sequence voltage results in reduction of the negative sequence current seen by the STATCOM. Since this control structure is using two angles for controlling VSC output voltage, it is called *Dual Angle Control (DAC)* strategy. PSCAD/EMTDC results verified the validity of the proposed control structure. Finally, experimental results form a very unique hardware confirmed the predicted theoretical and simulation results.

APPENDIX

3. 8 Appendix (3-A)

The 2nd harmonic oscillations of the q component of STATCOM current in positive synchronous frame due to negative sequence current was calculated as in (3-35). As discussed in section (3.4), injecting 2nd harmonic oscillations in phase with signal of equation (3-35) as α_{ac}, generates a 90˚ leading 2nd harmonic oscillation at DC-link voltage as:

$$A\,cos\left(2\omega t-\frac{\pi}{2}-\theta_i^-\right) \tag{3-36}$$

As discussed in section (3.3), interaction between VSC switching function and DC-Link voltage oscillations of equation (3-36) generates a negative sequence voltage as in (3-37) at the STATCOM terminal. Positive and negative signs are related to negative sequence current initial phase with respect to STATCOM bus negative sequence voltage ($\theta_i^- \approx \theta_v^- \pm \frac{\pi}{2}$).

$$\pm A' sin(-\omega t+\alpha+\theta_v^-) \tag{3-37}$$

Considering that α is almost zero, the negative sequence voltage of the equation (3-37) is in the same phase as postulated STATCOM bus negative sequence voltage source under fault conditions.

Chapter4: DC-side Series Active Power Filter for STATCOM Performance under System Faults

4.1 Introduction

The combination of increasing electric power demand and restriction in the transmission system expansion makes the development and application of power electronics based controller for power system a high priority[32]. VSC-based STATCOM is a voltage regulating device used on the AC-power system. It is controlling the voltage of the bus which is connected to by acting as either sink or source of the reactive power to the grid. The angle-controlled STATCOM is tailored to minimizing the switching losses for the transmission level applications. Unlike the PWM-controlled STATCOM It is switched at line frequency to achieve lower system losses. The first such installation was ±100 MVAr STATCOM at TVA Sullivan substation [34]. This was followed by the NYPA installation of a FACTS controller, known as the Convertible Static Compensator (CSC), at the Marcy 345 kV substation in New York State. Two 100 MVA VSCs are connected to the system through shunt and series transformers. This arrangement of the converters allows STATCOM, SSSC, UPFC, or IPFC deployment at the bus and two of the lines exiting the substation. The operation of the STATCOMs and shunt converter in the UPFC mode is based on angle-controller strategy [30]. 150 MVA STATCOM at Laredo and Brownsville substation at Texas, 160 MVA STATCOM at Inez substation in Eastern Kentucky, 43 MVA PG&E Santa Cruz STATCOM and 40 MVA KEPCO (Korea Electric Power Corporation) STATCOM at Kangjin substation in South Korea are few examples of the other angle-controlled STATCOMs.

High quality output voltage of this kind of STACOM is provided by line-frequency-switched pulse inverters. 24-pulse and 48-pulse inverters are commonly used for this kind of STATCOM at the transmission level since the current THD is around 1-2% with low overall converter losses. The operation of the angle-controlled STATCOM is based on controlling only the angle of the output voltage vector (α). It has been shown in [19] that by a slight change of the inverter output voltage vector angle (α) , the inverter is able to provide inductive/capacitive reactive power. In this type of inverter, the VSC output voltage magnitude is varied indirectly by changing the DC bus voltage. The control structure of the angle-controlled STATCOM is depicted in Figure 4-1.

Angle-controlled STATCOM performance under unbalanced conditions and system faults is an important issue. Basically, there are two challenges. One is the second harmonic oscillations that appear on the dq positive synchronous frame control signals due to the negative-sequence signals. It is possible to get rid of these 2^{nd} harmonic disturbances using the rejection notch filters at twice the line frequency. The other challenge is the large negative-sequence current that flows to the converter. This negative-sequence current generates 2^{nd} harmonic oscillations on the DC-link. The protection system will trip the STATCOM either due to the STATCOM over current (to protect the converter switches) or because of the over/under voltage on the DC-bus due to the large DC-bus 2^{nd} harmonic oscillations. Therefore, the STATCOM is not able to fulfill its reactive power support functionality under unbalanced conditions and system faults when it might be needed the most. Apart from that, it will take several fractions of an hour to start up the tripped STATCOM.

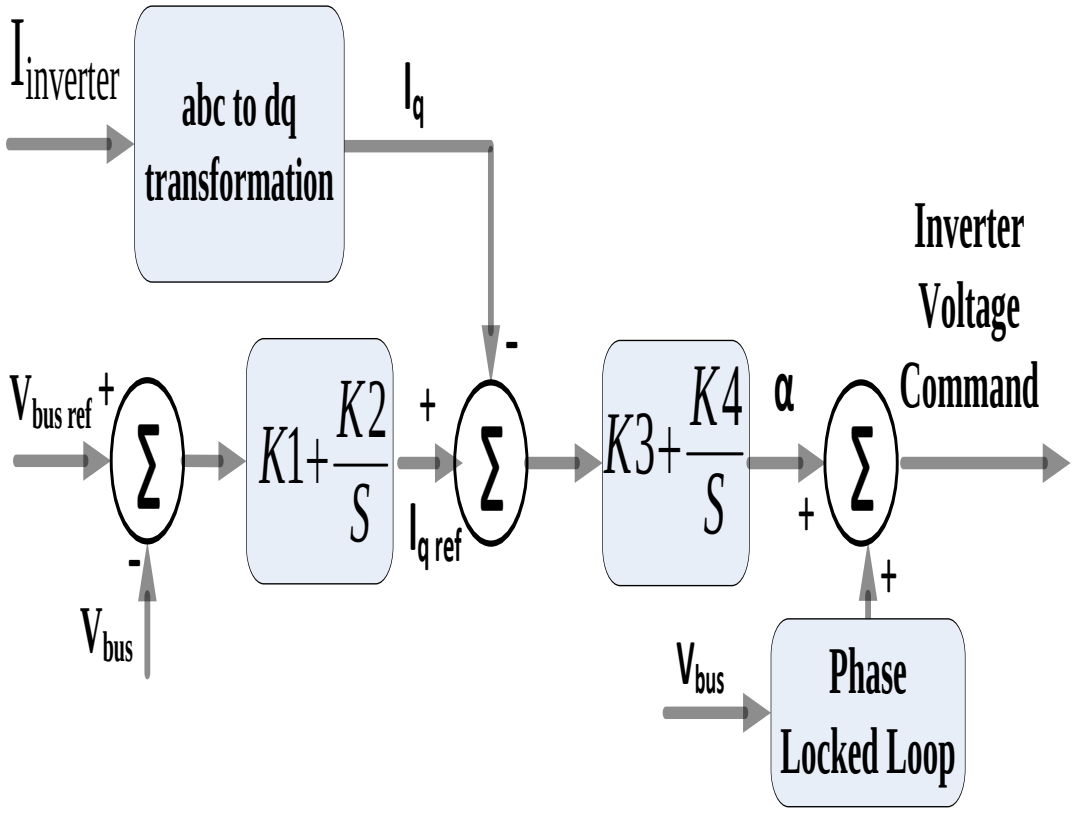


Figure 4-1. Control structure of an angle-controlled STATCOM

Many different control structures have been proposed by researchers to improve the VSC performance under fault conditions [36]-[54], and [56]-[61]. These are focused on mainly generating the current reference in both positive and negative synchronous frame to regulate the power or voltage at the PCC [49].However, all these methods are based on direct controlling both the angle and magnitude of the VSC output voltage and are not applicable for angle-controlled STATCOMs with only one control input angle (α).

This chapter presents a solution to limit the STATCOM negative-sequence current under unbalanced condition and system faults. This is achieved by adding a single phase inverter in

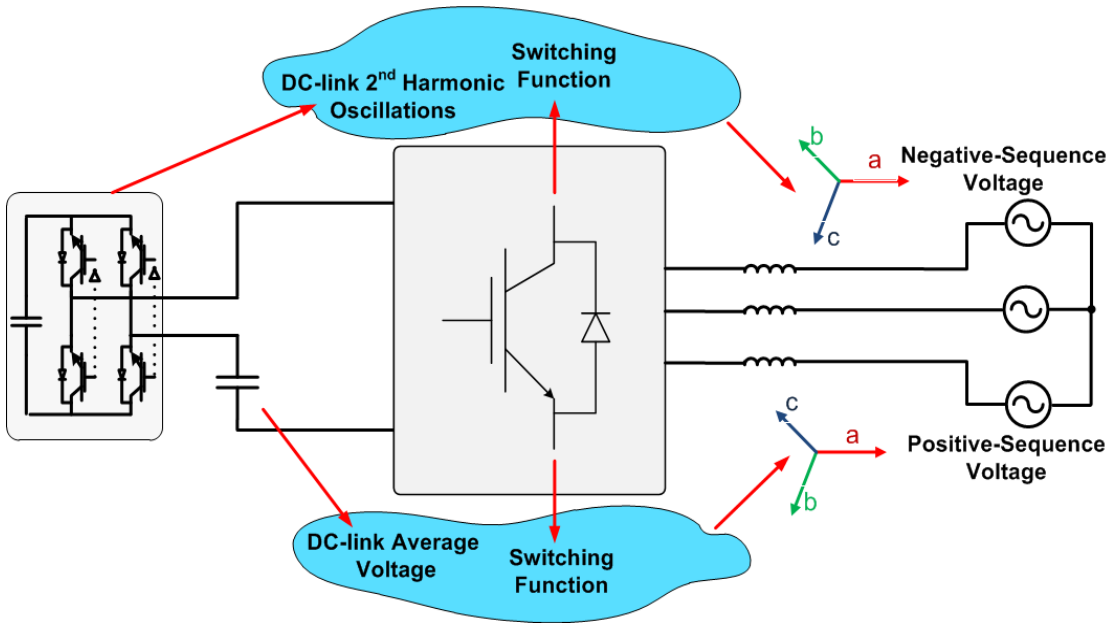


Figure 4-2. Simultaneous and independent control of positive and negative-sequence voltages

series with the DC-link capacitor. This inverter generates controllable 2nd harmonic oscillations with appropriate phase and amplitude. The interaction between the VSC switching function and the single phase inverter 2nd harmonic oscillations generates required negative-sequence voltage at the VSC output terminals to force the STATCOM negative-sequence current to zero. By adding the single phase inverter, it is possible to control both the positive and negative-sequence voltage at the VSC output terminals. The positive-sequence controller regulates the positive-sequence voltage by changing the average of the DC-link voltage while the negative-sequence controller regulates the negative-sequence voltage by controlling the phase and amplitude of the DC-link voltage 2nd harmonic oscillations. This idea is conceptually illustrated in Figure 4-2.

In this chapter, following the introduction, VSC voltage and current under fault conditions are calculated. Then, the equations that describe the dynamics of the STATCOM negative-sequence current are calculated in detail. These equations are used to develop the proposed control structure. The validity of the proposed solution is supported by the precise PSCAD/EMTDC simulation of the NYPA 48-pulse STATCOM.

4.2 VSC under unbalanced conditions

Symmetrical component are most commonly used for analysis of three-phase unbalanced electrical systems. In this method a set of unbalanced three phase phasor is split into two symmetrical positive and negative-sequences and one zero-sequence component. Based on this theory, tie line currents of the STATCOM in Figure 4-3 under fault condition will be as:

$$i_a = i_a^+ + i_a^- + i_a^0 \tag{4-1}$$

$$i_a = i^+ \sin(\omega t + \theta_i^+) + i^- \sin(\omega t + \theta_i^-) + i^0 \sin(\omega t + \theta_i^0) \tag{4-2}$$

$$i_b = i^+ \sin\left(\omega t + \theta_i^+ - \frac{2\pi}{3}\right) + i^- \sin\left(\omega t + \theta_i^- + \frac{2\pi}{3}\right) + i^0 \sin(\omega t + \theta_i^0) \tag{4-3}$$

$$i_c = i^+ \sin\left(\omega t + \theta_i^+ + \frac{2\pi}{3}\right) + i^- \sin\left(\omega t + \theta_i^- - \frac{2\pi}{3}\right) + i^0 \sin(\omega t + \theta_i^0) \tag{4-4}$$

The zero-sequence current flow to the STATCOM tie line can be prevented using appropriate transformer configuration. As it was mentioned earlier, the only control input of the angle-controlled STATCOM is the angle α, which is always applied identically to all three phases of the inverter. Therefore, the switching function for an angle-controlled STATCOM is always symmetric. By neglecting all the voltage harmonics except the

fundamental (which is a fair assumption for a 24 and 48-pulse inverter due to output voltage THD typically around 3%) the switching function for phase a, b, and c can be represented as:

$$s_a = K\,sin(\omega t + \alpha) \tag{4-5}$$

$$s_b = K\,sin\left(\omega t + \alpha - 2\frac{\pi}{3}\right) \tag{4-6}$$

$$s_c = K\,sin\left(\omega t + \alpha + 2\frac{\pi}{3}\right) \tag{4-7}$$

where K is the factor for the inverter which relates the DC-side voltage to the amplitude of the phase to neutral voltage at the inverter AC-side terminals. α is the angle by which the inverter voltage vector leads/lags the line voltage vector. Then the inverter terminal fundamental voltage is calculated as:

$$e_a = K\,v_{DC}\,sin(\omega t + \alpha) \tag{4-8}$$

$$e_b = K\,v_{DC}\,sin\left(\omega t + \alpha - 2\frac{\pi}{3}\right) \tag{4-9}$$

$$e_c = K\,v_{DC}\,sin\left(\omega t + \alpha + 2\frac{\pi}{3}\right) \tag{4-10}$$

The interaction between the fundamental frequency inverter switching function and the negative-sequence component of the current produces 2nd harmonic oscillations on the DC-link voltage and current [39], [40]. Therefore, the general expression of DC-link voltage during unbalanced condition becomes:[37]

$$v_{DC} = V_{dc} + V_{dch2}\cos(2\omega t + \theta_v^{dc}) \tag{4-11}$$

where V_{dc} is the average value and V_{dch2} is the amplitude of the 2nd harmonic oscillations of DC-Link voltage. Substituting (4-11) in (4-8)-(4-10), the inverter output voltages when the DC-link voltage is distorted by 2nd harmonic oscillations due to the unbalanced AC system are calculated as:

$$e_a = \mathrm{K}\,V_{dc}\sin(\omega t + \alpha) + \frac{KV_{dch2}}{2}\sin\left(3\omega t + \alpha + \theta_v^{dc}\right) + \frac{KV_{dch2}}{2}\sin(-\omega t + \alpha - \theta_v^{dc}) \quad (4\text{-}12)$$

$$e_b = \mathrm{K}\,V_{dc}\sin\left(\omega t + \alpha - 2\frac{\pi}{3}\right) + \frac{KV_{dch2}}{2}\sin\left(3\omega t + \alpha + \theta_v^{dc} - 2\frac{\pi}{3}\right) + \frac{KV_{dch2}}{2}\sin(-\omega t + \alpha - \theta_v^{dc} - 2\frac{\pi}{3}) \quad (4\text{-}13)$$

$$e_c = \mathrm{K}\,V_{dc}\sin\left(\omega t + \alpha + 2\frac{\pi}{3}\right) + \frac{KV_{dch2}}{2}\sin\left(3\omega t + \alpha + \theta_v^{dc} + 2\frac{\pi}{3}\right) + \frac{KV_{dch2}}{2}\sin(-\omega t + \alpha - \theta_v^{dc} + 2\frac{\pi}{3}) \quad (4\text{-}14)$$

Equations (4-12)-(4-14) show that the interaction between switching function and the DC-link voltage 2nd harmonic oscillations generates fundamental negative-sequence voltage at the VSC output terminals. Basically, the unbalanced AC- system conditions can be emulated by postulating a set of negative-sequence voltage source in series with STATCOM tie line [19]. The basic idea of the proposed solution is to generate required fundamental negative-sequence voltage vector at the VSC output terminals to attenuate the effect of postulated negative-sequence bus voltage under fault condition. The generated negative-sequence voltage results in a reduction of the negative-sequence current seen by the STATCOM. It is important to note that interaction between the switching function and the DC-link voltage 2nd harmonic oscillations also generates a 3rd harmonic voltage at the VSC output terminals.

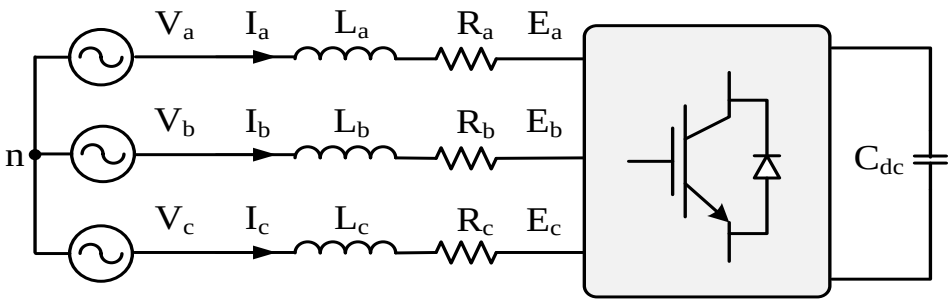


Figure 4-3. Equivalent circuit of a VSC connected to AC system.

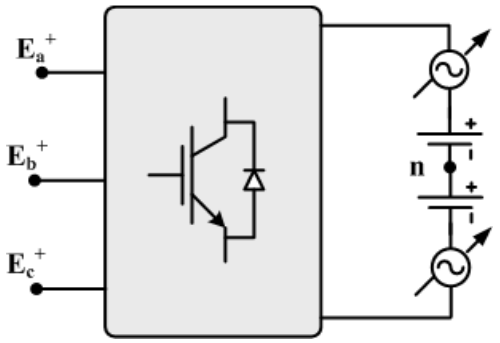


Figure 4-4. Equivalent circuit of the inverter used for calculation of the fundamental negative-sequence voltage vector at VSC output terminals.

This 3rd harmonic voltage is positive-sequence and phase a, b, and c are 120 degree apart. Basically, the negative-sequence current flow due to unbalanced AC-system condition generates the 2nd harmonic oscillations on the DC-link voltage. These oscillations generate fundamental negative-sequence voltage and 3rd harmonic voltage at the VSC terminals. Similar to the fundamental negative-sequence voltage, the amplitude of this 3rd harmonic voltage is decided by the DC-link voltage 2nd harmonic oscillations. This chapter will show that by controlling 2nd harmonic oscillations on the DC-link voltage the negative-sequence current will reduce significantly. Decreased negative-sequence current will inherently reduce

Table 4-1: calculation and simulation results of one three level NPC 48-pulse inverter

DC Bus Voltage (KV)	Pos. Seq. Fundamental Theory (kV)	Neg. Seq. Fundamental Theory (kV)	Pos. Seq. Fundamental Simulation (kV)	Neg. Seq. Fundamental Simulation (kV)
v_{DC}=12+1sin(2wt)	345	14.37	342.5	14.23
v_{DC}=12+2sin(2wt)	345	28.75	342.5	28.46
v_{DC}=12+3sin(2wt)	345	43.12	342.5	42.78
v_{DC}=12+4sin(2wt)	345	57.50	342.5	56.9
v_{DC}=12+5sin(2wt)	345	71.87	342.5	70.25

the DC-link voltage 2nd harmonic oscillations. Reduction in the DC-link voltage 2nd harmonic oscillations results in decrease in the 3rd harmonic voltage and consequently current at STATCOM tie line.

The negative-sequence voltage calculated in equation (4-12)-(4-14) was verified with PSCAD/ EMTDC simulation of a three-level Neutral Point Clamped (NPC) based 48-pulse inverter. The DC-side of the inverter is supplied from two series connected 6 kV DC voltage sources in series with two variable AC voltage sources as shown in Figure 4-4. The AC-side is left open circuit. Table 4-1 compares the theoretical value of the positive and negative-sequence output voltage with simulation results. In the first row, for example, the inverter output negative-sequence voltage according to equation (4-12) is $\frac{345}{12\times2}\times 1 = 14.37\ kV$ which perfectly matches with simulation results. Figure 4-5 indicates the harmonic content of the inverter output voltage with two different values of 2nd harmonic oscillations added to the DC-link and compares them with base case i.e. without any oscillations on the DC-link voltage. As can be observed in this figure, with different 2nd harmonic oscillation on the DC-bus the fundamental voltage remains unchanged. The change in the other harmonics,

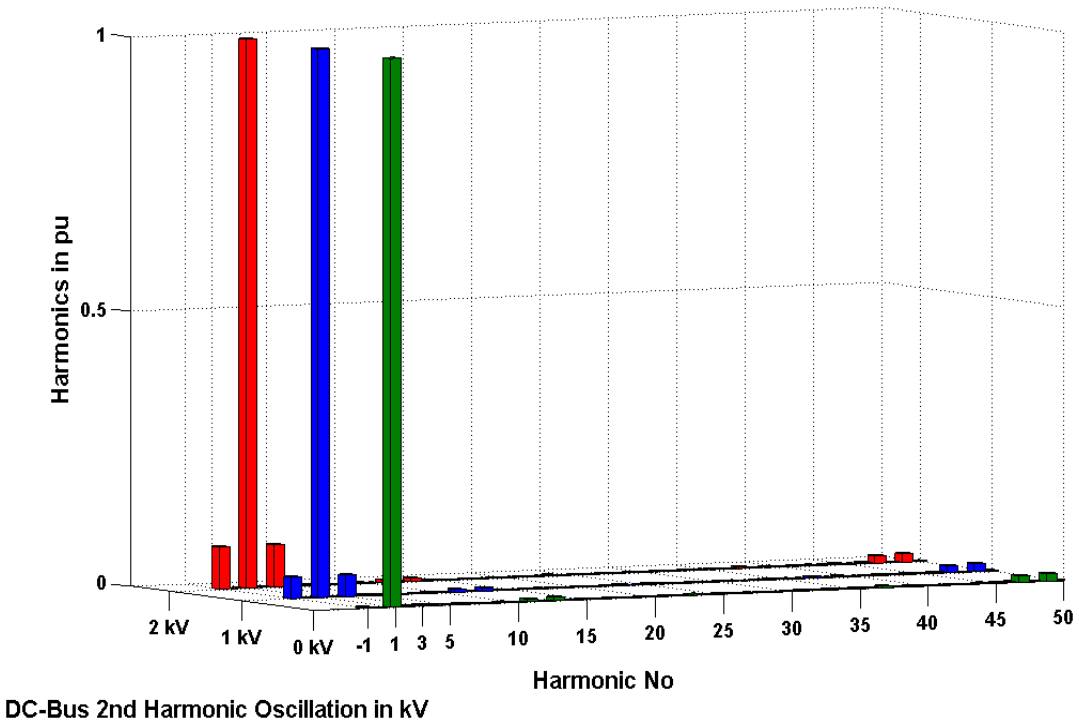


Figure 4-5. 48-pulse inverter output voltage harmonic content with different 2nd harmonic oscillations added to the DC-link voltage.

excluding the 3rd harmonic and negative-sequence voltage, is also negligible. This idea of generating desirable negative-sequence voltage vector by controlling the DC-link voltage 2nd harmonic oscillations has been used in this paper to develop the proposed controller.

4.3 Proposed Control Structure Development

4.3.1 Derivation of STATCOM equations in the negative synchronous frame

As discussed in the previous section, STATCOM voltage and current during unbalanced conditions can be calculated by postulating a set of negative-sequence voltage in series with the STATCOM tie line as shown in Figure 4-6. Negative-sequence current at STATCOM

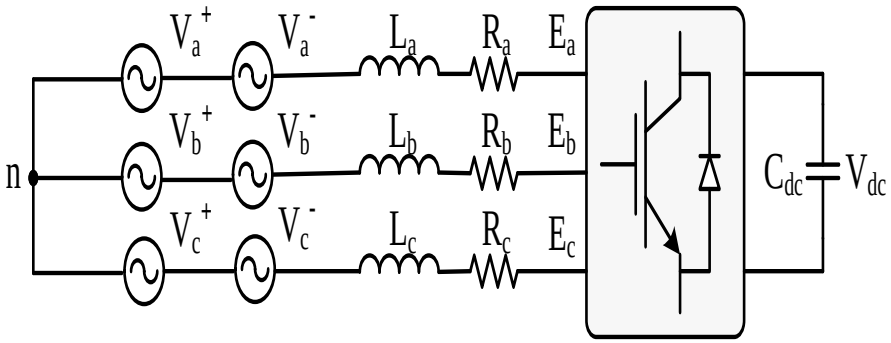


Figure 4-6. STATCOM equivalent circuit with series negative-sequence voltage sources

tie line generates 2nd harmonic oscillations at the DC-link voltage. These 2nd harmonic oscillations generate the negative-sequence voltage at STATCOM terminals as calculated in (4-12)-(4-14). Assuming 2nd harmonic oscillation at DC-link voltage as:

$$V_{dch2}\cos(2\omega t + \alpha') \tag{4-15}$$

Then generated negative-sequence voltages at STATCOM terminal are calculated as in (4-16)-(4-18).

$$e_a^- = \frac{KV_{dch2}}{2}\sin(-\omega t + \alpha - \alpha') \tag{4-16}$$

$$e_b^- = \frac{KV_{dch2}}{2}\sin(-\omega t + \alpha - \alpha' - \frac{2\pi}{3}) \tag{4-17}$$

$$e_c^- = \frac{KV_{dch2}}{2}\sin(-\omega t + \alpha - \alpha' + \frac{2\pi}{3}) \tag{4-18}$$

The derivative of STATCOM tie line negative-sequence currents with respect to time are calculated as in (4-19)-(4-21).

$$\frac{di_a^-}{d_t} = \frac{-R}{L} i_a^- + \frac{(e_a^- - V_a^-)}{L} \quad (4\text{-}19)$$

$$\frac{di_b^-}{d_t} = \frac{-R}{L} i_b^- + \frac{(e_b^- - V_b^-)}{L} \quad (4\text{-}20)$$

$$\frac{di_c^-}{d_t} = \frac{-R}{L} i_c^- + \frac{(e_c^- - V_c^-)}{L} \quad (4\text{-}21)$$

Transformation from abc to negative synchronous frame is defined as: [28]

$$f_{dq}^- = T(-\omega t) f_{abc}^- \quad (4\text{-}22)$$

where:

$$T(-\omega t) = \frac{2}{3}\begin{bmatrix} \cos(-\omega t) & \cos(-\omega t - \frac{2\pi}{3}) & \cos(-\omega t + \frac{2\pi}{3}) \\ -\sin(-\omega t) & -\sin(-\omega t - \frac{2\pi}{3}) & -\sin(-\omega t + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \quad (4\text{-}23)$$

and ωt is the STATCOM ac-bus phase locked loop output.

Figure 4-7 illustrates the instantaneous negative-sequence STATCOM bus (v^-) and inverter output voltage (e^-) in the negative synchronous frame. Vector v^- is assumed to have an arbitrary angle of Θ'. The d and q components of these two vectors are calculated as:

$$e_d^- = |e^-| \cos(\alpha - \alpha') = \frac{KV_{dch2}}{2} \cos(\alpha - \alpha') \quad (4\text{-}24)$$

$$e_q^- = |e^-| \sin(\alpha - \alpha') = \frac{KV_{dch2}}{2} \sin(\alpha - \alpha') \quad (4\text{-}25)$$

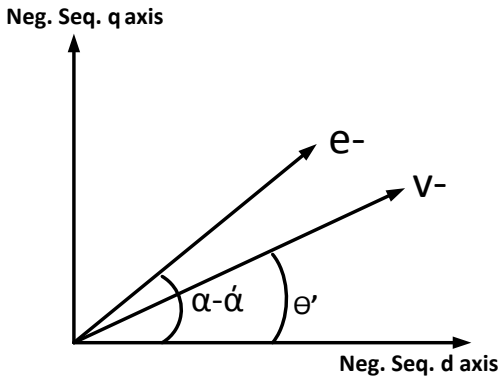


Figure 4-7. STATCOM instantaneous vectors in the negative synchronous frame

$$v_d^- = |v^-|\cos(\theta') \tag{4-26}$$

$$v_q^- = |v^-|\sin(\theta') \tag{4-27}$$

Transforming equation (4-19)-(4-21) based on (4-23), we find:

$$\frac{d}{dt}i_d^- = \frac{-R}{L}i_d^- - \omega i_q^- + \frac{K}{2L}V_{dch2}\cos(\alpha - \alpha') - \frac{1}{L}v_d^- \tag{4-28}$$

$$\frac{d}{dt}i_q^- = \frac{-R}{L}i_q^- + \omega i_d^- + \frac{K}{2L}V_{dch2}\sin(\alpha - \alpha') - \frac{1}{L}v_q^- \tag{4-29}$$

Equation (4-28) and (4-29) describe the dynamics of the VSC AC-side negative-sequence current, in terms of negative synchronous frame variables and 2nd harmonic oscillations of the DC-link voltage. These equations show that the dynamics of the STATCOM tie line negative-sequence current d and q components (i_d^- , i_q^-) are related to the phase and amplitude of the DC-link voltage 2nd harmonic oscillations.

4.3.2 Proposed Controller

As discussed, the proposed solution is based on adding a single phase inverter in series with DC-bus. This inverter generates controllable 2nd harmonic oscillations with appropriate

phase and amplitude. These oscillations generate negative- sequence voltage at STATCOM output terminals. Generated negative-sequence voltage reduces the negative-sequence current seen by the STATCOM. Attention should be taken that the single phase inverter is sized for the DC-link voltage 2nd harmonic rather than the DC-link average voltage. Single phase inverter design issues have been discussed in the following section of this paper. This part of the paper presents the control structure used to calculate the required reference amplitude and phase for the single phase inverter to limit the STATCOM negative-sequence current.

As discussed in section (4.3), adding a 2nd harmonic oscillation of equation (4-15) into the DC-link voltage will generate negative-sequence voltage of equation (4-16)-(4-18) at VSC output terminals. The objective of the controller is to calculate the desirable amplitude (V_{dch2}) and phase (α') of the DC-link voltage 2nd harmonic oscillations which force the STATCOM negative-sequence currents to zero. Two PI controllers are used to regulate the d and q components of the STATCOM negative-sequence current in the negative synchronous frame (i_d^- , i_q^-). A rejection notch filter at double the line frequency has been added to the measured current in the negative synchronous frame to isolate the negative- sequence controller from the positive-sequence signals. The reference values for the i_d^- and i_q^- are set to zero. The outputs of these two PI controllers are the required negative-sequence voltage vector d and q components (e_d^-, e_q^-) in the negative synchronous frame at VSC output terminals to achieve zero negative-sequence current flow. Having calculated e_d^- and e_q^-, V_{dch2} and α' are calculated as:

$$V_{dch2} = \frac{2}{K}\sqrt{{e_d}^{-2} + {e_q}^{-2}} \tag{4-30}$$

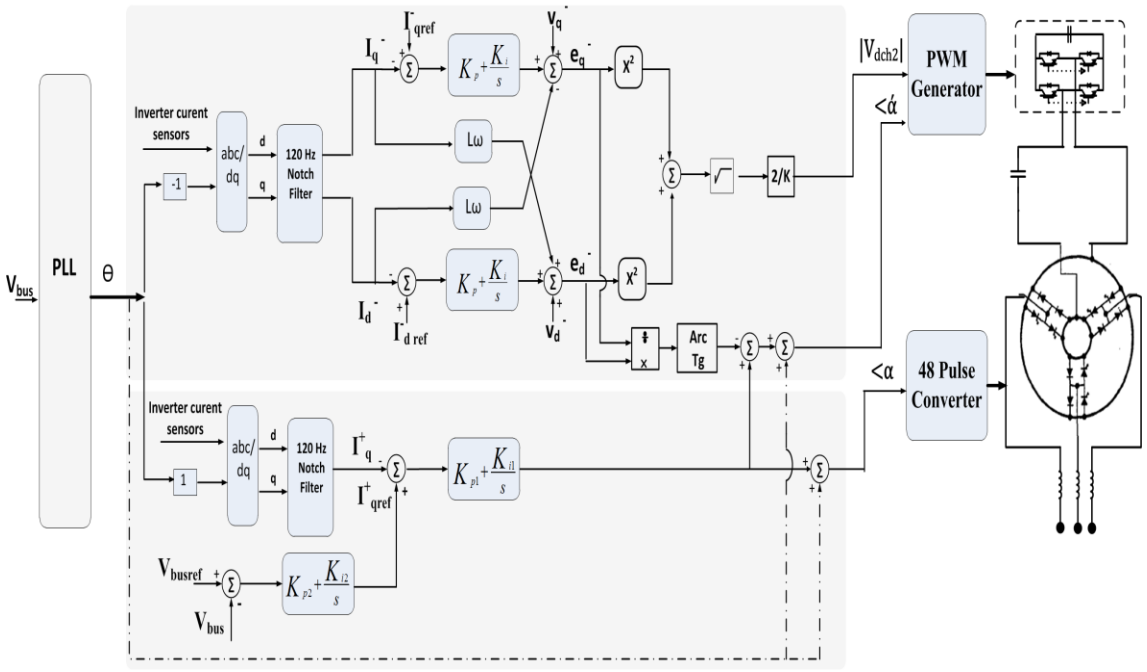


Figure 4-8. Control Structure

$$\alpha' = \alpha - \tan^{-1}\frac{e_q^-}{e_d^-} \tag{4-31}$$

The proposed control structure is illustrated in Figure 4-8.

4.3.3 Controller Design Consideration

This part of the chapter discusses the controller design considerations to obtain a non-oscillatory and stable response. Equation (4-28) and (4-29) can be rewritten as in:

$$e_d^- = L\frac{d}{dt}i_d^- + Ri_d^- + L\omega i_q^- + v_d^- \tag{4-32}$$

$$e_q^- = L\frac{d}{dt}i_q^- + Ri_q^- - L\omega i_d^- + v_q^- \tag{4-33}$$

The coupling between the negative-sequence d and q components can be removed by adding proper terms to the controller output. Feed-forwarding the v_d^- and v_q^- to the controller

output also improves the converter dynamic performance. Hence, the general expression of $e^{-}_{d\,ref}$ and $e^{-}_{q\,ref}$ in the laplace domain can be written as:

$$e^{-}_{d\,ref} = \left(i^{-}_{dref} - i^{-}_{d}\right)\left(k_p + \frac{k_p}{T_i s}\right) + L\omega i^{-}_{q} + v^{-}_{d} \tag{4-34}$$

$$e^{-}_{q\,ref} = \left(i^{-}_{qref} - i^{-}_{q}\right)\left(k_p + \frac{k_p}{T_i s}\right) - L\,\omega i^{-}_{d} + v^{-}_{q} \tag{4-35}$$

These two equations show that the reference voltage of the single phase inverter can be split into two components. One of them is obtained from the PI controller and the other one is feed-forward term. Having added these feed-forward terms, then i^{-}_{d} and i^{-}_{q} become related to the e^{-}_{d} and e^{-}_{q} through a simple first order transfer function as in (4-36), and (4-37).

$$i^{-}_{d} = \frac{1}{R}\left(\frac{1}{1 + s\tau}\right)e^{-}_{d} \tag{4-36}$$

$$i^{-}_{q} = \frac{1}{R}\left(\frac{1}{1 + s\tau}\right)e^{-}_{q} \tag{4-37}$$

where:

$$\tau = \frac{L}{R} \tag{4-38}$$

From the control point of view a converter can be considered as an ideal power transformer with a time delay. The output voltage of the converter is assumed to follow a voltage reference signal with an average time delay due to the PWM switching. Hence, the general expression of the transfer function between the reference negative-sequence voltage and generated negative-sequence voltage will be as in[62]:

$$\frac{e_d(s)/e_q(s)}{e_{dref}(s)/e_{qref}(s)} = \left(\frac{1}{1 + sT_t}\right) \tag{4-39}$$

Where, T_t is the average time delay of the single phase inverter and is inversely proportional to its switching frequency. The d and q independent current control loop are shown inFigure 4-9. The open loop transfer function of the current controller is calculated as in (4-40).

$$G_{C,OL} = k_p\left(\frac{1+T_i s}{T_i s}\right)\left(\frac{1}{1+T_t s}\right)\frac{1}{R}\left(\frac{1}{1+\tau s}\right) \tag{4-40}$$

There are many different methods for tuning a PI controller [62]-[64]. For low order controlled plants the modulus optimum (absolute value optimum criterion) is often used in the conventional analog controller tuning because of its simplicity and fast response. When the controlled system has one dominant time constant and other minor time constant, the standard form of the control system transfer function for the modulus optimum is achieved by cancelling the largest time constant, while the closed loop gain should be larger than unity for as high frequencies as possible [62],[65]. The modulus optimum tuning criteria for this system gives the PI controller parameters as:

$$T_i = \tau \tag{4-41}$$

$$k_p = \frac{\tau R}{2T_t} \tag{4-42}$$

Therefore, the final open loop and close loop transfer function will be as follows:

$$G_{C,OL} = \frac{1}{2{T_t}^2 s^2 + 2T_t s} \tag{4-43}$$

$$G_{C,cL} = \frac{\frac{1}{2{T_t}^2}}{s^2 + \frac{1}{T_t}s + \frac{1}{2{T_t}^2}} \tag{4-44}$$

The closed loop transfer function is a simple second order system with natural frequency of $\omega_n = \frac{1}{\sqrt{2}\,T_t}$ and damping factor of $\frac{1}{\sqrt{2}}$. The response time with 2% criterion is $8T_t$. However, the real response time of the system is greater than eight times of the single phase inverter average delay. This is due to the filters that are used in the controller. Apart from the rejection notch filter at double the line frequency that are used to eliminate the effect of the fundamental positive-sequence signals, low pass filters should also be used to smooth the controller signals. These filters add a considerable delay and increase the system response time. In the real system implementation, non-ideal feedback also adds a delay to the system response time.

The notch filter passes all the frequencies except the notch frequency unaltered and attenuates the notch frequency to a very low level. It can be realized by multiplying two quadratic factors as calculated in:

$$\frac{s^2 + {\omega_n}^2}{s^2 + 2\zeta\omega_n s + {\omega_n}^2} \tag{4-45}$$

The damping factor (ζ) of the denominator is set to 0.5 to remove the overshoot at notch frequency (120 Hz) while, the numerator damping factor is set to zero to create a very strong undershoot at notch frequency. The final transfer function of the implemented notch filter is calculated as in:

$$\frac{s^2 + (2 \times \pi \times 120)^2}{s^2 + 2 \times \pi \times 120 s + (2 \times \pi \times 120)^2} \tag{4-46}$$

Figure 4-10 indicates the bode plots of the implemented notch filter.

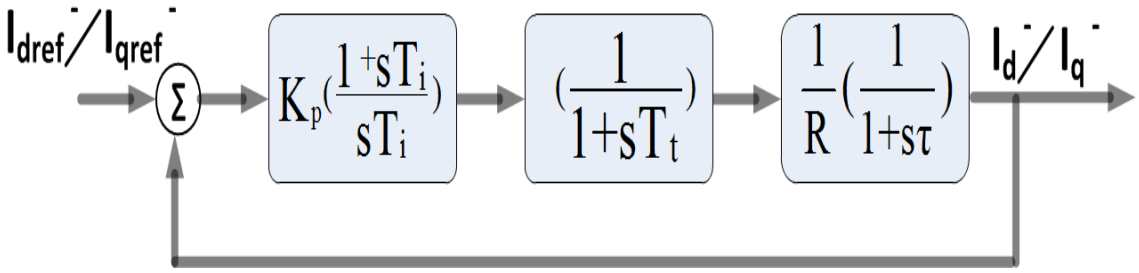


Figure 4-9. d and q current control loop [63]

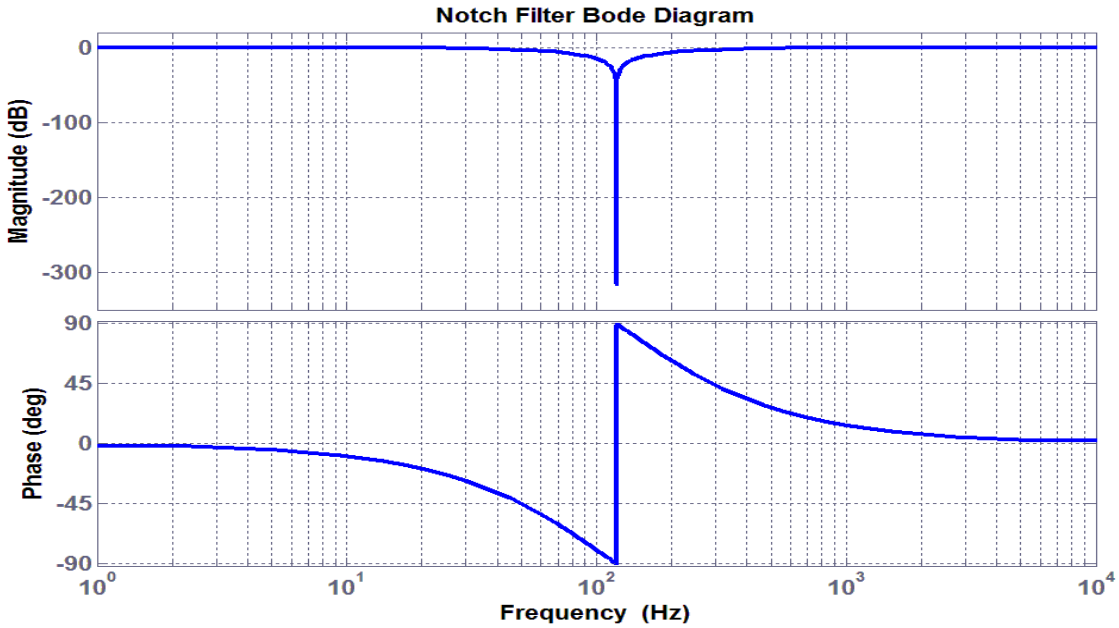


Figure 4-10. Notch filter bode plots

It is also important to note that the Phase Locked Loop (PLL) used in this simulation is deigned such that it only follows the positive-sequence voltage. Therefore, the AC-system unbalanced conditions do not affect the PLL performance[66],[67]. The Block diagram of the PLL is illustrated in Figure 4-11.

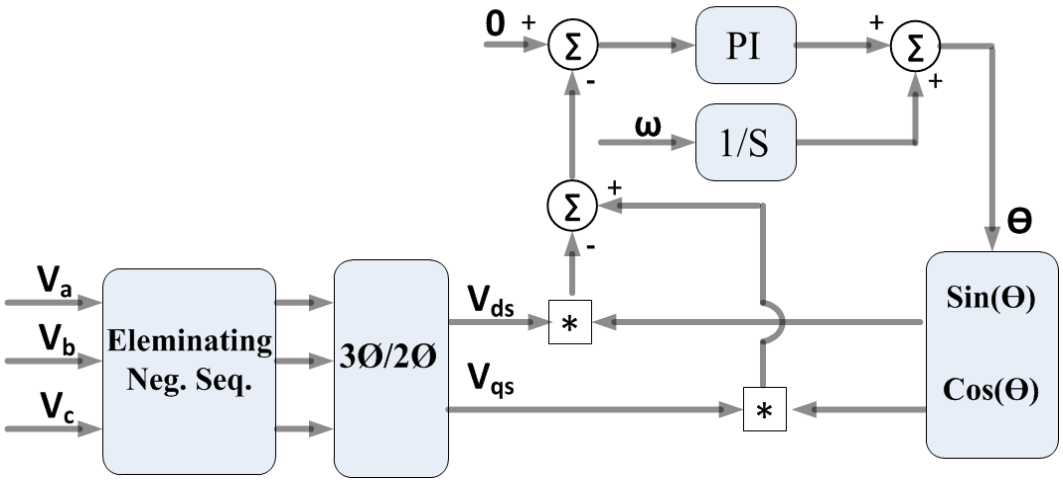


Figure 4-11. Block diagram of the Phase Locked Loop

4.4 PSCAD simulation results

To verify the proposed solution, 100 MVA, 345 kV, 48-pulse STATCOM at the NYPA Marcy substation has been simulated in PSCAD with all the details as shown in Figure 4-12.The structure of this STATCOM has already been described in the chapter 2 and only a brief outline is given here. The VSC consists of 4 three level Neutral Point Clamped (NPC) three phase inverters (A1, B1, C1), (A2, B2, C2), (D1, E1, F1), and (D2, E2, F2). Their square wave outputs are combined electromagnetically to generate a 48-pulse output voltage waveform and their DC sides are connected to a common DC-bus. The output voltages of the three level NPC poles are combined through auxiliary and shunt transformers. The primary winding of the auxiliary transformer is doubly fed open wye winding with 11.9 kV rated voltage across the winding. The secondary winding is doubly fed open zigzag winding with the same voltage rating as the primary winding i.e. 11.9 kV. The voltage across the secondary leads the primary by 30 degree. The shunt transformer aids in voltage waveform

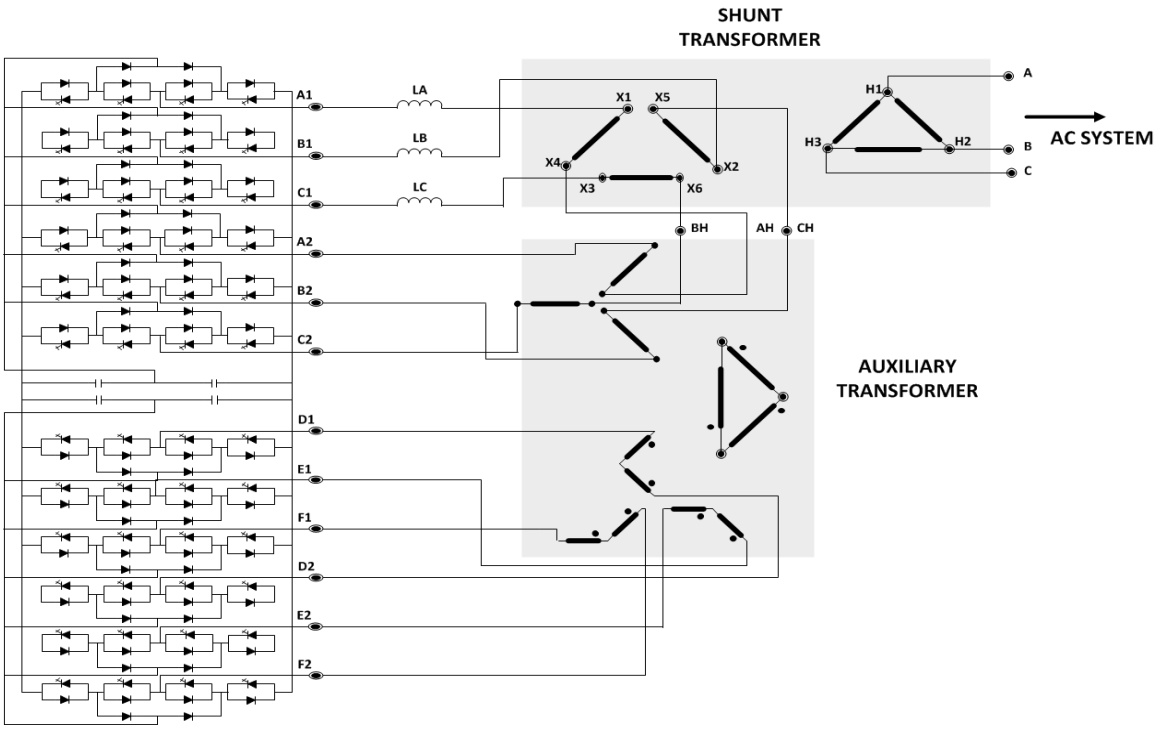


Figure 4-12. Power circuit of the NYPA three-level NPC 48-pulse inverter

construction and serves to couple the synthesized voltage to the 345 kV transmission system. The shunt transformer has standard delta connected primary windings rated 345 kV, and open delta secondary windings rated 21.4 kV across the winding [30].The AC-system zero-sequence current, in case of ground faults in the AC-system, is filtered out by the primary winding delta connection. Therefore, the AC-system zero-sequence current does not flow on the STATCOM tie line. The detailed description of the 48-pulse inverter along with its output voltage harmonic analysis has already been discussed in the chapter 2 of this thesis.

Figure 4-13 presents the 48-pulse output voltage of this inverter when the DC-link voltage is not connected to the single-phase inverter. This is the same inverter that was used to obtain the results in Table 1, and Figure 4-5. The DC-side series single phase inverter

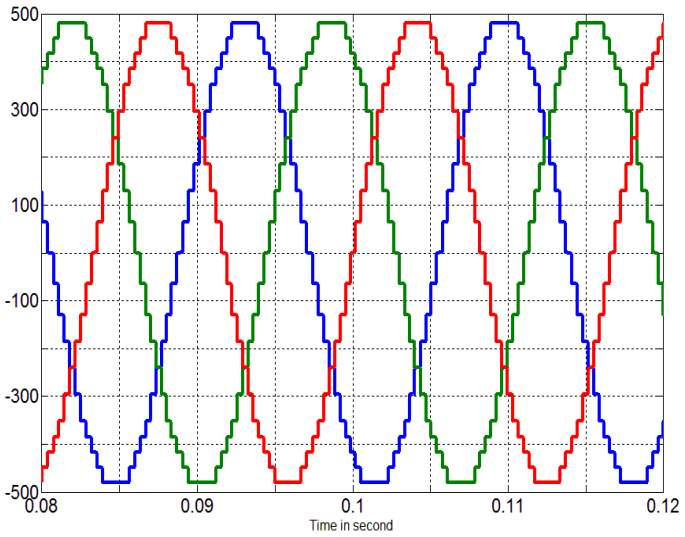


Figure 4-13. The 48-pulse output voltage when the DC-link is not connected to the single phase inverter.

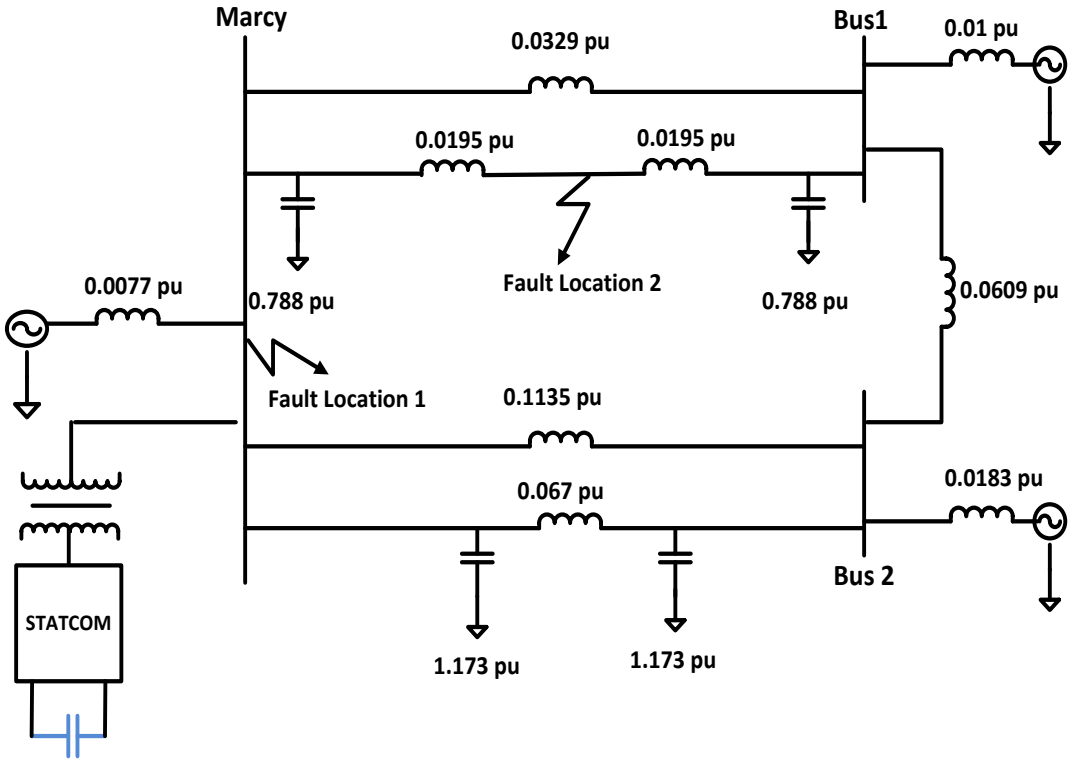


Figure 4-14. NYPA 3-bus AC system

along with proposed control structure has been added to the NYPA STATCOM model. This STATCOM is connected to the 3-bus 345 kV AC-system model of the New York Power Authority as shown in Figure 4-14. Table 4-2 summarizes the simulated system parameters.

Table 4-2: Simulation parameters

Parameters	Values
Frequency	*60 Hz*
Source voltages (LL)	*345 kV*
STATCOM Capacitor	*1000 μF*
STATCOM tie line resistance	*2 ohm*
STATCOM tie line inductance	*5 mH*
DC-link Voltage	*12 kV*

In this part of the chapter, different types of the AC-faults are applied at different locations of the 3-bus AC-system and the controller capability to limit the negative-sequence current is analyzed in detail.

Figure 4-15-(a) illustrates the STATCOM performance with and without the proposed solution under a Single Line to Ground (SLG) fault condition. The fault is applied right at the STATCOM bus (fault location 1 in Figure 4-14). The STATCOM works in capacitive mode of operation and injects 100 MVAr reactive power to the grid. At t=0.3, the SLG fault is applied at phase a while the STATCOM works with the conventional controller. At t=0.45, the STATCOM switches to work with the proposed controller. As can be observed in this figure, immediately after the proposed controller starts to work, the negative-sequence

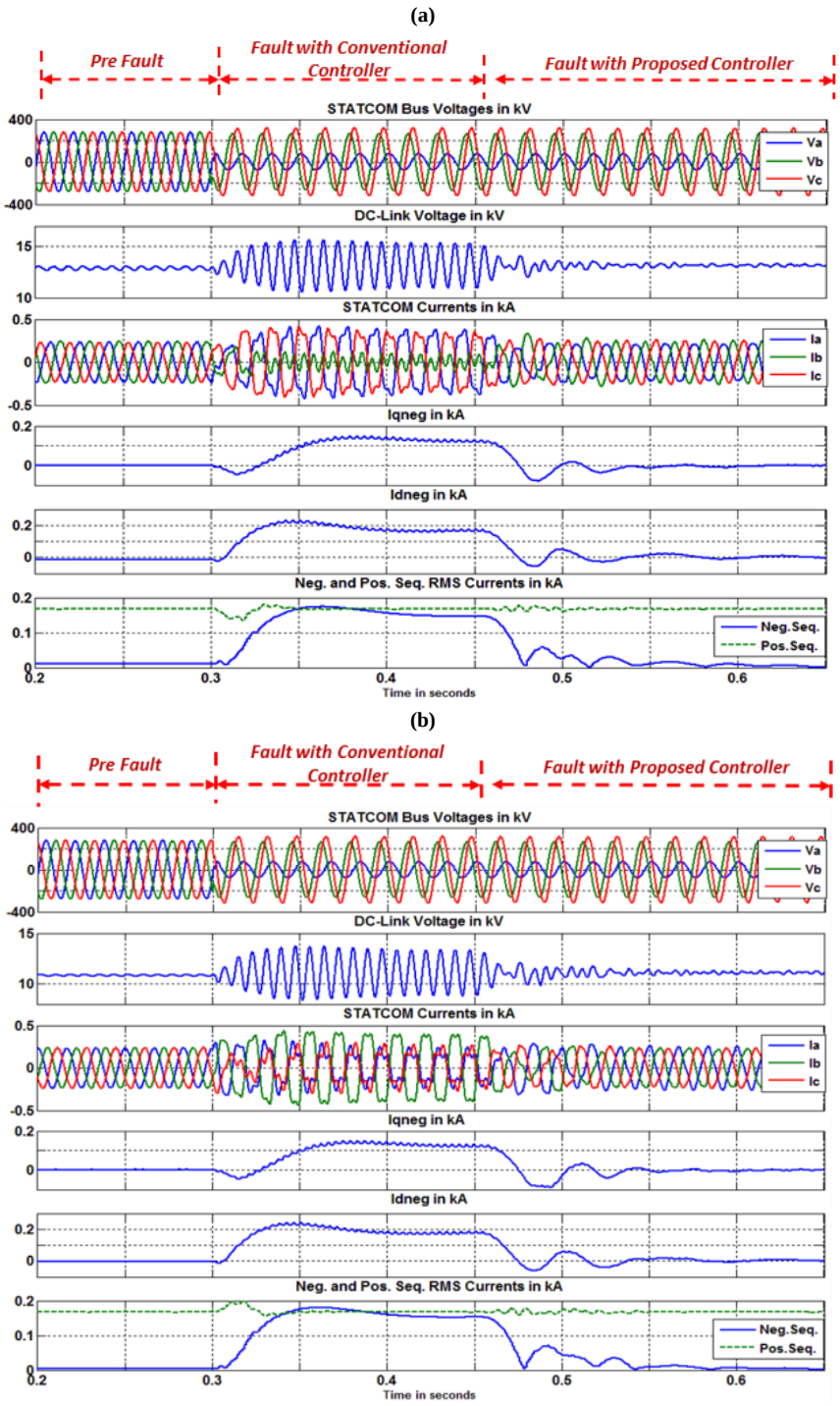


Figure 4-15. STATCOM performance with and without proposed solution under phase a SLG fault right at STATCOM bus (fault location1) when STATCOM is working in capacitive (a) and inductive (b) mode of operation. The current THD reaches from 1.2% before fault to around 2.9% after fault with proposed controller in both inductive and capacitive modes.

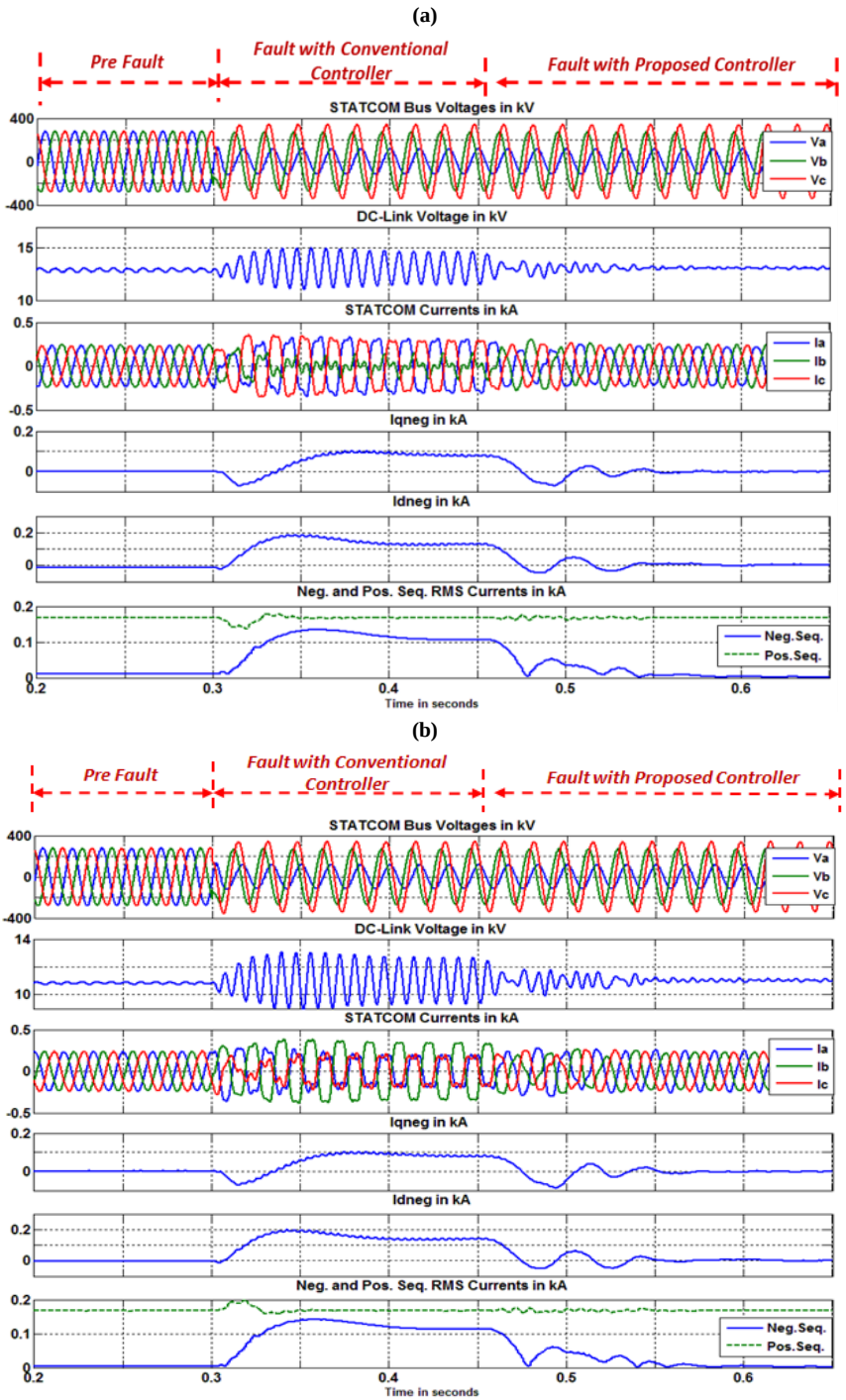


Figure 4-16. STATCOM performance with and without proposed solution under phase a SLG fault in the middle of the Marcy-Bus1 345 kV transmission line (fault location2) when STATCOM is working in capacitive (a) and inductive (b) mode of operation. The current THD reaches from 1.2% before fault to around 2.3% after fault with proposed controller in both inductive and capacitive modes.

current reaches to zero. Reduced negative-sequence current will dramatically decrease the DC-link voltage 2nd harmonic oscillations. Figure 4-15-(b) demonstrates the same results as in Figure 4-15-(a) for the time that STATCOM is working in inductive mode of operation. SLG fault is the most common fault in power systems. Therefore, the controller performance when there is a SLG fault at different location of the 3-bus AC-system has been analyzed in detail. Figure 4-16-(a) illustrates the STATCOM voltage and current waveforms with and without the proposed solution when there is a SLG fault at phase a in the middle of the 345 kV Marcy-Bus1 transmission line (fault location 2 inFigure 2-12 Figure 4-14). The STATCOM works in the capacitive mode of operation and injects 100 MVAr reactive power to the grid. Figure 4-16-(b) presents the same results as in Figure 4-16-(a) for the time that the STATCOM works in the inductive mode of operation and absorbs 100 MVAr from the grid. Results in Figure 4-16 prove the capability of the controller in limiting the negative-sequence current for the SLG fault in the middle of the 345 kV transmission line.

Theoretically, the performance of the proposed controller does not depend on the type of the AC-system fault. Basically, whenever there is a negative-sequence current flow to the STATCOM, no matter what kind of the AC-system fault caused it, the controller commands the VSC to generate a controllable negatives-sequence voltage at the VSC output terminals to force the STATCOM negative- sequence current to zero. However, since different types of the AC-system faults cause different fault dynamics, the controller performance under a very severe line to line fault has also been illustrated here. Figure 4-17-(a), and (b) demonstrate the STATCOM voltage and current waveforms with and without the proposed controller in the capacitive and inductive mode of operation respectively. This time a line to line fault

between phase b and c is applied in the middle of the 345 kV outgoing transmission line (fault location 2). As can be observed in Figure 4-17(a), associated with capacitive mode of operation, after applying the fault at t=0.3 seconds the negative-sequence RMS current reaches around 800 A. This increase in the negative-sequence current leads to fault peak current of around 2000 A at phase c. However, when the STATCOM switches to work with the proposed controller, the negative-sequence current reaches around zero and DC-link voltage second harmonic oscillations reduce dramatically. The fault peak current reduces from about 2000 A to less than 200 A. This reduction in fault peak current prevents the protection system from over current tripping while the safe operation of the switches and other STATCOM power components is provided.

So far in the presented simulation results, it was assumed that the fault is applied when the STATCOM works with the conventional controller and then after few cycles the STATCOM is switched to work with the proposed controller. This is the worst case that can happen and it was shown that even under the worst case scenario the controller limits the negative- sequence current well. However, in the real situation the proposed controller is in service throughout the entire time that the STATCOM is in operation. Figure 4-18-(a) demonstrates the STATCOM pre and post fault waveforms without the proposed controller when there is a SLG fault in the middle of the outgoing transmission line (fault location 2).Figure 4-18-(b) illustrates the same pre and post fault waveforms exactly under the same operating condition as in Figure 4-18 -(a) for the time that the STATCOM is equipped with single phase inverter and its controller. As can be observed in these figures, the proposed controller successfully limits the negative sequence current and DC-link voltage oscillations.

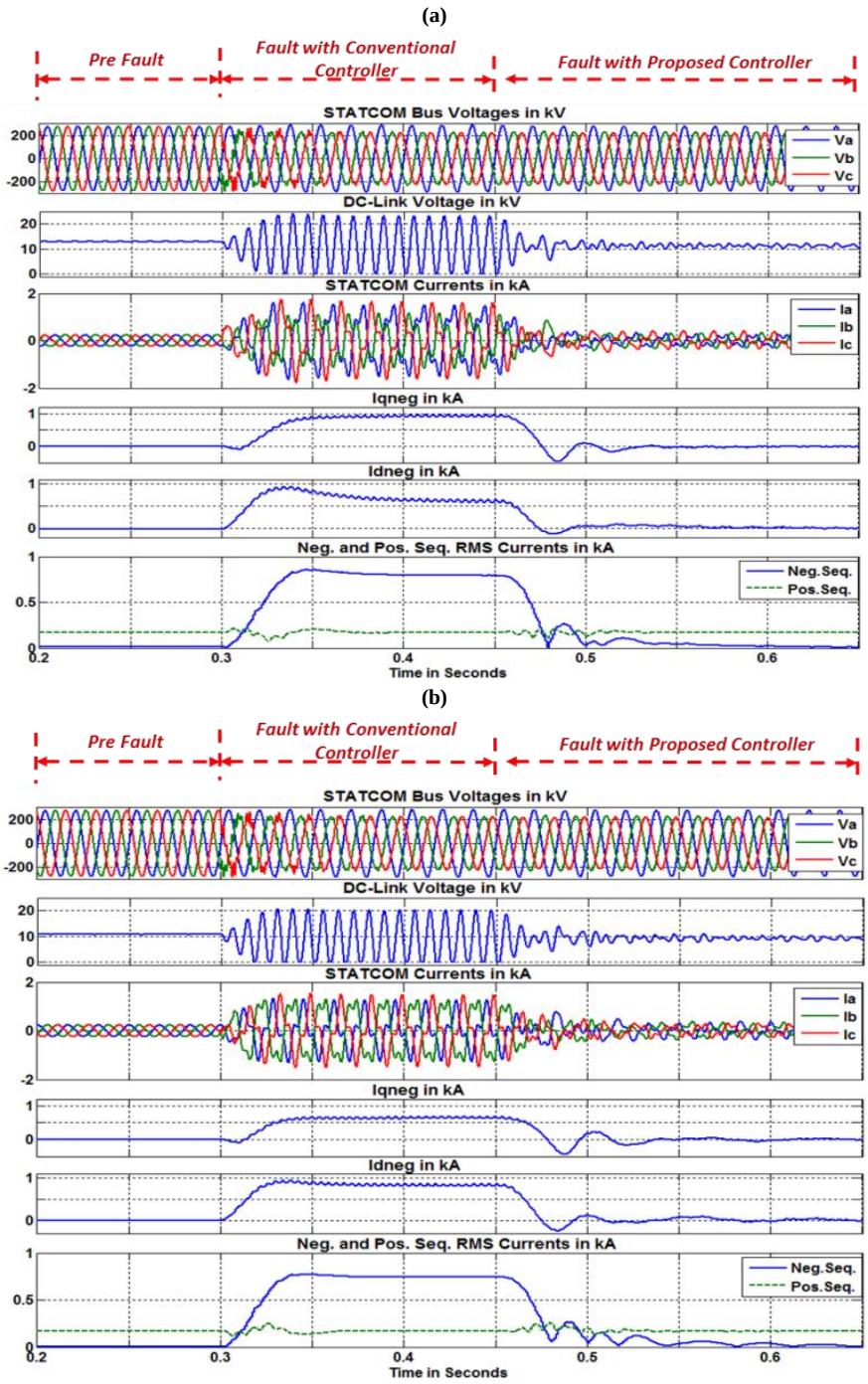


Figure 4-17. STATCOM performance with and without proposed solution under Line to Line fault between phase b , and c in the middle of the Marcy-Bus1 345 kV transmission line (fault location2) when STATCOM is working in capacitive (a) and inductive (b) mode of operation. The current THD reaches from 1.2% before fault to around 23% after fault with proposed controller in both inductive and capacitive modes.

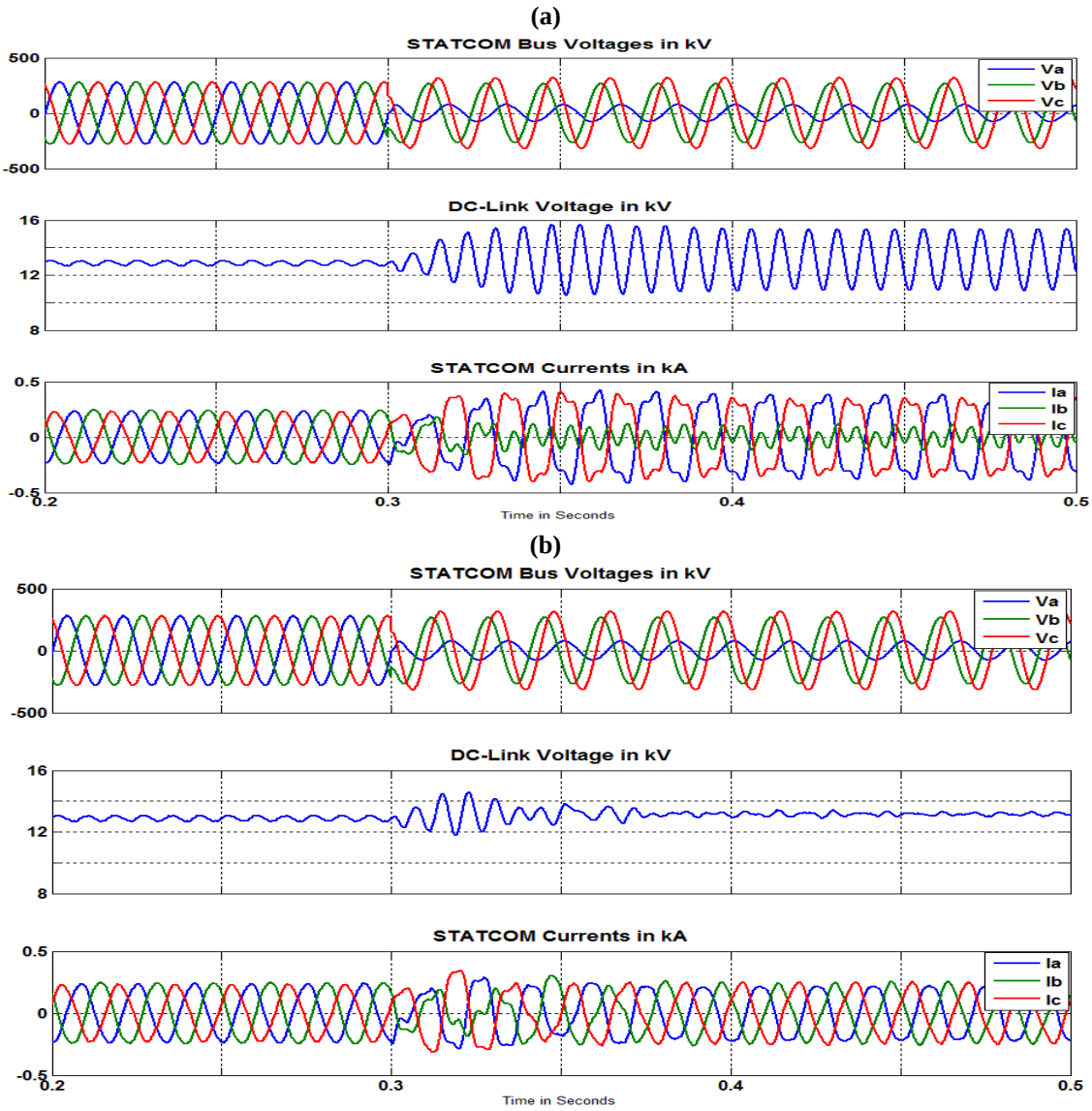


Figure 4-18. STATCOM performance with (b) and without (a) proposed solution under phase a SLG fault right at STATCOM bus (fault location1) when STATCOM is working in capacitive mode of operation.

As discussed earlier, the single phase inverter is sized for the 2nd harmonic oscillations that should be generated to control the negative-sequence current and not the DC-link average voltage. The value of the required 2nd harmonic oscillations to be generated by the single

phase inverter depends on the power system characteristics of the area where the STATCOM is installed. The single phase inverter should be sized based on the worst case (most severe fault) that can happen and STATCOM is supposed to remain online under that fault condition. The single phase inverter switches rating depends on the converter topology i.e. the number of the switches that will be placed in the series and parallel connection in each valve of the single phase inverter. Apart from the inverter rating, the other thing to be considered is the required energy source to keep the single phase inverter DC-bus energized. Ignoring the converter losses, theoretically during the steady state the single phase inverter does not need any source of real power connected to its DC-bus. Under normal condition, the voltage across the single phase inverter is zero and therefore no active power is required. When fault happens, transiently it needs energy to generate the desired 2^{nd} harmonic oscillation at its output terminals. However, when the 2^{nd} harmonic voltage is established across the single phase inverter, the DC-link 2^{nd} harmonic current goes to zero and therefore the single phase inverter does not consume any energy. Therefore, by proper design of the single phase inverter DC-link capacitor, the single phase inverter does not need a big energy source to keep its DC-bus energized. The single phase inverter DC-link can be energized using the substation auxiliary transformer (if it has enough extra capacity, else one dedicated auxiliary transformer) through a regular rectifier. This concept has been demonstrated in Figure 4-19. This figure illustrates the STATCOM negative-sequence current and single phase inverter current (which is the same as DC-link current) and voltage before and after applying a line to line fault in the middle of the Marcy-Bus1 345 kV transmission line. As can be observed, before applying the fault the single phase inverter current and voltage are

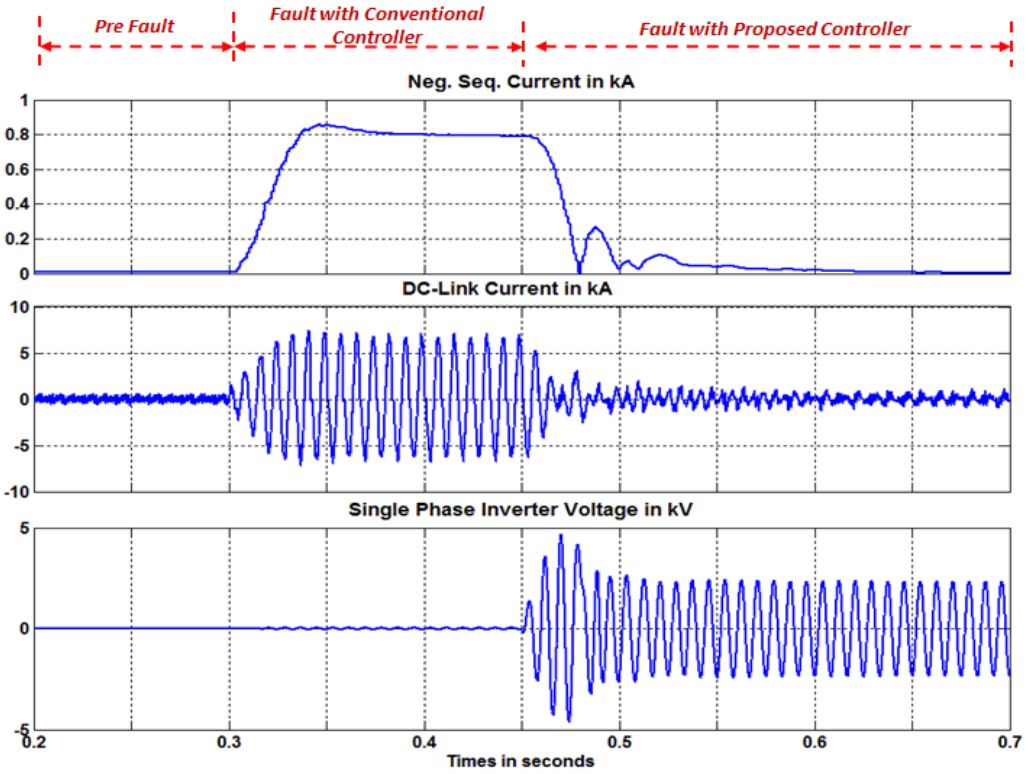


Figure 4-19. STATCOM negative-sequence current and single phase inverter current and voltage under a Line to Line fault in the middle of the Marcy-Bus1 345 kV transmission line

zero. Right after applying fault at t=0.3 seconds the negative-sequence current flows to the STATCOM and consequently the 2nd harmonic voltage and current appear on the DC-link. Since the STATCOM is still working with the conventional controller, the single phase inverter voltage is zero. At t=0.45 second, the STATCOM starts to work with the proposed controller and therefore the 2nd harmonic voltage is established across the single phase inverter. During the transient time that single phase inverter 2nd harmonic voltage reaches from zero to its steady state value and DC-link 2nd harmonic current reaches from its fault value to zero, the single phase inverter consumes energy. However, when the single phase

inverter 2nd harmonic voltage reaches to steady state, as can be seen in Figure 4-19, the DC-link 2nd harmonic current reaches to zero and the single phase inverter does not need any real power.

The proposed solution system losses are also an important design consideration. Basically, the STATCOM losses are around 1 MW under nominal condition i.e. 100 MVA of reactive power injection/absorption. Under severe unbalanced conditions and AC-system faults, the STATCOM losses increase dramatically (over 2 times and even more) due to the large fault current that flows through the 48-pulse inverter switches and magnetics. However, when the STATCOM is working with proposed solution the negative sequence current is forced to zero and therefore the STATCOM losses remain the same as the balanced condition. The single phase inverter losses are decided by the fault current i.e. the larger fault current the more losses. The single phase inverter losses are much smaller than the STATCOM losses due to the following reasons: 1) the single phase inverter works only under unbalanced condition which does not last for a long time in the transmission level. 2) When an unbalanced fault happens, only during a very short transient time, the converter losses are considerable. That is the time when the 2nd harmonic voltage is being generated across the single phase inverter terminals. However, when the required 2nd harmonic voltage is generated, the single phase inverter current (DC-link current) goes to zero and therefore the inverter losses decrease dramatically.

4.5 Summary

This chapter specifically proposed a solution to improve the transmission level angle-controlled STATCOM performance under unbalanced AC-system conditions and system faults. The main improvement is to decrease the negative-sequence current and DC-link voltage oscillations substantially under power line faults. The proposed solution is based on adding a single phase inverter in series with the DC-bus. This single phase inverter generates controllable oscillation with twice the line frequency on the DC-link. These oscillations generate negative-sequence voltage at STATCOM output terminals. This controllable negative-sequence voltage forces the negative-sequence current seen by the STATCOM to zero. Based on the proposed solution, one specific controller is designed which provides the capability of simultaneously controlling both positive and negative-sequence voltages. PSCAD simulation results verified the validity of the proposed solution.

Chapter 5: Oscillatory Angle Control Scheme for PWM Static Synchronous Compensators under Unbalanced Conditions and System Faults

5.1 Introduction

Significant voltage drops are usually observed at industrial load buses when there is a power fault at some point in the supplier utility or a sudden change in the utility load. This happens particularly if the industrial load is supplied through a long distribution feeder. Reactive power compensation is conventionally used to improve the load voltage profile and enhance the power factor. Voltage Source Converter (VSC) based STATCOMs controlled by the PWM techniques, are commonly used for the purpose of voltage regulation and power factor correction particularly for the sensitive industrial loads. The VSC based STATCOM are also widely used in the DG systems like photovoltaic, and wind generation in the distribution level [68]. A major drawback of using the VSC-based STATCOM is however, their sensitivity to the voltage disturbances especially unbalanced condition and system faults. To protect the semiconductor switches from the huge fault current flow, the STATCOM is tripped under utility system fault or severe unbalanced conditions when its reactive power support functionality is really needed. Moreover, most of the faults are unbalanced and results in voltage dips, which produce current harmonics and unbalance that also cause the STATCOM current protection to trip[68].Therefore, from the protection philosophy point of view, the VSC-based STATCOM with conventional current controller

either should be tripped or its power components should be overdesigned to tolerate the huge negative sequence current under unbalanced conditions and grid fault.

Basically, the inverter power components and switches must be designed for the peak continuous operating current and for the peak continuous operating voltage. Generally there is a designed margin beyond this point to accommodate some percentage overload as well as specified abnormal operating condition particularly unbalanced condition and grid faults. The MVA rating of the equipment and hence the cost is derived from the product of peak voltage and current (considering the fault and unbalanced condition), regardless of whether they occur at the same time or not[26]. Hence, the appropriate controller which is capable of limiting the fault current and consequently decrease the converter design margin will significantly reduce the converter equipment rating and cost.

It is highly beneficial to keep the STATCOM available during the power system faults when its reactive power support functionality may be needed the most. On the other hand, if the protection system trips the converter, it takes several fraction of an hour depending on the size of the converter to discharge the DC-link and check the healthiness of the entire system [25].Hence, several practical methods have been proposed and implemented to attenuate the effect of unbalanced line voltage on the converter performance under system faults.

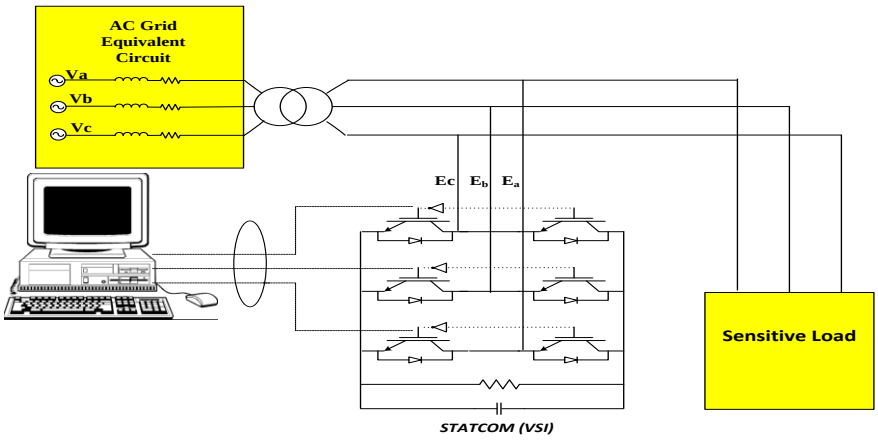


Figure 5-1. Voltage regulation of a load sensitive to voltage dip using a PWM VSC-based STATCOM

As the amount of the wind power around the world increases, system operators have been forced to tighten their grid connection rules-known as grid codes- in order to limit the effect of the wind powers on the network quality and stability. To achieve compliance with grid codes, some sort of the reactive power support like VSC-based STATCOM with appropriate fault ride through capability is required [69].Therefore, revisiting the VSC dynamics under power system disturbances seems to be an imperative factor in wind power expansion. Whereas the basic operating of the VSC-based STATCOM is well established in the literature, the fault performance has received relatively lower attention. This chapter proposes an **alternative** current control structure to improve the PWM VSC-based STATCOM performance under severe unbalanced conditions and system faults. The main improvement is to decrease the negative sequence current under fault conditions. Limiting the negative sequence current will reduce the MVA rating and cost of the converter power equipment and switches.

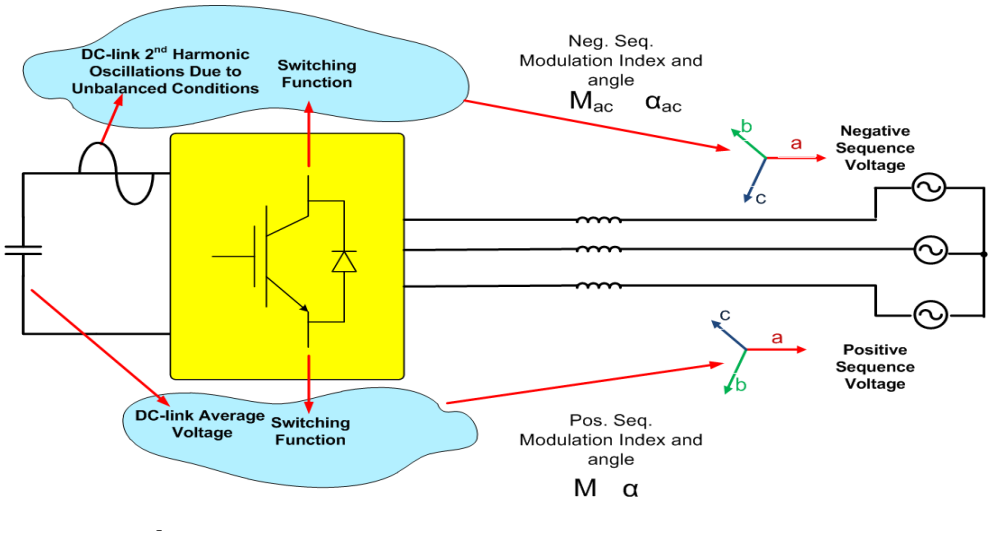


Figure 5-2. Simultaneous controlling of Neg. Seq. and Pos. Seq. voltages

In the proposed control structure, the conventional current controller in synchronous frame is in charge of controlling the VSC positive sequence output voltage. This is done by calculation of modulation index (M), and desired output voltage angle (α) based on calculated values of reference d and q component of the output voltage in synchronous frame. A new part is added to the conventional vector current controller in synchronous frame that controls the VSC output negative sequence voltage. The controllable negative sequence voltage attenuates the effect of the line negative sequence voltage due to the unbalanced condition and reduces the negative sequence current seen by the STATCOM. The output of this part of the controller is an oscillatory angle (2^{nd} harmonic oscillation) with appropriate amplitude (M_{ac}) and phase (α_{ac}) as shown in Figure 5-2.The output of the negative sequence voltage controller will be added to the α.

This chapter is organized as follows. Section 5.2 reviews the research and advances in the control of VSC under unbalanced conditions and grid faults. Section 5.3 analyses the behavior of the VSC under fault conditions and obtains the required equations to develop the proposed controller. Section 5.4 presents the VSC output voltage harmonic content when 2^{nd} harmonic oscillations are added to the DC-link voltage. In section 5.5, the proposed control structure and its implementation are presented. Proposed controller stability will also be discussed in this part of the paper. PSCAD/EMTDC simulation results and Hardwar-In-the-Loop testing results present in section 5.6 and 5.7.

5.2 Backgrounds on controlling the VSC under unbalanced conditions

Since the VSC is the main building block of the VSC-based STATCOM, it is imperative to study the methods, proposed by different technical literature, for controlling and modeling of the VSC under grid unbalanced conditions. The VSC performance under unbalanced grid conditions has been studied in details in [40]. This paper calculates the AC, and DC-side voltage and current harmonic contents due to AC-side negative sequence current flow under unbalanced conditions. Authors in [38] have visualized the VSC under unbalanced grid condition as two independent subsystems of positive and negative sequence. The required current references for each subsystem is calculated and based on that, appropriate PWM switching pattern is obtained accordingly. The proposed controller in [38]however, suffers from singularity under very severe unbalanced condition. This model also ignores the power exchange with VSC interface inductor. This approximation is valid for low power VSCs where the interface reactors are relatively small due to high switching frequency. However for high power applications, with limited switching frequency due to switching losses, the

interface reactors are normally large and cannot be ignored in the model [28]. Authors in [37], [45], [46], and [47] have improved the method used in [38] by considering the instantaneous power at the Point of Common Coupling (PCC) instead of converter poles, and have obtained the better converter performance. The proposed method in [37], [45], and [47] have improved the previous work by [38], however, this method suffer from solving nonlinear equations in real time and low bandwidth of the current regulator due to the extraction of the current sequence components [25]. Authors in [28] proposed a unified dynamic model and controller for the VSC under unbalanced grid conditions and system faults. Despite the almost ripple free DC-link voltage and limiting the negative sequence current, the proposed method is strongly dependent to the value of interface inductance and DC-link capacitor. This method also requires a very high gain in the DC-link voltage controller. In [25], authors for the BTB systems, proposed a high bandwidth control scheme originated from Lyapanuv methods in the popular dq synchronous frame. No need for any sequence or harmonic extraction blocks and resonant compensators are the main advantages of the proposed method especially for system operating at low switching frequency (9-15 times). Many other control structures have been proposed by the researchers to improve the VSC performance under fault conditions [48]-[54], and [70]-[75]. These are focused on mainly generating the current reference in both positive and negative synchronous frame to regulate the power or voltage at the point of common coupling (PCC) [25].

5.3 Analysis of VSC under unbalanced operating conditions

Symmetrical components are most commonly used for analysis of three-phase unbalanced electrical systems. In this method, a set of unbalanced three phase phasor is split

into two symmetrical positive and negative sequences and one zero sequence component. Based on this theory, tie line currents of the phase a of a STATCOM in Figure 5-3 under fault condition will be as:

$$i_a = i_a^+ + i_a^- + i_a^0 \tag{5-1}$$

neglecting zero sequence current:

$$i_a = i^+ \sin(\omega t + \theta_i^+) + i^- \sin(\omega t + \theta_i^-) \tag{5-2}$$

$$i_b = i^+ sin\left(\omega t + \theta_i^+ - \frac{2\pi}{3}\right) + i^- sin\left(\omega t + \theta_i^- + \frac{2\pi}{3}\right) \tag{5-3}$$

$$i_c = i^+ sin\left(\omega t + \theta_i^+ + \frac{2\pi}{3}\right) + i^- sin\left(\omega t + \theta_i^- - \frac{2\pi}{3}\right) \tag{5-4}$$

the VSC positive sequence fundamental frequency switching function can be written as in (5-5)-(5-7).

$$s_a = M\, sin(\omega t + \alpha) \tag{5-5}$$

$$s_b = M\, sin\left(\omega t + \alpha - 2\frac{\pi}{3}\right) \tag{5-6}$$

$$s_c = M\, sin\left(\omega t + \alpha + 2\frac{\pi}{3}\right) \tag{5-7}$$

M is the modulation index, and α is the angle by which the inverter voltage vector leads/lags the line voltage vector. Then the inverter terminal voltage is calculated as:

$$v_a = \mathrm{M}\ \frac{v_{DC}}{2} \sin(\omega t + \alpha) \tag{5-8}$$

$$v_b = \mathrm{M} \frac{v_{DC}}{2}\ \sin\left(\omega t + \alpha - 2\frac{\pi}{3}\right) \tag{5-9}$$

$$v_c = \mathrm{M}\frac{v_{DC}}{2}\sin\left(\omega t + \alpha + 2\frac{\pi}{3}\right) \tag{5-10}$$

The interaction between the fundamental frequency inverter switching function and the negative sequence component of the current, produces 2nd harmonic oscillations on the DC-link voltage and current [39] and [40].Therefore general expression of the DC-link voltage during unbalanced condition becomes:[37]

$$v_{DC} = V_{dc} + V_{dch2}\cos(2\omega t + \theta_v^{dc}) \tag{5-11}$$

where $\mathrm{V_{dc}}$ is the average value and $\mathrm{V_{dch2}}$ is the amplitude of 2nd harmonic oscillations of DC-Link voltage. Substituting (5-11) to (5-8)-(5-10), the inverter output voltages when the DC-link voltage is distorted by 2nd harmonic oscillations due to the unbalanced AC system are calculated as:

$$v_a = \mathrm{M}\,\frac{V_{dc}}{2}\sin(\omega t + \alpha) + \frac{MV_{dch2}}{4}\sin(3\omega t + \alpha + \theta_v^{dc}) + \frac{MV_{dch2}}{4}\sin(-\omega t + \alpha - \theta_v^{dc}) \tag{5-12}$$

$$v_b = \mathrm{M}\,\frac{V_{dc}}{2}\sin(\omega t + \alpha - 120) + \frac{MV_{dch2}}{4}\sin(3\omega t + \alpha + \theta_v^{dc} - 120) + \frac{MV_{dch2}}{4}\sin(-\omega t + \alpha - \theta_v^{dc} - 120) \tag{5-13}$$

$$v_c = \mathrm{M}\frac{V_{dc}}{2}\sin(\omega t + \alpha + 120) + \frac{MV_{dch2}}{4}\sin(3\omega t + \alpha + \theta_v^{dc} + 120) + \frac{MV_{dch2}}{4}\sin(-\omega t + \alpha - \theta_v^{dc} + 120) \tag{5-14}$$

Equations (5-12)-(5-14) shows that the interaction between switching function and the DC-link voltage 2nd harmonic oscillations generates fundamental negative sequence voltage at the VSC output terminals. Basically the unbalanced AC system conditions can be emulated by postulating a set of negative sequence voltage source in series with STATCOM tie line[19].

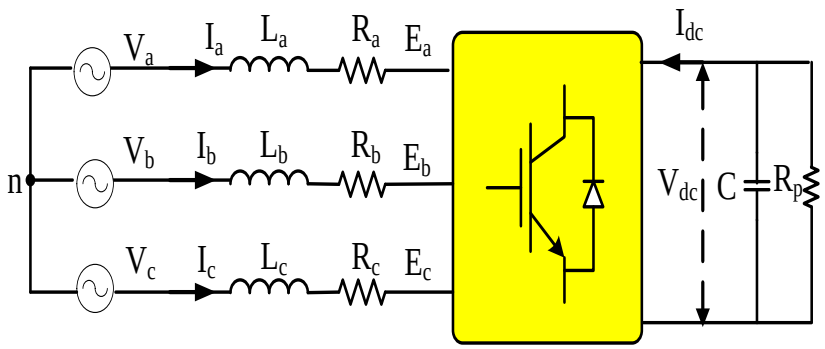


Figure 5-3. Equivalent circuit of an VSC connected to AC system

The basic idea of proposed control strategy is to generate required fundamental negative sequence voltage vector at the VSC output terminals to attenuate the effect of the postulated negative sequence bus voltages. The generated negative sequence voltage, results in reduction of the negative sequence current seen by the STATCOM under fault conditions. It is important to note that interaction between switching function and the DC-link voltage 2nd harmonic oscillations also generates 3rd harmonic voltage at the VSC output terminals. This 3rd harmonic voltage is positive sequence and phase a, b, and c are 120 degree apart. Basically the negative sequence current flow due to unbalanced AC-system condition generates the 2nd harmonic oscillations on the DC-link voltage which will be reflected as fundamental negative sequence voltage and 3rd harmonic voltage at the VSC terminals. No matter if there is any negative sequence voltage controller or not the 3rd harmonic voltage is being generated at the VSC output terminals. This chapter will show that by controlling 2nd harmonic oscillations on the DC-link voltage, the negative sequence current and consequently the fault peak current will reduce significantly.

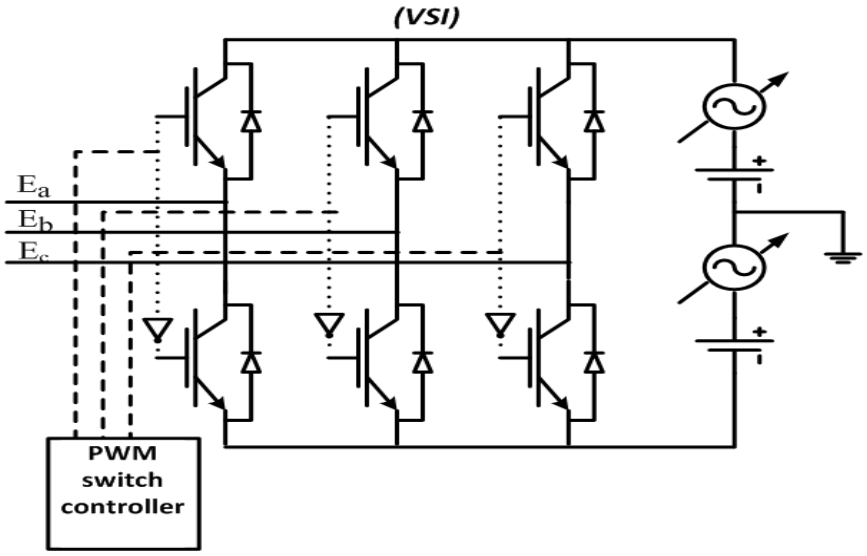


Figure 5-4. 2- level inverter with variable AC-sources used to calculate the generated negative sequence voltage at VSC terminals

5.4 Voltage spectral content

The idea of generating controllable negative sequence voltage at the VSC output terminals by controlling the 2nd harmonic oscillations of the DC-link voltage has been verified in this section. The analytical calculations and Matlab simulation results verifies the validity of this idea.

The amount of the calculated negative sequence voltage in (5-12)-(5-14) was verified by simulation of a two level VSC in Matlab/Simulink. The DC-side of this converter is supplied from a two series connected DC voltage sources in series with two variable 120 Hz AC voltage sources as shown in Figure 5-4.The AC-side is left open circuit. The 2nd harmonic oscillation amplitude of the DC-link voltage is set to 0, 10, 20, and 30 percent of the DC source voltage. Figure 5-5 shows the converter output voltage with 2nd harmonic oscillation

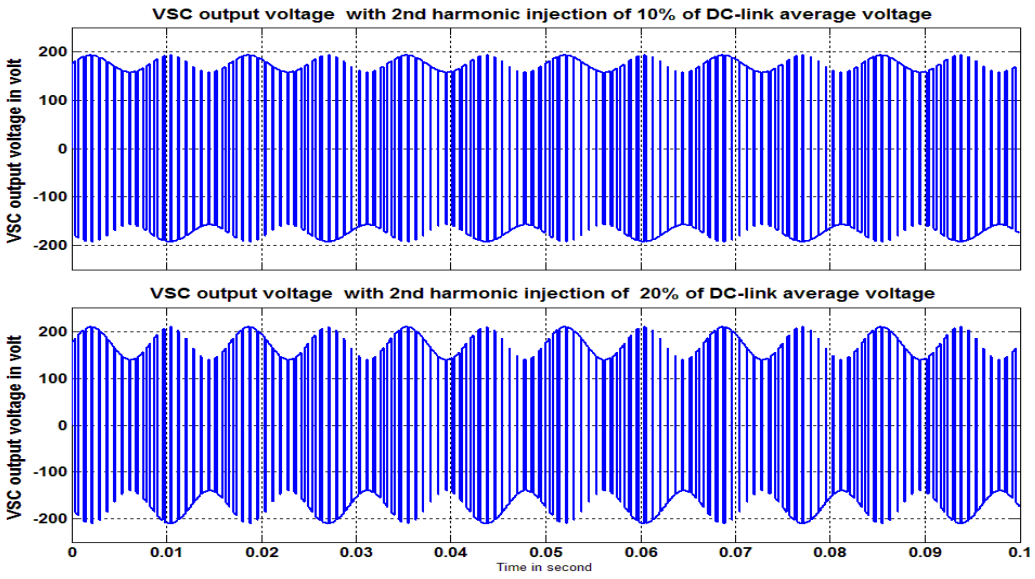
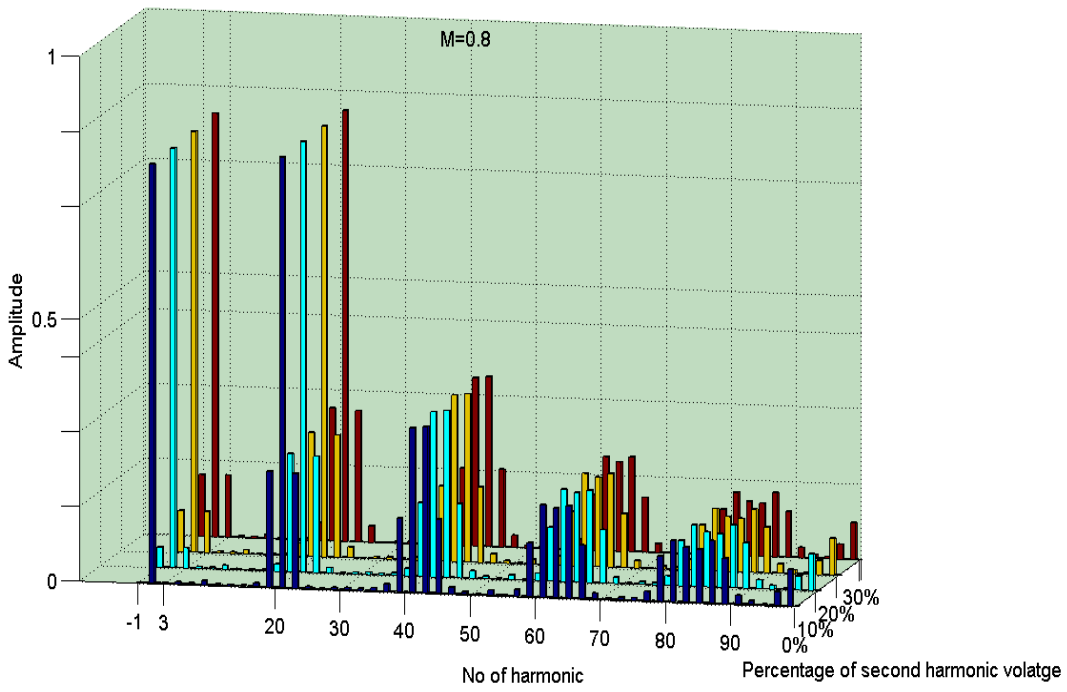


Figure 5-5. VSC output voltage with 2nd harmonic injection of 10% and 20% of the DC-link average voltage

of 10%, and 20% of the DC source voltage and modulation index of 0.9. According to the equation (5-12)-(5-14), these 2nd harmonic oscillations are not influencing the positive sequence fundamental frequency. The spectral content of the output voltage for modulation index of 0.8, and 0.9 with 2nd harmonic oscillation amplitude of 0, 10, 20, and 30 percent of the DC source voltage and switching frequency of 1260 Hz is presented in Figure 5-6. It was found that the amount of fundamental positive and negative sequence components calculated in (5-12)-(5-14) perfectly match the simulation results. It is also important to note that after adding 2nd harming oscillations to the DC-bus, the other high order harmonics (except the negative sequence and 3rd harmonic) remain almost unchanged.

(a)



(b)

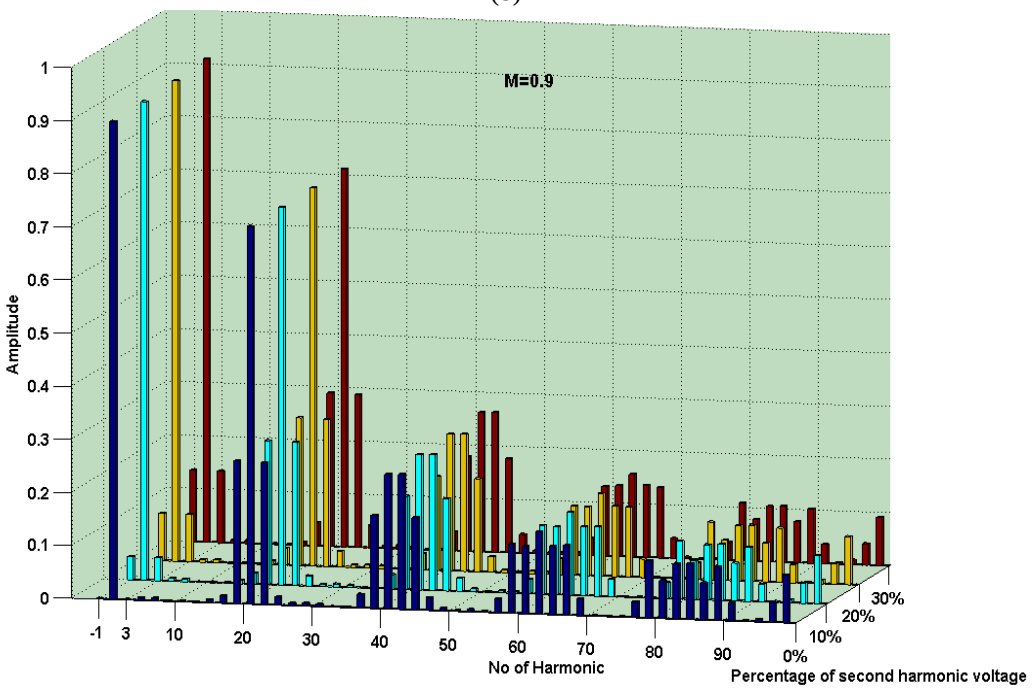


Figure 5-6. Inverter output voltage with modulation index of 0.8(a), and 0.9 (b) and switching frequency of 1260 Hz when different percentages of 2nd harmonic oscillations (with respect to the DC-link average voltage) are added to the DC-link voltage.

5.5 Proposed Control Structure Development

5.5.1 Derivation of STATCOM equations in the negative synchronous frame

As it was discussed in the previous section, the STATCOM voltage and current during unbalanced conditions can be calculated by postulating a set of negative sequence voltage source in series with STATCOM tie line as shown in Figure 5-7.As discussed earlier, negative sequence current at STATCOM tie line generates 2nd harmonic oscillations at the DC-link voltage. These 2nd harmonic oscillations will be reflected as negative sequence voltage at STATCOM terminals as calculated in (5-12)-(5-14).

Assuming 2nd harmonic oscillation at DC-link voltage as:

$$V_{dch2}\cos(2\omega t + \theta_{vdc}) \tag{5-15}$$

then reflected negative sequence voltages at STATCOM terminal are calculated as in (5-16)-(5-18).

$$e_a^- = \frac{MV_{dch2}}{4}\sin(-\omega t + \alpha - \theta_{vdc}) \tag{5-16}$$

$$e_b^- = \frac{MV_{dch2}}{4}\sin(-\omega t + \alpha - \theta_{vdc} - \frac{2\pi}{3}) \tag{5-17}$$

$$e_c^- = \frac{MV_{dch2}}{4}\sin(-\omega t + \alpha - \theta_{vdc} + \frac{2\pi}{3}) \tag{5-18}$$

The derivative of STATCOM tie line negative sequence currents with respect to time are calculated as in (5-19)-(5-21).

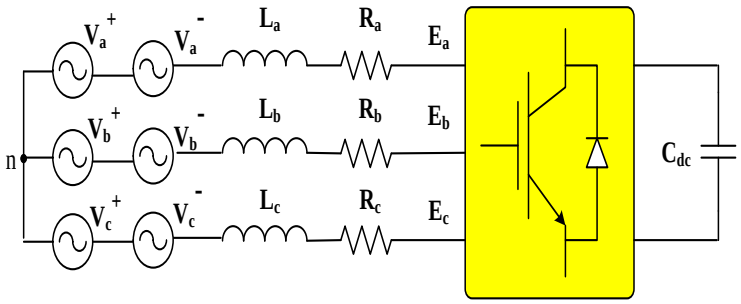


Figure 5-7. STATCOM equivalent circuit with series negative sequence voltage sources

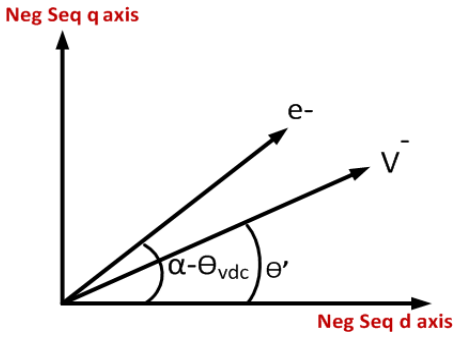


Figure 5-8. STATCOM instantaneous voltage vectors in the negative synchronous reference frame

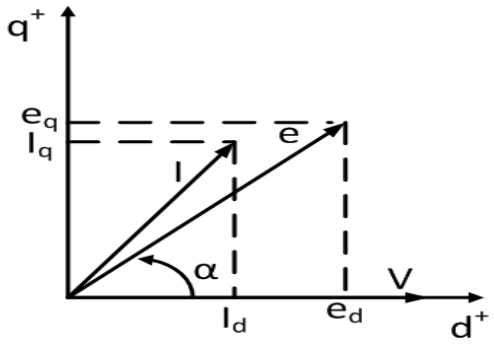


Figure 5-9. STATCOM vectors in the positive synchronous frame

$$\frac{di_a^-}{d_t} = \frac{-R}{L} i_a^- + \frac{(e_a^- - V_a^-)}{L} \quad (5\text{-}19)$$

$$\frac{di_b^-}{d_t} = \frac{-R}{L} i_b^- + \frac{(e_b^- - V_b^-)}{L} \quad (5\text{-}20)$$

$$\frac{di_c^-}{d_t} = \frac{-R}{L} i_c^- + \frac{(e_c^- - V_c^-)}{L} \quad (5\text{-}21)$$

Transformation from abc to negative synchronous frame is defined as:

$$f_{dq}^{-} = T(-\theta) f_{abc}^{-} \tag{5-22}$$

Where:

$$T(-\theta) = \frac{2}{3}\begin{bmatrix} \cos(-\theta) & \cos(-\theta - \frac{2\pi}{3}) & \cos(-\theta + \frac{2\pi}{3}) \\ -\sin(-\theta) & -\sin(-\theta - \frac{2\pi}{3}) & -\sin(-\theta + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \tag{5-23}$$

and θ is the STATCOM bus phase lucked loop output. Figure 5-8 illustrates the instantaneous negative sequence STATCOM bus (v^{-}) and inverter output voltage (e^{-}) in the negative synchronous frame. Vector v^{-} is assumed to have an arbitrary angle of Θ'. d and q components of these two vectors are calculated as:

$$e_d^{-} = |e^{-}| \cos(\alpha - \theta_{vdc}) = \frac{MV_{dch2}}{4} \cos(\alpha - \theta_{vdc}) \tag{5-24}$$

$$e_q^{-} = |e^{-}| \sin(\alpha - \theta_{vdc}) = \frac{MV_{dch2}}{4} \sin(\alpha - \theta_{vdc}) \tag{5-25}$$

$$v_d^{-} = |v^{-}| \cos(\theta') \tag{5-26}$$

$$v_q^{-} = |v^{-}| \sin(\theta') \tag{5-27}$$

Transforming equation (5-19)-(5-21) based on (5-23), and considering the equation (5-24)-(5-27) for the bus and STATCOM voltage we find:

$$\frac{d}{dt} i_d^{-} = \frac{-R}{L} i_d^{-} - \omega i_q^{-} + \frac{MV_{dch2}}{4L} \cos(\alpha - \theta_{vdc}) - \frac{1}{L} v_d^{-} \tag{5-28}$$

$$\frac{d}{dt} i_q^{-} = \frac{-R}{L} i_q^{-} + \omega i_d^{-} + \frac{MV_{dch2}}{4L} \sin(\alpha - \theta_{vdc}) - \frac{1}{L} v_q^{-} \tag{5-29}$$

Equation (5-28) and (5-29) describe the dynamic of the VSC AC-side negative sequence current, in terms of negative synchronous frame variables and 2nd harmonic oscillations of the DC-link voltage. Basically, these equations show that the dynamics of STATCOM tile

line negative sequence current d and q components are related to the phase and amplitude of the DC-link voltage 2nd harmonic oscillations.

5.5.2 DC-link voltage dynamics

As discussed earlier, proposed controller is based on generating required fundamental negative sequence voltage vector at the VSC output terminals to attenuate the effect of postulated negative sequence bus voltage under fault conditions and to limit the negative sequence current. The required negative sequence voltage vector is obtained by controlling the 2nd harmonic DC-link voltage oscillations. This part of the chapter shows that DC-link voltage 2nd harmonic oscillations are controlled by adding appropriate oscillations to the angle of the conventional vector current controller output i.e. angle α. First the transfer function between the α and DC-link voltage is obtained. As the dq equations of the STATCOM current under balanced system condition has already been discussed in different literature, only a brief outline is given here to make the paper consistent. The AC-side equation of the STATCOM in Figure 5-3 can be written as follows:

$$\frac{di_a}{d_t} = \frac{-R_s}{L} i_a + \frac{(e_a - V_a)}{L} \tag{5-30}$$

$$\frac{di_b}{d_t} = \frac{-R_s}{L} i_b + \frac{(e_b - V_b)}{L} \tag{5-31}$$

$$\frac{di_c}{d_t} = \frac{-R_s}{L} i_c + \frac{(e_c - V_c)}{L} \tag{5-32}$$

Considering Figure 5-9 which illustrates the AC-side circuit vectors in the positive synchronous frame and transforming equation (5-30)-(5-32) from abc domain to positive synchronous frame we yield:

$$\frac{d}{d_t}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} -\frac{R_s}{L} & \omega \\ -\omega & -\frac{R_s}{L} \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix} + \frac{1}{L}\begin{bmatrix} e_d - |V| \\ e_q \end{bmatrix} \quad (5\text{-}33)$$

To analyze the DC-link voltage behavior with respect to the α, it is necessary to include the DC-side circuit of the VSC in our equations. By the nature of the basic physical laws, the instantaneous power at the AC and DC terminals of the VSC is equal. Therefore the power balance equation when the converter losses are ignored can be written as follows:

$$C\frac{d}{dt}v_{dc} = \frac{-3}{2v_{dc}}(e_d i_d + e_q i_q) \quad (5\text{-}34)$$

Having linearized the state equations ((5-33), and (5-34)), then the Small variations of the DC-link voltage around a chosen steady state point when all the losses are ignored is related to angle α perturbation through the following equation.

$$\frac{\Delta v_{dc}}{\Delta \alpha} = \frac{-6i_{q0}LMs^2 - 3M^2V_{dc0}\omega_0 - 6i_{q0}LM{\omega_0}^2}{8CLs^3 + (3M^2 + 8CL{\omega_0}^2)s} \quad (5\text{-}35)$$

Numerical calculation for one STATCOM has been done to illustrate the DC-link voltage behavior in response to changing α. This is exactly the same STATCOM that has been used in the simulation and Hardware-In-the-Loop test. Figure 5-10 indicates the bode plots of the DC-link variation with respect to the α perturbation when the STATCOM is working around different capacitive and inductive steady-state points. A remarkable point evident in these figures is that introducing 2nd harmonic oscillations to the α, results in 90˚ lagging 2nd harmonic oscillations on the DC-link voltage in both inductive and capacitive mode of operation. The relationship between the α perturbation and DC-link voltage variation when modulation index is varied form a very high value to a very low value was

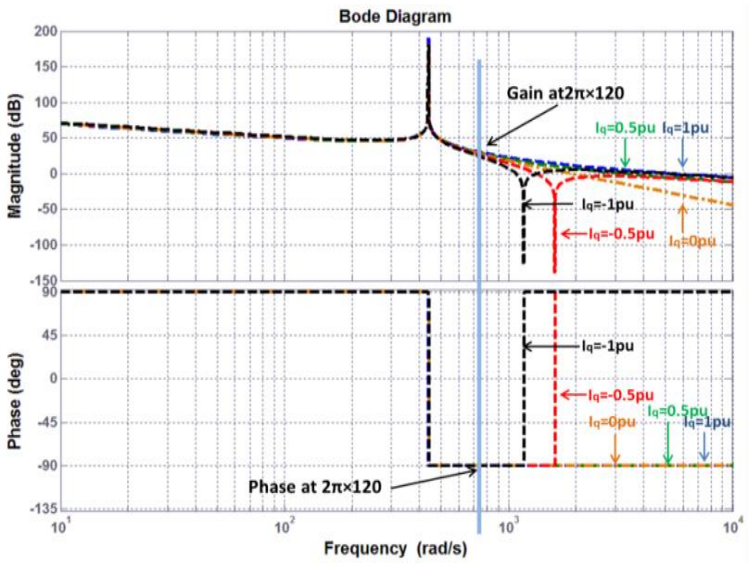


Figure 5-10. Bode plots of the DC-link voltage perturbation against α perturbation around different inductive and capacitive equilibrium points. Positive and negative Iq corresponds to the capacitive and inductive mode of operations respectively.

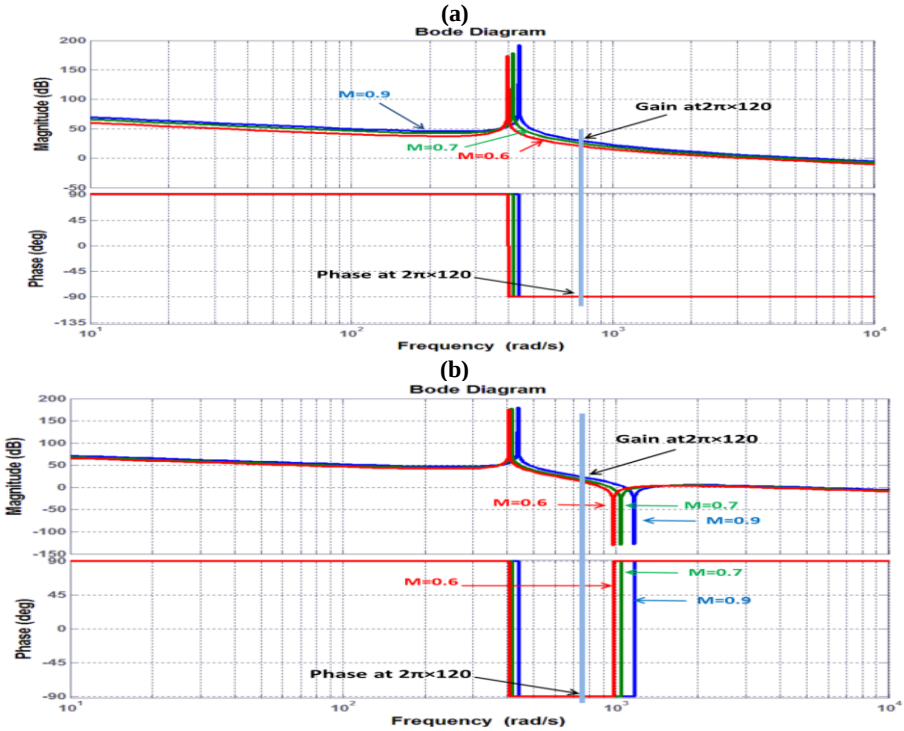


Figure 5-11. Bode plots of the DC-link voltage perturbation against α perturbation around one capacitive (a)/inductive (b) equilibrium point with different modulation index.

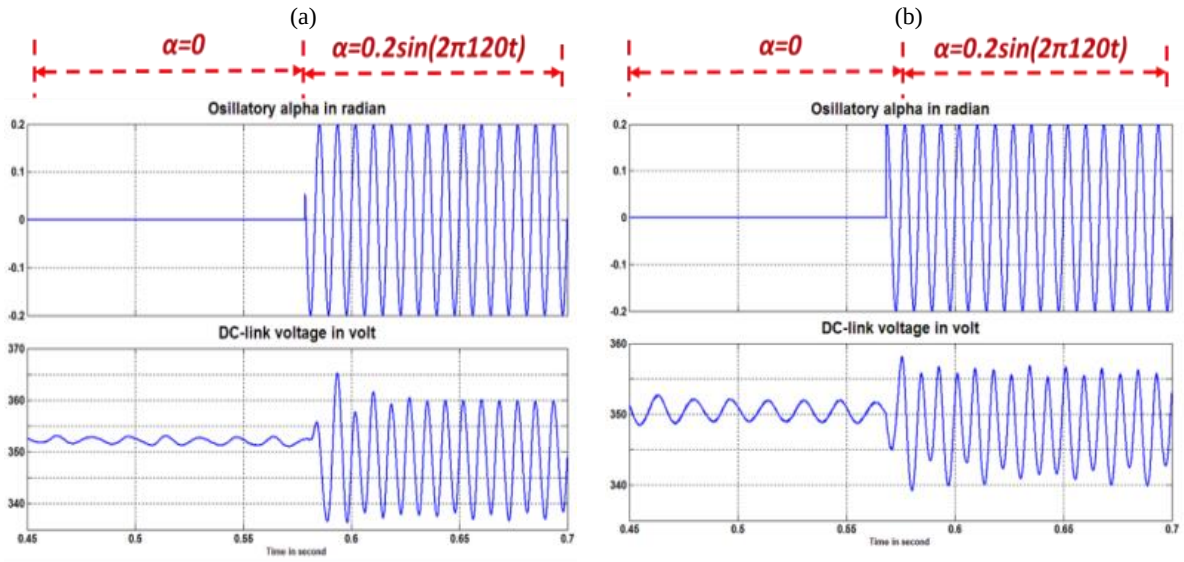


Figure 5-12. DC-link voltage 2nd harmonic oscillations generated by introducing 2nd harmonic oscillations to α in both capacitive (a) and inductive (b) operation modes.

also investigated in both capacitive and inductive mode of operation. As can be observed in Figure 5-11-(a), corresponding to the capacitive mode of operation, even with different modulation indices, introducing 2^{nd} harmonic oscillations to the α, results in 90˚ lagging 2^{nd} harmonic oscillations on the DC-link voltage. The same results were obtained for the inductive mode as shown in the Figure 5-11-(b).These results have also been verified by PSCAD/EMTDC simulation results. As can be seen in Figure 5-12, adding an oscillation of $0.2sin(2\omega t)$ radian to the α, results in 90˚ lagging 2^{nd} harmonic oscillations on the DC-link voltage in both inductive and capacitive mode of operations. This concept of 90˚ phase shift between DC-link voltage and α 2^{nd} harmonic oscillation has been used to develop the proposed controller. The application of this concept to develop the proposed controller has been discussed in detail in the following section and appendix 5-A.

5.5.3 Proposed Controller

In the proposed control structure, the conventional PWM vector controller is used to control the positive sequence reactive current and consequently the VSC positive sequence output voltage. The amplitude and phase of the positive sequence voltage is determined by the modulation index (M) and angle (α) as shown in Figure 5-13. Rejection notch filter at double the line frequency has been added to the measured current in synchronous frame to isolate the positive sequence controller from the negative sequence signals. The output of the negative sequence voltage controller is a 2^{nd} harmonic oscillation with appropriate phase (α_{ac}) and amplitude (M_{ac}) to generate the required negative sequence voltage vector at the VSC terminals to attenuate the effect of the postulated negative sequence bus voltage under fault conditions. The generated negative sequence voltage results in reduction of the negative sequence current seen by the STACOM. The phase of this oscillation (α_{ac}) is coming from the 2^{nd} harmonic oscillations of the q-axis component of the tie line current in the positive synchronous frame when system is unbalanced.

Basically negative sequence current appears as 2^{nd} harmonic oscillations in the q-axis component of the line current in positive synchronous frame as calculated in (5-36). It is shown in appendix 5-A that adding a 2^{nd} harmonic oscillation in phase with the signal of equation (5-36) to the α, will generate negative sequence voltage in phase with v^{-} (STATCOM bus negative sequence voltage due to unbalanced conditions and faults) at the STATCOM terminals. The amplitude of the negative sequence voltage controller output (M_{ac}) is regulated by a PI controller. The proposed control structure is demonstrated in Figure 5-13.

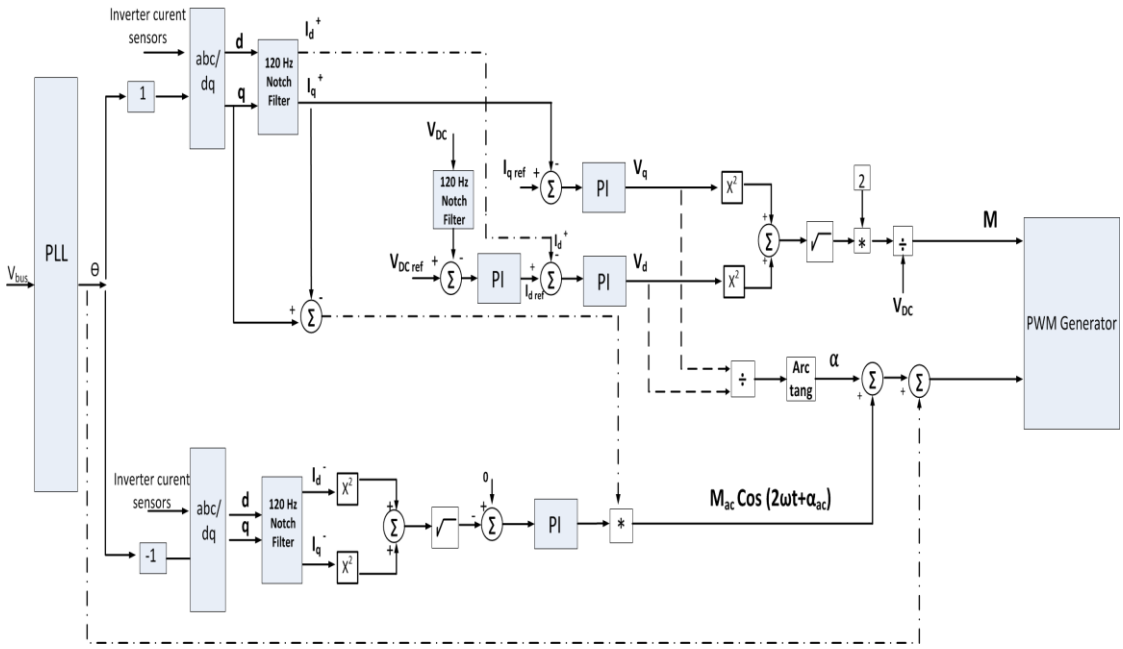


Figure 5-13. Proposed control structure

$$\frac{2}{3}\begin{bmatrix} i^- \sin(-\omega t + \theta_i^-) \\ i^- \sin\left(-\omega t + \theta_i^- - \frac{2\pi}{3}\right) \\ i^- \sin\left(-\omega t + \theta_i^- + \frac{2\pi}{3}\right) \end{bmatrix}\left[-sin\theta \quad -\sin(\theta - \tfrac{2\pi}{3}) \quad -\sin(\theta + \tfrac{2\pi}{3})\right]= \tag{5-36}$$

$$i^- \cos(-2\omega t + \theta_i^- + \pi) = i^- \cos(2\omega t - \theta_i^- + \pi)$$

5.5.4 Proposed Controller Stability

The proposed controller was presented and discussed in details in the previous parts of the chapter. The objective of this part of the chapter is to focus on the proposed controller design with intent of deriving the required equations and transfer functions to analyze the controller stability. The dynamics of the VSC negative sequence current was obtained in the equations (5-30), and (5-31). It was shown that the VSC negative sequence current is decided by the 2nd harmonic oscillations of the DC-link voltage and negative synchronous frame

variables. It was also proved with analytical calculation and simulation results that introducing second harmonic oscillations to the α, results in 90˚ lagging 2nd harmonic oscillations on the DC-link voltage.

Assuming a negative sequence controller output of:

$$M_{ac}\cos(2\omega t + \alpha_{ac}) \tag{5-37}$$

and ignoring the converter delay, the steady-state DC-link voltage 2nd harmonic oscillations will be as in (5-38):

$$V_{dch2}\cos(2\omega t + \theta_{vdc}) = KM_{ac}\cos\left(2\omega t + \alpha_{ac} - \frac{\pi}{2}\right) \tag{5-38}$$

where K is the DC-link voltage to α transfer function amplitude at ω=2π×120. Substituting the equation (5-38) into equations (5-28), and (5-29) yields the following equations:

$$\frac{d}{dt}i_d^- = \frac{-R}{L}i_d^- - \omega i_q^- - \frac{MKM_{ac}}{4L}\sin(\alpha - \alpha_{ac}) - \frac{1}{L}v_d^- \tag{5-39}$$

$$\frac{d}{dt}i_q^- = \frac{-R}{L}i_q^- + \omega i_d^- + \frac{MKM_{ac}}{4L}\cos(\alpha - \alpha_{ac}) - \frac{1}{L}v_q^- \tag{5-40}$$

Equations (5-39), and (5-40) are nonlinear if α_{ac} is regarded as an input variable. However, by linearizing the equations, we are able to find useful solution for small deviations around a chosen steady state equilibrium point. Linearizing equation (5-39) and (5-40) yields the following equation:

$$\frac{d}{dt}\begin{bmatrix}\Delta i_d^- \\ \Delta i_q^-\end{bmatrix} = \begin{bmatrix}\frac{-R}{L} & -\omega_0 \\ \omega_0 & \frac{-R}{L}\end{bmatrix}\begin{bmatrix}\Delta i_d^- \\ \Delta i_q^-\end{bmatrix} + \tag{5-41}$$

$$\begin{bmatrix} \frac{-1}{L} & 0 & \frac{-M_0K}{4L}sin(\alpha_0-\alpha_{ac0}) & \frac{M_0KM_{ac0}}{4L}cos(\alpha_0-\alpha_{ac0}) \\ 0 & \frac{-1}{L} & \frac{M_0K}{4L}cos(\alpha_0-\alpha_{ac0}) & \frac{M_0KM_{ac0}}{4L}sin(\alpha_0-\alpha_{ac0}) \end{bmatrix} \begin{bmatrix} \Delta v_d^- \\ \Delta v_q^- \\ \Delta M_{ac} \\ \Delta \alpha_{ac} \end{bmatrix}$$

Based on equation (5-41), the transfer function of $\frac{\Delta i_d^-}{\Delta M_{ac}}$, $\frac{\Delta i_d^-}{\Delta \alpha_{ac}}$, $\frac{\Delta i_q^-}{\Delta M_{ac}}$, and $\frac{\Delta i_q^-}{\Delta \alpha_{ac}}$ are calculated in the following equations (Subscript 0 denotes the steady state values):

$$\frac{\Delta i_d^-}{\Delta M_{ac}} = \frac{KM_0\sin(\alpha_{ac0})(R+Ls) - KLM_0\omega_0\cos(\alpha_{ac0})}{4(L^2s^2 + L^2{\omega_0}^2 + 2LRS + R^2)} \quad (5\text{-}42)$$

$$\frac{\Delta i_d^-}{\Delta \alpha_{ac}} = \frac{KM_0M_{ac0}\cos(\alpha_{ac0})(Ls+R) + KLM_0M_{ac0}\omega_0\sin(\alpha_{ac0})}{4(L^2s^2 + L^2{\omega_0}^2 + 2LRS + R^2)} \quad (5\text{-}43)$$

$$\frac{\Delta i_q^-}{\Delta M_{ac}} = \frac{KM_0\cos(\alpha_{ac0})(R+Ls) + KM_0L\omega_0\sin(\alpha_{ac0})}{4(L^2s^2 + L^2{\omega_0}^2 + 2LRs + R^2)} \quad (5\text{-}44)$$

$$\frac{\Delta i_q^-}{\Delta \alpha_{ac}} = \frac{KLM_0M_{ac0}\omega_0\cos(\alpha_{ac0}) - KM_0M_{ac0}\sin(\alpha_{ac0})(Ls+R)}{4(L^2s^2 + L^2{\omega_0}^2 + 2LRS + R^2)} \quad (5\text{-}45)$$

To analyze the proposed controller stability, we have to make sure that the output of the negative sequence controller does not lead to infinite negative sequence current. In the proposed controller, the M_{ac} is the product of the PI controller output and the amplitude of the 2nd harmonic oscillations of the q-axis component of the tie line current in the positive synchronous frame as shown in Figure 5-13. To simplify the stability analysis and without loss of generality, the amplitude of the 2nd harmonic oscillations of the q-axis component of the tie line current is replace by a variable gain of K_c. Then we vary the K_c from zero to very high value, and for each value of the K_c, we have to make sure that the closed loop poles of the compensated $\frac{\Delta i_d^-}{\Delta M_{ac}}$ and $\frac{\Delta i_q^-}{\Delta M_{ac}}$, do not have positive real part. The block diagram of the

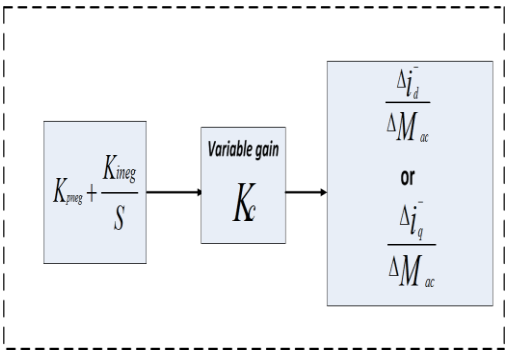
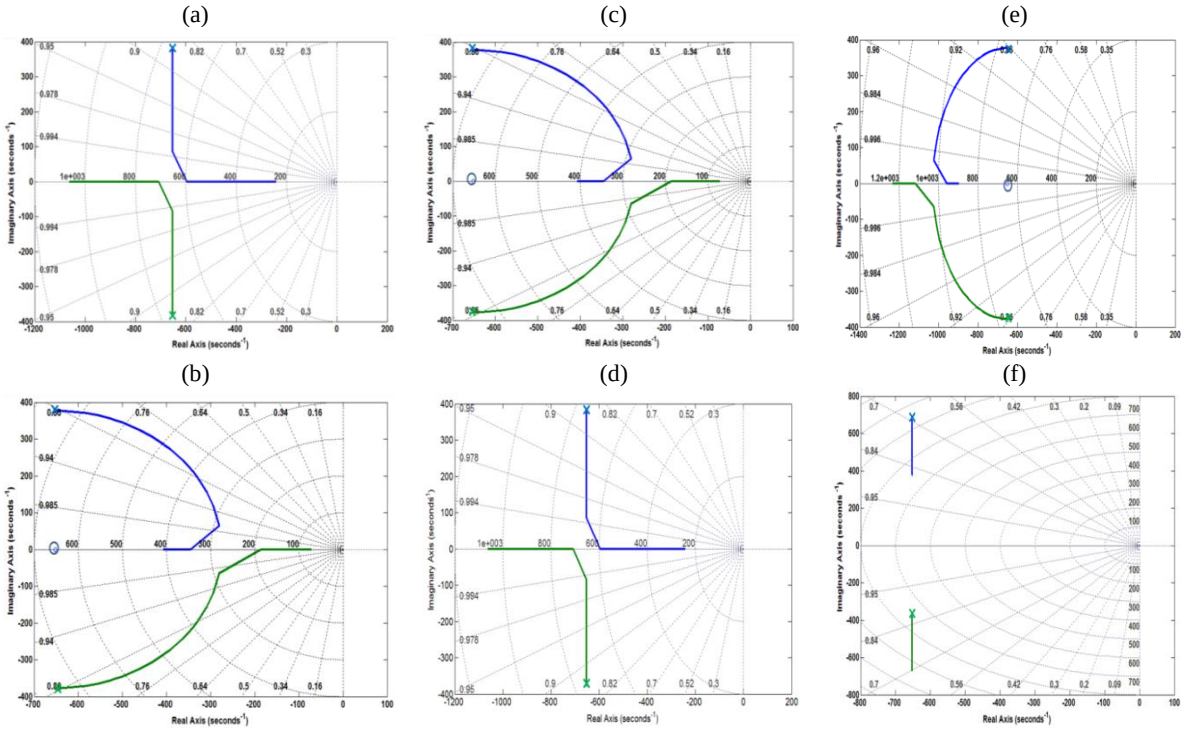


Figure 5-14. Block diagram of the compensated $\frac{\Delta i_d^-}{\Delta M_{ac}}$ and $\frac{\Delta i_q^-}{\Delta M_{ac}}$

compensated $\frac{\Delta i_d^-}{\Delta M_{ac}}$ and $\frac{\Delta i_q^-}{\Delta M_{ac}}$ are shown in Figure 5-14. Exactly the same values of the K_{pneg} and K_{ineg} which were used in the simulation and Hardware-In-the-Loop test have been used here. The root locus of the compensated $\frac{\Delta i_d^-}{\Delta M_{ac}}$ and $\frac{\Delta i_q^-}{\Delta M_{ac}}$ when K_c is varied from zero to a high value for three different values of α_{ac0} i.e. 0, 90, and -90 are depicted in the Figure 5-15. As can be observed in this figure, closed loop poles of the compensated $\frac{\Delta i_d^-}{\Delta M_{ac}}$ and $\frac{\Delta i_q^-}{\Delta M_{ac}}$ never go to the right half plane that validates the stability of the proposed controller.

5.6 PSCAD Simulation Results

In this part, PSCAD/EMTDS simulation of the 2-level PWM controlled VSC-based STATCOM, which used in the previous section for controller stability analysis, has been used to verify the proposed controller performance. This STATCOM has been deployed to fulfill the reactive power support functionality for one sensitive load. Passive filters are used to improve the STATCOM current Total harmonic Distortion (THD). The single line diagram of the simulated test system is demonstrated in Figure 5-16. Table 5-1 indicates the



Closed loop poles of the compensated $\frac{\Delta i_d^-}{\Delta M_{ac}}$ (a) and $\frac{\Delta i_q^-}{\Delta M_{ac}}$ (b)when α_{ac0}= 0

Closed loop poles of the compensated $\frac{\Delta i_d^-}{\Delta M_{ac}}$ (c) and $\frac{\Delta i_q^-}{\Delta M_{ac}}$ (d) when α_{ac0}= 9 0

Closed loop poles of the compensated $\frac{\Delta i_d^-}{\Delta M_{ac}}$ (e) and $\frac{\Delta i_q^-}{\Delta M_{ac}}$ (f) when α_{ac0}= -9 0

Figure 5-15. Closed loop rout locus of the compensated $\frac{\Delta i_d^-}{\Delta M_{ac}}$ and $\frac{\Delta i_q^-}{\Delta M_{ac}}$ with three different values of α_{ac0} i.e. 0, 90, and -90

test system parameters. Figure 5-17 demonstrates the STATCOM performance with and without proposed controller under single line to ground (SLG) fault at phase a, right at load bus. The STATCOM is operating in the capacitive mode. I_{dneg} and I_{qneg} represent the negative sequence STATCOM tie line current d and q axis components in negative synchronous frame respectively. After applying fault at t=0.6 second the negative sequence current reaches from zero to about 28 amps when the STATCOM is working with conventional PWM controller and injecting 8 amps of capacitive current to the grid. In contrast with conventional controller, negative sequence current reaches only to 7 amps after applying fault when

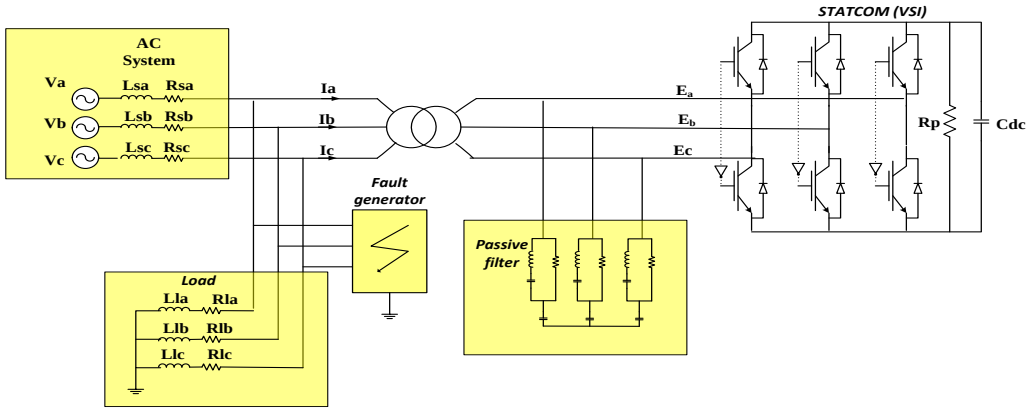


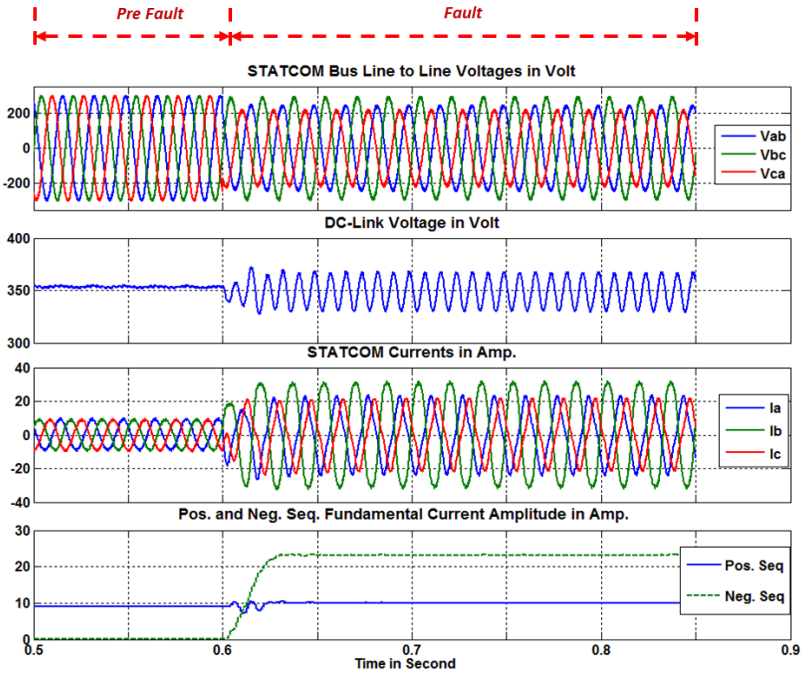
Figure 5-16. Single line diagram of the simulated test system

Table 5-1 Test system parameters

Parameters	Values
Fundamental frequency	*60 Hz*
Source voltage	*208 V LL rms*
Source inductance	*1.5 mH*
Switching frequency	*1260 Hz*
DC capacitor	*1000 μF*
DC-link voltage	*350 V*
Estimated inverter loss resistance	*4000 Ω*
Transformer leakage inductance	*2.3 mH*
Transformer copper loss resistance	*1.5 Ω*

STATCOM is equipped with proposed controller. DC- link voltage oscillations are also lower. This reduction in negative sequence current decreases the fault peak current from about 36 amps at phase b in case of STATCOM with conventional controller to less than 14 amps in case of STATCOM with proposed controller. The same scenario which was used to verify the controller performance in capacitive mode has been used to evaluate the proposed controller performance in inductive mode of operation. As can be observed in Figure 5-18 associated with inductive mode of operation, significant negative sequence and consequently fault peak current reduction is obtained in case of STATCOM with proposed controller comparing to the STATCOM with conventional controller.

(a)



(b)

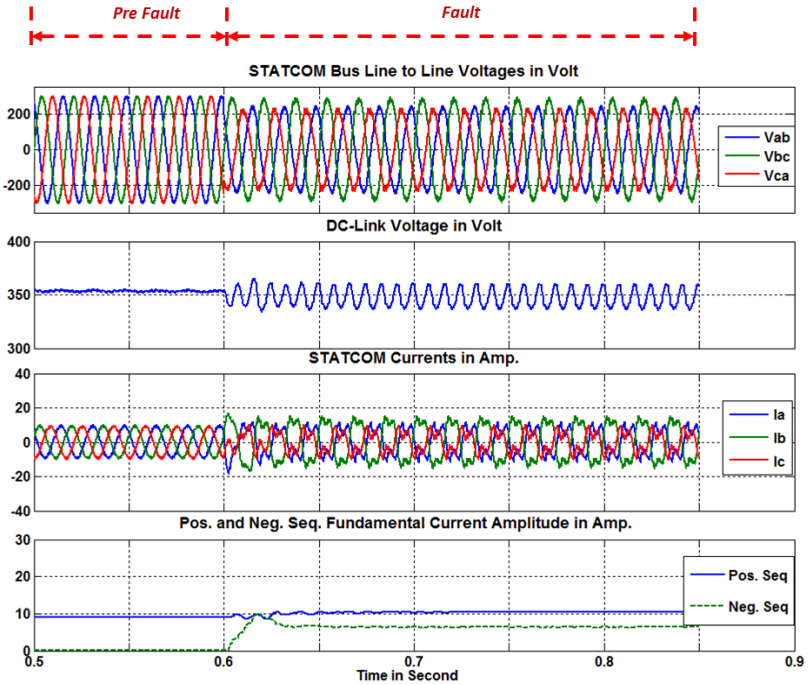
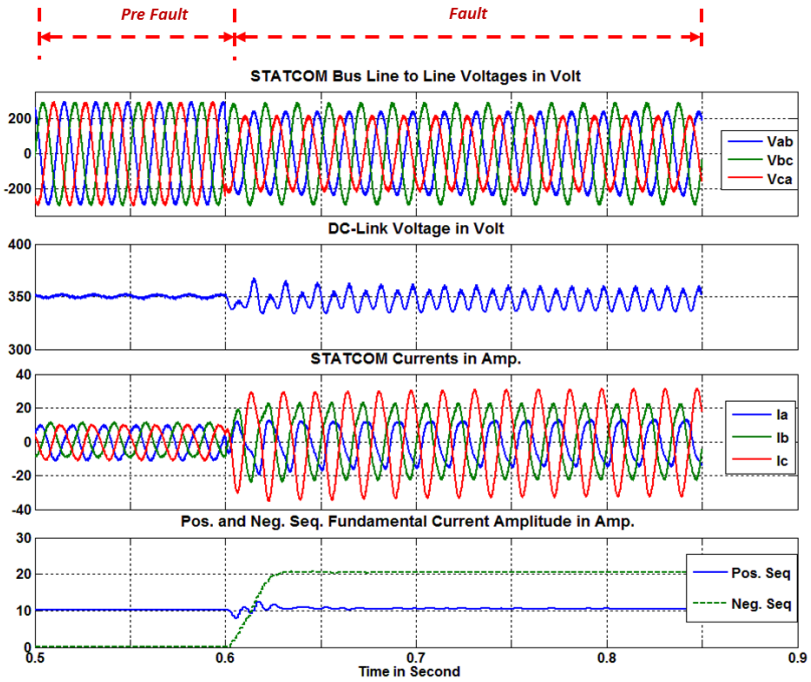


Figure 5-17. STATCOM performance with (b) and without (a) proposed controller when STATCOM is working in capacitive mode

(a)



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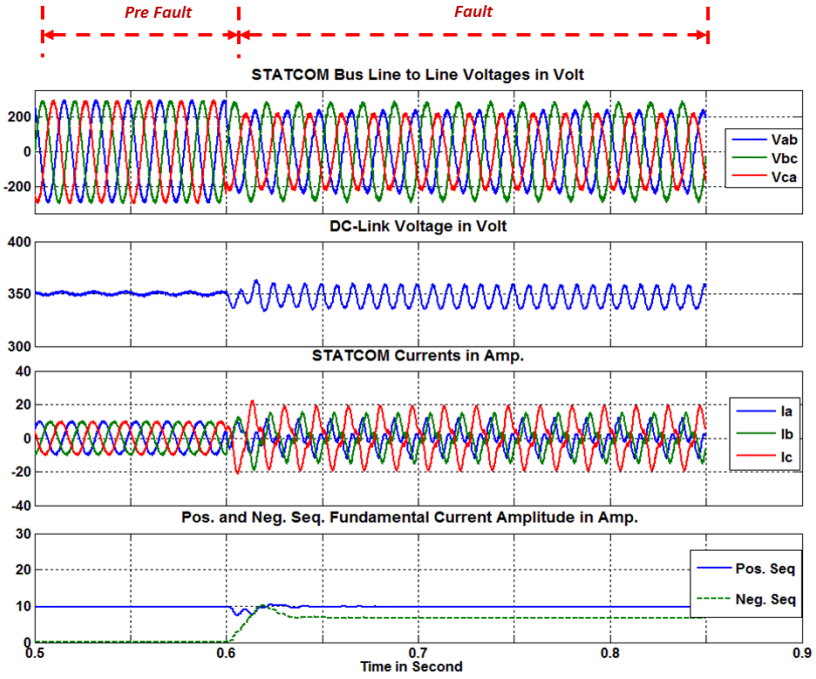


Figure 5-18. STATCOM performance with (b) and without (a) proposed controller when STATCOM is working in inductive mode

5.7 Hardware-In-the-Loop- test

A Hardware-in-the-Loop test has been done to verify the proposed controller performance. Exactly the same test system used for PSCAD/EMTDC simulation has been emulated in the Typhoon HIL (Hardware-in-the-Loop testing equipment). The converter firing signals are being generated in an external controller which is properly communicating with Typhoon HIL via an interface board as shown in Figure 5-19.

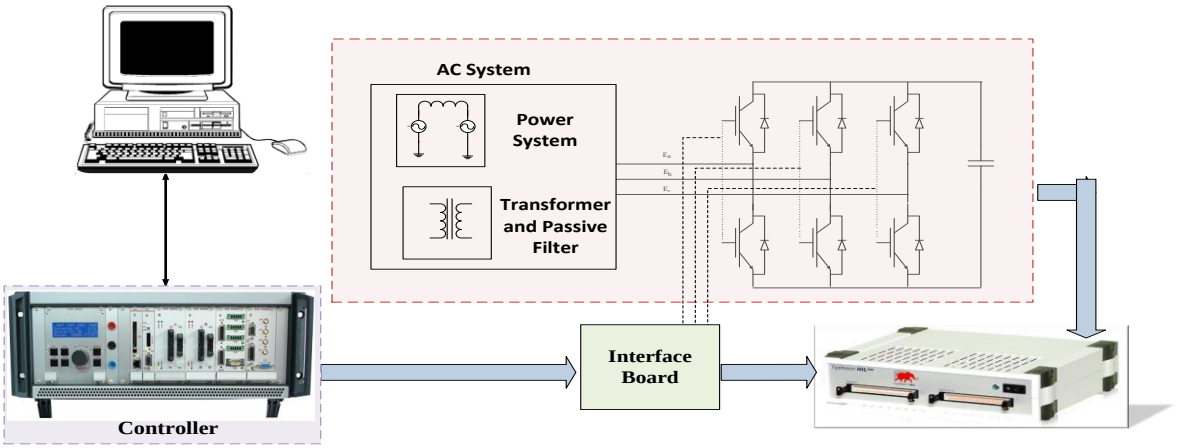


Figure 5-19. Hardware-in-the-Loop test system

Figure 5-20, and Figure 5-21 demonstrate the STATCOM fault performance without and with the proposed controller when the STATCOM is working in capacitive mode of operation respectively. Like the simulation verification, attention has been taken to the SLG fault right at load bus at phase a. As can be observed in these figures, the value of the negative sequence current, in the case of STATCOM with proposed controller, is less than of half of its value when the STATCOM is working with conventional controller. The fault

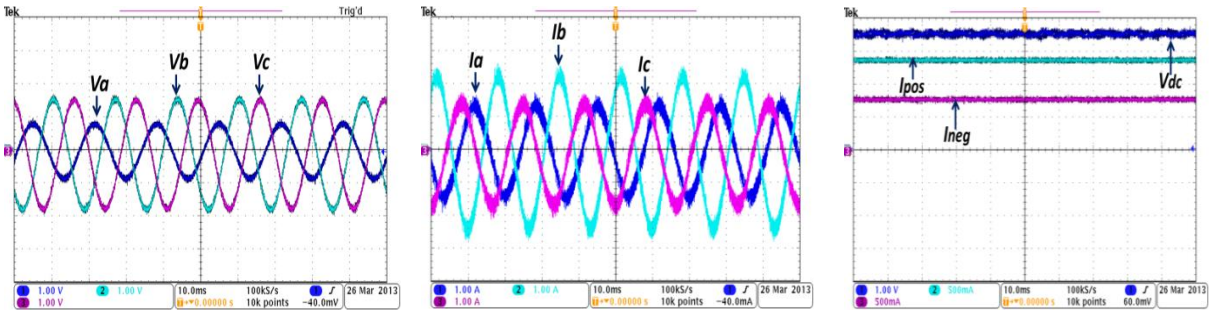


Figure 5-20. Capacitive mode performance of the STATCOM under SLG fault without proposed controller. Voltage scale: 100V/div. and Current scale:5A/div.

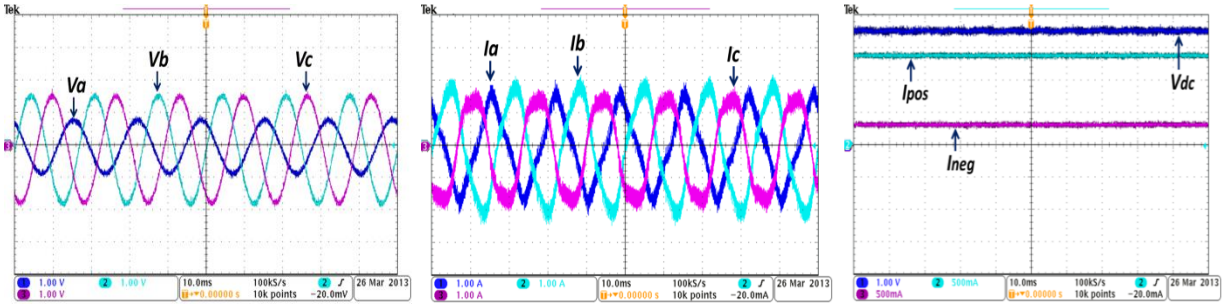


Figure 5-21. Capacitive mode performance of STATCOM under SLG fault with proposed controller. Voltage scale: 100V/div. and Current scale:5A/div.

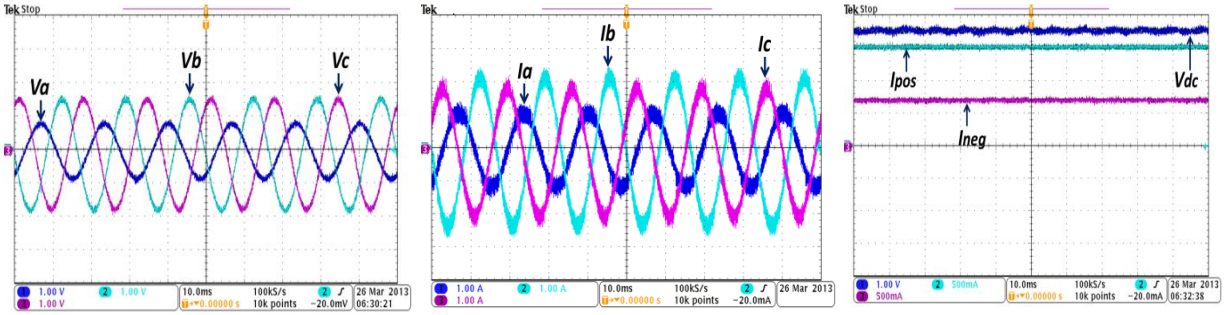


Figure 5-22. Inductive mode performance of STATCOM under SLG fault without proposed controller. Voltage scale: 100V/div. and Current scale:5A/div.

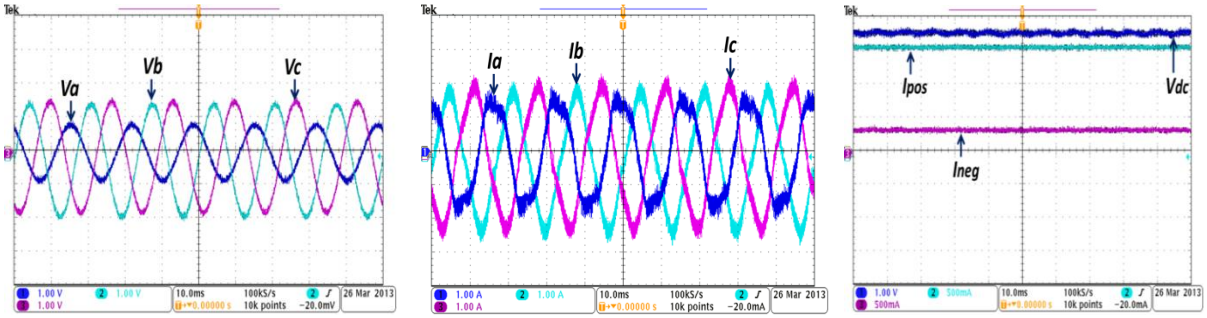


Figure 5-23. Inductive mode performance of the STATCOM under SLG fault with proposed controller. Voltage scale: 100V/div. and Current scale:5A/div.

peak current is also decreased with proposed controller comparing to the conventional controller. The same test which was applied to the STATCOM in capacitive mode of operation has been used to verify the proposed controller performance when the STATCOM is working in inductive mode of operation. As can be observed in Figure 5-22, and Figure 5-23, associated with inductive mode of operation, the negative sequence current with proposed controller reaches to the half of its value comparing to the case of the STATCOM with conventional controller.

5.8 Summary

PWM controlled VSC-based STATCOMs are commonly used for the purpose of voltage regulation and power factor correction in the distribution level. In spite of superior feature of fast voltage regulation and reactive power support functionality, VSC-based STATCOMs have the major drawback of being sensitive to the grid disturbances, especially the unbalanced condition and grid faults. Moreover, when the STATCOMs are used in the Distributed Generation (DG) applications or reactive power support of the sensitive industrial load, the unbalanced condition becomes even more intolerable. This chapter proposed an

alternative control structure to keep the VSC-based STATCOM online during the unbalanced condition and system faults by limiting the negative sequence current. This eliminates the need to redesign/overdesign of the STACOM power components and over rating of the semiconductor switches to operate under fault current. Proposed controller performance was verified by simulation and Hardware-In-the-Loop test.

APPENDIX

5.9 Appendix 5-A

The 2nd harmonic oscillations of the q component of STATCOM current in positive synchronous frame due to negative sequence current was calculated as in (5-36). As discussed in section 5.4, adding 2nd harmonic oscillations in phase with signal of equation (5-36) to α, generates a 90˚ lagging 2nd harmonic oscillation at DC-link voltage as:

$$A\cos\left(2\omega t+\frac{\pi}{2}-\theta_i^-\right) \tag{5-46}$$

As discussed in section 5.3, interaction between the VSC switching function and DC-Link voltage oscillations of equation (5-46) generates a negative sequence voltage as in (5-47) at STATCOM terminal. Positive and negative signs are related to negative sequence current initial phase respecting to STATCOM bus negative sequence voltage ($\theta_i^- \approx \theta_v^- \pm \frac{\pi}{2}$).

$$\pm A'\sin(-\omega t+\alpha+\theta_v^-) \tag{5-47}$$

Considering that α is almost zero, the negative sequence voltage of the equation (5-47) is in the same phase as postulated STATCOM bus negative sequence voltage source under fault conditions.

Chapter6: Instantaneous Fault Current Limiter for PWM-Controlled VSCs Faults

6.1 Introduction

VSCs (shown in Figure 6-1) are now widely used in many grid-connected applications including FACTS devices, Dynamic Voltage Restore (DVRs) and as active interfaces for Distributed Generation (DG) systems (for instance photovoltaic, wind, fuel cells and micro turbines). Benefits of using a VSC are sinusoidal grid currents and high controllability of both active and reactive power. PWM-controlled VSC have the major drawback of being sensitive to the grid disturbances especially the unbalanced condition and system faults [68]. Unbalanced input voltage produces large negative sequence current flow into the converter which results in oscillations with frequency equal to twice of the AC-system frequency on the DC-link voltage [29][40],[39], and [40]. This negative sequence current flow might damage the semiconductor switches. Basically the inverter power components and switches must be designed for the peak continuous operating current and for the peak continuous operating voltage. Generally there is a designed margin beyond this point to accommodate some percentage overload as well as specified abnormal operating condition particularly unbalanced condition and grid faults. The MVA rating of the equipment and hence the cost is derived from the product of peak voltage and current (considering the fault and unbalanced condition), regardless of whether they occur at the same time or not[26]. Hence, the appropriate controller which is capable of limiting the fault current and consequently

decrease the converter design margin will significantly reduce the converter equipment rating and cost.

Beside the negative sequence voltage, the input voltage distorted with other harmonics also causes converter performance deterioration by generating harmonics on the DC-link voltage. These DC-link voltage harmonics will be reflected as other harmonics at the VSC output terminals and will exacerbate the current THD.

Different solutions have been proposed by the researchers to improve the PWM-controlled VSC performance under unbalanced conditions [36]-[54] . These are focused on mainly generating the current reference in both positive and negative synchronous frame. The calculated current references will pass through a controller which generates the required reference voltage to regulate the power or voltage at the point of common coupling (PCC)[25].

This part of the thesis presents an alternative solution to improve the PWM-controlled VSC performance under unbalanced conditions and system faults and also under distorted input voltage condition caused by other harmonics rather than the negative sequence voltage. This solution is based on direct calculation of the reference voltage without using current regulator. Under unbalanced input voltage and AC-system faults, the proposed controller calculates the reference negative sequence voltage which is required to be generated at VSC output terminals to force the negative sequence current to zero. This negative sequence voltage reference is obtained by simple measurement and scaling in abc time domain without using current regulator. This simple voltage reference calculation makes the proposed solution very simple and fast. Using the same procedure, the proposed solution is also-

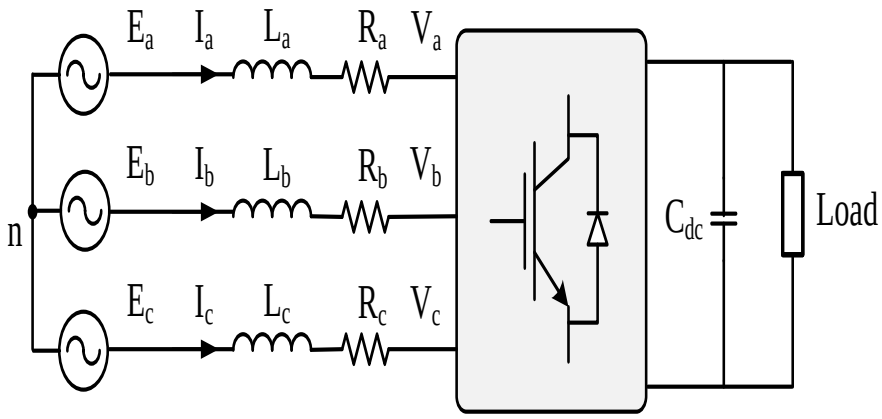


Figure 6-1. VSC connected to the grid

-capable to directly calculate the other harmonic voltage reference beside the negative sequence voltage to force that specific harmonic current flow to zero. This instantaneous selective current harmonic elimination improves the converter current THD and consequently leads to smooth and stable DC-link voltage.

6.2 Proposed Control Structure

Basically, the unbalanced AC-system conditions can be emulated by postulating a set of negative sequence voltage source in series with VSC tie line [19]as shown in Figure 6-2.The basic idea of the proposed solution under unbalanced condition and AC-system faults is to generate the required fundamental negative sequence voltage vector at the VSC output terminals to attenuate the effect of postulated negative sequence bus voltage. The generated negative sequence voltage, results in reduction of the negative sequence current seen by the VSC under fault conditions. The reference negative sequence voltage is obtained based on the direct measurement and scaling of the PCC negative sequence voltage. When an AC-system fault occurs, negative sequence voltage is generated at the PCC. This generated

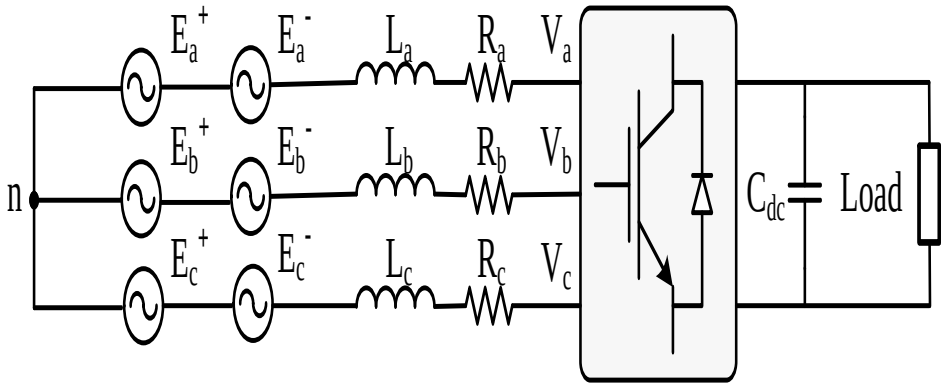


Figure 6-2. Converter equivalent circuit with series negative sequence voltage sources

negative sequence voltage is instantly measured and then controller commands the VSC to generate the same negative sequence voltage at the VSC output terminals to force the VSC negative sequence current to zero. Since the reference voltage calculation is carried out instantly, (without using current regulator) the controller is very simple and fast. It is also important to note that proposed solution is not dependent to the circuit components value. Theoretically, circuit components value and also ac-system topology do not affect the propose solution performance. The PCC negative sequence voltage is calculated as in (6-1)-(6-3) [66].

$$\begin{bmatrix} E_{an} \\ E_{bn} \\ E_{cn} \end{bmatrix} = \begin{bmatrix} E_a \\ E_b \\ E_c \end{bmatrix} - A_1 A_2 \begin{bmatrix} E_a \\ E_b \\ E_c \end{bmatrix} \tag{6-1}$$

where the E_{an}, E_{bn}, and E_{cn} are the negative sequence components of the PCC voltage. The matrix A_1 and A_2 are calculated as in (6-2) and (6-3).

$$\mathrm{A}_1 = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \tag{6-2}$$

$$A_2 = \begin{bmatrix} \frac{1}{2} & \frac{-1}{2j\sqrt{3}} & \frac{1}{2j\sqrt{3}} \\ -1 & 0 & -1 \\ \frac{-1}{2j\sqrt{3}} & \frac{1}{2j\sqrt{3}} & \frac{1}{2} \end{bmatrix} \tag{6-3}$$

The same procedure has been used to limit the higher current harmonics. Assume that current spectrum contains considerable amount of one specific harmonic which makes the converter current distorted and also generates oscillations on the DC-link voltage. This distorted condition can also be emulated by postulating a set of harmonic voltage sources in series with equivalent grid voltage sources. The proposed controller commands the converter to generate that specific harmonic voltage. This generated harmonic voltage must have the same amplitude and phase as of the PCC harmonic voltage. Similar to fault conditions, voltage reference calculation for that specific harmonic is carried out by direct measurement. Harmonic extraction is fulfilled using transformation to synchronous reference frame at selected harmonic frequency and passing the transformed signal through a low pass filter. Finally the filtered signals will be transformed to the abc domain. The proposed solution has been conceptually illustrated in Figure 6-3. As can be observed in this figure the proposed control scheme has been added to the conventional controller which generates the positive sequence voltage reference for a PWM-controlled rectifier. The positive sequence voltage reference is calculated using two PI controller that regulate the d and q component of the rectifier current [38]. Basically the active and reactive powers in the synchronous reference frame are calculated as in:

$$P = \frac{3}{2}(e_d i_d + e_q i_q) \tag{6-4}$$

$$Q = \frac{3}{2}(e_q i_d - e_d i_q) \tag{6-5}$$

The reference reactive power is set to zero to have a unity power factor. The reference active power is calculated such that the DC-link voltage remains constant at the DC-link voltage reference value. As can be observed in Figure 6-3 the reference active power is calculated using a PI controller that regulates the DC-link voltage. Having calculated the reference active and reactive power, the reference i_d and i_q are calculated as in [38] :

$$\begin{bmatrix} i_d^* \\ i_q^* \end{bmatrix} = \frac{2P^*}{3D} \begin{bmatrix} e_d \\ e_q \end{bmatrix} \tag{6-6}$$

Where

$$D = ({e_d}^2 + {e_q}^2) \tag{6-7}$$

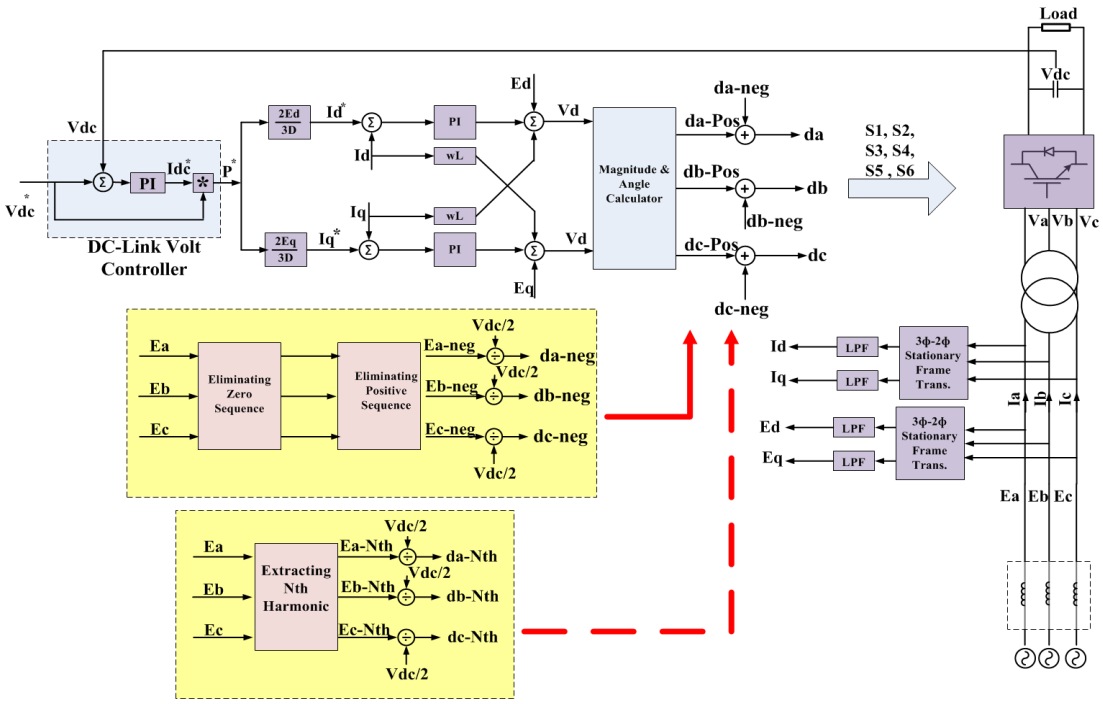


Figure 6-3. Proposed control structure

6.3 PSCAD simulation results

This part of the paper presents the PSCAD verification of the controller. The control structure of Figure 6-3 has been implemented on a PWM-controlled rectifier. This rectifier is connected to the grid through a transformer. Single line diagram of the simulated test system is demonstrated in Figure 6-4. Table 6-1 summarizes the test system parameters.

To verify the basic idea of the controller, one set of negative sequence voltage sources has been added in series with the grid voltage sources. These negative sequence voltage sources mimic the steady state of the AC-system under fault condition. The AC-system faults dynamics will be investigated later in this chapter when different kinds of the faults are applied at different location of the AC-system. Figure 6-5-(a) demonstrates the converter waveforms with and without the proposed controller when there is a negative sequence voltage injection in series with the AC-system voltage sources. Initially the system works with conventional controller and AC-system is balanced. At t=0.3 seconds the negative sequence voltage as big as 20% of the system nominal voltage is injected to the AC-system. Converter is still controlled with conventional controller. At t=0.45 seconds the proposed solution starts to work and forces the negative sequence current to around zero and reduces the fault peak current. Decrease in the negative sequence current flow results in dramatic reduction of the DC-link voltage 2^{nd} harmonic oscillations.

The proposed controller capability to eliminate the other current harmonic besides the negative sequence has also been verified by simulation results. This time one set of voltage sources with frequency equal to three times of the line frequency is added in series with the

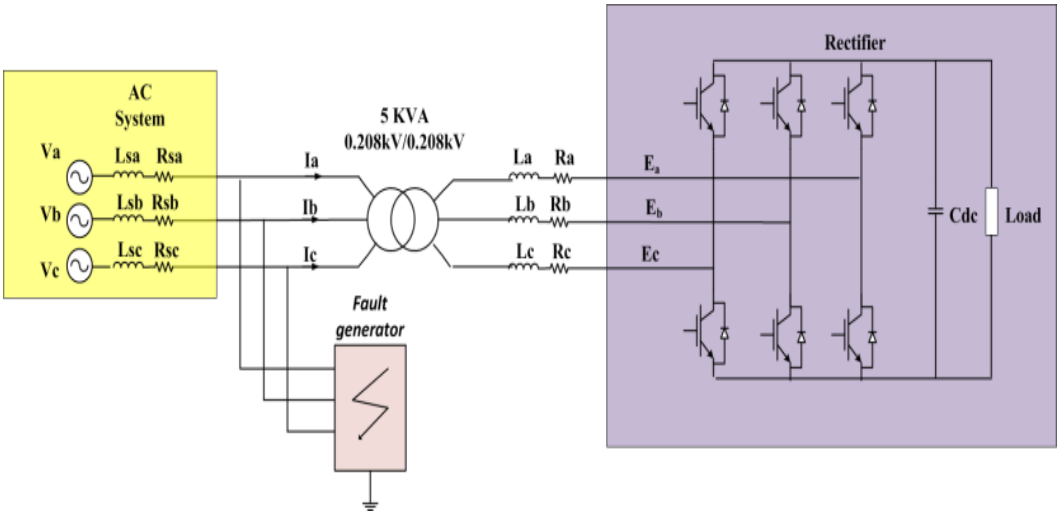


Figure 6-4. Single line diagram of the simulated test system

Table 6-1. Test system parameters

Parameters	Values
Fundamental frequency	*60 Hz*
Source voltage	*208V-LL rms*
Source inductance	*1.5 mH*
Switching frequency	*5 k Hz*
DC capacitor	*1000 μF*
DC-link voltage	*350 V*

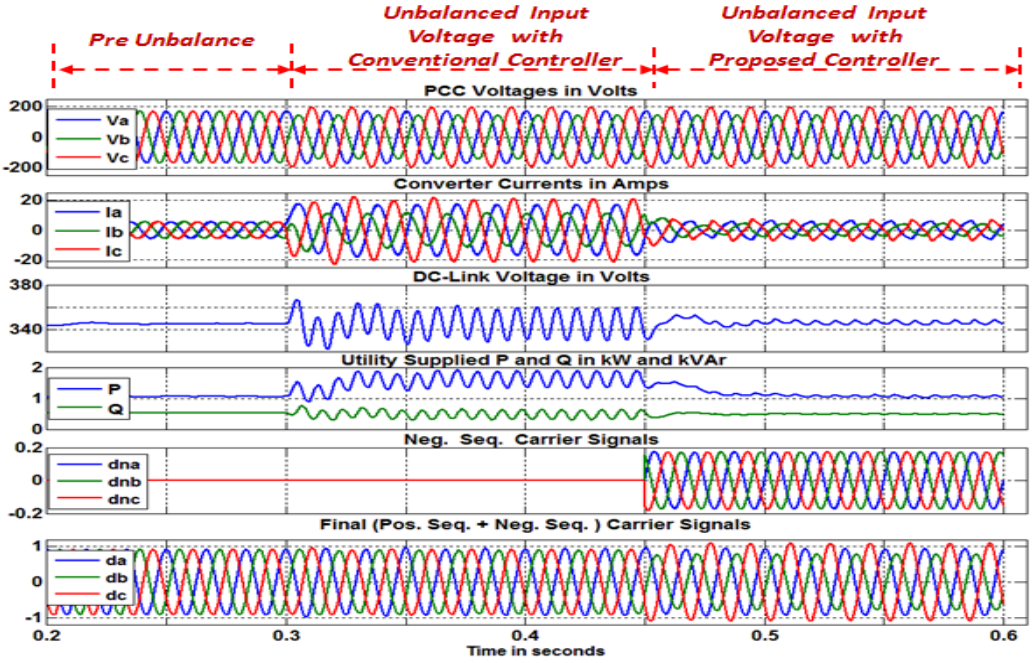
grid voltage sources. Figure 6-5-(b) demonstrates the same results as in Figure 6-5-(a) for the time that 3rd harmonic voltage as big as 20% of the system nominal voltage is being injected in to the AC-system. As can be observed in this figure, after applying the 3rd harmonic voltage injection at t=0.3 seconds, the converter current becomes distorted. These current harmonics generate severe oscillations on the DC-link voltage. However, when the converter starts to work with the proposed controller at t=0.45 seconds, the current distortion is decreased dramatically. The controller reduces the 3rd harmonic current by commanding the

converter to generate the 3rd harmonic voltage with appropriate amplitude and phase at the VSC output terminals. The amplitude and phase of this generated 3rd harmonic voltage are the same as the injected 3rd harmonic voltage in series with the grid voltage sources. Results in Figure 6-5-(b) prove the capability of the proposed solution in limiting the 3rd harmonic current flow and consequently removing the DC-link voltage oscillations when the input voltage is distorted with 3rd harmonic voltage.

As mentioned earlier, the controller performance has also been verified under severe fault conditions. Figure 6-6 illustrates the converter performance with and without the proposed controller when there is a severe Single Line to Ground (SLG) fault at phase *A* right at PCC. As can be observed in Figure 6-6-(a), associated with converter with conventional controller, after applying fault at t=0.3 seconds the converter current increase dramatically due to the negative sequence current flow. The DC-link voltage oscillations are also very severe. In contrast with conventional controller, the converter fault performance with the proposed controller is improved dramatically when it works with proposed controller. The controller measures the PCC negative sequence voltage throughout the entire operation time and commands the converter to generate the same negative sequence voltage at its output terminals. This results in dramatic reduction of the negative sequence current as can be seen in Figure 6-6-(b).

In the presented simulation results in Figure 6-6, it was assumed that the proposed controller is in service throughout the entire time that the converter is in operation. This is the way that the controller is supposed to operate. Basically the controller is always under

(a)



(b)

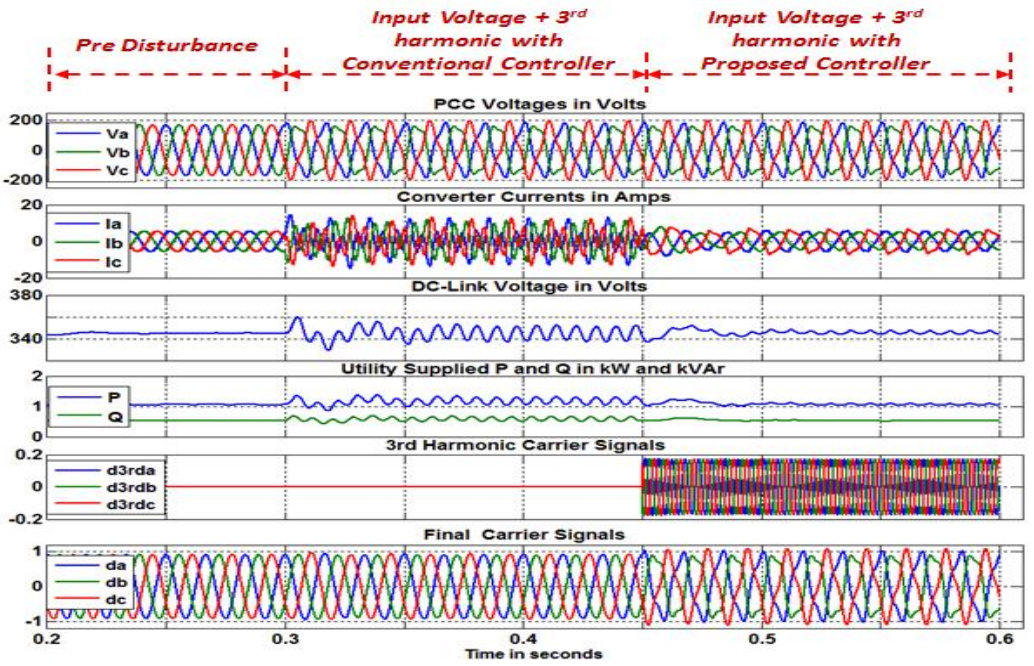
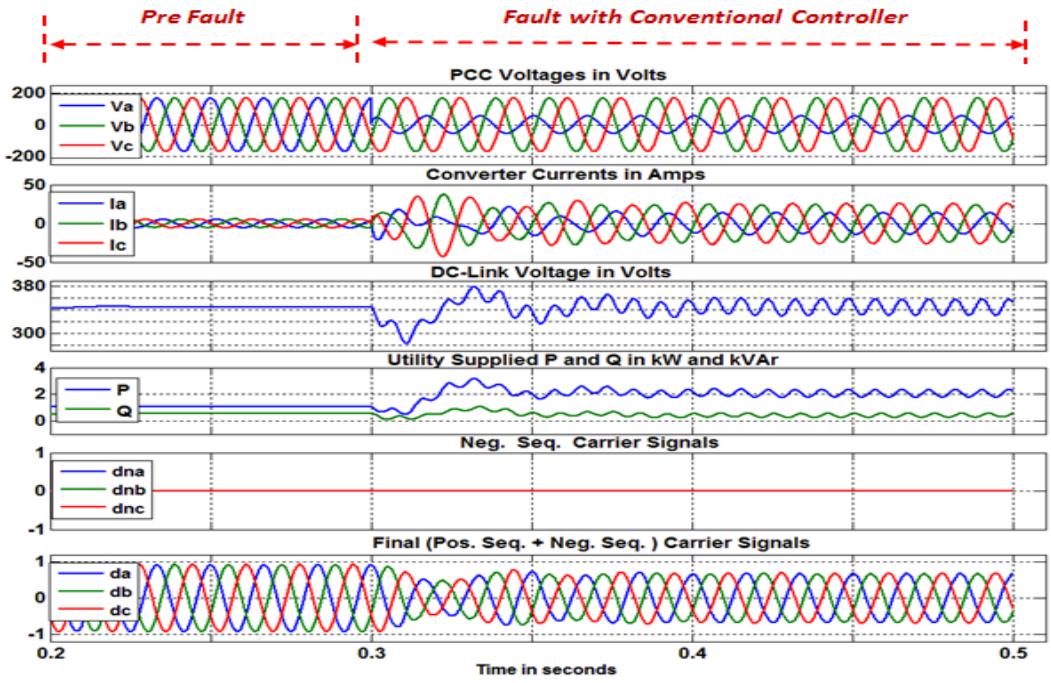


Figure 6-5. Converter performance with and without proposed controller when there is negative (a)/3rd harmonic (b) voltage injection as big as 20% of the nominal system voltage in series with grid AC sources

(a)



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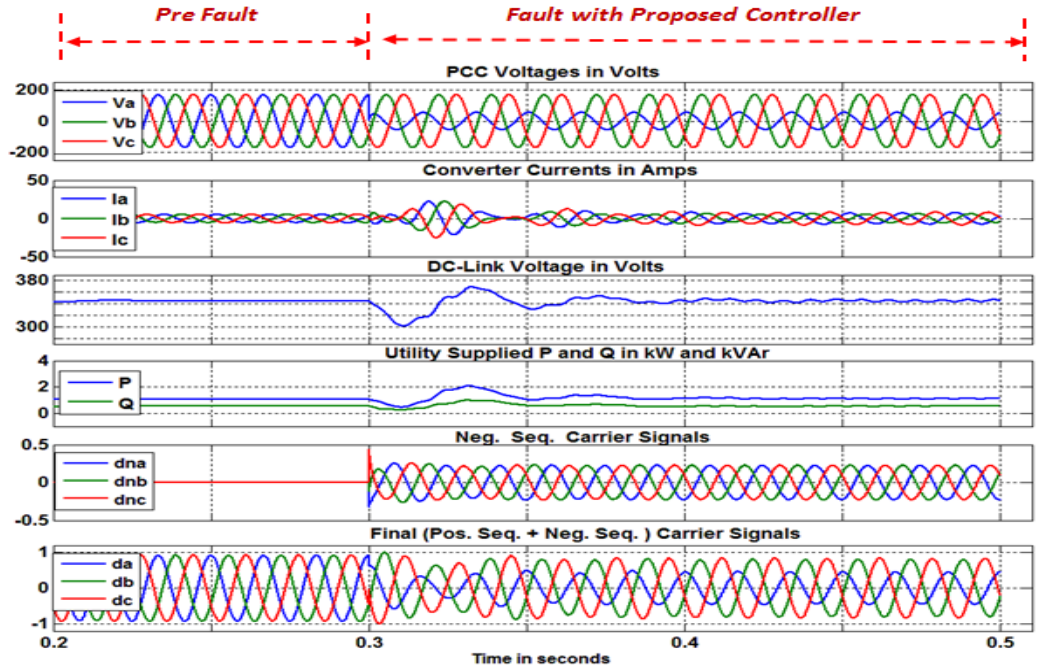

Figure 6-6. Converter performance with (b) and without (a) proposed controller under SLG fault at phase A right at PCC

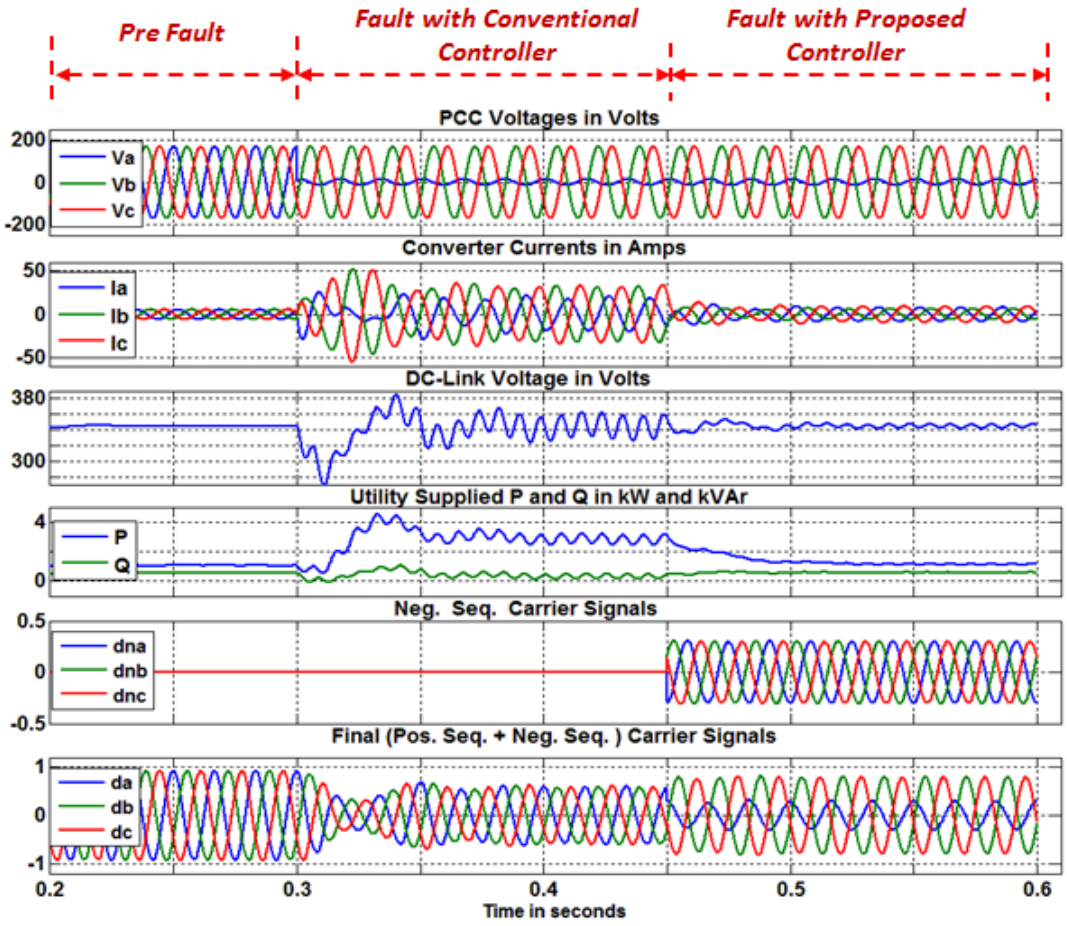

Figure 6-7. Converter performance with and without proposed controller under SLG fault at phase A right at PCC

operation and whenever it detects the negative sequence voltage at the PCC voltage will command the converter to generate the same negative sequence voltage. In another scenario, it is assumed that the converter initially works with the conventional controller. Fault is applied and after few cycles the converter starts to work with the proposed controller. This is the worst case that can happen and it is shown in Figure 6-7 that even under the worst case scenario the controller limits negative sequence current well. Basically, Figure 6-7

demonstrates the converter pre and post fault waveforms with and without the proposed controller when there is a SLG fault at phase *A* right at the PCC. Initially the system works with the conventional controller under balanced condition. At t=0.3 seconds SLG fault is applied and consequently the VSC current and DC-link become distorted. At t=0.45 seconds the proposed solution starts to work and commands the converter to generate the measured negative sequence voltage at its output terminals. As can be observed in this figure the negative sequence current and consequently fault peak current is deceased dramatically in case of converter with proposed controller compared to the case of converter with conventional controller. Decreased negative sequence current flow results in reduction of the DC-link voltage 2^{nd} harmonic oscillations.

6.4 Hardware-In-the-Loop- test

A Hardware-in-the-Loop test has been done to verify the controller performance. Exactly the same test system used for the PSCAD simulation has been emulated in the Typhoon HIL (Hardware-in-the-Loop testing equipment). The converter firing signals are being generated in an external controller which is properly communicating with Typhoon HIL via an interface board as shown in Figure 6-8.

Figure 6-9 demonstrates the steady state performance of the rectifier. The DC-link voltage is fixed at 350 V. As can be observed the DC-link voltage and also converter voltages and currents are exactly the same as the simulation results.

Figure 6-10- Figure 6-11 demonstrate the converter steady state fault performance with and without the proposed controller. Similar to the simulation verification, the fault is applied at phase *A* right at the PCC. Figure 6-10 and Figure 6-11 illustrate the PCC and DC-link

voltages and converter currents when it works with conventional controller. As can be seen in these figures, under SLG fault condition with conventional controller the negative sequence current and therefore the fault peak current is very large. The Dc-link voltage 2nd harmonic oscillation is also very severe.

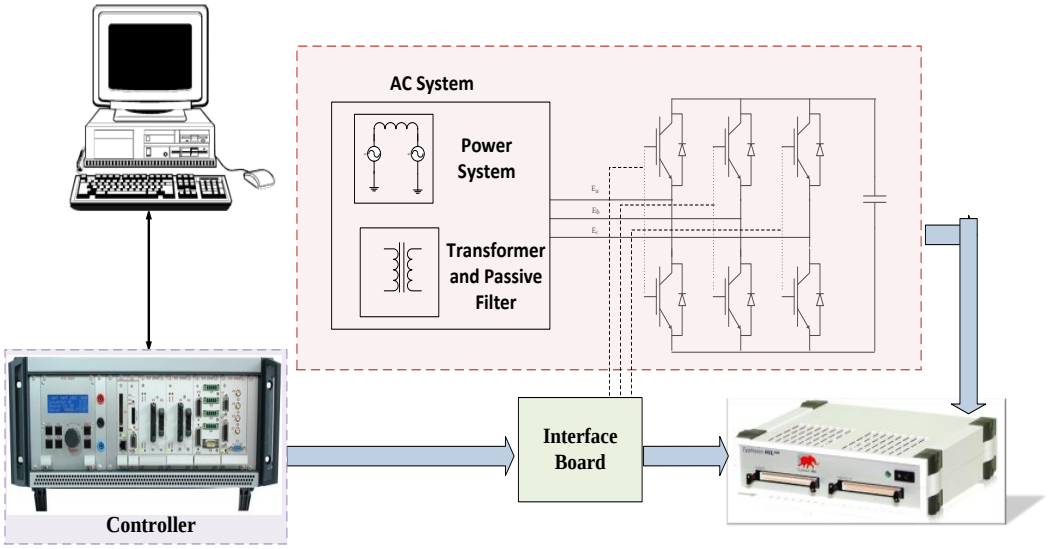

Figure 6-8. Hardware-in-the-Loop test system

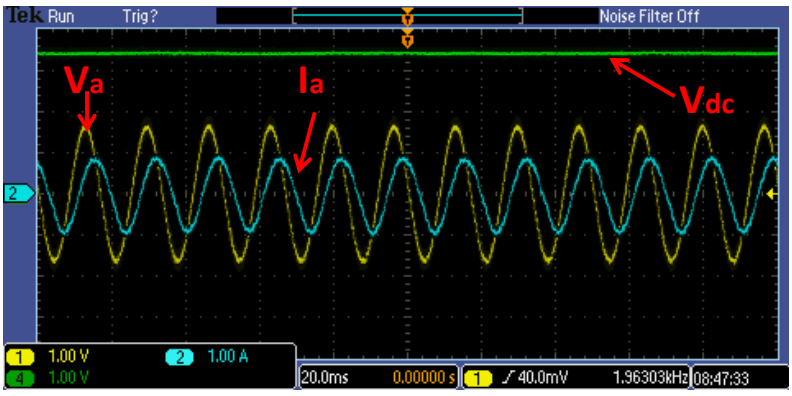

Figure 6-9. Rectifier voltages and current under normal condition. Voltage scale: 100V/div. and Current scale: 10A/div.

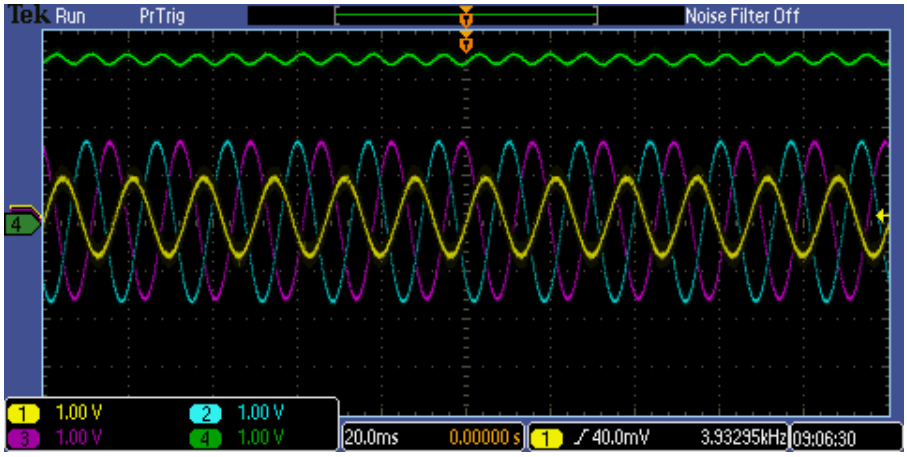

Figure 6-10. PCC and DC-link voltages under SLG fault at phase A when converter works with conventional controller. Chanel 1, 2, 3, and 4 indicate the Va, Vb, Vc, and DC-link voltage respectively. Voltage scale: 100V/div.

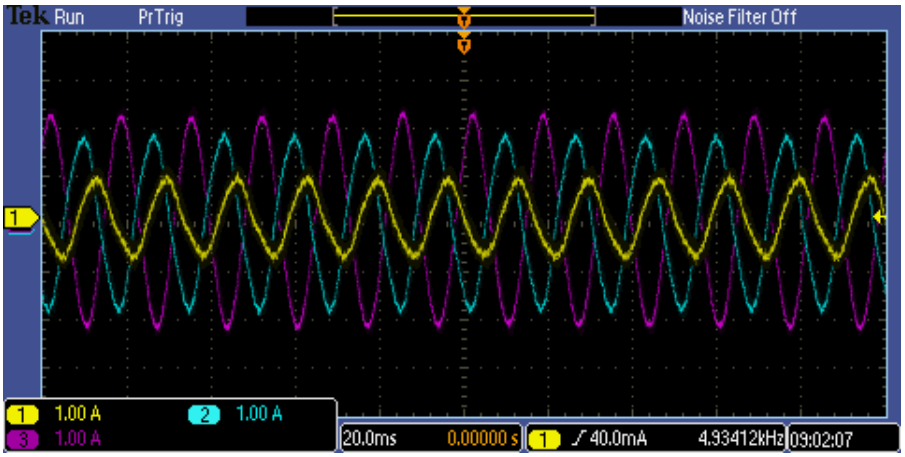

Figure 6-11. Converter currents under SLG fault at phase A when it works with conventional controller. Chanel 1, 2, and 3indicate Ia, Ib, and Ic respectively. Current scale:10A/div

By contrast, when the converter works with the proposed controller the negative sequence current is limited well. Reduced negative sequence current decreases the DC-link voltage 2nd harmonic oscillations. These results are depicted in Figure 6-12, and Figure 6-13.

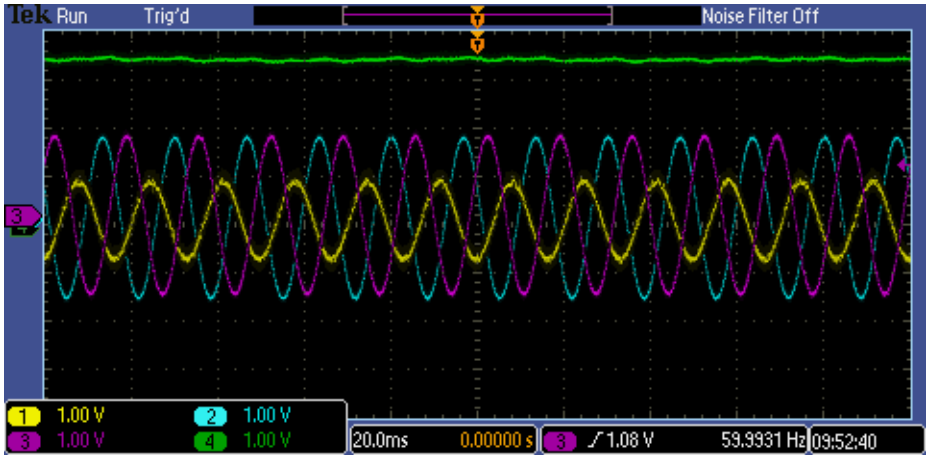

Figure 6-12. PCC and DC-link voltages under SLG fault at phase A when converter works with the proposed controller. Chanel 1, 2, 3, and 4 indicate the Va, Vb, Vc, and DC-link voltage respectively. Voltage scale: 100V/div.

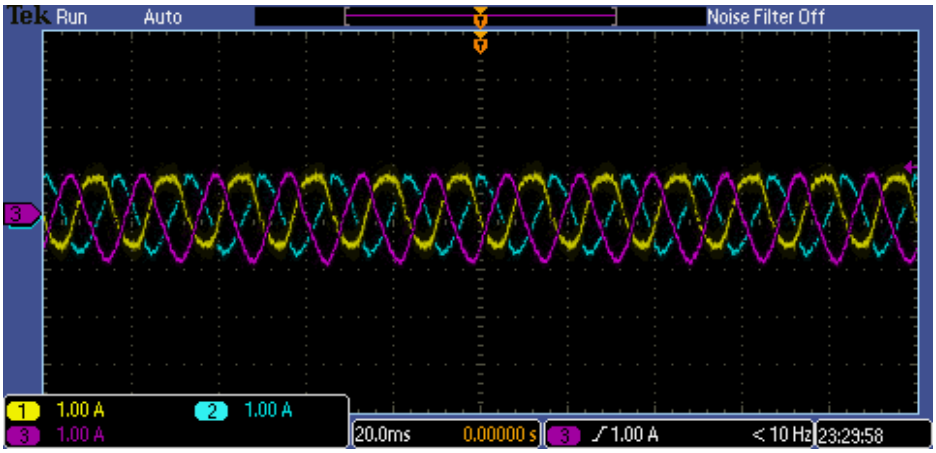

Figure 6-13. Converter currents under SLG fault at phase A when converter works with the proposed controller. Chanel 1, 2, and 3 indicate the Ia, Ib, and Ic respectively. Current scale:10A/div.

As can be observed in the simulation and Hardware-in-the-loop test results, applying SLG fault at phase A leads to a maximum fault current at phase C. To make a better comparison between the converter performance with and without the proposed controller, the

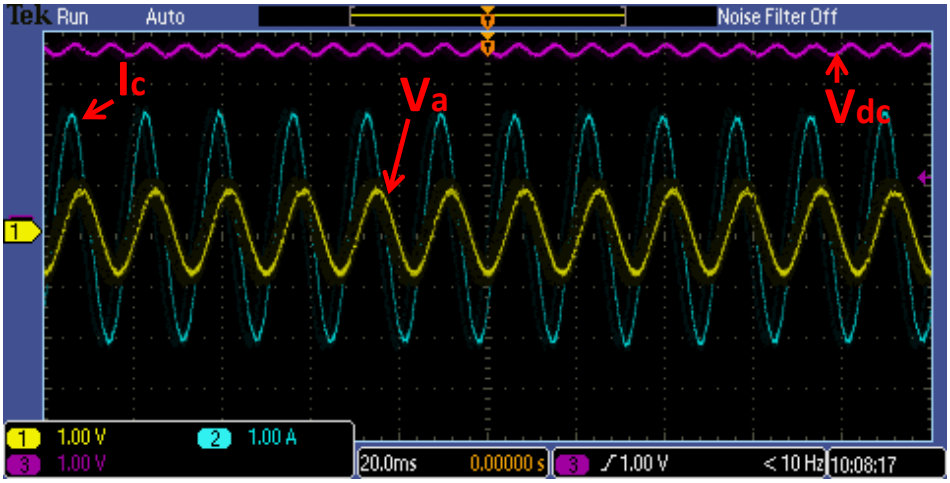

Figure 6-14. Converter performance with conventional controller under SLG fault at phase A. Voltage scale: 100V/div. and Current scale:10A/div

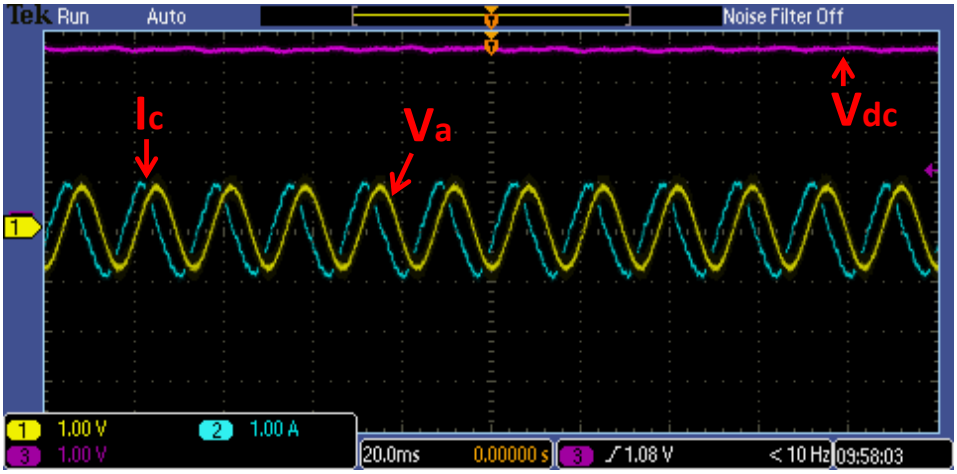

Figure 6-15. Converter performance with the proposed conroller under SLG fault at phase A. Voltage scale: 100V/div. and Current scale:10A/div.

phase C current and phase A and DC-link voltages are depicted separately in Figure 6-14, and Figure 6-15. As can be seen in these figures, the proposed controller limits the fault current at phase C dramatically. It is also important to note that the proposed controller keeps

the rectifier DC-link voltage smooth and stable at its reference value even under AC-system fault conditions.

6.5 Summary

The PWM-controlled VSCs are commonly used in industrial and utility applications. In spite of superior features of fast voltage regulation and stable DC-link voltage, PWM-controlled VSCs have the major drawback of being sensitive to the grid disturbances especially the unbalanced condition and system faults. Unbalanced input voltage generates large negative sequence current flow into the converter which results in oscillations with twice the line frequency on the DC-link voltage. Beside the negative sequence voltage, the input voltage distorted with other harmonics also causes converter performance deterioration by generating harmonics on the DC-link voltage. This Chapter presented an alternative solution to improve the PWM-controlled VSC performance under unbalanced conditions and system faults and also under distorted input voltage condition caused by other harmonics rather than the negative sequence voltage. The effectiveness of this solution was verified by simulation and Hardware-In-the-Loop test.

Chapter7: A control structure to increase the controllability range of the Unified Power Flow Controller

7.1 Introduction

Increasing the electric power demand and restrictions in the power system expansion due to the high cost and environmental issues urge the utility companies to deploy the devices which will increase the level of the power to be transmitted on the existing transmission lines. UPFC is the most versatile FACTS devices which can be used in the transmission level to increase the power transfer capability, operational functionality, and power flow controllability of the power system [76]-[94].

The UPFC generates a fully controllable voltage in both amplitude and phase in series with a bus which supplies an outgoing transmission line. This injected voltage will provide the capability of independent control of the active and reactive power flow through the transmission line. This unique feature of controlling power flow in desired amount can benefit the power system operators in different ways. It can be used to mitigate the power system congestion by decreasing the power flow of an over loaded line. It can also be used to increase the power flow of a critical tie line up to its thermal limit without a decrease in the stability margin. The increasing interest in the electricity market deregulation also makes the control of the power flow into the specific corridor of the AC system more important than the past.

It is the intention of this chapter of the thesis to describe the basic principle of the UPFC operation and to discuss the different control strategy appropriate for a high power transmission level UPFC installation. The close attention has been taken to the specific type of the UPFC in which the DC-link voltage is not constant but regulated over a range of the values. Most of the existing UPFC installations around the world are of this kind. And finally a control structure has been proposed to increase the operational limit of this kind of the UPFCs. Proposed controller performance has been verified by precise PSCAD simulation results.

7.2 Basic principle of the UPFC

Figure 7-1 indicates a simplified schematic of a UPFC. AS can be observed in this figure, the main features are two inverters. One is connected in series with transmission line through a series insertion transformer and the other one is connected in parallel with the line through a shunt insertion transformer. These two inverters are coupled to each other through a common DC-link. The series inverter injects a synchronous controllable voltage in series with transmission line to control the active and reactive power. The injected voltage vector can have different angles with respect to the transmission line current vector. Therefore in the process of injecting voltage, series inverter, exchange active and reactive power with transmission line [26]. The reactive power is supplied by the series inverter. Shunt inverter is in charge of injecting (in both directions) series inverter required active power into the DC-link from the transmission line. The series inverter then uses this transmitted power to the DC-link to interchange with transmission line. Basically, the UPFC exchanges the active power with transmission line in both direction based on the series inverter demand through

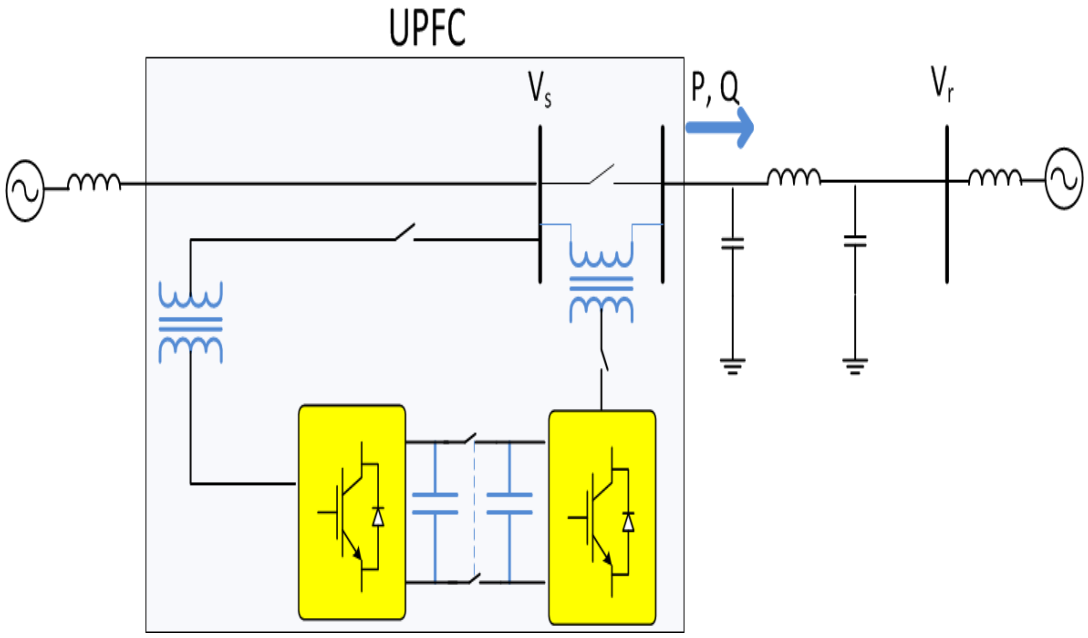

Figure 7-1. UPFC single line

the shunt inverter. Therefore, ignoring the converter losses, the net active power exchange between the UPFC and transmission line is zero[26].

7.3 UPFC steady state operation

Figure 7-2 represents a very simple model of the UPFC connected in series with a transmission line. In this model the UPFC is replaced by a controllable voltage source V_{se} [20]. ρ is the angle of the V_{se}. It is freely variable between 0 and 2π at any transmission angle $0 \leq \delta \leq \pi$. Assuming that sending and receiving end of the transmission line have the same voltage amplitude, then:

$$V_s = Ve^{j\frac{\delta}{2}} \tag{7-1}$$

$$V_r = Ve^{-j\frac{\delta}{2}} \tag{7-2}$$

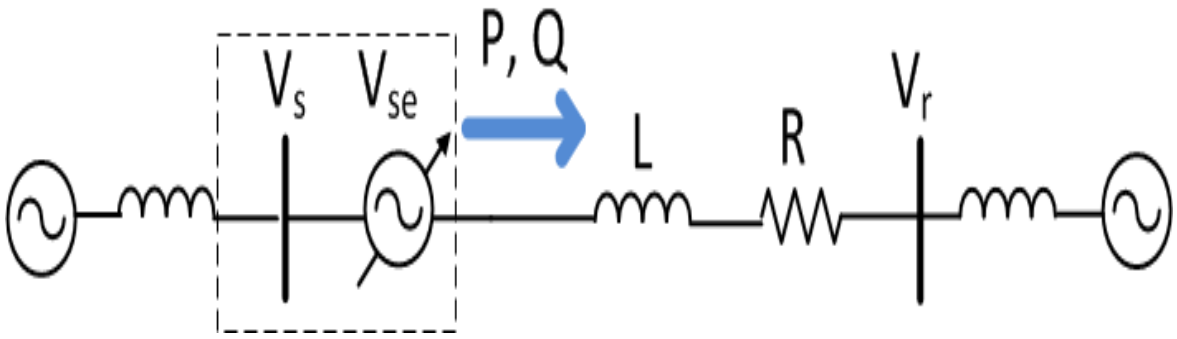

Figure 7-2. Simplified model of the UPFC connected to the sending end of the transmission line

$$V_{se} = V_{se} e^{j(\frac{\delta}{2}+\rho)} \tag{7-3}$$

The active and reactive power flow through the transmission line calculated as in:

$$P - jQ = V_r(\frac{V_s + V_{se} - V_r}{jX})^* \tag{7-4}$$

where:

$$P = \frac{V^2}{X}\sin(\delta) - \frac{VV_{se}}{X}\cos(\frac{\delta}{2} + \rho) \tag{7-5}$$

$$Q = \frac{V^2}{X}(1 - \cos(\delta)) - \frac{VV_{se}}{X}\sin(\frac{\delta}{2} + \rho) \tag{7-6}$$

The first term of (7-5), and (7-6) calculates the line active and reactive power flows when there is not any UPFC. The second term of these equations however, is related to the amount of the active and reactive power flows due to the UPFC installation. Inspection of these equations and considering the fact that ρ can be any arbitrary angle between 0 and 2π, indicates that the active and reactive power flows of the transmission line are controllable between $-\frac{VV_{se}}{X}$ and $\frac{VV_{se}}{X}$ independent of angle δ.

7.4 Series inverter dynamics

The dynamics of the UPFC series inverter has been discussed in [78]-[81].This part of the thesis briefly discusses the series inverter dynamics. Different control structures proposed by the researchers are presented here and the performance of each of them has been analyzed precisely.

The derivative of the line currents with respect to the time of the UPFC depicted in Figure 7-1 is calculated as:

$$\frac{d}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} \frac{-R}{L} & 0 & 0 \\ 0 & \frac{-R}{L} & 0 \\ 0 & 0 & \frac{-R}{L} \end{bmatrix}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \frac{1}{L}\begin{bmatrix} V_{sa} + V_{sea} - V_{ra} \\ V_{sb} + V_{seb} - V_{rb} \\ V_{sc} + V_{sec} - V_{rc} \end{bmatrix} \tag{7-7}$$

where V_s , and V_r, are the sending, and receiving end of the transmission line voltages and V_{se} is the series inverter voltage. Transformation from abc to the synchronous frame is defined as: [28]

$$f_{dq} = T(\omega t) f_{abc} \tag{7-8}$$

Where:

$$T(\omega t) = \frac{2}{3}\begin{bmatrix} \cos(\omega t) & \cos(\omega t - \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \\ -\sin(\omega t) & -\sin(\omega t - \frac{2\pi}{3}) & -\sin(\omega t + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \tag{7-9}$$

and ωt is the ac-bus phase locked loop output.

Transferring (7-7) to the synchronous frame (dq) based on (7-9), we will find:

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \frac{-R}{L} & \omega_0 \\ -\omega_0 & \frac{-R}{L} \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix} + \frac{1}{L}\begin{bmatrix} V_{sd} + V_{sed} - V_{rd} \\ V_{sq} + V_{seq} - V_{rq} \end{bmatrix} \tag{7-10}$$

Transferring (7-10) from time domain to the Laplace domain, then the d and q component of the transmission line current will be calculated as in [78]:

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = A \times \begin{bmatrix} V_{sd} + V_{sed} - V_{rd} \\ V_{sq} + V_{seq} - V_{rq} \end{bmatrix} \tag{7-11}$$

$$A = \begin{bmatrix} \frac{(R + Ls)/L^2}{s^2 + 2\frac{R}{L}s + {\omega_0}^2 + \left(\frac{R}{L}\right)^2} & \frac{\frac{\omega_0}{L}}{s^2 + 2\frac{R}{L}s + {\omega_0}^2 + \left(\frac{R}{L}\right)^2} \\ \frac{-\frac{\omega_0}{L}}{s^2 + 2\frac{R}{L}s + {\omega_0}^2 + \left(\frac{R}{L}\right)^2} & \frac{R + Ls}{s^2 + 2\frac{R}{L}s + {\omega_0}^2 + \left(\frac{R}{L}\right)^2} \end{bmatrix} \tag{7-12}$$

The diagonal elements of the matrix A (direct transfer functions) directly relate the i_d to the V_{sed} and i_q to the V_{seq} and the off-diagonal elements (cross transfer function) relate the i_d to the V_{seq} and i_q to the V_{sed} [78]-[81]. Figure 7-3 illustrates the bode plots of the direct and cross transfer functions. Inspection of these plots indicates that in the low frequency range (f $\leq$ 10 Hz), the i_d is more coupled to V_{seq} rather than V_{sed}. The i_q is also more coupled to the V_{sed} rather than V_{seq}in the same frequency range. This means that the steady state d-axis current $i_{d\infty}$ is predominantly controlled by the q-axis voltage V_{seq}, whereas the steady state q-axis current $i_{q\infty}$ is proportional to the d-axis voltage V_{sed} [80].

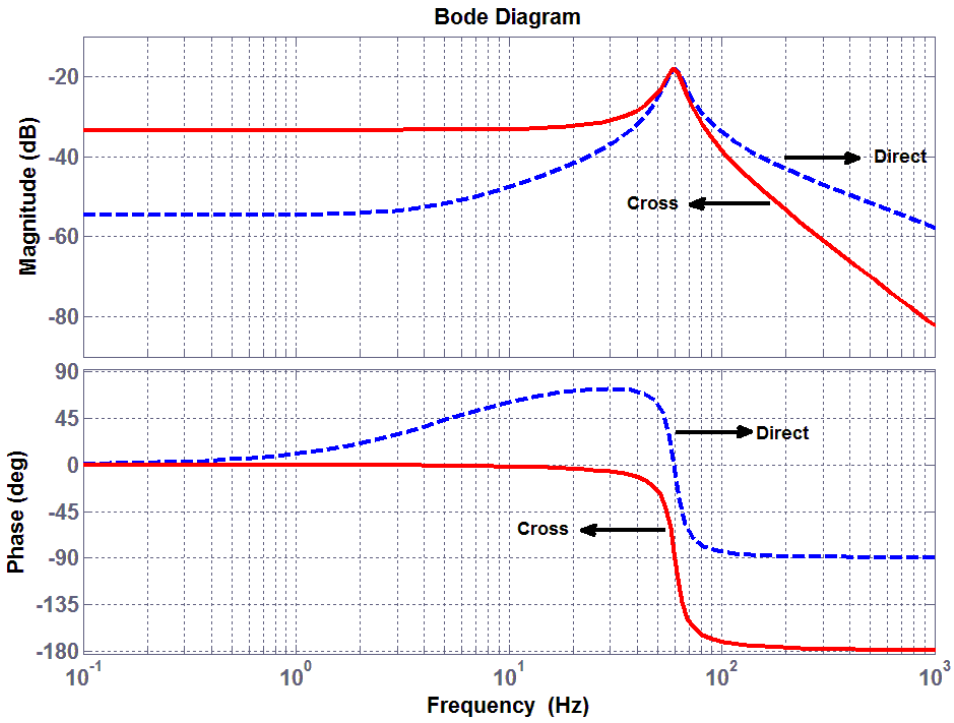

Figure 7-3. Bode plots of the direct and cross transfer functions. R=4Ω, L=0.123 H (X/R=11.6). The R, and L values are based on the 345 kV simulation AC-system explained in the section 7.7

7.5 Different series inverter control structures

7.5.1 Cross-coupling control method

Figure 7-4 indicates the control structure of the Cross-Coupling method. The d and q component of the line current are regulated using PI controllers. As can be observed, the output of the d-axis current regulator calculates the q component of the series inverter voltage and the q-axis current regulator calculates the d component of the series inverter voltage. As discussed earlier, this is due to the fact that i_d is more coupled to V_{seq} rather than V_{sed} and i_q is also more coupled to the V_{sed} rather than V_{seq} for very low frequency ranges.

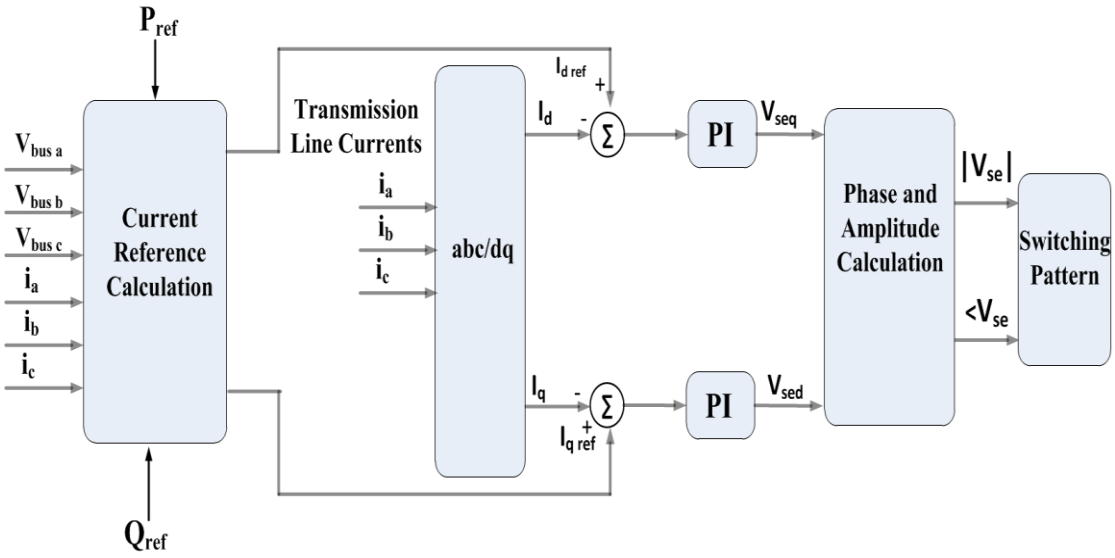

Figure 7-4. Cross-coupling controller

The reference value for the i_d and i_q are set based on the desired amount of the active and reactive power flow. Based on this figure the reference voltage vector of the series inverter is calculated as in [78]:

$$\begin{bmatrix} V_{sed}^* \\ V_{seq}^* \end{bmatrix} = \begin{bmatrix} 0 & -Kq - \dfrac{K_{qI}}{s} \\ K_p + \dfrac{K_{pI}}{s} & 0 \end{bmatrix} \begin{bmatrix} i_d^* - i_d \\ i_q^* - i_q \end{bmatrix} \tag{7-13}$$

Where K_p and K_q are the proportional gain of the active and reactive power controller. The integral gain of K_{pi}, and K_{qi} are added to remove the steady state error.

7.5.2 Advanced control method

The advanced control method is obtained by adding K_r to the diagonal elements of the Cross coupling control matrix. The K_r is the control gain which is used to damp the power

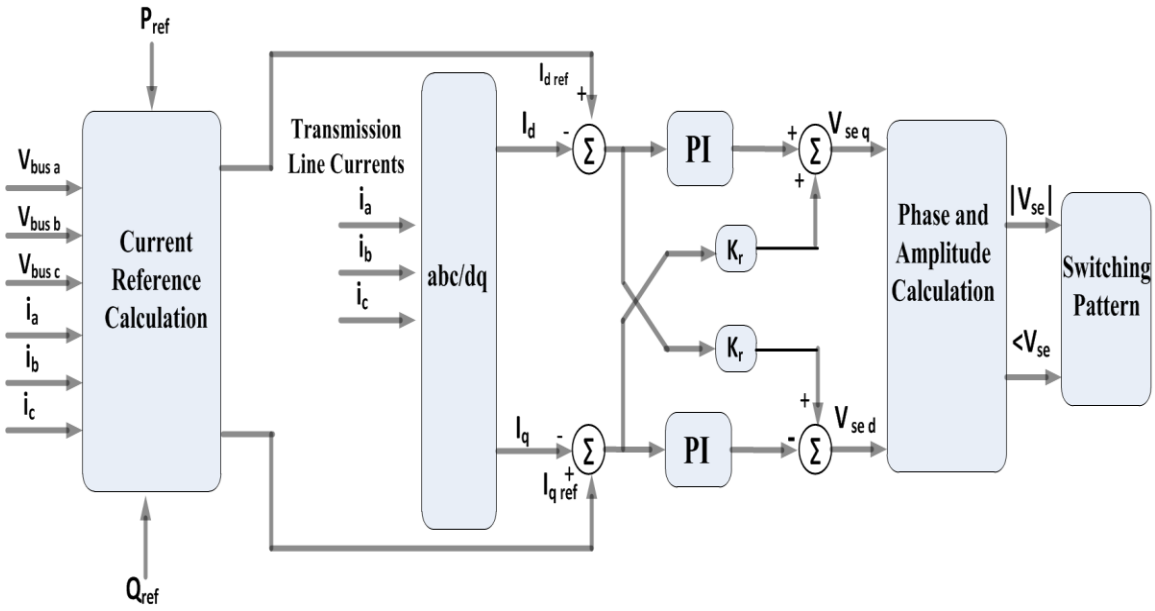

Figure 7-5. UPFC advanced controller

fluctuation. It is important to note that this power fluctuation is different from the "power swing" oscillations understood by the power system engineers. Power swings are low frequency oscillation (less than 1 Hz) related to the moments of inertia of the turbine alternator. Basically the K_r is used to damp the oscillations associated with UPFC operation in the range of 100 Hz and higher [79].

Figure 7-5 indicates the control structure of the advanced control method. Based on this figure, the d and q components of the series inverter voltage are calculated as in:

$$\begin{bmatrix} V_{sed}^* \\ V_{seq}^* \end{bmatrix} = \begin{bmatrix} K_r & -Kq - \dfrac{K_{qI}}{s} \\ K_p + \dfrac{K_{pI}}{s} & K_r \end{bmatrix} \begin{bmatrix} i_d^* - i_d \\ i_q^* - i_q \end{bmatrix} \quad (7\text{-}14)$$

It was mentioned earlier that for high frequency range the amplitude of the direct transfer function is greater than the cross transfer function. It means that dynamics of the i_d is more

controllable with V_{sed} and also the i_q transient is more controllable with V_{seq}. That is the reason that K_r sits in the diagonal elements of the matrix in (7-14). K_r is identical for both d and q axis controller because the transfer function of $\frac{i_d}{V_{sed}}$ is exactly the same as the one for $\frac{i_q}{V_{seq}}$. Proper calculation of the K_r leads to the effective damping of the oscillations related to the UPFC operation. Following calculations obtains an equation that can be used to determine the proper value for K_r.

Ignoring the shunt inverter current, then the transmission line currents are related to the UPFC series inverter voltages and also transmission line voltages as in:

$$\begin{bmatrix} V_{sa} + V_{sea} - V_{ra} \\ V_{sb} + V_{seb} - V_{rb} \\ V_{sc} + V_{sec} - V_{rc} \end{bmatrix} = (R + L\frac{d}{dt}) \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{7-15}$$

Assuming that $V_s = V_r$ then

$$\begin{bmatrix} V_{sea} \\ V_{seb} \\ V_{sec} \end{bmatrix} = (R + L\frac{d}{dt}) \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{7-16}$$

Transforming (7-16) from abc domain to the synchronous reference frame:

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \frac{-R}{L} & \omega \\ -\omega & \frac{-R}{L} \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \frac{1}{L}\begin{bmatrix} V_{sed} \\ V_{seq} \end{bmatrix} \tag{7-17}$$

And then the UPFC series inverter voltages are calculated as in:

$$\begin{bmatrix} V_{sed} \\ V_{seq} \end{bmatrix} = \begin{bmatrix} R + L\frac{d}{dt} & -\omega_0 L \\ \omega_0 L & R + L\frac{d}{dt} \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} \tag{7-18}$$

From the control point of view a converter can be considered as an ideal power transformer with a time delay. The output voltage of the converter is assumed to follow a voltage reference signal with an average time delay due to the converter switching. Hence, the general expression of the transfer function between the reference series inverter voltage and generated voltage will be as in [62]:

$$\frac{V_{sed}(s)/V_{seq}(s)}{V^*_{sed}(s)/V^*_{seq}(s)} = \left(\frac{1}{1+sT_t}\right) \tag{7-19}$$

Where, T_t is the average time delay of the series inverter and is decided by the converter topology and its switching technique. Let's assume that the series inverter can generate the reference voltage s very quickly and T_t is negligible. Then we will have:

$$\begin{bmatrix} V^*_{sed} \\ V^*_{seq} \end{bmatrix} = \begin{bmatrix} V_{sed} \\ V_{seq} \end{bmatrix} \tag{7-20}$$

Substituting V_{sed} and V_{seq} from (7-14) into (7-18) we will find:

$$\begin{bmatrix} K_r & -k_q \\ K_p & K_r \end{bmatrix} \begin{bmatrix} i^*_d - i_d \\ i^*_q - i_q \end{bmatrix} = \begin{bmatrix} R + L\frac{d}{dt} & -\omega_0 L \\ \omega_0 L & R + L\frac{d}{dt} \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} \tag{7-21}$$

(7-21) can be rewritten as in:

$$\begin{bmatrix} R + K_r + L\frac{d}{dt} & -(k_q + \omega_0 L) \\ (Kp + \omega_0 L) & R + K_r + L\frac{d}{dt} \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} K_r i^*_d - k_q i^*_q \\ K_p i^*_d + K_r i^*_q \end{bmatrix} \tag{7-22}$$

Taking the Laplace transformation of (7-22) leads to:

$$\begin{bmatrix} R + K_r + Ls & -(k_q + \omega_0 L) \\ (Kp + \omega_0 L) & R + K_r + Ls \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} K_r i^*_d - k_q i^*_q \\ K_p i^*_d + K_r i^*_q \end{bmatrix} \tag{7-23}$$

Based on (7-23), the transfer functions of $\frac{i_d}{i_d^*}$ and $\frac{i_q}{i_q^*}$ are calculated as in:

$$\frac{i_d}{i_d^*} = \frac{\frac{K_r}{L}s + k_p\left(\frac{L\omega_0 + k_q}{L^2}\right) + K_r(\frac{R+K_r}{L^2})}{s^2 + \frac{2(K_r+R)}{L}s + \frac{(\omega_0 L + k_p)(\omega_0 L + k_q) + (K_r+R)^2}{L^2}} \tag{7-24}$$

$$\frac{i_q}{i_q^*} = \frac{\frac{K_r}{L}s + k_q\left(\frac{L\omega_0 + k_p}{L^2}\right) + K_r(\frac{R+K_r}{L^2})}{s^2 + \frac{2(K_r+R)}{L}s + \frac{(\omega_0 L + k_p)(\omega_0 L + k_q) + (K_r+R)^2}{L^2}} \tag{7-25}$$

As can be observed (7-24), and (7-25) are second order transfer functions with following characteristics:

$$\omega_n = \frac{\sqrt{(\omega_0 L + k_p)(\omega_0 L + k_q) + (K_r+R)^2}}{L} \tag{7-26}$$

$$\zeta = \frac{K_r + R}{\sqrt{(\omega_0 L + k_p)(\omega_0 L + k_q) + (K_r+R)^2}} \tag{7-27}$$

And therefore the settle down time is calculated as in:

$$\tau = \frac{1}{\zeta\omega_n} = \frac{L}{(K_r+R)} \tag{7-28}$$

Inspection of (7-28) reveals the fact that the response time of the UPFC can be controlled to some extent by adjusting the K_r. The greater the K_r the faster the system response time would be. However there should be a compromise between the fast response and also non-oscillatory response without a severe over shoot. Usually in the second order systems by setting the damping ration (ζ) to 0.8, the step response of the system is pretty fast and without any oscillation. The system does not over shoot either. Considering the damping

ratio of 0.8 for the UPFC closed loop transfer function, then the K_r will be calculated as in [79]:

$$K_r = \frac{\zeta \sqrt{\left(\omega_0 L + k_p\right)\left(\omega_0 L + k_q\right)}}{\sqrt{1-\zeta^2}} - \mathrm{R} \tag{7-29}$$

7.6 Shunt inverter (STATCOM) controller

As discussed earlier, the shunt inverter provides the required active power that series inverter exchanges with the transmission line from the line itself. It can do this power transfer in both directions i.e. to the grid or from the grid based on the series inverter demand. The remaining capacity of the shunt inverter is used for the reactive power support functionality exactly like the Static Synchronous Compensator STATCOM. All the UPFCs, regardless of their converter topology, can be divided into two different types depending on the shunt inverter control strategy. One type is the UPFC with vector controlled or PWM-based shunt inverter. In this type, the DC-link voltage that is regulated to a constant reference value is chopped with the PWM pulses to any arbitrary voltage vector [29], and [95]. However, this type of the inverter maybe uneconomical for many transmission level FACTS devices due to the high switching losses of the PWM VSCs. In the other type of the UPFC, the shunt inverter operation is based on controlling only the angle of its output voltage i.e. angle-controlled STATCOM. In the previous chapters the angle-controlled STATCOM has been presented and analyzed in details. To make this chapter of thesis self-sufficient, only a brief outline of the angle-controller has been given. It has been shown in [19] that by a slight change of the inverter output voltage angle (α), for a controlled time, the inverter is able to

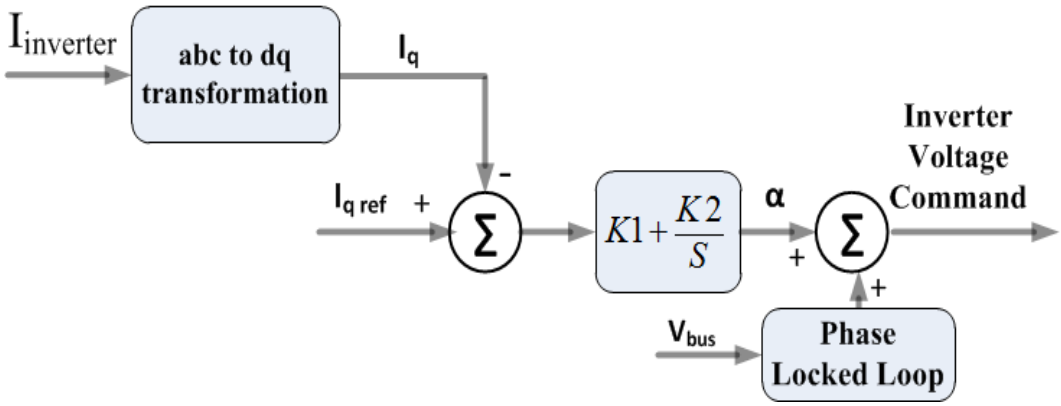

Figure 7-6. Angle-controlled STATCOM control structure

provide inductive/capacitive reactive power. Basically by controlling the α toward the positive/negative direction, for a controlled time, the DC-link voltage is driven lower/higher and therefore the VSC output voltage decreases/increases accordingly. In this type of the inverter, the ratio between AC and DC voltages is kept constant and the VSC output voltage magnitude is varied indirectly by changing the DC-bus voltage. Since angle α is the only control input in this control strategy, it is called angle-controller. Control architecture of the angle-controller STATCOM is illustrated in Figure 7-6. Angle-control STATCOM is switched at line frequency to achieve the lower system losses. High-quality output voltage of the angle-controlled STACOM is provided by multi-pulse inverters. 24-pulse and 48-pulse inverters are commonly used for this kind of the STATCOMs [29]. A group of Neutral Point Clamped (NPC) inverters are electromagnetically coupled using transformers to synthetize the output voltage. Low converter losses along with high voltage quality output make the angle-controlled STATCOM an attractive solution for the transmission level applications. Figure 7-7 indicates a 345 kV, 100 MVA 48- pulse STATCOM performance in inductive

($i_{q\,sh}$=1 pu) and capacitive ($i_{q\,sh}$= -1 pu) mode of operation. This is the same STATCOM was presented in chapter 2 of the thesis and also is exactly the same STATCOM that has been used to construct the UPFC model used in the Simulation verification part of this chapter. As can be seen in this picture, the DC-link voltage is not fixed and is varied over a range of the values. The maximum DC-link voltage is obtained when the STATCOM works in the capacitive mode of operation with its maximum capacity. The minimum DC-link voltage, however, is obtained at the operating point at which the STATCOM works in the inductive mode with its maximum capacity.

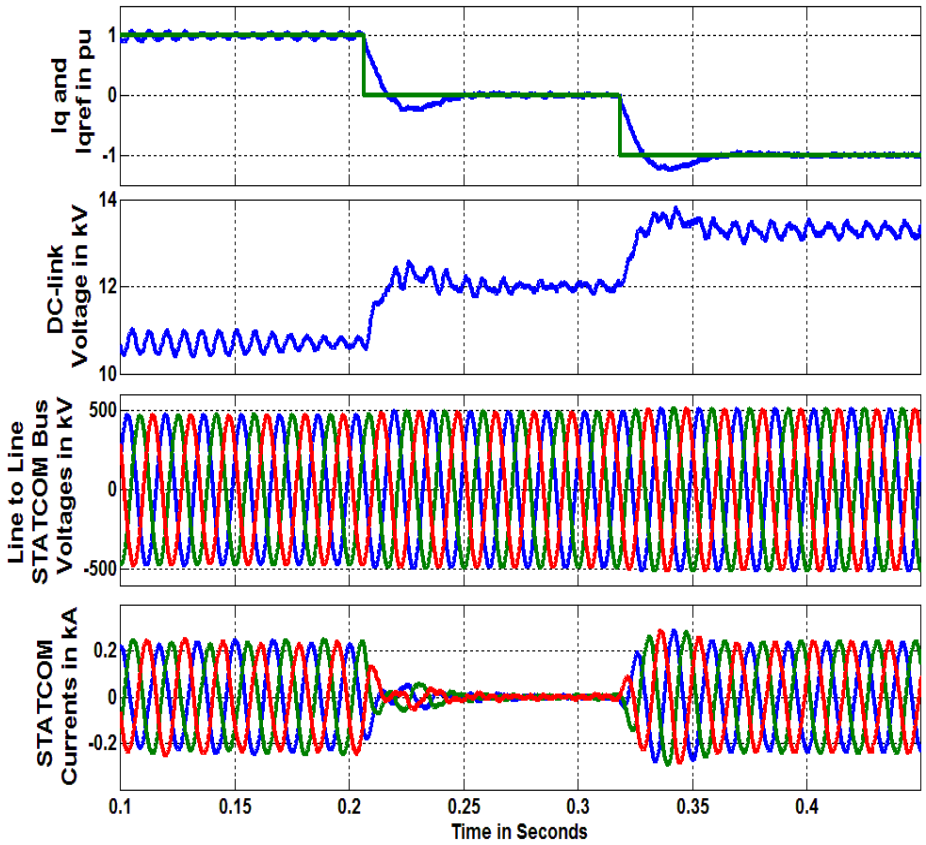

Figure 7-7. 48-pulse angle-controlled STATCOM performance with different current references. Per unit values are based on 345kV, and 100 MVA system

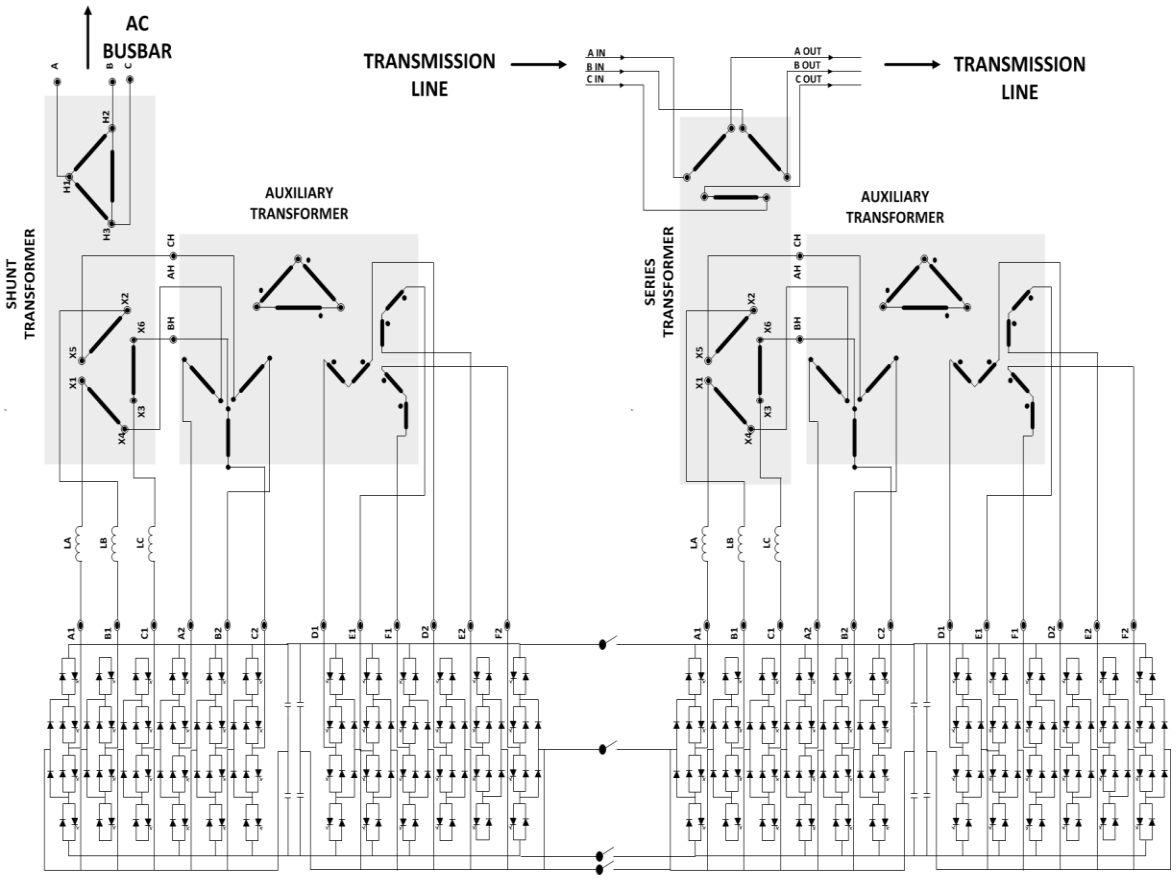

Figure 7-8. Power circuit of the UPFC used in the simulation verification. This UPFC model is developed based on the NYPA UPFC at Marcy substation[30]

7.7 Simulation system configuration

The PSCAD UPFC model used for the simulation verification has been developed based on the NYPA UPFC at Marcy substation in the state of the New York. The series and shunt Voltage Source Converters (VSCs) consist of 4 three level NPC three phase inverters (A1, B1, C1), (A2, B2, C2), (D1, E1, F1), and (D2, E2, F2). Their square wave outputs are combined electromagnetically to generate a 48-pulse output voltage waveform and their DC sides are connected to a common DC-bus. The output voltages of the three level NPC poles are combined through auxiliary and shunt/series transformers as shown in Figure 7-8.

The primary winding of the auxiliary transformer is doubly fed open wye winding with 11.9 kV rated voltage across the winding. The secondary winding is doubly fed open zigzag winding with the same voltage rating as the primary winding i.e. 11.9 kV. The voltage across the secondary leads the primary by 30 degree. The shunt transformer aids in voltage waveform construction and serves to couple the synthesized voltage to the 345 kV transmission system. The shunt transformer has standard delta connected primary windings rated 345 kV, and open delta secondary windings rated 21.4 kV across the winding [30] **.**Its rating is 100 MVA. Similar to the shunt transformer, the series transformer aids in voltage construction and also serves to couple the synthesized voltage with the transmission line. It has doubly fed open delta primary winding for injecting a nominally rated voltage of 11 kV into the line. The secondary side of the series transformer is the same as the shunt transformer. The shunt inverter works with angle-controller.

The simulated UPFC model has the capability to work on two different modes. One mode is Power flow controller and the other one is voltage injection. In power flow controller mode the reference values for the V_{sed}^{*} and V_{seq}^{*} are decided by the series inverter controller (either cross-coupling or advanced control method) as discussed earlier. However, in the voltage injection mode the system operator has the capability to manually set the desired value for the d and q component of the series inverter voltage. Having calculated the V_{sed}^{*} and V_{seq}^{*} , the angle and amplitude of the series inverter voltage is simply calculated. The amplitude of the series inverter voltage is controlled by changing the period of zero voltage of the NPC inverters used to construct the series 48-pulse inverter. The amplitude of the series inverter voltage is directly proportional to the cosine of this angle (σ_{se}). The σ_{se} is

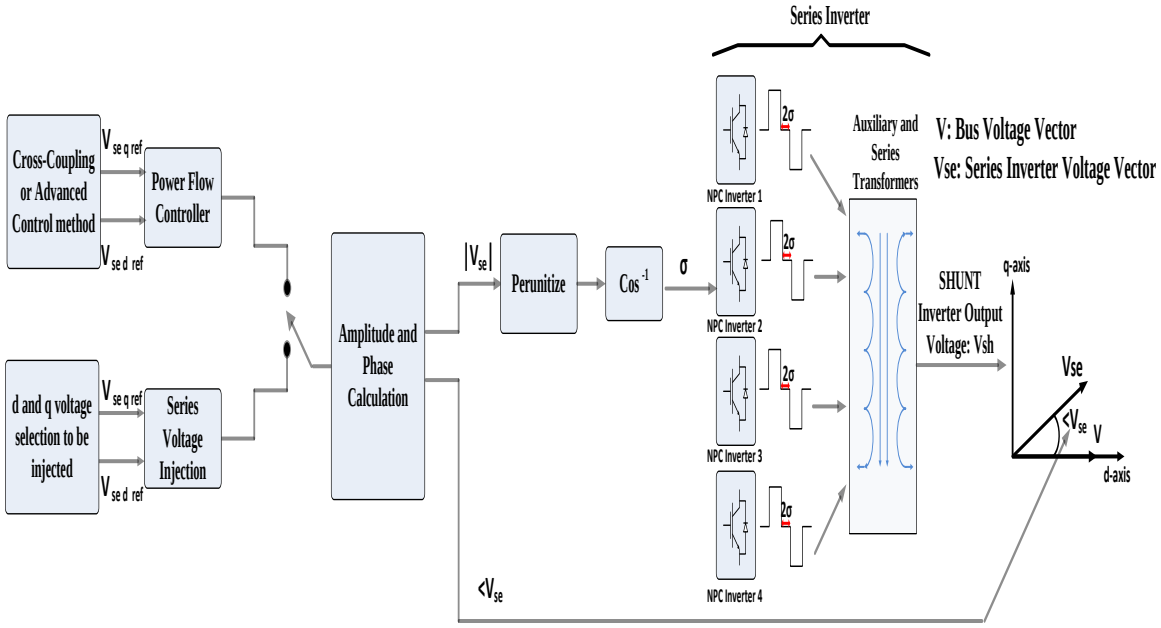

Figure 7-9. Series 48-pulse inverter control

calculated by per unitizing the amplitude of the desired series inverter voltage (calculated by the controller) and taking the inverse cosine of it. The variation of the DC-link voltage (due to shunt inverter operation) is not taken into account. The magnitude is per unit of output voltage at any time. The switching pattern of the series inverter has been conceptually illustrated in Figure 7-9.

7.8 Simulation results of the UPFC connected to the 2-Machine AC-System

In this part, the UPFC model developed based on the UPFC at Marcy substation (Figure 7-8) has been connected to the simple 2-Machine AC-system as shown in Figure 7-10. The value of the transmissions line Inductance and resistance are based on the real 345 kV transmission line. All the per unit values are based on a 345 kV and 100 MVA system. The UPFC performance with both discussed control strategies i.e. cross-coupling and advanced-

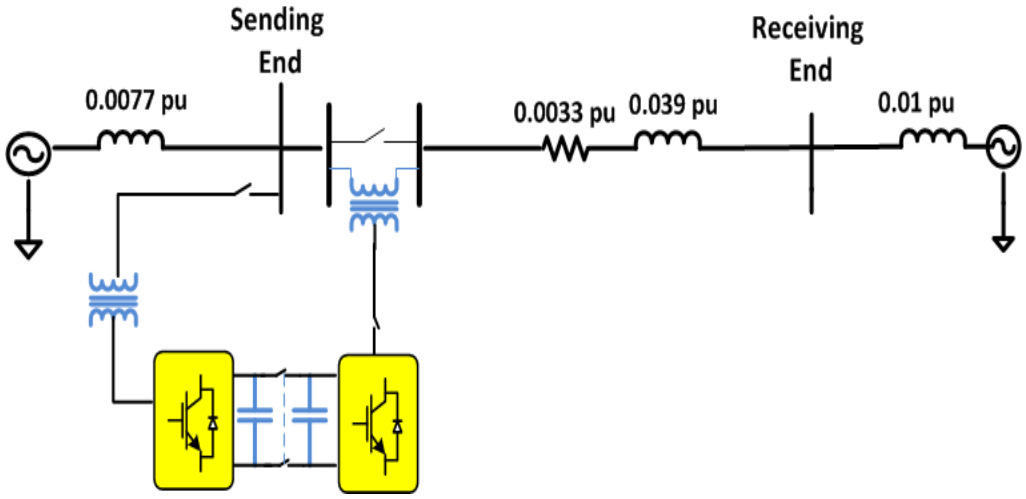

Figure 7-10. PSCAD UPFC model developed based on the NYPA UPFC at Marcy substation connected to the 2-Machine AC-system

-control methods have been presented in this section.

The waveforms of Figure 7-11 indicate the UPFC performance when it works in the voltage injection mode. Initially the reference value for the d and q component of the series injection voltages (V_{sed}^{*}, V_{seq}^{*}) are set to zero. The sending and receiving end generator voltages are identical in both amplitude and phase and consequently there is not any active and reactive power flow through the transmission line. At around t=0.3 seconds a step change in V_{sed}^{*} is applied. This voltage injection coincident with d-axis leads to a considerable change in the reactive power flow through the transmission line. It reaches from zero to more than 100 MVAr. The active power flow remains almost unchanged. Results in Figure 7-11perfectly proves the fact that that reactive power flow (i_q) is more coupled with V_{sed} in the low frequency ranges as discussed earlier in this chapter. Figure 7-12 indicates the same results as in Figure 7-11 for the time that step change is applied in the q direction. As can be

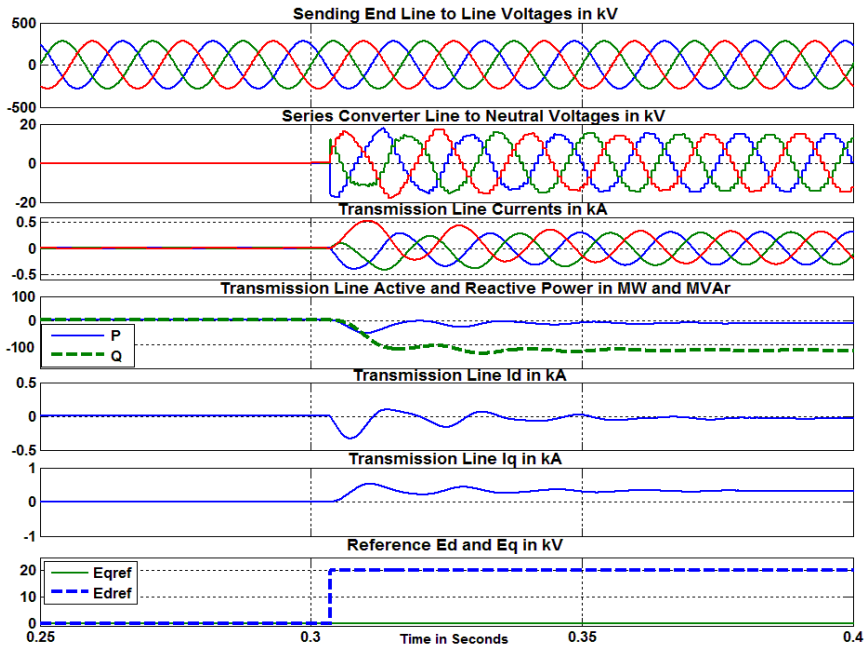

Figure 7-11. The UPFC performance with a step change in the d component of the series inverter voltage reference value. (The UPFC works in the voltage injection mode)

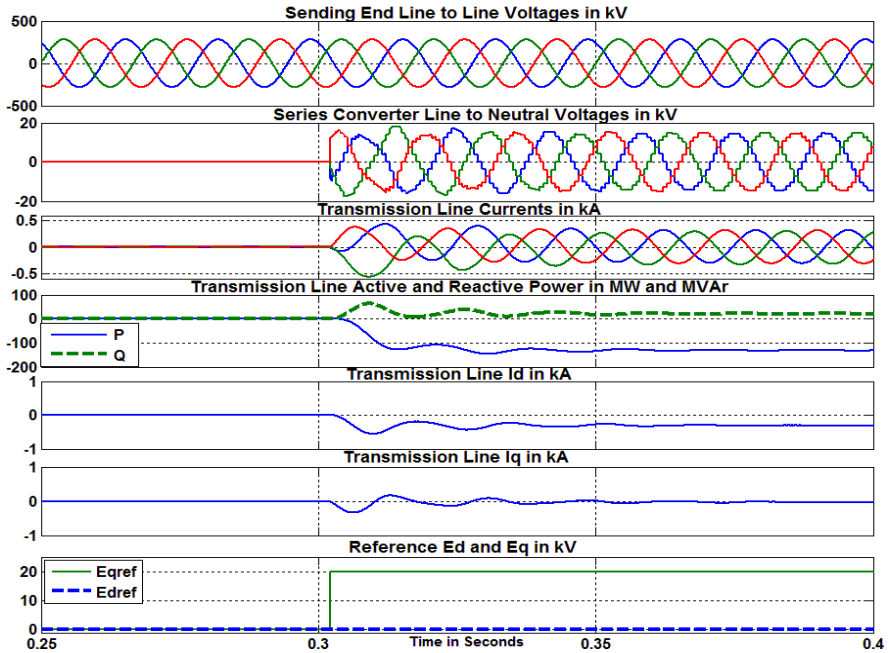

Figure 7-12. The UPFC performance with a step change in the q component of the series inverter voltage reference value. (The UPFC works in the voltage injection mode)

observed here, after applying the step change in the V_{seq} the active power reaches from zero to more than 100 MW while the change in the reactive power is negligible. This is a proof for the fact that V_{seq} is coupled with active power (i_d) in the low frequency range.

In all the remaining simulation results of this chapter the UPFC works in the power flow controller mode. Therefore, for simplicity, herein after we don't mention the UPFC control mode knowing that it always works in power flow controller mode.

Results in Figure 7-13 present the UPFC performance with a step change in the active power reference value when it is controlled with cross-coupling method. These results are compared with waveforms of Figure 7-14 which shows the same waveforms and under same condition for the time that UPFC is controlled with advanced control method. As can be observed in Figure 7-13, initially the reference value for the $i_{d\,ref}$ and $i_{q\,ref}$ (active and reactive power) are set to zero. At t=0.3 seconds there is a step change in the $i_{d\,ref}$ from zero all the way to 0.3 kA. The d component of the transmission line current follows its reference value and reaches to around 0.3 kA after considerable fluctuations. The current overshoot is also considerable. Another remarkable point evident in this figure is that the step change in the $i_{d\,ref}$ induces considerable fluctuations into the i_q and consequently into the reactive power flow through the transmission line. In contrast with cross-coupling controller, when UPFC works with advanced controller method the d component of the transmission line follows its reference value without any fluctuation. As can be observed in Figure 7-14, there is not any overshoot either. The cross-coupling between the d and q component of the transmission line has also decreased dramatically.

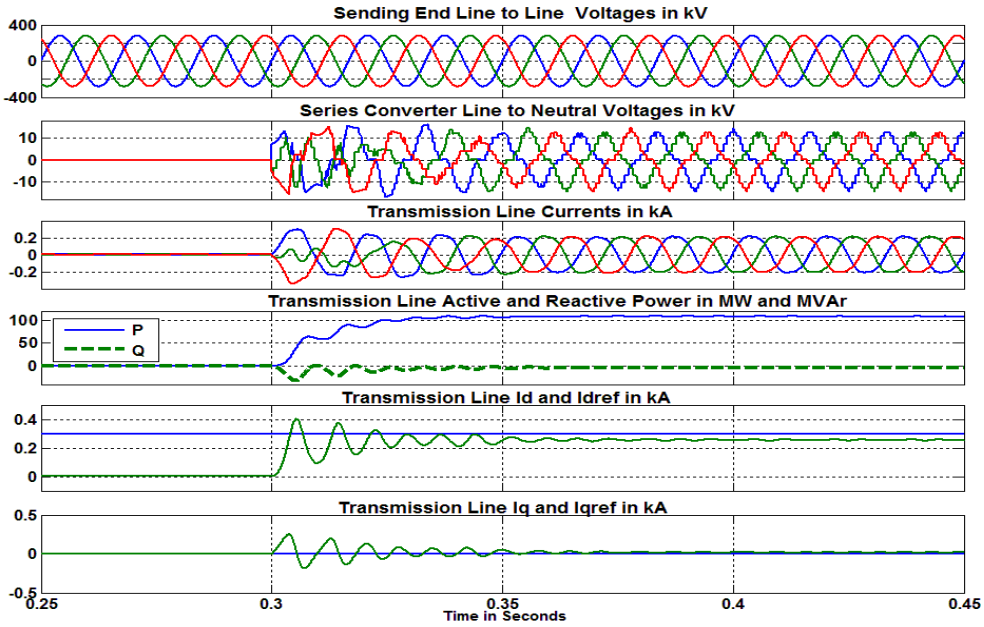

Figure 7-13. UPFC performance with a step change in the $i_{d\ ref}$ (active power reference). UPFC works in power flow controller mode with series inverter in cross-coupling method

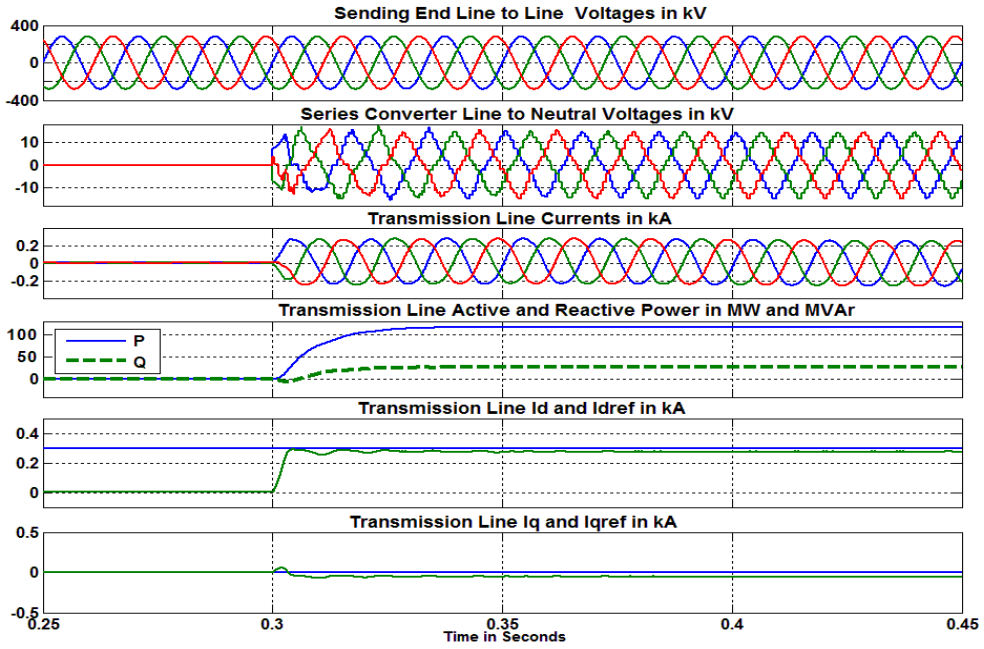

Figure 7-14. UPFC performance with a step change in the $i_{d\ ref}$ (active power reference). UPFC works in power flow controller mode and series inverter is controlled with advanced control method

The waveforms of Figure 7-15 and Figure 7-16 present the same results as in Figure 7-13 and Figure 7-14 but this time the step change in the $i_{d\,ref}$ is applied in the opposite direction. Again it is clearly seen that when the UPFC works with advanced controller method the fluctuations in the currents and power is completely eliminated and also the cross coupling between the i_d and i_q decreases dramatically in comparison with the time that UPFC works with cross-coupling method.

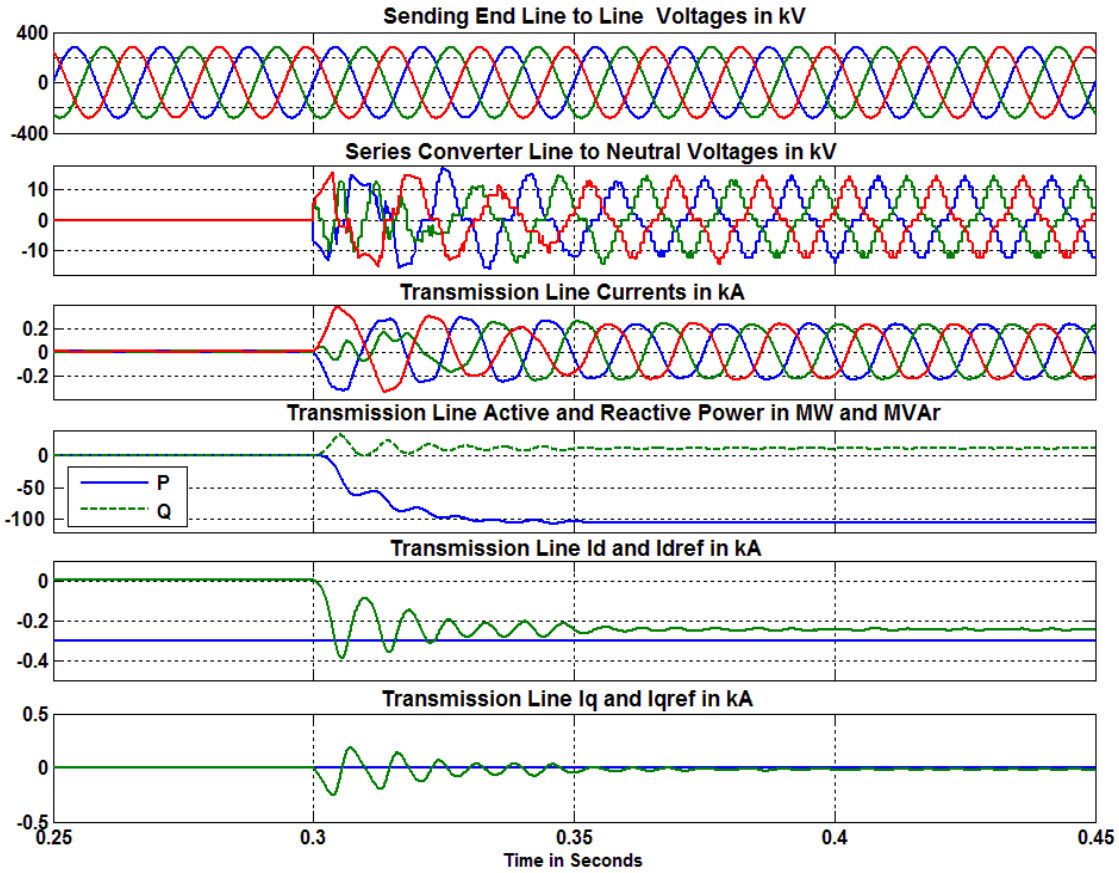

Figure 7-15. UPFC performance with a step change in the $i_{d\,ref}$ (active power reference). UPFC series inverter is controlled with cross-coupling method.

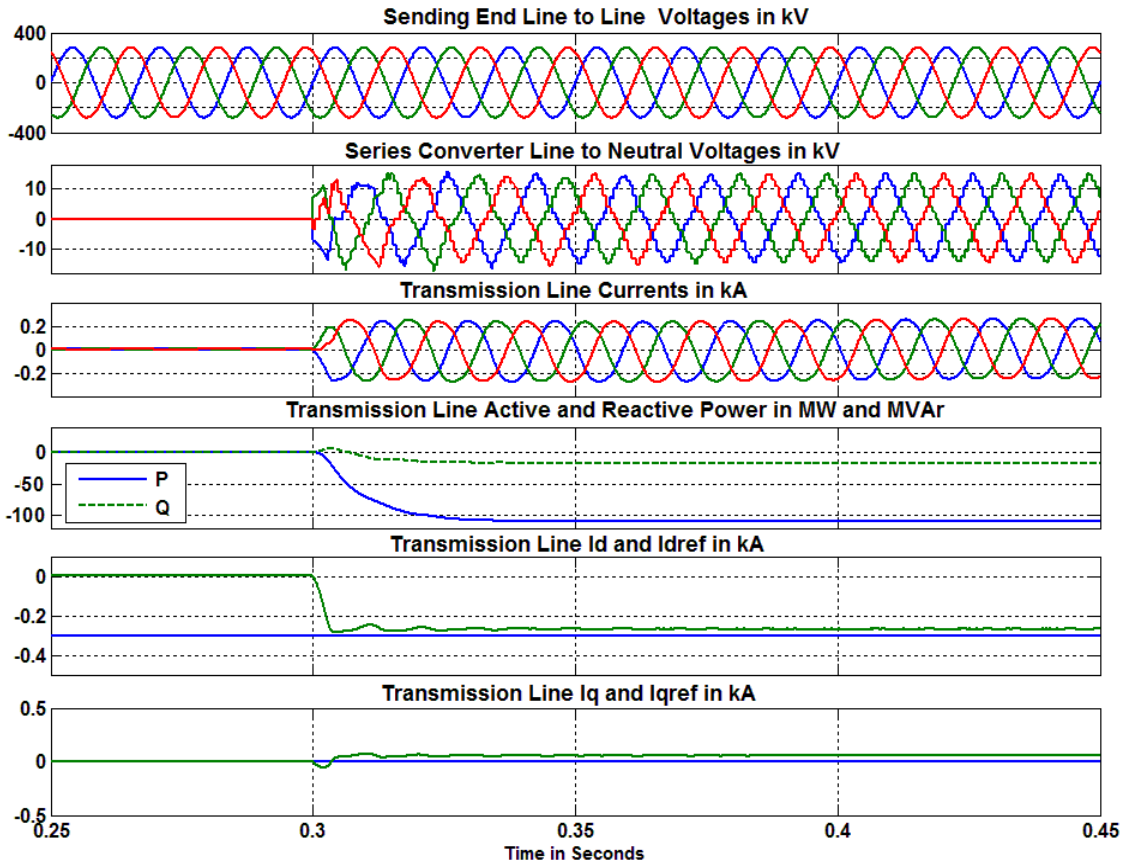

Figure 7-16. UPFC performance with a step change in the $i_{d\ ref}$ (active power reference). UPFC series inverter is controlled with advanced control method.

Results in Figure 7-17, and Figure 7-18 present the simulation results of the UPFC works with advanced control method and a step change in the $i_{q\ ref}$ in two different directions but identical values. As can be seen in these two figures the q component of the transmission line current follows its reference value quickly and smoothly without any oscillation.

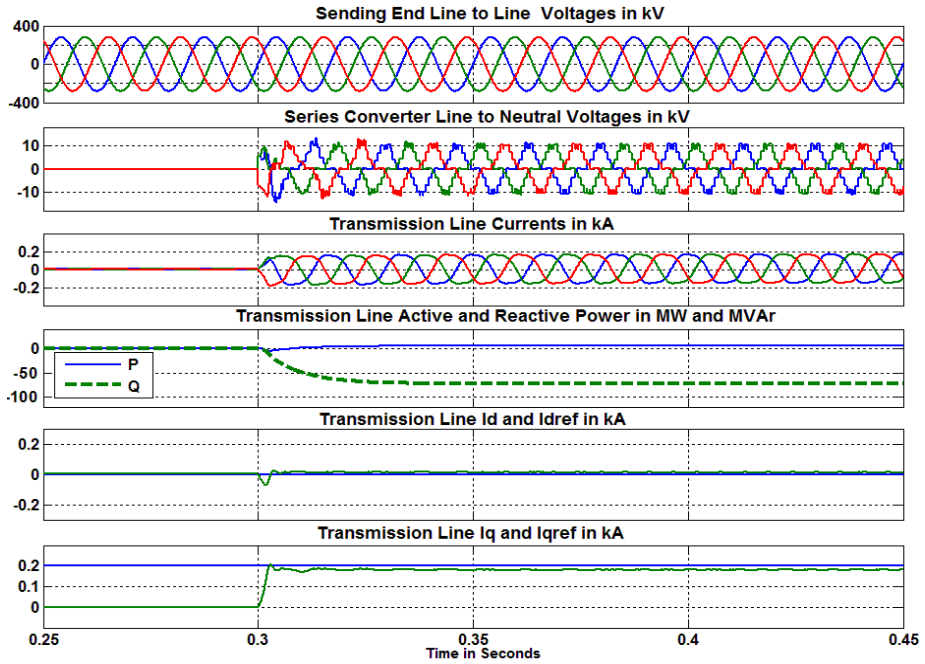

Figure 7-17. UPFC performance with a step change in the $i_{q\,ref}$ (reactive power reference). UPFC series inverter is controlled with advanced control method

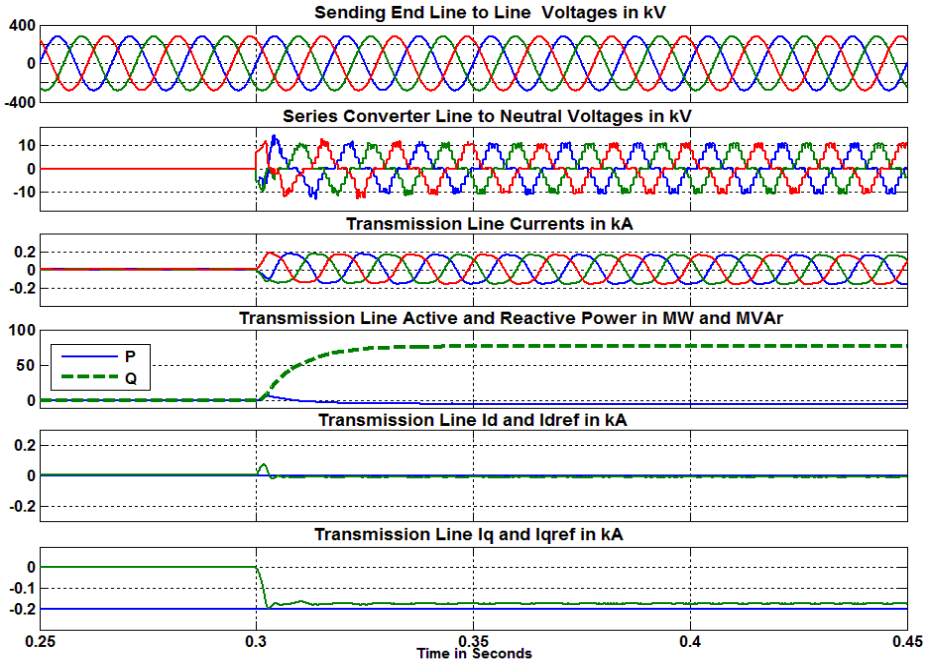

Figure 7-18. UPFC performance with a step change in the $i_{q\,ref}$ (reactive power reference) when the series inverter is controlled with advanced control method.

7.9 UPFC operational limit

It was mentioned in the previous section that UPFCs with DC-link voltage regulated over a range of the values (angle- controlled shunt inverter) have gained more interest in the transmission level applications due to the lower converter losses. For simplicity, this type of the UPFC is hereinafter referred to as UPFC.

As discussed, the UPFC active and reactive power flows are independently controllable in the range of $\frac{VV_{se}}{X}$ and $\frac{-VV_{ser}}{X}$ independent of the phase difference between the sending and receiving end bus voltages [20]. V is the amplitude of the sending and receiving end voltages and V_{se} is the amplitude of the injected series inverter voltage. X represents the inductance of the transmission line. Therefore, the maximum UPFC active and reactive power controllability range is directly proportional to the maximum series inverter voltage value. Regardless of the converter topology and control strategy, the series inverter voltage value is directly proportional to the DC-link voltage level.

$$V_{se} = K_{ser} V_{dc} \tag{7-30}$$

K_{ser} relates the DC-link voltage to the series inverter output voltage and depends on the converter topology and rating. Inspection of this equation indicates that when the UPFC DC-link voltage is not fixed and is regulated over a range of the values, the maximum series voltage injection and consequently UPFC active and reactive power controllability range varies with shunt inverter operating conditions. The minimum controllability range obtains when the shunt inverter works in the inductive mode of operation with its maximum capacity. At this operating condition, the DC-link voltage reaches to its minimum value. In contrast with inductive operation mode, when the shunt inverter works in the capacitive

mode with its maximum capacity, the DC-link voltage reaches to its maximum level. The UPFC controllability range reaches to its maximum accordingly.

7.10 Proposed Solution

This section presents a solution to increase the UPFC controllability range when the shunt inverter works in the inductive operation mode (Minimum DC-link voltage level). Assume that the shunt inverter is set to absorb a specific amount of the inductive current ($i_{q\,sh}$) from the grid. It is well known that the amount of the reactive power (inductive or capacitive) is directly proportional to the difference between the amplitude of the bus voltage and shunt inverter output voltage as calculated in (7-31). The shunt inverter output voltage is proportional to the DC-link voltage (7-32).

$$i_{q\,sh} \approx (|V| - |V_{sh}|) \tag{7-31}$$

$$|V_{sh}| = K_{sh} Cos(\sigma)\, V_{dc} \tag{7-32}$$

K_{sh} is the constant factor for the shunt pulse-inverter which relates the DC-side voltage to the amplitude of the AC-side output voltage. The $0^{\circ} \leq \sigma \leq 90^{\circ}$ is the period of zero voltage of the NPC inverters used to construct the shunt pulse- inverter. If the σ increases ($Cos(\sigma)$ decreases) the $|V_{sh}|$ will decrease according to (7-32). Therefore, the STATCOM angle controller must increase the DC-link voltage to increase the V_{sh} amplitude to its previous value (before changing the σ) such that $i_{q\,sh}$ and consequently STATCOM operating point remains unchanged. This is the main idea of the proposed solution i.e. to increase the DC-link voltage without changing the STATCOM operating condition. Increased DC-link voltage will increase the maximum UPFC series inverter voltage injection (equation (7-30)) and consequently increase the UPFC active and reactive power flow controllability range. In

the normal operation, the σ is set to an angle which results in the minimum THD of the output voltage. By increasing the σ from its optimal value, the output voltage THD increases. However, by limiting the σ in the specific range, the output voltage THD remains acceptable. Especially for the 48-pulse inverters, it is possible to change the σ in the considerable range with acceptable voltage THD. Figure 7-19 illustrates how the fundamental voltage amplitude and the output voltage THD of the simulation system 48-pulse inverter varies when σ increases from zero to 90˚. To obtain the results of Figure 7-19, the DC-link voltage capacitor of the shunt inverter is replaced by the DC-link voltage sources to fix the DC-link voltage at the 12 kV. The AC-side (shunt transformer primary winding) is left open circuit. As can be observed in this figure, the change in the fundamental voltage amplitude is proportional to the cosine of the σ, as calculated in (7-32). The greater the σ, the lower fundamental voltage amplitude is being generated. It can also be observed that the minimum THD of 3% is obtained at σ_{opt} =3.75˚. By increasing the σ form its optimal value, the voltage THD increases. However, for a considerable range of the σ, the voltage THD does not change substantially. The STATCOM tie line impedance (including the shunt inverter leakage inductance) is also seen as large impedance for the high order harmonics such as 23rd , 25th , 47th , and 49th and therefore, these harmonics can barely reach to the grid. It will be shown in the simulation results that even for the large value of the δ the current THD does not increase dramatically.

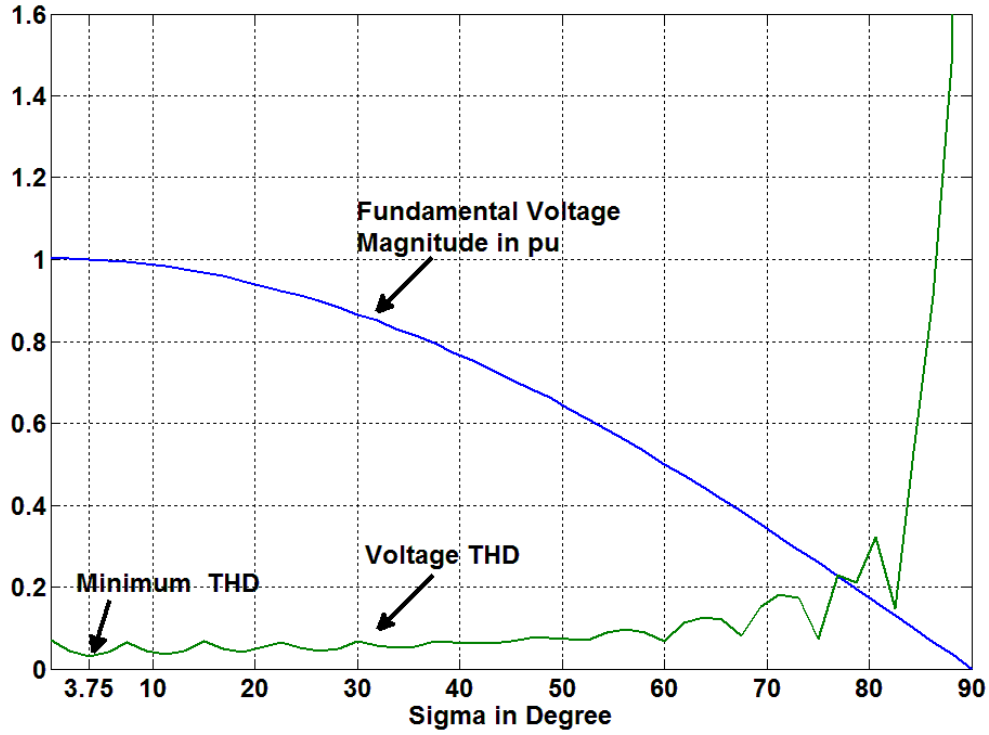

Figure 7-19. Fundamental voltage amplitude and the output voltage THD of the simulation system 48-pulse inverter when σ increases from zero to 90˚. Per unit values are based on 345kV, and 100 MVA

Based on this concept, the following solution is presented to increase the UPFC controllability range. Assume that the shunt inverter works in the inductive mode of operation and the transmission line active and/or reactive power flows are not able to follow their reference values due to the low DC-link voltage. In this solution, the σ is increased from its optimal value (σ_{opt}) to a calculated value (σ_{cal}). σ_{cal} is calculated as :

$$V_{sh1} = K_{sh}Cos(\sigma_{opt})V_{dc} = V_{sh2} = K_{sh}Cos(\sigma_{cal})V_{dc\,ref} \tag{7-33}$$

$$\sigma_{cal} = Cos^{-1}(\frac{V_{dc}Cos(\sigma_{opt})}{V_{dc\,ref}}) \tag{7-34}$$

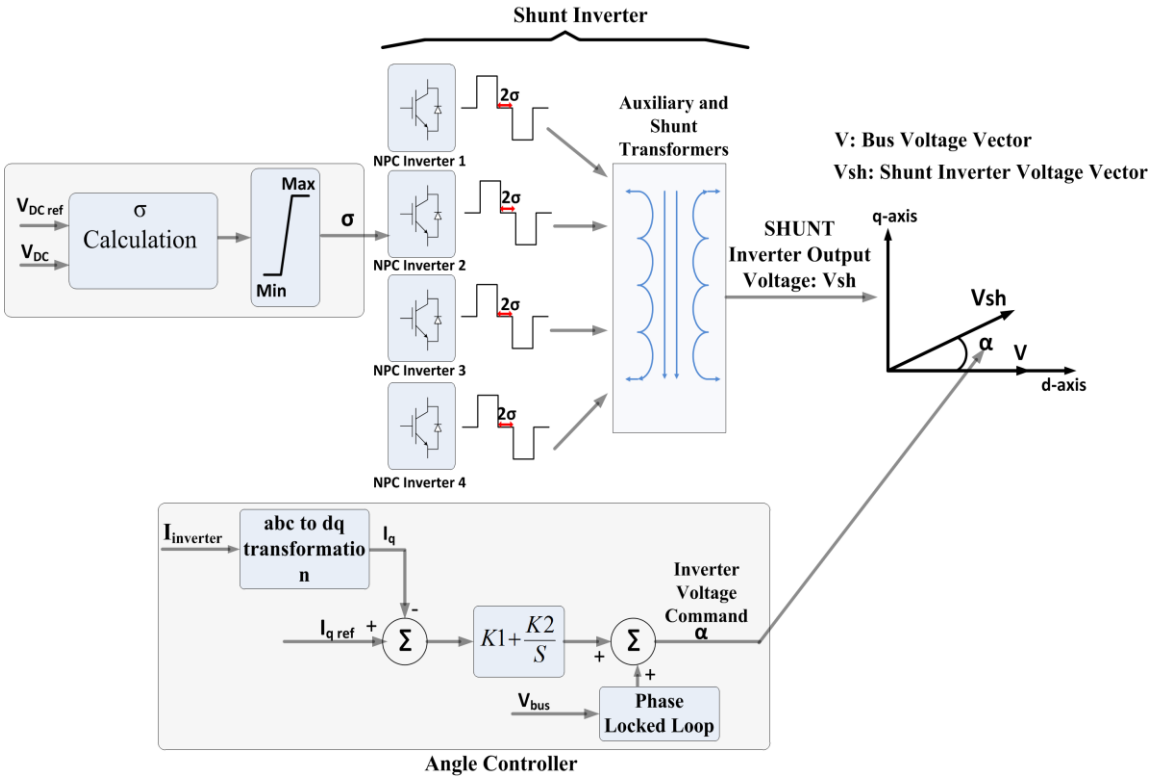

Figure 7-20. Proposed control structure

σ_{cal} is calculated based on the fact that the shunt inverter angle-controller, keeps the STATCOM output voltage unchanged after changing the σ such that the $i_{q\,sh}$ and consequently STATCOM operating point remains constant. V_{sh1} and V_{sh2} are the shunt inverter output voltages before and after changing the σ. After changing the σ to σ_{cal} , the angle-controller brings the DC-link voltage up such that in the steady state the STATCOM output voltage V_{sh2} reaches to its previous value of V_{sh1}. $V_{dc\,ref}$ is the desired DC-link voltage set by the system operator such that the transmission line active and reactive values become closer to their reference values. This solution is conceptually illustrated in Figure 7-20.

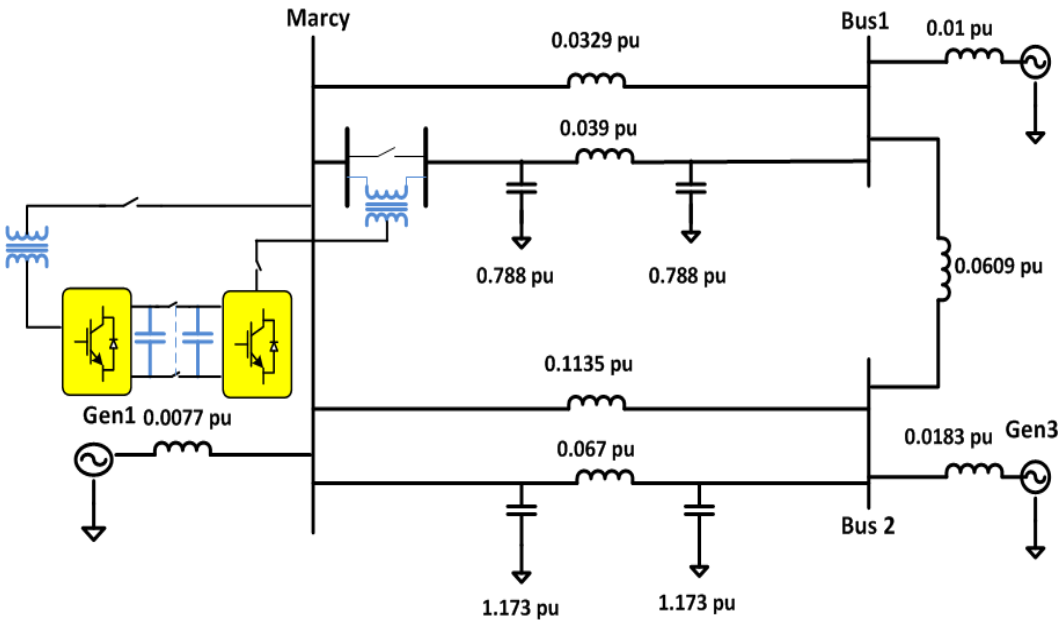

Figure 7-21. Simulation system, UPFC model based on the NYPA UPFC at Marcy substation is connected to the NYPA 3-bus AC-system. All the per unit values are based on 100 MVA and 345kV system.

7.11 Simulation Results of the UPFC Connected to the New York Power Authority 3-Bus Ac-system model

This part of the paper presents the simulation results of the proposed solutions. The UPFC model developed based on the NYPA UPFC (Figure 7-8) has been connected to the reduced order 3-bus AC-system model of the NYPA power system as shown in Figure 7-21. As discussed in the previous sections, the shunt inverter is controlled with angle-control strategy. The series inverter is controlled with advanced control method.

Plots in Figure 7-22 illustrate the basic UPFC performance. Initially (from t=0.2 seconds to t=0.3 seconds) the UPFC is not in the operation and therefore the series injection voltage is zero. As can be seen in this figure, the transmission line active power is about 610

MW which is corresponding to $i_d = 1.45$ kA ($P = \frac{3}{2}|V|i_d \approx \frac{3}{2} \times 345 \times \sqrt{\frac{2}{3}} \times 1.45$). The reactive power flow is at around 20 MVAr. At t=0.3 the UPFC starts to work with settings of $i_d \approx 1.2$ kA (P=510 MW), and $i_q = 0$ (zero reactive power flow). As can be seen, the active and reactive power flows follow their references very quickly and smoothly. At t=0.4 seconds the reference for the i_d is switched to 1.7 kA (718 MW) while the i_q reference remains at zero. The active power flow increases quickly from 510 MW to around 720 MW, while the reactive power remains almost unchanged.

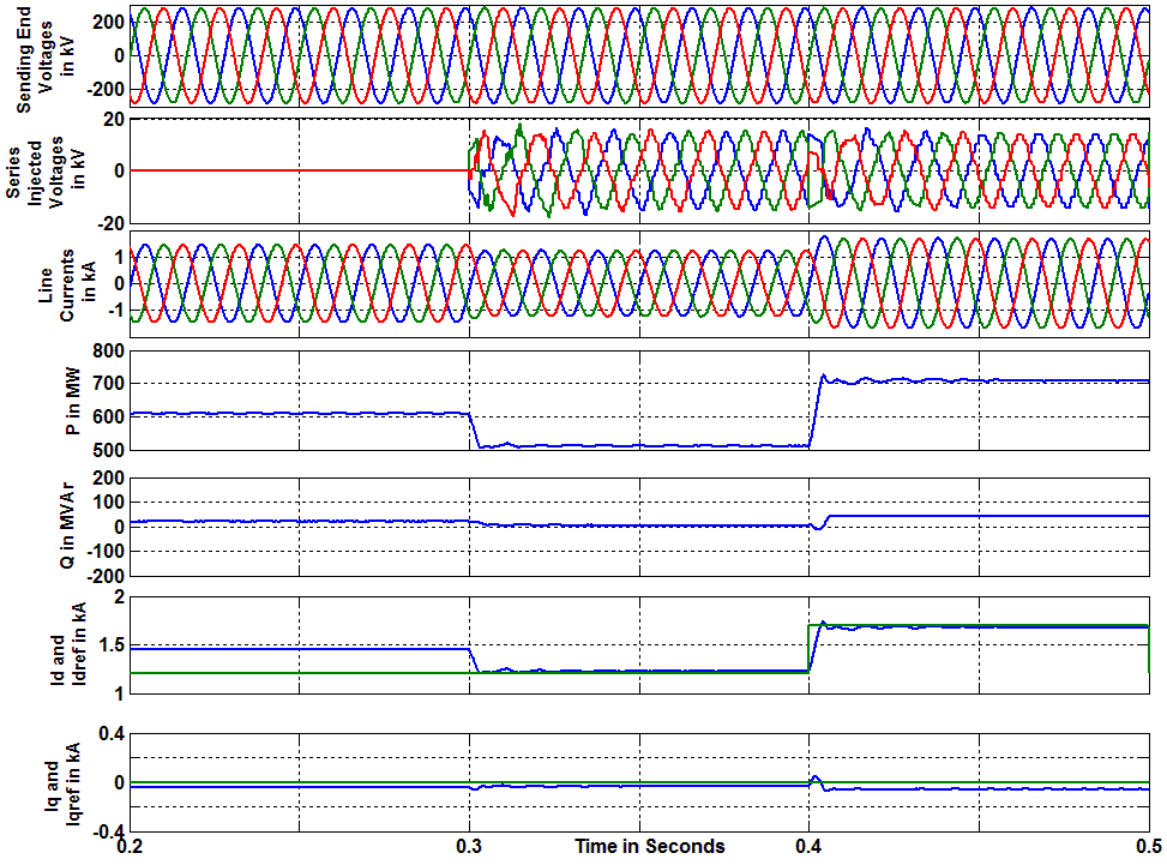

Figure 7-22. Simulated UPFC performance with different active and reactive power references

Plots inFigure 7-23 illustrate the UPFC performance with and without the proposed solution. Initially the transmission line active and reactive power flows are around 730 MW, and 70 MVAr respectively. The shunt inverter is set to inject 1 pu capacitive current (167.347 A, all the per unit values are based on 100 MVA, and 345 kV system) to the grid. At t=0.5 seconds the shunt inverter is switched from the capacitive mode to the inductive mode and absorbs 1pu of inductive current from the grid. This change in the shunt inverter operating point results in DC-link voltage reduction from 13kV to 10.65 kV. This reduction in the DC-link voltage decreases the series inverter voltage injection and therefore the transmission line active and reactive power decrease from their reference values. At t= 0.6 seconds, the σ is switched from its optimal value (3.75˚) to σ_{cal} =27.6˚. This σ_{cal} is calculated based on (7-34) to bring the DC-link voltage from V_{dc}=10.65 kV to $V_{dc\,ref}$ =12 kV. Increased DC-link voltage increases the series injection voltage and therefore the transmission line active and reactive power flows get closer to their reference values. It is important to note that after changing the σ, the STATCOM operating point remains unchanged and keeps absorbing 1pu of inductive current from the grid. Plots in Figure 7-24 indicate the same results as in Figure 7-23 for the time that UPFC works with and without the proposed solution but this time the $V_{dc\,ref}$ is set to 13 kV. Similar to the previous test, initially the shunt inverter injects 1 pu of capacitive current to the grid and then at t=0.5 seconds it is switched from capacitive mode to the inductive mode and absorbs 1pu of inductive current from the grid. Let us assume that it is very important for the power system operator to keep transmission line active and reactive power flow as close as possible to their

reference values. Therefore, the reference value of the DC-link voltage is set to 13kV which is the DC-link voltage level before the shunt inverter switched to inductive mode. From t=0.5 to t=0.6 seconds the UPFC works with conventional controller and as can be observed the line active and reactive powers are deviated from their reference values. At t=0.6 seconds the σ is switched from its optimal value 3.75˚ to σ_{cal} =35˚ to obtain the DC-link voltage of 13 kV. This increase in the DC-link voltage brings the transmission line active and reactive power close to their reference values while the STATCOM operating point remains unchanged.

Under the same scenario, Figure 7-25, and Figure 7-26 verify the proposed solution when the DC-link voltage is set to 11.5 kV (σ_{cal} =22.4˚) and 12.5 kV (σ_{cal} =31.7˚) accordingly.

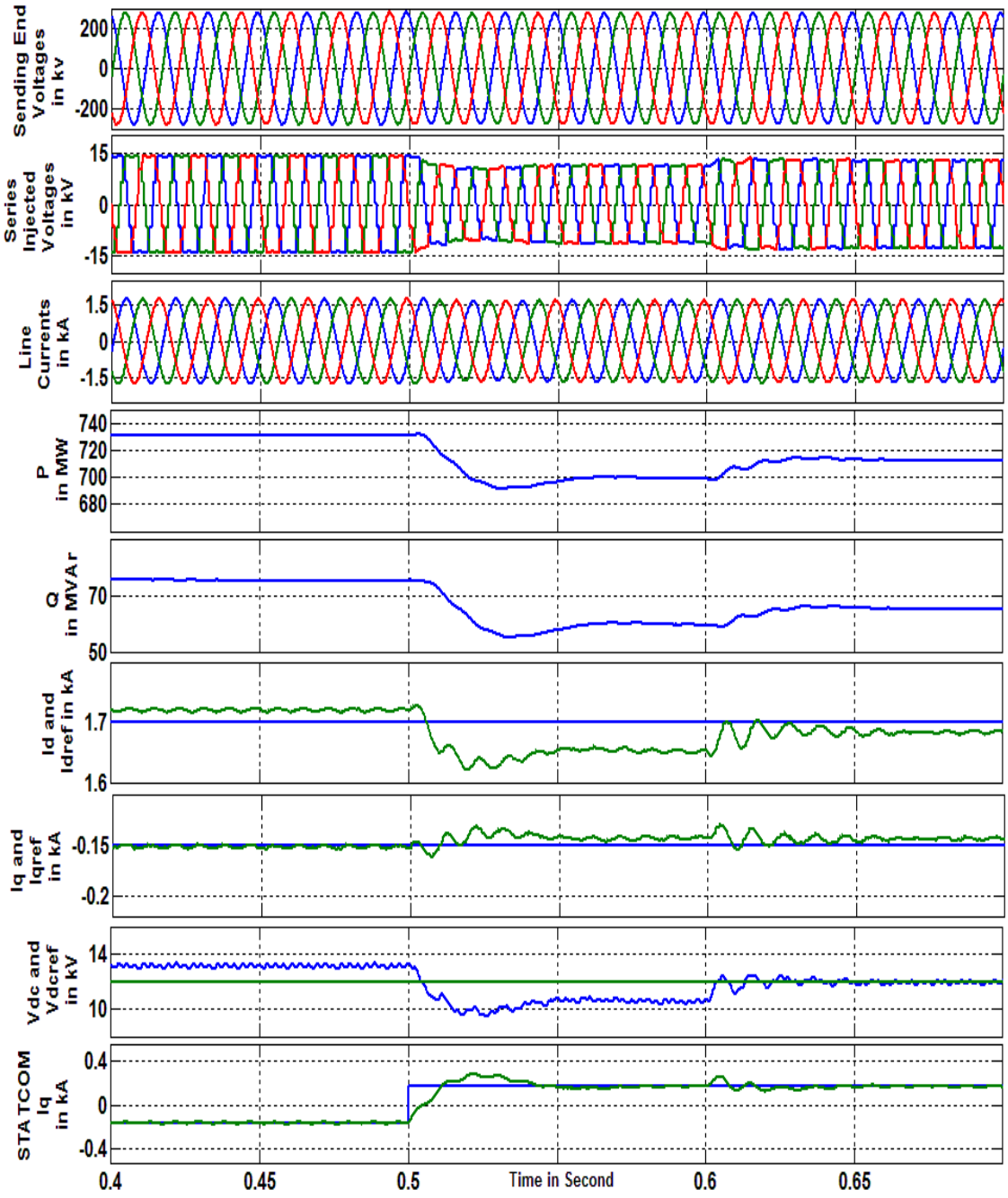

Figure 7-23. UPFC performance when the shunt inverter operating point changes form fully capacitive to fully inductive with and without proposed solution. The desired DC-link voltage is set to 12kv (σ_{cal} =27.6˚).

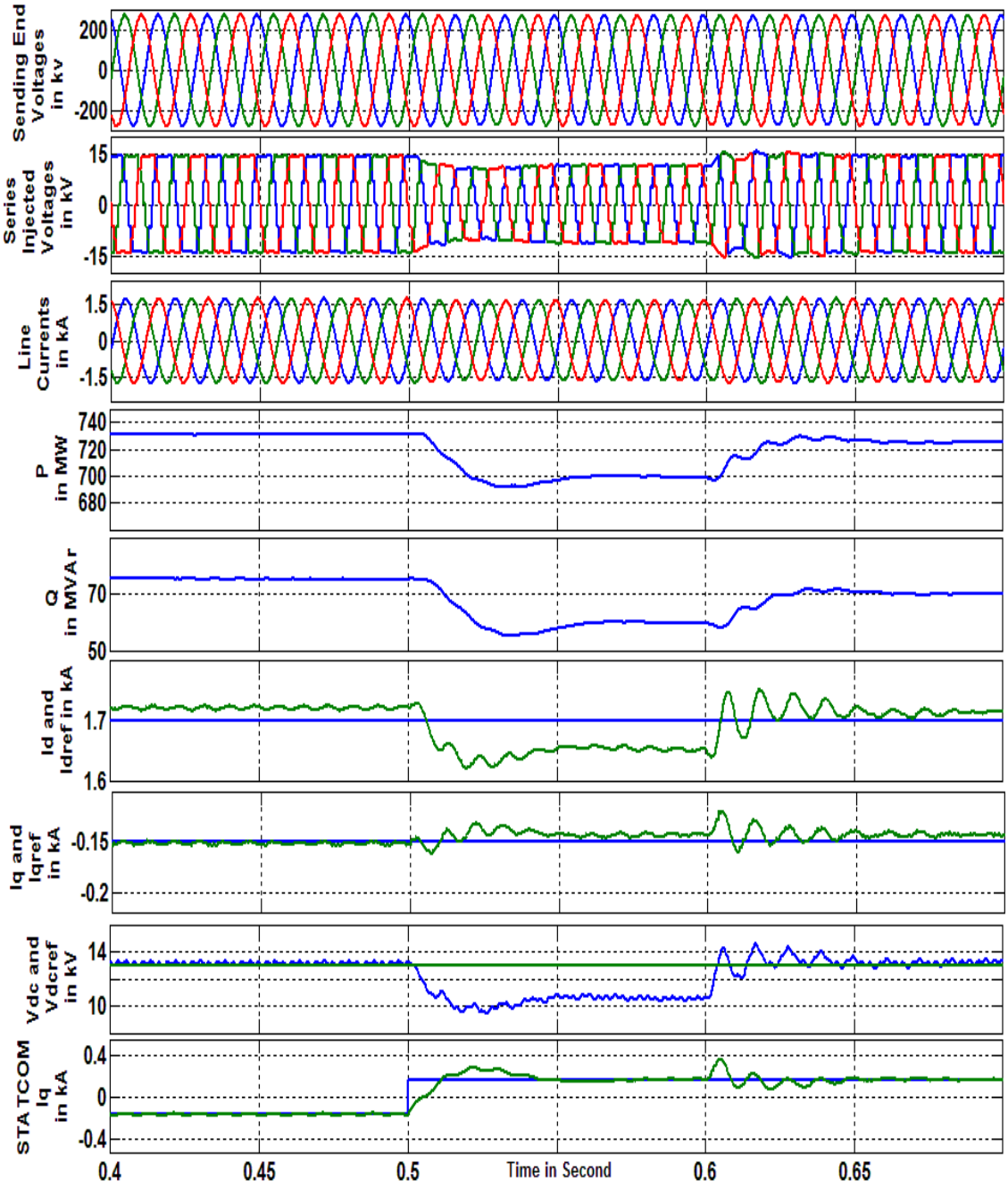

Figure 7-24. UPFC performance when the shunt inverter operating point changes form fully capacitive to fully inductive with and without proposed solution. The desired DC-link voltage is set to 13kv (σ_{cal} =35.1˚).

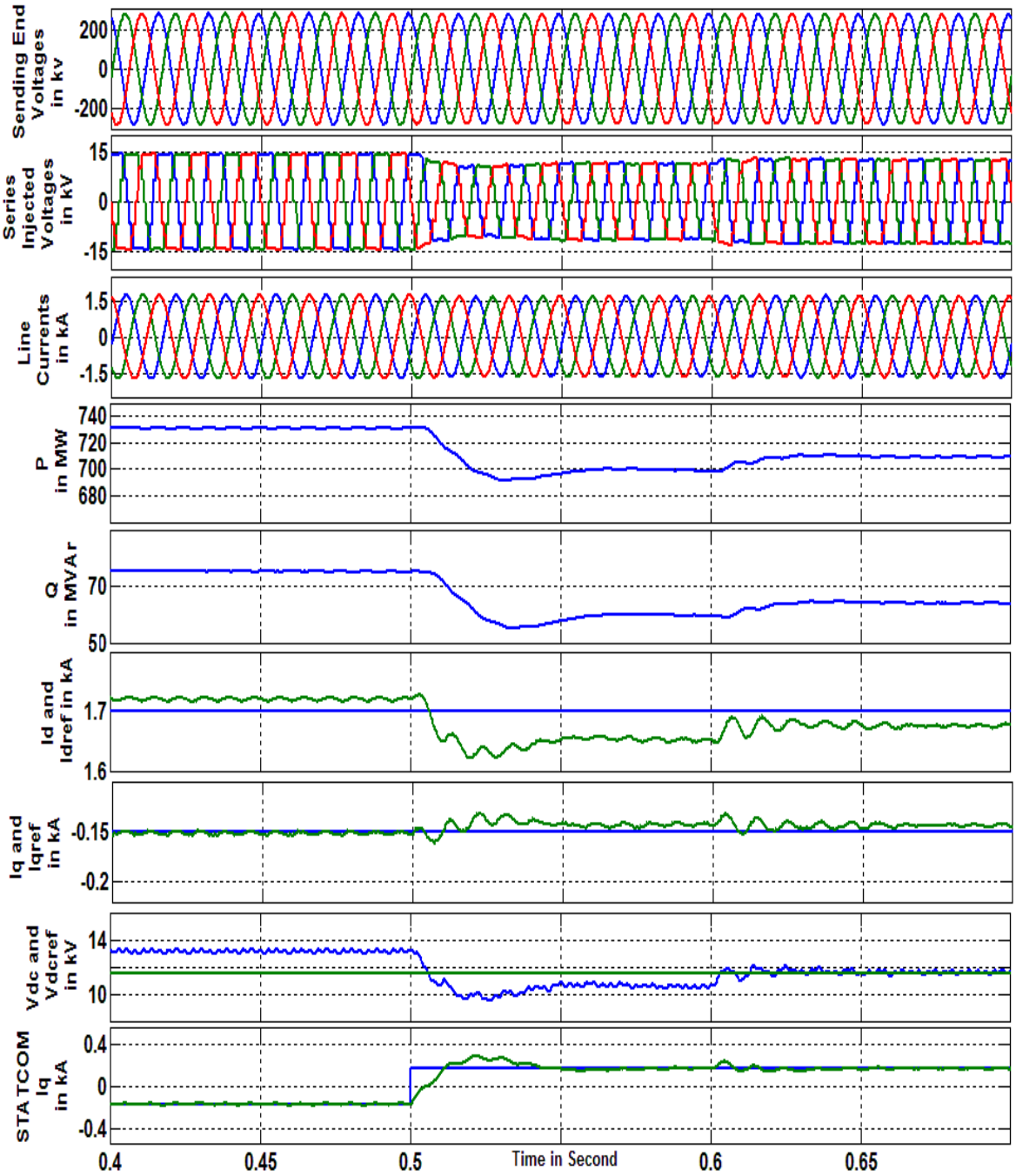

Figure 7-25. UPFC performance when the shunt inverter operating point changes form fully capacitive to fully inductive with and without proposed solution. The desired DC-link voltage is set to 11.5kv (σ_{cal} =22.4˚).

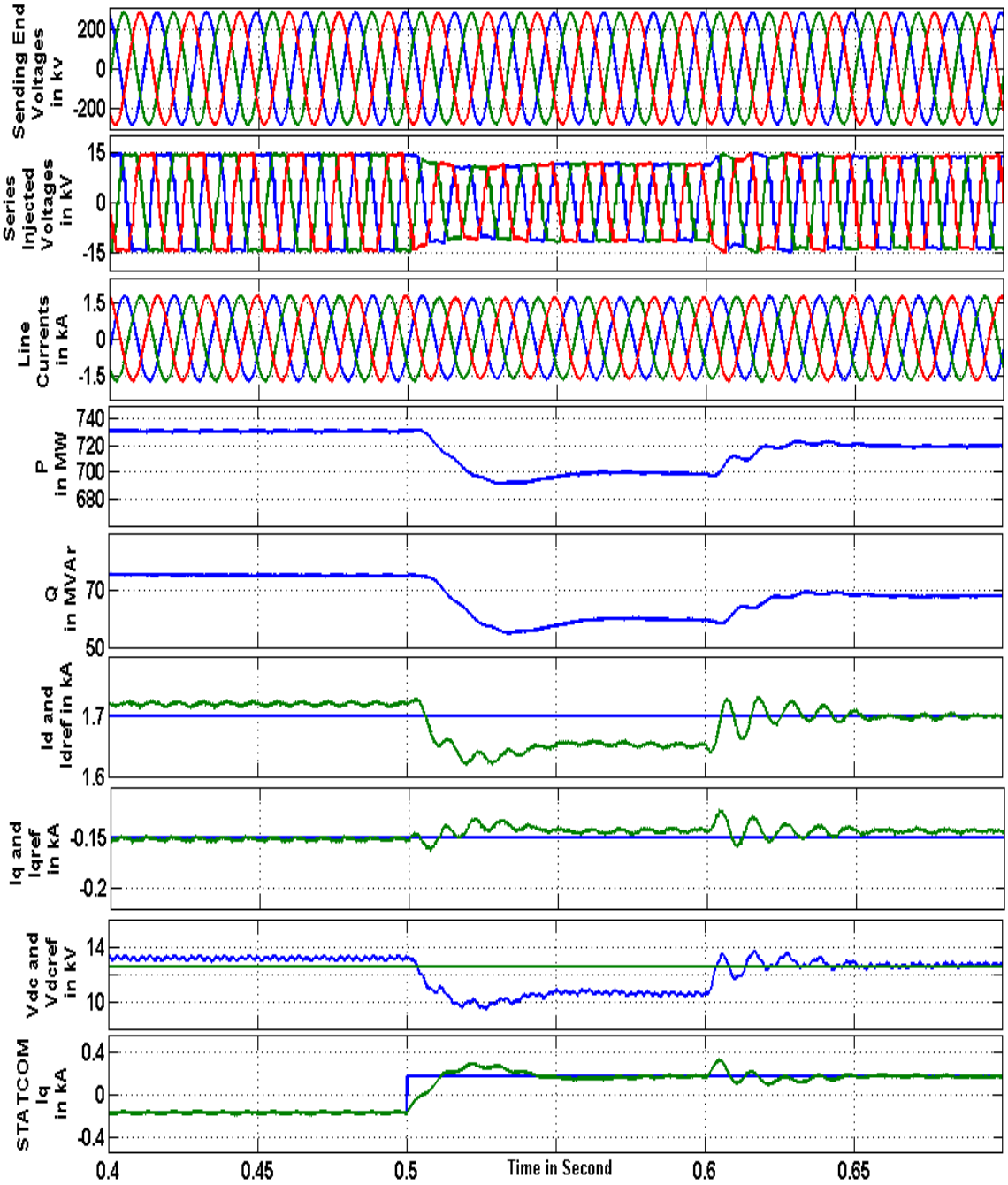

Figure 7-26. UPFC performance when the shunt inverter operating point changes form fully capacitive to fully inductive with and without proposed solution. The desired DC-link voltage is set to 12.5 kv (σ_{cal} =31.7˚).

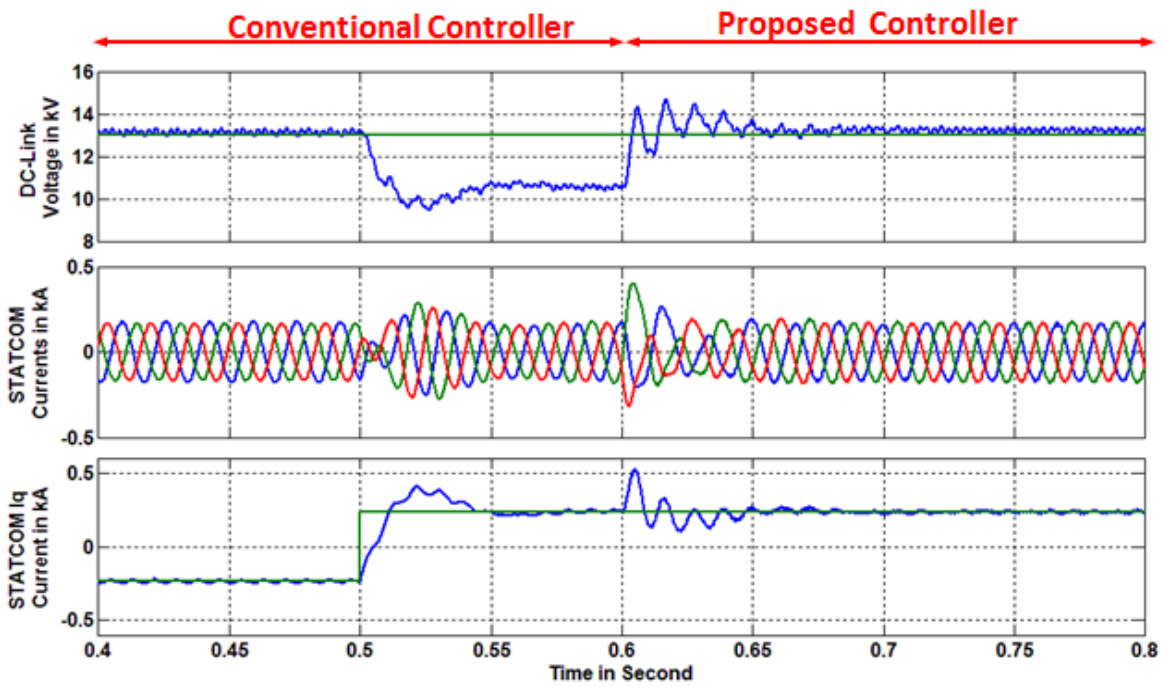

Figure 7-27. UPFC shunt inverter performance when the shunt inverter operating point changes form fully capacitive to fully inductive with and without proposed solution.

Plots in Figure 7-27 take a close attention to the shunt inverter performance of Figure 7-24. This picture mainly focusses on the STATCOM three phase currents. As can be observed, after the UPFC starts to work with the proposed solution at t=0.6 seconds, the STATCOM currents reach to their steady states after just a few cycles.

As discussed in the previous section, the STATCOM tie line impedance is seen as a large impedance by the high order harmonics generated due to the increase in the σ. Therefore, those high order harmonics can barely reach to the grid. Figure 7-28 indicates the STATCOM current THD with different σ values. As can be observed in this figure, it is possible to change the σ in a large range of the values without too much change in the STATCOM current THD.

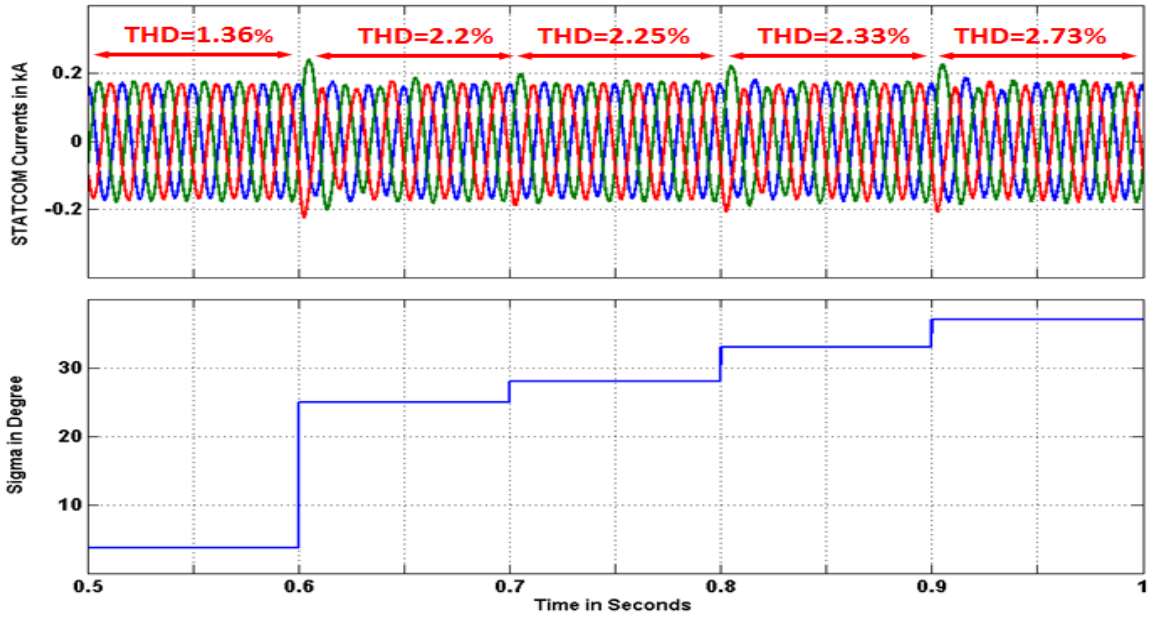

Figure 7-28. UPFC shunt inverter currents and their THD with different δ values.

7.12 Summary

This chapter proposed a solution to increase the controllability range of the specific type of the UPFC in which the DC-link voltage is regulated over a range of the values instead of a constant value. This kind of the UPFCs are very attractive for the transmission level applications due to their low converter losses. Many of the UPFC installations around the world are of this kind. The proposed solution was validated with PSCAD simulation results.

Chapter 8: Summary of the work

This chapter provides a summary of the dissertation and brings out the contribution of each chapter.

Followed by the introduction, chapter 2 provided a literature survey on essential topics of this research. It started with calculating a mathematical model for generally a VSC and particularly a STATCOM connected to the grid. That was followed by the introduction of the existing control structures for the STATCOM (PWM-based vector controller, and angle-controller) and discussing the pros and cons of each of them for the transmission level application.

Chapter 3 addressed the issues regarding the angle-controlled STATCOM performance under AC-system faults. It started with calculation of the DC, and AC-sides waveforms of the STATCOM under unbalanced condition and afterward these equations were particularly used to develop the Dual angle controller. DAC limits the STATCOM fault currents and removes the DC-link voltage 2^{nd} harmonic oscillation under severe unbalanced conditions and AC-system faults. The proposed DAC performance was validated by the simulation and experimental results.

Chapter 4 addressed the same issue of the Angle-controller STATCOM performance under unbalanced condition and AC-system faults that was discussed in the preceding chapter but proposed an alternative solution to resolve it. A new converter topology along with appropriate control structure was presented in this chapter that limits the negative sequence currents under system faults. The proposed solution was validated by the simulation results.

Chapter 5 used the basic idea of the chapter 3 to develop an alternative control structure that improves the PWM-controlled VSC-based STATCOM performance under AC-system fault conditions. The theoretical results of this chapter were supported by the simulation and Hardware-In-the- Loop-test results.

Chapter 6 proposed a control structure that improves the grid-connected PWM-controlled VSC currents Total Harmonic Distortion (THD) and removes the DC-link voltage oscillations when the input voltage is distorted by the low/high order harmonics. The input voltage harmonic can range from (-1) which corresponds to the unbalanced AC-system conditions to any high order harmonic (providing that the switching frequency is high enough). In particular, when the input voltage is unbalanced due to the fault condition, the proposed controller instantly limits the negative sequence current and removes the DC-link voltage oscillations. The proposed controller performance was validated by the precise simulation and Hardware-In-the- Loop-test results.

Chapter 7 started with deriving the mathematical model of the UPFC series inverter. Based on this model, existing power flow controller were discussed and analyzed with appropriate simulation results. A close attention was taken into the specific type of the UPFC in which the DC-link voltage is not fixed but regulated over the range of the values. This type of the UPFC was discussed in detail through this chapter. Finally this chapter ended up with proposing a controller that increases the controllability range of this type of the UPFC when the DC-link voltage is at its minimum value.

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