ABSTRACT

DUTTA, SUMIT. Controls and Applications of the Dual Active Bridge DC to DC Converter for Solid State Transformer Applications and Integration of Multiple Renewable Energy Sources. (Under the direction of Subhashish Bhattacharya).

The Dual Active Bridge (DAB) converter was first developed in the University of Wisconsin Madison in 1989. Since then the converter has gained popularity because of its high power density, high efficiency due to ZVS operation under wide load range, bidirectional operation and high frequency isolation. The traditional control of the converter is based on phase shift modulation. The primary bridge which supplies power phase leads the secondary bridge which absorbs power. Extensive research has been done previously on the small signal analysis and the dynamics of the converter. In order to further improve the speed of response of the converter and to have a control on the DC bias level in the high frequency transformer current, a digital predictive current mode controller for the DAB converter is proposed in this thesis. The first chapter discusses the proposed current mode control. The controller is shown to track the reference current within a switching period provided the correct inductance information has been provided to the controller. Additional control methods are developed to observe and remove DC bias flux in the high frequency transformer and the high frequency inductor. Experimental results are provided to verify the working principles of the current controller. In the second portion of the thesis, a multi-terminal topology variant of the DAB converter was explored with storage and renewable energy integration. A multi – limb core transformer based DAB converter (MLC-DAB) is proposed and developed for this application. The equivalent circuit of the MLC-DAB topology is developed using the gyrator concept and the advantage and disadvantage of the proposed topology is shown with respect to a single core multiple winding DAB topology or a series connected multi-terminal DAB topology. A pulse

width modulation (PWM) based input current control is developed for the MLC-DAB to integrated different renewable energy sources operating at different maximum power points. In the final chapter of the thesis the application of the DAB converter in the DC stage of a Solid State Transformer (SST) is discussed. A single phase cascaded solid state transformer is considered with the DAB converter in the DC to DC stage. A soft start algorithm is proposed for the SST to reduce inrush currents at startup. The MLC-DAB topology is considered for the cascaded single phase SST and is shown to require simpler control compared to a conventional DAB topology. A micro grid is developed with two parallel connected single phase single stage SST with MLC-DAB. The system is demonstrated experimentally in grid tied mode with power being injected into the grid from renewable energy source (emulated by DC source) integrated to the MLC-DAB stage of the SST. In case of grid failure a black start mode algorithm is developed and is implemented with one of the SST acting as a master and maintain the PCC voltage while the slave SST work in constant current injection mode. The critical load points are recognized within the micro-grid and black start algorithms are developed to provide for uninterrupted power to the critical load points.

Controls and Applications of the Dual Active Bridge DC to DC Converter for Solid State Transformer Applications and Integration of Multiple Renewable Energy Sources

by
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DEDICATION

To my mother, father and my little brother….

BIOGRAPHY

The author was born in Calcutta (India) on the 31st of January 1984. He did his schooling from the Ramakrishna Mission Vidyalaya Narendrapur. He finished his bachelor studies from the Indian Institute of Technology, Kharagpur, India in 2008 from the department of Electrical Engineering with specialization in Energy Engineering. Since the August of 2008 the author has been enrolled in the Electrical Engineering Department perusing the Ph.D. in Electrical Engineering with focus on Power Electronics and Controls.

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Chapter 1 Introduction

1.1. Research back ground

The recent years have seen the growing need of the renewable energy sources (RES) integrating to the conventional grid. With the development of Power Electronic converters along and the advancement of power semiconductor devices, RES can now be directly integrated to the existing grid by means of various power converter topologies. DC to DC converters provide the interface so that the RES can operate at maximum power point, and DC to AC inverters are used as an interface to the conventional 60 Hz grid. Amongst the several topologies that are available for the RES integration the solid state transformer (SST) topology is becoming widely popular [1], [2] concept. The SST is considered to be a replacement for the conventional 60 Hz transformer. It has an AC front end followed by an isolated DC to DC stage followed by inverter supplying a load or another grid (Fig. 1.1).

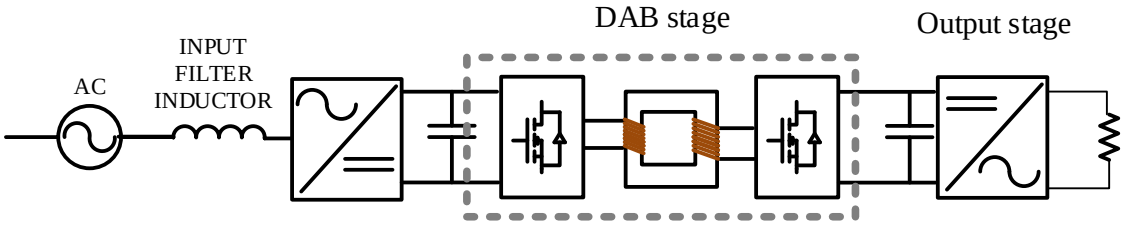


Figure 1.1: Solid State transformer topology

The SST unlike a conventional 60 Hz transformer is a multifunctional device. In addition to providing isolation it provides a DC bus to integrate the renewable energy sources to form a DC-micro grid [3], [4], [5].

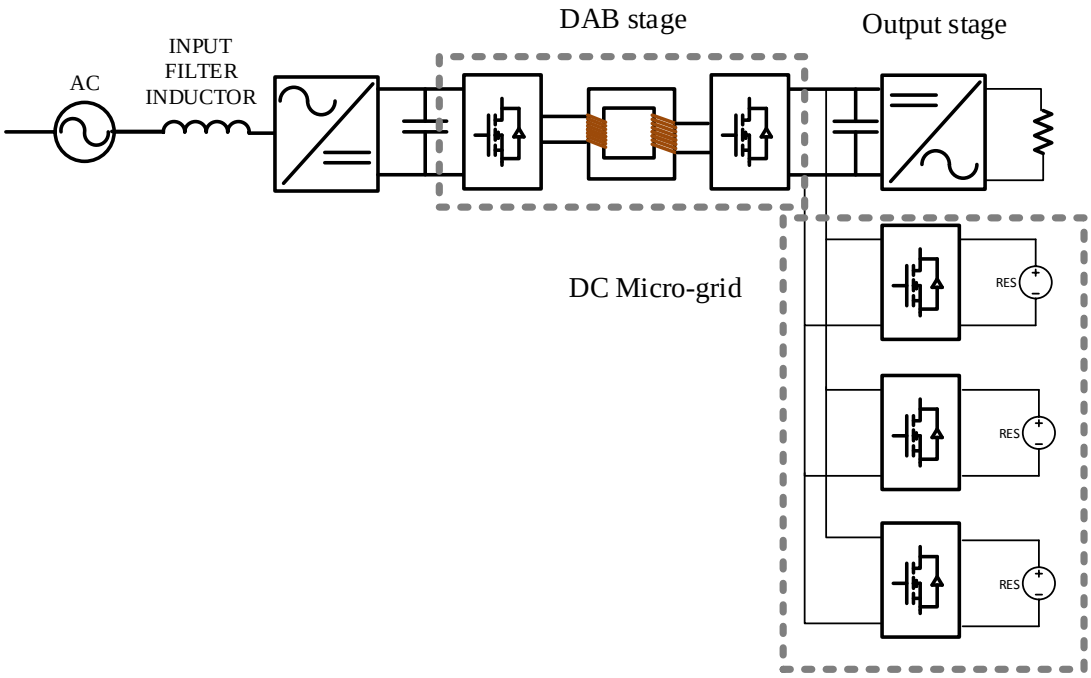


Figure 1.2: The SST topology with the DC micro-grid

One of the most popular DC-DC topology for the SST application is the Dual Active bridge converter (DAB) which is the main topic of discussion in this thesis. The DAB converter was first developed in 1989 in University of Wisconsin, Madison [6], [7], as an isolated DC to DC converter for higher power application. Both single phase and three phase topology was developed. The topology has high-frequency isolation along with bidirectional power flow

capability. It is capable of soft switching (ZVS turn on) that reduces the turn on switching losses. All these properties make the DAB a very suitable candidate for the SST application. The closed loop control and small signal transfer function of the converter has also been derived in [6], [8], [9]. The traditional control of the DAB converter is based on phase shift modulation where the leading bridge provides power to the lagging bridge. A dual loop control for the DAB has been proposed in [9]. Both the outer (voltage) and the inner (current) control loop are based in PI regulators with the assumption that the inner loop is faster than the outer loop by a factor of 10. This decouples the outer voltage and inner current loop but a bandwidth limit on the outer voltage control loop. To improve the outer voltage bandwidth, the inner current loop bandwidth needs to be improved which can be achieved by implementing a predictive current mode control. However in literature the predictive current mode control for the DAB has not been reported.

1.2. Motivation

Considering the DAB converter having a dual loop control, in order to improve the bandwidth of the outer voltage loop the inner current loop has to be made fast. This provides the motivation of developing a predictive current control as the inner current loop for the DAB converter. The predictive current control proposed in [10] has the advantage of providing a response within one switching cycle, thus having a bandwidth equal to the switching frequency. This allows the outer voltage loop to have a higher bandwidth of operation and thus provide for a faster response. Furthermore the inner current loop based on average current measurement [1] requires continuous sampling over one switching cycle or half cycle. The

predictive current mode control on the other hand requires sampling only once or twice in the switching cycle that reduces burden on the controller. This provides the motivation for investigating the predictive current mode control for the DAB converter. The renewable energy integration however provides a different challenge for the DAB converter. (Fig. 1.2). Parallel connection of several different renewable energy sources requires either master-slave mode of control or parallel DC droop mode of control [11]. The complexity in controls provides the motivation of integrating the RES directly within the DAB magnetic stage. This leads to a multi-terminal DAB stage design where different terminals are connected to different RES. The quad – active bridge (QAD) converter has been proposed [4] where multiple input bridges are connected to a RES and the output bridge is load connected or grid tied. Fig. 1.3, the multi-active bridge topology, the windings connected to each RES cuts the same flux. Hence they get the same induced voltage across each winding. Mismatch in the winding voltages with the source voltage will lead to circulating reactive current flowing through the converter bridges [22] leading to higher losses and lower efficiency. Further topologies in the multiport DAB have been reported in [4], [13] (Fig. 1.4). Thus in case there is wide voltage variation between the different renewable sources, there is a requirement for decoupling the different sources from each other. The problem of cross coupling between the renewable energy sources have been dealt with in [4]. However a topology based solution was never considered to decouple the individual RES from each other while still maintaining galvanic isolation.

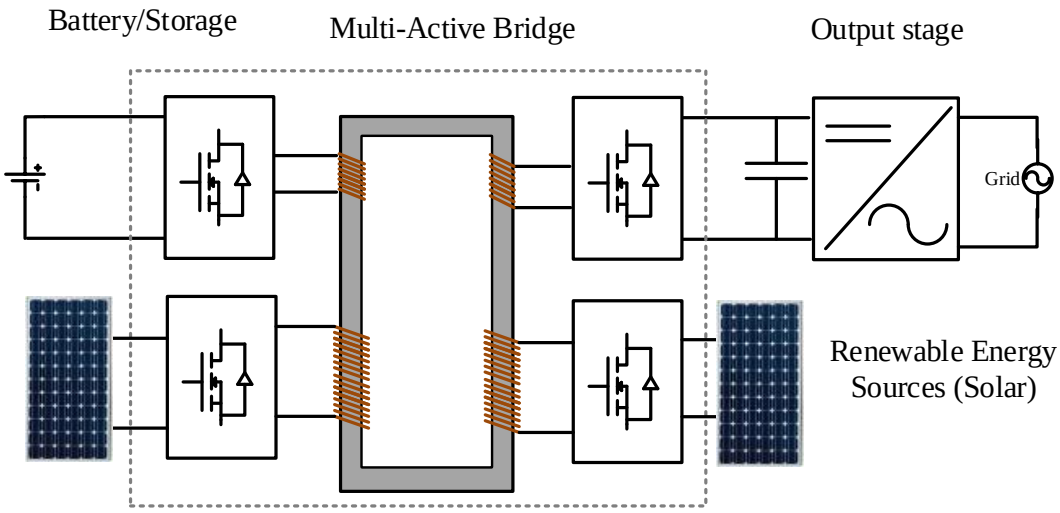


Figure 1.3: The multi-active bridge topology with grid tied output (Solar panels from CA Solar)

This led to the search for an alternate topology to integrate multiple RES while decoupling each source from the other. The concept of flux accumulation was considered and instead of a single limb core, a multi-limb approach was developed and the windings, instead of linking to a single common core, were linked to separate limbs to decouple individual sources from each other.

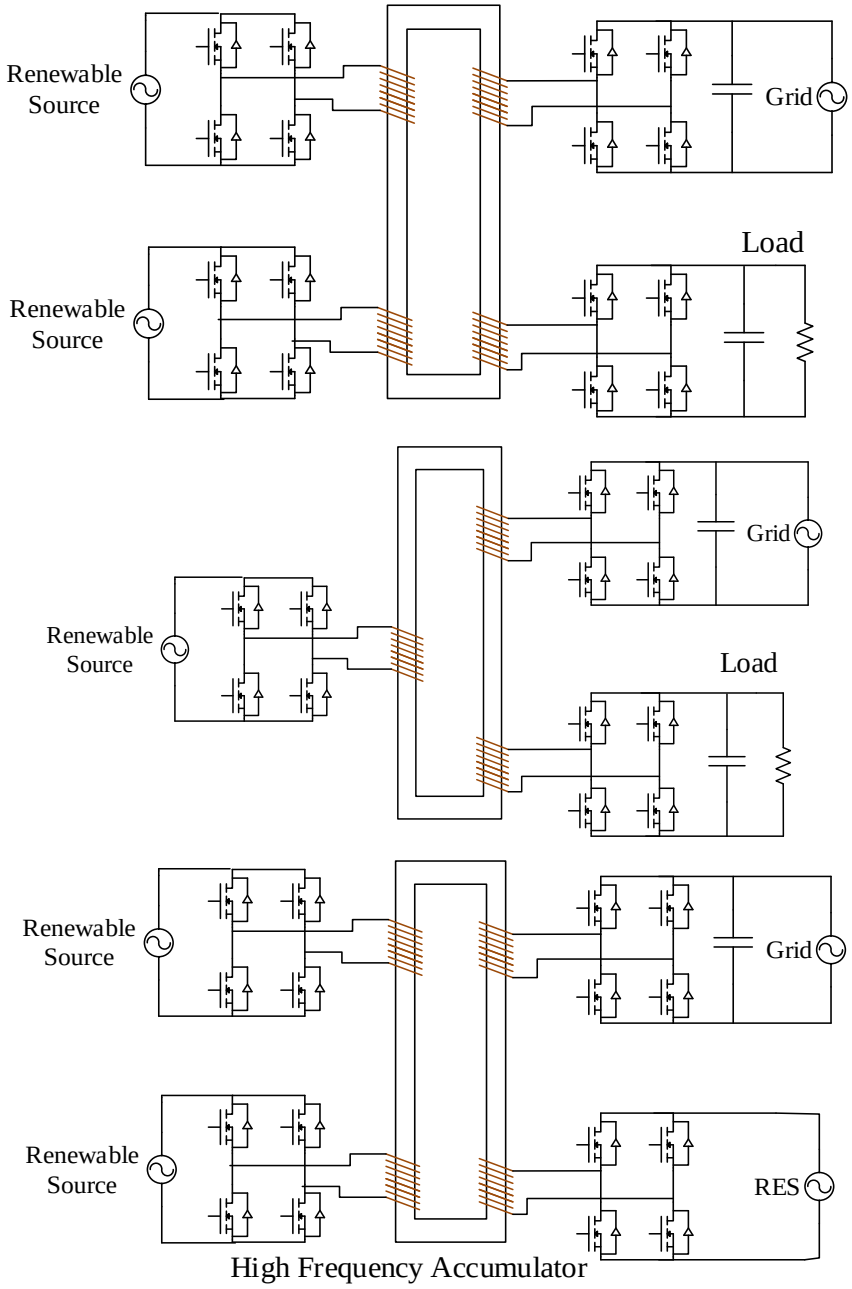


Figure 1.4: Different configurations of a multi-port DC-DC topology with a high frequency accumulator stage as reported in [13].

1.3. Thesis outline

Chapter 2 discusses the predictive current mode control for the DAB converter. Based on the different sampling points of the switching cycle, there can be different predictive current controllers. The different current controllers have been discussed in details with simulation results. Experimental verification of the controller has also been shown with step change in the current response to show that as the reference changes, the controller is capable to track the change in one switching cycle. Since the controller is heavily dependent on the leakage inductance value, a compensation loop was also proposed to remove the error due to leakage inductance mismatch. The compensation algorithm has also been verified through experimental results.

Chapter 3 proposes the multi-terminal DAB converter for multiple renewable energy source integration. The problem of circulating reactive power has been addressed by implementing a multi-limb core transformer for the DAB (MLC-DAB) that acts as an energy accumulator. Power flow control was demonstrated with power smoothening using battery as an energy buffer. Input current control was also implemented and demonstrated with experimental verification showing the ability of the converter to do maximum power point tracking.

Chapter 4 demonstrates the application of the developed MLC- DAB from Chapter 3 for grid integration of renewable energy sources. A single phase solid state transformer topology was considered with a cascaded front end with three DC bus. The MLC-DAB was integrated

into the DC stage of the SST showing simpler control on the front end as well as the DC bus. A parallel MLC-SST test bed was developed and the system was islanded to form a micro-grid with two parallel SST. Power sharing was demonstrated under islanding condition with master-slave mode of control.

1.4. Research contributions

The following are the research contributions from the dissertation:

1. A duty cycle mode of control was developed for the Dual Active Bridge converter.
2. A phase shift based predictive current mode control was developed for the Dual Active Bridge Converter.
3. A duty cycle based predictive current mode control was developed for the Dual Active Bridge Converter.
4. A stability analysis was performed to show the dependence of the phase shift mode predictive controller on the leakage inductance value and the stability limit have been reported.
5. A compensation algorithm was developed to compensate for the L-variation in the controller.
6. A multi - limb –core based Dual Active Bridge converter (MLC-DAB) was proposed with multiple input and single output for integrating multiple renewable energy sources to the converter.

7. Equivalent circuit for the 3 – limb core and 5 – limb core based multi-limb transformer was developed using the gyrator principle.
8. A PWM based input current control algorithm was developed to separately control the source currents of different sources connected to the MLC-DAB converter.
9. An alternate DC - DC converter topology for the DC stage of the cascaded solid state transformer was proposed based on the multi-limb transformer topology (MLC-DAB based SST) and the advantages in the control applications were shown.
10. A renewable energy hub concept was proposed to integrate multiple renewable energy sources to the grid based on the MLC-DAB concept.
11. A black start sequence was developed for parallel MLC-DAB based SST operation during islanding using the Master slave mode of power sharing.

Chapter 2 Current Control of Dual Active Bridge Converter

2.1. Introduction

The Dual Active Bridge (DAB) converter (Fig. 2.2) has two H-Bridges (primary and secondary) that are switched at 50% duty cycle. Power flow is controlled from one bridge to another by phase shift modulation [6]. A duty cycle modulation for the DAB converter to increase the ZVS range under light load condition have been reported [14], [15], [48]. However no research has been done on implementing a fast predictive current mode control. Nor has there been any research on removing the DC bias in the high frequency transformer currents under load transients or steady state. The first section of this chapter provides the motivation of implementing a fast inner current loop along with the outer voltage loop. An analog based peak current controller is also proposed in the following section. Next the digital predictive current controller is proposed based on the phase shift approach. A duty cycle mode of control is proposed that is implemented to remove the DC bias in the transformer current. Finally a power based controller is proposed that allows parallel operation of the converters with power balancing. The proposed controllers are verified with simulation platform (MATLAB Simulink) and experimental results.

2.2. Motivation for implementing a fast current mode control

A dual loop control (outer voltage loop with inner current loop) is the most popular method for controlling any DC to DC or DC to AC converter since it provides a current limit

for the converter. For the Dual Active Bridge Converter, the inner current control is implemented by half cycle moving window averaging on the high frequency transformer current. The outer voltage loop gives the desired reference current. The inner current loop produces the phase shift to match the average current equal to the reference (Fig. 2.1). The inner loop is required to be faster than the outer loop by at least a factor of 10 [9]. The output of the inner current loop is the phase shift angle that controls the power flow from the primary to the secondary bridge. The average current (Fig. 2.1) can be obtained both from analog stage or digital stage (moving window averaging) based on the implementation requirement [1].

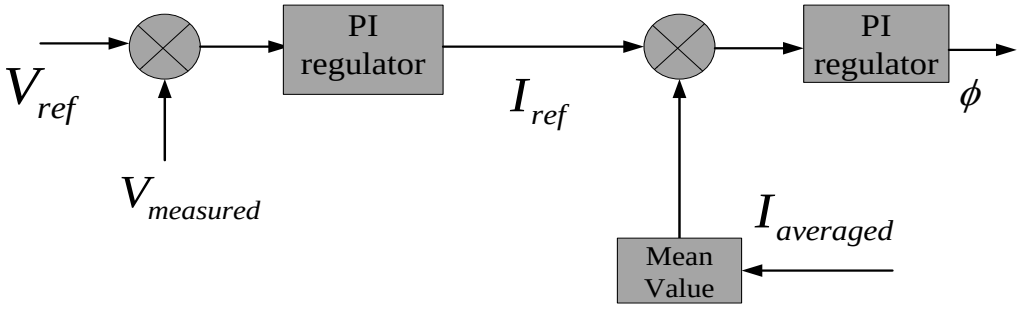


Figure 2.1: Block diagram of the DAB average current controller

However this mode of control imposes bandwidth limit on the outer voltage controller. Considering an example, if the switching frequency is 10 kHz, the inner current control can have a bandwidth of 1 kHz that limits the outer voltage bandwidth to 100 Hz. This bandwidth limit may be undesirable where the controller needs to compensate for fast load change. By implementing a predictive current control as the inner loop, the band width of the inner loop

can be made equal to the switching frequency i.e. 10 kHz allowing the maximum voltage control bandwidth to 1 kHz.

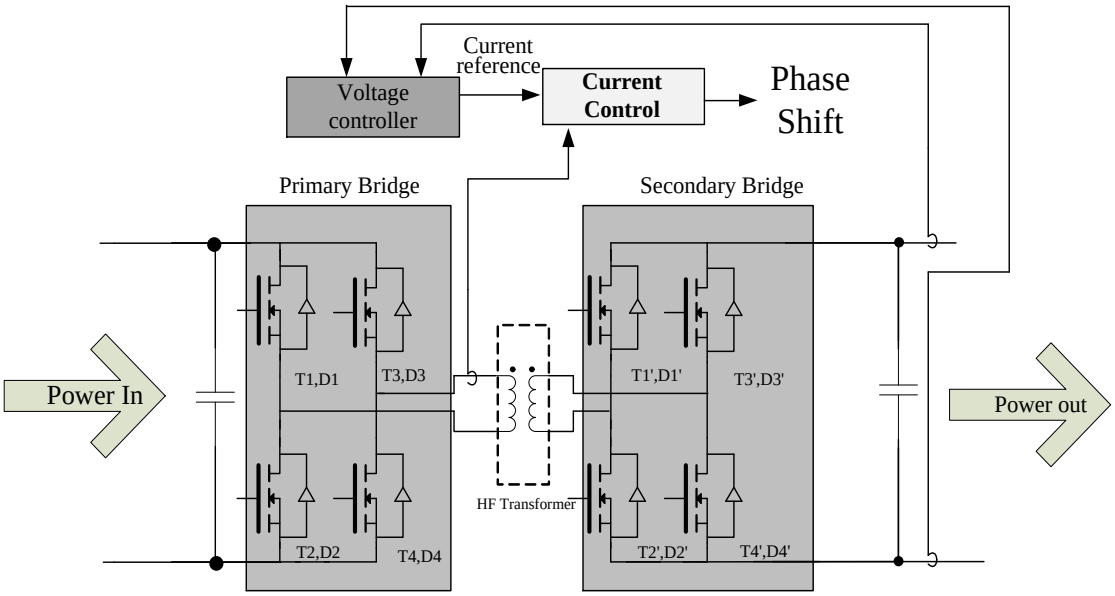
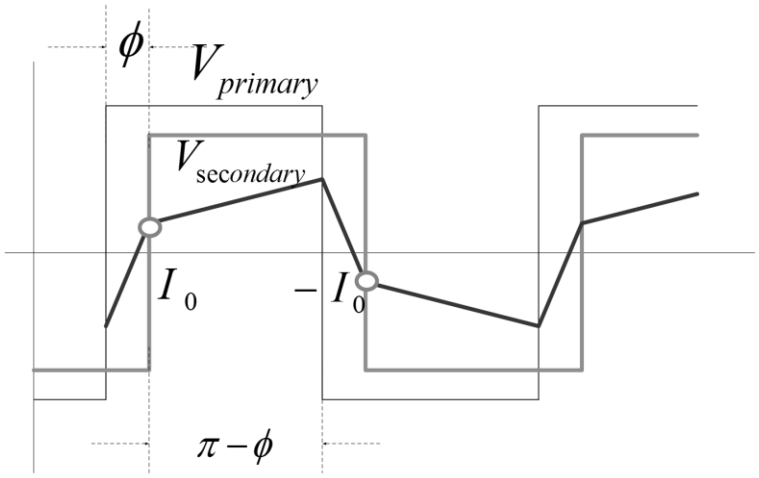


Figure 2.2: Circuit diagram of the DAB converter

2.3. Peak current mode control

The analog peak current mode control [16, Chapter 12] is a fast current mode control that provides an instantaneous control for the current (inductor current in Fig. 2.3) within one switching cycle since there is no compensator lag in the inner current loop. The peak current mode control for the DAB converter is proposed in this section of the chapter. In the peak current control mode the primary is the master bridge that switches with constant 50 % duty cycle. The transformer current is constantly monitored. The reference generated by the voltage

loop I_0 is compared with the measured value $I_{transformer}$ (Fig. 2.3 & Fig. 2.4) the switching scheme for the control is shown in Fig. 2.3. The switching is realized using an S R flip flop. There is no phase shift as such unlike average mode of control. Power flow is hence controlled by the current reference generated by the voltage controller. Although the name of the controller is peak current mode control, it is really not the peak current that is being monitored. The reference current can be used to regulate the current at $\omega t = \varphi$ or the current at $\omega t = \pi$ using different switching schemes. The switching scheme to regulate the current at $\omega t = \varphi$ has been discussed.



$$If\ I_{transformer} \geq I_0 \quad turn\,on\ S_5 \,\&\, S_8 \ \ turn\,off\ S_6 \,\&\, S_7$$

$$If\ I_{transformer} \leq -I_0 \quad turn\,on\ S_6 \,\&\, S_7 \ \ turn\,off\ S_5 \,\&\, S_8$$

Figure 2.3: Peak Current Control (switching scheme) for the DAB

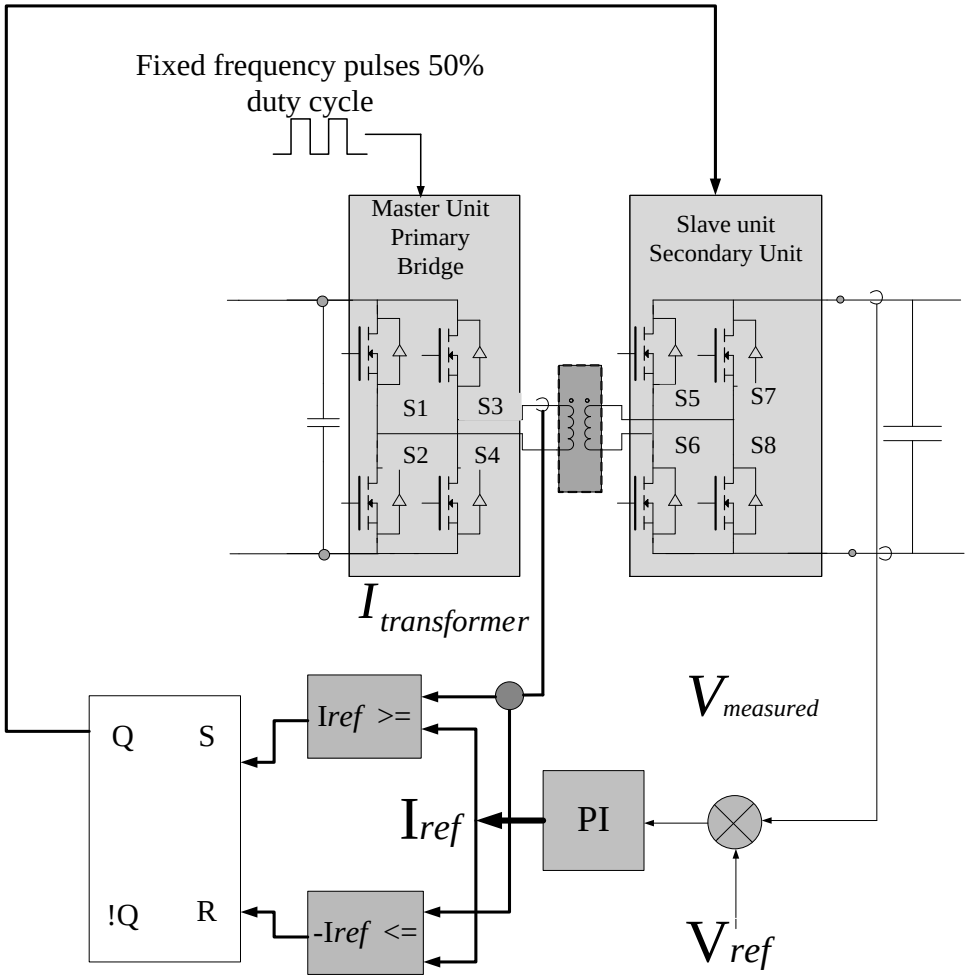


Figure 2.4: Controller for the peak current control.

The current I_0 at $\omega t = \varphi$ that is set to follow the desired reference can be related to the input voltage V_{in} and output voltage V_{out} as per (2.1).

$$I_0 = -\frac{V_{in}}{\omega L}\left(d\varphi + \frac{\pi}{2}(1-d)\right),\ d = \frac{V_{out}}{V_{in}}, \omega = 2\pi F_{switching} \tag{2.1}$$

$F_{switching}$ is the switching frequency of the converter, L is the leakage inductance of the transformer and φ is the phase shift angle between the primary and the secondary bridge. Thus

for a perticular *d* the current I_0 becomes fixed that drives the set and reset points on the SR flip flop of the peak current control. This control is fast and takes place within one switching cycle of the of the converter. However the disadvantage is that continuous sampling is demanded and has to take place in analog domain. A digital implementation of this controller is difficut which provides the motivation for the predictive current mode of control where the sampling can take place once or twice within one cycle and the control implementation can be done based on those sampled values only.

2.4. Predictive current mode control

The predictive current mode control [10] works by predicting the next state control parameter (phase shift or duty cycle) based on the previous state values. The predictive control mode for the DAB converter based on the phase shift is discussed in the following section.

2.4.1. Predictive Phase Shift Mode of Control

The predictive phase shift control for the DAB is discussed in this section. The current is sampled once in every switching cycle and the phase shift angle is calculated and updated at the beginning of the next cycle. Based on the number of times the current is sampled in the cycle and update takes place and the calculations are done, the predictive phase shift mode of control can be classified as follows:

1) Half cycle mode of control
2) Full cycle mode of control

Both the methods have their own respective advantages and disadvantages from the control and parameter sensitivity point of view. The following sections discuss the two controllers in details.

2.4.2. Predictive Half Cycle Phase Shift Mode of Control

In this mode of control the current is sampled at $\theta = 0$ and the current at $\omega t = \pi$ (or $\omega t = \varphi$) is the reference current and they are related as shown in Fig. 2.5 and Fig. 2.6. The required phase shift angle is pre-calculated from the equations shown in (2.2a) or (2.2b) and updated at the beginning of each switching cycle. The disadvantage of this mode of control is the sampled point $\theta = 0$ and the reference point $\omega t = \pi$ (or $\omega t = \varphi$) are not the same (Fig. 2.5). Hence we might need an added loop that observes the reference point. This observer model can also serve as a control loop to reduce parameter sensitivity of the controller. A mismatch between the desired reference and the actual reference might occur of there is an error in the inductor value that has been fed to the controller. Under such circumstance the error will be carried over in the phase angle calculation without the controller knowing. Fig. 2.6 explains the idea behind the installation of the observer. In this particular case the predictive controller samples the current at $\omega t = 0$ and the reference current is at $\omega t = \varphi$. If the current is sampled at $\omega t = 0$ and the current at $\omega t = \varphi$ is considered as the reference then the sampled current I_0 is related to the reference current I_{ref} as follows in (2.2a)

$$I_{ref} = I_{\omega t=\varphi} = I_0 + \frac{V_{in} + V_{out}}{\omega L}\varphi \qquad (2.2a)$$

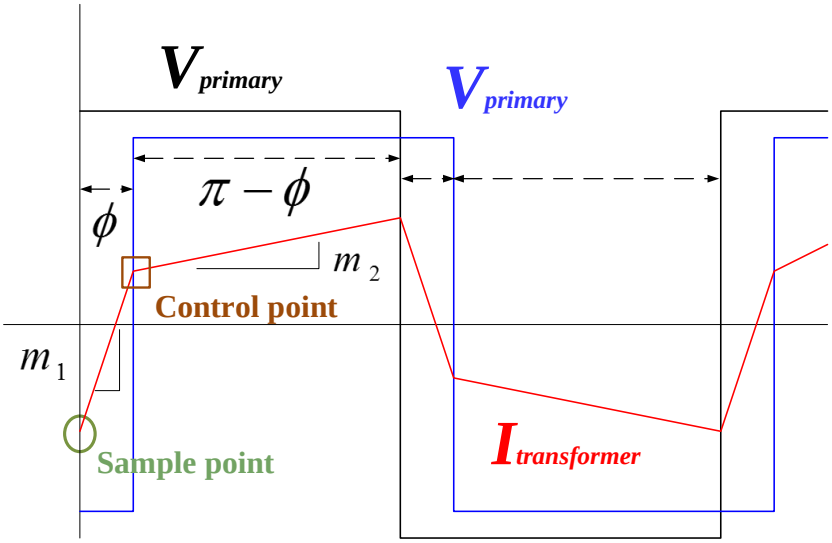


Figure 2.5: Predictive phase shift control

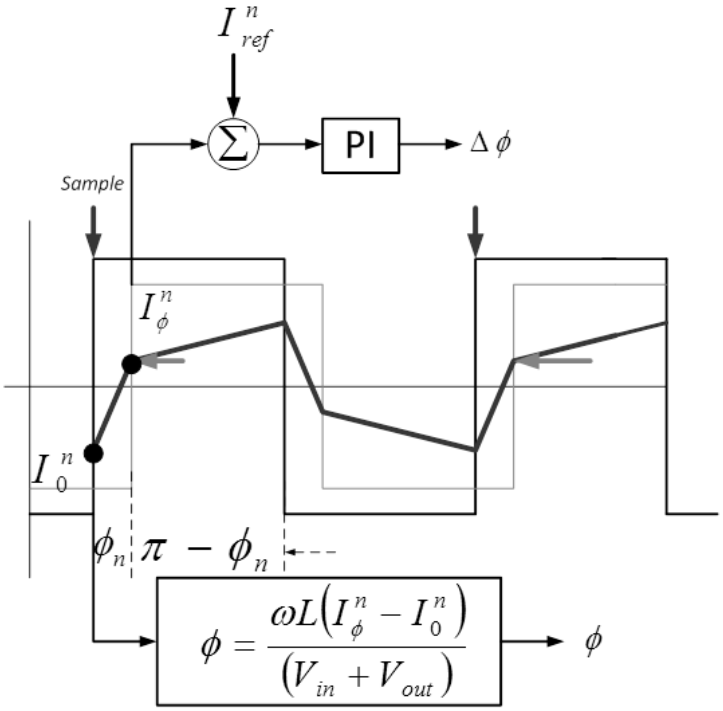


Figure 2.6: Observer loop for the Phase shift Predictive Current Controller

Keeping the sampling point same if the current is referred at $\omega t = \pi$ the equation becomes as follows in (2.2b)

$$I_{ref} = I_{\omega t=\pi} = I_0 + \frac{V_{in} + V_{out}}{\omega L}\varphi + \frac{V_{in} - V_{out}}{\omega L}(\pi - \varphi) \qquad (2.2b)$$

From either (2.2a) or (2.2b) the phase shift angle can be calculated in a deadbeat fashion. The phase angle updates within one cycle and does not depend on the previous state value. However since the sampled point is not observed, the predictive equation is heavily dependent on the accuracy of the measured leakage inductor value. In order to make the controller insensitive additional observer is introduced as shown in Fig. 2.6. The observer samples the current at the referring points on the switching cycle, at $\omega t = \varphi$ in the case of Fig. 2.6. Since this is the reference current, a proportion-integral control loop is implemented that adds an error phase angle to the predicted phase to compensate for the error (Fig. 2.6). Fig. 2.7 shows the simulation results with the observer in place. An error was intentionally inserted in the inductor value in the controller. L_{actual} was 100 μH while $L_{controller}$ was 150 μH. The green in the figure is the reference current coming from the controller while red was the real reference current generated by the predictive law in (2.2a). We see that the control action generated by the installed observer actually brings back the sampled current to the reference current.

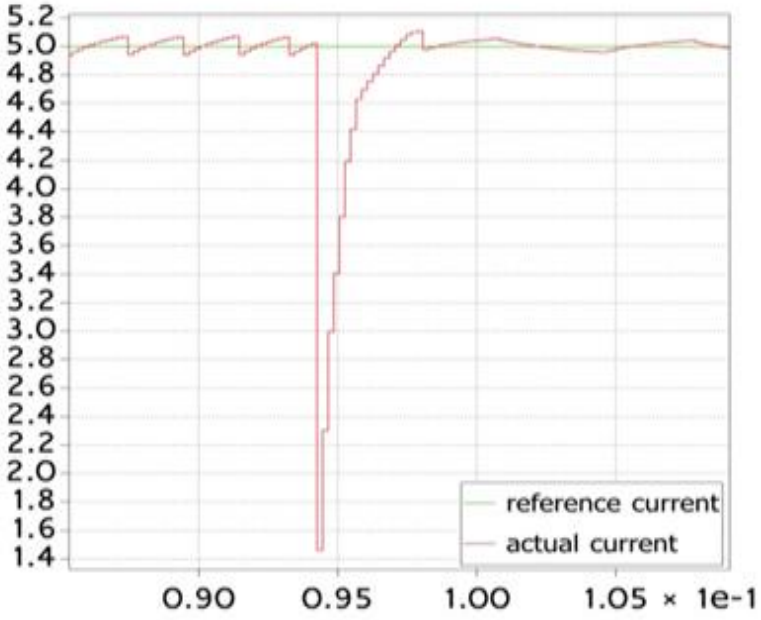


Figure 2.7: Simulation result showing the effect of the observer

2.4.3. Predictive Full Cycle Phase Shift Mode of Control

In this mode the sampled current and the referenced current occur at the same point. The controller samples the current at the mid-point of the half cycle i.e. at $\omega t = \pi/2$ (Fig. 2.8). This sampling mode is adopted since sampling at the beginning ($\omega t = 0$) or middle of the cycle ($\omega t = \pi$) means sampling at a switching instant. The current sensor may pick up the switching noise and that might lead to erroneous control action. Hence the current is sampled and held in the ADC register at the middle of the half cycle or when the up-down counter in the DSP reaches the count value N (Fig. 2.8). There is no switching action at this instant. Interrupt is generated at the instant when the counter reaches N/2 on down count. All the control calculations are done at that point. Once the new phase shift value is calculated from old value and the error,

the new value is loaded phase shift resistor and the effect takes place at the beginning of the next counter period when the counter starts counting up from zero. The next state phase shift angle φ_n+1 can be related to φ_n as per (2.3).

$$\varphi_{n+1} = \varphi_n + \frac{(I^{n+1} - I^n)\omega L}{\Delta V_1 - \Delta V_2}, \qquad where \;\; I^{n+1} = I_{ref} \tag{2.3}$$

The principle advantage of this mode of control is that the sampled current and the reference current occur at the same point in the switching cycle. Hence an additional observer is not required. In case of inductance mismatch the system is convergent.

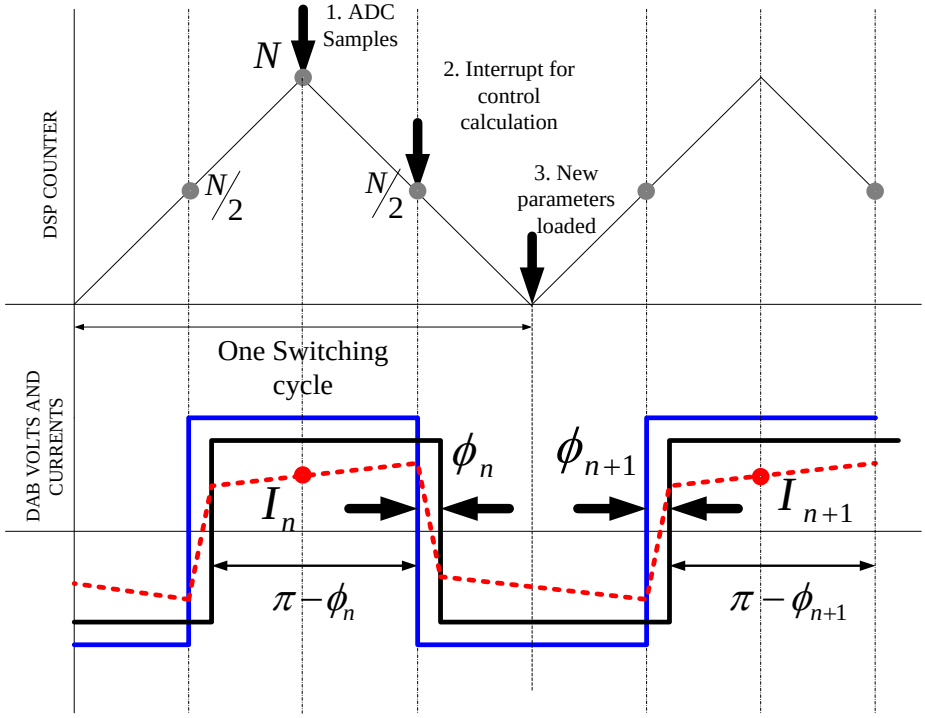


Figure 2.8: The Predictive Full Cycle mode of control implementation diagram

It can be mathematically proven that in the event that there is an error in the leakage inductance measurement and if that error is within a particular bound, the actual current will converge to the reference current within several cycles. The proof is as follows:

$$i_{n+1} = i_n + \frac{\Delta V_2}{\omega L}\frac{\pi}{4} - \frac{\Delta V_1}{\omega L}\varphi_n - \frac{\Delta V_2}{\omega L}(\pi - \varphi_{n+1}) + \frac{\Delta V_1}{\omega L}\varphi_{n+1} + \frac{\Delta V_2}{\omega L}\left(\frac{\pi}{4} - \varphi_{n+1}\right) \tag{2.4}$$

Where $\Delta V_1 = V_{in} + V_{out}$ and $\Delta V_2 = V_{in} - V_{out}$. Substituting 3 in 4 we get:

$$i_{n+1} = I_{ref}\left(\frac{L_{dsp}}{L_{act}}\right) + I_n\left(1 - \frac{L_{dsp}}{L_{act}}\right) = I_{ref}\left(\frac{L}{L+\Delta L}\right) + I_n\left(\frac{\Delta L}{L+\Delta L}\right) \tag{2.5}$$

Here $L_{dsp} = L$ and $L_{act} = L + \Delta L$.

$$\therefore i_{n+2} = I_{ref}\left(\frac{L}{L+\Delta L}\right)\left(1 + \frac{\Delta L}{L+\Delta L}\right) + I_n\left(\frac{\Delta L}{L+\Delta L}\right)^2$$

$$\therefore i_{n+3} = I_{ref}\left(\frac{L}{L+\Delta L}\right)\left[1 + \frac{\Delta L}{L+\Delta L} + \left\{\frac{\Delta L}{L+\Delta L}\right\}^2\right] + I_n\left(\frac{\Delta L}{L+\Delta L}\right)^3$$

$$\therefore \lim_{k\to\infty} i_{n+k} = I$$

$$= I_{ref}\left(\frac{L}{L+\Delta L}\right)\lim_{k\to\infty}\left[1 + \frac{\Delta L}{L+\Delta L} + \cdots\left\{\frac{\Delta L}{L+\Delta L}\right\}^{k-1}\right]$$

$$+ I_n\left(\frac{\Delta L}{L+\Delta L}\right)^k \tag{2.6}$$

$$\therefore I = I_{ref}\left(\frac{L}{L+\Delta L}\right)\frac{1}{1 - \frac{\Delta L}{L+\Delta L}} = I_{ref}, since \lim_{k\to\infty}\left(\frac{\Delta L}{L+\Delta L}\right)^k \approx 0$$

The above proof shows that if the measured value of the inductor L_{dsp} is offset from the actual value of the inductance L_{act} by a margin of ΔL there is convergence in the geometric progression (2.6) as long as $\Delta L \leq L$ and the sampled current will converge to the reference current within several cycles. The simulation result in Fig. 2.9 shows the operation of the controller with gradually increasing ΔL. The L_{act} was 100 μH. In the figure when $\Delta L < L$ the converter is stable and the sampled current tracks the reference current. But when $\Delta L = L$ occurs the current goes out of bound making the system unstable.

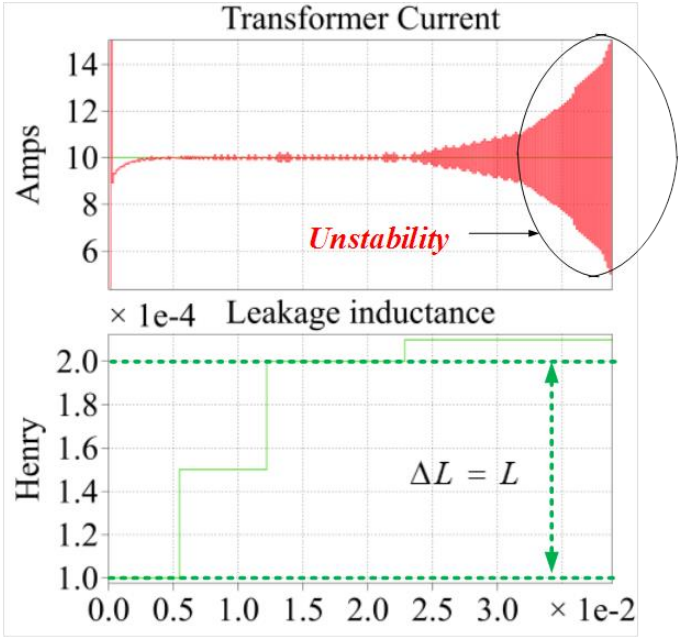


Figure 2.9: Stability loss due to inductor value mismatch

In the next section of the paper an alternate duty cycle mode of switching is shown for the DAB converter. The primary switches are still switched at 50 % duty cycle but the secondary

switches are duty cycle modulated. There are several advantages of that method of modulation. The normal proportional-integral based controller in duty cycle mode is discussed first followed by the predictive duty cycle based control.

2.5. Duty cycle mode of control

A PWM based duty cycle mode of control has already been established to increase the ZVS range under light load conditions. The motivation behind the duty cycle mode of control proposed here is to remove the unwanted DC bias in the high frequency inductor of the DAB that might lead to saturation [17]. The duty cycle mode of control proposes an alternate switching strategy on the secondary side of the DAB converter [41], [42]. The primary side is switched to 50% of the period. The secondary side switches are switched independently using duty cycle modulation. The duty cycle switching strategy is described in Fig. 2.10. Switches (S_6, S_7) and (S_5, S_8) of the secondary bridge are required to be turned on for the period shown in the timing diagram. When the diode is conducting at the beginning of the switching period (S_6 & S_7) are turned on. After the required duty period that switches are forced turned off forcing the diodes (D_5 and D_8) to take over. The gate pulse for the switches (S_6, S_7) is given by the red pulse while that of switches (S_5, S_8) is given by the dotted blue pulse. The duty cycle for the switches is less than one quarter of the entire switching period ($\pi/2$). The switches on the secondary side can be cross switched since (S_6 & S_7) share the same pulse while (S_5 & S_8) share the same pulse. In the dead-time where no switches are turned on the diodes (D_5, D_8) & (D_6, D_7) keep the current flowing. This control is possible since the secondary bridge is lagging in nature. This mode of control makes the duty cycle for the switches (S_6, S_7) and (S_5, S_8)

independent of each other. By changing one duty with respect to the other it is possible to apply positive volts seconds or negative volt seconds across the DAB inductor terminals and force a DC bias in the high frequency AC current. In other words if there is a DC bias already in the current, it is possible to remove it by selecting the duty cycles properly. The control loop shown in Fig. 2.11 has two inner current loops. In one loop the current sampled is $\omega t = 0$ and in another loop it is $\omega t = \pi$. From the timing diagram it is clear that the turn on period of S_6 and S_7 determines the value of I_π. Hence the loop containing I_π produces the duty cycle d_1 that controls the opening and closing of S_6 & S_7. Similarly the loop with I_0 controls the duty cycle for switches S_5 and S_8.

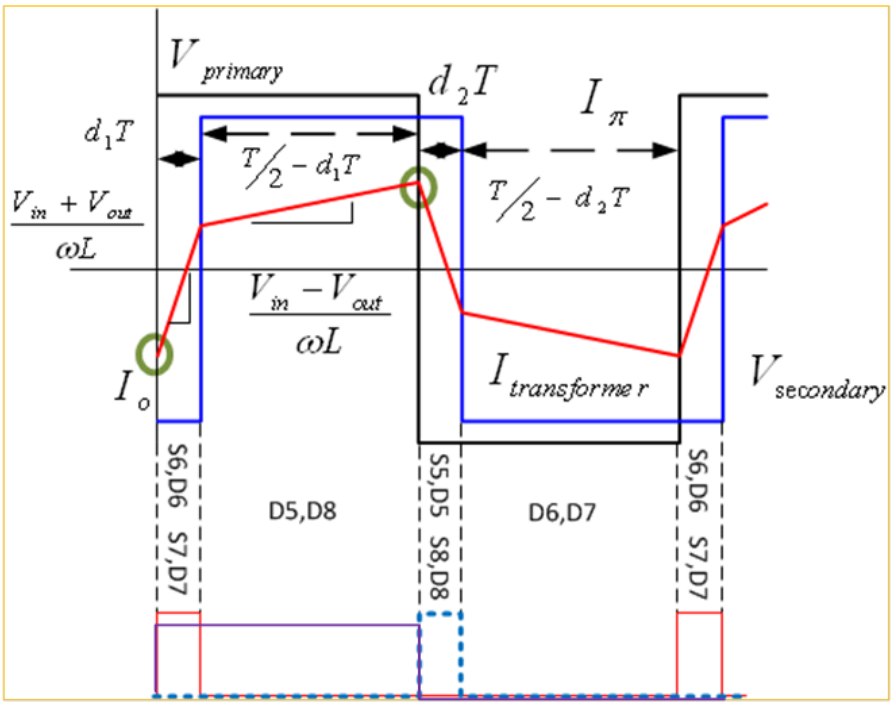


Figure 2.10: The Duty Cycle mode of control with the timing diagram

Since the duty cycle mode of control has two current loops (Fig. 2.11) the controller tries to regulate both the positive current and the negative current separately forcing the current to be AC through the DAB inductor. The advantage over normal 50% switching mode of control as shown in the simulation results of a DAB converter in Fig. 2.12.

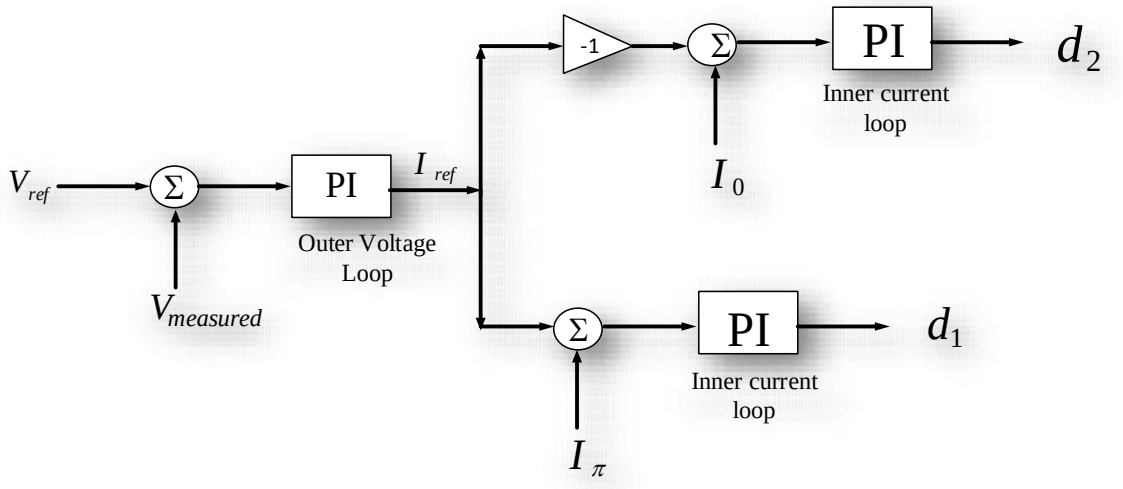


Figure 2.11: The Duty Cycle mode of control block diagram

The plot shows the integral of the high frequency inductor current over time (termed as "charge" or "Q"). When there is a DC bias in the current i.e. unequal volts-seconds has been applied across the inductor terminals, the charge increases or in other words pushes the B-H curve upwards hence pushing the inductor into saturation. When the problem is remedied and the unequal volt seconds removed we see that there is still residual charge in the plot, indicating residual flux in the transformer. Hence to prevent further saturation of the inductor we not only need to remove the dc bias in the volts-seconds but we need to give "reverse" volts-seconds to

remove any residual magnetism in the core. This is not possible with the fixed 50% duty cycle mode of switching. With the duty cycle mode of switching this is possible by adding negative volts seconds across the inductor (Fig. 2.14) with the different combination of the duty cycles. However in-case there is an isolation transformer, this method fails to remove DC bias in the transformer core flux. Further discussion of this problem is presented in the following section.

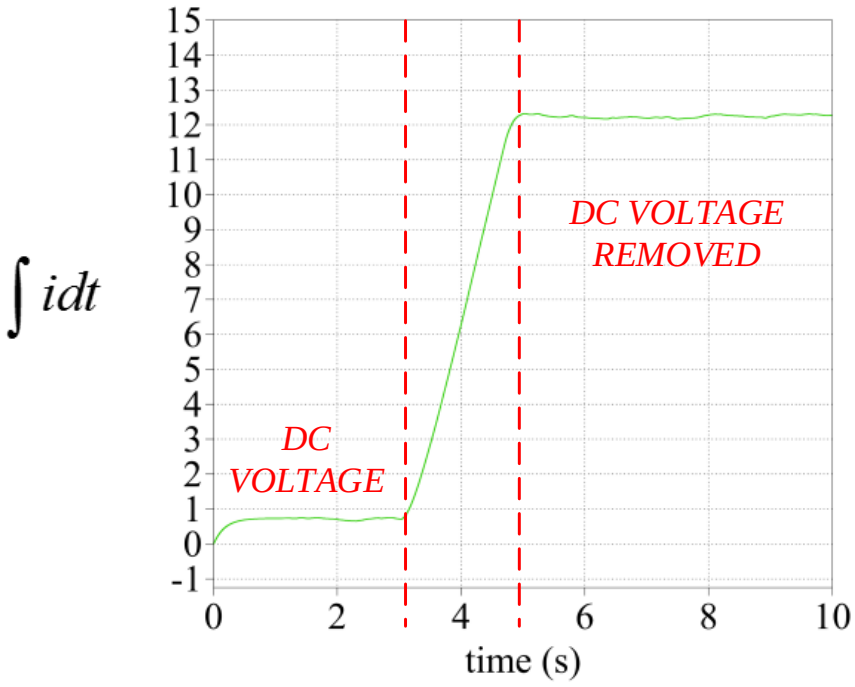


Figure 2.12: Q vs Time Plot with traditional phase shift mode of control

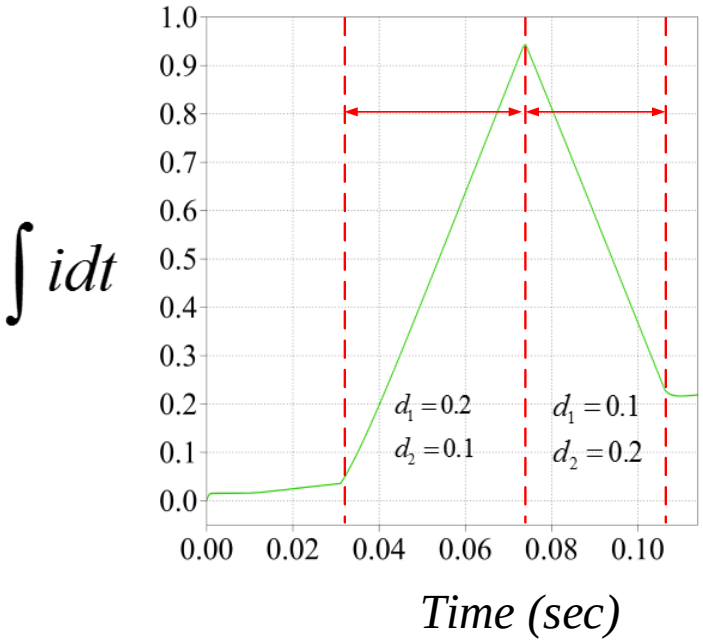


Figure 2.13: Q vs Time Plot with duty cycle mode of control

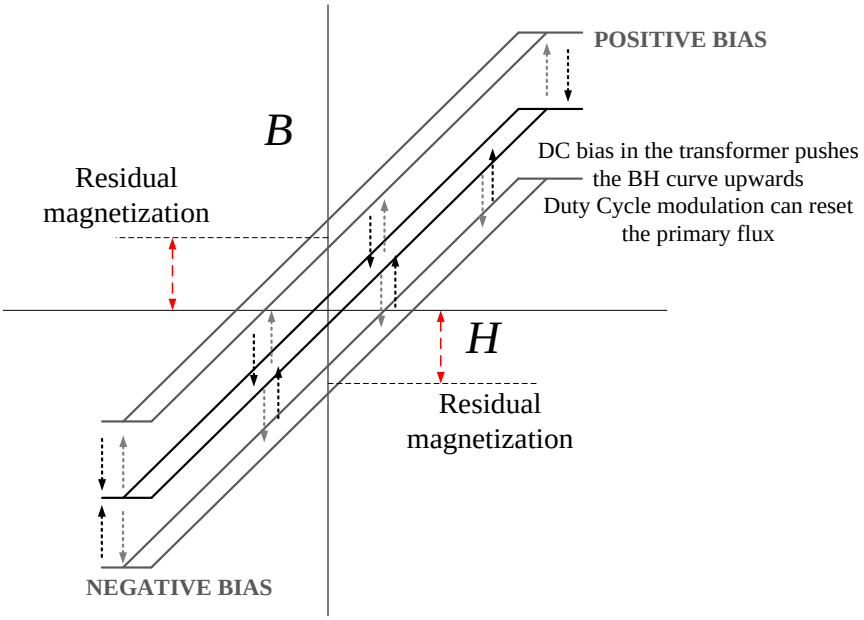


Figure 2.14: Duty cycle control resetting the B-H curve of the Inductor

2.6. Contribution of magnetizing current in the HF DAB transformer

In the previous section the duty cycle mode of control was proposed which eliminates the DC bias in the high frequency load current. However the DC bias in the magnetizing current was not analyzed. Since dc bias in the magnetizing current and not the load current is responsible for saturating the high frequency DAB transformer it is important to analyze which bridge provides the magnetizing current to the transformer. This can be proved by analyzing the T-model of the high frequency transformer (Fig. 2.15). It can be assumed without any loss of generality that the primary side of the transformer has leakage *kL* and the secondary side (*1-k)L*. The magnetizing inductance is L_m. Superposition principle is used to calculate the magnetizing current. Considering the primary voltage V_{prim} the magnetizing current contributed by the primary bridge I_m^{prim} is given by (2.7)

$$I_m^{prim} = \left[\frac{V_{prim}}{kL + \frac{(1-k)LL_m}{(1-k)L + L_m}}\right]\frac{(1-k)L}{[(1-k)L + L_m]}$$

$$= \frac{V_{prim}(1-k)L}{kL[(1-k)L + L_m] + (1-k)LL_m} \qquad (2.7)$$

with $= 1 \xrightarrow{yields} I_m^{prim} = 0$. Thus from (2.7) we see that if the entire leakage is on the primary side the secondary is the one supplying the magnetizing current and vice versa. The cause of the DC bias in the DAB transformer has been analyzed in [17]. Since the primary switches are switched at 50 % duty cycle semiconductor non-idealities may have a large contribution to the DC flux in the transformer. The secondary side on the other hand is duty cycle modulated.

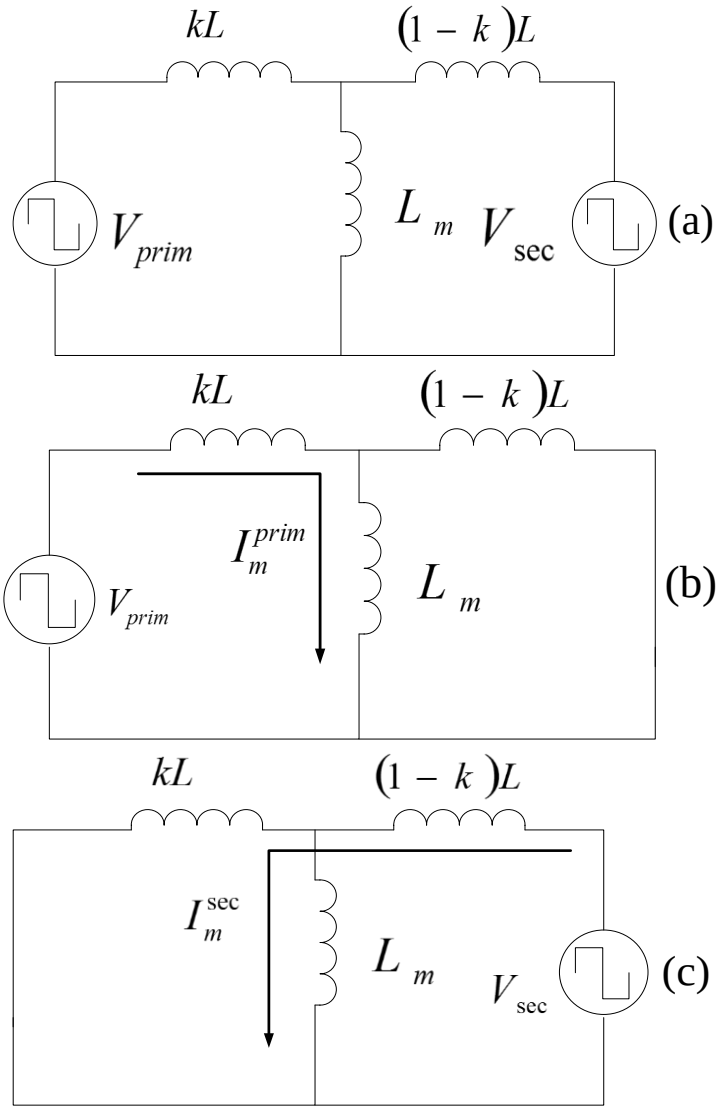


Figure 2.15: The T-model of the high frequency transformer with the distributed leakage between the primary and the secondary

Hence any DC bias can be removed using controlled switching of the secondary switches. In the following section several operating modes are shown based on the distribution of the

leakage inductance of the transformer and how each bridge contributes to the magnetizing flux and what can be the possible control strategy to maintain the flux to be AC.

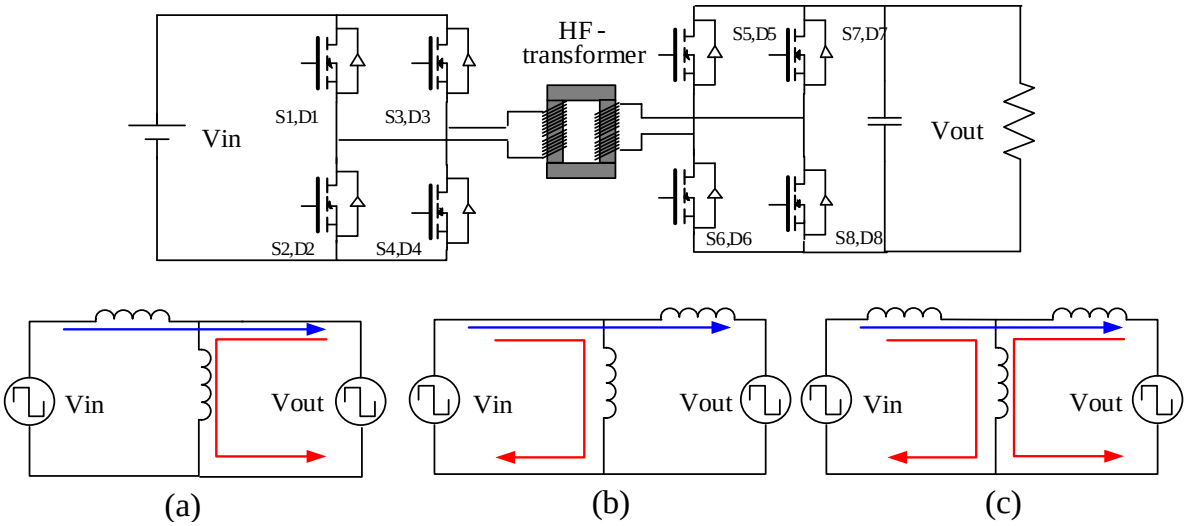


Figure 2.16: Equivalent circuit of the High frequency DAB transformer

2.6.1. Case 1: Entire Leakage is on primary side

The isolated DAB converter in Fig. 2.16 is considered as an example. In Fig. 2.16a the entire leakage is on the primary side of the transformer. Hence the secondary side is supplying the magnetizing current (I_m shown in red). The load current I_{load} is shown in blue. Since the secondary side is duty cycle modulated, both the magnetizing and the load current are functions of the duty cycles d_1 and d_2. The secondary side can monitor the flux level in the transformer core and adjust d_1 and d_2 so that there is no dc bias in the flux. The load current might have DC offset generated by unequal volt-seconds from the primary that might saturate the inductor.

The duty cycles cannot be adjusted to compensate for this as it might inject DC flux in the transformer. Thus this configuration of leakage inductance is not a good design to eliminate DC bias. Implementing such a transformer is possible with coaxial wound transformer (CWT) [18], [19], [20]. The CWT has the structural advantage that gives a control over the leakage inductance of the transformer. Hence by designing the CWT as such we can precisely place the leakage inductance of the transformer on the primary or on the secondary side.

2.6.2. Case 2: Entire Leakage is on secondary side

In the case that the entire leakage is on the secondary side (Fig. 2.16b) the load current is still a function of the duty cycles but the magnetizing current is not. The magnetizing flux is supplied by the primary bridge. Hence any unequal volt-seconds generated by the primary bridge due to non-idealities in switching [17] will lead to a DC flux in the transformer. The duty cycle modulation on the secondary will have no effect on the transformer flux. However, it can still be implemented to prevent saturation in the secondary side leakage inductance. The transformer bias can be eliminated by adding a positive or a negative bias in the primary switching. The inductor bias can be eliminated separately by the duty cycle modulation.

2.6.3. Case 3: Distributed Leakage

In the case of distributed leakage (Fig. 2.16c), both the primary and the secondary side has leakage inductance, and both the sides contribute to the magnetizing current. Hence non idealities in both the primary and the secondary bridge contribute to the DC bias in the transformer flux. Under such conditions the duty cycle modulation proposed earlier in the

secondary bridge will be unable to remove the DC flux in the transformer core. To remove the DC flux an analog based controller is proposed (Fig. 2.17). Fig. 2.17 shows the controller for flux control in the transformer core. It is assumed the primary is fixed at 50 % duty-cycle. The secondary had a steady state duty cycle of 50 % onto which the controller adds Δd_{sec}. It is assumed that the primary and the secondary switching non-idealities add together to produce the unequal volt-seconds in the transformer core. The controller samples the primary current and the secondary current and takes a difference which gives the magnetizing current I_m. Under ideal condition I_m is AC or in other words the integral over one cycle (Q_{cycle}) will be zero. However if either the primary or the secondary bridge generates unequal volts-seconds then DC offset will appear. The controller compensates by comparing the Q_{charge} to 0 by producing an additional Δd_{sec} to nullify the effect. As a result (Fig. 2.19) the dc component from the magnetizing current is channeled out to the load current which now contains the AC and the DC component. Fig. 2.18 shows the simulation result for such a system. The simulation shows the dc offset being removed from the magnetizing current but appearing on the load current. Based on the amount of dc offset that is present in the load current the inductor may saturate or operate at higher loss if there is air-gap to support DC flux. This is not desirable and a solution is proposed in the following section.

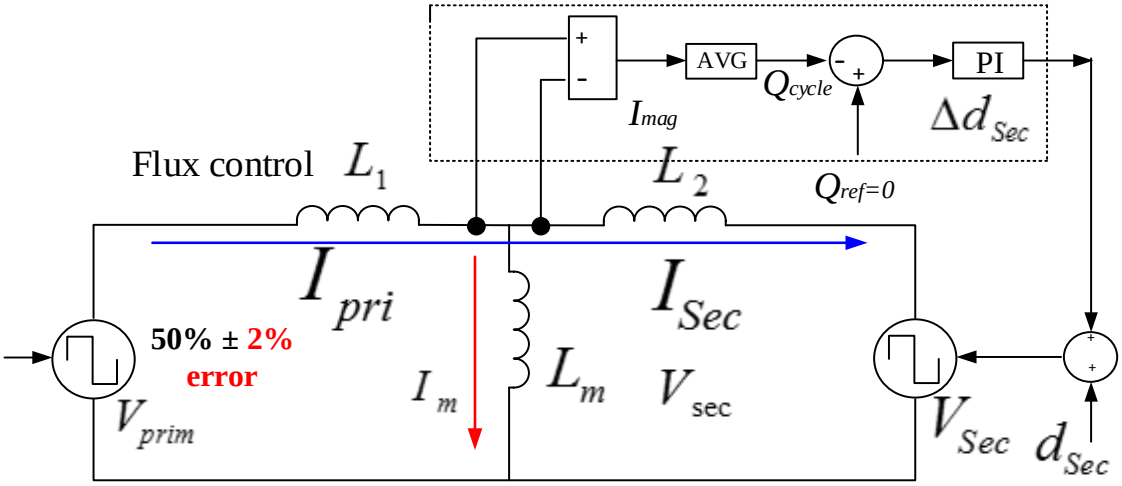


Figure 2.17: Controller for transformer flux DC level control in case of distributed leakage

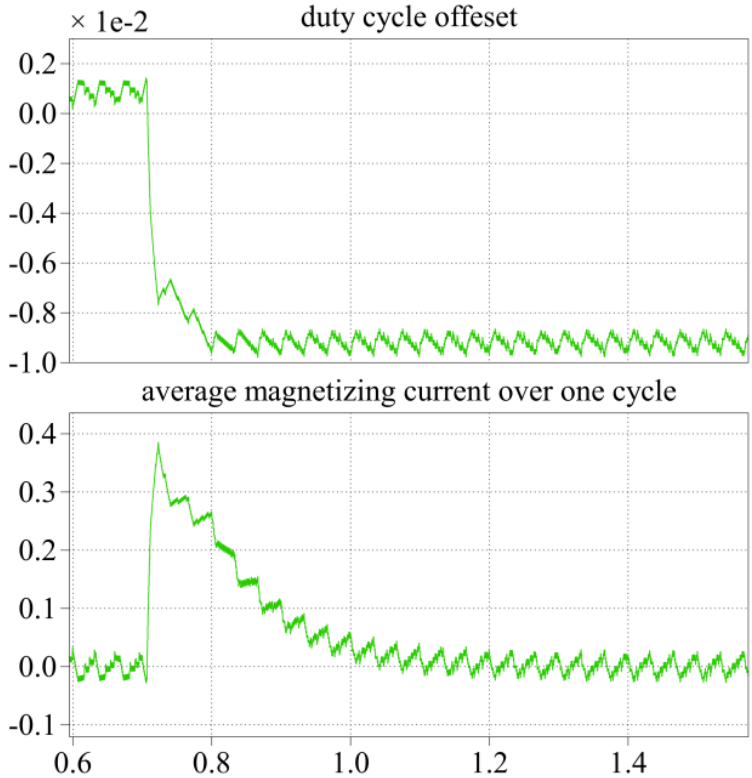


Figure 2.18: Simulation results for the flux removal algorithm showing the magnetizing current averaged over one cycle.

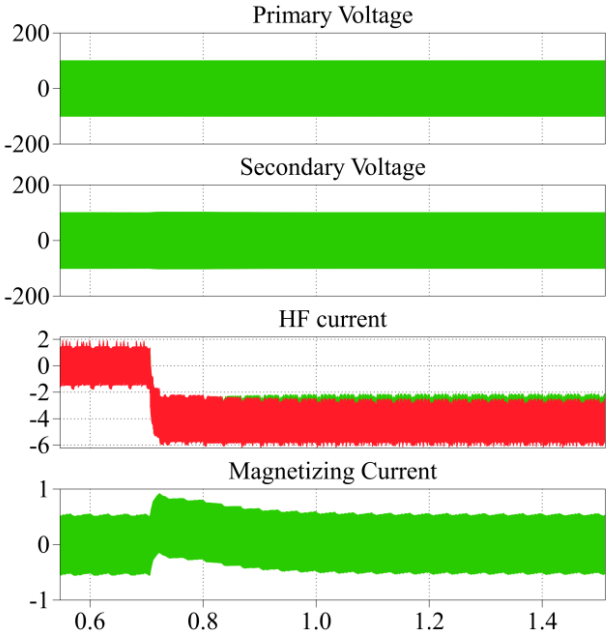


Figure 2.19: Simulation results for the DC flux removal algorithm

2.6.4. Case 4: Duty Cycle mode of control with Flux control

In order to prevent DC bias in the load current that might saturate the DAB inductor a duty based control is to be implemented on the secondary side. The assumption is that the leakage inductance has to be on the secondary side. Hence the primary supplies the transformer flux and the secondary controls the inductor flux (Fig. 2.20). The transformer flux is controlled by adjusting the DC bias in the primary bridge. If the leakage inductance is on the secondary side the primary bridge will provide the magnetizing current and control the transformer flux. Using both these control mode taken together it is possible to completely remove any DC bias either in the magnetizing current or the load current.

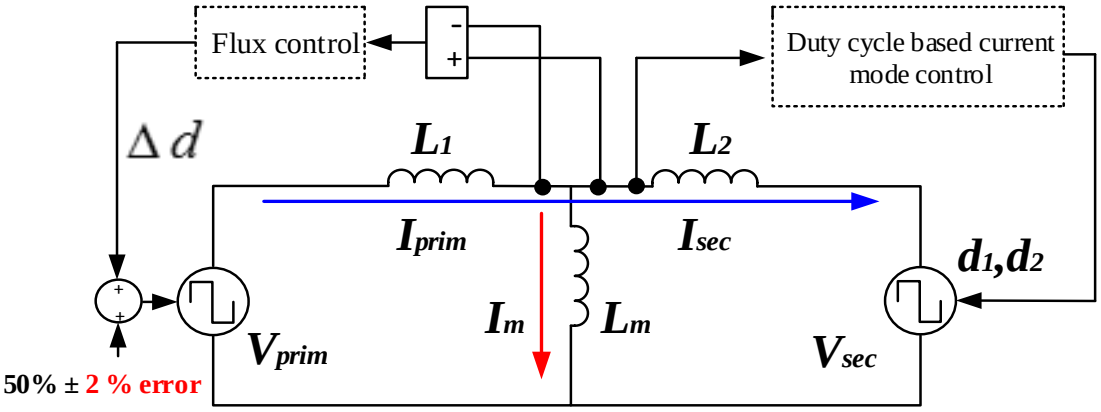


Figure 2.20: Controller for complete DC flux removal

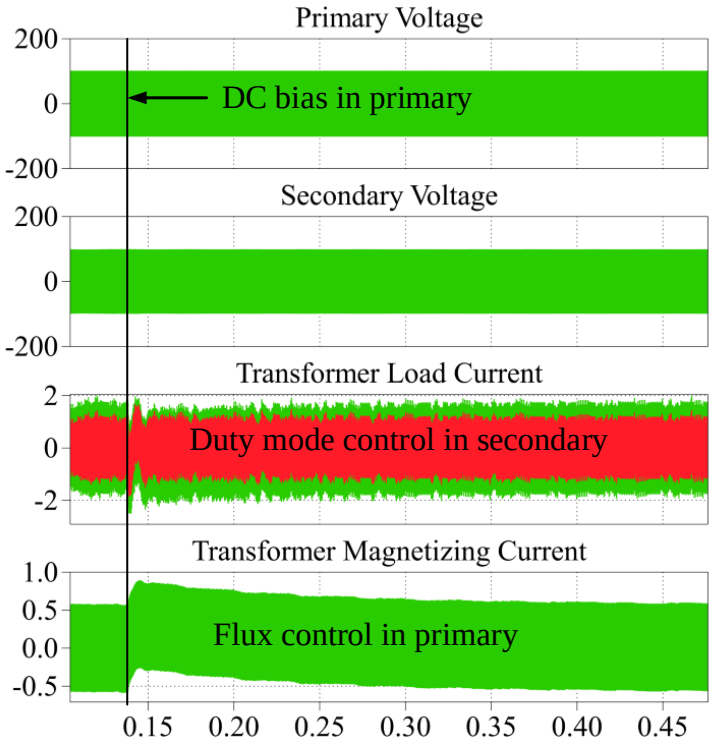


Figure 2.21: Simulation results for complete DC flux removal algorithm

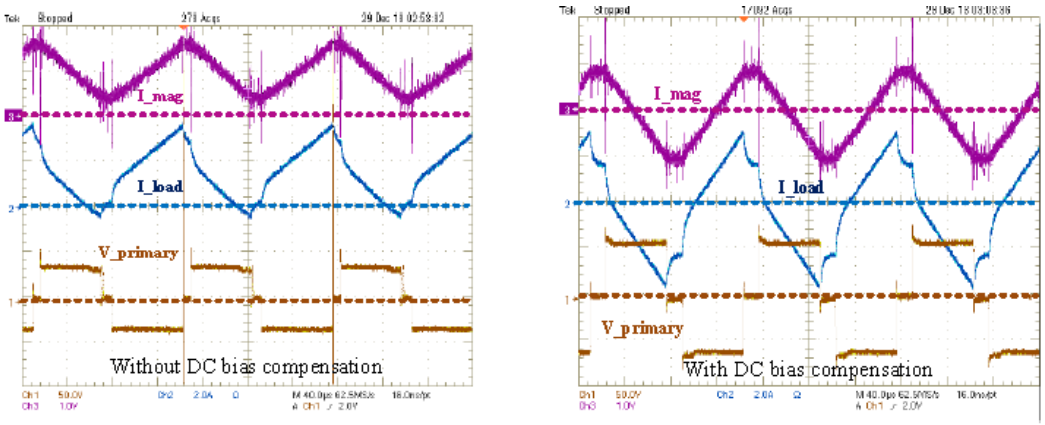


Figure 2.22: Experimental results for DC flux removal algorithm

Fig. 2.22 shows the experimental results for the proposed controller. The current sensors used for the purpose of measuring the high frequency DAB current are LEM sensors that output a current signal that is first converted to a voltage signal by a loading resistor and then sent to the ADC. By arranging the loading it is possible to isolate the magnetizing current and convert it into voltage and provide it to the ACD for DC bias measurement. Fig. 2.22 shows the experimental result of such an effort where the magnetizing current has been extracted from the primary and the secondary current difference and the DC bias has been calculated and compensation has been provided.

2.7. Predictive duty cycle mode of control

The efficacy of the duty cycle mode of control in removing the DC bias in the DAB inductor has been shown in the previous section (Section 2.6.4). This provides the motivation for developing a predictive algorithm for the duty cycle mode of control. Based on the control strategy the duty cycle mode of control can be further classified in the following categories:

1) Half Cycle mode of control

2) Full cycle mode of control

3) Full Cycle equal area mode of control

2.8. Half cycle mode of control

In this mode of operation the sampling is done at two instances in the switching cycle, at $\omega t = 0$ and at $\omega t = \pi$. The current sampled at $\omega t = 0$ refers the current at $\omega t = \pi$ as the reference and the current sampled at $\omega t = \pi$ refers the current sampled at $\omega t = 0$ of the next cycle as the reference (Fig. 2.23). The equations driving the controller are given in (2.8a) and (2.8b).

$$I_{ref}^{\pi} = I_0 + m_1 d_1 T_s + m_2 \left(\frac{T_s}{2} - d_1 T_s\right) \quad (2.8a)$$

$$I_{ref}^{0} = I_\pi + m_1 d_2 T_s + m_2 \left(\frac{T_s}{2} - d_2 T_s\right) \quad (2.8b)$$

Where $m_1 = \frac{V_{in}+V_{out}}{L}$, $m_2 = \frac{V_{in}-V_{out}}{L}$. This control is a deadbeat control as the response takes place within one cycle. Since the positive reference is same as the negative reference in magnitude, this makes sure that the current through the transformer is AC. Any DC component is removed by changing the duty cycles (d_1 & d_2) accordingly. Fig. 2.24 shows the simulation results of the transient response of the duty cycle modulated control. The reference current is changed from -10 amps to - 5 amps at $\omega t = 0$ and from 10 to 5 amps at $\omega t = \pi$. It can be seen from the simulation result that the sampled current changes the value within one switching cycle (Fig. 2.24 green and red).

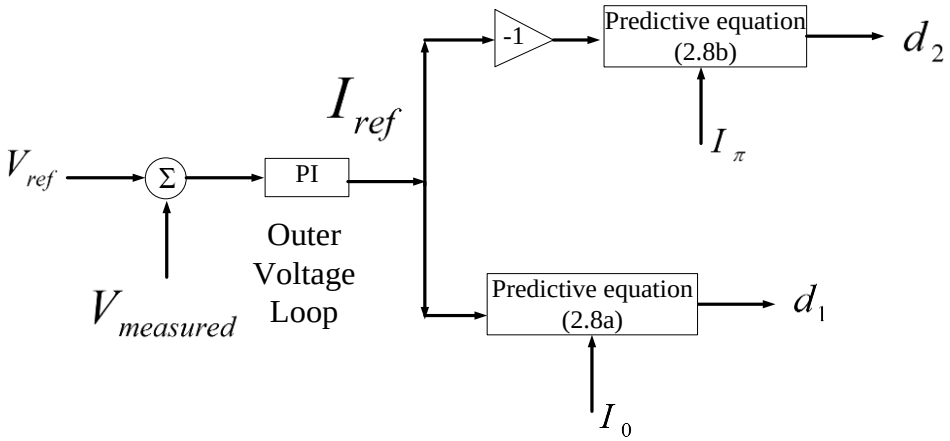


Figure 2.23: Controller diagram for the half cycle duty cycle mode of control

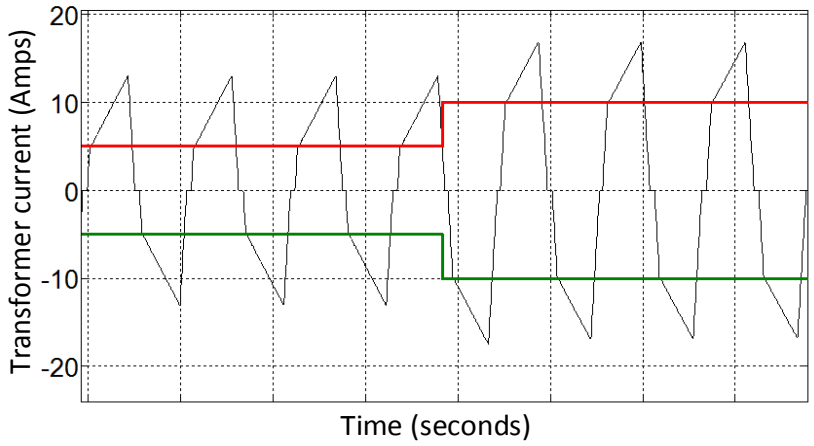


Figure 2.24: Transient response of the half cycle duty cycle mode of control

2.9. Full cycle duty cycle mode of control

The full cycle duty cycle mode of control is different from the half cycle duty cycle mode of control in the sense that the sampled current in one cycle is the reference current for the previous cycle. The timing diagram for the full cycle mode of control is shown in Fig 2.25.

Two different timing modes are discussed here. One with the sampling done at the beginning of the switching cycle (Fig 2.25) is using a down counter and another with sampling done at the middle of a half cycle using an up-down counter (Fig 2.26). The advantage of using the up-down counter is that the ADC can sample at the mid-point of the up count i.e. at count = N/2. This mode is preferred, since that the current sampled will be free of switching transients compared to the down counter used in Fig 2.25. Two up-down counters represented by the two triangles offset by 180° (black or counter 1 and dotted blue or counter 2) are required in this case as two currents are sampled, one in the positive half cycle and another in the negative half cycle. The ADC samples when the counter is at $^{N}/_{2}$ at up-count of the black counter or counter 1. The sampled value is the current from the positive half cycle I_n^1. Interrupt generated at counter 1 = N does one set of the control calculations (2.9a). In the control calculations the assumption is that the current in the next cycle i.e. I_{n+1}^1 will reach the desired reference value generated by the outer voltage loop. The computed value is d_{n+1}^1 and is loaded to the compare register of the counter 2. This generates the duty cycle for the counter 2 (the blue pulse in Fig. 2.26). Similar set of events take place with counter 2 one half-cycle earlier or later. The negative current I_{n-1}^2 is sampled at up count of the counter 2. Interrupt is generated and the control calculations take place at counter 2 = N and d_n^2 is calculated (2.9b) which is loaded on the compare register of counter 1 and generates the pulse shown in black (Fig. 2.26). The control calculations for the full cycle duty cycle mode are as follows

$$I_{n+1[ref]}^1 = I_n^1 + m_2 \frac{T_s}{4} - m_1 d_n^2 T_s - m_2 \left(\frac{T_s}{2} - d_n^2 T_s\right) + d_{n+1}^1 T_s + m_2 \left(\frac{T_s}{4} - d_{n+1}^1 T_s\right) \quad (2.9a)$$

$$I^2_{n[ref]} = I^2_{n-1} - m_2\frac{T_s}{4} + m_1 d^1_n T_s + m_2\left(\frac{T_s}{2} - d^1_n T_s\right) - d^2_n T_s - m_2\left(\frac{T_s}{4} - d^2_n T_s\right) \quad (2.9b)$$

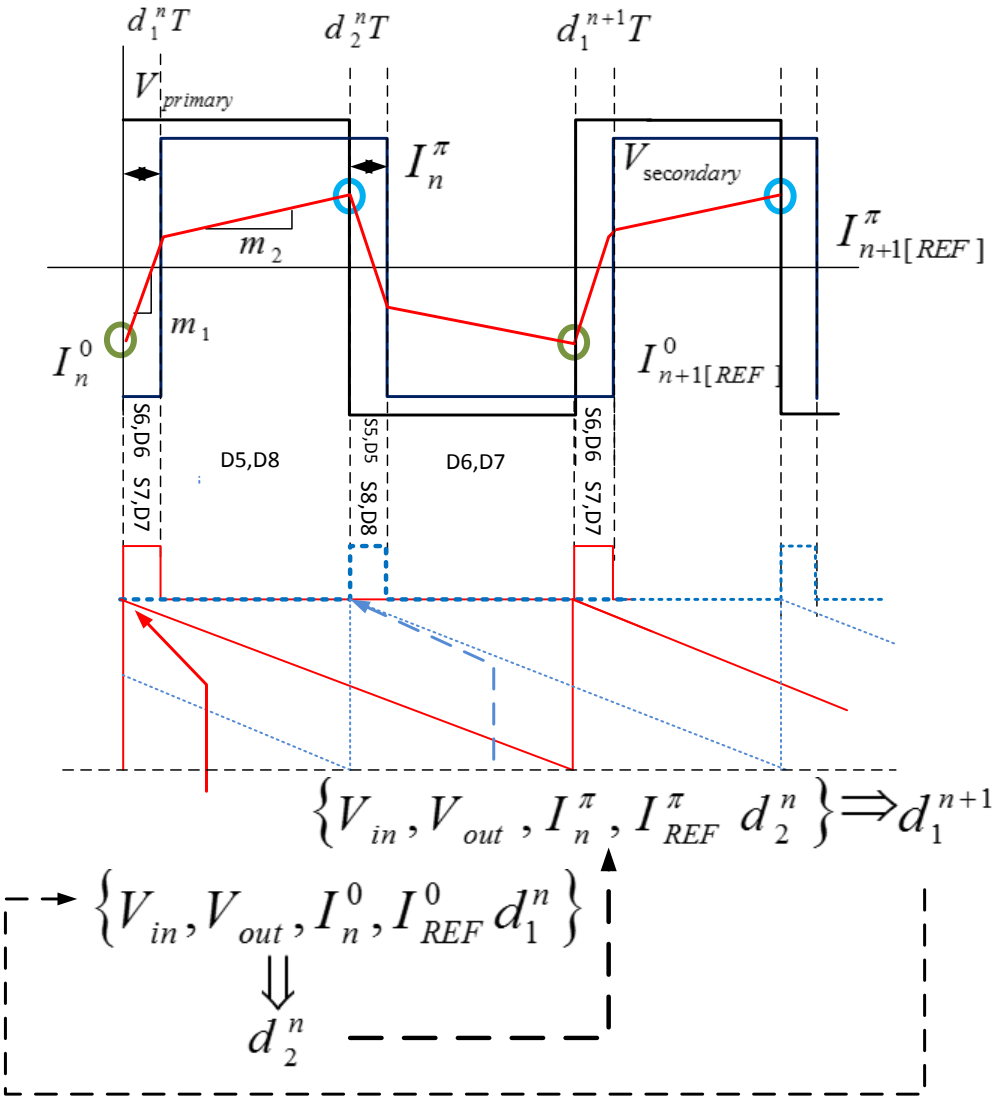


Figure 2.25: Timing diagram for the full cycle duty cycle mode of control using down counters

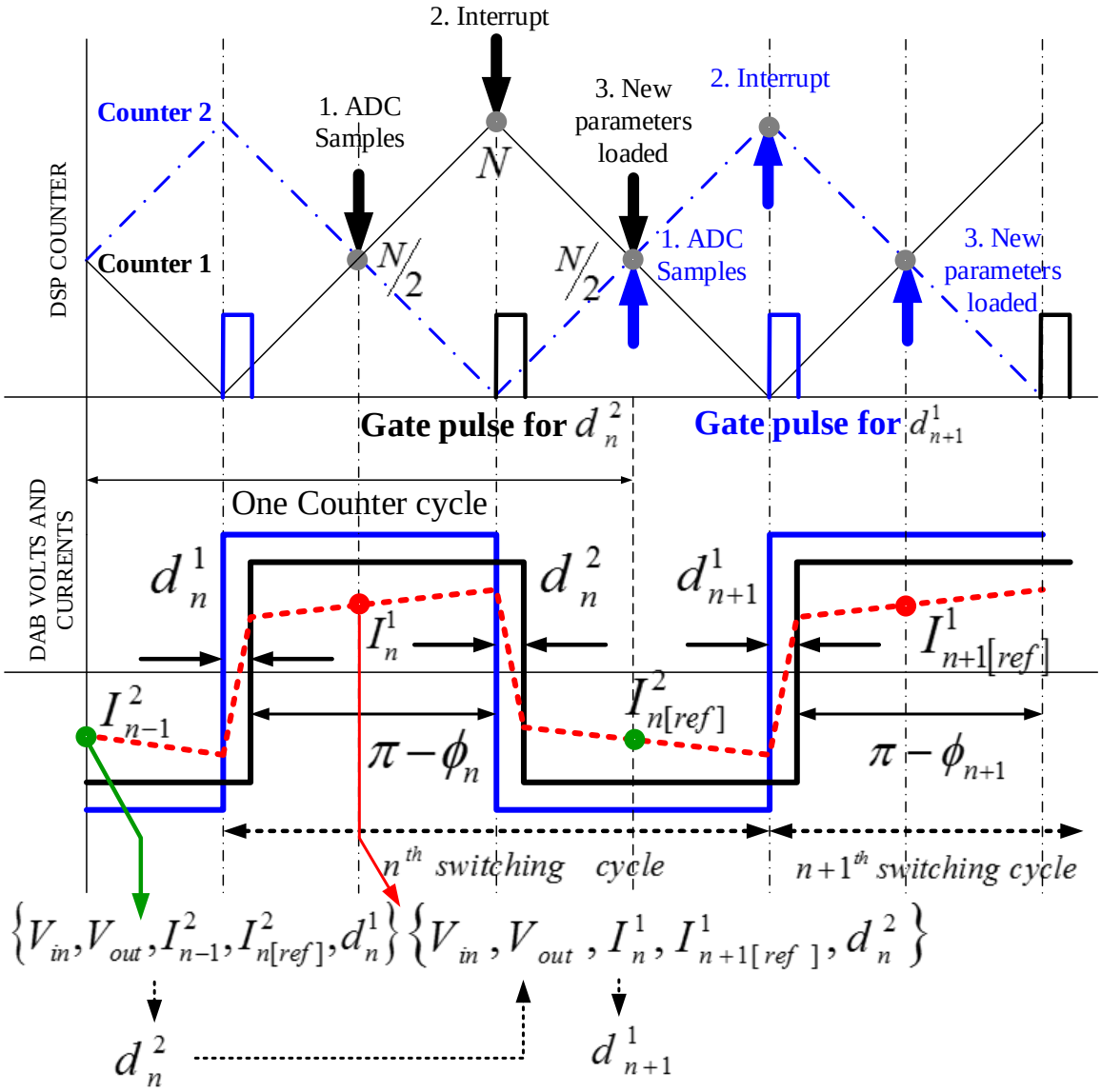


Figure 2.26: Timing diagram for the full cycle duty cycle mode of control using up-down counters

Both the equations in (2.9a) and (2.9b) are cross coupled i.e. the solution for the n+1 step in equation in (2.9a) is dependent on the value of the n step solution of equation in (2.9b) and so on. Hence this is not a dead beat method and the system converges after several cycles. Fig.

2.27 shows the simulation result of the full cycle duty cycle mode of control. The transformer current is given a DC bias by switching off one of the devices in the primary of the DAB. The device is then turned on and it can be seen from the simulation result in Fig. 2.27 that the DC bias is removed within one switching cycle of the converter. Although this method is computationally simple, the current needs to be sampled twice in every switching cycle and with high frequency that may be difficult. Hence an alternate method is proposed where the current is sampled just once in the switching cycle and still the current is forced to be AC. The method is equal area method and is proposed in the following section.

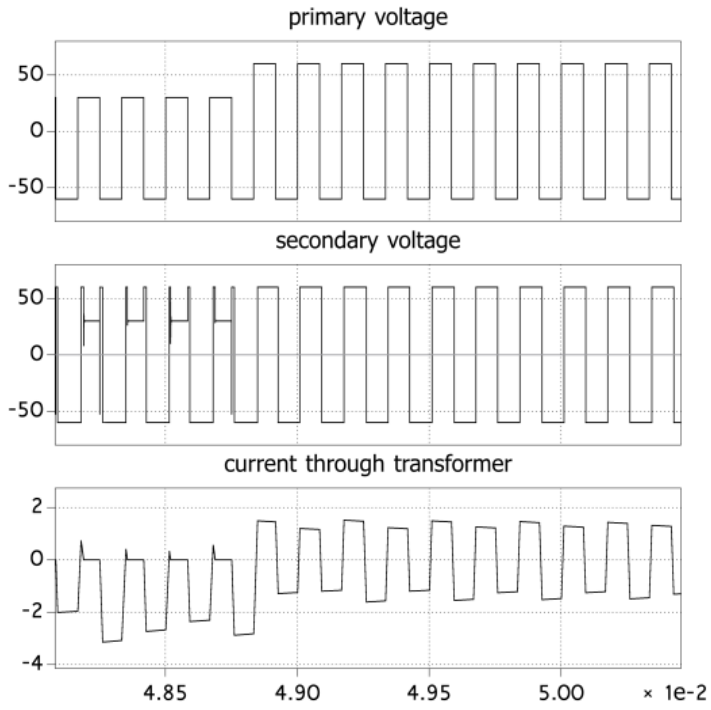


Figure 2.27: Simulation result for the full cycle duty cycle mode of control

2.10. Equal area mode of control

The equal area mode of control is an extension of the duty cycle mode of control. The idea is to sample the current at the start of the switching cycle and make it to follow a reference current that comes from the voltage PI controller. Considering the n[th] switching cycle and the (n+1)[th] cycle, we can get the following equation for the current:

$$i_{n+1} = i_n + \frac{V_{in} + V_{out}}{L} d_1 T_s + \frac{V_{in} - V_{out}}{L}\left(\frac{T_s}{2} - d_1 T_s\right) - \frac{V_{in} + V_{out}}{L} d_2 T_s$$
$$- \frac{V_{in} - V_{out}}{L}\left(\frac{T_s}{2} - d_2 T_s\right) \qquad (2.10)$$

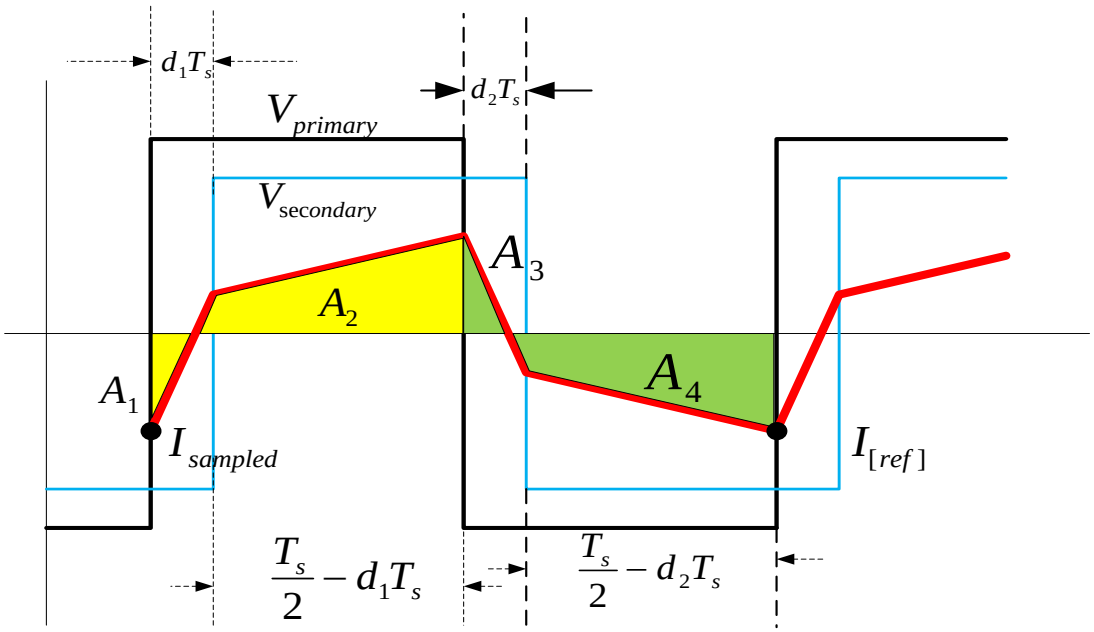


Figure 2.28: Equal area mode of control

Assuming that in one cycle the corrective action is achieved and the above equation simplifies as shown in (2.11)

$$\left(I_{ref} - I_n\right)\frac{L}{2V_{out}T_s} = d_1 - d_2 \tag{2.11}$$

This is not enough to calculate the value of the duty cycles since there are two unknowns and one equation (2.11). This can be used to make the current through the transformer a perfect AC i.e. remove any DC offset in it. That can be done by equating the area under the curve of current in the positive half cycle (Fig. 2.28) $(A_1 + A_2)$ to that of the negative half cycle $(A_3 + A_4)$ i.e.

$$A_1 + A_2 = A_3 + A_4 \tag{2.12}$$

Here $(A_1 + A_2)$ is a function of d_1 and $(A_3 + A_4)$ is a function of d_2. So from equations in (2.11) & (2.12) we get the solutions for d_1 and d_2 as in (2.13).

$$d_1 = \frac{\left(-I_n^2L^2 + 2I_nI_{ref}L^2 - I_{ref}^2L^2 - 2I_nLT_sV_{out}\right)}{4TV_{out}\left(I_nL - I_{ref}L + T_sV_{out}\right)} - \frac{\left(2I_{ref}LT_sV_{out} - T_s^2V_{in}V_{out} + T_s^2V_{out}^2\right)}{4TV_{out}\left(I_nL - I_{ref}L + T_sV_{out}\right)}$$

$$d_2 = \frac{\left(I_n^2L^2 - 2I_nI_{ref}L^2 + I_{ref}^2L^2 - 4I_{ref}LT_sV_{out}\right)}{4TV_{out}\left(I_nL - I_{ref}L + T_sV_{out}\right)} - \frac{\left(-T_s^2V_{in}V_{out} + T_s^2V_{out}^2\right)}{4TV_{out}\left(I_nL - I_{ref}L + T_sV_{out}\right)} \tag{2.13}$$

The duty cycle values are loaded in the corresponding counters and the gate pulses are generated. Fig. 2.29 shows the transient response for the equal area mode of control. The current through the transformer in the DAB was intentionally given a DC bias by turning off one of the switches on the primary side. The switch was then turned on and the predictive

controller is able to remove the dc bias in once cycle. The same exercise was done with a simple voltage based control and it is seen that it takes much more time for the controller to fully remove the DC bias in the current.

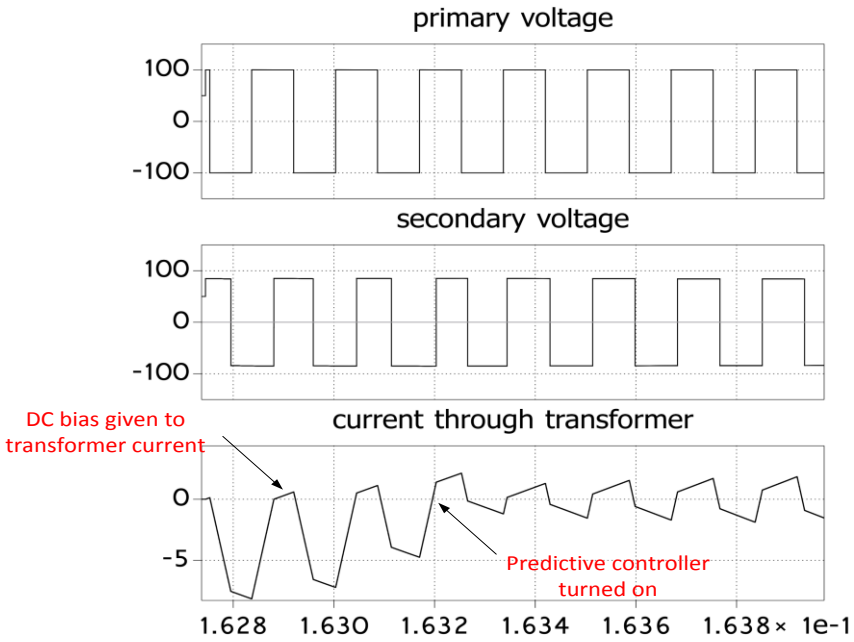


Figure 2.29: Transient response of the equal area mode of control

The Fig. 2.28 shows the equal area mode of control with instant update. However the controlling point may be two cycles down the line of the sampling point as shown in Fig. 2.29 with $A_1 + A_2 + A_5 + A_6 = A_4 + A_3 + A_7 + A_8$

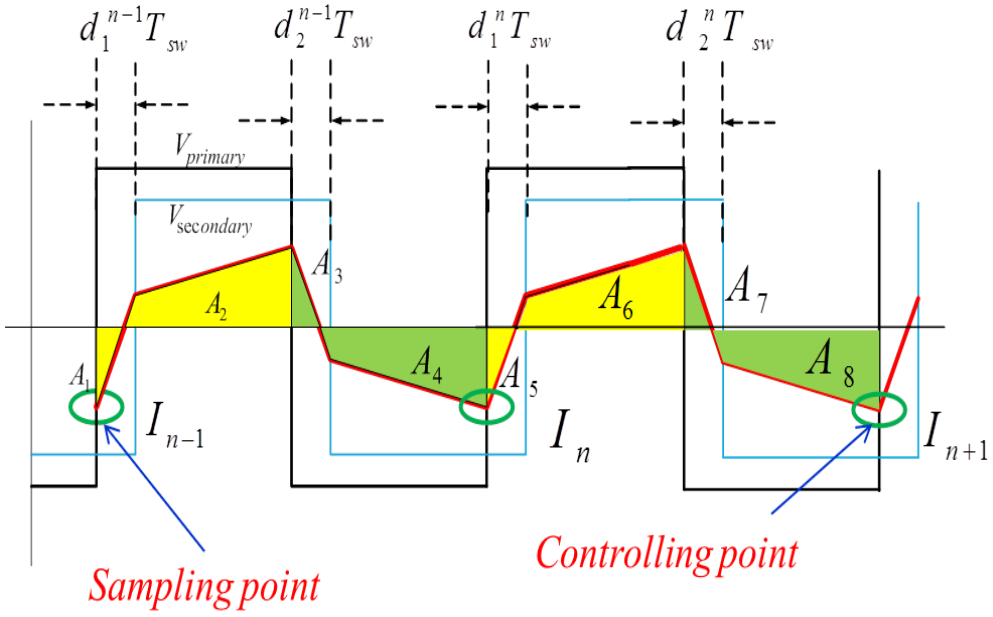


Figure 2.30: Equal area mode of control with control point two cycles down the line

2.11. Power mode of predictive control

So far the predictive controller regulates a particular current peak point within a cycle. But in case where there is power sharing required between parallel connected DAB converters (Fig. 2.31), this mode of control is not suffice. Here power balancing requirement is critical if the converters input stage is series connected to block higher DC bus voltage. The previously discussed methods will force the peak point currents to a referenced value. If the referenced value is at $\omega t = \varphi$ where φ is the phase shift, then the expression of the current at that point is given as (2.14).

$$I_{\varphi} = \frac{V_{in}}{\omega L}\left[\frac{V_{out}}{V_{in}}\varphi + \frac{\pi}{2}\left(1 - \frac{V_{out}}{V_{in}}\right)\right] \tag{2.14}$$

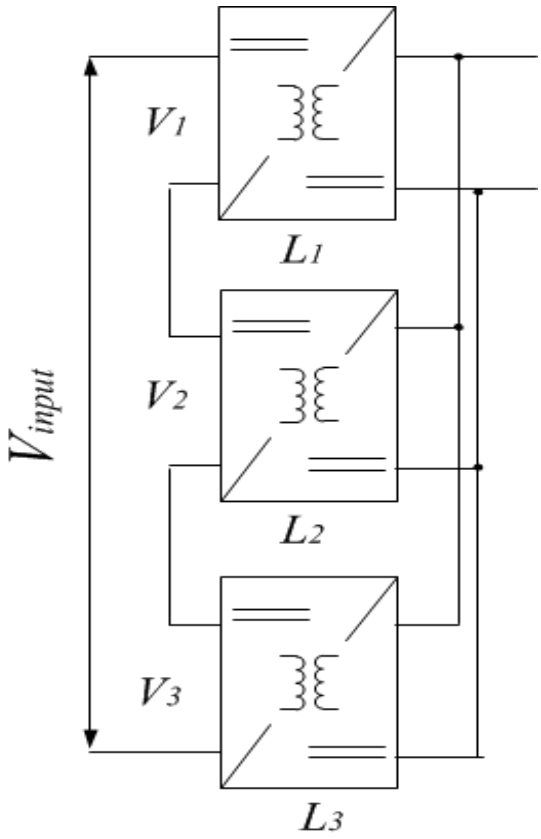


Figure 2.31: Power Balance in series input parallel output DAB stages

Considering multiple DAB connected with series input, parallel output mode with different leakage inductances (L_1,L_2 ...), the predictive controller with the current reference tracking, will force the individual DAB to work at different phase shift angles $(\varphi_1, \varphi_2, \dots)$ where according to (2.15),

$$\varphi_1/_{L_1} = \varphi_2/_{L_2} = \cdots \text{ (Assuming } V_{in} = V_{out}) \tag{2.15}$$

But the power transfer equation for the DAB is given as (2.16).

$$P_{transferred} = \frac{V_{in}V_{out}}{\omega L}\varphi\left(1 - \frac{\varphi}{\pi}\right) \tag{2.16}$$

Hence for power balance in parallel connected DAB the relationship between the phase shift angle and the leakage inductance turns out as (2.17)

$$\frac{\varphi_1}{L_1}\left(1-\frac{\varphi_1}{L_1}\right)=\frac{\varphi_2}{L_2}\left(1-\frac{\varphi_2}{L_2}\right)=\cdots \tag{2.17}$$

Since the relationship mentioned in 2.15 ≠ 2.17 therefore the control modes discussed above is not suffice for power mode control. For that a different approach has to be taken that is somewhat similar to the area mode control discussed in the previous section. Fig. 2.33 shows the controller block diagram.

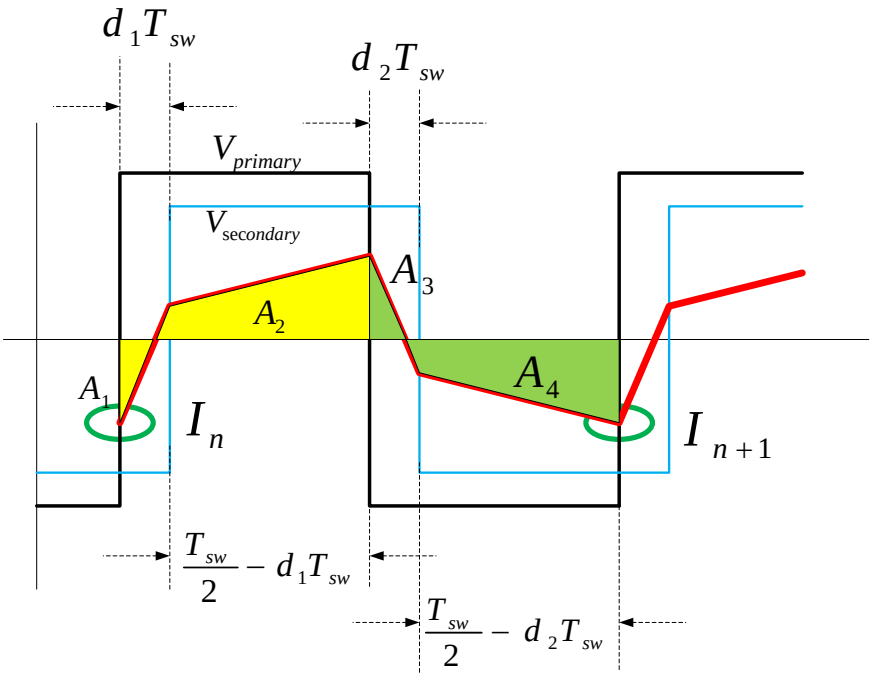


Figure 2.32: Power mode of predictive control

The current is sampled at $\omega t = 0$. An external voltage loop provides the power reference (Fig 2.33). With the generated P_{ref} and the I_0 from the sampled current the controller calculates the required phase shift angle to produce the required power by calculating the area under the curve in the positive half cycle (yellow shaded portion in Fig. 2.32).

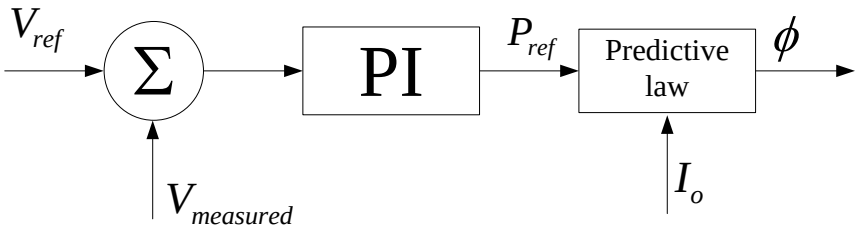


Figure 2.33: Controller block diagram for the power mode of predictive control

The phase shift angle calculated from the power mode control is given as (2.18).

$$\varphi = \pi - \sqrt{\pi}\sqrt{\frac{\pi V_{in}\Delta V_1 - 2\omega L P_{ref} + 2I_0\omega L V_{in}}{V_{in}(\Delta V_1 - \Delta V_2)}} \tag{2.18}$$

Where $\Delta V_1 = V_{in} + V_{out}$ and $\Delta V_2 = V_{out} - V_{in}$. This shows the relation of the phase angle with power is quadratic in nature as the way it should be from (2.16).

2.12. Experimental verification of predictive control

This section of the chapter presents the experimental verification of the predictive controller. In order to show the efficacy of the predictive controller, a step change in the current

reference was provided. If working properly, the controller will be able to track the change in one cycle (deadbeat control).

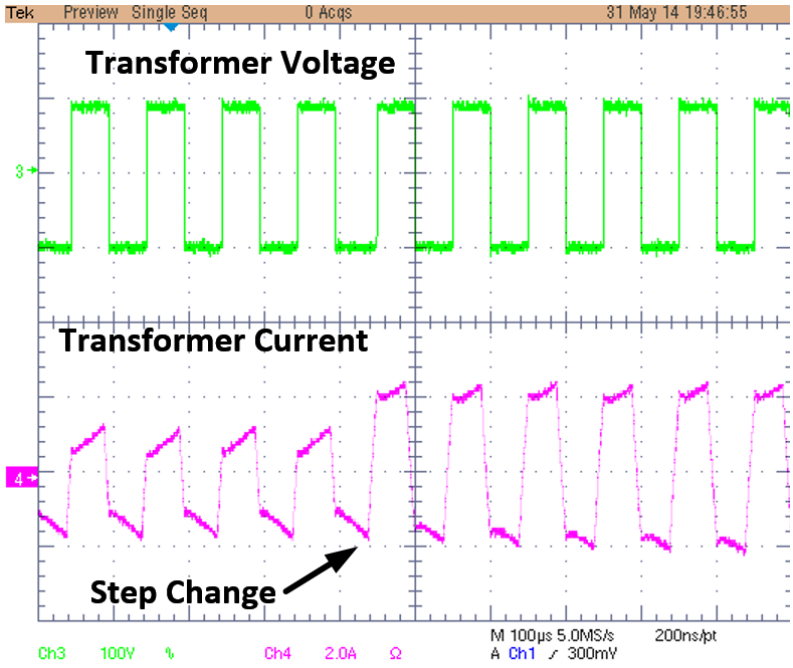


Figure 2.34: Transient test of the half cycle phase shift current mode control

Fig. 2.34 shows the step change in the current reference from the controller and the converter tracking the change in one cycle in deadbeat fashion. The control algorithm is mentioned in section 2.4.2 and equation (2.2a). The current is sampled at $\omega t = 0$ and referenced at $\omega t = \varphi$. Based on the reference value the phase shift angle has been calculated. In the setup the input voltage is 120V, the switching frequency is 10 kHz, the leakage inductance of the transformer is 0.77 mH. The current reference is changed in step from 1A to 2A.

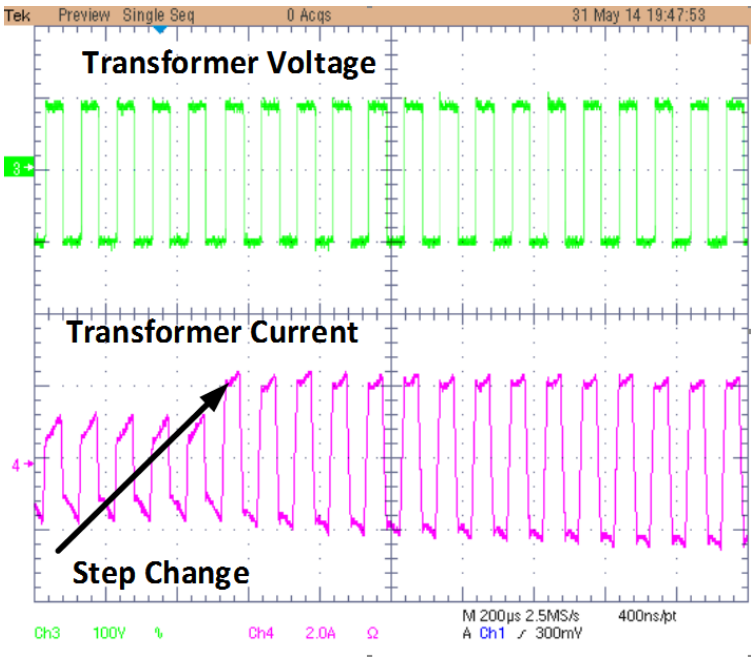


Figure 2.35: Transient test of the half cycle phase shift current mode control showing the $^{L}/_{R}$ decay.

Fig. 2.35 shows the zoomed out view of the current response. This shows the $\tau = {}^{L}/_{R}$ decay time for the current. In this present case the transformer shows a leakage resistance of 0.3 Ω. In an ideal transformer the resistance is supposed to be negligible. Hence the step change on the current reference will introduce a slowly decaying AC waveform. In an ideal transformer as $R \to 0, \tau \to \infty$. Hence the transformer current will have a permanent DC offset. This might lead to saturation of the transformer or higher losses due to the DC offset. To remedy that the duty cycle mode of control was proposed in section 2.5. The predictive half cycle mode of control proposed in section 2.8 has been implemented in the experimental setup. The current sampled at $\omega t = 0$ is referenced to the current at $\omega t = \varphi$ and the current sampled at $\omega t =$ is referenced to current sampled at $\omega t = \pi + \varphi$. Here φ represents the phase shift angle that

would have manifested in the phase shift mode of control. The controller equations are similar to that in 2.8a and 2.8b and hence is not further derived.

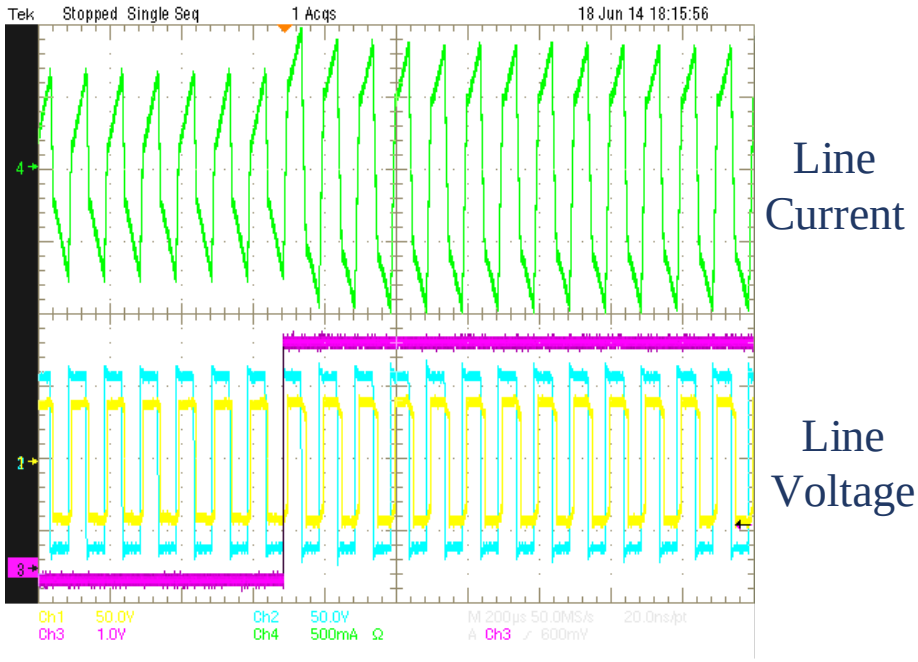


Figure 2.36: Transient test of the half cycle duty cycle current mode control.

Fig. 2.36 shows the experimental result for the duty cycle mode of control. The important difference to the previous result is the absence of the L/R decay. Since the duty cycle of the secondary bridges are operating independently, the current changes both in the positive and the negative half cycle. The controller that has been used is the TMS320F28335. Since this mode requires double sampling with in one switching cycle, the interrupt is called based on the ADC EOC. The ADC SOC is triggered by the EPWM modules as per the Fig. 2.25. The

red down counter corresponds to EPWM 1 while the blue counter corresponds to EPWM 3 phase shifted by π. ADC SOC is triggered every time EPWM 1 counter reaches the period value and EPWM 3 counter reaches the period value. These SOC signals are OR-ed in the DSP and hence sampling take place two times in the cycle, once at $\omega t = 0$ and $\omega t = \pi$. The load mode registers in the EPWM modules are set to load the compare values in the registers immediately further reducing delay. Fig. 2.37 shows the duty cycle change with the step change in the current reference value from 1A to 2A. The predictive controller still requires an inductance information to operate optimally. However the leakage inductance of the transformer may change with time due to different causes. Hence a compensation algorithm was proposed in section 2.4.3 and simulation verification was shown in Fig. 2.7. However it requires further sampling at the point of referencing. In the experimental setup a simpler algorithm was implemented. Since in the first half cycle the current was sampled at $\omega t = 0$ and referenced at $\omega t = \varphi$, it is first assumed that the current has reached the required reference at $\omega t = \varphi$. With this assumption the current at $\omega t = \pi$ is calculated as per (2.19).

$$I_{\pi}^{calc} = I_{ref} + \frac{\Delta V_2}{L_{DSP}}\left(\frac{1}{2} - d_1\right)T_s \tag{2.19}$$

Here $\Delta V_2 = V_{out} - V_{in}$ and L_{DSP} ($\neq L_{act}$) is the erroneous inductance value input to the controller and d_1 is the duty cycle calculated from the predictive controller as per equations (2.8a) and (2.8b). If $L_{DSP} = L_{act}$ in that case $I_{\pi}^{calc} = I_{\pi}^{ref}$. In order to compensate for the change in the inductance value with time a compensation loop is run parallel to the controller with a slower bandwidth. The output of the compensator is ΔL which is added to L_{DSP} and

replaces L in (2.8a) and (2.8b). Fig. 2.38 shows the controller block diagram for the compensation for the inductance error in the controller.

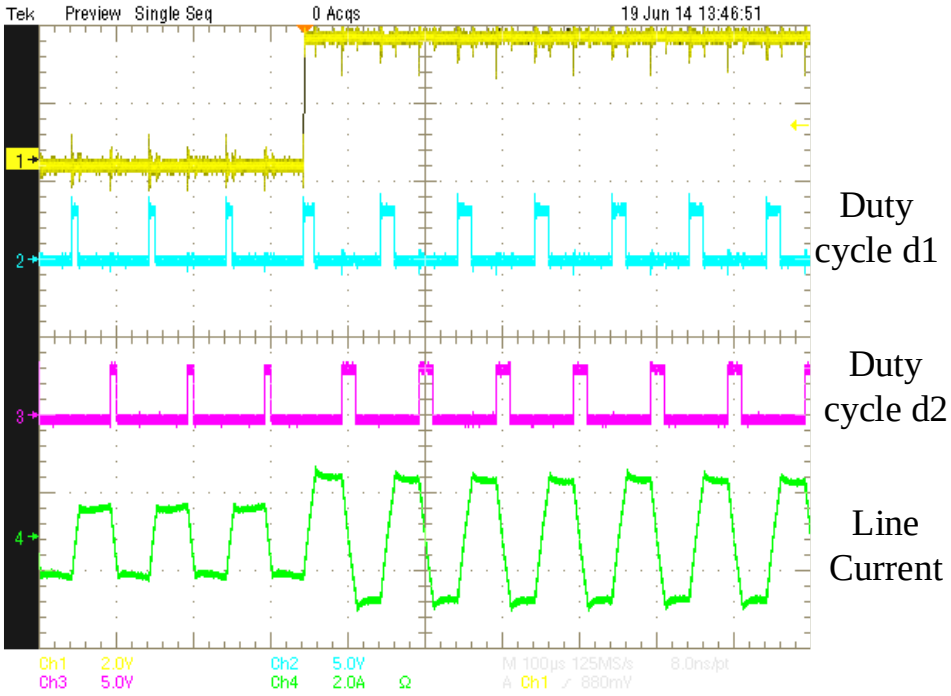


Figure 2.37: Transient test of the half cycle duty cycle current mode control along with the changes in the duty cycles d_1 and d_2

Fig. 2.39 shows the experimental result for the compensation loop implemented in the controller. The measured transformer leakage inductance is 0.936 mH and the erroneous inductance value was set as 0.7 mH. It is seen that the controller compensates for the error by introducing the ΔL which gets added to L_{DSP} to track the reference correctly.

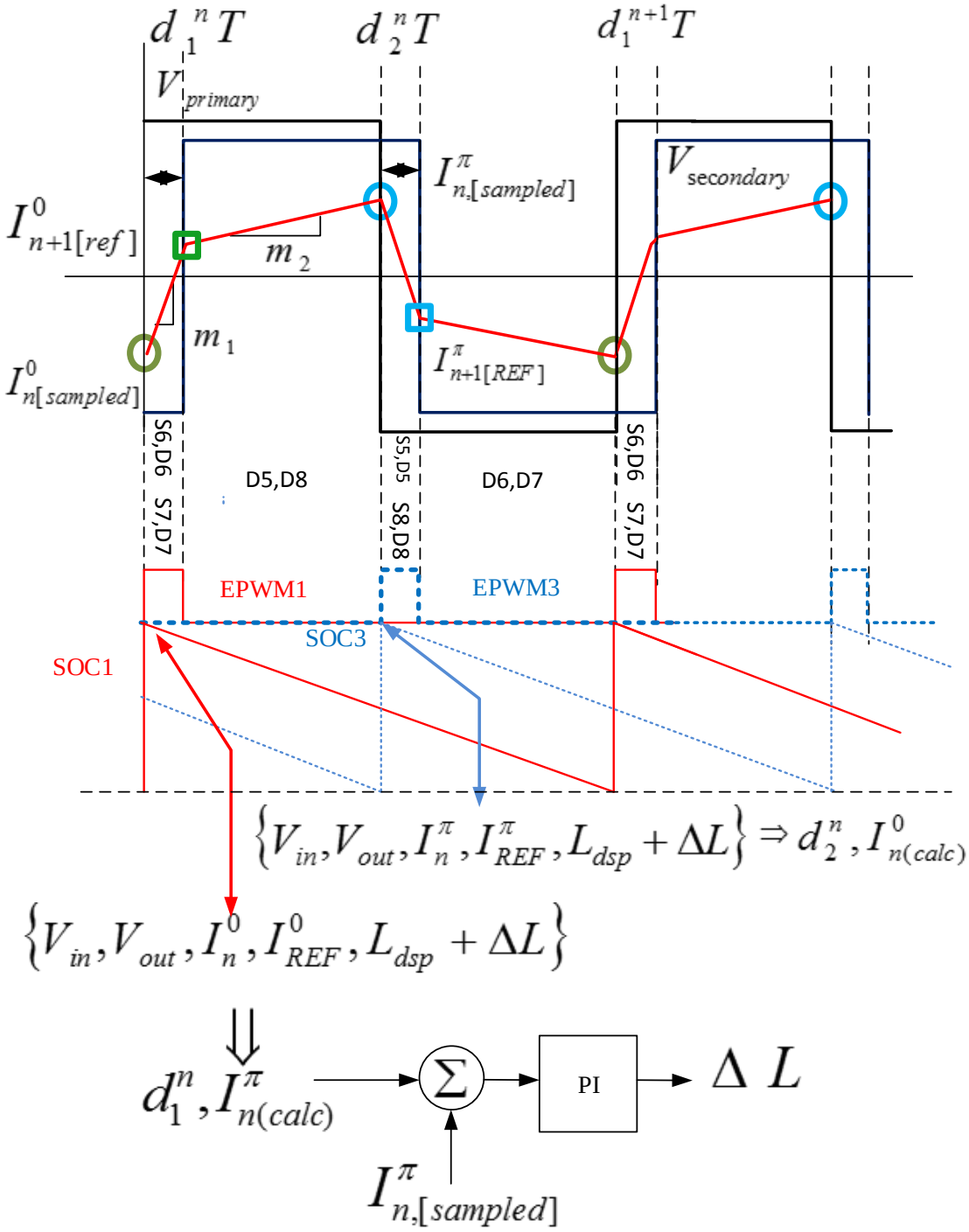


Figure 2.38: Controller diagram for the leakage inductance error compensation

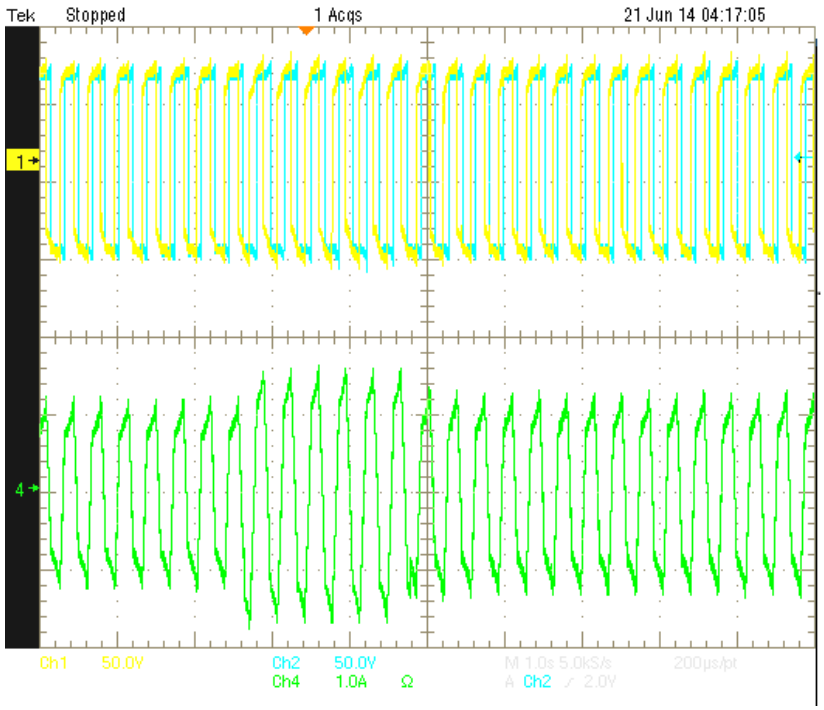


Figure 2.39: Transient test of the leakage inductance error compensation

2.13. Conclusions

In this chapter the digital predictive current mode control have been applied to the DAB converter. The main results obtained in this chapter is summarized as follows:

- A predictive phase shift controller was proposed for the dual active bridge converter. The controller is of dead beat in nature and updates the control variable in one cycle.
- The controller was shown to be sensitive of the leakage inductance value of the transformer hence a compensation loop was implemented to make the system insensitive of the change in inductance value.

- A duty cycle mode of control was proposed for the Dual Active Bridge Converter. The proposed control was shown to remove any DC bias in the transformer current by adjusting the duty cycles independently.
- A predictive duty cycle mode of control was proposed. The proposed control was shown to be dead beat in nature. In order to remove the DC bias in the transformer current an equal area criterion was imposed to calculate the duty cycles. The equal area criterion forces the area under the DAB transformer current waveform to zero to remove unwanted DC bias.
- A power based predictive controller was proposed that predicts the phase shift angle based on the required power transfer. The power based controller was shown to have second order response due to the quadratic nature of the power angle curve.
- Experimental verification of the phase shift predictive controller was performed. A step change in the current reference was provided and the controller was shown to follow the reference in one cycle. However a L/R decay was shown to exist in the current as per the transformer L/R time constant.
- Experimental verification of the duty cycle mode of control was performed. With a step change in the current reference, the controller was shown to respond within one switching cycle. Due to the asymmetric variation in the duty cycle, the current waveform was shown to be free of the L/R transient, which was otherwise present in the phase shift predictive current mode control.

- An analysis was done to understand the contribution of the primary and the secondary bridges in supplying the magnetizing current of the high frequency transformer in the DAB. A method was proposed to sense the DC bias in the current by implementing a moving window average on the magnetizing current and a compensating DC offset was then given to the primary or the secondary switches to remove any unwanted DC bias in the magnetizing current.

Chapter 3 Multi-terminal application for the Dual Active Bridge converter for multiple Renewable Energy Source integration

3.1. Introduction

In this chapter of the thesis a multi-terminal DAB is considered with multiple inputs and single output for the purpose of renewable energy integration. Extensive research has been done on the integration of renewable energy sources (RES) to a common DC bus using parallel DC to DC converter [11]. DC droop control or master slave mode of control is employed for power sharing between the parallel DC to DC converters. The introduction of the SST concept [21], has provided the motivation of integrating the renewable energy sources directly into the high frequency magnetic stage of the topology, i.e. the DAB stage. This provides the benefit of galvanic isolation using minimum magnetic component. Integration of multiple renewable energy sources in the DAB topology is an interesting topic of research. In [13] several multiport DAB topology has been mentioned. In [4] and [12] a gyrator based concept for the multiport DAB topology has been proposed. Since RES may have fluctuating voltage profile due to the intermittency of power available, when source voltage magnitudes are different the single core topology [13] will drive a reactive current through each of the source bridges leading to losses. In this chapter a flux accumulation based approach has been followed to decouple individual RES from each other. This has been achieved using a multi-limb-core transformer based topology. It is fundamentally a multi terminal DAB converter with multiple primaries and a single secondary. Power transfer take place between the primary and secondary using phase

shift modulation. Instead of the primaries linking a single core, they are all linked to different cores that are connected to a central limb, to which the secondary winding is connected. This central limb acts as a flux accumulator. Equivalent circuit of the topology has been derived to explain the decoupling of the individual RES. A PWM based switching strategy has been proposed to control the source current in order to operate the RES at their individual maximum power point.

3.2. Circulating current in a single limb core topology

The circulating current in a single limb core based topology is the motivation driving the research in this chapter. This section discuses in more detail the single limb core topology. Fig. 3.1 shows the single limb core based multi-active bridge topology. Circulating current will exist between the primaries provided $V_1 \neq V_2 \neq V_3 \neq V_4$. The circulating current not only depends on the magnitude of the voltage mismatch but also on the leakage inductances linking the individual windings (Fig 3.2). However the circulating power is also a function of how the leakage is distributed in the windings. This provides the motivation of understanding how the distribution of leakage will affect the circulating current which has been discussed in section 3.3 and 3.4.

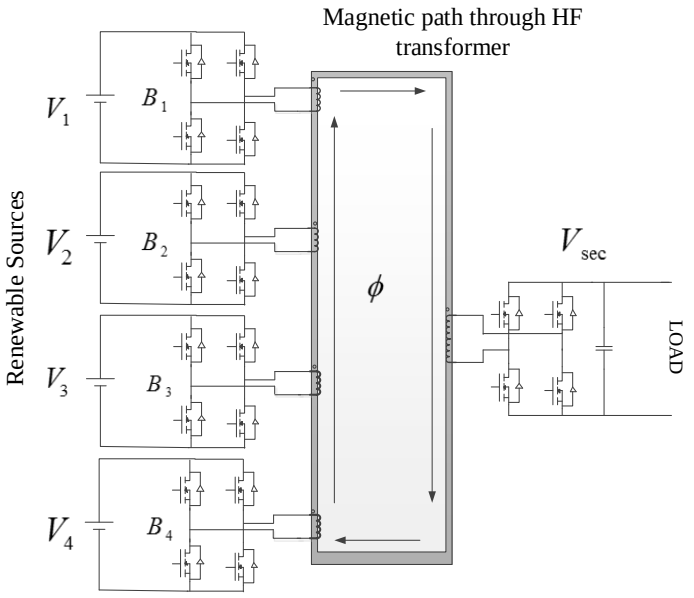


Figure 3.1: The Multi-Active Bridge converter concept based on a single limb core topology

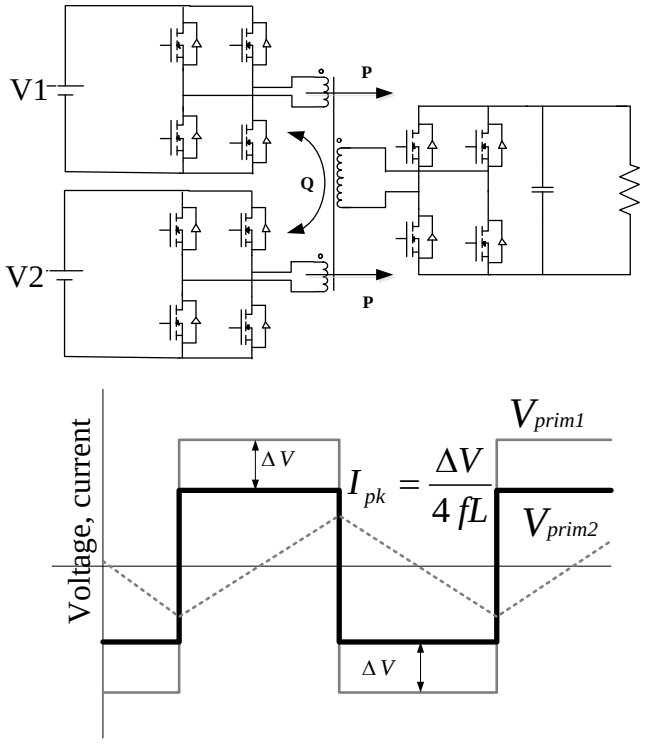


Figure 3.2: Circulating current due to voltage mismatch

3.3. Leakage inductance distribution and the impact on the circulating reactive power

Leakage inductance of the primary and the secondary windings are the most important factor in determining the circulating reactive power in the system. For simplicity the triple active bridge system is considered (Fig. 3.2) with two primaries and one secondary. The equivalent diagram of the system is shown in Fig. 3.3.

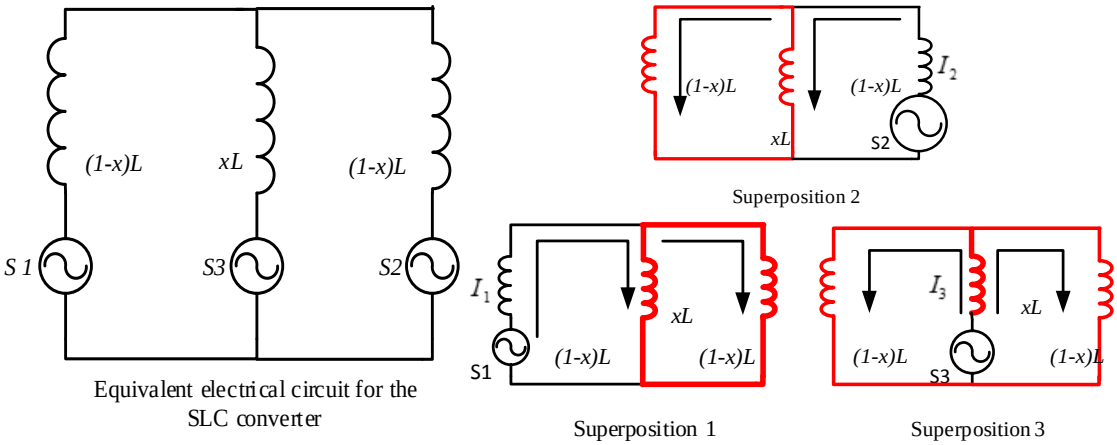


Figure 3.3: Circulating current due to voltage mismatch in the primaries

The three bridges are voltage sourced hence modelled by voltage sources S_1, S_2 for primary 1 and primary 2 and S_3 for the secondary lagging bridge. The leakage inductance can be considered to be distributed between the primaries and the secondary as shown in Fig. 3.3. A symmetrical distribution is considered to make the calculations simpler. In order to calculate the reactive power supplied by the sources the superposition theory is used. The superposed

circuits are shown in Fig. 3.3. The current supplied by the sources are given as I_1 for source S_1, I_2 for source S_2 and so forth. The net current then can be calculated according to the superposition theory. I_{S1} is the net current for source S_1, I_{S2} for source S_2 and so forth. Q_1 is the reactive power supplied by the source S_1 , Q_2 by source S_2. P_1 is the real power supplied by the source S_1, P_2 by source S_2. δ is the phase lag in radians of the secondary bridge with respect to the primary bridges. ω is the switching frequency of the converter in radians per second. It can be mathematically derived from the expressions of the reactive powers that both Q_1 and Q_2 has a minimum with $x = 0$. Hence the entire leakage of the individual windings has to be on the primary side with minimum possible leakage on the secondary. This is possible with a coaxial winding transformer (CWT). The following section proposes the CWT based topology in details.

3.4. Coaxial Winding transformer (CWT) based topology

The coaxial based topology has been shown in Fig. 3.4. In a CWT based topology the transformer leakage inductance can be controlled by changing the radii of the primary or the secondary conductors (3.1) [20].

$$L_{leakage} = kln\frac{r_2}{r_1} \tag{3.1}$$

In order to keep the leakage on the primary side, the primary conductor is kept within the secondary conductor. Fig. 3.4 shows the topology of the CWT based accumulator. The different primary bridges are connected to different RES forming accumulator concept. Since

RES are the primary sources, MPPT operation becomes an important aspect for the topology to handle. An MPPT driven input DC current control has been investigated in the following section to make each primary operate at different phase angle (δ) to supply the power available. The following section treats the concept in details.

Table 3.1: Current and power contributed by each source in the multi-active bridge topology

Parameters	Values
I_1	$\frac{V_1}{j(1-x^2)\omega L}$
I_2	$\frac{V_2}{j(1-x^2)\omega L}$
I_{S1}	$I_1 - \frac{I_3}{2} - xI_2$
I_{S2}	$I_2 - \frac{I_3}{2} - xI_1$
P_1	$-\frac{V_1 V_3 \sin\delta}{(x+1)\omega L}$
P_2	$-\frac{V_2 V_3 \sin\delta}{(x+1)\omega L}$
Q_1	$\frac{V_1^2 - (xV_1V_2) - V_1V_3(1-x)\cos\delta}{(1-x^2)\omega L}$
Q_2	$\frac{V_2^2 - (xV_1V_2) - V_2V_3(1-x)\cos\delta}{(1-x^2)\omega L}$

One of the bridges can be connected to a battery as shown in Fig. 3.4 and act as energy storage in times of excess generation. One of the bridges is connected to the primary side rectifier and can be used to send back power to the grid or take power from the grid should the need arise. Since the bridges are connected to RES, hence the MPPT operation becomes an important

aspect to investigate. The primary and the secondary H bridges are switched at 50% duty cycle with the secondary bridge lagging to transmit the power as per (3.2).

$$P_{transferred} = \frac{V_{in}V_{out}\sin\delta}{\omega L} \tag{3.2}$$

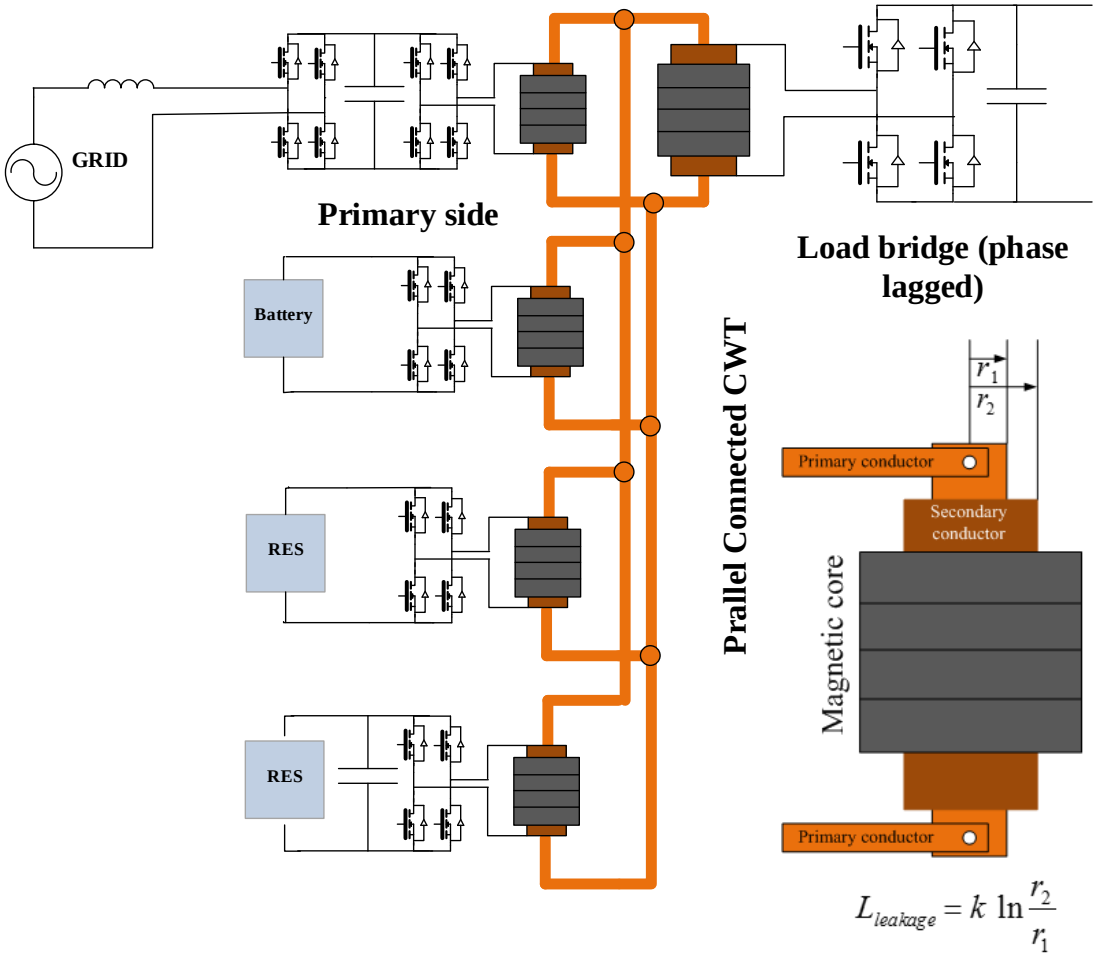


Figure 3.4: Multi-terminal CWT based topology as a renewable energy accumulator

3.5. Input current control in the CWT based topology

Without a loss of generality we can assume that each RES operates at different operating point which translates into different δ as per (3.2). Fig. 3.5 proposes the control scheme for the CWT based topology schematically. Since the entire leakage is assumed to be on the primary side each primary is decoupled from the other primary and power transfer only takes place between individual primary and the secondary. The equivalent electrical circuit for the fundamental frequency is given in Fig. 3.5. Since each sub circuit is completely decoupled from each other there is no circulating reactive power between the primaries due to DC bus voltage mismatch. As per in Fig.3.5 the entire circuit can be separated out into 4 sub-circuits, one for each primary. L_1, L_2 ... are the leakage associated with each primary. The power transferred is as per (3.2). The total power transferred to the secondary is

$$P_{TOTAL} = \sum_{i=1}^{4} \frac{V_{PRIMi} V_{SEC} sin\delta_i}{\omega L_i} \tag{3.3}$$

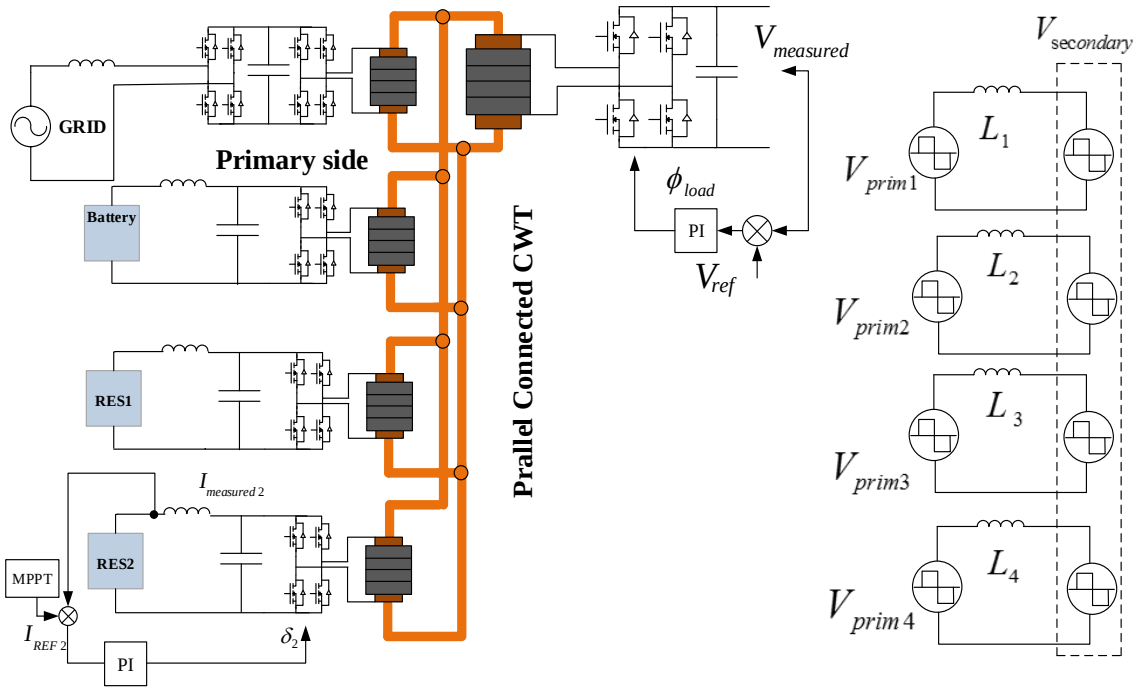


Figure 3.5: Input current control operation on the CWT based topology

3.6. Series connected transformer based topology

The coaxial based design for a high frequency transformer has several disadvantages. Some of the disadvantages have been explained in [20]. They are:

1. Edge effect

2. Limit in the number of turns.

The edge effect as mentioned in [20], shows that the leakage is considerable on the edges of the transformer than the inside of the cylinder. Hence there is a requirement of adding more magnetic core element in the transformer core to achieve significant self-inductance on the

primary side. Adding more core material increases weight and for applications where weight saving is a concern, this becomes a problem. The limit in the number of turns is a fundamental problem for the coaxial transformer. In Fig. 3.5 we see a 1:1 configuration. However in case a step up in voltage is required it is desirable to add more number of turns to the secondary side of the transformer. This will add more unwanted leakage inductance on the secondary side. The decoupled sub-circuit assumption will no longer remain valid (Fig.3.5). Due to these disadvantages a series connected topology has been proposed.

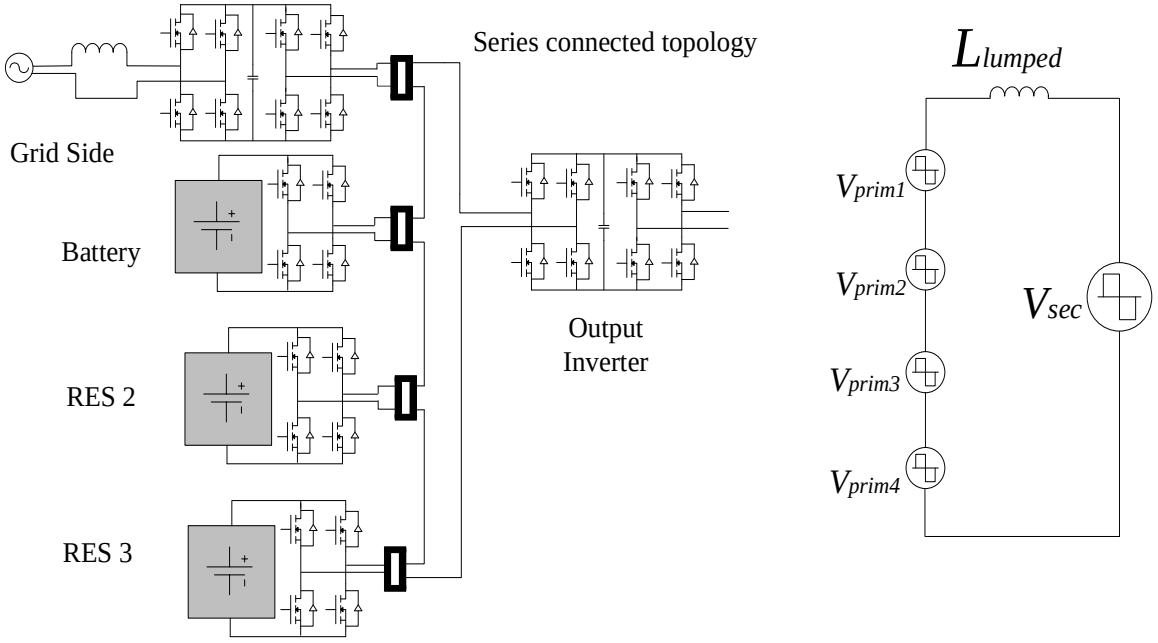


Figure 3.6: The series connected topology

The series connected topology and the equivalent circuit is shown in Fig. 3.6. All the high frequency primary voltages are in series and in phase. Therefore the fluctuation in the voltage does not drive any additional reactive power between the primary voltages. Unlike the CWT topology the leakage inductance can be distributed between the primary and the secondary. Hence the transformer design becomes much easier. The number of turns can be manipulated to achieve the necessary voltage step up on the secondary side. The power transfer between the primaries and the secondary take place through the lumped inductor (L_{lumped}) in Fig. 3.6 which is the sum total of all the leakage inductances of all the windings (primary and secondary). Provided there is no phase shift between the primary voltages, and the secondary voltage lags the primary by angle δ, the power transfer is given by (3.4).

$$P_{TOTAL} = \frac{\left(\sum_{i=1}^{4} V_{prim\,i}\right) V_{sec} \sin\delta}{\omega L_{lumped}} \tag{3.4}$$

The different functionalities of the accumulator topology have been laid out in the introduction of the paper. One of the principle functionality of the accumulator is to have MPPT based current or voltage control to make the RES deliver the maximum power under any voltage. MPPT operation was possible on the CWT topology. The MPPT operation for the series connected topology is discussed in the following section.

3.7. Input current control in the series connected topology

Input current control is possible in the series connected topology using duty cycle modulation as shown in Fig.3.7.

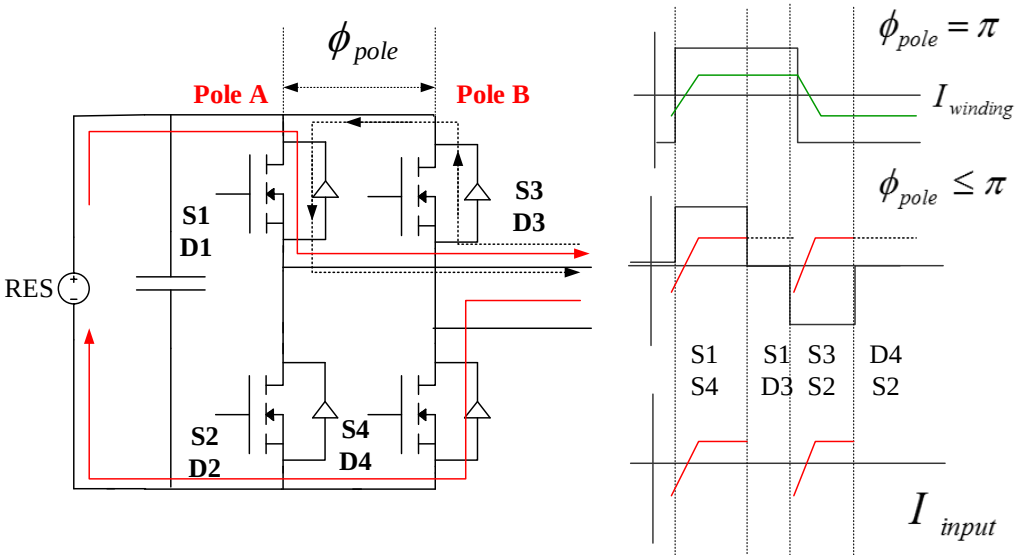


Figure 3.7: The Duty Cycle modulation to implement input current control

Fig. 3.7 shows the schematic of the duty cycle mode of control to achieve the input current regulation. A phase shift is given in the primary poles as shown in Fig. 3.7. A pole to pole phase shift (i.e. between Pole A and Pole B) of π implements the 50 % voltage waveform. If the pole phase shift is less than π we get a zero level in between. This dead time is created when the current from the winding circulates between the switches and the diodes (S_1, D_3) or (D_1, S_3). Many such combinations exist depending on the current direction and the previous switching state. This switching strategy helps to partially decouple the input current from the winding current as per (3.5).

$$I_{source} = \frac{\varphi_{pole}}{\pi} I_{winding} \tag{3.5}$$

Without the loss of generality it can be considered that one of the RES connected to the peripheral winding and the H-bridge needs to operate at a lower I_{ref} generated from the MPPT algorithm, while the rest of the peripheral windings have a pole phase shift of π. In Fig. 3.7 the green is the winding current common to all peripheral and central winding. For the bridge that does MPPT we have $\varphi_{pole} \leq \pi$. For that bridge (Fig. 3.7) at the beginning of the switching period S_1 and S_4 are turned on and pole to pole voltage is V_{DC} . During this time the winding current flows through the switches S_1 and S_4 (red arrow in Fig. 3.7) and the source. Hence the source supplies power. Then after $\omega t = \varphi_{pole}$ the switch S_4 is turned off. Since at this time the current is positive, it forward biases the diode D_3 and flows through it. Thus it introduces a zero state in the pole to pole voltage. The winding current then circulates through S_1 and D_3 (dotted line in Fig. 3.7). The source does not provide any current at that instant and is disconnected. Thus by controlling φ_{pole} we can control the amount of current drawn from the source and implement MPPT. Since $\varphi_{pole}^{MAX} = \pi$ we have an upper limit on the MPPT current which is equal to the input current of the other RES with the bridges operating at $\varphi_{pole} = \pi$. Experimental results validating the control scheme will be shown at the later sections on a low voltage prototype.

3.8. A multi-limb transformer topology

In this section an alternate to the series connected topology has been proposed. The multi limb core topology [22] is shown in Fig. 3.8. The peripheral limbs have windings that are connected to H-bridges connected to RES, battery or grid tied. The peripheral limbs generate

the flux that is accumulated in the central limb. The winding in the central limb is connected to the H-bridge that is connected to the output load. The primary bridges are switched at 50 % duty cycle. There is no phase difference between the primaries. The secondary is lagged with respect to the primary to regulate the output voltage. Hence the switching is exactly similar to the series connected topology. The 5-limb core structure is shown in Fig. 3.8. The primary sources are connected to the peripheral limb via H-bridge while the central limb accommodates the secondary winding. One of the primaries is connected to energy storage. An electrical equivalent circuit is derived in the following section which show how each individual voltage sources, although connected by the fused magnetic structure, is decoupled. The magnetic equivalent circuit of the MLC based topology is shown in Fig 3.9. It is functionally similar to the series connected topology. The similarity is explained in the following section.

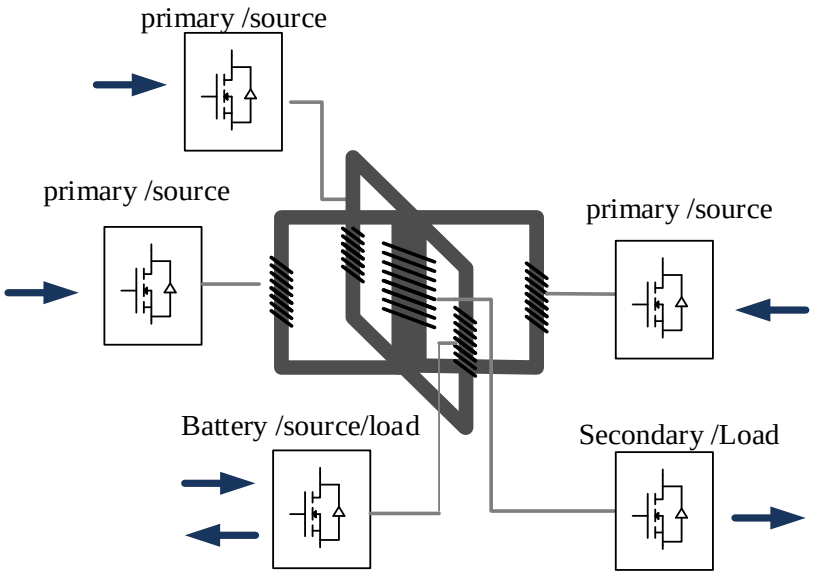


Figure 3.8: The MLC based topology

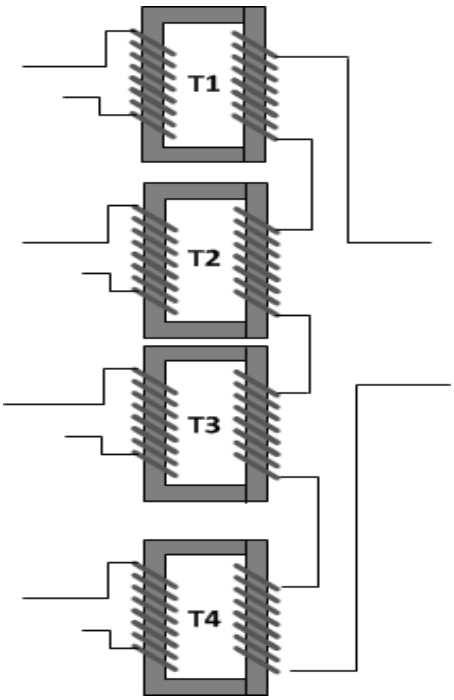


Figure 3.9: Electrical equivalent of the MLC topology

3.9. Electrical equivalent circuit of the MLC topology

Fig. 3.9 shows the magnetic equivalent circuit for the MLC transformer in terms of modular cores. Since the interface between the electrical stage and the magnetic stage acts as a natural gyrator, bond graph model is an effective approach to derive the equivalent model of the system [23], [24], [25]. A simpler three limb core topology was considered for the bond graph analysis. Using the natural gyrator principle the bond graph for the three limb core transformer was developed.

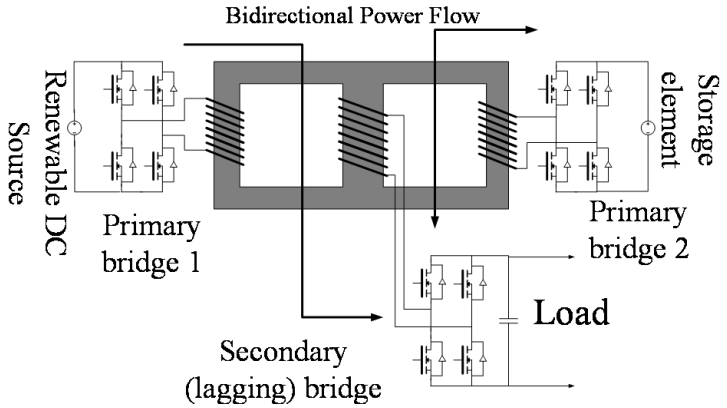


Figure 3.10: A three-limb transformer based topology

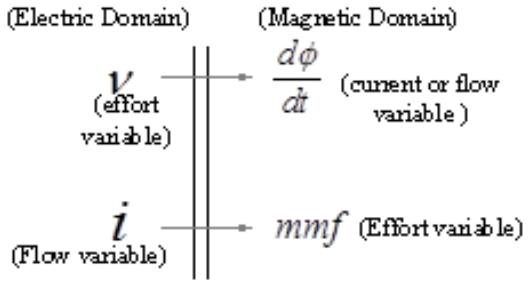


Figure 3.11: The natural gyrator principle

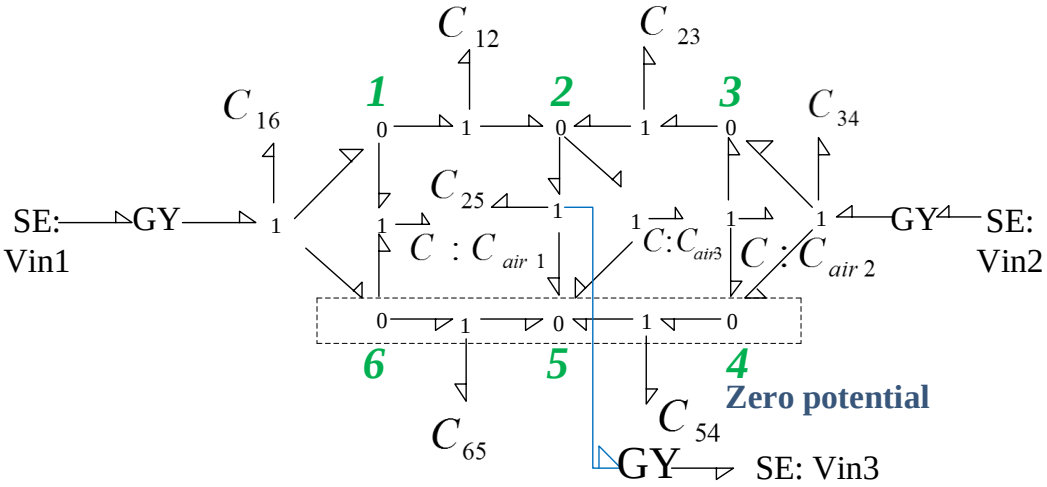


Figure 3.12: The bond graph model for the three-limb core transformer topology

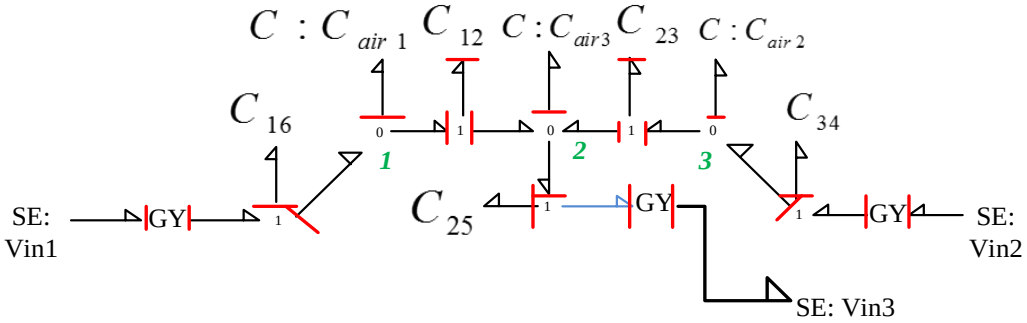


Figure 3.13: Simplified bond graph model

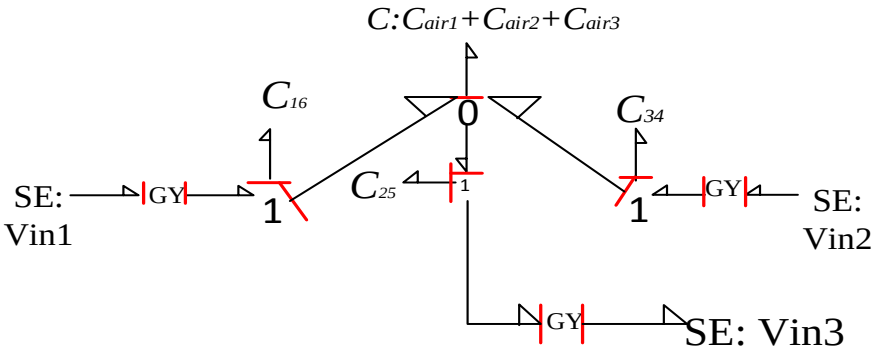


Figure 3.14: Bond graph model with further simplifications

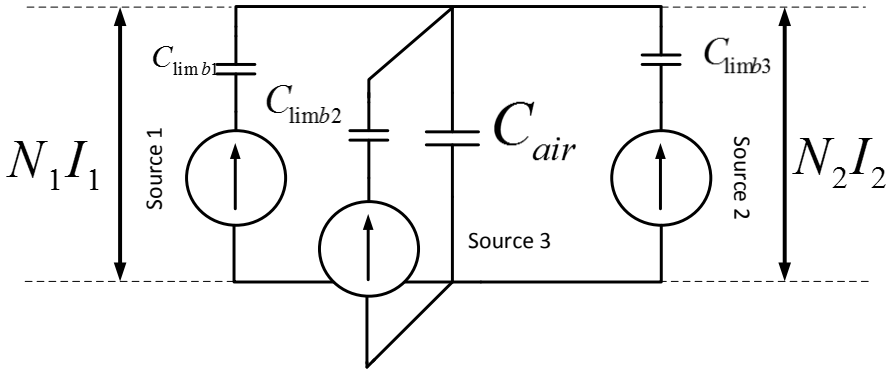


Figure 3.15: Electrical equivalent of the magnetic stage of the MLC topology

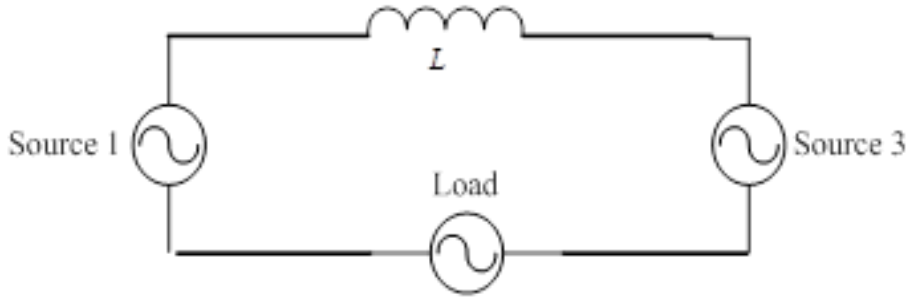


Figure 3.16: Electrical equivalent of the electrical stage of the MLC topology

The bond graph modeling for the three limb core is shown in Fig. 3.12. There are three electromagnetic interfaces for a three-limb core. Hence the bond graph has three gyrator bonds denoted as |GY|. The nodes of the magnetic circuit are marked (1, 2, to 6) as shown in Fig. 3.12. The permeance of the limbs between the successive nodes are denoted as C_{12}, C_{23}, C_{34}, etc. The permeance of air are C_{air1}, C_{air2} etc. The final equivalent circuit in the magnetic domain is two current sources connected in parallel with the load (Fig. 3.15). The inverse dual of the circuit is considered to represent the system in terms of electrical circuit components. As suggested in Fig. 3.16, the equivalent circuit comprises of series connected voltage sources with a lumped inductance L which is the sum of the leakage inductances of the three windings. Since the voltage sources are connected in series they become independent of each other. However the same current flows through all of them. Hence from the circuit point of view, the three limb core can be considered to be composed of two separate single phase transformers with the secondary connected in series (as shown in Fig. 3.17).

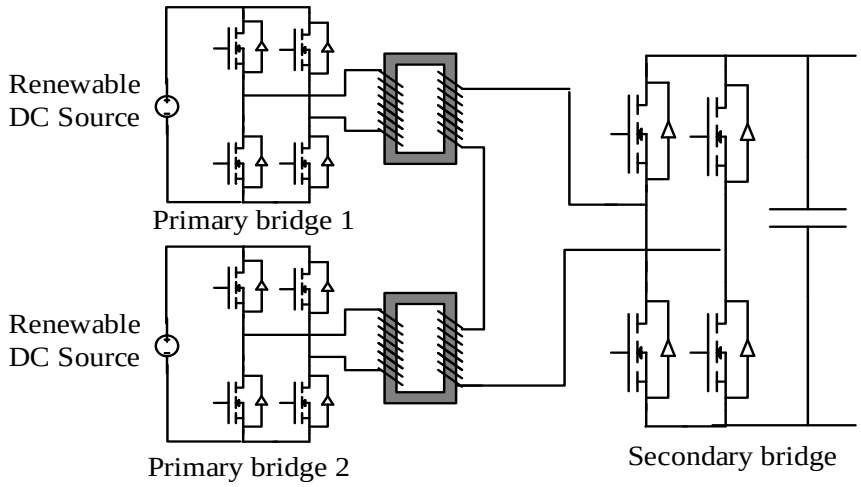


Figure 3.17: Electrical equivalent of the three limb MLC topology

3.10. Advantages of the MLC topology based on the copper usage

The MLC topology works by accumulating the fluxes generated in the peripheral limbs in the central limb (Fig. 3.18). Hence the flux cut by the windings in the central limb is a summation of the fluxes in the individual peripheral limb. Since the flux adds up in the central limb (Fig 3.18), with the same number of windings, the voltage induced in the central winding adds up as well. For example with N number of windings in each peripheral winding and central winding, and with peak voltage V in each peripheral winding, the induced voltage in the central winding is *xV*, where *x* is the number of peripheral limbs. To achieve the same in a series connected winding, the number of turns required is *xN*. This shows that there is a significant gain in copper. However the gain is not simply *(x-1) N* turns. Since the flux in the central limb adds up, the cross sectional area needs to increase as well to avoid saturation. Hence for a 1:1 application if the individual peripheral limbs have cross sectional area of A,

then the central limb will have cross sectional area of *xA*. Hence with increase in cross sectional area the perimeter of the central limb will increase as well. Hence each turn in the central limb will be longer than that of the peripheral limbs. Gain factor is defined as in (3.6).

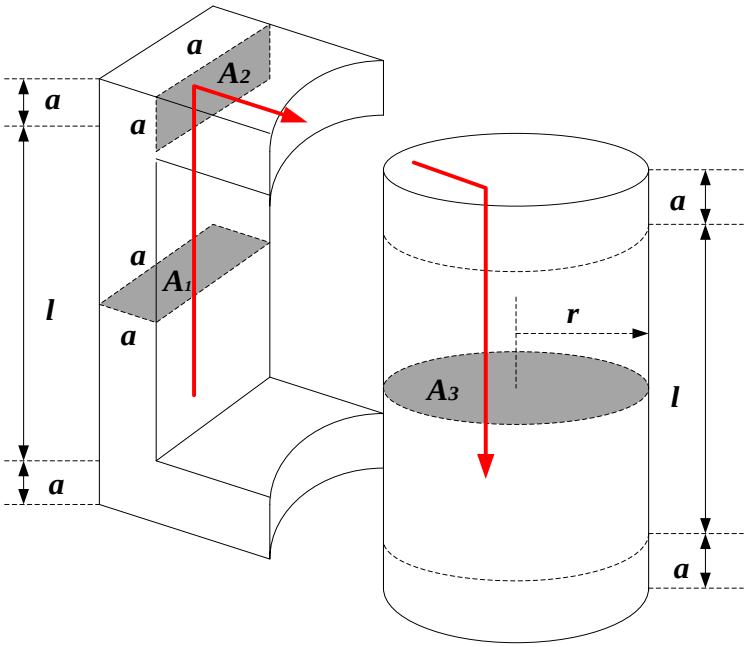


Figure 3.18: Flux path in a peripheral and the central winding

$$Gain\ factor = \frac{Length\ of\ copper\ used\ by\ the\ central\ limb}{Length\ of\ copper\ used\ by\ series\ connected\ cores} \tag{3.6}$$

To calculate the gain factor it is assumed that the peripheral limbs have a square cross section and the central limb has circular cross sections (Fig. 3.18). Let each side of the peripheral limb be "*a*" and the central limb have a radius "*r*". Then from the area constraint we have (3.7).

$$xa^2 = \pi r^2 \tag{3.7}$$

Considering the winding length of the core to be "*l*", the wire thickness to be negligible, the area of copper required in MLC central limb is $2\pi rl$ and that for series connected transformers the area of coppered surface is $4xal$. Therefore gain factor is:

$$gain\ factor = \frac{2\pi rl}{4xal} \tag{3.8}$$

In (3.8) if we substitute (3.7) we get the following gain factor (3.9).

$$gain\ factor = \frac{.886}{\sqrt{x}} \tag{3.9}$$

This proves that lower the gain factor shows advantage of the MLC transformer w.r.t. the series connected core topology (Fig. 3.19). It is seen from the plot of the gain factor against the number of peripheral limbs that the gain factor is lesser at higher number of peripheral limbs. It is also important to note that with increase in the number of limbs the physical construction of the transformer becomes complicated. The MLC structure is not modular in nature. If the need arises to increase or decrease in number of RES, the whole transformer needs to be redesigned. However, where weight is an issue, it is important to note that the MLC structure provides a significant advantage by reducing the amount of copper used.

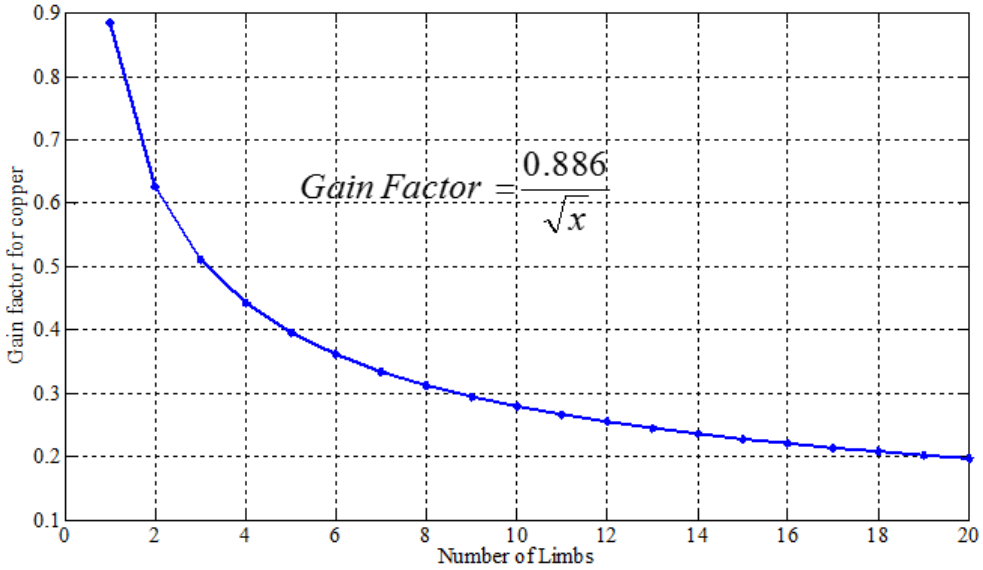


Figure 3.19: Plot of the gain factor w.r.t. the number of limbs

3.11. Magnetic core material requirement in MLC topology

In the previous section and as shown in (3.7), the area of cross section of the central limb has to be addition of the area of cross section of the peripheral limb. This shows that apparently there is no gain in magnetic material for the MLC topology. This section deals with the magnetic core requirements in greater details. The cross sectional area of the cores depend on the voltage induced (V_{LIMB}) on the particular limb as per (3.10).

$$V_{LIMB} = 4NAf_{switching}B_{peak} \tag{3.10}$$

Here N is the number of turns in the winding, A is the cross sectional area of the limb $f_{switching}$ is the switching frequency and B_{peak} is chosen for the particular material. Hence the cross sectional area depends on the winding terminal voltage. Now the problem statement itself

states that the RES bus voltages are variable in nature. Hence in the MLC topology the peripheral limbs that see the intermittent RES voltages has to be rated for the maximum voltage possible. In the series connected topology, on the secondary series side there is no control over the voltage distribution. Hence the entire transformer has to be over rated (i.e. both the primary and the secondary limb) than the terminal maximum terminal voltage available from the RES. As an example a particular case is considered in Fig. 3.20. A five limb MLC topology is simulated in PLECS. The four peripheral limbs are connected to RES while the secondary limb is the load. The RES voltage swings from a maximum of 2 kV to zero. The output voltage is regulated to 8 kV. The extreme case is considered when only one RES is supplying the load while the rest of the RES dc bus doesn't have voltage. The results are shown in Fig. 3.20. The peripheral limb 1 supplies the voltage from the RES. The rest of the peripheral limbs don't have a DC bus. It is seen that the flux in the peripheral limb 1 (Fig. 3.20) reaches a maximum peak of 0.027 Weber when it is the only source supplying energy. With the rest of the DC buses turned on the flux level drops to 0.02 Weber. Similarly in a series connected topology the same condition was tested with one primary having the rated DC bus from the RES with the other primaries having zero DC bus. The rest of the parameters were i.e. switching frequency, total leakage, etc. were kept the same (Fig. 3.21).

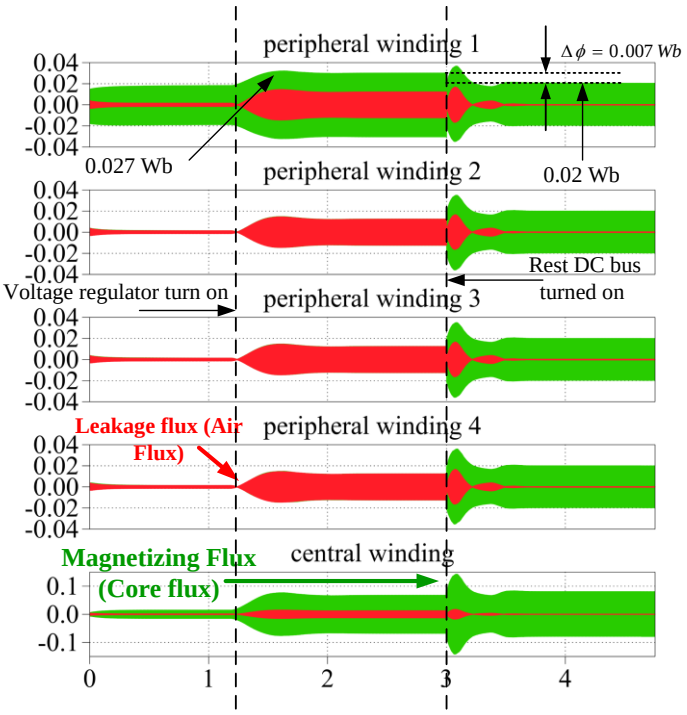


Figure 3.20: Flux plot for the MLC based topology

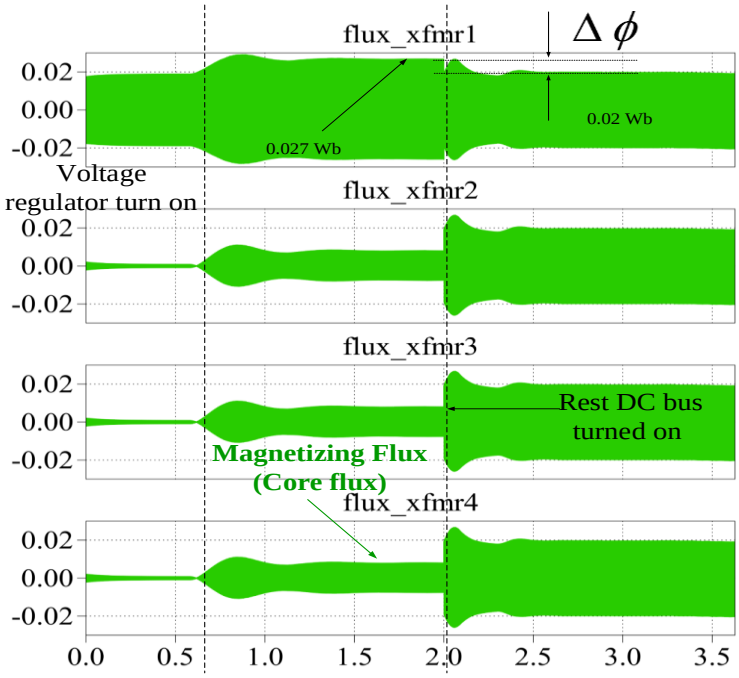


Figure 3.21: Flux plot for the SLC based topology

It was seen that the peak flux was 0.027 Weber as well. In this case there were 4 cores in the SLC and 4 peripheral limbs and 1 central limb in the MLC. The core material required for the primary winding limbs are same in the SLC and MLC. Let the winding length be *l* both for primary and secondary (Fig.3.18). The secondary limb peak flux for the SLC will be same as the primary limb peak flux since a single magnetic path connects the primary and the secondary winding. The required cross section for the secondary limb in each of the transformers in the SLC configuration is $A_{SLC} = \frac{.027}{B^{peak}}$ from (3.10) and the volume required is $V_{SLC} = \frac{.027}{B^{peak}} l$. Since there are four single phase transformers in the SLC configuration, the total volume is $V_{SLC} = \frac{.027}{B^{peak}} 4l$. For the MLC configuration the flux linked to the secondary winding in the central limb is 0.08 Weber. Hence the area of the central limb has to be $A_{SLC} = \frac{.08}{B^{peak}}$ from (3.10) and the total volume of the central limb is $V_{MLC} = \frac{.08}{B^{peak}} l$. Since there is only one central limb we have a gain in volume in the MLC configuration (3.11).

$$\Delta V = V_{SLC} - V_{MLC} = \frac{.028}{B^{peak}} l \tag{3.11}$$

A more generic analysis is as follows:

$$Vol^{SLC} = \frac{4lV_1}{4N_1 f_{sw} B_{pk}} + \frac{4lV_2}{4N_2 f_{sw} B_{pk}} \tag{3.12}$$

$$Vol^{MLC} = \frac{3lV_1}{4N_1 f_{sw} B_{pk}} + \frac{3lV_2}{4N_2 f_{sw} B_{pk}} + \frac{lV_{sec}}{4N_{sec} f_{sw} B_{pk}} \tag{3.13}$$

$$\Delta Vol = \frac{lV_1}{4N_1 f_{sw} B_{pk}} + \frac{lV_2}{4N_2 f_{sw} B_{pk}} - \frac{lV_{sec}}{4N_{sec} f_{sw} B_{pk}} \tag{3.14}$$

$$for\ \Delta Vol \geq 0\ we\ get\ \frac{V_1}{N_1} + \frac{V_2}{N_2} - \frac{V_{sec}}{N_{sec}} \geq 0 \tag{3.15}$$

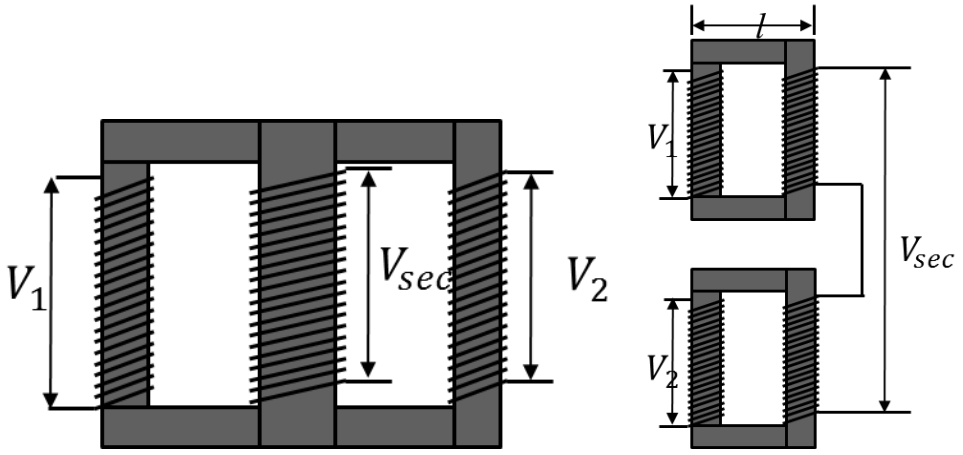


Figure 3.22: Three-limb MLC and SLC topology

Therefore it can be seen from (3.15) that by choosing the rated voltages properly we can obtain a gain in the magnetic core materiel used in the transformer while going to the MLC based topology from the SLC topology.

3.12. Design of a MLC transformer based on the magnetic stage loss analysis

This section details out a design for the MLC 5-limb core transformer using the ferrite core from Magnetics-inc, of material F type 0P49925UC.

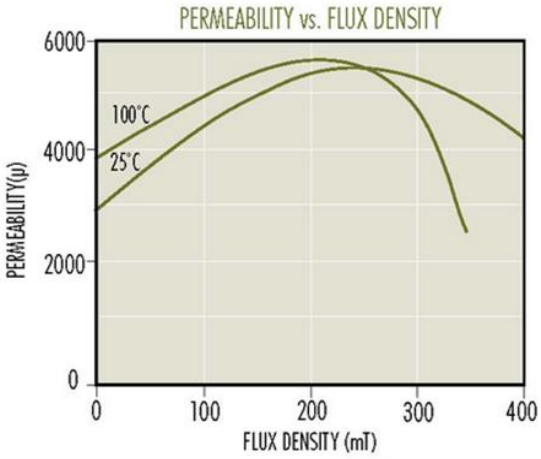


Figure 3.23: B-H characteristic of the core material used for the construction of the MLC topology (source: http://www.mag-inc.com/products/ferrite-cores/f-material)

The plot of the permeability and the flux density for core in use is shown in Fig. 3.23. The plots were obtained from the website (www.mag-inc.com) for the ferrite core material F-type.

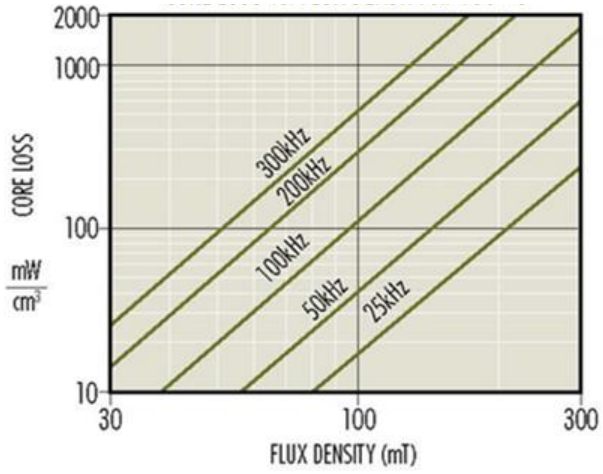


Figure 3.24: Core loss for the ferrite core material (F) (source: www.mag-inc.com/products/ferrite-cores/f-material)

The switching frequency is 10 KHz and the voltage across the peripheral limbs are 100V. The central limb core sees a voltage of 400V. The system power is 1KW. The saturation magnetic flux density for the core used is 0.47 T. The optimum flux density is calculated by minimizing the total losses in the magnetic stage as per the following analysis:

$$P_{total\ loss} = P_{core} + P_{cu} \tag{3.16}$$

Minimizing the losses w.r.t. the peak flux density ΔB we get

$$\frac{dP_{total\ loss}}{d(\Delta B)} = \frac{dP_{core}}{d(\Delta B)} + \frac{dP_{cu}}{d(\Delta B)} = 0\ or\ \frac{dP_{core}}{d(\Delta B)} = -\frac{dP_{cu}}{d(\Delta B)} \tag{3.17}$$

This gives the condition for determining the operating peak flux density for the transformer core. The derivatives of the core power loss and copper loss w.r.t. peak flux density are given as [16, (15.11), and (15.12)]:

$$\frac{dP_{core}}{d(\Delta B)} = \beta K_{fe}(\Delta B)^{(\beta-1)} A_C l_m\,, \qquad \frac{dP_{cu}}{d(\Delta B)} = -2\left(\frac{\rho \vartheta_1^2 I_{rms}^2}{4K_u}\right)\left(\frac{MLT}{W_A A_C^2}\right)(\Delta B)^{-3} \tag{3.18}$$

Substituting the derivative values from (3.18) into (3.17) we get the following expression for the optimum flux density for the core:

$$\Delta B = \left[\frac{\rho \vartheta_1^2 I_{rms}^2}{2K_u}\frac{MLT}{W_A A_c^3 l_m}\frac{1}{\beta K_{fe}}\right]^{\left(\frac{1}{\beta+2}\right)} \tag{3.19}$$

Table 3.2 gives the definition of each of the parameters mentioned in (3.19) and provides the corresponding values for the used case.

Table 3.2: Parameter definition and values required for optimum flux density calculation

Parameter	Definition	Value
ρ	Resistivity of the copper wire	1.724e-6 (Ohm-cm)
ϑ	Volt seconds for the positive half cycle across the transformer	0.005 (V-seconds)
I_{rms}	RMS current through the transformer windings	3 Amps at steady state
MLT	Mean length per turn for the wire	15.24 cm
K_u	Window fill factor	0.5
W_A	Window area for the core	16.1 cm^2
A_c	Cross sectional area of the core	.0013 m^3
l_m	Mean length of the magnetic path	19.04 cm
β	Steinmetz parameter	2.85
K_{fe}	Frequency dependent core material constant	24.7
ΔB	Peak flux value obtained in the central or the peripheral limb	T

Using the values mentioned in table 3.2 in (3.19) the peak flux density for the peripheral windings in the MLC transformer come out as shown in table 3.3. From (3.10) it is now possible to calculate the number of windings in each limb (central and peripheral) also mentioned in table 3.3.

Table 3.3: Peak flux and the number of turns obtained for the central and peripheral limb

	ΔB	N (number of Turns)
Central Limb	0.15 T	25
Peripheral Limb	0.18 T	50

The losses in the magnetic stage of a power converter can be classified into two categories:

- Core loss components
- Copper loss components

3.12.1. Core loss calculations

The core loss is a manifestation of the hysteresis loss of the magnetic core element and is a function of the material, the operating frequency and the peak flux density. The losses in the core can be measured by the Steinmetz equation [26] given by (3.20)

$$P_v = k f^{\alpha} \hat{B}^{\beta} \tag{3.20}$$

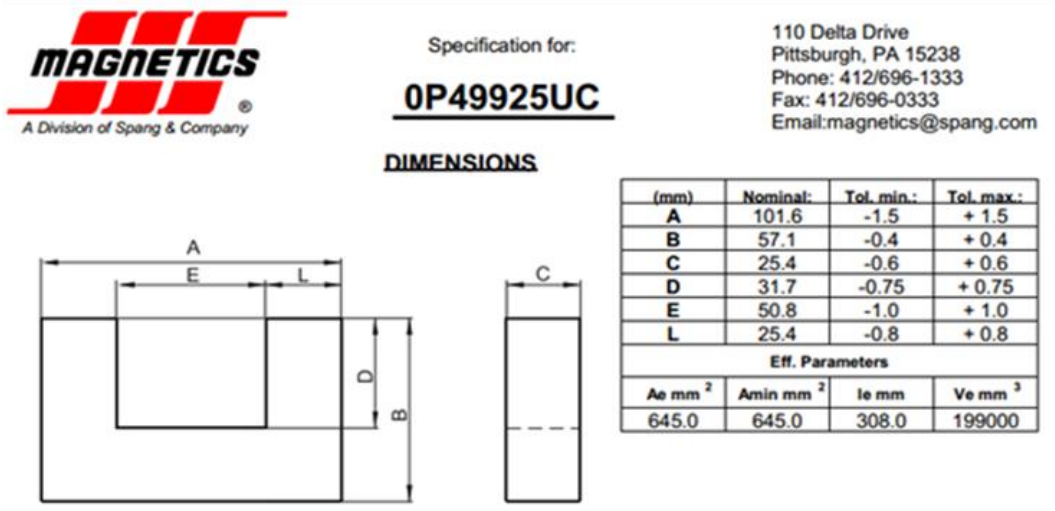
Here P_v is the core loss in mW/cm^3, the parameters *k, α,* and *β* are the Steinmetz parameters that depends on the magnetic material used, *f* is the operating frequency in kHz and $\hat{B}$ is the peak flux density in kG (kilo-Gauss, where 1 Gauss = 10^{-4} T). However, the equation (3.20) is the core loss formula where the excitation voltage is sinusoidal in nature. In case of non-sinusoidal flux waveform the modified Steinmetz equation has been proposed in [26], [27].

$$P_v = \frac{1}{T_s} \int_0^{T_s} k_i \left| \frac{dB}{dt} \right|^{\alpha} (\Delta B)^{\beta - \alpha} dt \tag{3.21}$$

Where the peak to peak flux density is ΔB, T_s is the switching period and k_i is given as (3.22)

$$k_i = \frac{k}{(2\pi)^{\alpha-1}\int_0^{2\pi} |\cos\theta|^{\alpha} 2^{\beta-\alpha} d\theta} \tag{3.22}$$

The modified Steinmetz equation the parameters *k, α,* and *β* are same as the original Steinmetz equation (3.21). The power loss per unit volume will be given by the equation (3.22) which needs to be multiplied by the total core volume to give the total power loss in the core. The core used in this application is a ferrite core part number: 0P49925UC from Magnetics-inc shown in Fig 3.25.



(mm)	Nominal:	Tol. min.:	Tol. max.:
A	101.6	-1.5	+ 1.5
B	57.1	-0.4	+ 0.4
C	25.4	-0.6	+ 0.6
D	31.7	-0.75	+ 0.75
E	50.8	-1.0	+ 1.0
L	25.4	-0.8	+ 0.8

Eff. Parameters			
Ae mm ^{2}	Amin mm ^{2}	le mm	Ve mm ^{3}
645.0	645.0	308.0	199000

Figure 3.25: Core dimensions for the used core 0P49925UC (source: www.mag-inc.com)

The Steinmetz parameters *k, α,* and *β* for the core material (F-type) is given in table 3.4.

Table 3.4: Steinmetz parameters for the ferrite material "F" (source: http://fmtt.com/Coreloss2009.pdf)

Frequency Range	k	α	β
$f \leq 10\ kHz$	0.79	1.06	2.85
$10kHz \leq f \leq 100\ kHz$	0.0717	1.72	2.66
$100kHz \leq f \leq 500\ kHz$	0.0573	1.66	2.68
$f \geq 500\ kHz$	0.0126	1.88	2.29

The volume of a 5-limb MLC transformer is given as shown in table 3.5.

Table 3.5: Core volume data for the MLC transformer

Section	Volume
Peripheral section (C cores, 8 cores in total)	200 cm^3 (each), 1600 cm^3 (total)
Central limb (I-cores, 4 in total)	66 cm^3 (each), 264 cm^3 (total)

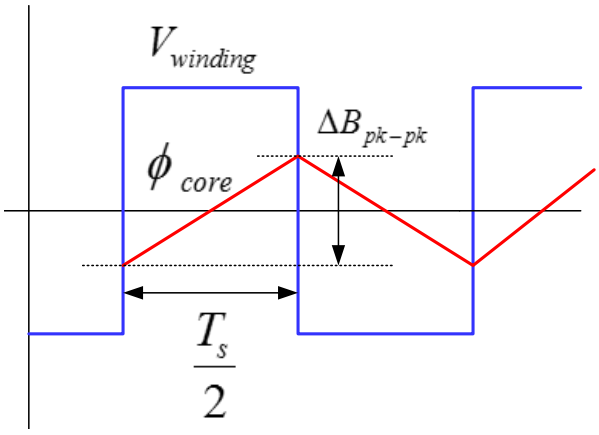


Figure 3.26: The waveform showing the voltage and flux plot in the transformer core

Since the core flux wave shape is non-sinusoidal in nature, the modified Steinmetz equation is used in this case. Since the transformer was designed with a peak flux density of 0.15T, the

peak to peak ΔB in (3.21) is 0.3T. Since the flux wave shape is triangular, the $^{dB}/_{dt}$ is a constant and equals to $^{0.3}/_{(0.5 * T_s)}$ where for a 10 kHz system T_s = 0.0001. Using the Steinmetz parameters from table 3.2, k_i is calculated as 0.0511 using (3.22). Using the information from table 3.3 the core loss was found to be minimum with central winding number of turns as 50 and peripheral winding number of turns 50. Thus the power loss per unit volume is calculated as per (3.21) which comes out as 14.8 mW/ cm^3 for the central limb and 4.6 mW/ cm^3 for the peripheral limbs. Multiplying the volume with the core loss per unit volume, the total core loss comes out as 11.39 W for a 1kW system. For a similar rated SLC based topology, the volume breakdown is shown in table 3.6.

Table 3.6: Core volume data for the SLC transformer

Section	Volume
Peripheral section (C cores, 8 cores in total)	200cm^3 (each), 1600 cm^3 (total)
Central limb (I-cores, 8 in total)	66 cm^3 (each), 528 cm^3 (total)

Therefore the total volume of the SLC based topology is 2128 cm^3. The power per unit volume for the SLC topology is 4.67 mW/ cm^3. Thus the total core loss for the SLC based topology is 9.93 W for a 1 kW system.

Table 3.7: Core loss data for the MLC and the SLC transformers

Total System rating	Core Loss in MLC	Core Loss in SLC
1000W	11.39W	9.93W

3.12.2 Copper loss calculations

The copper losses are a direct function of the r.m.s. current flowing through the windings. The copper used in the MLC transformer with the core mentioned before is a function of the number of turns used and the perimeter of the core. The net copper loss is given by:

$$P_{cu} = I_{rms}^2 R_{AC} \tag{3.23}$$

Where I_{rms} is the r.m.s. current through the transformer windings.

Table 3.8: Table showing the total resistance of the windings for the MLC transformer with 50 turns both on peripheral winding and 50 turns on the central winding

Length of copper used (cm)	Resistance (mOhms) per cm	Total winding resistance (Ohms)
3048 (peripheral) + 1016 (central)	0.311	1.26

7	42	43.75	33½	237.00	.009	7341	.136	.009	7179	.139	.011	6570	.152
8	42	50.00	33	207.38	.009	6423	.156	.010	6281	.159	.011	5794	.173
9	42	56.25	32½	184.33	.010	5710	.175	.010	5583	.179	.012	5168	.193
10	42	62.50	32	165.90	.010	5139	.195	.011	5025	.199	.012	4671	.214
15	42	93.75	30½	110.60	.013	3426	.292	.013	3350	.299	.015	3166	.316
20	42	125.00	29	82.95	.015	2569	.389	.016	2513	.398	.017	2399	.417
25	42	156.25	28	66.36	.016	2055	.487	.017	2010	.498	.018	1928	.519
30	42	187.50	27½	55.30	.018	1713	.584	.019	1675	.597	.020	1615	.619
40	42	250.00	26	41.48	.021	1285	.778	.022	1256	.796	.023	1223	.818
50	42	312.50	25	33.18	.023	1028	.973	.025	1005	.995	.025	985	1.02
60	42	375.00	24½	27.65	.025	856	1.17	.027	838	1.19	.027	822	1.22
75	42	468.75	23½	22.12	.028	685	1.46	.030	670	1.49	.030	659	1.52
100	42	625.00	22	16.59	.032	514	1.95	.035	503	1.99	.035	496	2.02
125	42	781.25	21	13.27	.036	411	2.43	.039	402	2.49	.038	398	2.51
150	42	937.50	20½	11.06	.040	343	2.92	.042	335	2.99	.042	333	3.00
175	42	1093.75	19½	9.48	.043	294	3.40	.046	287	3.48	.045	286	3.50
3	43	14.52	38½	714.33	.005	21533	.0464	.005	20964	.0477	.007	17614	.0568
4	43	19.36	37	535.75	.006	16150	.0619	.006	15723	.0638	.008	13598	.0735
5	43	24.20	36	428.60	.007	12920	.0774	.007	12579	.0795	.009	11072	.0903
6	43	29.04	35½	357.17	.007	10767	.0929	.008	10482	.0954	.009	9378	.107
10	43	48.40	33	214.30	.009	6460	.155	.010	6289	.159	.011	5814	.172
20	43	96.80	30	107.15	.013	3230	.310	.014	3145	.318	.015	2991	.334
30	43	145.20	28½	71.43	.016	2153	.464	.017	2096	.477	.018	2015	.496
60	43	290.40	25½	35.72	.022	1077	.929	.024	1048	.954	.025	1032	.969
100	43	484.00	23	21.43	.029	646	1.55	.031	629	1.59	.031	621	1.61
150	43	726.00	21½	14.29	.035	431	2.32	.038	419	2.39	.038	417	2.40
3	44	12.00	39	864.33	.004	27034	.0370	.005	26247	.0381	.007	21303	.0469
4	44	16.00	38	648.25	.005	20276	.0493	.006	19685	.0508	.007	16748	.0597
5	44	20.00	37	518.60	.006	16221	.0616	.007	15748	.0635	.008	13691	.0730

Figure 3.27: The data sheet for the used Litz wire for the transformer winding (source: http://www.mwswire.com/pdf_files/mws_tech_book/page16_17_18_19.pdf)

The current can be expressed in the following equation as [9: (6.6),(6.7)] follows.

$$i(\omega t = 0) = -\frac{V_{in}}{2\omega L}\left[\left(1 - \frac{V_{out}}{V_{in}}\right)(\pi - \varphi) + \left(1 + \frac{V_{out}}{V_{in}}\right)\varphi\right] \tag{3.24}$$

$$i(\omega t = \varphi) = \frac{V_{in}}{2\omega L}\left[\left(1 + \frac{V_{out}}{V_{in}}\right)\varphi + \left(1 + \frac{V_{out}}{V_{in}}\right)(\pi - \varphi)\right] \tag{3.25}$$

From (3.24) and (3.25) the r.m.s. current in the peripheral winding and the central winding can be calculated. The r.m.s. current obtained for the used case MLC-DAB system at rated condition is shown in table 3.9.

Table 3.9: R.M.S. current through the central and peripheral winding of the MLC-DAB at rated condition

r.m.s. current (central limb)Amps	r.m.s. current (peripheral limb)Amps
2.6 Amps	2.6 Amps

Hence the total copper loss using the resistance values from table 3.8 and the r.m.s. current value in table 3.9 has been calculated as 8.5 W. For a similar rated series connected core topology the total copper loss can be calculated using the resistance value from table 3.10 and the r.m.s. current value of 2.6 Amps as 12.8 W.

Table 3.10: Table showing the winding resistance for the series connected core transformer

Length of copper used (cm)	Resistance ($mOhms$) per cm	Total winding resistance (Ohms)
6096	0.311	1.9

Table 3.11: Total loss for a 1 KW system in the MLC and the series connected case

Topology	Core Loss (W)	Copper Loss (W)	Total Loss (W)
MLC topology	11.4	8.544	19.94
Series connected topology	10	12.8	32.8

Table 3.11 shows the comparative loss values for the MLC DAB and the series connected transformer topology with a significant gain in copper loss for the MLC -DAB.

3.13. Proximity effect in the windings

The mutual inductances between the primaries have been neglected in the analysis so far. But with the increase in the number of peripheral limbs the effect of the mutual inductances become more important as the peripheral limbs come close to each other spatially (Fig.3.28). An equivalent electrical model for the magnetic stage of the transformer is shown in Fig. 3.29 along with the coupling capacitors that model the mutual inductances of the neighboring peripheral limbs. The flux linked with the limb PL_1 is λ_1, the mutual inductance between PL_1 and PL_2 and PL_4 are L_{12} and L_{14}. The self-inductance (leakage inductance) of the coil is L_1. The current in the limb 1 winding is i_1, in limb 2 is i_2 and in limb 4, i_4. The voltage equation comes out as follows (3.26):

$$\lambda_{L1} = L_1 i_1 + L_{14} i_4 + L_{12} i_2 \, , v_1 = i_1 R_1 + d\lambda_{L1}/dt \tag{3.26}$$

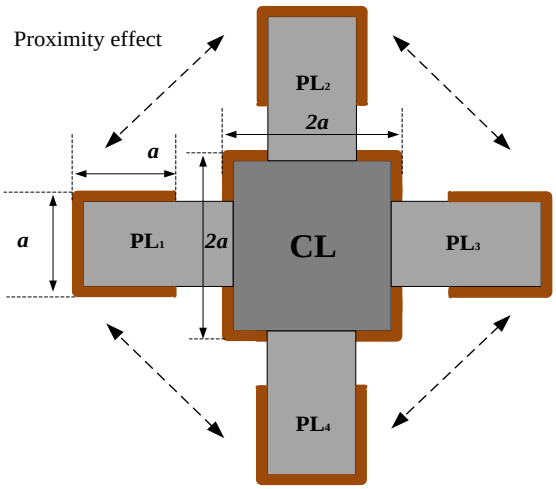


Figure 3.28: Top view of the five limb core MLC topology

Thus the limb 1 voltage v_1 is dependent on the mutual inductances between the neighboring limbs. The mutual inductances increase with the limbs coming closer. The coupling capacitors appearing in a five limb core is shown in the Fig. 3.29. For limb PL_1 and PL_2 the coupling capacitor is C_{12}, between PL_4 and PL_1 it is C_{14} and so on. The coupling is only considered for the spatially close limbs. No coupling is assumed between the limbs PL_1 and PL_3. Since the motivation behind the MLC configuration is the decoupling of the individual primaries, this mutual coupling is a disadvantage.

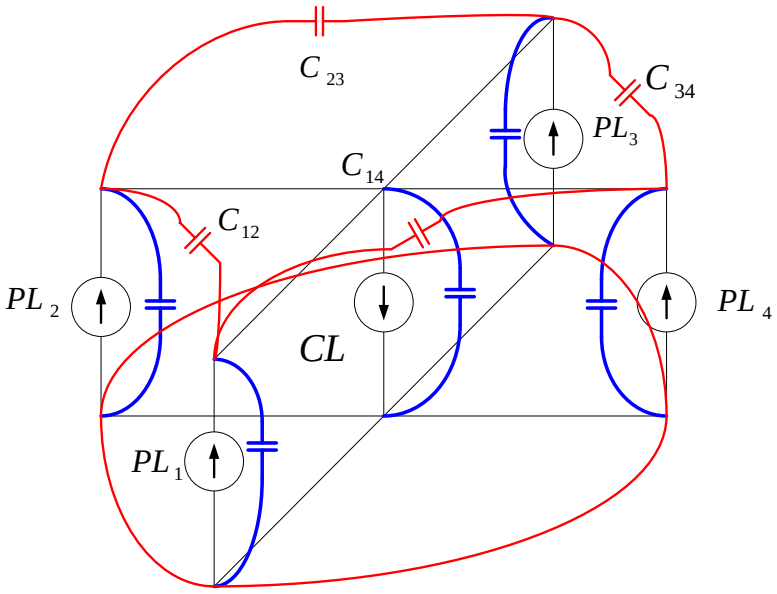


Figure 3.29: Electrical equivalent circuit of the MLC topology with the capacitors

3.14. Power flow equations in the MLC topology

The power flow equations can be derived from the equivalent circuit of the MLC converter. Again the three limb core is used for simplification. Similar analysis is valid for a five limb core model.

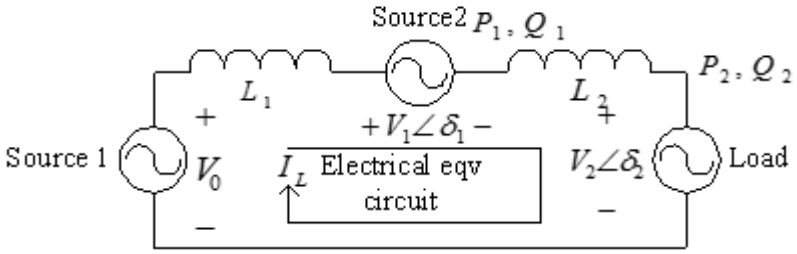


Figure 3.30: Electrical equivalent circuit of the three limb core topology with two source and one load

The equivalent circuit for the three limb core is shown in Fig. 3.30. V_o & V_1 are the primary voltages while V_2 is the secondary voltage, and $L_1 + L_2$ is the lumped sum of the winding inductances all three taken together. The current in the circuit can be derived as (3.27):

$$I_L = \frac{V_0 + V_1\angle\delta_1 + V_2\angle\delta_2}{j\omega L} \tag{3.27}$$

$$P_1 = \frac{V_1 V_2 \sin(\delta_2 - \delta_1)}{\omega L} - \frac{V_o V_1 \sin\delta_1}{\omega L}\bigg|_{\delta_1=0} = -\frac{V_1 V_2 \sin(\delta_2)}{\omega L} \tag{3.28}$$

$$P_2 = \frac{V_1 V_2 \sin(\delta_1 - \delta_2)}{\omega L} - \frac{V_o V_2 \sin \delta_2}{\omega L}\bigg|_{\delta_1=0} = -\frac{(V_1 + V_0) V_2 \sin(\delta_2)}{\omega L} \tag{3.29}$$

P_1 is the power injected by source 2 to the load and P_2 is the summation of power injected by source 1 & 2 to the load. In the derivation δ_1 (relative phase shift between source 1 & 2) is made zero. Thus, both the two sources are in same phase which reduces real power flow between the primaries. Power flow between the primaries and the secondary hence depends solely on the secondary phase angle δ_2.The power angle graph is given in Fig. 3.37 based on (3.28) and (3.29). The maximum is at $\delta_2 = \frac{\pi}{2}$. Similar argument can be extended to the five limb core topology. Provided all the primary bridges are in phase, the power angle curve will be similar as that in Fig. 3.27.

3.15. A small signal model for the MLC-based DAB converter for analyzing the parameter sensitivity

The electrical equivalent circuit for the MLC based DAB topology is shown in Fig. 3.32. Since the primary sources are connected in series and the same current (winding current) flows through all the sources, the MLC based DAB topology can be simplifies to a simple DAB topology to study the system dynamics and derive the small signal model. The small signal model for a single phase DAB has been derived in [9]. The small signal model and the transfer functions for the MLC based DAB is derived based on the single phase DAB. Identifying the state variables as the output capacitor voltage and the inductor current, the state space equations for the average model of the DAB [9,(6.17)] is given in (3.30).

$$\begin{bmatrix} \dot{I} \\ \dot{V} \end{bmatrix} = \begin{bmatrix} 0 & \frac{2k_1 - 1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} I \\ V \end{bmatrix} + \begin{bmatrix} \frac{2k - 1}{L} \\ 0 \end{bmatrix} V_{in} \tag{3.30}$$

The expression k_1 and k can be expressed [9, (6.13), (6.14)] as per (3.31)

$$k_1 = \frac{2\varphi + (\frac{V_{out}}{V_{in}} - 1)\pi}{4\pi(1 + \frac{V_{out}}{V_{in}})} \; and \; k = k_1 + \frac{1}{2}\left(1 - \frac{\varphi}{\pi}\right) \tag{3.31}$$

In (3.30) L is the leakage inductance of the transformer, C is the output capacitor, R is the load, I is the leakage inductor current or the winding current and V is the output capacitor voltage. Linearizing the average model provides the small signal model [9, (6.18)-(6.21)].

$$\begin{bmatrix} \frac{d\tilde{I}}{dt} \\ \frac{d\tilde{V}}{dt} \end{bmatrix} = \begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix} \begin{bmatrix} \tilde{I} \\ \tilde{V} \end{bmatrix} + \begin{bmatrix} B_{11} \\ 0 \end{bmatrix} \widetilde{V_{in}} + \begin{bmatrix} E_{11} \\ 0 \end{bmatrix} \tilde{\varphi} \tag{3.32}$$

$$A_{11} = -\frac{2V_{in0}}{T_s(V_{in0} + V_0)} \tag{3.33}$$

$$A_{12} = \frac{1}{2}\left(\frac{V_{in0}T_s\big((\varphi_0 - 3\pi)V_{in0} - 2V_0\pi\big) + 4\pi LI_0V_{in0} - \pi T_sV_0^2}{\pi T_sL(V_{in0} + V_0)^2}\right) \tag{3.34}$$

$$B_{11} = \frac{V_0(T_s\varphi_0V_0 - 2\pi LI_0) + \pi T_sV_{in0}(V_{in0} + 2V_0)}{\pi T_sL(V_{in0} + V_0)^2} \tag{3.35}$$

$$E_{11} = \frac{V_0}{\pi L\left(\frac{V_0}{V_{in0}} + 1\right)} \tag{3.36}$$

For the used case transformer the parameters and their values are provided in table 3.8. The control to output transfer function can now be derived [9, (6.22) – (6.25)] as shown.

$$G_{vd}(s) = \frac{\tilde{I}(s)}{\widetilde{\varphi(s)}}\Bigg|_{\widetilde{u(s)}=0} \tag{3.37}$$

$$G_{vd}(s) = \frac{Num(s)}{Den(s)} \tag{3.38}$$

Table 3.12: MLC-DAB converter parameters

Parameters	Value	Representation
V_{in0}	400V	Steady State input voltage
V_0	400V	Steady State output voltage
φ_0	$\frac{\pi}{6}$	Steady State Power angle
L	0.7 mH	Lumped leakage inductance of the transformer
I_0	2.5 Amp	Average inductor current over one switching half-cycle
T_s	100µs	Switching period

Where $Num(s)$ and $Den(s)$ are the numerator and denominator of the transfer function.

$$Num(s) = \frac{E_{11}}{C} \tag{3.39}$$

$$Den(s) = s^2 + s\left(\frac{1}{RC} - A_{11}\right) - \frac{A_{11}}{RC} - \frac{A_{12}}{C} \tag{3.40}$$

3.16.1. Transformer leakage inductor sensitivity analysis for open loop system

The transfer function $G_{vd}(s)$ is dependent on the value of the inductor (leakage inductance) of the transformer, since the parameter A_{12} in the denominator is a function of the leakage inductance. Fig. 3.31 shows the bode plot of the transfer $G_{vd}(s)$ showing the change in the phase margin of the open loop system with the change in the leakage inductance of the transformer. Table 3.13 shows the trend variation of the phase margin with the leakage inductance.

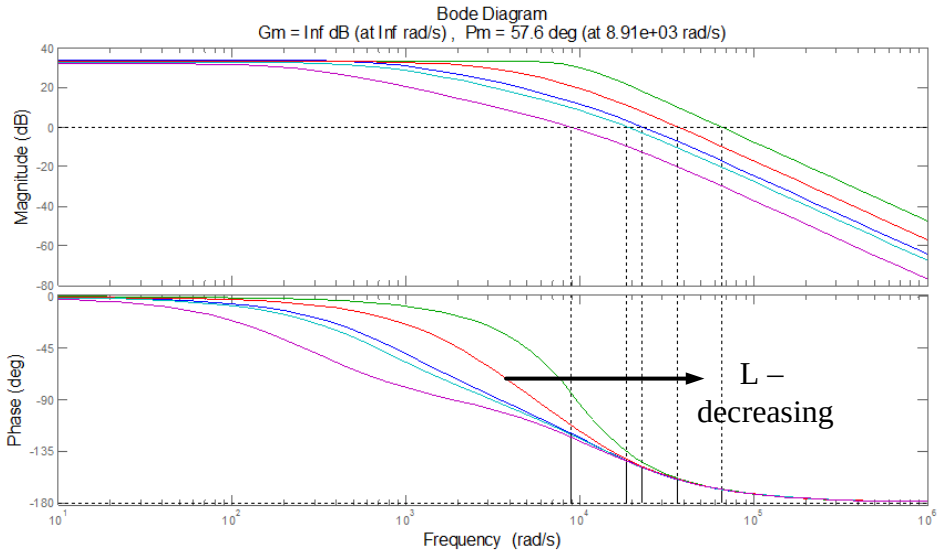


Figure 3.31: Bode plot for the control to output transfer function $G_{vd}(s)$ showing the variation in phase margin with leakage inductance

The denominator of the transfer function (3.34) can be written as

$$Den(s) = s^2 + Bs - C \tag{3.41}$$

Where B and C are:

$B = \frac{1}{RC} - A_{11}$, $C = \left[\frac{A_{11}}{RC} + \frac{A_{12}}{C}\right]$. Thus only C is a function of the leakage inductance. The poles $p_{G_{vd}}$ of the transfer function are therefore,

$$p_{G_{vd}} = -\frac{B}{2} \pm \sqrt{\frac{B^2}{4} + C} \tag{3.42}$$

Now to obtain the sensitivity of the poles with the variation in L, (3.42) is partially differentiated w.r.t. L.

$$\frac{\partial p_{G_{vd}}}{\partial L} = \frac{\partial\left[-\frac{B}{2} \pm \sqrt{\frac{B^2}{4} + C}\right]}{\partial L} = \frac{\partial\left[\sqrt{\frac{B^2}{4} + C}\right]}{\partial L} = 0 \tag{3.43}$$

This criterion leads to

$$\frac{\partial C}{\partial L} = 0 \; substituting, \frac{\partial A_{12}}{\partial L} = 0 \tag{3.44}$$

This leads to the following criterion

$$V_{in0}T_s\big((\varphi_0 - 3\pi)V_{in0} - 2V_0\pi\big) - \pi T_s V_0^2 = 0$$

Substituting $V_0 = mV_{in0}$, we get

$$\varphi_0 = \pi(m+1)^2 + 2\pi \tag{3.45}$$

However since $\max(\varphi_0) = \frac{\pi}{2}$ hence clearly (3.45) is invalid, which proves that the open loop system cannot be made insensitive of L.

Table 3.13: Leakage inductance dependence on the system stability

Leakage inductance	Phase margin	Settling time	Percentage Overshoot
0.1 mH	11.9 ^{o}	0.8msec	11%
0.3 mH	20.4 ^{o}	1.8msec	0
0.7 mH	30.7 ^{o}	5msec	0
1mH	36.3 ^{o}	7msec	0
3mH	57.6 ^{o}	22.5msec	0

In the following subsection an inner current loop controller design is presented that improves the operation of the close loop system with the variation of L.

3.16.2. Design of a Compensator for improving the variation in stability due to variation in L

In the previous section it was shown that the open loop system is sensitive of L. The variation in L has an impact on the system stability (table 3.13). In this section a control method is proposed that improves the system stability by improving the gain margin with the variation in L. The closed loop poles of the system is shown in equation (3.42). Since the poles are function of the L, variation in L will affect the variation in the pole location and hence the system stability. Since the poles occur in conjugate pair with one pole closer to the origin while the other further away, the pole closer to the origin will have a greater effect on the system stability. This provided the motivation of implementing a compensator that cancels the dominant pole closer to the origin with its zero. Fig 3.32 shows the proposed controller.

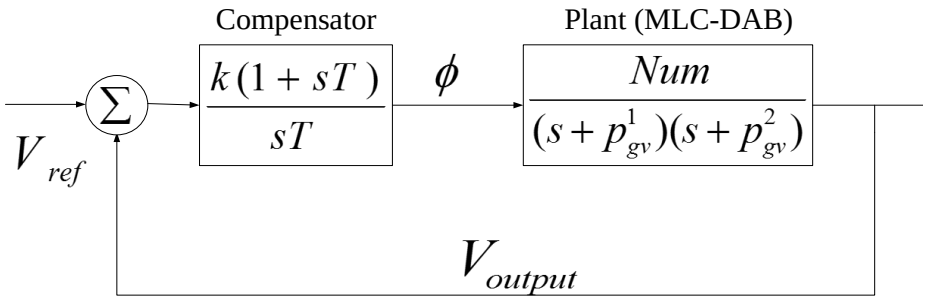


Figure 3.32: Compensator designed to compensate for the variation in L

The controller parameter can be designed by identifying the pole closer to the origin.

$$T = \frac{1}{p_{gv}^1}, if\ p_{gv}^1 < p_{gv}^2 \tag{3.46}$$

the compensator transfer function $Comp(s)$ with the above design is as:

$$Comp(s) = .05\left[\frac{1 + {}^{s}/_{1200}}{{}^{s}/_{1200}}\right] \tag{3.47}$$

The variation in L and the consequent effect on the controller stability is shown with the example case in Fig. 3.35. The phase margin variation is shown in table 3.14.

Table 3.14: Table showing the phase margin w.r.t change in L

Leakage Inductance (mH)	Phase Margin(degrees)
3	53.6
1	78.5
.7	86.8
.5	93.7
.1	111

The sensitivity coefficient of the open loop and closed loop transfer function are calculated in the following section.

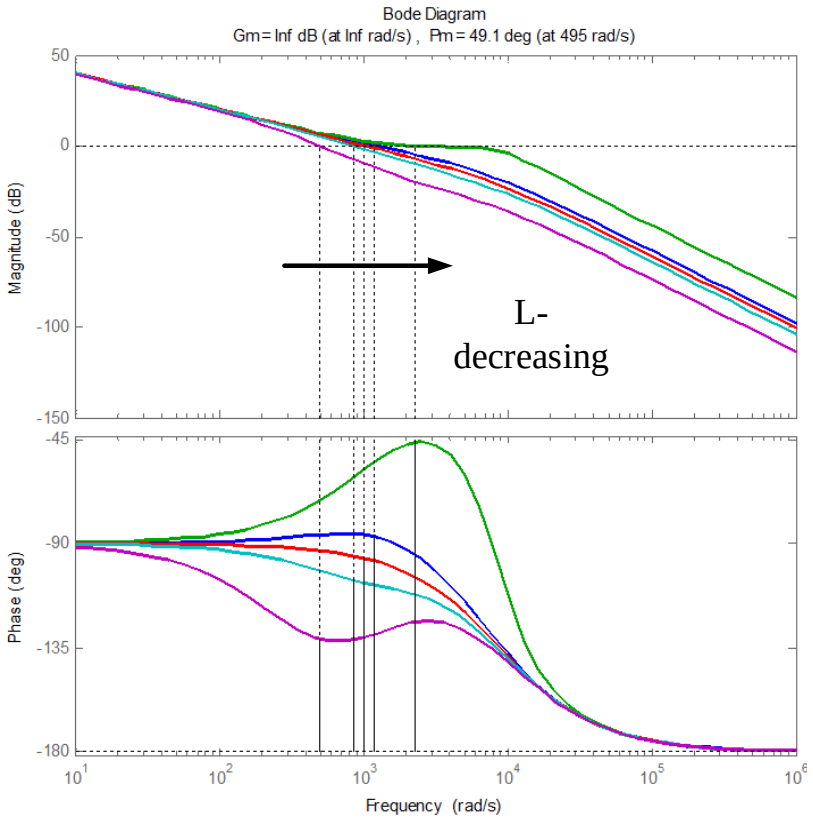


Figure 3.33: Variation of the phase margin and stability of the closed loop system with the compensator with the variation in the leakage inductance (L) of the transformer.

3.16.3. Evaluation of transfer function sensitivity coefficient:

The transfer function sensitivity coefficient w.r.t. change in L for the open loop system is represented as follows:

$$S_{ol} = \frac{\frac{\partial G_{vd}}{G_{vd}}}{\frac{\partial L}{L}} = \frac{\partial G_{vd}}{\partial L}\frac{L}{G_{vd}} \tag{3.48}$$

Since $G_{vd} = \frac{Num(s)}{Den(s)}$, (3.48) can be simplified as follows:

$$S_{ol} = L\left[\frac{1}{Num}\frac{\partial Num}{\partial L} - \frac{1}{Den}\frac{\partial Den}{\partial L}\right] \tag{3.49}$$

Substituting from (3.48) and (3.49), the open loop sensitivity function can be expressed as follows:

$$S_{ol} = -1 - \frac{L}{Den(s)}\left[\frac{V_{in0}[(\varphi_0 - 3\pi)V_{in0} - 2V_0\pi] - \pi V_0^2}{2C\pi(V_{ino} + V_0)^2}\right] \tag{3.50}$$

The close loop sensitivity coefficient with the changes in the forward transfer function can be evaluated as follows:

$$S_{cl} = \frac{\partial T(s)/T(s)}{\partial G_{vd}(s)/G_{vd}(s)} = \frac{\partial}{\partial G_{vd}(s)}\left[\frac{G_{vd}(s)Comp(s)}{1 + G_{vd}(s)Comp(s)}\right].\frac{G_{vd}(s)}{\left[\frac{G_{vd}(s)Comp(s)}{1 + G_{vd}(s)Comp(s)}\right]}$$

$$= \frac{1}{1 + G_{vd}(s)Comp(s)} \tag{3.51}$$

Where $T(s)$ is the closed loop transfer function, $Comp(s)$ is the compensator transfer function from (3.47), and $G_{vd}(s)$ is the open loop system transfer function from (3.37). The open loop sensitivity coefficient and the closed loop sensitivity coefficient are plotted in Fig. 3.34. With the addition of the compensator the sensitivity coefficient shows better attenuation throughout the frequency range.

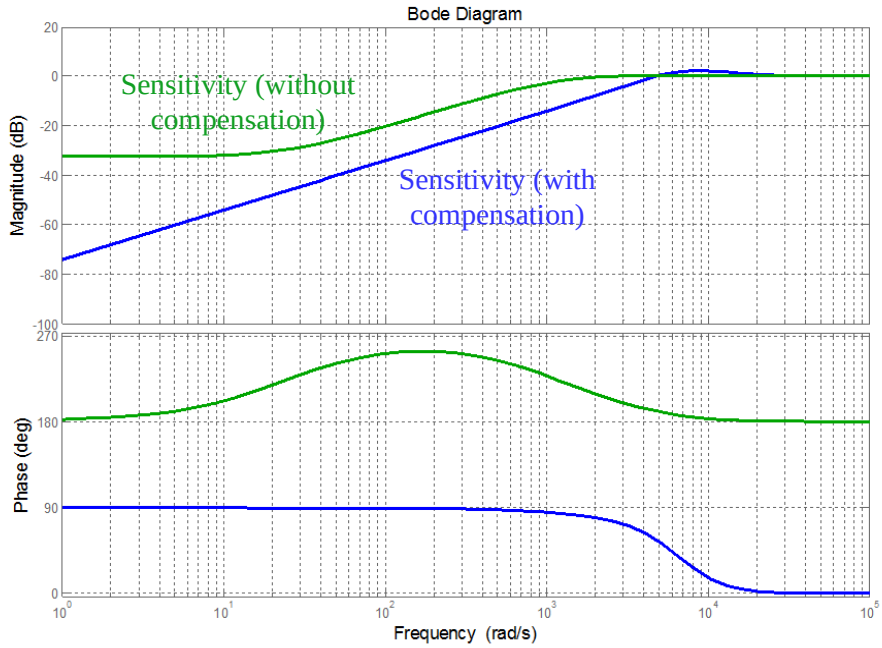


Figure 3.34: Sensitivity coefficient plot for the open loop system (green) and the closed loop system (blue) showing better attenuation of the sensitivity under closed loop operation

3.16.4. Effect of wide variation in input voltage on the converter transfer function

Since the motivation of implementing the MLC-DAB was to integrate RES with fluctuating power profile, it is important to analyze the impact of input voltage swing on the converter source to output transfer function. The source to output transfer function as derived in [9, (6.29)] is given as (3.52).

$$G_{vg}(s) = \frac{\widetilde{V_o}(s)}{\widetilde{V_{ino}}(s)} = \frac{N_{vg}(s)}{Din(s)}, where, N_{vg}(s) = \frac{B_{11}}{C} \tag{3.52}$$

The variation in phase margin of $G_{vg}(s)$ with the variation in input voltage V_{ino} is shown in table 3.15.

Table 3.15: Variation in the phase margin of source to output transfer function with the variation in source voltage

Input Voltage (V)	Phase margin (degrees)
50	87.8
100	133
200	138
400	144
600	152
800	160

From table 3.15 it is clear that with the change in source voltage the system has significant phase margin and hence the system is stable. Fig. 3.35 shows the magnitude and phase plot for the $G_{vg}(s)$ transfer function showing the phase margin under different input voltage conditions. However the variation in the control to output transfer function is more sensitive on the input voltage swing. Table 3.16 shows the variation in phase margin w.r.t. the input voltage variation on the $G_{vd}(s)$. Since the system goes out of stability with the decrease in the input voltage, this provides the motivation for integrating a storage element in the system that provides support during the source voltage fluctuations. The following section discusses the storage (battery) integration and output power (or voltage) regulation algorithm.

Table 3.16: Variation in phase margin for the control to output transfer function

Input Voltage (V)	Phase margin (degrees)
50	9.53
100	18
200	32
400	52
600	64
800	75.1

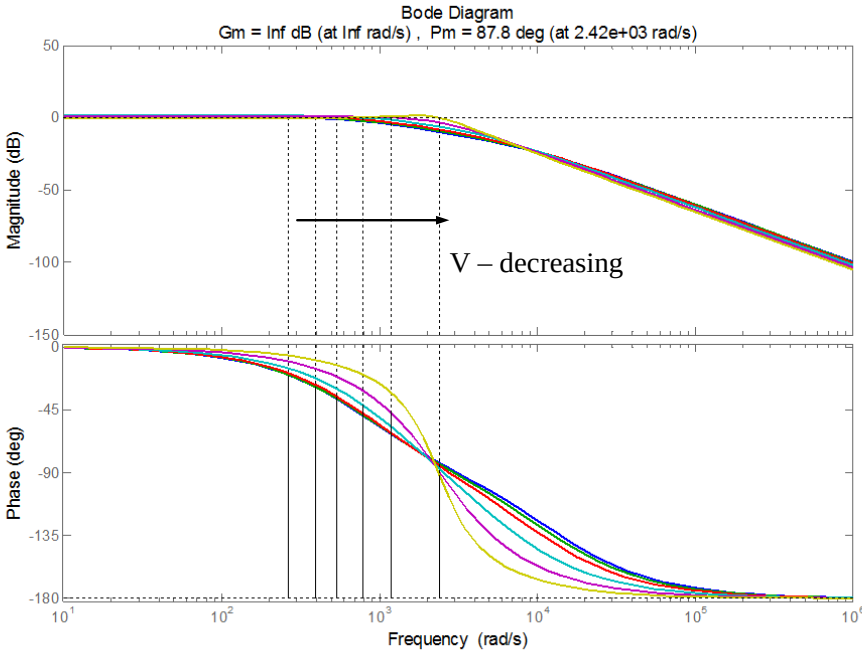


Figure 3.35: The plot of G_{vg} w.r.t. changes in the source voltage showing the stable phase margin

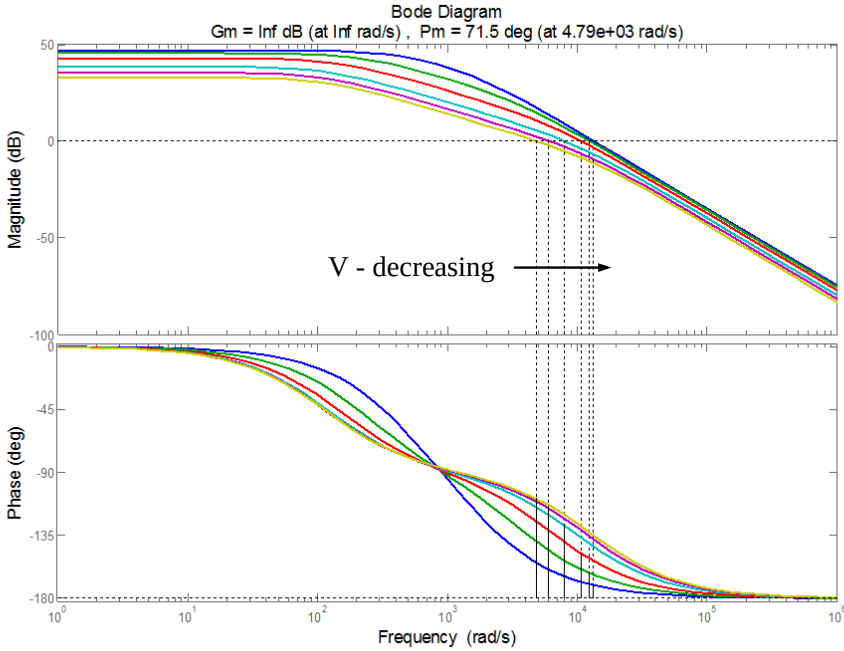


Figure 3.36: Magnitude and phase plot for the variation in control to output transfer function with the variation in input voltage

3.16. Power smoothing algorithm using energy storage:

Since the motivation of implementing the MLC-DAB was to integrate RES with fluctuating power profile, a power smoothening algorithm has been proposed in this section. This algorithm uses a storage element to act as an energy buffer while supplying a regulated load. A five limb core MLC topology was considered and one of the peripheral limbs was connected to a battery bank. Two distinct modes of the converter are defined based on the role played by the battery storage element. The accumulator mode is where the battery acts as a source and the distributor mode is where the battery is charged at a constant current. The secondary phase shift angle δ_2 is observed. If the angle goes below a certain lower threshold then the converter switches over to the distribution mode i.e. the battery is charged. This is achieved by phase lagging the H-bridge connected to the battery with respect to the other primaries. As a result the load increases and the operating power angle increases as well. In the distributor mode if the operating angle keeps on increasing and hit a maximum the controller then switches over to accumulator mode. The battery now supplies the load by syncing up with the other primaries. Thus the converter always operates within the angle$[\varphi_{max}, \varphi_{min}]$. Fig. 3.37 explains the process with respect to the power angle curve. The converter will go into accumulator mode when the battery charging current reaches a maximum value. If a precise control of the charging or the discharging current is needed one might implement the duty cycle modulation for input current control explained in previous sections.

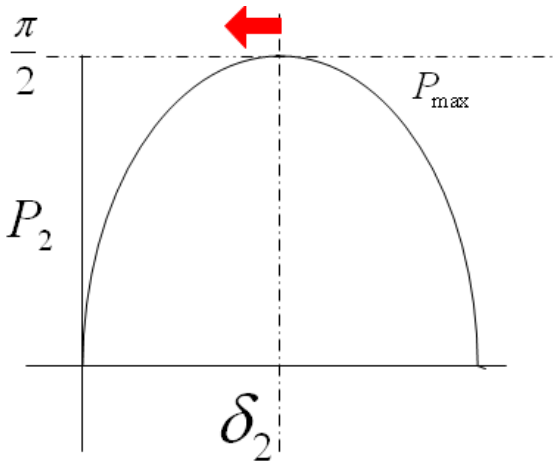


Figure 3.37: Power angle curve for the MLC topology

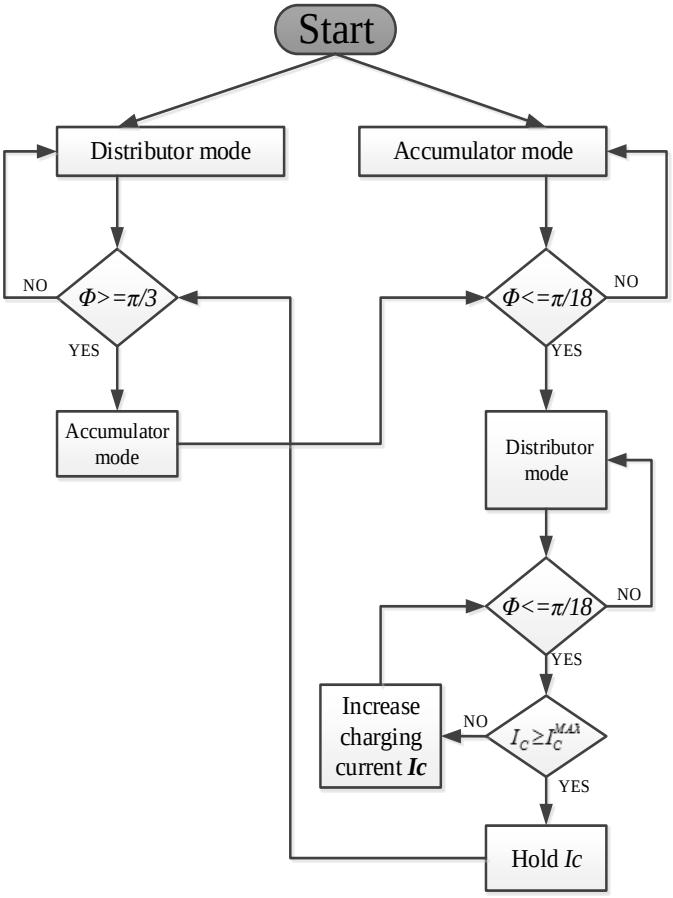


Figure 3.38: Control diagram for the energy management

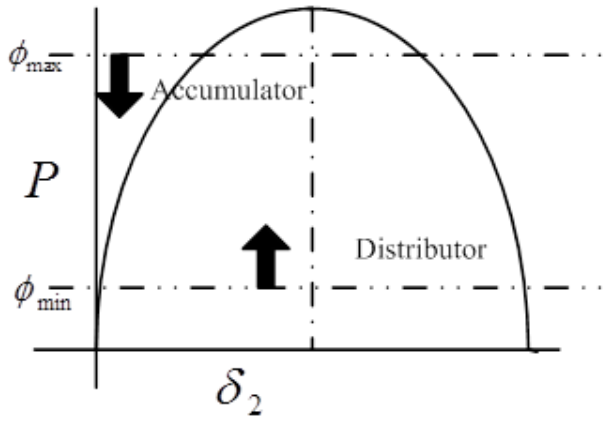


Figure 3.39: Energy management algorithm from the power angle perspective

3.17. Experimental results:

The lab setup is shown in Fig 3.40. The MLC transformer has five limbs; the peripheral limbs are attached to regulated dc power sources. One of the limb is attached to a motor-generator coupled system that implements wave energy with widely varying DC bus voltage. A battery pack is attached to one of the limbs that supplied current when the available power is low and takes in current in case of excess (Fig. 3.41) thus maintaining a regulated dc bus at the output. Figure 3.42 shows the MLC transformer with five limbs. The mechanical structure is three dimensional and hence requires support frames to build. Ferrite was chosen for the core material and litz wires for the winding. Fig. 3.43shows the terminal voltages for the MLC transformer.

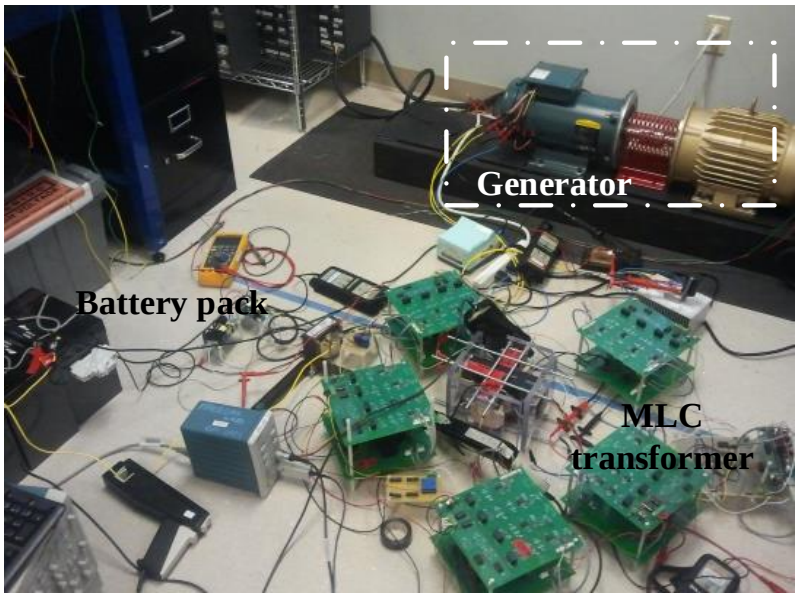


Figure 3.40: Lab setup for the MLC topology with the motor generator setup acting as a wave energy simulator

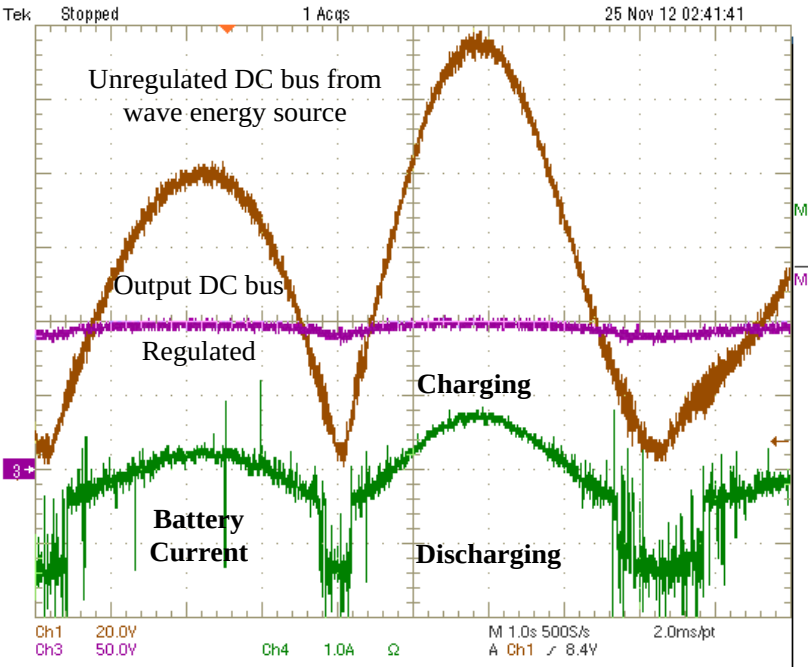


Figure 3.41: Experimental result showing the MLC regulating a DC bus with the wave energy and battery integrated

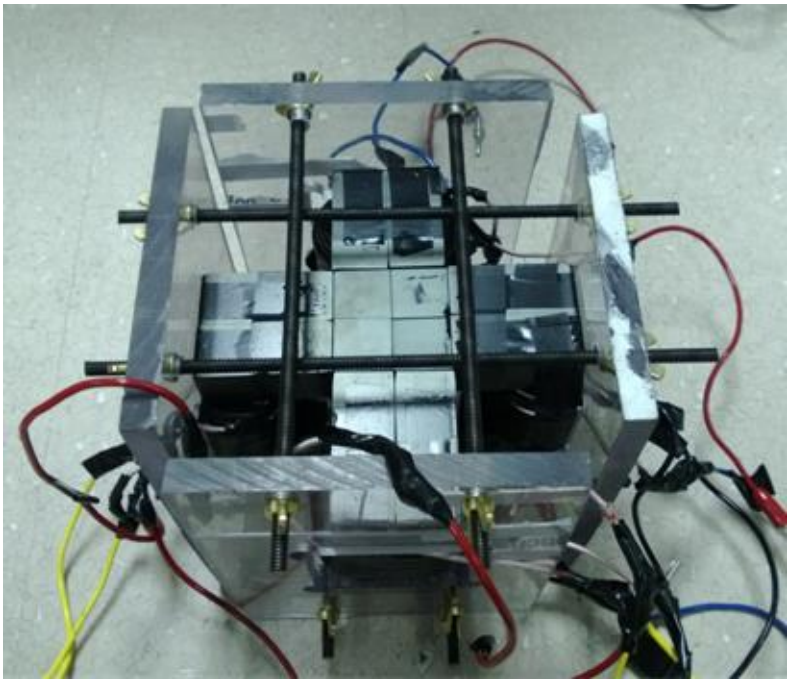


Figure 3.42: The five limb MLC transformer.

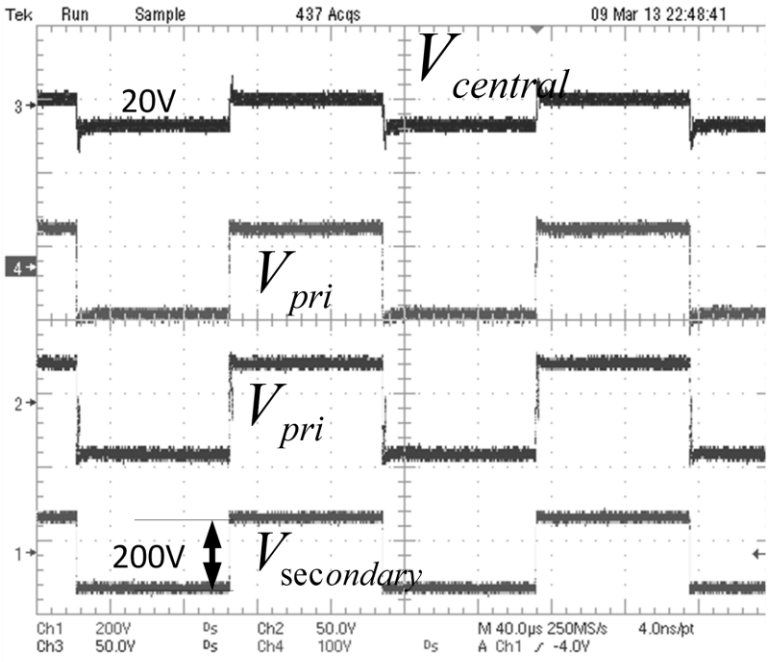


Figure 3.43: Terminal voltage waveforms for the five limb MLC transformer

The input current control operation has been demonstrated with experimental results as shown in Fig. 3.44. Duty cycle modulation was implemented on the primary H-bridges to regulate the current while the input DC bus voltage was changed. The current controller kept the current at the desired set point (one source at 0.8 amps and another at 0.5 amps).

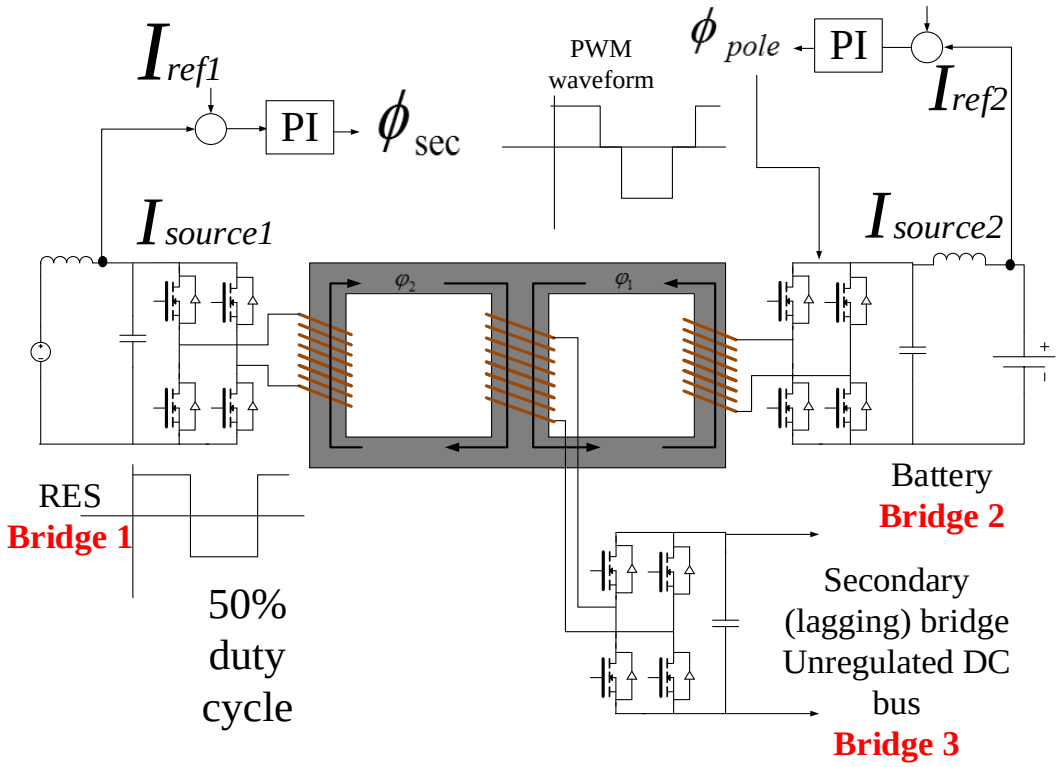


Figure 3.44: Control diagram for the input current control operation on the 3 limb MLC topology

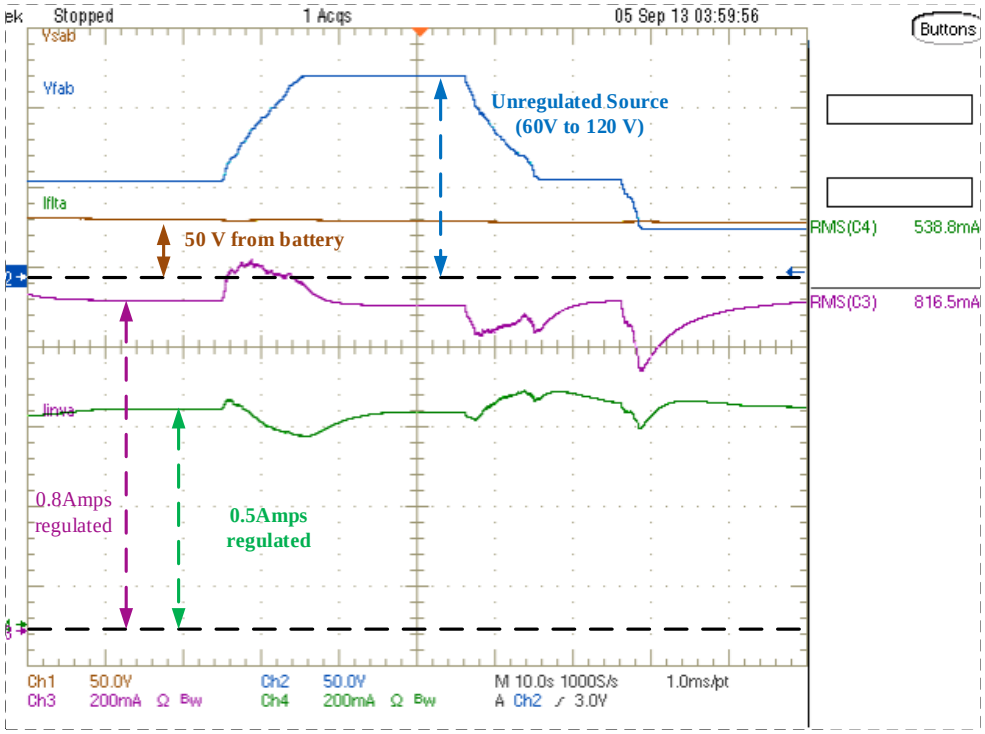


Figure 3.45: Experimental results for the three-limb MLC topology with input current control

3.18. Conclusions

In this chapter a multi-terminal DAB (MLC-DAB) converter topology was developed using a multi-limb core (MLC) transformer. The MLC topology shows an alternate approach to the multi – input single output DC to DC converter system with isolation. The main results obtained in this chapter are summarized as follows:

- In this chapter the MLC transformer based DAB was proposed and the equivalent electrical circuit was developed using the gyrator concept.

- The MLC-DAB topology was shown to utilize reduced copper and magnetic core material compared to an electrically equivalent series connected multi-terminal DAB topology.
- A PWM based input current control was developed to integrate different renewable energy sources operating at different maximum power point.
- A small signal analysis of the MLC-based DAB was done using the DAB small signal as the base model. The sensitivity analysis of the converter dynamics was shown w.r.t. the leakage inductance of the transformer. A controller was implemented to improve the sensitivity of the converter w.r.t. L variations.
- A loss calculation was done for the MLC transformer and compared with the competing series connected transformer topology. In terms of core loss and copper loss the MLC based topology was shown to have lower losses compared to the series connected transformer topology.
- A power smoothing algorithm was proposed. A fluctuating power source and a battery was integrated to supply a regulated load verifying the power smoothening algorithm.

In the next chapter of the dissertation the MLC-DAB has been applied to the solid state transformer topology for grid integration of multiple renewable energy sources.

Chapter 4 The solid state transformer application of the Dual Active Bridge converter

4.1. Introduction

The dual active bridge (DAB) converter and the MLC-DAB converter discussed in the previous chapters find various applications, such as traction, renewable energy integration, etc. One of the application is the DC to DC stage of the Solid State Transformer topology. In this chapter the solid state transformer (SST) application of the MLC-DAB is the main focus of discussion. Instead of the conventional transformer where the magnetic isolation is provided at 60 Hz, the solid state transformer topology proposes the isolation at high frequency [1], [2] reducing the overall size and weight. To obtain high frequency in the SST topology, the 60 Hz AC is rectified through an active front end and converted to DC. The DC to DC stage provides the isolation through the DAB converter. Several different topologies have been proposed for the SST topology with the DAB converter. For higher voltage applications a cascaded front end based topology have been proposed in [2], [21]. For three phase application a three phase front end have been proposed with a three phase DAB stage in [28], [29], [30]. In this chapter is a single phase solid state transformer topology have been considered for the integration of the MLC-DAB as the DC – DC stage. The advantages of integrating the MLC-DAB into the SST topology has been shown compared to DAB integration. A startup algorithm for the SST has been proposed to reduce inrush currents. A parallel MLC-DAB based SST test bed was developed to form a micro-grid and a black start algorithm was implemented to restore power

under islanding. The critical load points were identified within the micro-grid and uninterrupted power flow was demonstrated under islanding.

4.2. Single phase SST cascaded topology

The single phase cascaded SST topology is shown in Fig. 4.1.

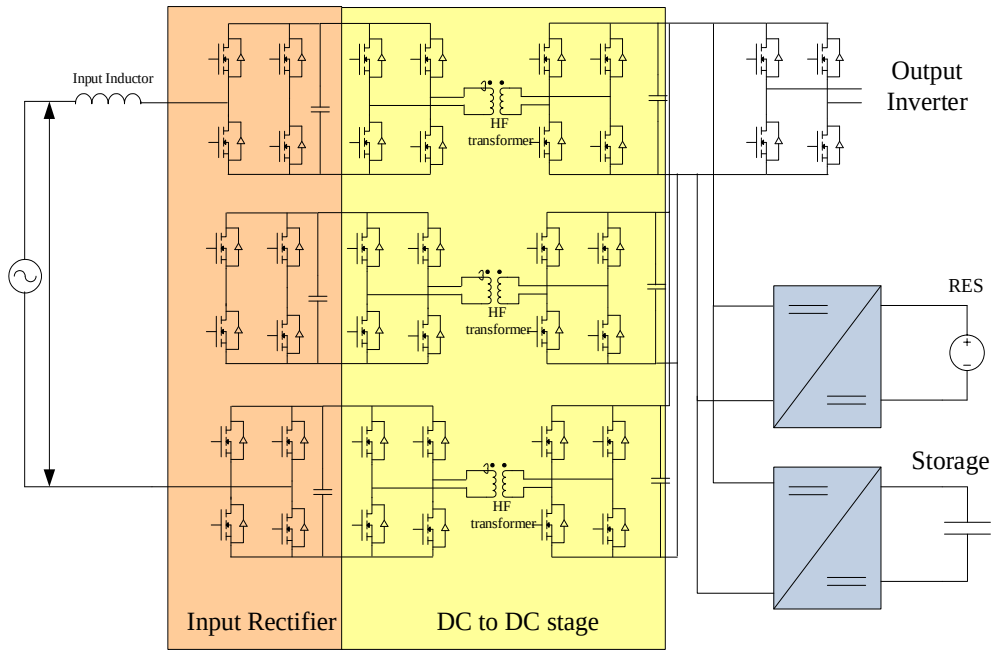


Figure 4.1: Single phase SST topology with cascaded front end and DAB for the DC to DC stages

The cascaded series connected front end converter produces a seven level voltage waveform to block the medium voltage ac bus in the input. This produces three DC buses that need to be balanced. Balancing of the DC buses are assigned both to the input rectifier stage as well as

the DC to DC stage which in this case is the Dual Active Bridge converter. The following section discusses the controls for the front end stage along with the voltage balance control.

4.3. Voltage balance control of the SST

The active front end controls have been extensively discussed in [1] and [31]. Fig. 4.2 shows the block diagram for the control of the front end.

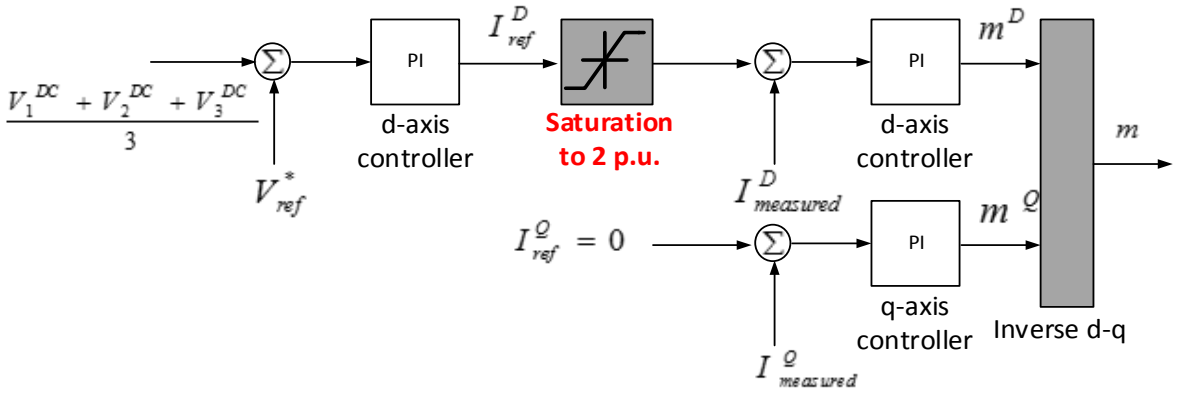


Figure 4.2: Vector Control of the active front end converter

The d-axes control the DC bus of the front end while the q-axes maintain the unity power factor operation. The outer voltage loop maintains the overall DC bus i.e. the sum of the DC bus. For individual DC bus control the additional voltage balance loop is required as shown in Fig. 4.3. This control observes each individual DC buses and adjusts the d-axes modulation required to maintain the balance. The d – axes modulation for the rectifier bridge 1 is given as$(m_d + \Delta m_1)$ for bridge 2 is given as $(m_d + \Delta m_2)$ and for bridge 3 is given as$(m_d - \Delta m_1 - \Delta m_2)$. The

third bridge doesnot have its own controller. In case of voltage sag the power goes below 1 p.u. the buses 1 and 2 maintain the rated voltage while the rest is on bus 3. Considering the voltages are balanced and the output dc bus voltages are gives as *E*. The rectifier terminal voltages are V_1, V_2, V_3 respectively. The power transferred by each bridge are P_1, P_2, P_3 and the modulation index in d-axes is given by m_1, m_2, m_3.

$$V_1 = E(m_1 + jq_1), V_2 = E(m_2 + jq_2), V_3 = E(m_3 + jq_3) \tag{4.1}$$

$$V_1 + V_2 + V_3 = V_{line} - j\omega L I_{line} \tag{4.2}$$

$$P_1 = I_{line} m_1 E\ , P_2 = I_{line} m_2 E\ , P_3 = I_{line} m_3 E \tag{4.3}$$

$$P_1^{DAB} = \frac{V_{in}V_{out}}{\omega L}\varphi_1\left(1 - \frac{\varphi_1}{\pi}\right)\ , P_2^{DAB} = \frac{V_{in}V_{out}}{\omega L}\varphi_2\left(1 - \frac{\varphi_2}{\pi}\right)\ , P_3^{DAB} = \frac{V_{in}V_{out}}{\omega L}\varphi_3\left(1 - \frac{\varphi_3}{\pi}\right) \tag{4.4}$$

The power transferred by DAB are given by (4.4) where $P_1^{DAB}, P_2^{DAB}\ and\ P_3^{DAB}$ are the power transferred by the DAB with leakage $L_1, L_2$and L_3. Under voltage sag when $P_{in} = P_{nominal}$ the power transferred by each DAB is one third of $P_{nominal}$. Under these situation no further control modifications is not required on the DAB side. If however under voltage sag $P_{in} < P_{nominal}$ in that case the $P_1^{DAB} = P_2^{DAB} = \frac{1}{3}P_{nominal}$ and $P_3^{DAB} = P_{in} - \frac{2}{3}P_{nominal}$. Depending on how much severe the voltage sag is the power transferred by the third DAB maybe zero. The phase shift angles are under such circumstances $\varphi_1 = \varphi_2 = \varphi_3 = \frac{\pi}{2}$. Since DAB1 and DAB 2 has input buses with voltage in them will transfer maximum power and will be heavily loaded. The

current through them will be the maximum. Since the voltage in input bus for DAB3 is below nominal rated value, DAB3 will be under rated load. This is not a desirable condition. We need the DAB to be equally balanced. Hence to avoid this condition, under severe voltage sag the rectifier output DC buses need to be brought down to a value that all the three buses can be balanced. Figure 4.7 shows the rectifier buses balance out even after 0.3 p.u. voltage sag by reducing the reference voltage to 0.6 p.u. This affects the DAB as the currents are now balanced and the power sharing is equal.

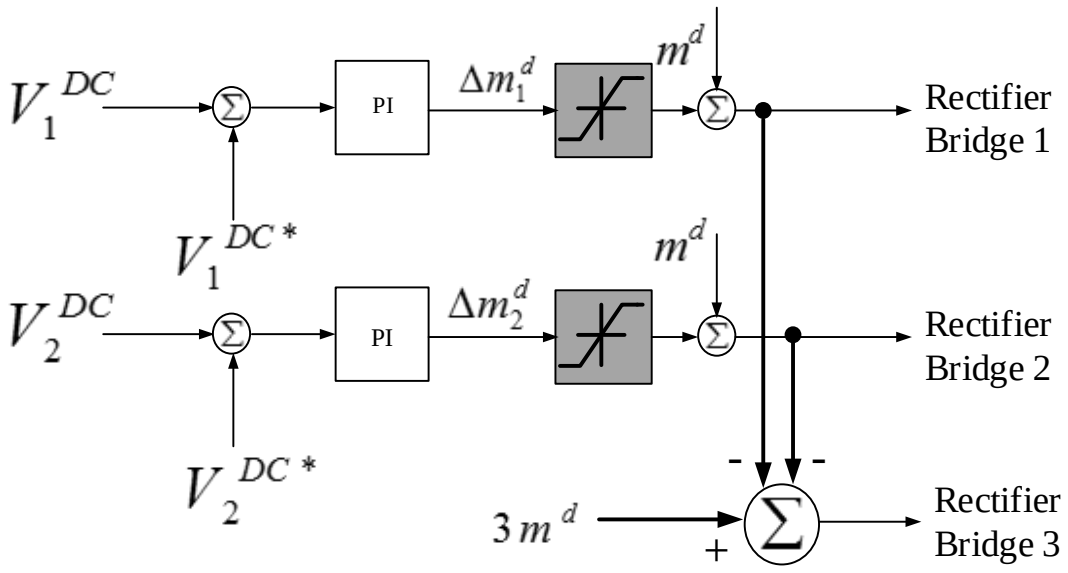


Figure 4.3: DC voltage balance control for the front end

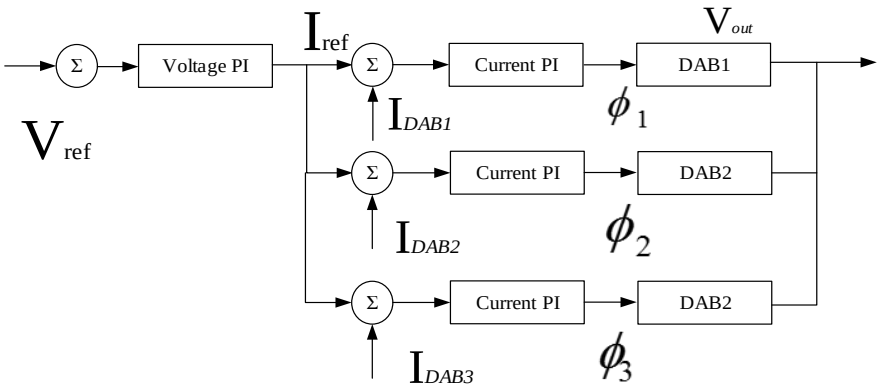


Figure 4.4: Power balance in the DAB stage

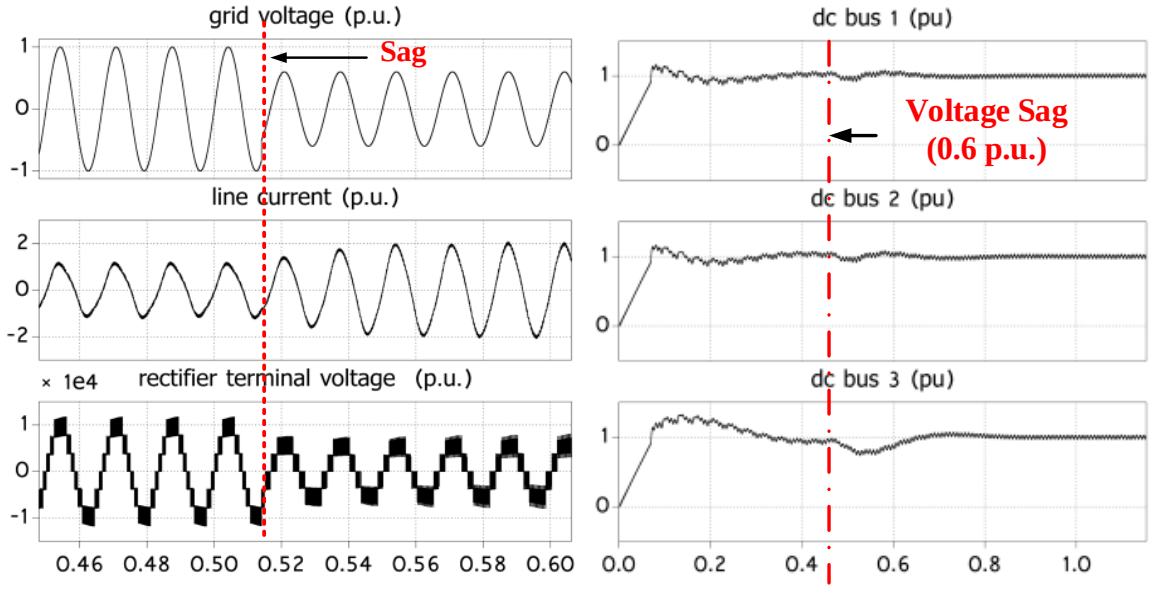


Figure 4.5: Simulation results with a voltage sag of 0.6 p.u. with the DC bus regulation intact

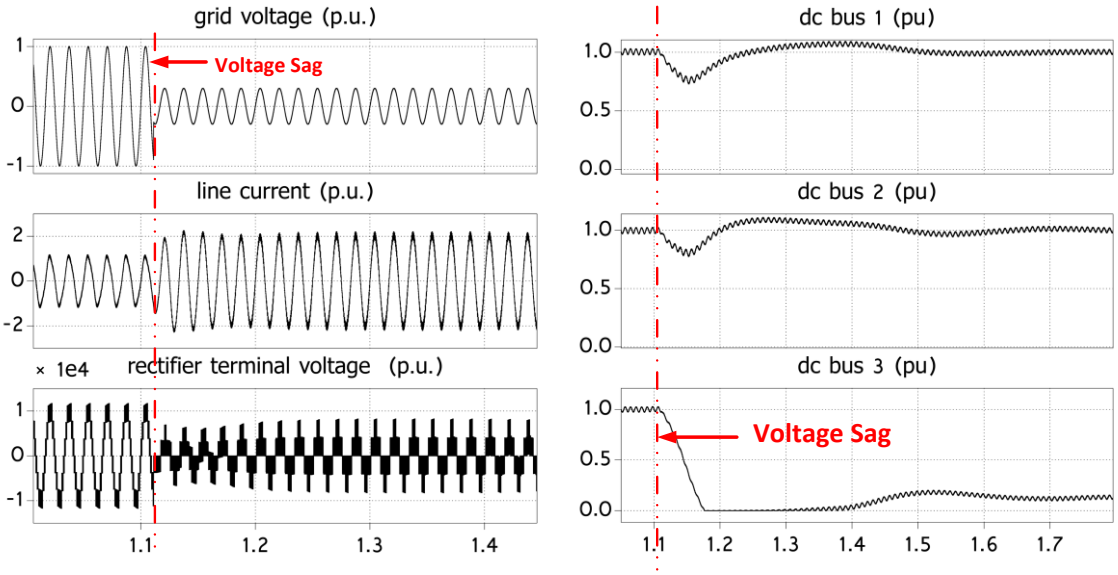


Figure 4.6 Input voltage sag of 0.3 p.u. with the DC bus collapse

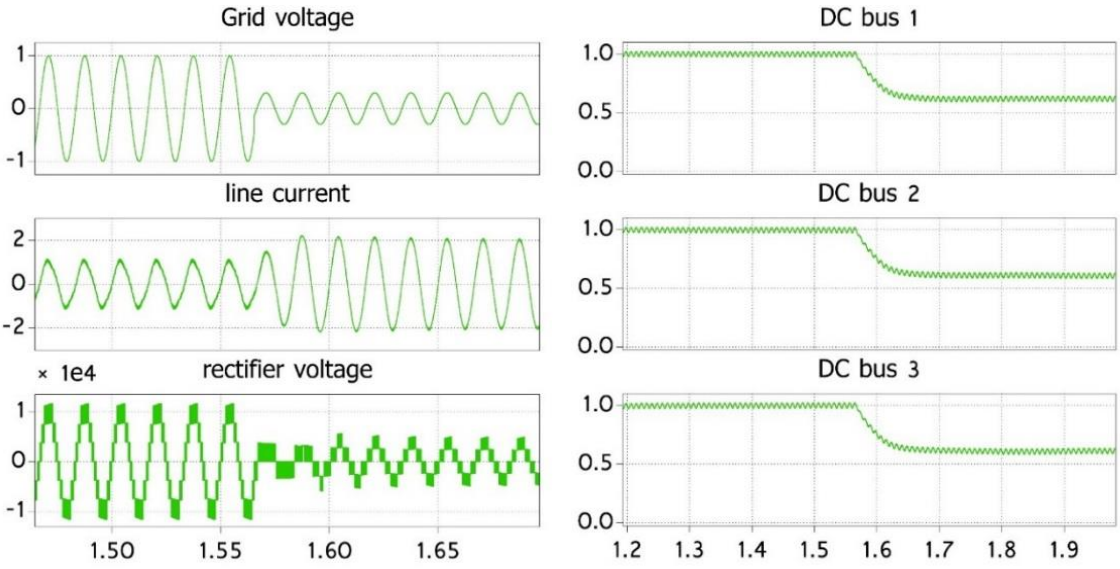


Figure 4.7: A 0.3 p.u. voltage sag with modified DAB power balance control to maintain DC bus balance

Fig. 4.4 shows the power balance control on the DAB stage under steady state operation. The outer voltage loop provides a current reference I_{ref} to the inner current loops. The measured current from each DAB is the high frequency inductor current sampled in a moving window fashion. Phase shift angle is generated for each DAB as the output of the current loop (Fig. 4.4). If the leakage inductance of the HF transformer of the individual DAB are different, the power transferred will be different as well (4.4). Hence the inner current loop maintains the power balance by providing the same average current reference. The power angle curve in Fig. 4.8 explains the power balance.

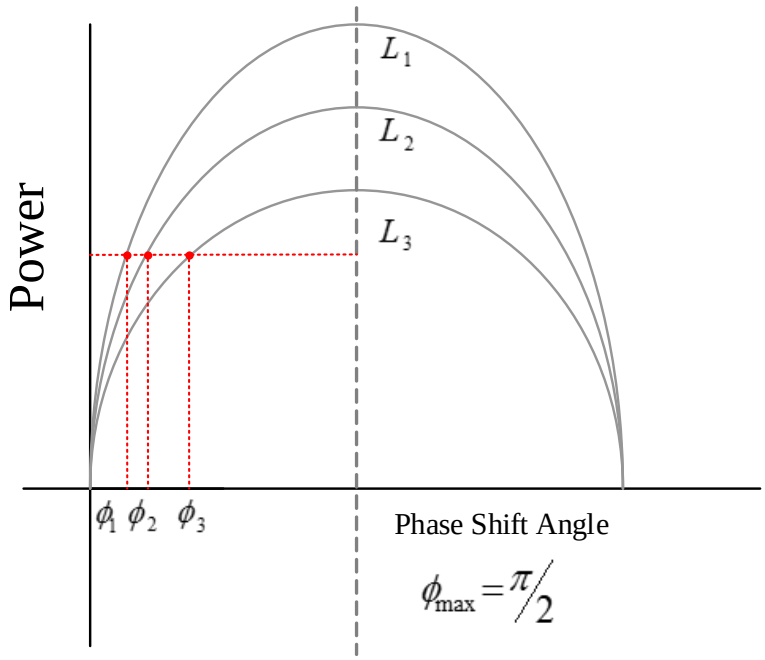


Figure 4.8: Power angle curve for the DAB with different leakage inductors and operating at different phase shift angles to transfer the same power

4.4. Inrush current limit at startup

The cascaded solid state transformer topology (Fig. 4.1) has three DC bus capacitors. Hence during startup there will be inrush current that might damage the front end switches. To limit the inrush current at start up a soft start algorithm is proposed in this section. In order to implement a soft start the DAB output bus is connected to an auxiliary dc source or a storage device. Considering the SST is disconnected from the grid this source charges up the rectifier buses. This is possible since DAB is a bidirectional DC to DC converter. The rectifier bridges will be switching under this condition as an inverter with the voltage reference from the PLL connected to the grid voltage. When the rectifier DC buses have reached a nominal rated voltage level the breaker is turned on connecting the grid to the rectifier. The rectifier changes over from inverter to rectification mode and regulates the DC bus. The auxiliary DC supply is disconnected or changes over to power absorbing mode and the power flows into the inverter to the load at its output. Adopting this method the inrush current is completely avoided and the start-up current is limited to 2 p.u. This is because neither the rectifier not the DAB sees an discharged DC bus while the power flow actually takes place. Fig. 4.9 shows the simulation results of the startup scheme described before. The current does not go beyond 1 p.u. and reaches steady state.

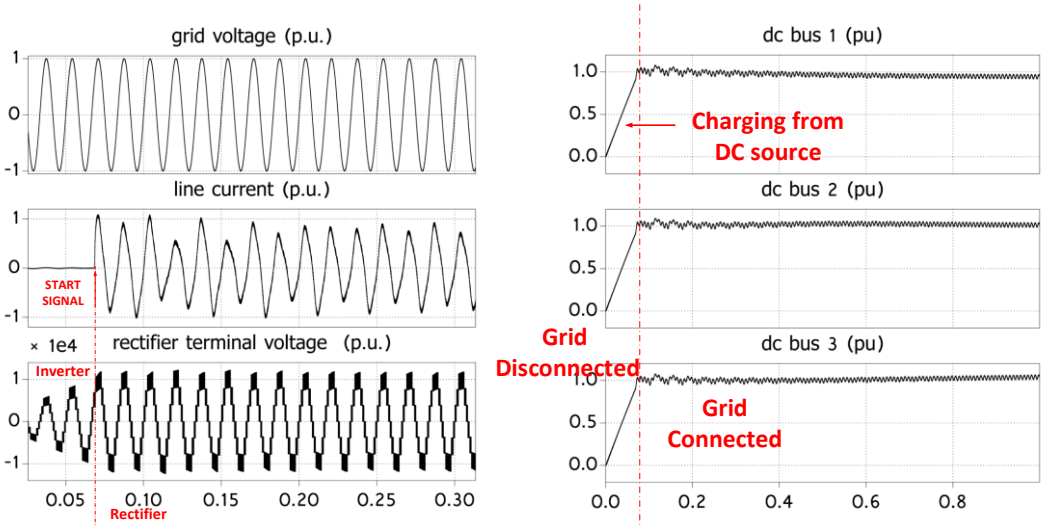


Figure 4.9: Soft Start of the SST from the auxiliary power supply

Table 4.1: Soft Start algorithm

Stage	Function
1	Startup is initiated from the LV side DC bus i.e. a battery bank or DRES
2	The DC stage charges up the rectifier side DC capacitor.
3	The rectifier works as inverter with $I_d = 0$ &$I_q = 0$.
4	When the dc bus capacitors reach nominal rated value the grid breaker is turned on.
5	The rectifier gains control of the dc bus and the power flow direction for the DC stage is reversed.

4.5. Single phase SST topology with the MLC –DAB topology:

In this section of the chapter an alternate topology is proposed in the DC to DC stage of the SST. The MLC-DAB topology proposed in the previous chapter has been used to replace the parallel DAB stages as shown in Fig. 4.10. The MLC-DAB topology has several

advantages in terms of reduction in magnetic material, copper and silicon area. The number of H-bridges is reduced on the secondary side since there is only one secondary winding. Battery or any other auxiliary DC source is directly connected to the transformer through an H-bridge, instead of being connected to the DC bus as in Fig. 4.10. The secondary bridge is connected to the central limb of the MLC and the primaries are connected to the peripheral limbs (Fig. 4.10). The central limb acts as an accumulator of flux from all the other limbs of the transformer. The primaries are all synchronized and switched at 50% duty cycle without any relative phase shift between them. Power transfer takes place by phase shifting the secondary with respect to the primary. A test bed of the MLC topology has been built as shown in Figure 4.12. The MLC-DAB based topology gives the advantage that we do not need to balance the dc bus voltage. Nor there is any requirement for power balance in the dc to dc stage. The reason is because the current in all the windings are same and hence same current flows through all the input terminals. The mismatch of the leakage inductance associated with each winding doesn't affect the power balance, since all the leakages add up in series.

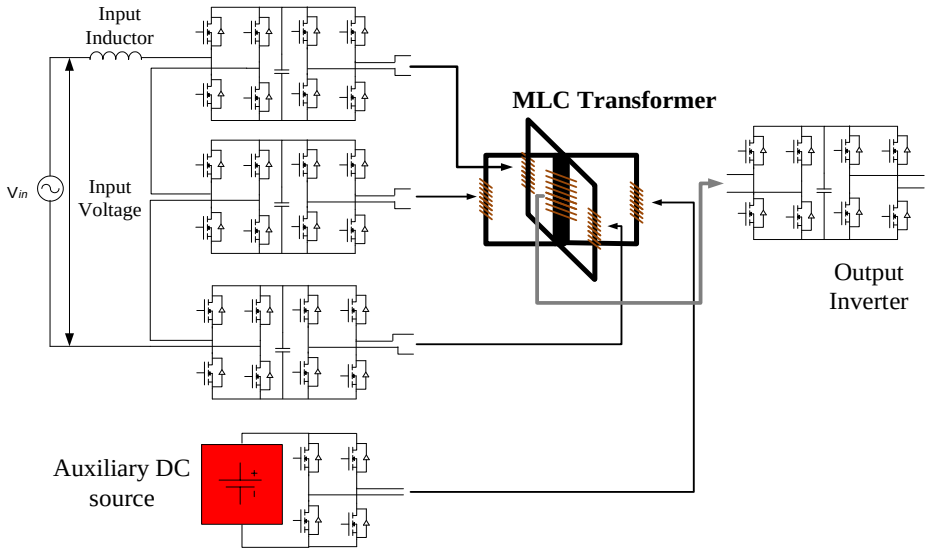


Figure 4.10: Single phase SST with the MLC transformer

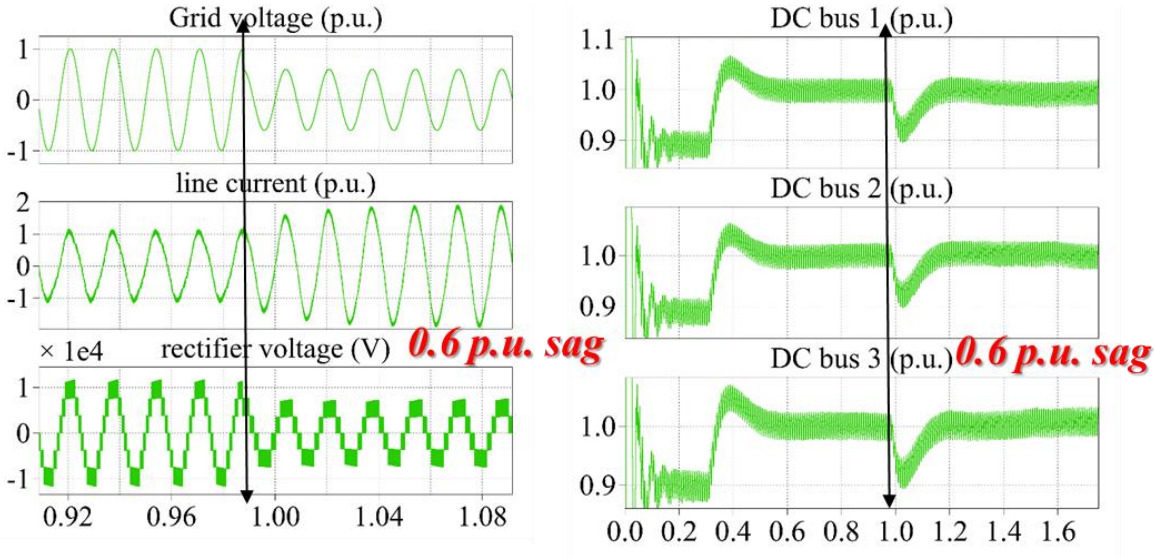


Figure 4.11: The voltage sag simulated with a MLC topology based SST without using any voltage bus balance control in the DC to DC stage as well as the front end stage

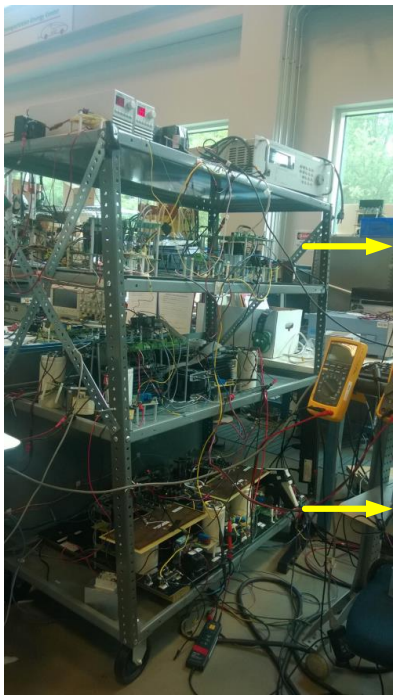


Figure 4.12: Experimental setup in the lab

4.6. Experimental results of the single phase SST topology showing the soft start and the MLC-DAB integration:

The experimental setup was developed in the lab as shown in Fig. 4.12. The parallel DAB based topology was developed first and the soft start algorithm was implemented as was discussed in section 4.4. Fig. 4.13 and Fig. 4.14 shows the experimental result of the soft start algorithm.

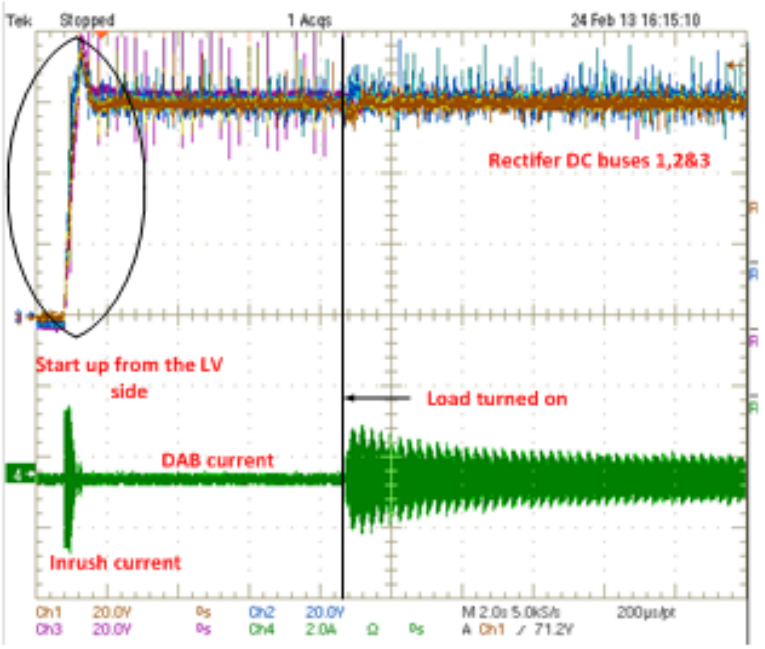


Figure 4.13: Soft start algorithm (DC side waveforms)

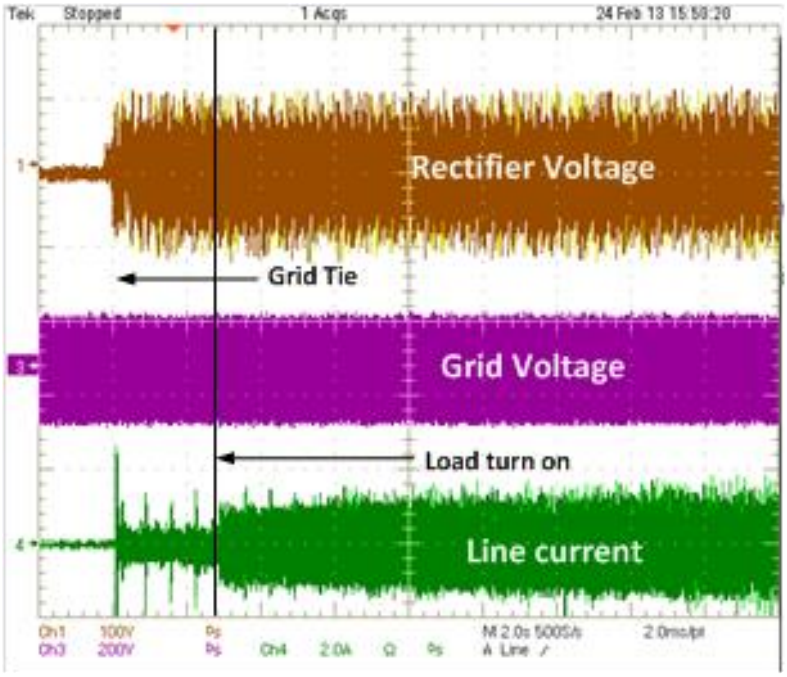


Figure 4.14: Soft start algorithm (AC side waveforms)

Fig. 4.13 shows the DC buses on the DAB input buses rising gradually as commanded by the controller. There is an inrush current still on the DAB stage. This comes from the auxiliary source connected to the output of the DAB DC bus. Further reduction in this current can be obtained if duty cycle modulation is done on the primary side of the DAB. Fig. 4.15 shows the steady state results of the MLC based SST topology as shown in Fig. 4.10. There is no voltage balancing loop in this case with the active front end. Fig. 4.16 shows the situation with voltage sag implemented in the MLC-SST. It is seen that the line current increases to provide the voltage regulation on the DC buses.

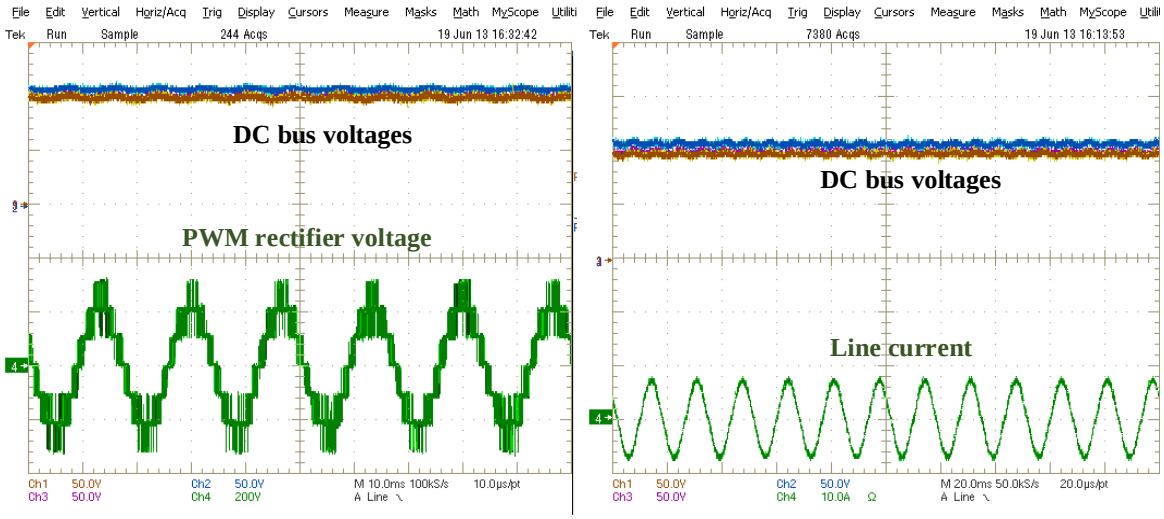


Figure 4.15: Steady state operation of the MLC based SST topology

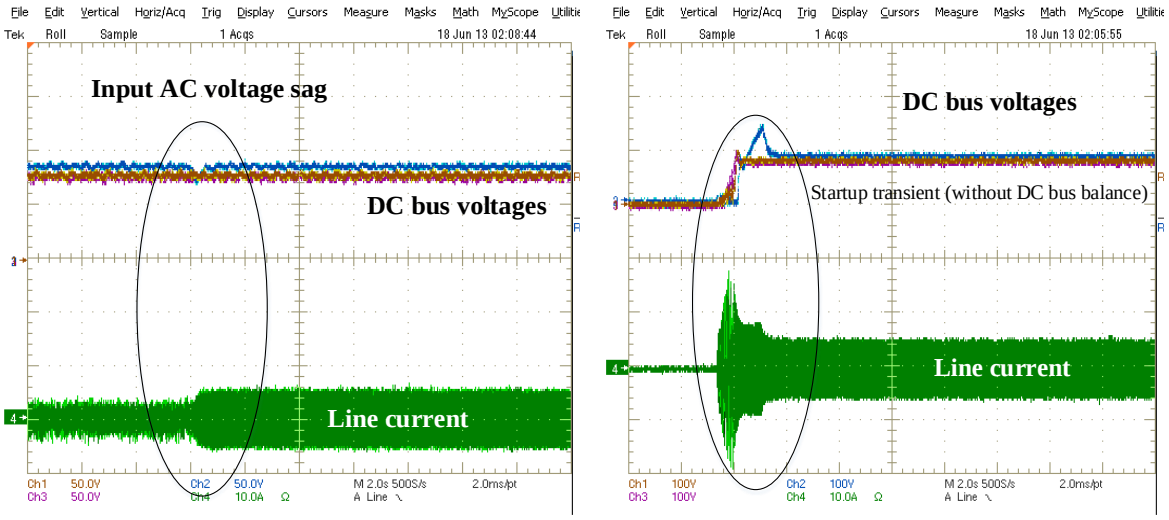


Figure 4.16: Experimental results showing the voltage sag compensation without the voltage bus balancing control (left). The right shows the startup pf the SST with the inrush current but without any voltage bus control

4.7. The renewable energy hub concept

The renewable energy hub (REH) concept is shown in Fig. 4.17. It is an extension of the solid state transformer concept with multiple renewable energy source (RES) integrations. In the solid state transformer the renewable energy integration takes place in the output DC bus of the DAB converter as shown in Fig. 4.18. Individual RES are tied to a common DC bus through an isolated DC to DC converter forming the local DC micro-grid. Parallel connection of these DC to DC converters require power balancing algorithms to be implemented on these converters. Several DC droop based control algorithms have been proposed [3], [11].

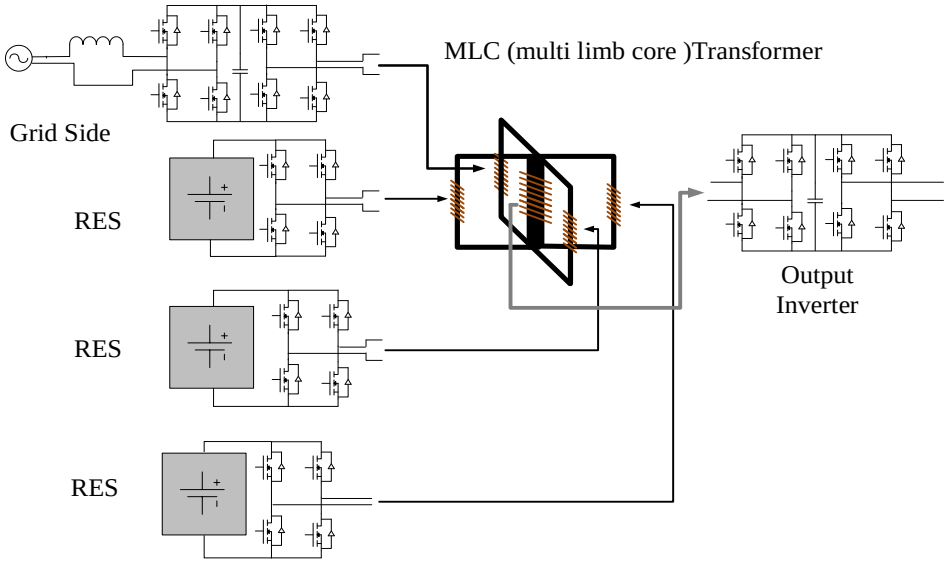


Figure 4.17: The renewable energy hub concept.

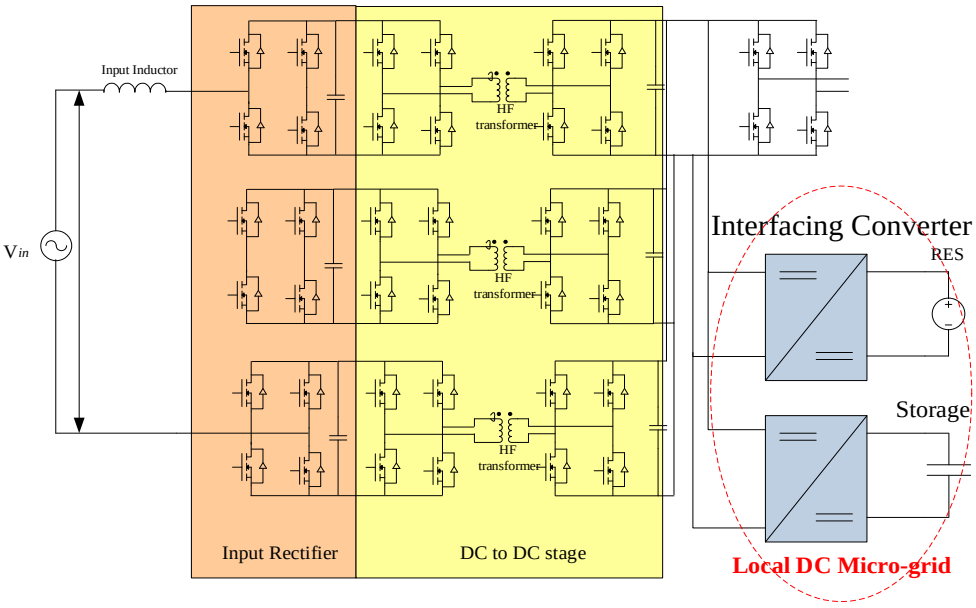


Figure 4.18: The single phase SST with the DC micro-grid concept.

However in the renewable energy hub concept as proposed in Fig. 4.17, the energy is accumulated in the central limb of the MLC transformer. Loss of modularity is a disadvantage in this topology but this gives easier control since no power sharing algorithm is required. Input current driven MPPT can be implemented as discussed in section 3.7 of chapter 3 using duty cycle modulation. Fig. 4.19 shows the control diagram in the MLC stage of the Renewable Energy Hub. In case there are multiple RES with multiple MPPT points it is possible to achieve individual current control for different operating points of individual RES connected to individual limbs. Considering the case where there are *n* RES and the current reference generated from the MPPT be I_k^{ref} where $k = 1,2, \dots n$. A sorting algorithm determines the maximum of these current references. The phase shift angle is set by the I_{MAX}^{ref}. The rest of the current references are attained by the PWM based duty cycle modulation as mentioned in sectioned 3.7. Fig. 4.20 and Fig. 4.21 shows the simulation results of the MPPT based current control for RES operation. There are four RES and the maximum is $I^{ref} = 10A$. This determines the phase shift between the primaries and the secondary connected to the central limb. Thus it is to be noted that the duty cycle of that bridge on the primary side is 50 % as shown in for voltage waveform V_1 in green in Fig. 4.21. The rest of the current references are less than 10A, i.e. 9A, 7A, and 5A. For them the primary bridges are duty cycle modulated with duty cycle as shown in (4.5)

$$d_1 = \frac{9}{10}, d_2 = \frac{7}{10}, d_3 = \frac{5}{10} \tag{4.5}$$

The voltage PWM wave form are shown in Fig. 4.21 with the duty cycle modulation.

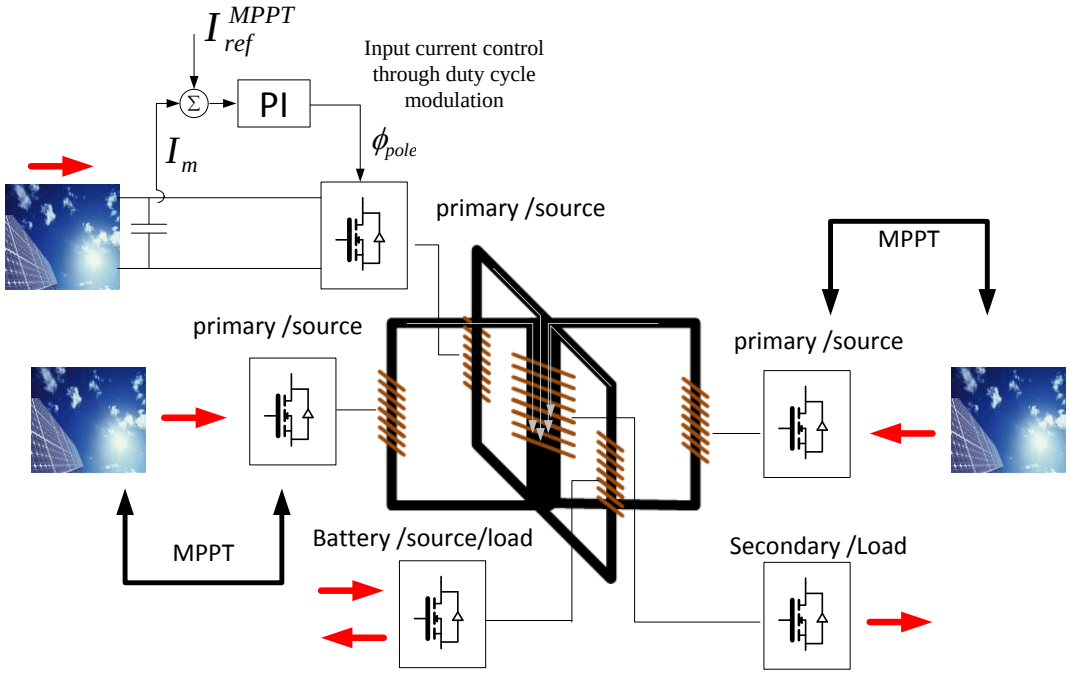


Figure 4.19: MPPT operation on the renewable energy hub.

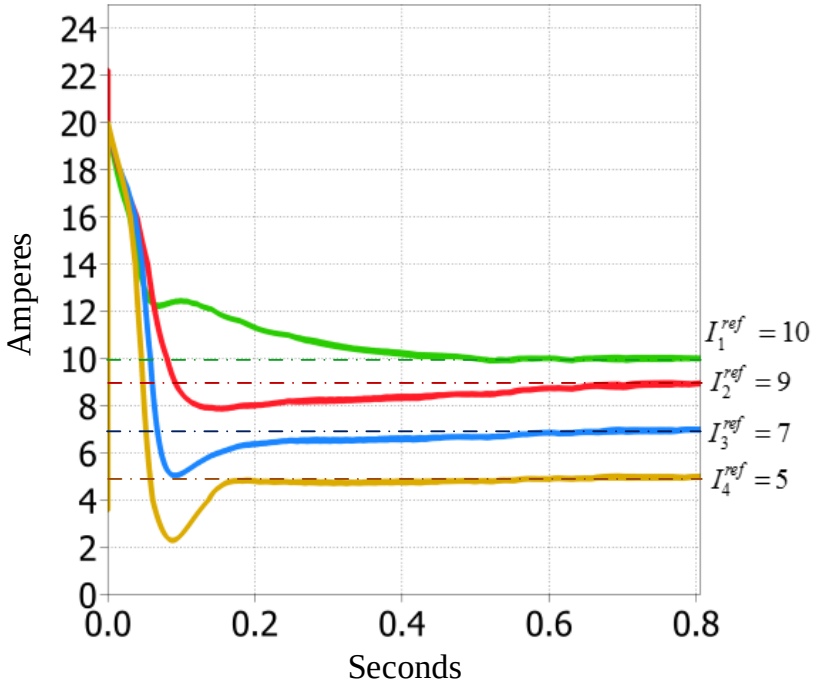


Figure 4.20: Input current control with different current references

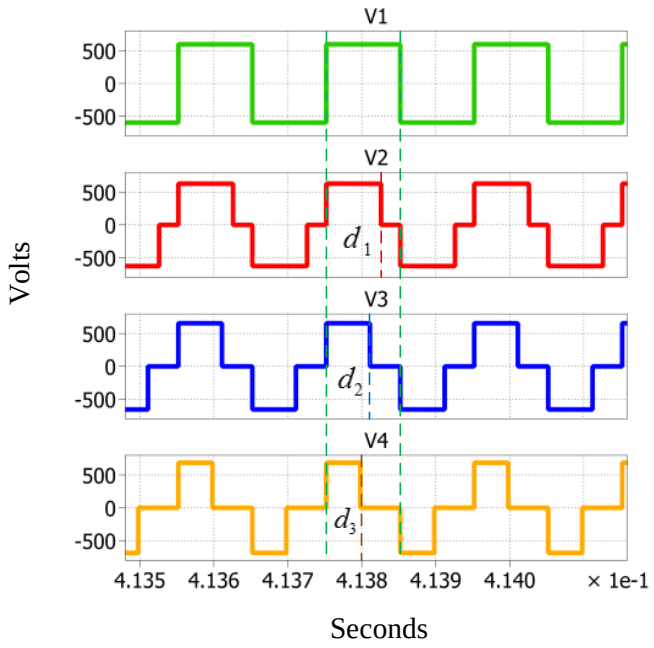


Figure 4.21: PWM voltage waveform showing the duty cycle modulation in order to obtain the current control

4.8. Energy management for the renewable energy hub

The primary purpose of the Renewable Energy Hub is to integrate renewables in to the grid and supply local load. However due to the intermittent nature of the RES, usually storage backup is provided. However in presence of the grid storage is not required where the grid itself provides the energy backup while the RES provides power to a local load.

Table 4.2: Power modes of operation

Modes	Function
$P_{RES} \geq P_{load}$	In this case the front end of the SST acts as an inverter and sources power back in the grid. The power available from the RES supplies the load and the excess power goes back to the grid.
$P_{RES} < P_{load}$	The sink mode is when the available power of the RES is not a match. The SST front end is in the rectifier mode.

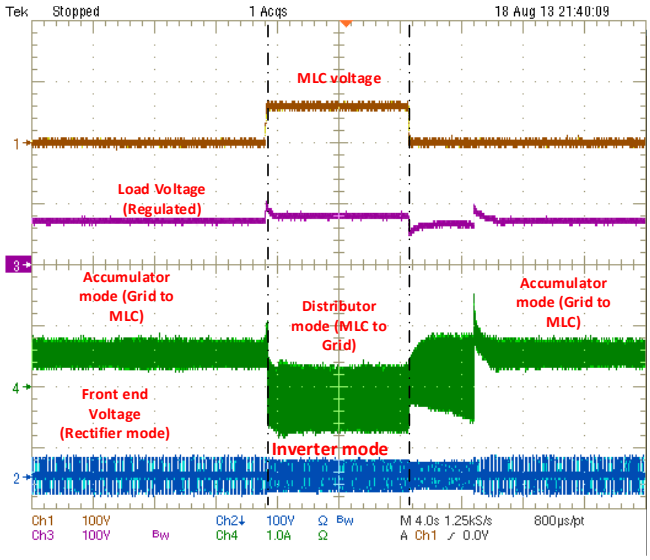


Figure 4.22: REH with the mode switching operation using the grid as the energy buffer.

4.9. Parallel operation of Single phase SST

This section of this chapter deals with the parallel operation of multiple single phase SST connected to a single phase AC bus. The main objective of this section is to study the parallel SST operation under different modes. Each SST is equipped with renewable energy source (RES) and a local load. In presence of grid each individual SST follows the grid voltage and

injects power or draws power from the grid based on the available RES. The front end of the SST acts as a rectifier in presence of the grid and maintains the DC bus. The power injected by the RES acts as a disturbance and in case $P_{RES} > P_{local\ load}$, the I_d^{ref} goes to negative to maintain the DC bus voltage and power flows back to the grid. Fig. 4.23 shows the schematic of the system.

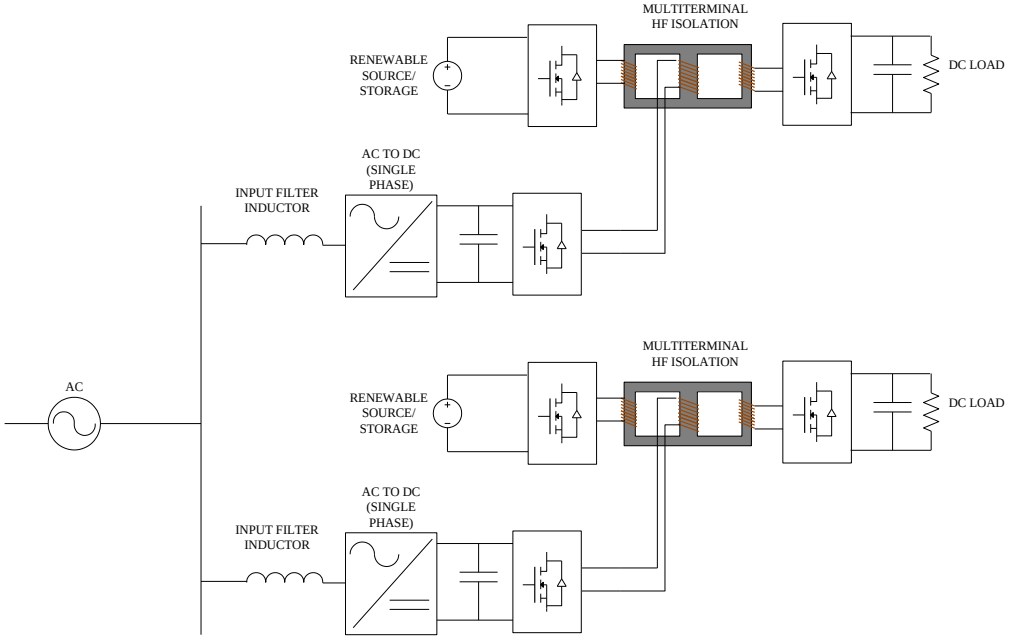


Figure 4.23: The parallel connection of two single phase SST

4.10. Controller design of the active front end of the SST

The front end controller has to be very robust in order to have good disturbance rejection due to the injecting RES from the DC to DC side. Fig. 4.24 shows the controller diagram for the front end control.

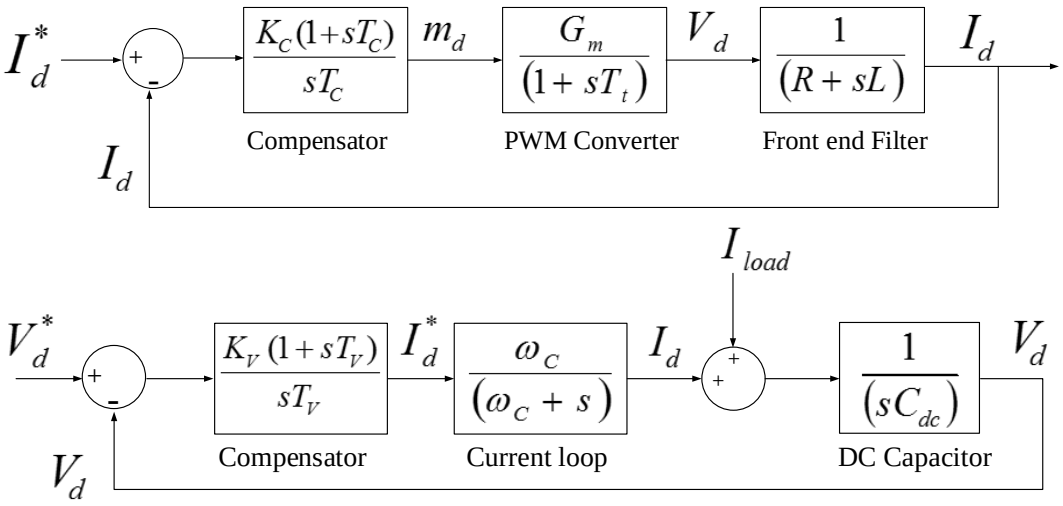


Figure 4.24: The controller diagram for the d-axes control of the front end. The inner current loop (above) is shown followed by the outer voltage loop (below)

The d-axes controller diagram is shown in Fig. 4.24. The q-axes controller is similar to the d-axes with the difference that there is no outer voltage loop and the $I_q^{ref} = 0$ for unity power factor applications. The PWM converter is modelled as $G_m/(1 + sT_t)$. Here $G_m = V_{DC}$ and T_t is the carrier frequency of the PWM which in this case is 10 kHz. The input filter inductor is modelled as a delay with time constant as $\tau_{filter} = L/R$ where R is the winding resistance of

the filter. The current controller parameters are K_c the proportional constant that determines the band width of the controller and T_c the time constant of the integrator. For a good current controller design the time constant of the controller is set to cancel the time constant of the filter i.e.

$$T_c = \tau_{filter} = \frac{L}{R} \tag{4.6}$$

With that the current controller band-width is set by choosing the appropriate value of K_c as per (4.7).

$$K_C = \frac{\omega_C L}{Z_{base}} \tag{4.7}$$

Here ω_c is the cutoff frequency of the current loop which is a tenth of the switching frequency i.e. 1 kHz in this case. The voltage controller is designed in a similar fashion. It is to be noted since there is a 120 Hz ripple in the DC voltage due to the system being single phase, the voltage bandwidth has to be a tenth of 120 Hz. Otherwise the controller will try to compensate for the ripple that will introduce a third harmonic in the line current. The controller parameters for the voltage control is K_v which the proportional part that determines the bandwidth of the controller and T_v that determines the time constant of integration of the integrator. The dominant system time constant for the voltage loop is determined by the capacitor. To compensate for that the proportional controller is chosen as

$$K_V = \omega_V C_{dc} Z_{base} \tag{4.8}$$

Here ω_V is the bandwidth of the voltage controller which is 10 Hz in this case. The integrator is designed to have infinite gain at zero frequency. Therefor T_V is kept around 5 Hz. Based on this design the controller was implemented in the hardware. Table 4.3 shows the experimental setup parameters.

Table 4.3: Experimental setup parameters

Parameters	Values
AC side filter inductor	3.5 mH
DC side capacitor	900μF
Switching frequency	10 kHz
DC bus voltage	100V
AC grid voltage	75V (peak)
Base line current (AC side)	5 Amps

Each individual SST has its own local load (Fig. 4.22). The local load is supplied by the SST by drawing power from the grid. Hence the front end starts off as a rectifier. The RES connected to each SST supplies power driven by MMPT input current control. In the test bed the current control has been implemented. A set current reference was given to the controller. Based on the current reference given the phase shift is generated between the RES connected peripheral-limb bridge and the front end bridge connected central-limb of the transformer.

4.11. The single phase PLL

The vector control of the front end converter requires the measurement of the grid voltage in order to calculate the voltage vector position. This can be achieved using a single

phase d-q PLL as shown in Fig. 4.25. In a single phase system the stationary reference frame (α-β reference frame) definition is different from a three phase system. In a three phase system V_α is usually aligned along V_A while the quadrature V_β is generated by the α-β transformation. In a single phase system also V_α is obtained by aligning it along the grid voltage. The V_β can be obtained by giving V_α a $\pi/2$ phase delay by storing the voltage values in a buffer for a quarter of the grid cycle. An alternate way of achieving this is to pass the voltage signal through an all pass filter transfer function and setting the phase shift to $\pi/2$ at $\omega = 2\pi 60$.

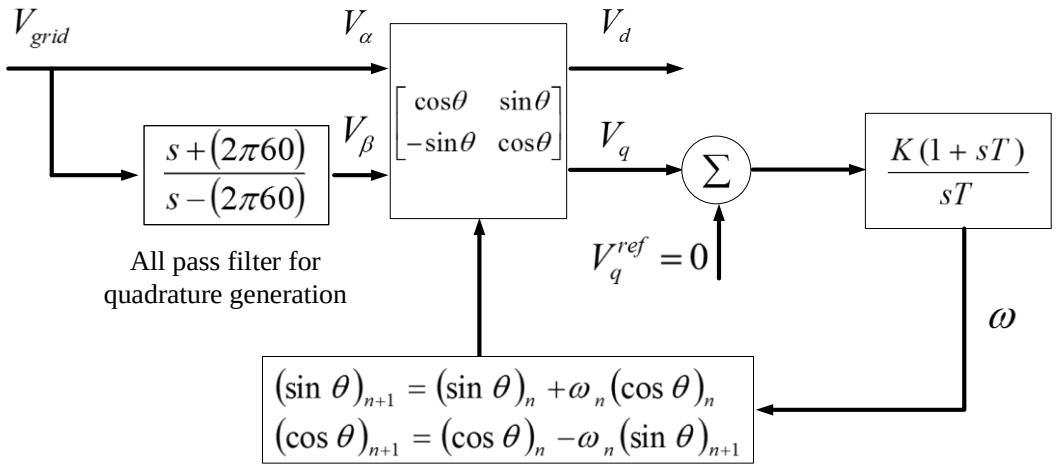


Figure 4.25: Controller diagram for the single phase d-q PLL with the all-pass filter for quadrature voltage vector generation

Fig. 4.25 shows the controller diagram for the single phase PLL. The first step is to obtain the stationary reference frame transformation by using the all pass filter as a quadrature generator. Once the V_α and V_β has been generated, the synchronous reference frame transformation is

done which gives the V_d and V_q. The calculated V_q is compared with the reference V_q which is zero since the V_α is aligned along the grid voltage. The output of the difference is the error that is fed to a PI compensator that gives the instantaneous grid frequency. Integrating the frequency will give the position of the voltage vector. But it is better to avoid integration or taking the sine or cosine of the phasor position angle since it requires invoking the math library in the DSP which requires more memory space. Hence a recursive algorithm was used to obtain the sine and cosine of the vector position angle directly as shown in Fig. 4.25.

4.12. Local load management for the single phase SST

The MLC based topology discussed in chapter 3 has been used in the DC to DC stage of the SST. One of the peripheral winding has been connected to the local load while the other windings are connected to RES. The central winding has been connected to the rectifier bridge. The mode where the RES supplied power to the local load has been already discussed extensively in chapter 3. The topic of discussion of this subsection is the mode where there is no power available on the RES, the front end provides the local load. Fig. 4.26 shows the power flow direction under different operating modes. The DC to DC stage is a three terminal device with Bridge 1 connected to the front end, Bridge 2 connected to the RES and Bridge 3 to the local load. If $P_{RES} > 0$ a part of the energy flows to the local load and a part flows back to the grid via Bridge 1 and the front end (blue arrow in Fig. 4.26). This mode is similar to the distributor mode discussed in chapter 3. The RES supplies power based on a MPPT driven input current control. Bridge 1 leads Bridges 2 & 3 based on the phase shift generated by the

input current controller for MPPT application on Bridge 2. If $P_{RES} = 0$ then the front end maintains the DC bus and provides power to the local load (red arrow in Fig. 4.26).

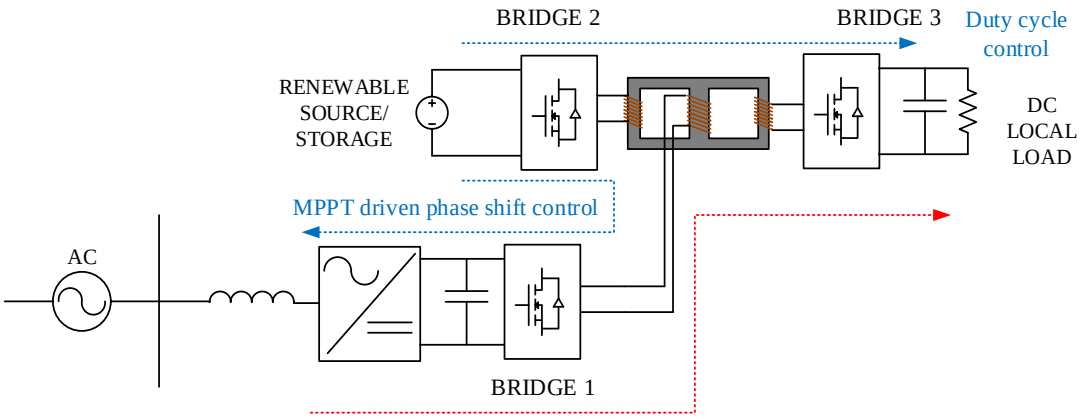


Figure 4.26: Power flow direction on the single phase SST

Since there is no phase shift between bridges 1 & 3, power transfer under condition $P_{RES} > 0$ take place only through duty cycle modulation. Fig. 4.27 (left) shows the experimental waveform for the duty cycle modulation with the power flowing from bridge 1 to bridge 3 (red arrow in Fig. 4.26). The duty cycle modulated waveform of the bridge 3 shows the fraction of the current in shaded portion that flows to the local load and charges it. Since the load is mostly inductive the current is triangle in nature, thus the maximum power transfer takes place with the duty cycle at a quarter of the switching cycle.

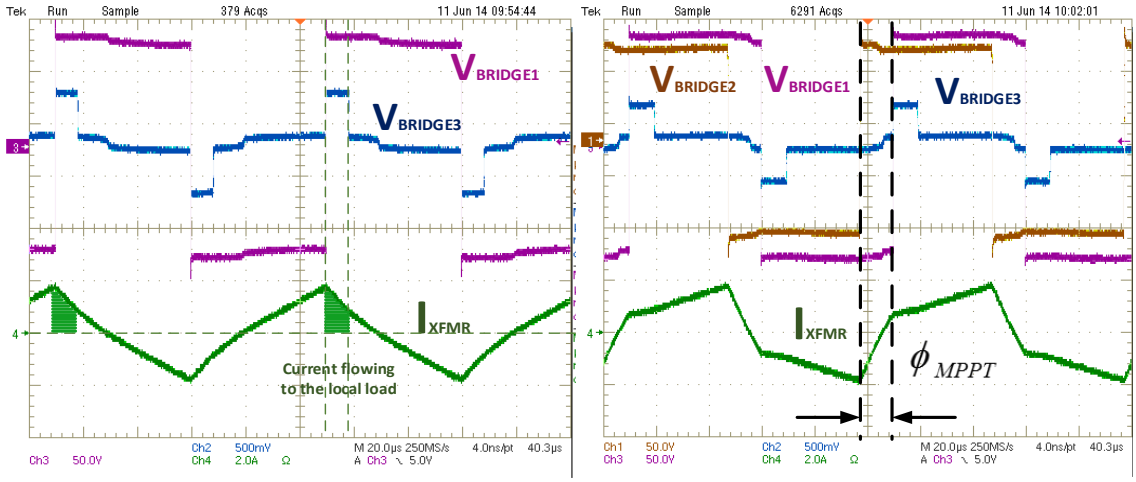


Figure 4.27: Local load management without the RES (left) and with power contribution from the RES (right)

Fig. 4.27 (right) shows the mode where the RES has been turned on to supply power back into the grid. The phase shift between the voltage of bridge 2 and bridge 1 or 3 is generated by the MPPT driven input current control. Fig. 4.28 shows the simulation results of the I_d reference generated by the front end control in presence and absence of the RES. With the RES off the front provides a positive I_d and feeds the local load. When the RES is turned on, the I_d polarity changes and power is supplied back to the grid with a negative. Fig. 4.29 shows the experimental results of the front end with and without the RES turned on. With the RES turned off the current flows out from the grid to the local load. In presence of RES the current is opposite polarity with the line voltage as power is flowing back into the grid.

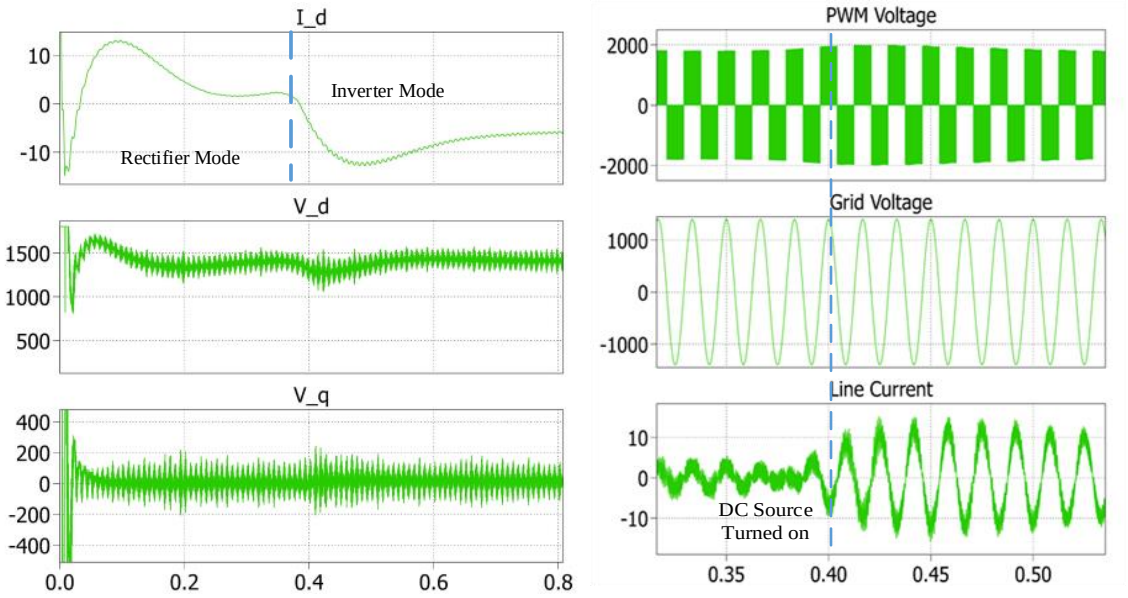


Figure 4.28: Simulation results showing the change in polarity of I_d with the RES switched on and off

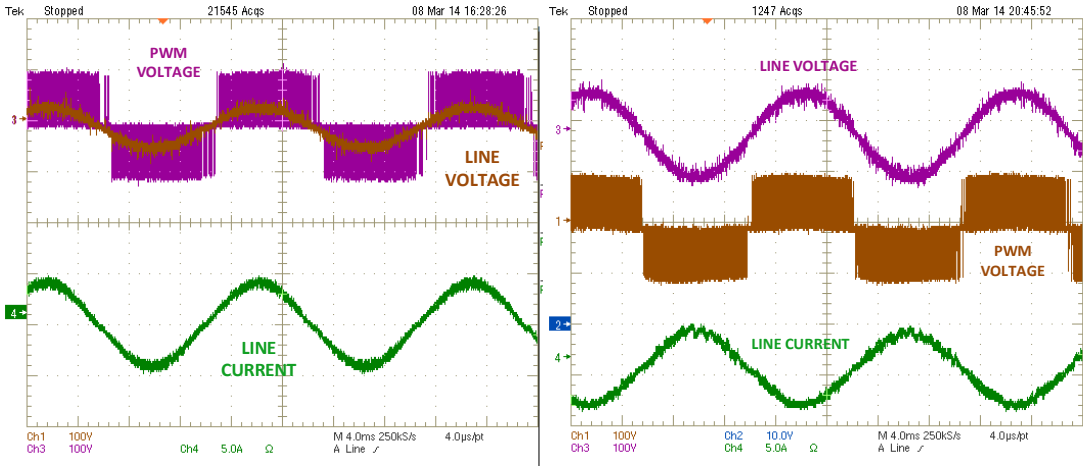


Figure 4.29: Experimental results showing the current and voltage waveform of the front end with and without the RES turned on

4.13. UPS operation of a single phase SST

This section discusses the UPS operation of SST in case of grid failure.

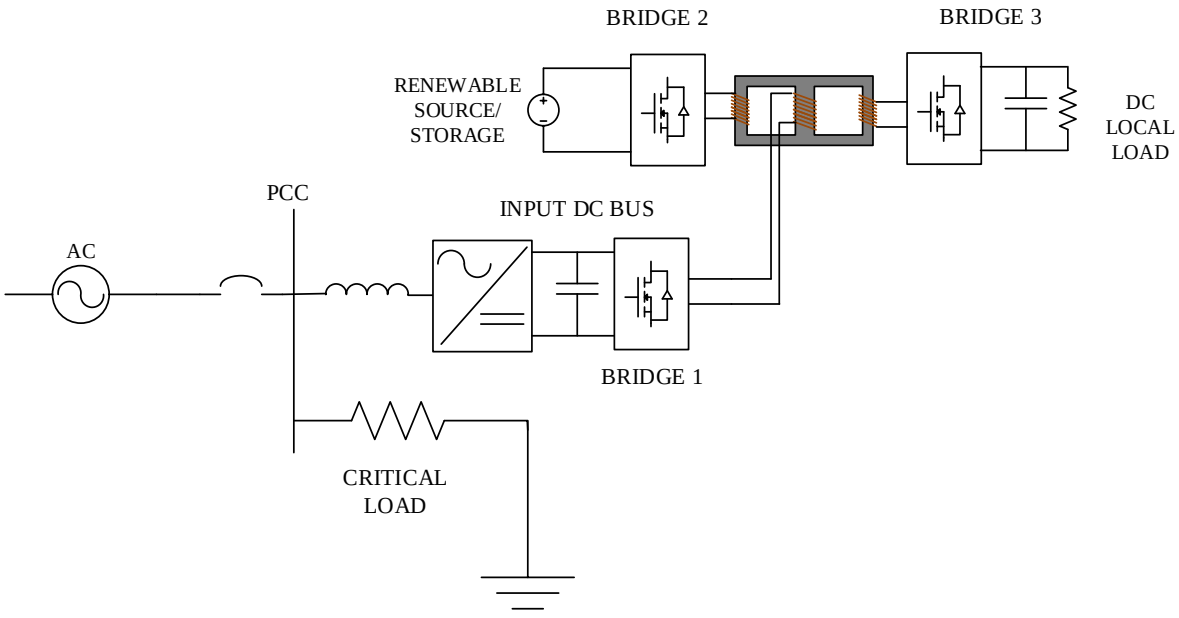


Figure 4.30: The single phase SST as a UPS system with a critical load

Fig. 4.30 shows the system setup for the UPS operation of the SST. The PCC of the SST with the AC bus has a local AC load. The grid is interfaced with an AC solid state breaker that islands the system in case of failure. The developed lab prototype doesn't include the islanding algorithm. Instead the system is islanded manually and the DSP unit is made aware. Under islanded operation several mode changes take place in the controller both for the front and the DC to DC stage. For the DC stage in grid connect mode the input current to bridge 2 drove the phase shift angle between bridge 2 and bridge 1&3. However under islanded mode the RES

needs to regulate the input DC bus (Fig. 4.30) giving up MPPT mode of operation. The local load will still be supplied. The front end will change into inverter mode of operation and will regulate the PCC AC voltage. For the DC to DC stage, regulating the input DC bus is the most critical function. And hence at the onset of islanding when the system goes through the black start mode, the DC stage is commanded to shed its local load and regulate the input DC bus voltage. After the PCC voltage has been established by the front end, the local load is supplied by the DC stage and the local load bus ramps up. Fig. 4.31 shows the black start operation in a flow chart form. Fig. 4.32 shows the experimental results with the islanding of the SST with the load shedding functionality. The load shedding provides a ramp increase in the local load while the AC bus power supply remains un-interrupted.

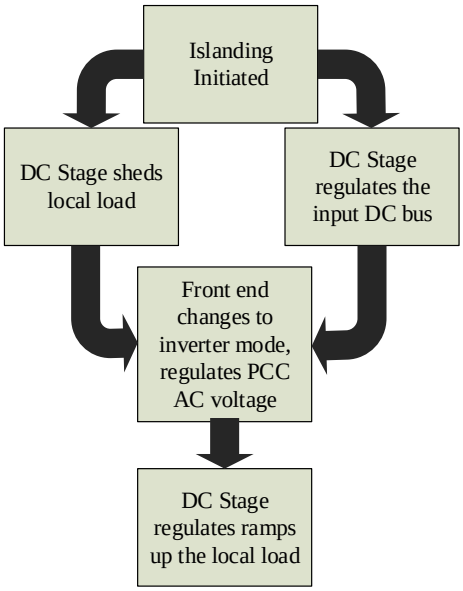


Figure 4.31: Flow chart diagram of the black start system for the SST supplying a critical load

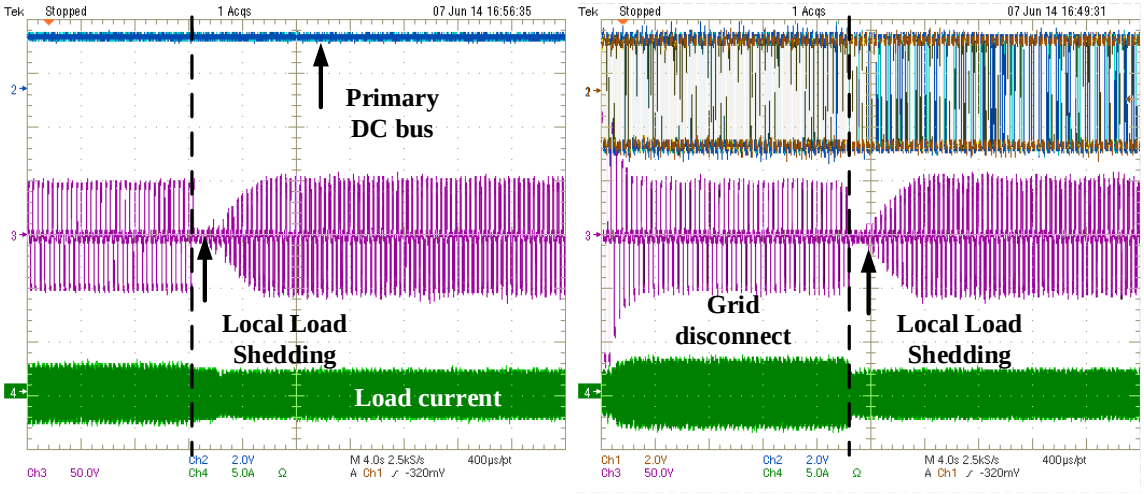


Figure 4.32: Experimental results of local load shedding during black start upon islanding from the AC grid.

4.14. Grid tied parallel operation

Fig. 4.23 shows the schematic of the grid tied operation of the two parallel SST. Under grid tied mode the front end acts as a rectifier to regulate the input rectifier DC bus while the RES connected to each DC stage supplies power to the DC bus in constant current mode. The front end current control adjusts accordingly to keep the DC bus regulated.

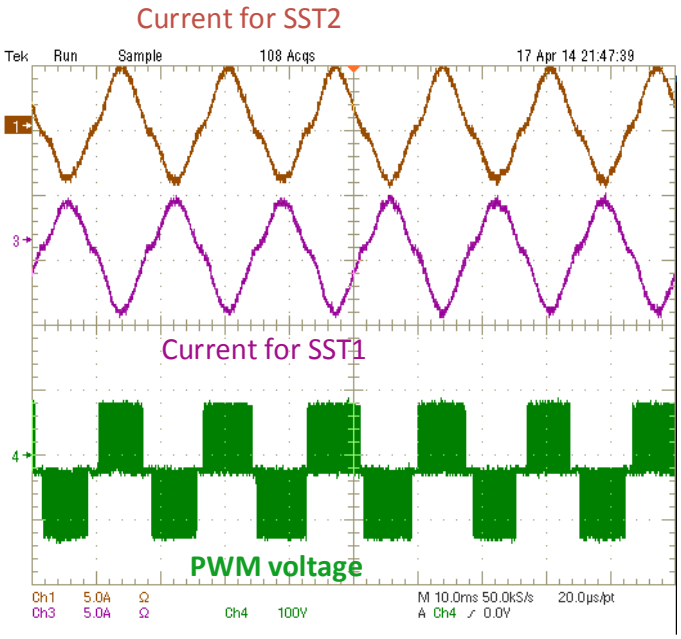


Figure 4.33: Experimental results for the two SST connected in parallel with grid. SST 1 is in the regenerating mode while SST 2 is in the load mode taking power from the grid

4.15. Black start operation of parallel connected SST in islanded mode

The final section of the chapter deals with the parallel operation of single phase SST connected to a PCC along with a critical load under islanded condition [32]. The power sharing between parallel connected inverters under islanded condition has been an extensive topic of research [33], [34], [35]. Droop mode of control is a popular approach to manage power sharing between parallel connected inverters where renewable energy sources are concerned. An alternate to the droop mode of control is the master slave mode of control. It is a simpler mode of control where one of the inverters define the PCC voltage while the other inverters supply power under constant current mode. In this case the system comprises of one SST that acts as

a master and defines the PCC voltage. The front end of the master SST acts as an inverter that controls the voltage of the PCC bus while the slave SST front end has two options.

1) The slave front end acts as a rectifier while the DC stage connected to the DC bus pushes power. Power flow in the DC stage is controlled by MPPT driven input current control. This has the advantage of proper utilization of the RES connected to the slave SST.

2) The second option is that the front end of the slave SST acts as a current controlled inverter and pushes power in to the PCC. In this case the DC stage of the slave SST controls the input DC bus voltage of the front end.

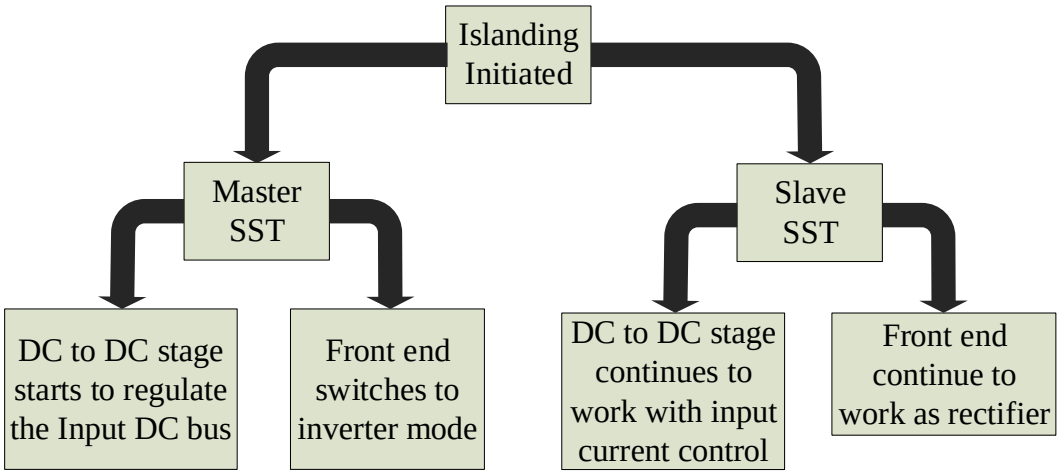


Figure 4.34: Flow chart diagram for the black start operation with the slave SST front end acting as a rectifier under islanded mode

Fig. 4.34 shows the black start up control flow chart diagram as per mode 1 discussed above. As soon as islanding has been detected and the grid breaker has been tripped, the master front

end reverts to inverter mode while simultaneously the DC to DC stage controls the input DC bus voltage. However there is no change in the control for the slave SST. Its front end continue to work as rectifier and the DC stage inject power in the input DC bus.

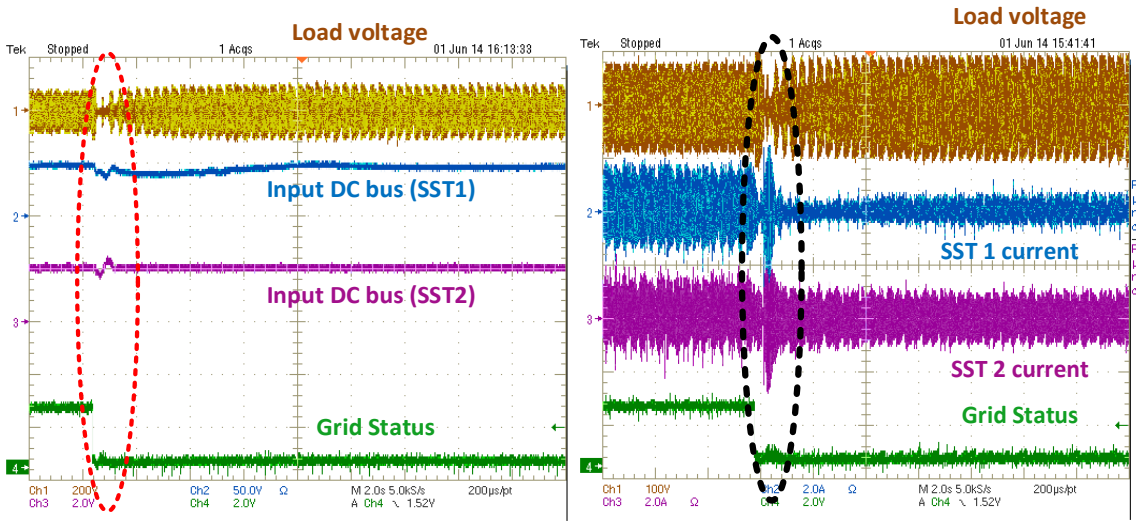


Figure 4.35: Experimental result of the black start of the parallel SST system with the slave SST front end working as a rectifier.

Fig. 4.35 shows the experimental result for the black start for the parallel SST system. It is seen that the load voltage sags at the time of grid failure. The black start introduces an undesirable transient on the load. In order to improve the load transient during the black start operation, the slave SST mode change is considered. In the grid connected mode front end of the slave SST works as a rectifier. However on grid disconnect the slave SST changes to current control inverter. Its DC to DC stage controls the inverter DC bus. On the master SST, the mode change remains same on the front end however the DC stage goes through load

shedding of the local load. The local load voltage reference is reset to zero and slowly ramps up.

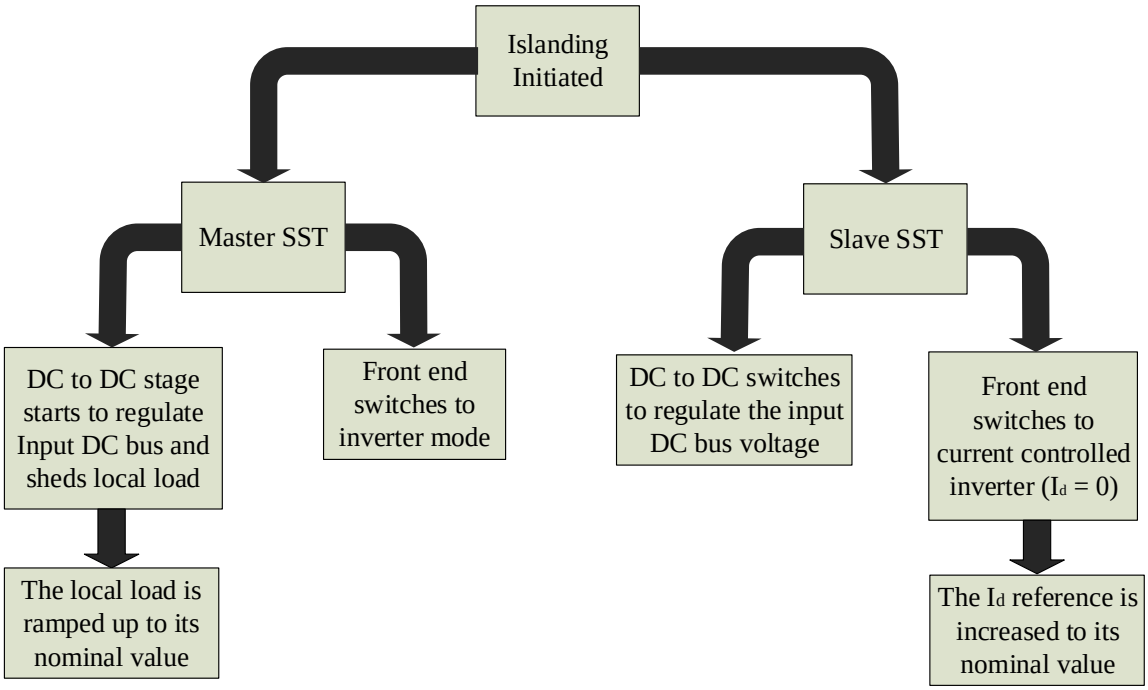


Figure 4.36: Flow chart sequence diagram of the black start operation of the parallel connected SST with the master undergoing local load shedding and the slave SST front end acting as a current controlled inverter

The flow chart in Fig. 4.36 has been implemented in the experimental setup. Fig. 4.37 shows the experimental results for the proposed black start sequence. The local load goes through a load shedding at the onset of the black start sequence. The critical load remains undisturbed.

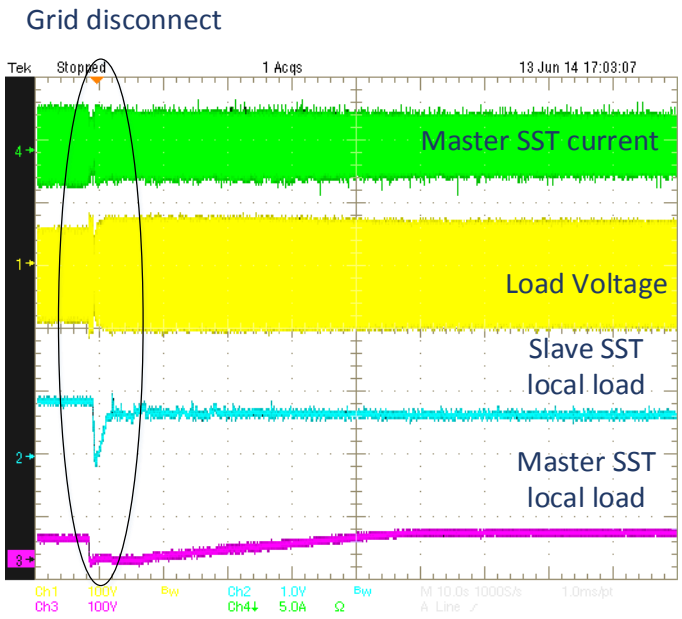


Figure 4.37: Experimental results of the black start operation under load shedding with the critical load connected to SST 2 (slave DC stage)

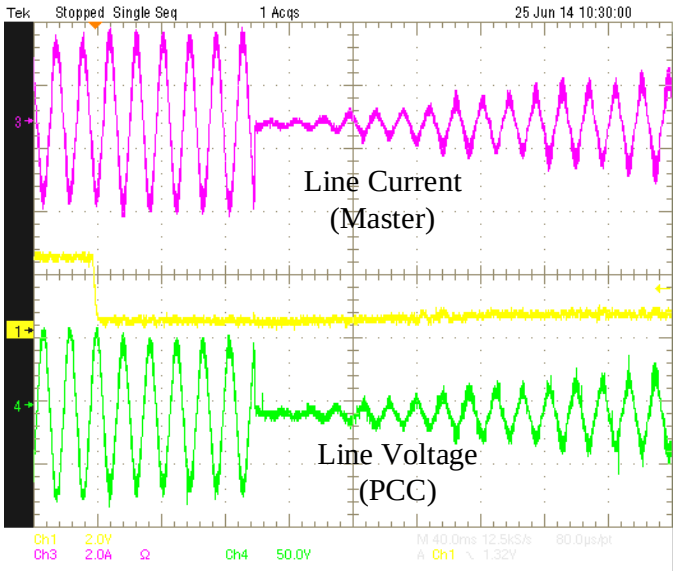


Figure 4.38: Black start without the feed-forward term on the master SST voltage controller

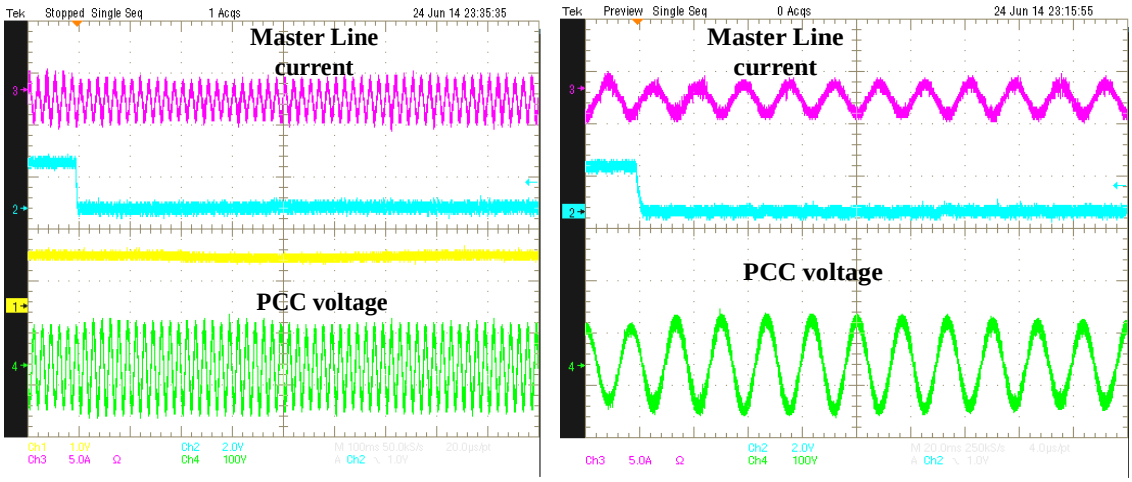


Figure 4.39: Experimental results of the black start operation showing the PCC voltage regulated by the master

In order to have an uninterruptable voltage regulation on the PCC by the master, the reference voltage is fed forward on the d-axes modulation index. Therefore the final modulation index that goes to the PWM module for gate pulse generation is shown in (4.9).

$$m_d^{PWM} = m_d^{ref(feedforward)} + m_d^{PI} \tag{4.9}$$

Here $m_d^{ref(feedforward)}$ is 0.75 p.u. and m_d^{PI} is the output from the PI compensator. Without the feed-forward the PCC voltage will go through a transient at the time of grid disconnect. Fig. 4.38 and Fig. 4.39 shows the PCC bus voltage without and with the feed forward during the black start. The feed forward loop takes care of the transient and makes the regulation better.

4.16. Critical load placement in SST topology:

Critical load connected to the SST be it in the DC stage or the AC stage needs uninterrupted power supply. Incase islanding has been detected and the grid shuts down it is important to have the critical loads connected at certain points so that the SST can supply uninterrupted power. In Fig. 4.40, the critical load points are marked in red. When the grid fails it is the job of the master to regulate the PCC voltage so that there is minimum interruption. The DC load connected to the master is assumed to be not critical. Hence a ramped reference is given similar to Fig. 4.32. For the slave SST the critical load is connected to the DC stage which can be considered as the norm. Thus the job of the slave SST is to regulate the local load with minimum interruption while the excess power can be injected to the grid. However there is a problem with this configuration for the load. Since the load is connected to the peripheral limb as per Fig. 4.40, the power transfer takes place through duty cycle modulation as explained in sec. 3.7. The duty cycle modulation itself is dependent on the phase shift between the peripheral limbs and the central limb which in this case is linked with the winding connected to the grid. Hence unless the front end starts injecting current to the grid, the phase shift between the peripheral limb and the central limb will not develop and this constrains the power supply to the critical load connected to the DC side. To remedy this on way is to link the peripheral limb to the grid connected front end and connect the critical load to the central limb as shown in Fig. 4.41. The second method may be is to simply increase the capacitor connected to the slave SST (in blue in Fig. 4.41) so that during the black start the capacitor supplies the transient energy while the phase shift between the peripheral and the central limb

is established. Fig. 4.42 shows the generalized system diagram with one master SST module (red) and multiple slave module with their own critical load connected to the DC stage. In grid connected mode the master SST is irrelevant. The SST front end act as rectifier maintain the input DC bus. Both the front end and the renewable energy together supply the power to the load connected to the central limb by phase shift mode of control.

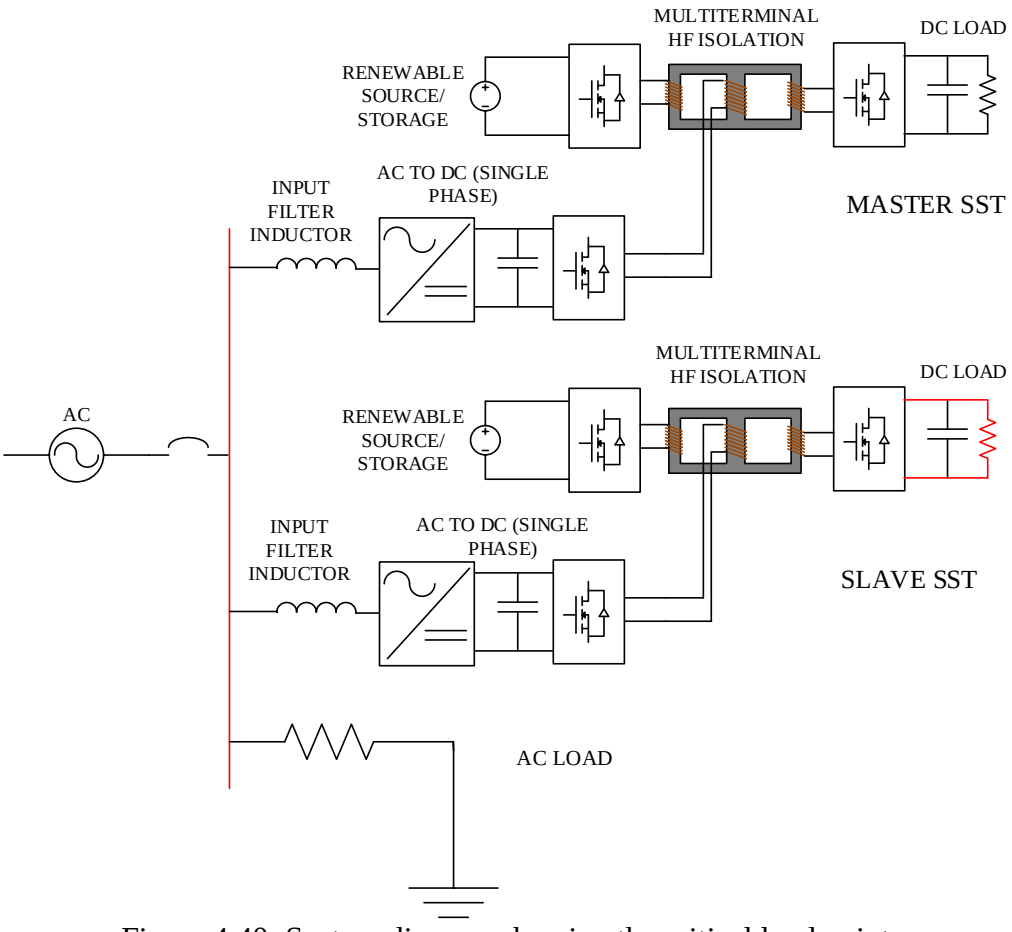


Figure 4.40: System diagram showing the critical load points

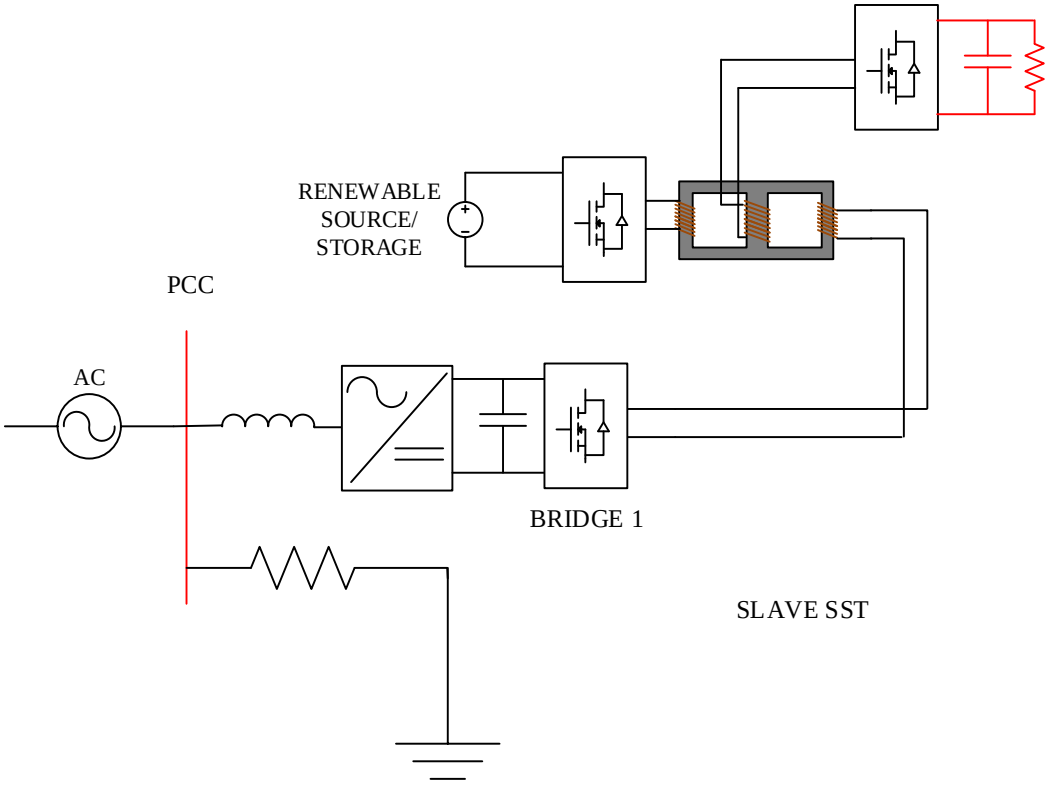


Figure 4.41: Slave SST showing the reconfigured winding arrangement.

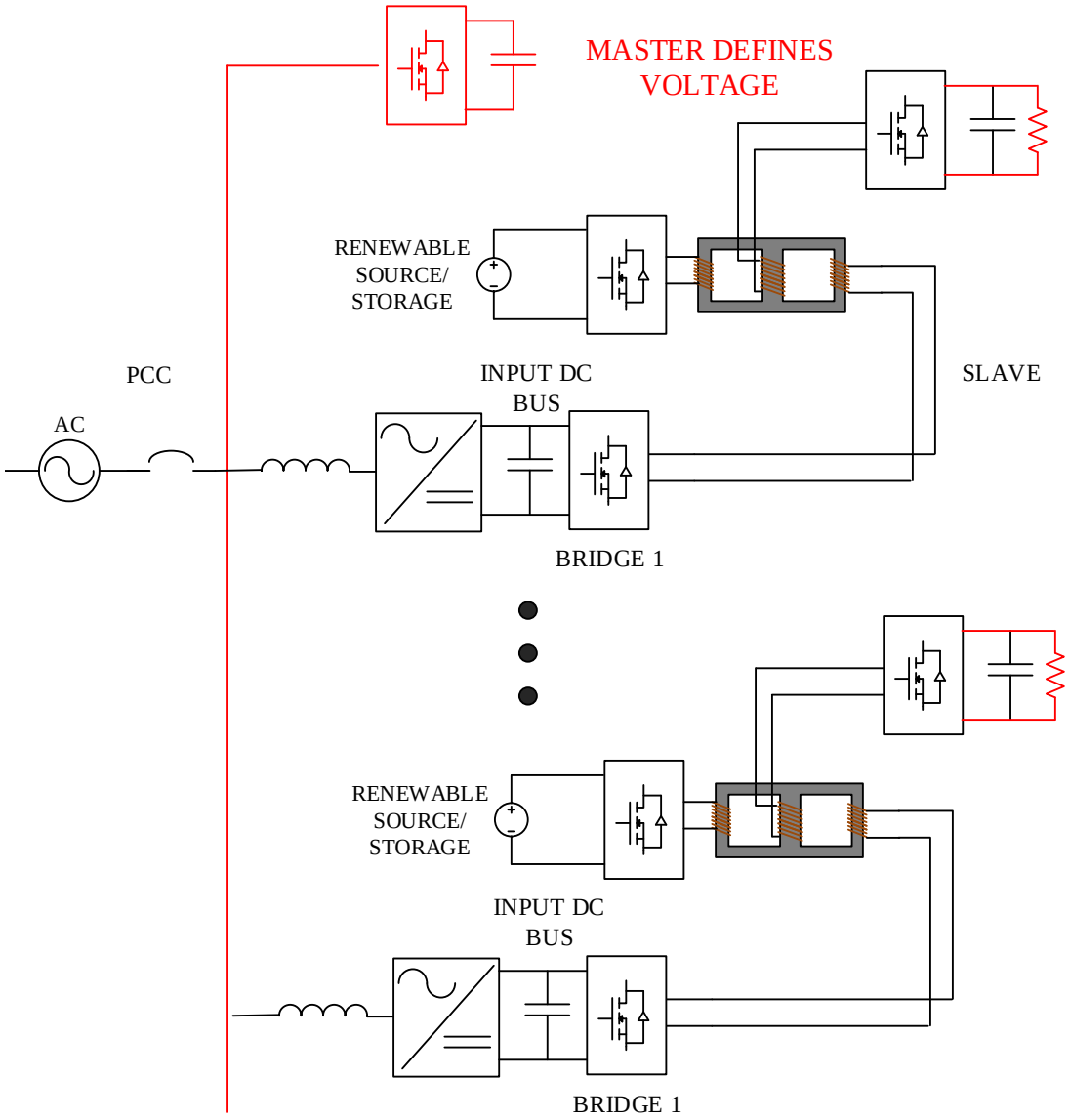


Figure 4.42: Slave SST showing the reconfigured winding arrangement.

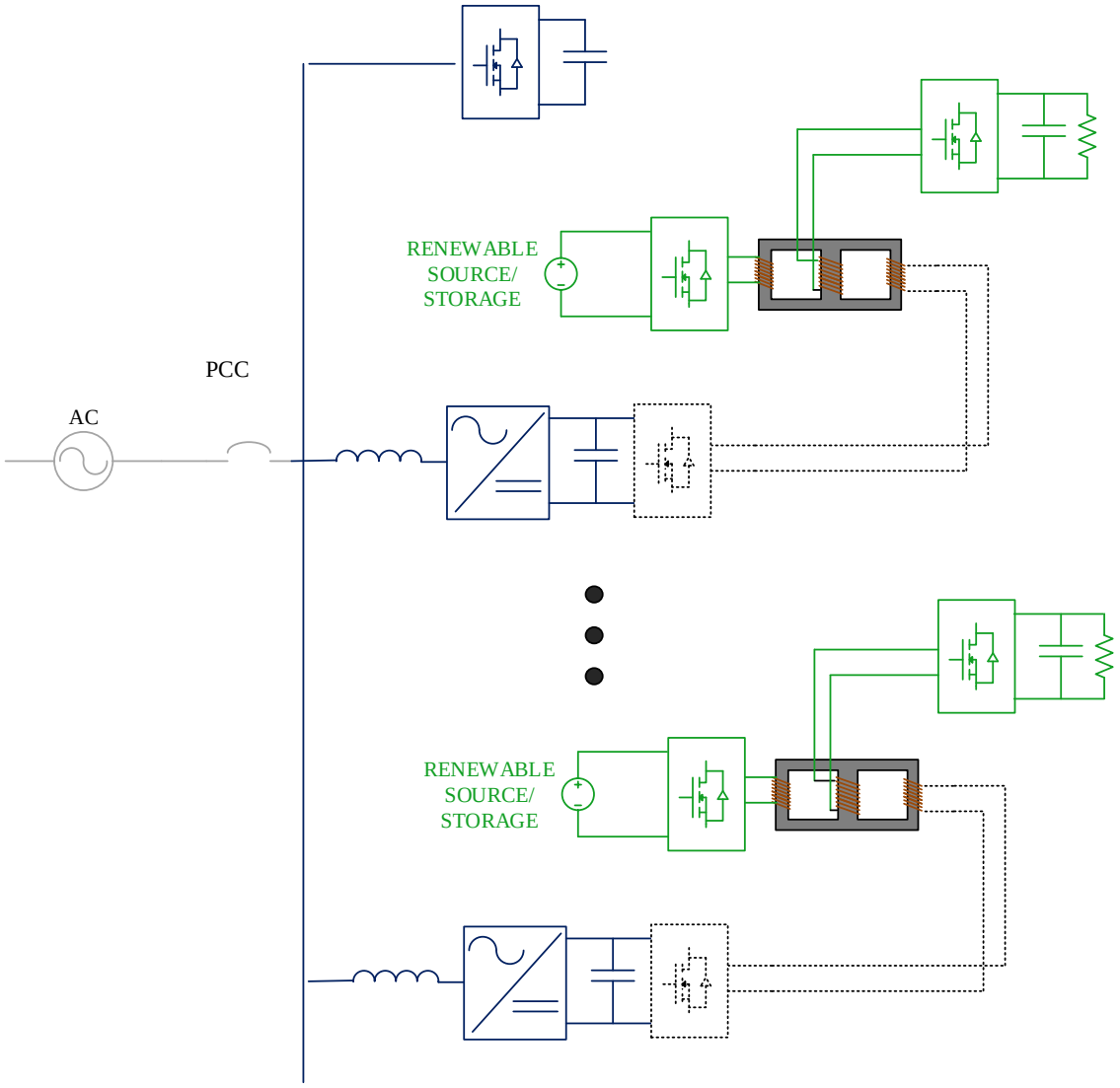


Figure 4.43: Black Start sequence (system diagram)

Fig. 4.43 shows the islanding scenario with the black start sequence. Once island has been detected and a micro-grid has been identified, one of the SST is identified as the master. Once that decision has been made, the other SST are considered slaves, with critical loads connected to them. The Master is to shed its own load as its most critical job is to regulate the PCC

voltage. Parallel to this the slave SST will maintain its critical load with the assumption that the renewable energy source coupled with the load capacitor (marked in blue in Fig. 4.43) provides enough energy to maintain uninterrupted power. Once the PCC voltage has been established, the rectifier bus further supports the critical load. In case the renewable energy sources have excess of energy, the front end converter provides a path for the power to flow out. In that case the master has to provide for storage for the excess energy.

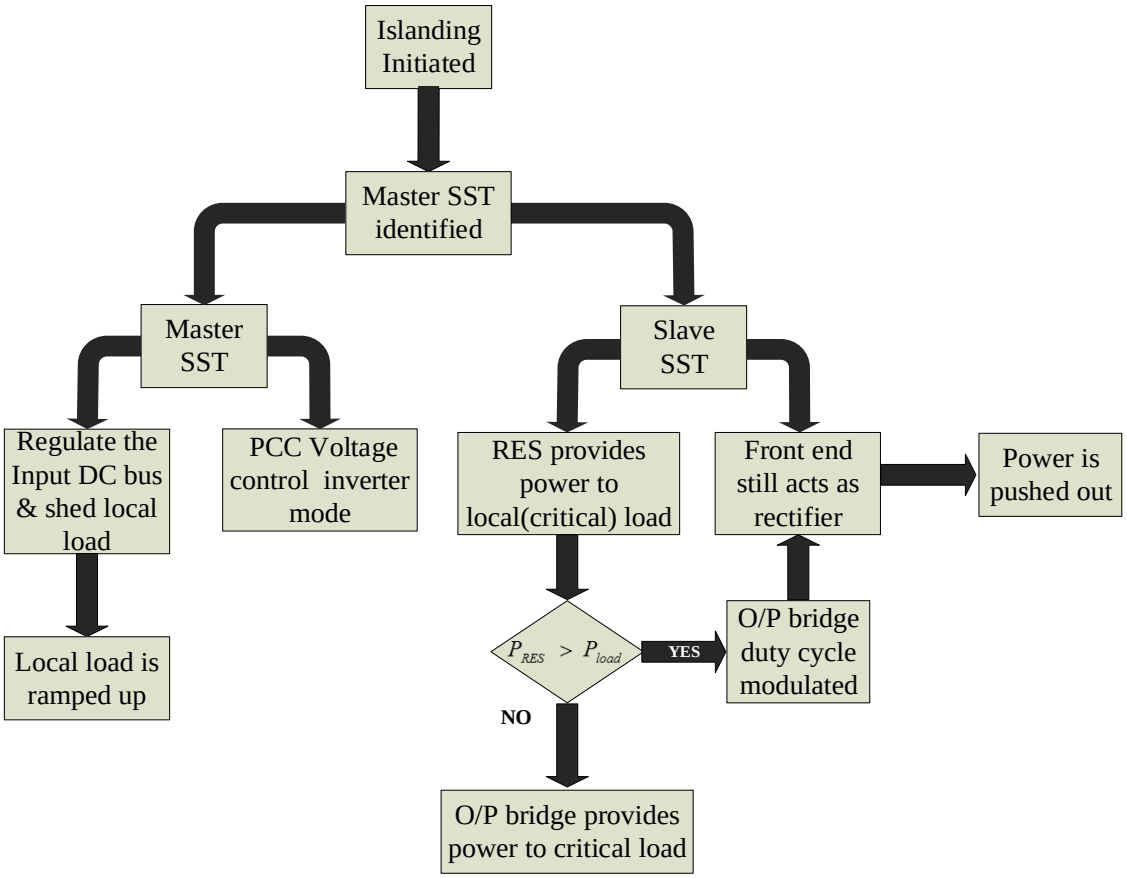


Figure 4.44: black start sequence flow chart diagram

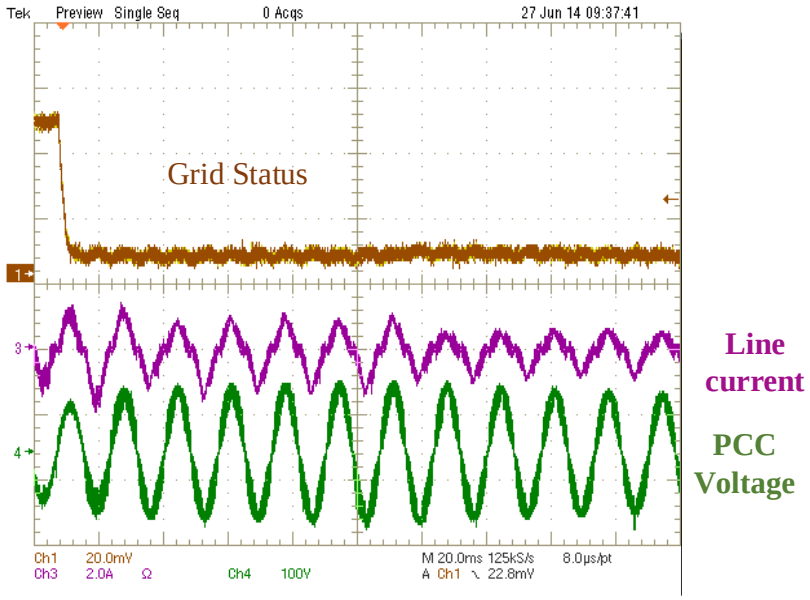


Figure 4.45: Black Start transient showing the PCC voltage and the line current

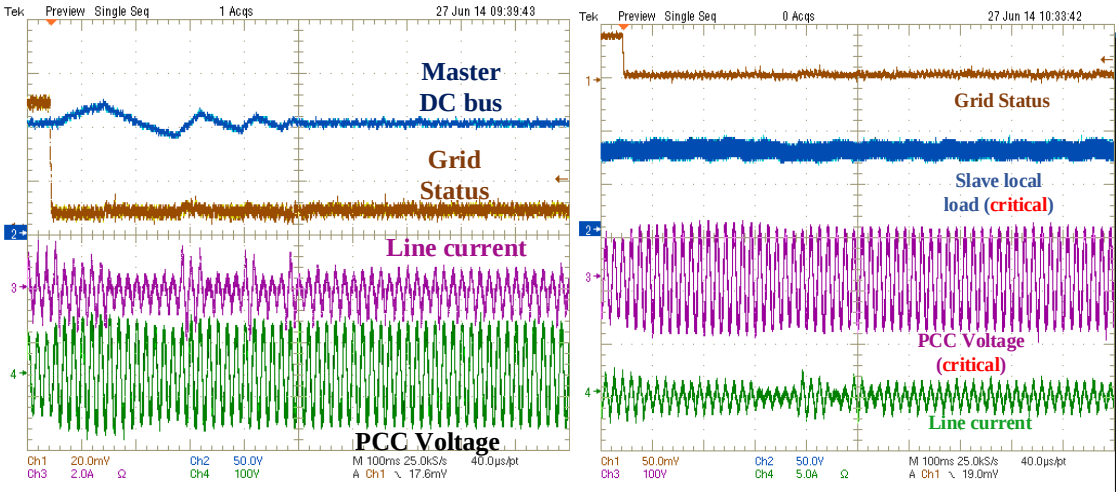


Figure 4.46: Experimental result showing the critical loads being kept undisturbed at the point of black start

4.17. Micro grid system stability

The front end control for the SST in Master Slave mode determines the micro-grid stability criterion. Fig. 4.47 shows the equivalent circuit diagram for the micro-grid in sequence 2 and sequence 3.

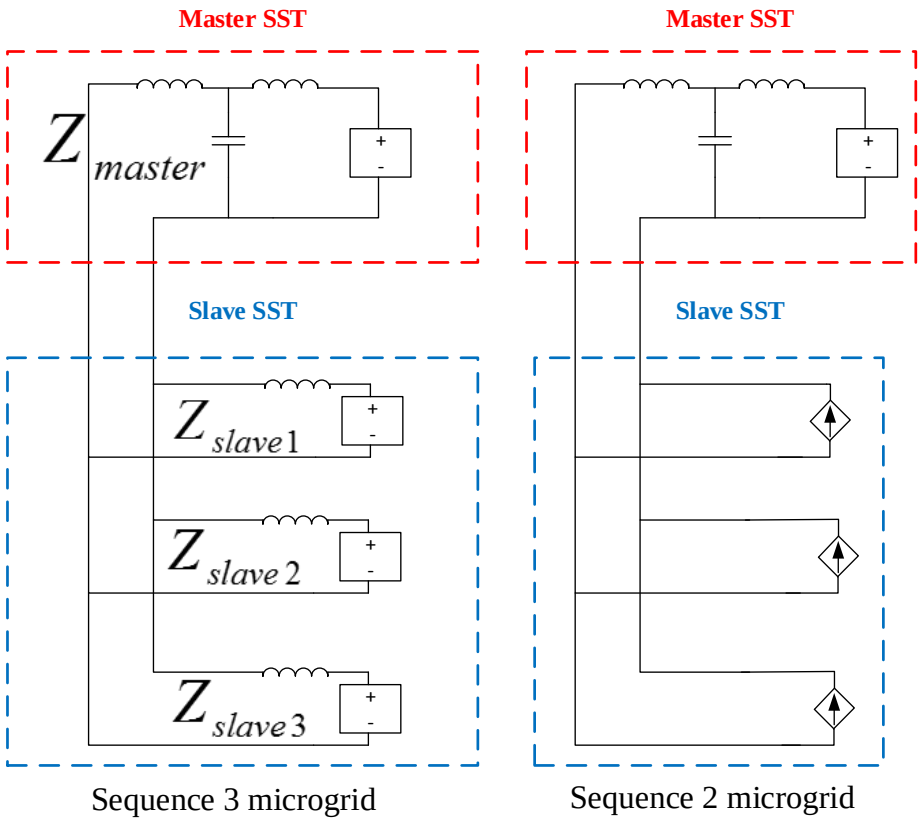


Figure 4.47: Equivalent circuit diagram for the micro-grid with sequence 3 and sequence2.

From Fig. 4.47 the sequence 2 micro-grid is inherently stable since the voltage sources and current sources do not interact with each other. However since in sequence 3 the front ends of the SST are all voltage sources, interaction is possible if the close loop controllers are not designed properly. The criterion for the closed loop stability is

$$Z_{master} \ll Z_{slave1} || Z_{slave2} || Z_{slave3} \; \forall \; f < f_{switching} \tag{4.10}$$

Therefore the close loop impedance of the master SST has to be lesser than the parallel combination of the impedances of all the slave SST [36]. With the increase in the number of slave SST this criterion gets more and more difficult to satisfy. Hence the sequence 2 is the best suited from the stability point of view. This leads to the sequence 4 explained in the following section.

4.18. Black Start Sequence 4

The sequence 4 was adopted to obtain greater stability for the micro-grid under transients. Fig. 4.48 shows the flow chart control diagram for the sequence 4. Here the front end acts like an inverter as in sequence 2 but the critical load is connected to the central limb and remains uninterrupted during the black start sequence. The tertiary limb is connected to the front end bridge and voltage of the DC bus is controlled. Upon islanding the following sequence of events take place:

- Master SST regulates PCC bus (same in all the sequences)
- Front end is current controlled inverter
- Bridge 1 & 2 are in phase and Bridge 3 is lagging both 1 & 2 (Fig. 4.48).

- Phase shift between bridge 1 or 2 and 3 is determined by the voltage regulation at the input bus of bridge 1
- Load can be regulated by PWM modulating Bridge 3

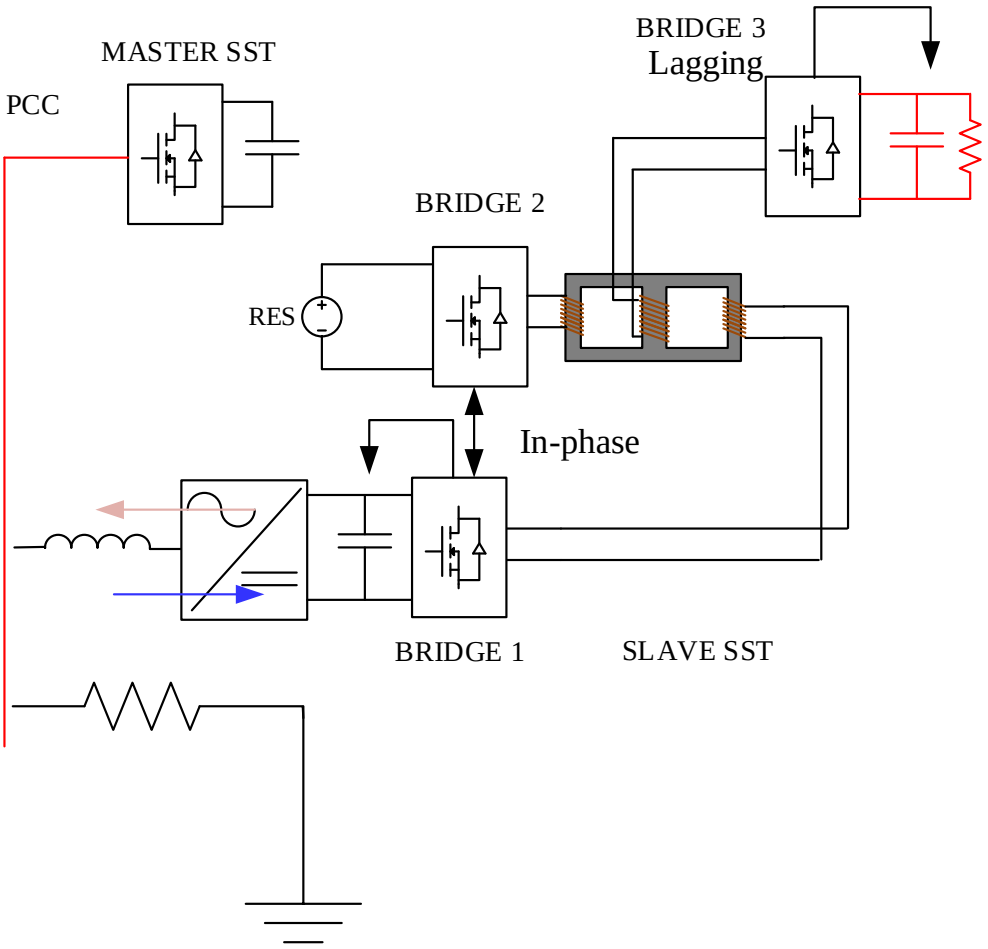


Figure 4.48: Sequence 4 Black start circuit diagram

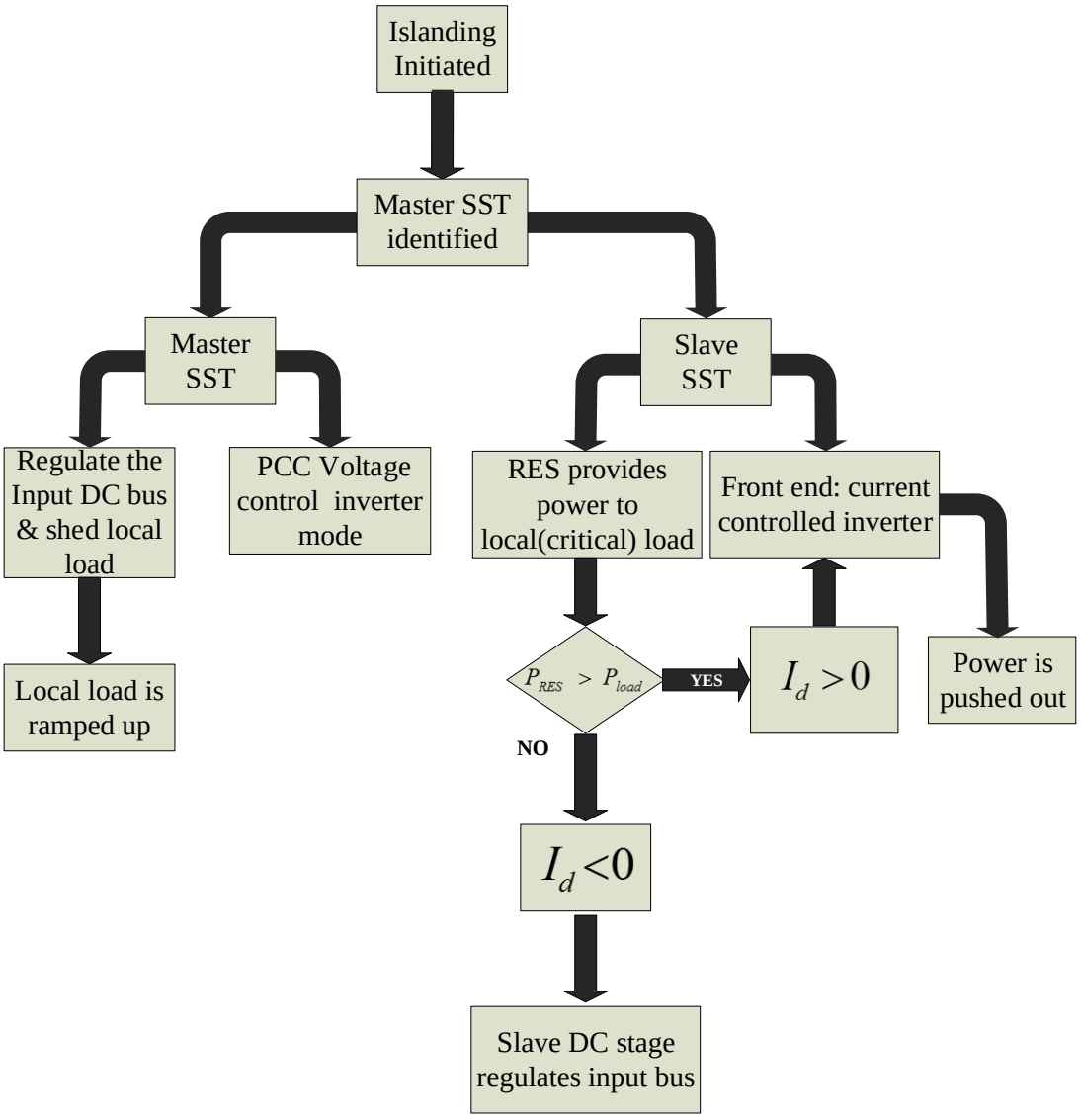


Figure 4.49: Flow chart diagram for the sequence 4 black start.

Depending upon the power availability at the RES, the switching of the DC stage will change.

Considering the case $P_{RES} < P_{load}$ the following is the switching scheme:

- Bridge 1 and Bridge 2 will be in phase
- Bridge 3 will be lagging

- The phase shift between 1or 2 and bridge 3 is dependent on the bridge 1 DC bus voltage.
- Voltage regulation on the load bridge 3 is made by duty cycle modulating bridge 3
- The I_{ref}^{d} is negative (i.e. power is flowing from the PCC into the DC stage) and a function of the difference between the power available at RES and the power demand at the load.

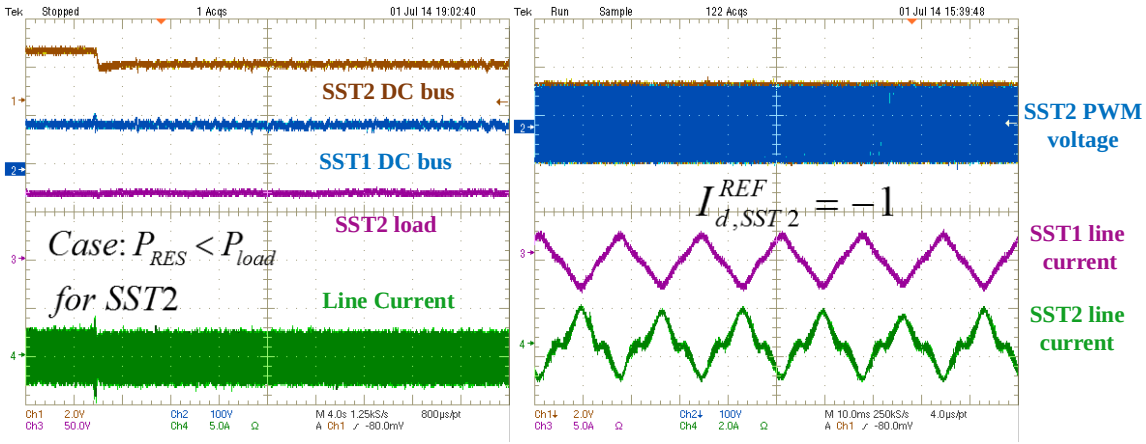


Figure 4.50: Experimental results for the black start sequence 4

Fig. 4.50 shows the experimental results at the instant of black start. The DC bus at the SST2 local load is undisturbed and the DC bus at the input of the master SST front end SST is undisturbed as well. However the SST2 DC bus after its front end has a sag that proves that the I_{ref}^{d} given to the front end converter is not high enough to push the input voltage of the SST2 front end high enough to its rated value. This shows that this mode of control needs a very good supervisory control for the power matching. The second figure shows the current

pushed out by the two SST (master and slave). They are in opposite polarity showing the $I^d_{master} > 0$ while $I^d_{master} < 0$ as it should be as per the control.

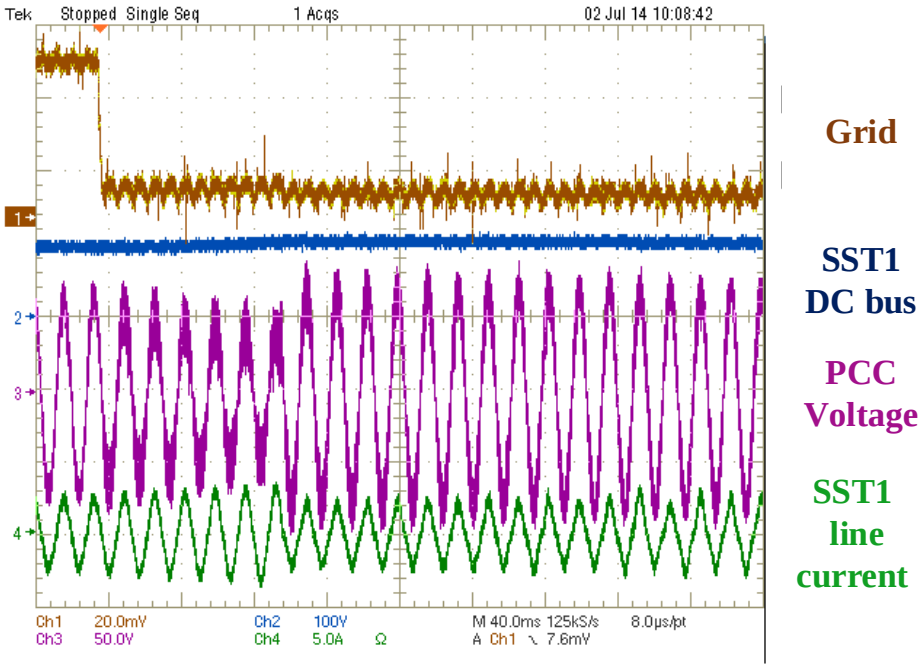


Figure 4.51: PCC voltage at the instant of black start (sequence 4)

Fig. 4.51 shows the PCC voltage at the instant of black start. Although there is a sag for a few cycles the voltage comes up and the micro-grid is stable. In the case where $P_{RES} > P_{load}$, the following is the switching scheme:

- Bridge 1 and Bridge 3 are lagging, Bridge 2 is the leading bridge.
- The phase shift angle is determined by the load requirement at Bridge 3.
- The bridge 1 DC bus is maintained by PWM modulating bridge 1

- The I_{ref}^{d} is positive (i.e. power is flowing to the PCC from the DC stage) and is a function of $P_{RES} - P_{load}$. This mode is very similar to the sequence 2.

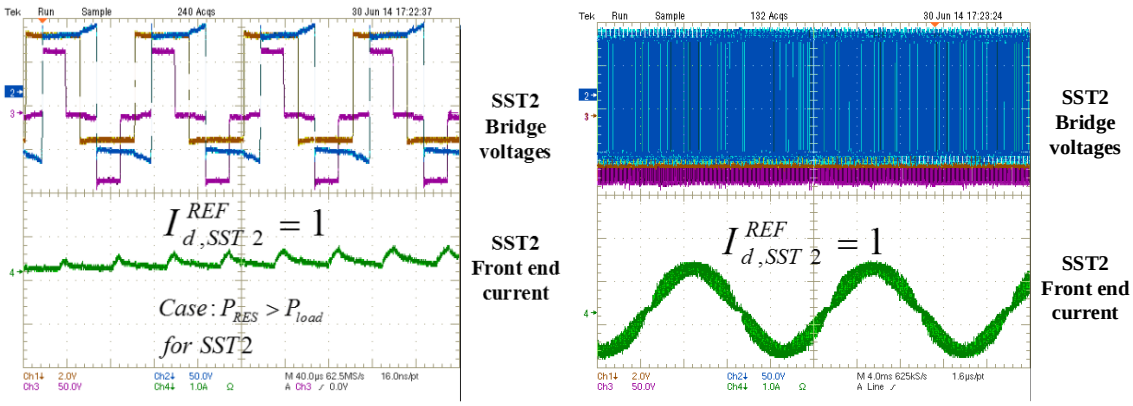


Figure 4.52: DC stage and front end current wave form after islanding has occurred

Fig. 4.52 shows the steady state results for the islanded conditions with the DC stage showing the PWM voltage waveforms and the AC stage showing the current injected into the load. So long in the discussions the condition that $P_{RES} >> P_{load}$, has been neglected. But this is a possibility when the generated RES power is higher than any load requirement in the micro-grid. In that case the master needs to supply storage to store the excess power. Fig. 4.54 shows the simulation results when the I_{ref}^{d} for the front end is ramped up from 5A to 10 A. The phase shift angle for the master is revered and the power flows into the DC stage and provided that there is a storage available, power flows into the storage device. The power flow diagram is shown in Fig. 4.53.

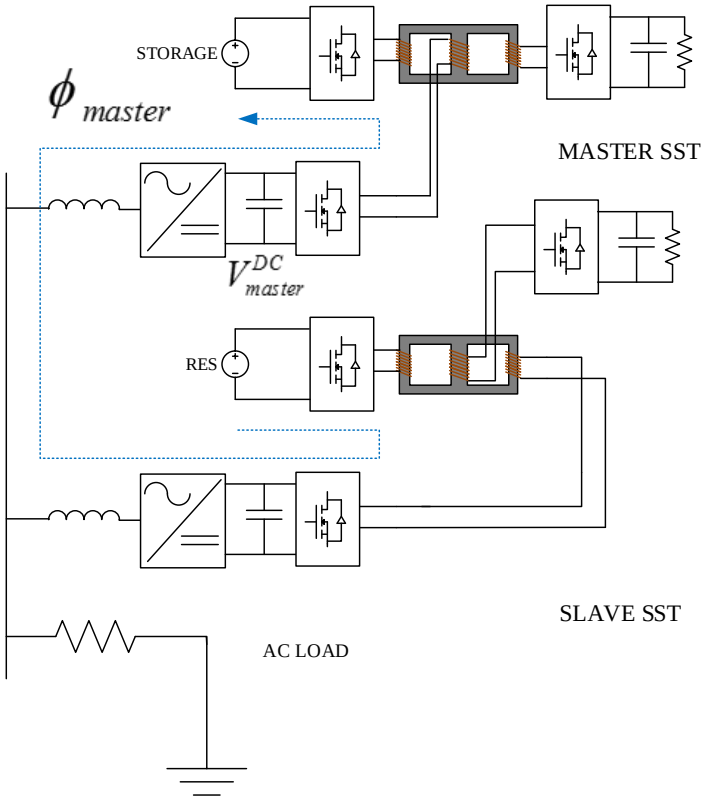


Figure 4.53: Power flow path in case of $P_{RES} >> P_{load}$

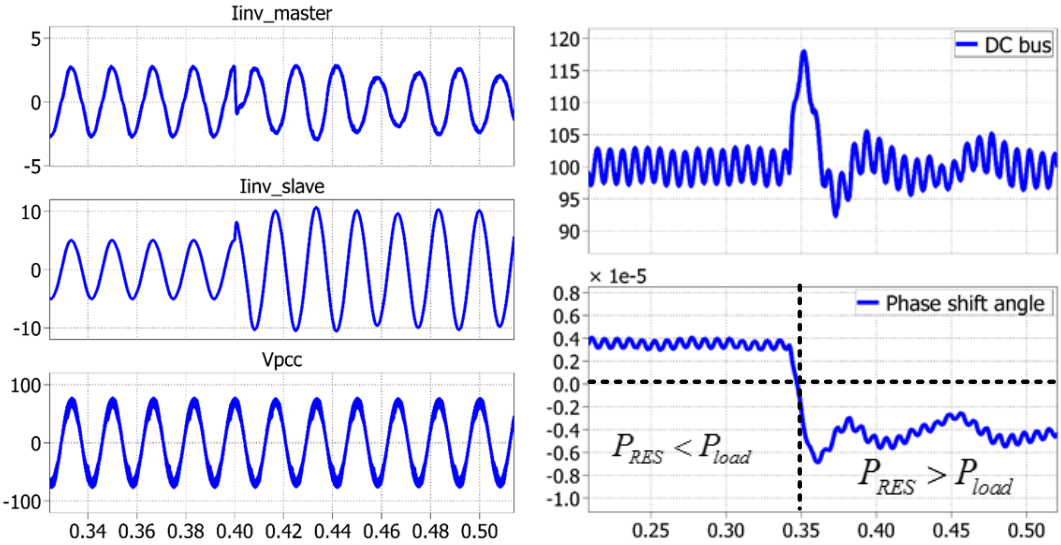


Figure 4.54: Power flow condition with $P_{RES} >> P_{load}$

4.19. Conclusions

In this chapter the solid state transformer application for the DAB converter was discussed. The results obtained in this chapter are summarized as follows:

- In the single phase cascaded solid state transformer topology a DC-DC stage was proposed based on the MLC-DAB topology. The proposed topology was shown to require no voltage balance for the cascaded stages and the DC stage. Experimental prototype of the MLC integrated SST was developed and the voltage balance was shown under startup and voltage sag conditions.
- During hard start to a single phase grid, the in rush current problem was shown for the MLC-SST as well as the conventional SST topology. To limit the inrush current a soft start algorithm was developed and implemented in a single phase cascaded SST topology. The algorithm was verified with an experimental prototype using a DC power supply for starting the SST, and the line current was shown to be limited during startup.
- For integrating renewable energy sources to the grid, a Renewable Energy Hub topology was proposed based on the MLC-DAB topology with one of the peripheral limbs grid tied.
- A parallel SST based micro-grid test bed was developed in hardware consisting of two MLC-SST connected in parallel. The MLC-SST have renewable energy sources connected to the DC terminal. Steady state grid tied operation was shown with the sources operating in input current control mode.

- A black start sequence was developed for a single SST supplying a critical load connected to the AC bus with load shedding on the local load connected to the SST.
- A black start sequence was developed for two SST supplying a critical load, where power balance between the SST are obtained using master-slave mode of control.
- Based on the critical loads connected to the SST, a black start sequences were developed and experimentally verified such that uninterrupted power is supplied to the critical loads.

Chapter 5 Conclusion

In the present thesis, novel current control strategies were developed for the Dual Active Bridge DC to DC converter. A multi-terminal Dual Active Bridge converter was developed for the purpose of integration of multiple renewable energy sources. A solid state transformer application for the dual active bridge converter was developed to demonstrate grid integration of renewable energy sources.

5.1. Summary of the main results

The main results obtained in the present thesis are summarized as follows:

- A duty cycle mode of control was developed for the dual active bridge converter. The proposed control was shown to remove DC bias from the high frequency isolation transformer current.
- A novel digital predictive current mode control was developed for the dual active bridge converter. The predictive control can be classified as follows:
    1. Phase shift control, where the transformer current is sampled once in the switching cycle and the output of the controller is the phase shift angle.
    2. Duty cycle control, where the transformer current is sampled twice in the switching cycle and the output of the controller is the duty cycle that modulates the secondary bridges of the DAB converter.

- Sensitivity analysis of the predictive controller was done with respect to the leakage inductance of the transformer. A compensation algorithm was developed to make the controller insensitive with the variation in the leakage inductance. The algorithm was experimentally verified in a hardware test bed where an error in the leakage inductance was intentionally provided to the controller.
- The predictive phase shift control and the predictive duty cycle control were both experimentally verified with a step change in the current reference and it was shown that the controller is capable to track the change with in one cycle.
- In the dual active bridge high frequency transformer, a moving window averaging was done to track the DC bias in the magnetizing current. A compensation algorithm was implemented by giving a compensating bias in the switches (primary or secondary) and the DC bias compensation was demonstrated.
- For the purpose of integrating multiple renewable energy sources a multi-input single output multi terminal dual active bridge converter was developed using a multi-limb core transformer for the high frequency isolation stage. Electrical equivalent circuit for the transformer was developed using the gyrator concept. The power transfer equation was developed and the small signal characteristics were analyzed.

- Analysis was done to show the multi-limb transformer based DAB topology using less copper and magnetic core material compared to a series connected multi-terminal DAB.
- A PWM based input current control was developed to integrate different renewable sources operating at different power points. The developed control algorithm was experimentally verified in a lab test bed where the multi-limb-core based dual active bridge converter was developed with four input terminals and one output terminal.
- For the multi-terminal dual active bridge converter, a power smoothing algorithm was developed where one of the input terminals were connected to an oscillating power source (wave energy emulator) and another input terminal to a storage device (battery). The developed algorithm was experimentally demonstrated to provide a regulated output using the battery as an energy buffer by alternatingly charging and discharging it.
- Solid state transformer application of the multi-terminal dual active bridge converter was demonstrated for the purpose of grid integration of renewable energy sources. Analysis was done followed by experimental verification to show the multi-terminal topology having a simpler control in terms of voltage balance, compared to a two terminal DAB topology.
- A soft start algorithm was developed for starting then solid state transformer using an auxiliary power supply and integrating it with the grid. The algorithm

was experimentally verified in a test bed and was shown to reduce inrush currents at startup.

- A micro-grid test bed was developed with two single phase solid state transformer with the multi-terminal dual active bridge converter for the DC stage. Islanding was done and a black start sequence was developed.
- The critical load points in the micro-grid was recognized and black start sequences were developed to supply uninterrupted power to the critical loads.
- The different black start sequences were experimentally verified and the un-interruption at critical load points were demonstrated during the instant of islanding.

5.2. Further scope of future research:

Since the control algorithms and topology developed in the thesis has been demonstrated on a low voltage prototype, high voltage application can be developed in the future.

The predictive current control algorithm from chapter 2 was focused on a single phase DAB topology, a similar predictive current mode controller may be developed for the three phase DAB topology. The DC bias monitoring algorithm as developed for a single phase DAB transformer may be implemented for a three phase transformer for the three phase DAB topology. A different reference can be adopted for the three phase topology. Instead of implementing the controller in the time domain as has been implemented in chapter 2, a space vector based approach can be adopted for implementing the control in three phase domain.

The multi-limb core transformer based DAB developed in chapter 3 may be implemented at higher voltage. Due to high $^{dv}/_{dt}$ at higher voltage, common mode currents will be an important constraints in the design of the transformer.

The micro-grid application for the MLC-DAB based SST was developed for a low voltage prototype in chapter 4. A high voltage prototype may be built with more renewable energy integration and storage integration. Islanding algorithm may be implemented with grid voltage sag and swell detection. Under islanded condition the stability of the micro-grid may be studied with power fluctuation in the renewable energy sources. Appropriate sizing of the storage components can be done based on these power fluctuations in the renewable energy sources.

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