

ABSTRACT

MIRZAEI TESHNIZI, HESAMEDDIN. Medium-Voltage DC Power Conversion and Distribution for Efficient Electric Power Delivery in Shipboard and Mobile Mining Application. (Under the direction of Dr. Subhashish Bhattacharya).

Medium-Voltage DC (MVDC) distribution and power conversion systems have become more attractive in recent years due to advances in power electronic technology. It can be used in a range of high power applications such as shipboard, electric propulsion in large multi-motor drives, and so on.

In this dissertation, first, the concept of a MVDC amplifier system for shipboard application is proposed. The dc amplifier system must provide a medium-voltage dc bus with the possibility of superposing a high bandwidth time-varying signal and should be capable of producing voltage excursions at a high slew-rate. This is intended to facilitate the development of new technologies, i.e., new high power non-linear loads based on power electronics, in all electric ships as part of the newly proposed MVDC ship power system. To achieve the required system characteristics, a specific ‘hybrid front-end’ is proposed in which a high-power, line-commutated multi-pulse thyristor-based front-end, which serves as the main AC-to-DC converter, is integrated with an IGBT-based DC active power filter (SDAF) connected in series on DC-bus. The system parameters and specifications for the MVDC amplifier system are set forth, and the proposed system solution is validated through both simulations and experimental results based on a 12-kVA, 400-V laboratory-scale DC amplifier test-bed.

Second, hybrid front-ends have also shown great promise in increasing the existing state-of-the-art AC-to-DC power conversion in large mobile mining equipment such as shovels and draglines. Hybrid front-end (HFE) converters based on hybrid topology of mature diode-

/thyristor-bridge technology and IGBT-based, AC active power filters have shown a path towards a simpler, more efficient and more reliable system. In this hybrid circuit topology, a 12-pulse thyristor-based AC-to-DC rectifier supports the main active power flow and an IGBT-based active power filter, which shares the same DC-link, is connected to point of connection to power grid for reducing total harmonic distortion (THD) and for providing partial VAR support. The system performance and control are validated through both steady-state and dynamic simulations. The modeling, design and digital control of active power filter in a 12-kVA, 208-VAC, 450-VDC laboratory-scale test-bed are presented. Comprehensive experimental results are presented which prove the feasibility, demonstrate different functionality, and show promising performance of the system in term of total efficiency, THD and reactive power compensation.

Third, size and weight are critical constraints in any application where space is limited such as in shipboard power system, mobile mining and so on. Thus, high switching frequency and high power density operation is required. Power semiconductor devices with high-voltage, high frequency and high-temperature operating capabilities are the enabling technology for more efficient and compact power conversion. A comparative design study of a high power medium-voltage converter with a 6.5 kV Si-IGBT/Si-PiN diode, a 6.5 kV Si-IGBT/SiC-JBS diode and a 10 kV SiC-MOSFET/SiC-JBS diode is presented. It is shown that the 6.5 kV Si-IGBT incorporating an anti-parallel SiC-JBS diode, with its high efficiency performance up to 5 kHz switching frequency, is a strong candidate for MW-range power converters. The 10 kV SiC-MOSFET/SiC-JBS diode remains an option for higher switching frequency (5-10 kHz) high power converters.

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Medium-Voltage DC Power Conversion and Distribution for Efficient Electric Power
Delivery in Shipboard and Mobile Mining Application

by
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Chapter 1 Introduction

1.1 MVDC Amplifier Work Motivation

In modern electric ships, there is demand for both energy and power. Traditionally, most of the energy produced onboard a ship is being supplied to the ship's propulsion system. Fortunately, the changes in propulsion system characteristics, such as top speed and acceleration, have been gradual and slow and thus, it has been possible to employ new energy sources and technologies to supply this extra energy demand via conventional ship electric power system [1], [2]. But, with the ships becoming more and more electric and with the nature of the electric loads on board such ships evolving from more energy demanding to more power demanding [2], [3], alternatives to the conventional ac power system are being considered.

Navy is embarking on the development of a Medium-Voltage DC (MVDC) (6-8kV) system in the Next Generation Integrated Power System (NGIPS), as shown in Figure 1, for application on future surface ships and submarines as a means of providing better fuel economy, architectural flexibility and electricity for high energy mission systems. The MVDC system, as proposed in navy's NGIPS technology roadmap [5], [6], will accommodate increased system power capacity using ship's limited available onboard space and weight considerations.

The MVDC system presents many advantages, like high frequency operation, transformer size reduction, higher power density, and potentially higher efficiency, however,

lack of design practices with respect to new fault detection and isolation techniques; the establishment of design methods to ensure system stability under highly non-linear loads; the standardization of methods for controlling prime movers and sharing load between power generation modules; and the development of new grounding strategy remain important technical challenges in implementing the MVDC system [4]-[8].

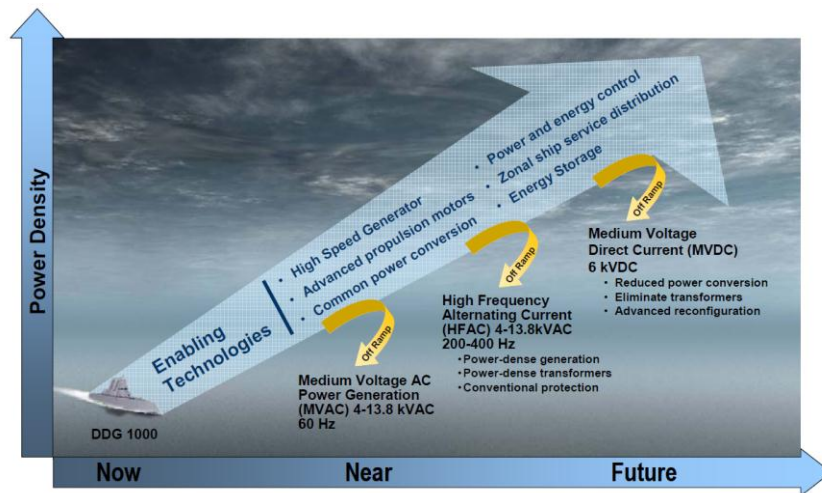


Figure 1 MVDC power system as the enabling technology for future ships [5].

In order to assist in de-risking the new MVDC technologies and developing new design practices, a test bed with sufficient experimental control capabilities is required. In particular, a highly controllable medium voltage dc bus must be generated. This can be done with a medium-voltage dc power amplifier system. The dc amplifier system must provide a medium-voltage dc bus with the possibility of superposing a high bandwidth time-varying signal and should be capable of producing voltage excursions at a high slew-rate.

1.2 Hybrid Front-End Converter Work Motivation

Surprisingly, it has not been very long since AC drive systems have been developed for almost a century old electrified mining industry. Mining apparatus, in particular excavation machines are used for material removal in surface mining applications and are typically classified as shovels, bucket wheel excavators, and draglines. Figure 2 is a representative diagram of the AC drive systems for multi-motor systems such as shovels or draglines in mining industry. The objective of the mines is to achieve the movement of the highest possible payload per hour while minimizing operating costs over the lifetime of the machines. The AC drive system for mining applications could not have succeeded without showing this improved performance factor which translates to a higher production rate compared to the traditional, well-practiced DC alternative [46]-[51].

Large mines are often located in the areas with limited infrastructures. This fact means commercial or grid connected power is not typically available and mostly it is generated at site. Therefore, to comply with utility or on-site generation plant requirements especially with respect to harmonics, active front-end (AFE) rectifiers have been chosen as the preferred front-ends for mining converters [46], [47], [51]. However, limited controller performance capability of the AFEs and reliability requirements lead to increased number of converters (can be more than 40 MW-AFEs in parallel) and overdesign of each converter [51].

On the other hand, there are sites where the regenerative power cannot be fed back to the mining distribution system, like Pribbenow mine located in Colombia S.A. with the

generation capacity of 24MW [54].The practical solution currently is simply to dissipate the excess energy into the resistive chopper banks to keep the DC link voltage of the AFEs within the acceptable range [46]-[50]. Figure 2 presents a representative example of load cycles in two major motoring and regenerative regions of a typical operation window showing a possibility to capture a large amount of regenerative energy.

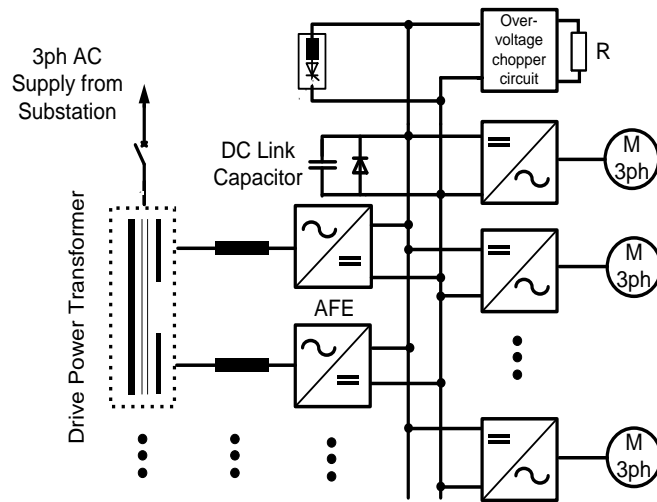


Figure 2 Circuit diagram of modern mobile mining equipment [51].

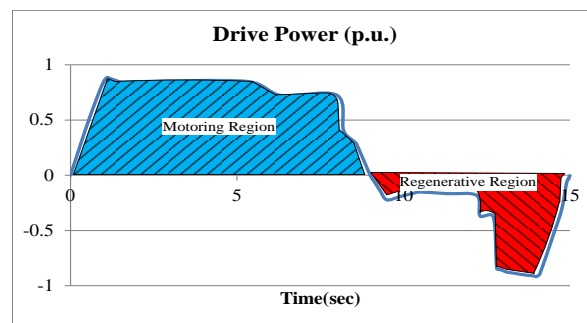


Figure 3 Example of a typical mining load profile showing major motoring and regenerative modes [51].

To solve the issues posed by the peak power demand, improve the performance, and enable smart energy utilization and less dependency on fossil fuels, peak shaving strategy is proposed in [53]. The regenerated power produced by the excavator is stored in an energy storage system and is used to reduce the peak demand of the drive system. Reduced peak demand not only reduces the energy costs but also provides significant reduction in investment as the power rating of the system components reduces.

Although the proposed ultracapacitor integrations have clear benefits to the system especially in terms of grid side peak current shaving and energy management of the mine; however, converter components rating of either electrical or mechanical parts, would not change significantly for large mining machines. It can be shown that the benefits from possible downsizing of components by utilizing ultracapacitor cannot be realized for a dragline and even for the shovel considering the desired harmonic performance, number of spare converters, weight and volume.

As a means of facilitating integration of supplementary ESS to mining electrical system, Hybrid Front-End (HFE) technology has been introduced in [51]. The HFE is based on the mature technology of multi-pulse thyristor-bridge and active power filter. The thyristor-bridge and active power filter share the same dc-bus. This topology has several benefits:

- Potential reduction in the number of FEs by utilization of available high current thyristors
- Controlled DC-bus voltage compatible for drives
- Controlled harmonic distortion as PCC of mine

- Controlled reactive power at PCC of mine for Volt/Var support
- Partial path for regenerative energy
- Built-in pre-charge circuit if needed

1.3 Si- and SiC-based Converter Design Work Motivation

In recent years, the need for power semiconductor devices with high-voltage, high frequency and high-temperature operating capabilities have been growing fast, especially, in military and power transmission/distribution applications, as the enabling technology for more efficient and compact power conversion [60].

In marine and shipboard military applications, size and weight are critical constraints in the design of shipboard power system (SPS), and thus, high switching frequency and high power density operation is required [1]. According to the office of naval research technology roadmap [5], [6], the navy is embarking on the development of a medium-voltage dc (MVDC) system of 6-8 kV voltage class in the next generation of integrated power system for future surface ships and submarines as a means of providing better fuel economy and architectural flexibility for high energy mission systems. The MVDC system will accommodate increased power capacity onboard by taking into consideration the ship's limited available space and weight constraints.

In the power transmission and distribution sectors, with the new smart grid application enabling large integration of renewable and distributed energy resources, 60 Hz distribution class transformers are envisioned to be replaced by more versatile, compact solid-state-based

transformers (SSTs) [62]. On the other hand, knowing that high power, high voltage transformers are the single most valuable asset in power transmission grid, concerns about enhancing the security of electricity in case of natural and man-made disasters in the 21st century, has led to research and development of emerging technologies such as solid-state transmission/distribution “recovery” transformer and active mobile substation (AMS) [63], [64]. These new technologies have to meet all functional requirements of standard 60 Hz transformers and, additionally, have to feature small size, weight and volume for transportability and ease of installation.

High voltage power semiconductors are at the core of any high power, power electronic conversion system. Thus, a comparative design study of high power semiconductor devices in medium-voltage converter application is needed to evaluate different technologies with respect to switching frequency capability, power loss and efficiency. The outcome of this design study provides a roadmap for high power application of each power semiconductor technology, especially, with regard to switching frequency capability and physical thermal limit.

1.4 Dissertation Outline

In chapter 2, MVDC system architecture for shipboard application is studied. Then, the concept of a medium-voltage dc (MVDC) amplifier system based on multi-pulse thyristor-based rectifier integrated with series DC active filter is proposed. This chapter sets forth the set of parameters and specifications of the medium-voltage dc amplifier system and proposes a specific circuit topology to achieve the required characteristics. Design issues of a medium-

voltage DC amplifier with a multi-pulse thyristor bridge front-end are presented. Simulations along with experimental results for a laboratory-scale test-bed are presented to verify the feasibility and to demonstrate highly dynamic performance of the proposed system configuration.

In chapter 3, a hybrid front-end (HFE) converter system for large mobile mining machines is presented. The current state-of-the-art system including both passive front-end (diode- or thyristor-based PFE) and active front-ends (IGBT-based AFE) and supplementary energy storage integration are presented. Steady-state and dynamic performance investigation and simulation of the proposed system is provided. Subsequently, design, modeling and implementation results of a laboratory-scale HFE test-bed are presented.

In chapter 4, a comparative design study of high power three-level neutral-point-clamped (3L-NPC) converter with 6.5 kV Si-IGBT/Si-PIN diode, 6.5 kV Si-IGBT/SiC-JBS diode and 10 kV SiC-MOSFET/SiC-JBS diode has been carried out. Equivalent circuit model, switching characteristics and loss measurements for 100 A power device modules are presented. Subsequently, a design methodology for the medium-voltage converters are presented based on switching characteristic and safe-operating-area (SOA) of those devices. Then, the developed power module models are utilized to evaluate power loss and efficiency of medium-voltage converters. Finally, chapter 5 presents the conclusion of the work.

Chapter 2 **Medium-Voltage DC Amplifier System for Shipboard Application**

2.1 Introduction

In a modern navy warship there is demand for both energy and power. Most of the energy on such ship is supplied to the propulsion system. Fortunately, the changes on the requirements of the propulsion systems, i.e. top speed and acceleration, have been gradual and thus, it has been possible to employ new energy sources and technologies being constrained to the limited ship space to cope with such condition even under traditional ship electric power system [1], [2]. This is has not been the case for the power requirements and there has been continuous radical shift on this front. The number of electric power mission loads and weapons such as electromagnetic launchers, rail and laser guns are increasing radically requiring enormous amount of power rather than energy [3]; and therefore, there remains the challenge of how to keep up with this soaring electric power demand in a ship's limited available space. Figure 4 compares electric power requirements of a line cruiser and a modern electric warship.

The obvious solution to this problem is to increase the ship power density. In the first attempt to tackle this issue, Integrated Power System (IPS) was proposed meaning a shared electric power generation for all types of ship electric load [4]. This was in contrast to the inefficient traditional approach of having dedicated generation for both propulsion and ship service loads.

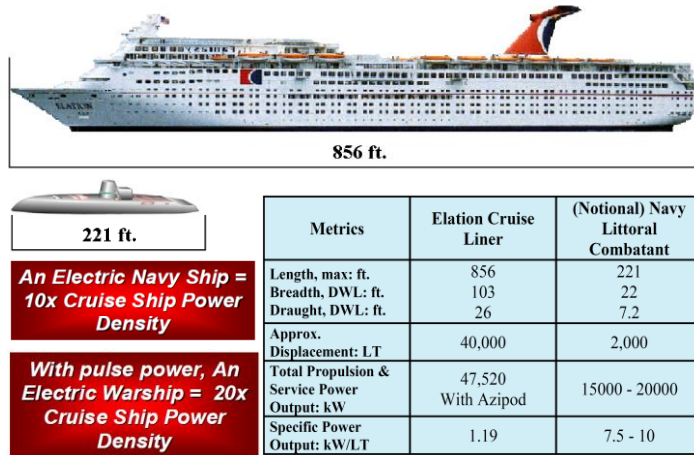


Figure 4 Comparison of power requirements of a line cruiser and an electric navy warship [1].

However, even the new IPS power system using conventional Medium-Voltage AC (MVAC) distribution system, which has been used for many years on navy ships, falls short of answering these soaring power demands due to its bulky infrastructure mainly because of huge, high power, 60-Hz three-phase transformers. This limits the usability of MVAC system for modern navy warfare ships which are geared toward more advanced electric type of loads in future. Considering the major issue of power density with future combatant ships, the Next Generation Integrated Power system (NGIPS) roadmap, developed by the Electric Ship Office (ESO) of Office of Naval Research (ONR), suggests the Medium-Voltage DC (MVDC) distribution as a viable solution to increase power density on the ship [5], [6]. Figure 5 shows the need for the MVDC power system as power density requirements onboard naval warships keep considerably increasing for future combatant ships.

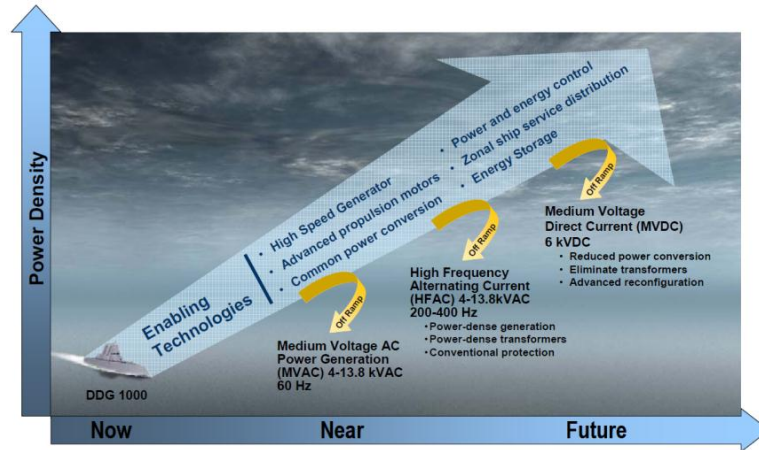


Figure 5 MVDC power system as the enabling technology for future combatant ships [5].

In comparison to a conventional AC system, the following advantages can be listed for a MVDC system [5]:

- High frequency operation and transformer size reduction
- Simpler cabling and potential for reduced size and weight
- Ease of paralleling generation units
- High power transfer capability based on the selected medium-voltage DC level
- Better fault controllability with control

Although the MVDC power distribution concept seems to be very attractive, there are important design issues and practical challenges that need to be addressed in order for it to become fully operational. Of special importance are the lack of design practices and guides with respect to fault detection and isolation techniques, the establishment of design methods to ensure stability under highly non-linear loads, the standardization of methods for

controlling prime movers sharing load between power generation modules, and the development of new grounding strategies, remain important technical challenges in implementing the MVDC system [5]-[8].

2.2 MVDC Power System for Shipboard Application

An example of integrated MVDC power system with both active (switching or non-linear) and passive (linear) loads hanging from the DC-bus, is shown in Figure 6. Active loads consist of switching DC-to-AC variable speed drive (VSDs) for propulsion, DC-to-DC converters for interfacing energy storage devices (ESDs), and solid-state transformers (SSTs) to adjust MVDC-bus to proper DC and/or AC voltage level for ship service and critical mission type of loads. The main “front-end (FE)” converter highlighted in Figure 6 is a medium-voltage, multi-MW, AC-to-DC converter which supports the DC-bus and needs to have high efficiency performance and satisfactory harmonic distortion profile on both AC and DC sides. For the purpose of FE realization, two main converter technologies can be considered: line-commutated front-ends and forced-commutated front-ends, studied separately in what follows.

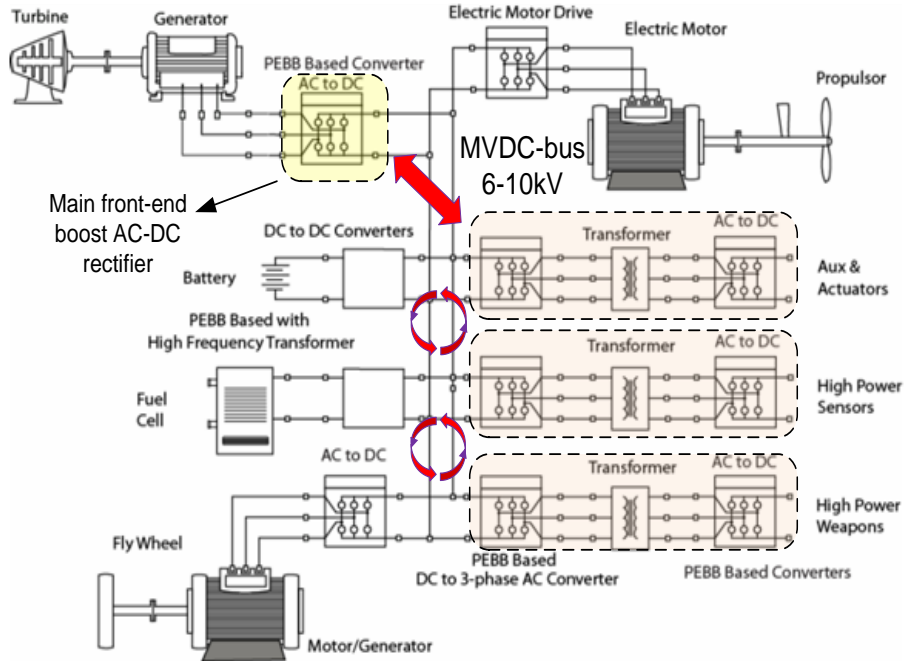
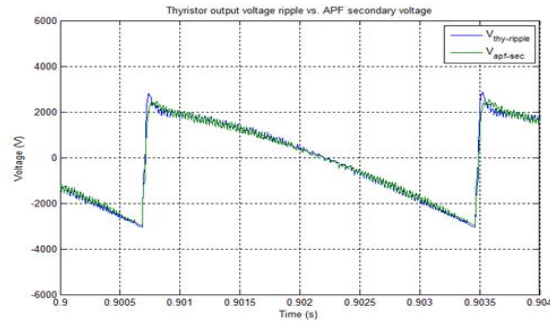


Figure 6 An integrated naval ship MVDC power system with different kinds of load hanging from DC-bus [1].

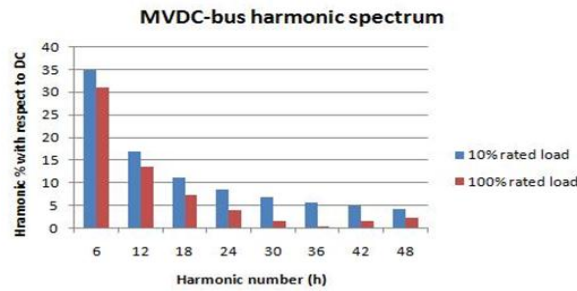
2.2.1 Line-Commutated Front-Ends

The line-commutated FEs consist of either multi-pulse diode-bridges or multi-pulse thyristor-bridges. The switching action in these converters occurs at 60-Hz line frequency; and therefore, they have a very high efficiency performance. In the case of multi-pulse thyristor-bridge configuration, the switching pulses can be delayed in order to regulate the DC output voltage. However, both these converters produce intrinsic harmonics on the DC-side that needs to be dealt with. Figure 7 shows AC ripple component of DC-bus and its corresponding harmonic frequency spectrum for a 20-kV DC, 5-MW, 6-pulse thyristor-bridge FE. As it can be seen, the voltage peak-to-peak ripple amplitude is 4 kV with harmonics corresponding to $6n$, with n being a positive integer, multiples of line frequency.

The 20-kV output DC voltage corresponds to rms AC input voltage of 15.2 kV and firing angle of 22°.



(a)



(b)

Figure 7 DC-side ac voltage ripple of a 5-MW, 6-pulse thyristor-bridge producing 20 kV medium-voltage dc bus (a), and dc-bus harmonic frequency spectrum at different loading condition (b).

2.2.2 Forced-Commutated Front-Ends

The force-commutated front-ends are three-phase AC-to-DC converters that are made of high-voltage, fully-controllable semiconductor power switches – thus, they are called active front-end (AFE) – like insulated-gate bipolar transistors (IGBTs) or insulated gate commutated thyristors (IGCTs). To achieve the medium-voltage DC-link for mega-watt (MW) power ranges, power devices are either connected in series in a 2-level power circuit

topology or are arranged in a multi-level circuit topology. In either case, due to switching loss consideration, semiconductor devices' power loss handling capability, and the type of cooling system applied, switching frequency for silicon devices is practically limited to 1-2 kHz [9]. This, on the other hand, means that the converter dynamic bandwidth is very limited which further implies that the MVDC-bus is more susceptible to non-linear load interactions within the system.

In the MVDC system, power electronic building blocks (PEBBs) convert the dc power to other levels of dc or ac voltage suited for the load [10]. An example of such system is given in [11], and depicted in Figure 9, where a 6-MW, 7.5-kV MVDC system is shown consisting of a 3-level, neutral-point-clamped (NPC) AC-to-DC converter, serving as the active front-end, and dual-active bridge (DAB) DC-to-DC converters, serving as PEBBs for converting the MVDC-bus to 1000-V DC-bus for power distribution to lower-voltage downstream loads. Many of the PEBBs DC-DC and DC-AC conversion units with tight output voltage regulation are constant power loads (CPLs) which present negative incremental impedance to the MVDC main AC-DC rectifier for certain voltage and frequency ranges [12]. Furthermore, it is shown in [13] that systems with CPLs which undergo large signal transients might end up having oscillatory responses if proper restrictions are not applied to the source impedance and CPLs. The DABs in Figure 8 constitute CPLs with tight out voltage regulation that could produce oscillatory disturbances on the MVDC-bus in response to large-signal transients. Sample scenarios of such disturbing, and potentially disruptive, events are simulated for the system of Figure 8. The simulations are carried out in MATLAB/Simulink for AFE switching frequency of 1080 Hz and the

simulation results for the MVDC-bus voltage response to 500-kW load step-up and step-down power excursions are shown in Figure 9. As it can be seen, large steady-state voltage ripples and severe transient voltage overshoots exist, which without proper control action, could disrupt and/or damage other sensitive loads, or in the worst-case scenario, ultimately cause the system to shut down.

Thus, it can be concluded the MVDC-bus power quality problems are either of periodic nature due to intrinsic harmonics caused by line-commutated FE technologies, or transitory/oscillatory nature caused by non-linear load interactions between the main FE and PEBBs hanging from the MVDC-bus.

An approach to damp the oscillations is by installing passive filters on the DC-link [14]. In this approach, the inertia of DC-bus is drastically increased such that the AC ripple component is decreased to the desired level and the DC-bus remains stiff through different loading conditions. While this approach is effective and works for a range of system configurations, it is bulky and costly due high number of large and expensive high-voltage capacitors, and it is inefficient because it is not able to dynamically adapt to changing system configurations and/or all loading conditions. In [15], a stabilizing controller using a nonlinear control method is used to make sure the DC-link remains stable under large signal CPL transients. This is not a generic solution to the problem since every DC-to-DC converter needs a special stabilizer; and moreover, in a MW MVDC system, the rating of such stabilizer would be large. Thus, there is a need for a fractionally-rated active device that can

act as a de-coupler or isolator such that these harmonics or disturbances can be decoupled or isolated from the system.

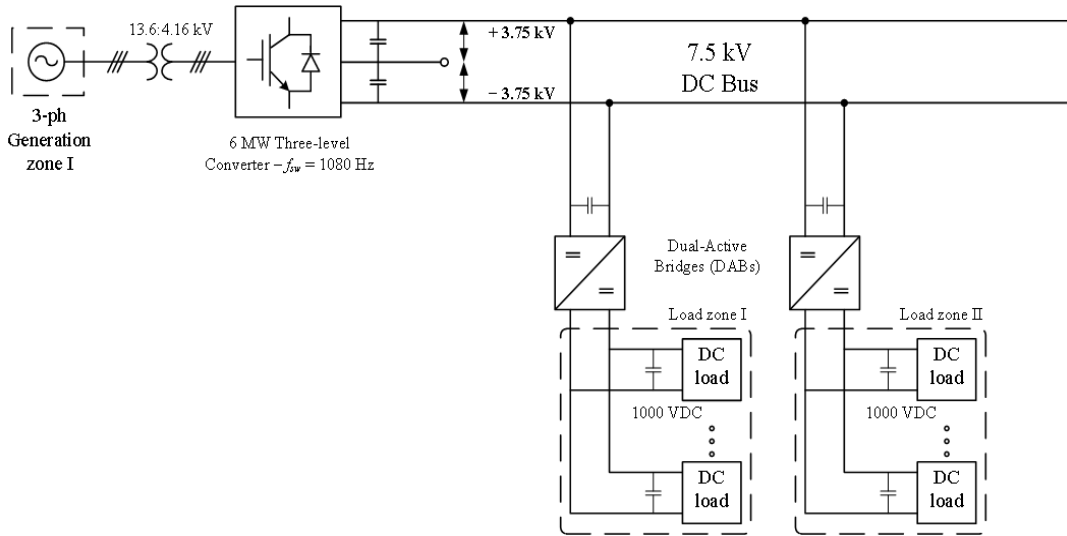


Figure 8 A 6-MW, 7.5-kV MVDC system consisting of a 3-level active front-end and dual-active bridge (DAB) DC-DC converters as active loads [11].

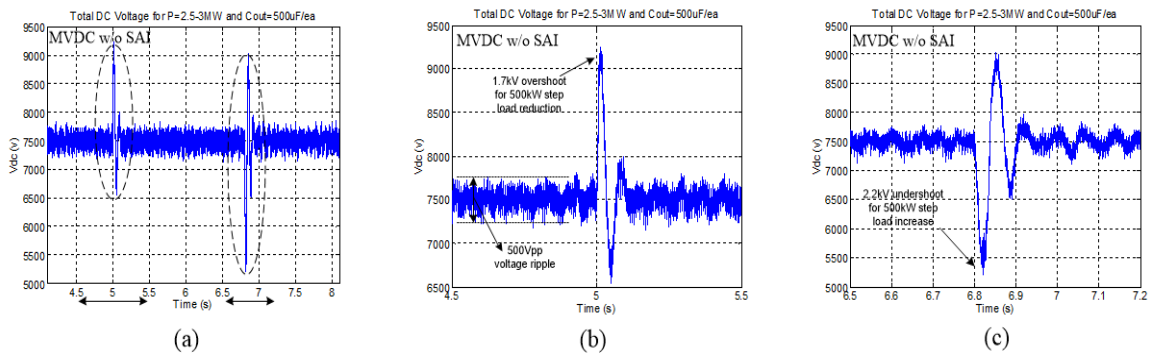


Figure 9 MVDC-bus voltage dynamics under 500-kW step load changes (a), zoomed out voltage response for the load step-down (b), and zoomed out voltage response for the load step-up (c) [11].

2.3 DC Active Filters

2.3.1 Introduction

In this section, methods to decouple and isolate interactions and disturbances in MVDC system are being studied. Basically, the methods fall into two categories: passive and active. Passive approach is mainly about installing more capacitor banks across DC-link to make it more robust during severe load power variations and/or non-linear interactions with the front-end such that the whole system remains stable under worst case and disturbances are kept bounded and within acceptable limits. This approach works fine but has the setback of changing system dynamics and requires more space; and therefore, offsets one major objectives of acquiring higher power density and reducing cost. Thus, the focus and effort in this section will be on active methods of filtering. These methods can be applied on both ac- and DC-side with respect to the main front-end rectifier. The AC-side active filtering techniques have been thoroughly visited and very well known in literature. However, for the obvious reason of disturbances/interactions happening on the DC-side and also, rectifier control system trying to decouple interaction on AC- and DC-side, AC-side filtering would not be as effective as DC-side filtering. Therefore, the focus will be on DC-side active methods also known as DC Active Power Filter (DC-APFs). In this context, an active modulator is either put in series, acting as series dc active filter (SDAF), or in parallel, acting as parallel dc active filter (PDAF). The DCAPF acts on the medium-voltage DC-bus such that it can controllably decouple any unwanted ripples and/or disturbances. DC-APFs have been applied to high-voltage dc (HVDC) [16]-[21] and magnet power supplies [22]-[33], but not to MVDC systems. Due to complete distinct nature of disturbances happening in MVDC

system, this section looks into design and control requirement of different DC-APF methods for such systems. The objective is to design the active filter with reasonable rating and size such it will sustain the system under worst case interactions and load variations. Hybrid approaches combining DC-APFs with passive DC filtering networks are taken to optimize the rating of dc active power filter system.

2.3.2 Circuit Topologies

In a DCAPF, an active modulator acts on the DC-bus such that it can controllably decouple any unwanted ripples and/or disturbances on the DC-bus. The modulator can be put in series acting as a controllable voltage source, or in parallel acting as a controllable current source. The operational concept is shown in Figure 10 in which the series modulator is acting as “Series DC Active Filter” (SDAF), and the parallel modulator is acting as a “Parallel DC Active Filter” (PDAF). The combination of these DCAPFs with passive filter leads to different hybrid topologies that are shown in Figure 11. A hybrid topology might be preferred over a pure active filtering solution due to better performance and size reduction of active elements in the modulator. On the other hand, the solution must be optimized such that it will not increase the cost or total size of the integrated system of rectifier and filter.

Traditional DCAPFs use transistor banks operating in the linear region and generate high losses due to large voltage drop and high current application [30]. Because of this, many other topologies were proposed. But, they can be classified in to two major categories: Series DCAPFs [24], [25], [31]-[35], and Parallel DCAPFs [36], [37]. In parallel configuration, DCAPF absorbs portion of load current ripple supplied by the rectifier. The larger the ripple impedance of the load, the better the compensation result. Therefore, when the injected ripple

impedance of DCAPF is not large enough compared to the impedance of load, i.e. at high load conditions, the ripple rejection and filtering performance of PDAF deteriorates for a given active filter rating [35], [37]. In series configuration though this is not the case. When the DCAPF is put in series with load, it shares the ripple voltage with load. Thus, it can be controlled such that the ratio of the injected ripple impedance by SDAF is far greater than load impedance; then practically independent of the load impedance, very small ripple voltage is produced across load terminals [35]. A relative comparison of active filter compensation performance is presented in Figure 12. As it can be seen, SDAF performance, especially at controller gain of unity, is superior to PDAF independent of load, whereas PDAF performance degrades with decreasing load. Therefore, SDAFs have better filtering performance over the parallel configuration due to its injected impedance being independently controllable regardless of load impedance at ripple harmonic frequencies.

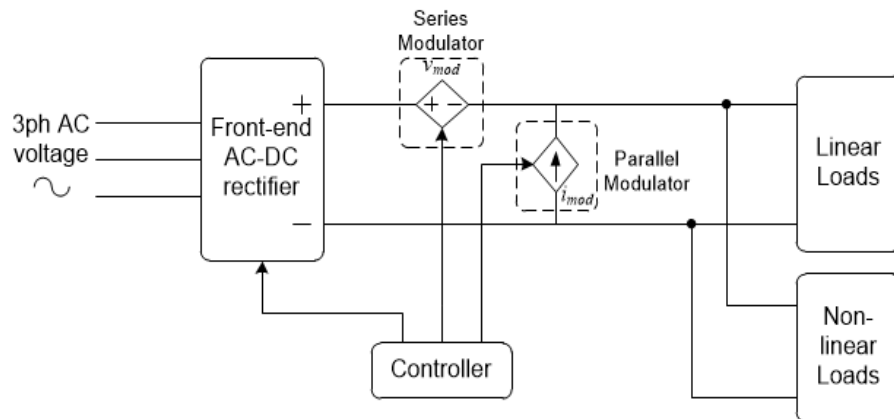


Figure 10 Series and parallel modulators acting on MVDC-bus to decouple/isolate ripples and disturbance.

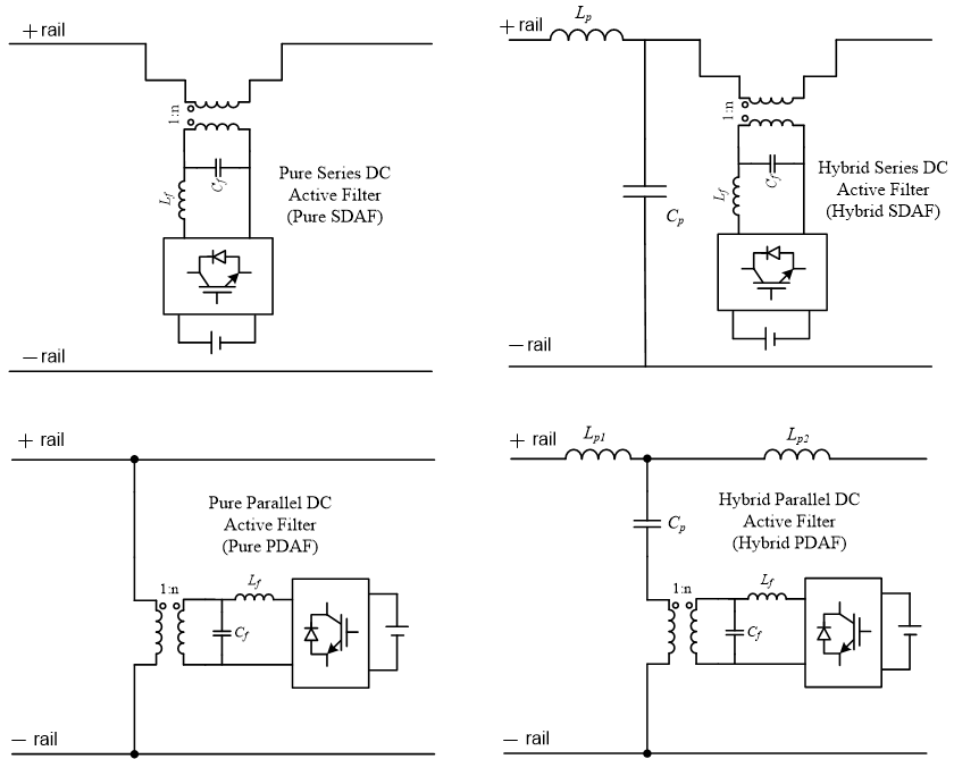


Figure 11 Pure series/parallel DC active filters and their possible hybrid topologies.

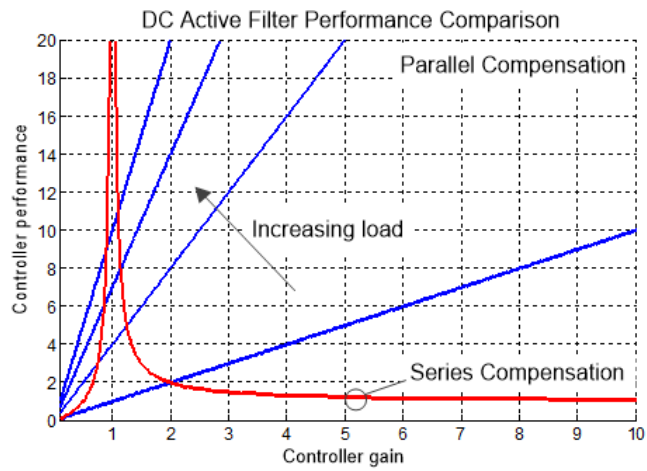


Figure 12 Relative comparison of series and parallel DC active filter performance.

2.4 Series DC Active Filter (SDAF) in MVDC System

For the MVDC system integrated with series DC active power filter (SDAF), both “phase-controlled rectifier” (PCR) and “active front-end” (AFE) rectifiers are considered. In both cases a hybrid series dc active filtering solution is adopted. The reason as will be demonstrated is that a hybrid filtering solution reduces active filter rating and results in better filtering performance.

2.4.1 Active Front-End (AFE)-based MVDC System

In the MVDC distribution system with AFE, such as the one shown in Figure 13, there is a main AC-to-DC active front-end rectifier which supplies all the active loads hanging from the DC-bus. To ensure power quality on the AC-side, the front-end rectifier is a PWM converter which emulates resistive behavior at its input terminals. To ensure power quality on the DC-side, a series dc active filter is integrated and connected in series between FE terminals and the loads. The series dc active filter here is, as well, called “Series Active Injector (SAI)” due to its main function of actively injecting impedance [11].

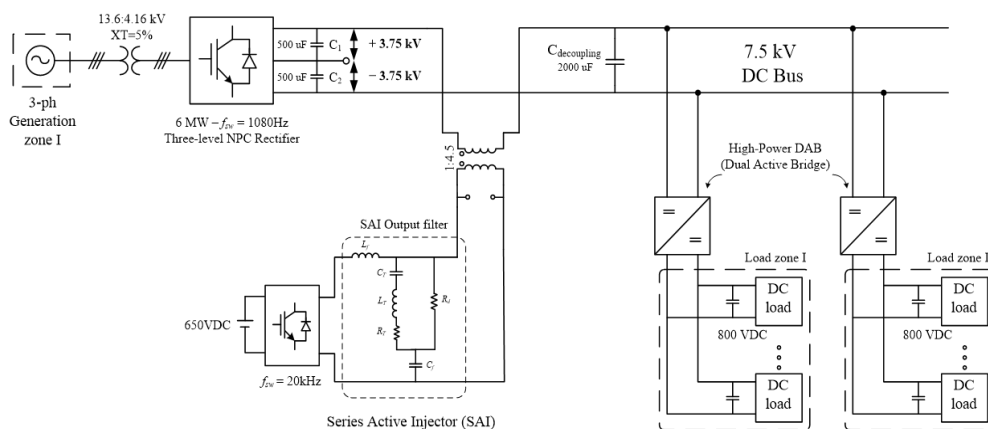


Figure 13 MVDC system incorporating SDAF/series active injector (SAI) [11].

1. Proposed Series DC Active Filter Control Scheme

The controller structure and its associated control block diagrams for the SDAF is provided in [11] and is shown in Figure 14. It consists of three major control loops in order to perform the desired functions. The final goal is to produce a voltage ripple at the output terminals – secondary or DC-side - of SAI's coupling transformer which is as close as possible, in all its signal attributes, to ripple components present at the output of the AFE rectifier but which possess an opposite phase in order to cancel each other out. Achieving this goal, the final DC-bus voltage post SAI will be smooth and free of the disturbances that would otherwise be there due to FE rectifier and active load non-linear interactions. SDAF consists of an H-bridge inverter, output switching ripple filter, and an output transformer which couples it to the MVDC-bus. It is the reference voltage to the PWM modulator of inverter which demands SDAF to produce a specific ripple component at its output. Due to hardware implementation limitations such as limited switching frequency, limited bandwidth, improper switching events, dead-time effect, and so on, not all and every single harmonic component is reproduced as it was intended to. It is the function of the control system to consider all those practical hardware limitations and non-idealities and, in closed-loop feedback control fashion, generate a reference voltage signal to the PWM modulator such that series active injection is made certain up to a specific frequency.

To accomplish the aforementioned goal considering hardware limitations, the following control actions are needed and are implemented:

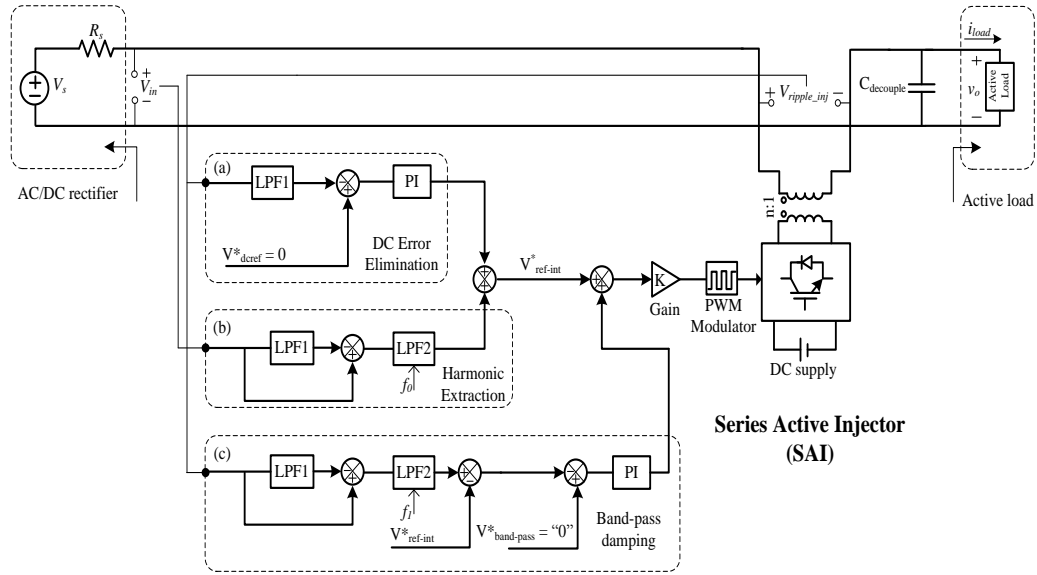


Figure 14 Series active injector – SDAF - controller block diagram [11].

- a) DC Error Elimination
- b) Harmonic Extraction
- c) Band-Pass Damping

During transient loading conditions, SDAF's output transformer can support a transitory DC voltage component which can lead to both DC saturation and error at the output terminals of the MVDC system. DC saturation can force SDAF to shut down; and thus, leave the system prone to disturbances. DC error is never good since it might disrupt the operation of loads that are hanging from DC-bus. As it is shown in block (a) in Figure 14, the injected output voltage ripple is measured and low-pass filtered (LPF) with a cut-off frequency of 1 Hz in order to extract the DC component; then, it is compared against a zero reference

voltage and the error is fed to a PI controller to make sure it is regulated to zero. The cut-off frequency of LPF1-(a) in Figure 14 is set to 1 Hz.

Block (b) in Figure 14 shows the “harmonic extraction unit” in SDAF’s controller structure. This block is considered the most important block in the controller structure since it is responsible for extracting the ripple component out of AFE rectifier’s output voltage and for conditioning it for active filter inverter. This provides SDAF/SAI with the ability to compensate for any oscillations resulting from the non-linear interaction of active loads hanging from the DC-bus and the main AFE rectifier. This is very important since the amplitude of such oscillations might get high enough at high powers to disturb all the other loads hanging from the same bus. The first control loop in harmonic extraction unit with LPF1-(b) cut-off frequency set to 1 Hz, extracts the whole ripple; and then, LPF2-(b) limits it to 1 kHz which is $1/20^{\text{th}}$ of active filter inverter’s 20 kHz switching frequency. The inverter effective bandwidth is 2.2 kHz which is actually $1/9^{\text{th}}$ of the switching frequency. LPF2-(b) cut-off frequency is chosen to be half the bandwidth such that it is made sure that the inverter is able to exactly reproduce those ripple components. This is due to the fact that even within converter bandwidth, because of dead-time effect, probable improper switching events, and other uncertainties, the inverter might not be able to perfectly reproduce its commanded reference voltage.

What remains between the harmonic extraction unit’s band-width and inverter’s bandwidth is to be actively damped such that it will not adversely interact with the rest of the system operation. Block (c) in Figure 14 shows the “band-pass damping” unit which is

responsible for performing that function. After extracting the ripple component from measured output voltage of SDAF through setting LPF1-(c) cut-off to 1 Hz, LPF2-(c) with a cut-off frequency of 2 kHz limits it to the bandwidth of active filter inverter. Frequency components up to 1 kHz are taken out by subtracting $V_{ref-inv}^*$ from extracted measured ripple, and the remaining band-pass signal is forced to zero through a PI controller as it can be seen in Figure 14.

Figure 15 shows different functions of SDAF in the frequency domain. For frequencies up to 1 kHz, SDAF is performing active filtering to cancel the ripples out. For band-pass frequencies between 1 kHz and 2.2 kHz bandwidth of inverter, SDAF is actively damping the ripple frequencies. Finally, frequencies which are above bandwidth of inverter are passively filtered and damped by the special, 4th-order inverter output switching ripple filter which is elaborated in section for series active filter design.

Figure 16 shows the steady-state performance of the SDAF controller. As it can be seen in the last subplot, the injected voltage by SDAF closely follows the ripple voltage produced by the AFE rectifier. Figure 17 shows the transient performance of the SDAF controller in which case a sudden 500 kW active load step-down is applied. As it can be seen, the transiently injected voltage by SDAF accurately follows the transient voltage resulted from step-down load change.

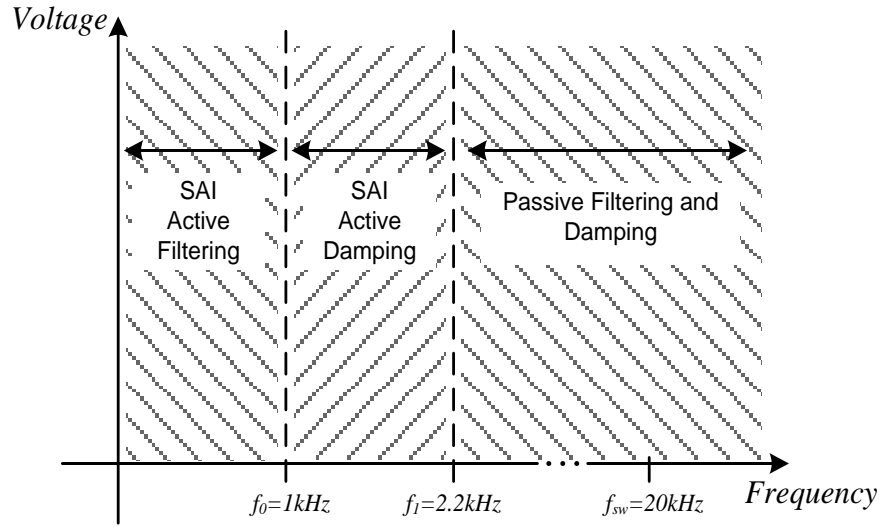


Figure 15 Frequency domain representation of different functions of SDAF [11].

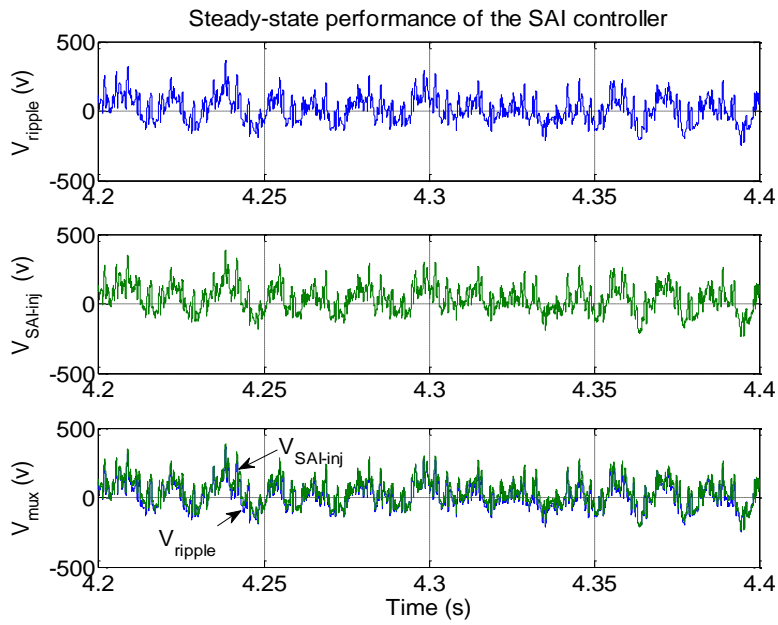


Figure 16 Steady-state performance of SDAF controller [11].

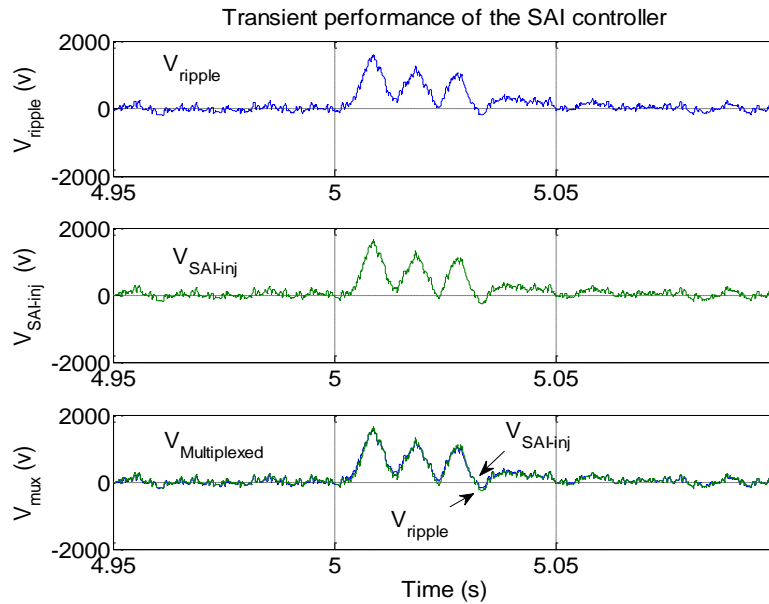


Figure 17 Transient performance of SDAF controller [11].

II. Series DC Active Filter Design

Figure 13 show the SDAF/SAI integrated into the MVDC system. The series active filter design is derived by the worst case voltage ripple and/or disturbance that it should follow. Since SADF is in series with the DC-link any ripple current forcibly passes through the SDAF after being transferred to primary side (AC-side) of the series coupling transformer. It is the slew-rate of this current that determines the critical output inductor of SDAF inverter. Knowing the current slew-rate, the DC-bus voltage value of inverter, and the switching frequency, the value of the inductor is chosen. A series of simulations are carried and the worst-case slew-rate is found to be $3 \text{ A}/\mu\text{s}$. Therefore, the value of the output inductor is chosen to be $200 \mu\text{H}$. The DC-bus voltage of the inverter and the turns-ratio of the

transformer are chosen such that the SDAF is able to follow voltage ripples and disturbances of up to 3 kV. That yields a transformer turns ratio ($N1:N2$) of 1:4.5 and an inverter DC-bus voltage of 650 V. The coupling transformer is designed to possess enough air-gap such it can normally operate under rated DC current without being driven into saturation. The converter switching frequency is chosen to be 20 kHz. This gives a maximum bandwidth (BW) of 2.2 kHz which is slightly less than $1/9^{\text{th}}$ of converter switching frequency [38]. Any harmonics that are produced at frequencies higher than the BW frequency experience phase and amplitude errors; and consequently, not only can it not effectively contribute to the disturbance rejection but it might even exacerbate it. Since the converter actively interacts with the front-side AC-to-DC rectifier and load side DC-to-DC converters hanging from the MVDC-bus, if proper corrective measure is not taken, the PWM switching harmonics may resonate with the rest of the system; and thus, instead of smoothing out disturbances and ripples, exacerbating them to further destabilize the system. The special 4^{th} -order output filter designed for the SDAF inverter has two major functions: to highly attenuate (> 30 dB) switching ripples resulting from PWM and to attenuate and dampen harmonic frequencies that exit between the regulator bandwidth of the inverter and its switching frequency. Figure 13 shows SDAF output filter topology and Figure 18 shows the magnitude and phase frequency response of the designed filter. Table 1 summarizes parameters of the designed SDAF filter.

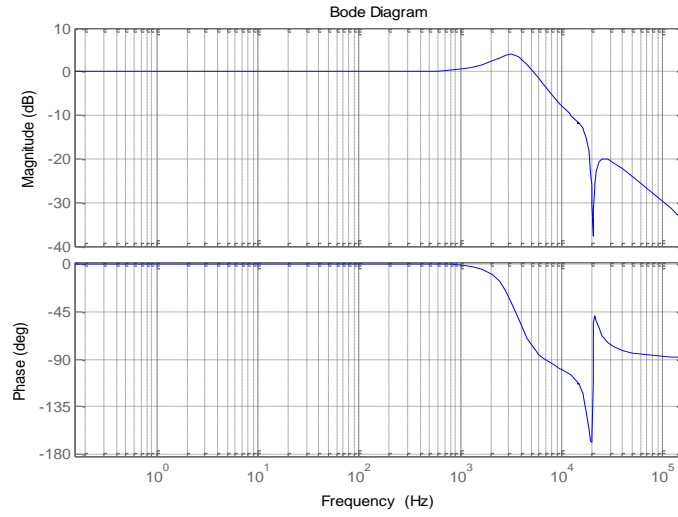


Figure 18 SDAF output filter magnitude and phase frequency response [11].

Table 1 SDAF parameters

Inverter	Rated power (kVA)	20
	DC-bus (V)	650
	Switching Freq (kHz)	20
Transformer	Turns ratio (N2/N1)	4.5
	Primary leakage inductance (uH)	0.3
	Secondary leakage inductance (uH)	10
Output filter	Lf (uH)	200
	Cf (uF)	10
	LT (uH)	128
	CT (nF)	500
	Rd (ohm)	4

III. AFE-based MVDC System Simulation Results with SDAF

A MVDC system similar to the one in Figure 13 is being designed and simulated in MATLAB/Simulink. From the main DC-bus, a number of high power DC-to-DC converters hang on that are rated in the range of 150 kW to 1 MW. The AC-to-DC rectifier and each DC-to-DC converter utilize 1080 Hz and 2 kHz switching frequencies, respectively. The output capacitors of the AFE rectifier are kept to the minimum possible value of 500 μF /ea. To investigate the interaction of active loads with the AFE, a medium-voltage system with 7.5 kV DC-bus is being considered. A total of 3 MWs of dual active bridge (DAB) DC-to-DC converter loads are being connected to the DC-bus. The system is initially running at 3 MWs of active load when at $t = 5\text{s}$ a 500-kW step decrease in load output power occurs. At $t = 6.8\text{s}$, the output power is restored to its original 3 MW value in a stepwise manner. For the SDAF to work, it is necessary to put a decoupling capacitor between the series active injector and the active loads. Therefore, a 2000 μF decoupling capacitor is applied between SAI and active loads. Figure 19 ~ Figure 21 show the simulation results for the 7.5 kV MVDC-bus system. As it can be seen, as a result of the load and source interaction, two types of disturbances, namely steady-state and transient, are induced on the DC-bus. The steady-state disturbances are formed as a result of load and source interaction, and the transient disturbances are formed as a result of step load changes in the system. Figure 19 shows the DC-bus voltage with and without the SDAF acting upon those disturbances to smooth them out. As it can be seen in Figure 19b, the DC-bus has become much smoother with regard to the Figure 19a.

In Figure 20, the 500-kW load step-down transient condition of MVDC system is zoomed out with and without SDAF in operation. As it can be seen from Figure 20a, the MVDC-bus undergoes a 1.7 kV (~ 22%) voltage overshoot without SDAF, whereas the overshoot is reduced to only 150 V (2%) with SDAF operation in Figure 20b.

In Figure 21, the 500-kW load step-up transient condition of MVDC system is zoomed out with and without SDAF in operation. As it can be seen from Figure 21a, the MVDC-bus undergoes a 2.2 kV (~ 29%) voltage overshoot without SDAF, whereas the undershoot is reduced to only 240 V (3.2%) with SDAF in operation. Also, it can be observed that the steady-state ripple amplitude is reduced to less than 50 V peak-to-peak as compared to the 500 V when SDAF is not in operation. Actually, the active damping function of SDAF is taking care of the transient conditions while the active filtering function is filtering out any steady-state oscillations induced on the DC-link.

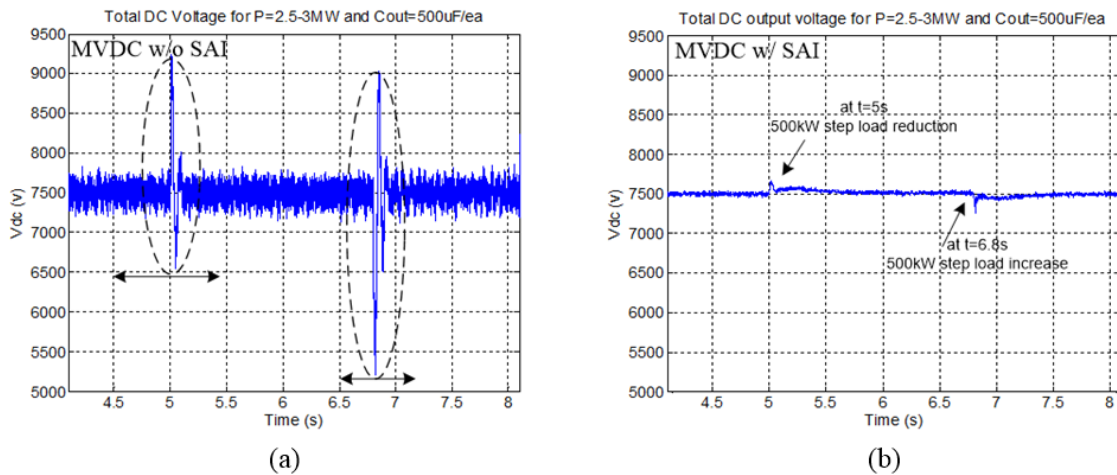


Figure 19 MVDC bus voltage response to 500-kW step load changes without SDAF in operation (a) and with SDAF in operation (b) [11].

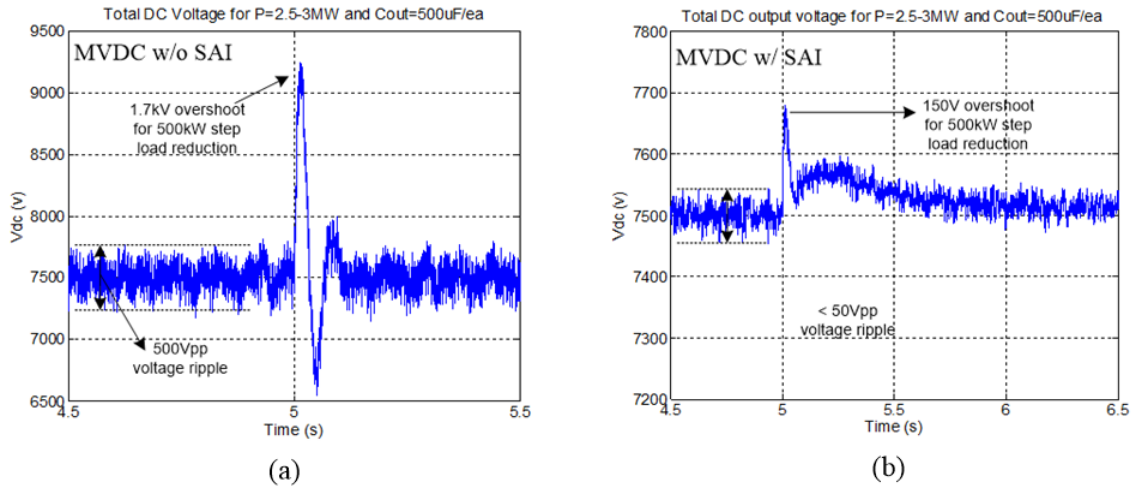


Figure 20 MVDC bus voltage response to 500-kW step-down load change without SDAF in operation (a) and with SDAF in operation (b) [11].

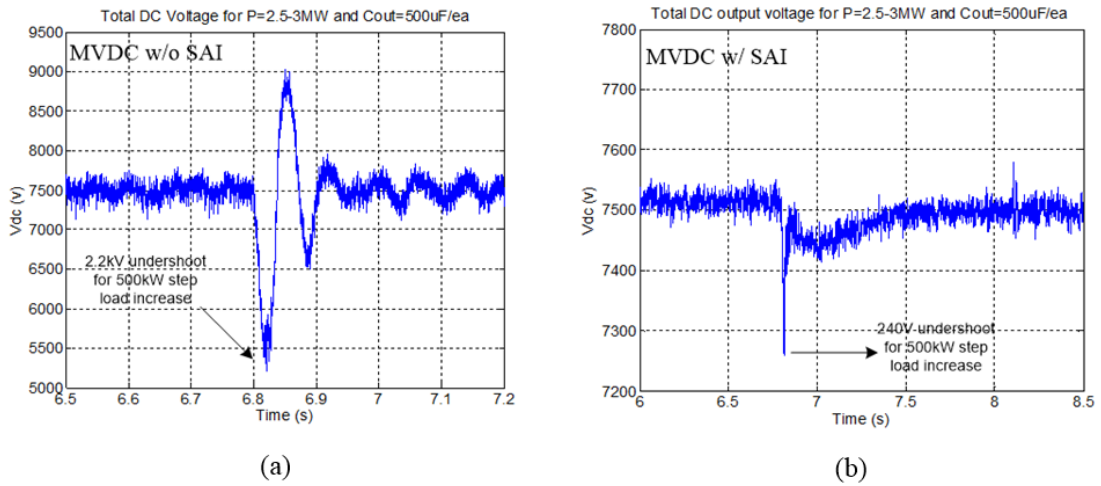


Figure 21 MVDC bus voltage response to 500-kW step-up load change without SDAF in operation (a) and with SDAF in operation (b) [11].

2.4.2 Phase-Controller Rectifier (PCR)-based MVDC System

1. The Proposed Circuit Topology

The proposed MVDC power supply system main circuit is shown in Figure 22 [39]. It consists of four parts: 12-pulse front-end rectifier, passive low-pass LCR filter, transformer-coupled series DC active power filter, and loads. In Figure 22, the 12-pulse thyristor-bridge comprises two 6-pulse PCRs connected in parallel at AC-side and in series at output DC-side. The passive low-pass filter, immediately after thyristor-bridge, partially filters out high frequency ripples well beyond SDAF bandwidth. Then, SDAF can remove nearly all of the undesired ripples left after passive filtering. As it can be seen in the power circuit diagram, SDAF deploys a special fourth-order output filter to eliminate switching frequency ripple and damp out unwanted harmonic frequencies between active filter effective bandwidth and the switching frequency. The primary side (AC-side) of the series dc coupling transformer is connected to active filter output filter and the secondary side (DC-side) is connected in series with the MVDC-bus. The SDAF has the same parameters as given in Table 1.

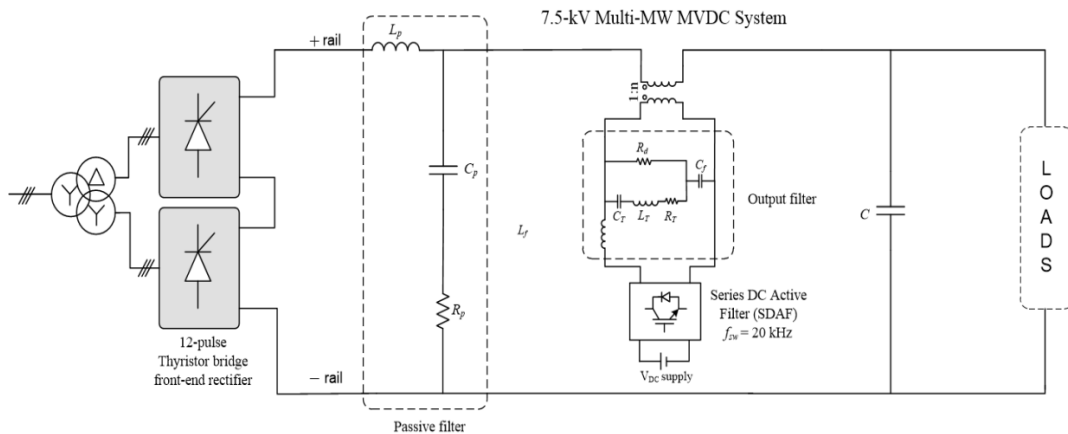


Figure 22 Proposed MVDC power supply integrated with series dc active filter [39].

II. Series DC Coupling Transformer (SDCT)

The series DC coupling transformer (SDCT), as it is shown in Figure 22, is the most crucial element in the system since it couples the DCAPF to the MVDC-bus. The secondary side (DC-side) of the transformer is always in series with positive DC rail and carries full load current at all time. This transformer has two main functions [34]: reactor to DC load current and transformer to DCAPF AC ripple injection. From DC circuit point of view, the transformer acts as a reactor, with its magnetizing inductance referred to the secondary side, in series with DC-link. In this case, enough air-gap should be introduced to the magnetic core such that the reactor does not saturate even under heavy DC load currents. From the AC ripple filtering point of view, the transformer needs large magnetizing inductance to have perfect coupling with positive DC rail such that AC ripple injection is done perfectly by active filter. That, on the other hand, requires the air gap introduced to the core to be small. Therefore, the reactor and transformer function requirements impose contradictory constraints on the value of magnetizing inductance. It should be also noted that the equivalent series reactance of SDCT affects the DC time constants of MVDC system. Since a fast DC dynamic response is desired in MVDC systems, the value of magnetizing inductance should be limited to a value which defines the maximum permissible DC time-constant of the system. From that analysis, the value of magnetizing inductance can be used in designing the transformer. The introduction of air-gap to transformer core increases the DCAPF rating and deteriorates its active filtering performance. Those are demonstrated in Figure 23 which shows the change in DC voltage ripple as per increase in magnetizing current when filter rating is held constant, and in Figure 24 which shows the filter kVA rating versus DC voltage

ripple when magnetizing current is held constant. A more thorough investigation of SDCT parameters impact of SDAF rating follows in the section 2.4.3.

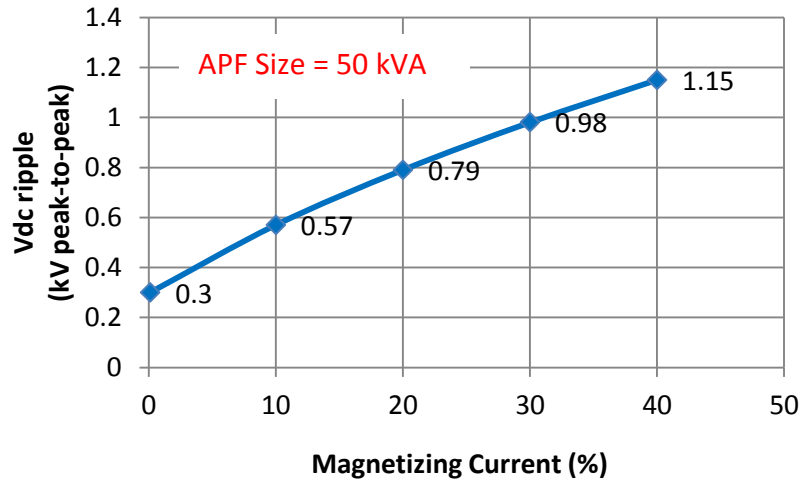


Figure 23 AC magnetizing current vs. DC voltage ripple.

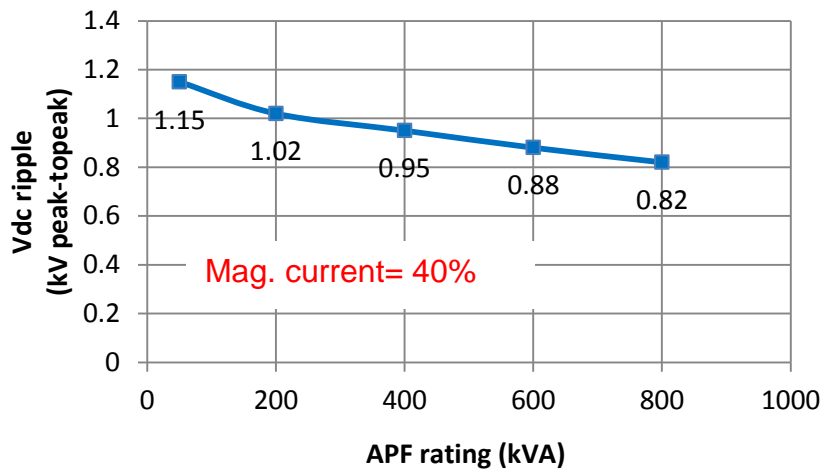


Figure 24 SDAF kVA rating versus DC voltage ripple.

III. PCR-based MVDC Simulation Results with SDAF

The steady-state simulation results of PCR-based MVDC system integrated with SDAF are presented here. The goal is to verify the operation and filtering performance of SDAF assuming the SDCT not to suffer from any DC bias/saturation problem. A system similar to the circuit shown in Figure 22 is designed and simulated in MATLAB/Simulink. The system parameters are given in Table 2. Figure 25 shows the MVDC-bus voltage before and after SDAF operation and Figure 26 shows load current AC ripple component. DC-bus voltage AC ripple harmonic profile analysis is provided in Table 3. As it can be seen, a total AC ripple compensation of 91% is achieved while the 12th harmonic component is compensated more than 98%. Figure 27 shows magnified AC ripple voltage after output of passive filter of PCR together with the injected AC voltage from SDAF. As is can be seen, SDAF injected voltage across DC-bus is almost perfectly tracking the ripple voltage. On the other hand, this means that the injected impedance ratio is really high or k (SDAF controller gain) is very close to one. That is shown in Figure 28.

Table 2 Simulated PCR-based MVDC system parameters

3ph AC voltage	Vs-ln	kVrms	5.25
12-pulse thyristor bridge DC reference	Vdc	kV	7.5
Output passive filter	Lp	mH	15
	Cr	uF	3.44
	Rp	mΩ	66
DC Active Power Filter	N2/N1	-	4.5
	DC bus	V	450
	f _{sw}	kHz	20

Table 2 Continued

DC load (resistive)	P_L	MW	3.75
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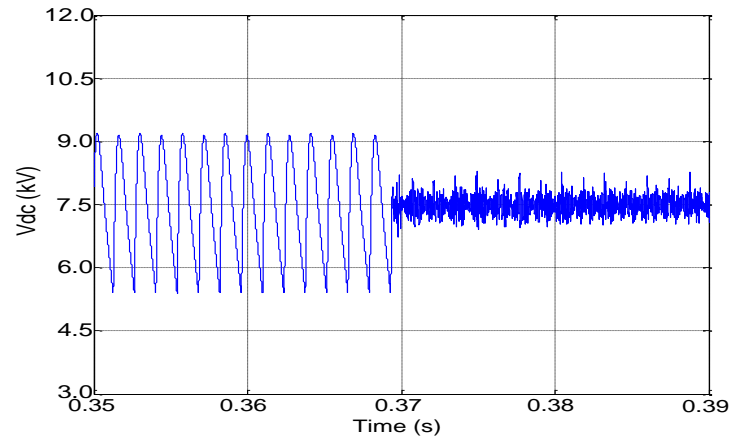


Figure 25 MVDC-bus voltage AC ripple before and after SDAF operation [39].

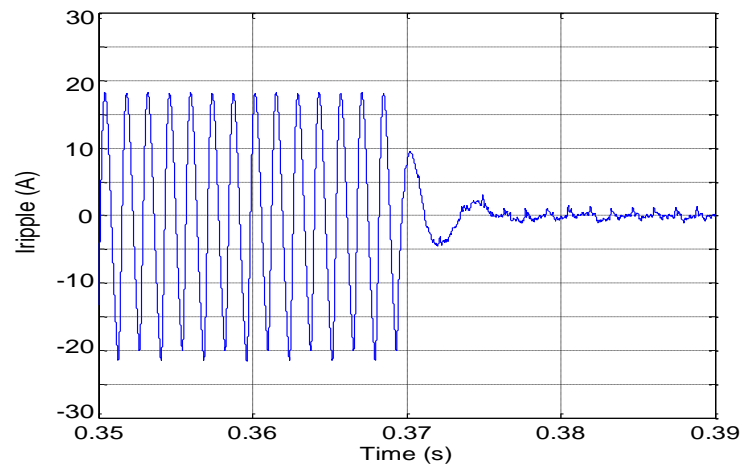


Figure 26 DC load current AC ripple component before and after SDAF operation [39].

Table 3 MVDC voltage ripple harmonic profile w/o and w/ SDAF

APF	Load ripple voltage harmonics spectrum (kV)						RF (%)	CMPF
	DC (kV)	12 th	24 th	36 th	48 th	60 th		
w/o	7.5	1.59	0.51	0.21	0.12	0.07	16	-
w/		0.03	0.04	0.01	0.05	0.04	2.4	91

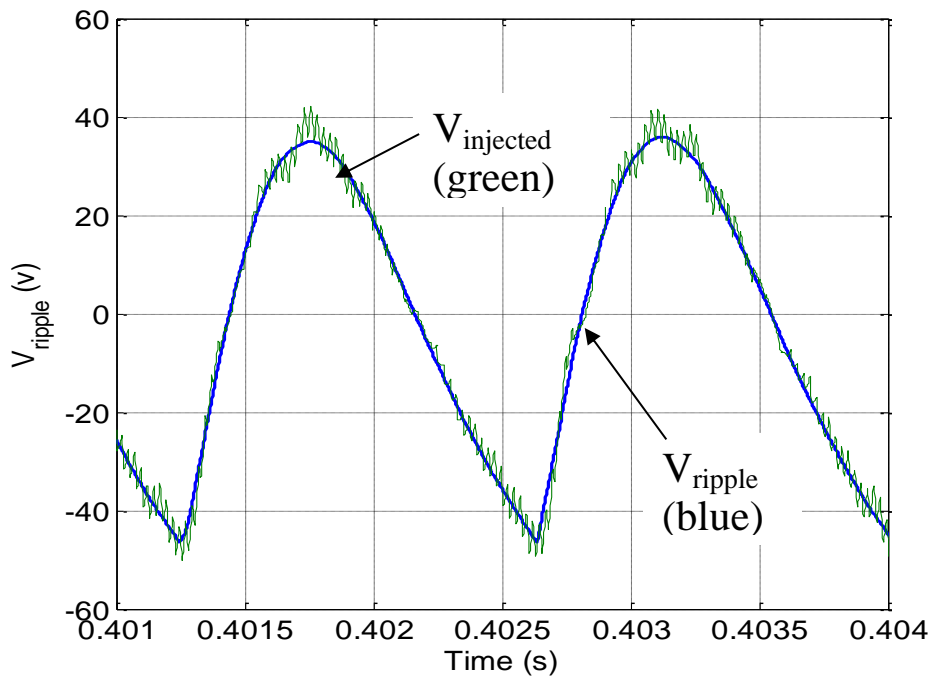


Figure 27 AC voltage ripple after passive filter in PCR-based MVDC system and injected AC ripple by SDAF [39].

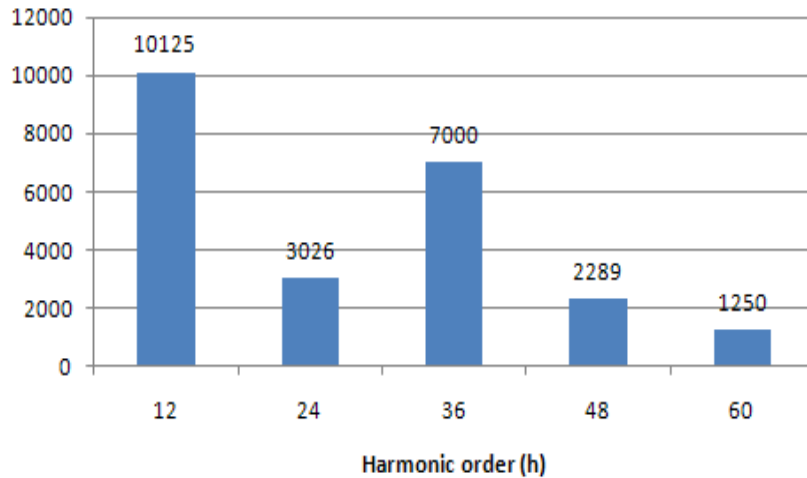


Figure 28 SDAF injected impedance ratio with respect to load impedance at different characteristic harmonic frequencies [39].

2.4.3 Factors Influencing Active Filter Sizing

The study here mainly focuses on some of the important parameters affecting the rating and performance of active filter. These parameters can be internal with respect to series active filter system, i.e. inverter parameters, coupling transformer etc., or external, as in line transformer leakage reactance to front-end rectifier. The parametric search will be done in steady-state mode. The goal is to understand how those set of parameters affect SDAF rating.

1. Series Coupling Transformer

Series coupling transformer is the most crucial element in the system since it couples the dc active filter to the MVDC-bus. As it was aforementioned, the transformer design is challenging since requirements for perfect active filter injection and for high DC saturation tolerance contradict each other. Nevertheless, the transformer design needs to incorporate air gap for it to be able to be put in series with MVDC-bus. The series coupling transformer

internal parameters is shown in Figure 29. The transformer has three main parameters: 1) magnetizing inductance (L_m); 2) winding resistances and reactances (R_1, L_1, R_2, L_2); and 3) winding turns ratio (N_2/N_1).

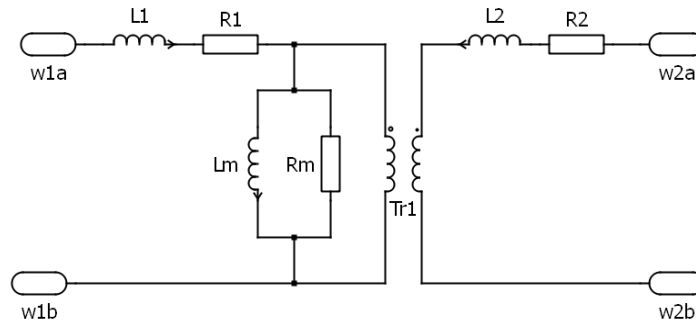


Figure 29 Transformer model considered for steady-state SDAF rating study.

SDAF parameters are as given in Table 1. The transformer parameters are per-unitized according to the following base values:

- $S_{base-trans} = S_{base} = 7.5\text{MVA}$
- $V_{b-pri} = 650\text{ V}$
- $V_{b-sec} = 2925\text{ V}$
- $Z_{1-base} = 0.056\ \Omega \rightarrow L_{b1} = 150\ \mu\text{H}$
- $Z_{2-base} = 1.14\ \Omega \rightarrow L_{b2} = 3\ \text{mH}$

2.4.3.I.2 Effect of Magnetizing Inductance (L_m)

To study the impact of the magnetizing inductance on the rating and performance, the following transformer parameters are assumed to be constant:

- $N_2/N_1 = 4.5$
- $R_1 (2\%) = 0.00112 \Omega$
- $L_1 (2\%) = 3 \mu\text{H}$
- $R_2(2\%) = 0.0228 \Omega$
- $L_2(2\%) = 60.4 \mu\text{H}$

Comparative analysis of impact of different magnetizing inductance values on the series dc active filter rating and performance are presented in Table 4 and Table 5. It can be observed that higher values of inductance reduce the rating of the active filter. In addition, compensation factor (CMPF) and ripple factor (RF) improves with higher inductance as shown. We define these performance factors as (2-1) and (2-2). The results of the analysis are demonstrated in Figure 30 and Figure 31.

$$CMPF (\%) = \frac{\tilde{V}_{dc-thy} - \tilde{V}_{dc-link}}{\tilde{V}_{dc-thy}} * 100 \quad (2-1)$$

$$RF (\%) = \frac{\tilde{V}_{dc-link}}{V_{dc-link}} * 100 \quad (2-2)$$

Table 4 Effect of magnetizing inductance on active filter rating and performance for $L_m = 0.3$ pu, 100% rated load (a), and 10% rated load (b).

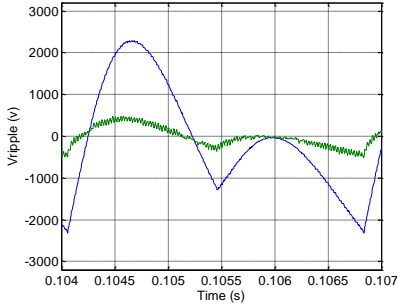
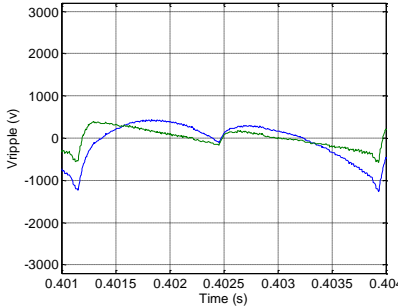
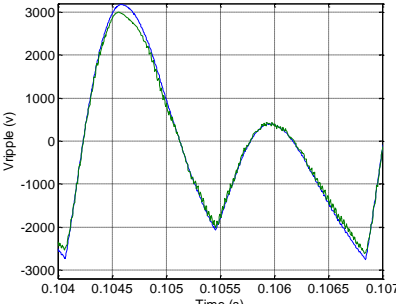
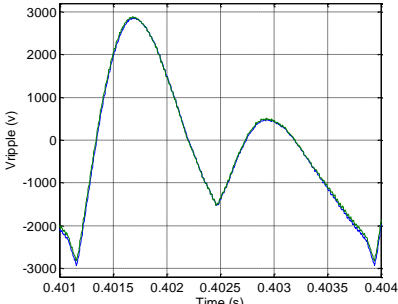
Lm (p.u.)	LOAD (% rated)	APF rating (kVA)	Vripple-pk		Vapf-sec-pk		CMPF (%)	RF (%)
			+	-	+	-		
0.3 (45uH)	10	65	2300	2300	500	500	18	20.5
	100	17	430	1270	400	560	29.5	5.5
			 <p>(a)</p>		 <p>(b)</p>			

Table 5 Effect of magnetizing inductance on active filter rating and performance for $L_m = 30$ pu, 100% rated load (a), and 10% rated load (b).

Lm (p.u.)	LOAD (% rated)	APF rating (kVA)	Vripple-pk		Vapf-sec-pk		CMPF (%)	RF (%)
			+	-	+	-		
30 (4500 uH)	10	25	3150	2750	2950	2650	94	2.1
	100	25	2860	2900	2900	2800	98	0.6
			 <p>(a)</p>		 <p>(b)</p>			

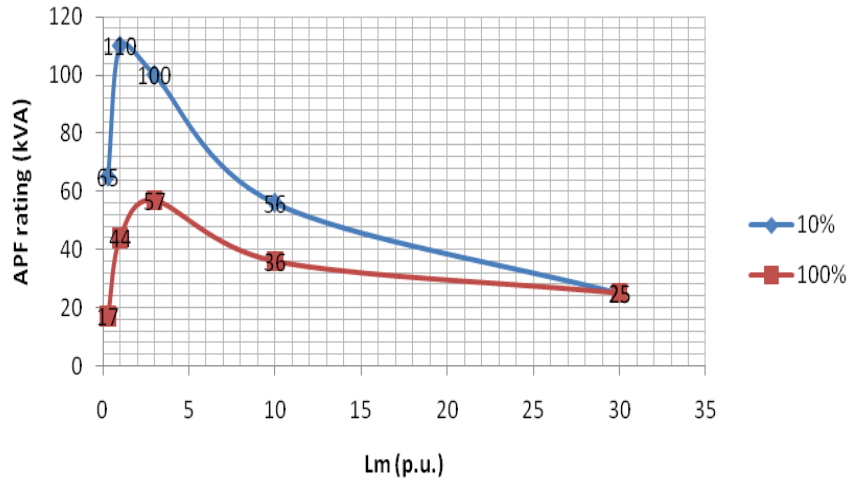


Figure 30 Series dc active filter rating vs. magnetizing inductance for 10% and 100% rated load current.

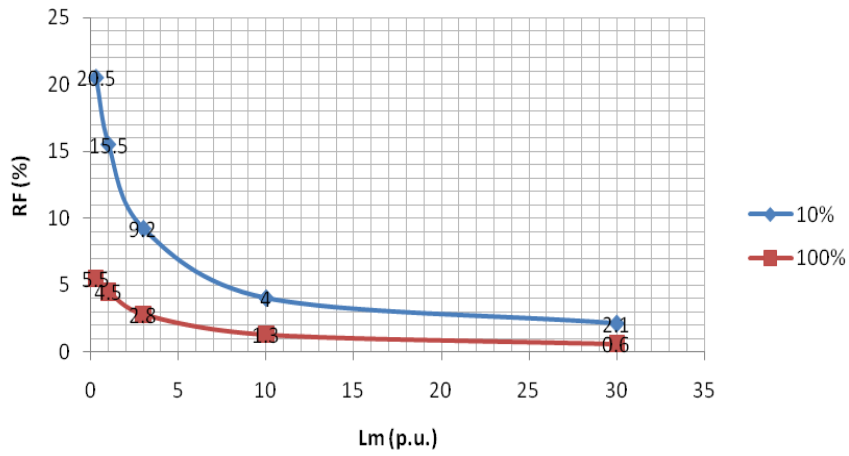


Figure 31 Medium-voltage dc bus ripple factor vs. magnetizing inductance for 10% and 100% rated load current.

2.4.3.I.4 Effect of Winding Resistance and Leakage Inductances ($R1, L1, R2, L2$)

In this study the magnetizing inductance and turns ratio are assumed to be constant at $L_m = 1$ p.u. (150 μ H) and $N_2/N_1 = 4.5$. The effect of leakage resistance and inductance is presented in Table 6. It can be observed that although the active power filter rating has increased, the filtering performance does not change very much.

Table 6 Effect of leakage resistance and inductance on series dc active filter rating

Lm (p.u.)	LOAD (% rated)	APF rating (kVA)	R&L (%)	CMPF (%)	RF (%)
1 (150 μH)	10	110	2	42.5	15.5
			40	38.5	16.3
	100	44	2	64.4	4.5
			40	73.3	4

2.4.3.I.5 Effect of Turns Ratio (N_2/N_1)

In this case L_m is assumed to be constant at 1 p.u. (150 μ H) and the resistance and leakage inductances to be each 2%. The effect of transformer turns ratio on active filter rating and performance is shown in Table 7 for $N_2/N_1 = 4.5$. Table 8 shows the effect of transformer turns ratio on active filter rating and performance when $N_2/N_1 = 10$. Here, it is interesting to observe that with a low magnetizing inductance value, increasing turns ratio greatly improves active filter compensation but does not change the active filter rating. The results of the analysis are demonstrated in Figure 32 and Figure 33.

Table 7 Effect of transformer turns ratio on active filter rating and performance for $N2/N1 = 4.5$, 100% rated load (a), and 10% rated load (b).

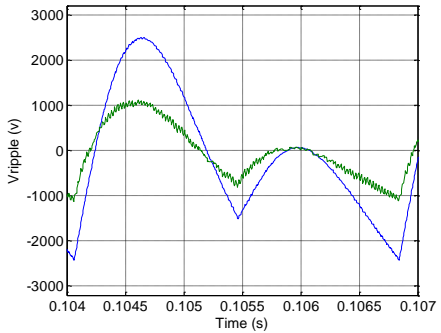
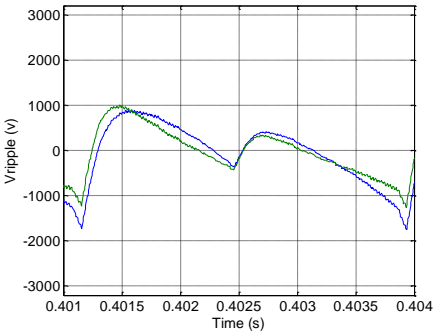
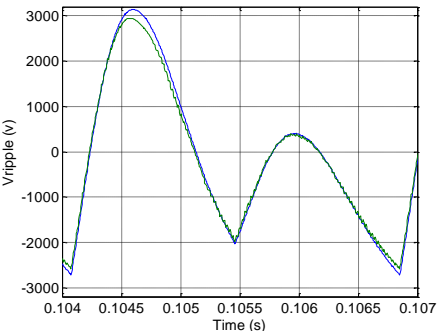
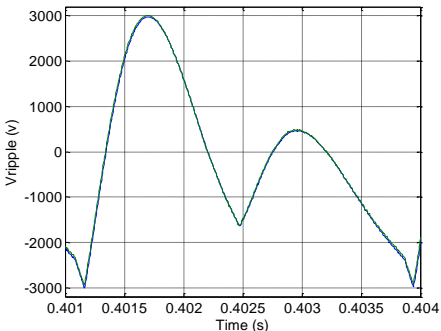
N2/ N1	LOAD (% rated)	APF rating (kVA)	CMPF (%)	RF (%)
4.5	10	110	42.5	15.5
	100	44	64.4	4.5
	 <p>(a)</p>		 <p>(b)</p>	

Table 8 Effect of transformer turns ratio on active filter rating and performance for $N2/N1 = 10$, 100% rated load (a), and 10% rated load (b).

N2/ N1	LOAD (% rated)	APF rating (kVA)	CMPF (%)	RF (%)
10	10	114	93.4	2.2
	100	114	98.7	0.4
	 <p>(a)</p>		 <p>(b)</p>	

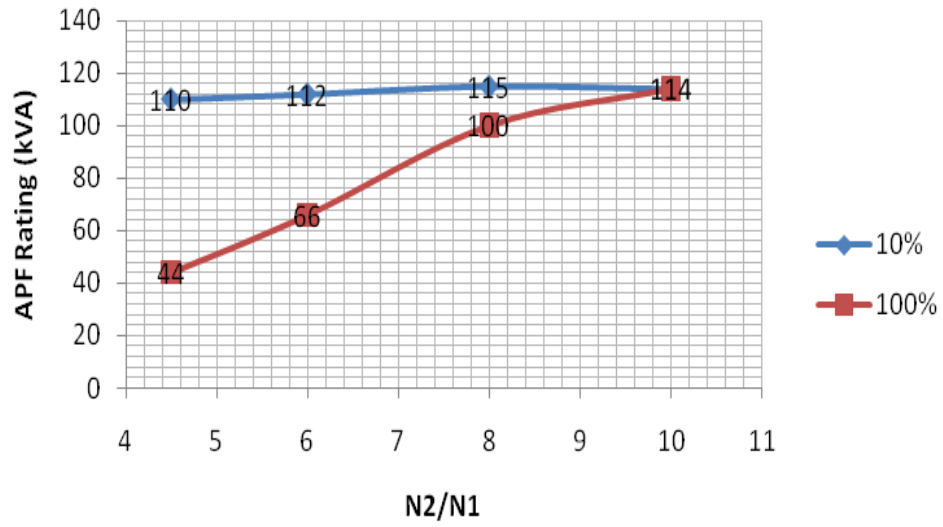


Figure 32 Series dc active filter rating versus turns ratio.

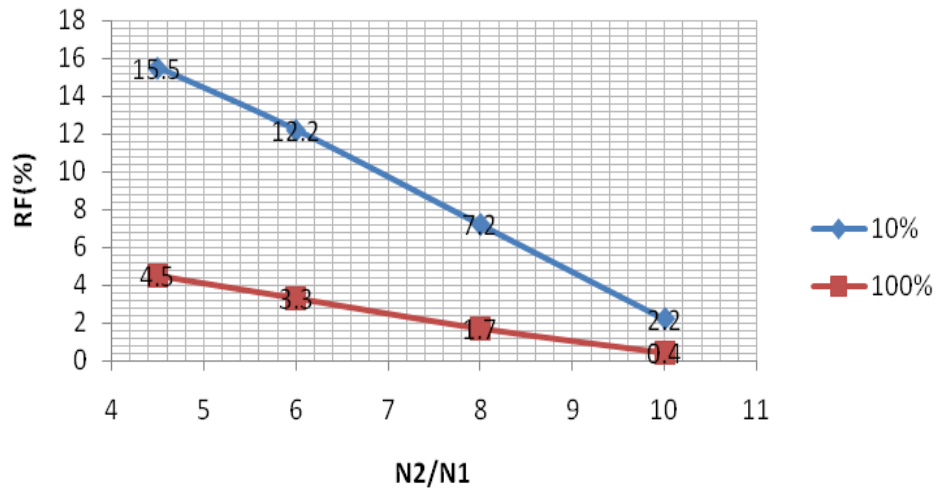


Figure 33 Series dc active filter ripple factor versus turns ratio.

II. Input Line Transformer Leakage Reactance (X_s)

This parametric search is carried out over a 7.5 MVA, 5 kV MVDC system with regard to input line transformer reactance in order to determine the rating of SDAF under worst-case firing angle and different resistive loading conditions. As it is known, the DC-side AC ripple of a thyristor-bridge rectifier is an increasing function of firing angle. For regular system operation, the angle is in the range of 15-25 degrees, not having very drastic DC-side ripple and not demanding very large input reactive power. Moreover, the normal operating angle is chosen as such in order to accommodate for both AC line voltage sags and swells. Since voltage swell disturbance increase the DC-side ripple and demands for more compensation effort by SDAF, a worst-case input phase voltage swell of 30% is considered over the period of simulation. That disturbance requires a firing angle of 45° in order to keep the DC output voltage constant at 5 kV. Having a firing angle of 45° , two extreme cases for the input, AC-side reactance are considered: 1% and 10% of base value. The point here is that the AC-side reactance value changes the slew-rate of AC ripple voltage on the DC-side. The larger the input reactance, the smaller the voltage ripple slew-rate; thus, the smaller the current ripple slew-rate becomes. The smaller the slew-rate, the better the SDAF inverter is able to compensate for the thyristor-bridge output voltage ripple. The system schematic is similar to Figure 22 except that the front-end is a 6-pulse thyristor-bridge. The SDAF parameters are:

- Transformer turns ratio (N_2/N_1) = 6
- DC-link voltage = 700 V
- Switching frequency = 7 kHz

2.4.3.III.1 $X_s = 1\%$ (60 μH)

In this case, the slew-rate is found to be 17 A/ μs which gives a theoretical limit of 41 μH on the output filter inductor of the SDAF inverter. AC-side three-phase power quantities are listed in Table 9; SDAF power rating under two loading conditions are listed in Table 10; and AC ripple harmonic analysis of the MVDC-bus is presented in Table 11. The harmonic spectrum of AC ripple component of MVDC bus is shown in Figure 34.

Table 9 AC-side three-phase power quantities ($X_s = 1\%$)

rated load (5MW)	APF	S_{in} (MVA)	P_{in} (MW)	Q_{in} (MVar)	PF	THD _i %	α_f° - (firing angle)
10%	w/o	0.78	0.55	0.455	0.705	43.35	45.1
	with	0.752	0.5	0.5	0.665	35.41	45.2
100%	w/o	0.776	0.546	0.459	0.704	42.7	45
	with	0.743	0.505	0.497	0.678	31.64	44.7

Table 10 SDAF power rating ($X_s = 1\%$)

rated load (5MW)	S_{rms} ($V_{rms}I_{rms}$) (kVA)	S_{peak} ($V_p I_p$) (kVA)	V_{rms} (V)		V_{peak} (V)		I_{rms} (A)		I_{peak} (A)	
			pri	sec	pri	sec	pri	sec	pri	Sec
10%	68	170	317	1902	630	3780	216	36	790	131.7
100%	142	500	260	1560	395	2370	550	91.7	1720	245.7

Table 11 AC ripple harmonic analysis of MVDC-bus ($X_s = 1\%$)

rated load (5MW)	APF	Harmonics									RF (%)	CMPF (%)
		DC (V)	6 th (%)	12 th (%)	18 th (%)	24 th (%)	30 th (%)	36 th (%)	42 nd (%)	48 th (%)		
10%	w/o	5000	34.92	16.92	11.22	8.39	6.71	5.59	4.79	4.19	31.2	-
	with		12.67	8.66	7.78	7.37	7.12	6.92	6.62	6.04		
100%	w/o		34.88	16.82	11.06	8.19	6.46	5.3	4.46	3.82	30.4	-
	with		8.58	3.69	2.26	1.56	1.16	0.9	0.73	0.61		

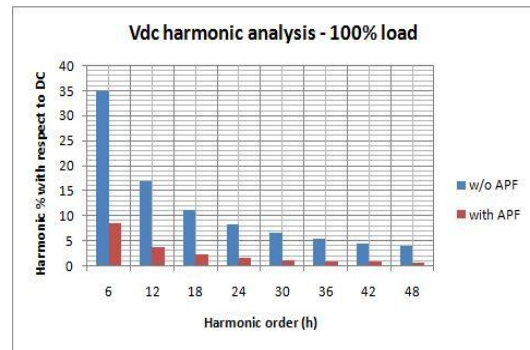
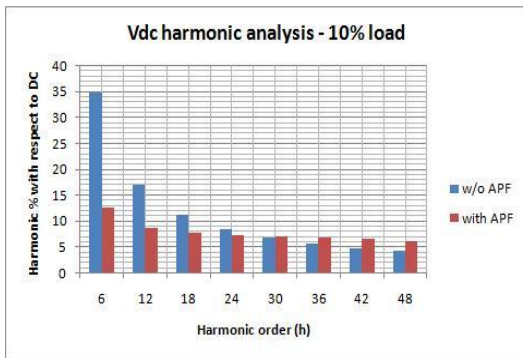


Figure 34 AC ripple harmonic spectrum of MVDC bus ($X_s = 1\%$).

2.4.3.III.2 $X_s = 10\%$ ($600 \mu H$)

In this case, it is found that the slew-rate of the output ripple current, under maximum output loading of 5 MW and maximum AC-side phase voltage swell of 30%, is 2.2 A/ μs . This slew-rate dictates a maximum filter inductor of 300 μH . AC-side three-phase power quantities are listed in Table 12; SDAF power rating under two loading conditions are listed

in Table 13; and AC ripple harmonic analysis of the MVDC-bus is presented in Table 14.

The harmonic spectrum of AC ripple component of MVDC bus is shown in Figure 35.

Table 12 AC-side three-phase power quantities ($X_s = 10\%$)

rated load (5MW)	APF	S_{in} (MVA)	P_{in} (MW)	Q_{in} (MVar)	PF	THD _i %	α_f° - (firing angle)
10%	w/o	0.776	0.545	0.46	0.704	42.71	45
	with	0.744	0.509	0.493	0.684	31.88	44.9
100%	w/o	7.61	5.27	4.82	0.692	36.74	43.5
	with	7.38	5.03	5	0.682	28.71	42.5

Table 13 SDAF power rating ($X_s = 10\%$)

rated load (5MW)	S_{rms} ($V_{rms}I_{rms}$) (kVA)	S_{peak} ($V_p I_p$) (kVA)	V_{rms} (V)		V_{peak} (V)		I_{rms} (A)		I_{peak} (A)	
			Pri	sec	pri	sec	pri	sec	pri	Sec
10%	28	100	213	1278	370	2220	126.5	21	345	57.5
100%	25	120	219	1314	455	2730	111	18.5	280	46.66

Table 14 AC ripple harmonic analysis of MVDC-bus ($X_s = 10\%$)

Rated load (5MW)	APF	Harmonics									RF (%)	CMPF (%)
		DC (V)	6 th (%)	12 th (%)	18 th (%)	24 th (%)	30 th (%)	36 th (%)	42 nd (%)	48 th (%)		
10%	w/o	5000	34.86	16.81	11.06	8.19	6.46	5.3	4.46	3.82	31	-
	with		6.01	4.4	3.26	2.46	1.87	1.43	1.11	0.88	6.75	78.2
100%	w/o		30.29	10.84	5.15	2.76	1.56	0.88	0.48	0.23	30.1	-
	with		1.32	0.54	0.27	0.14	0.06	0.01	0.02	0.04	1.18	96

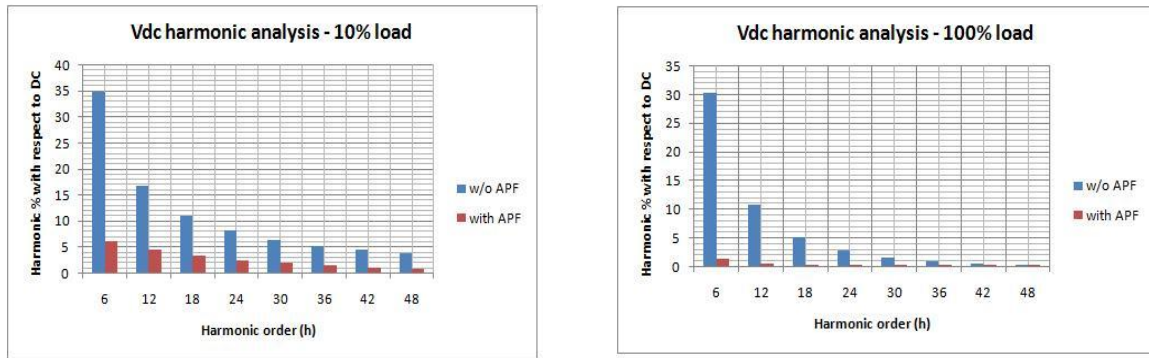


Figure 35 AC ripple harmonic spectrum of MVDC bus ($X_s = 10\%$).

As it can be seen from the results for input reactance (X_s) of 1%, the SDAF rms and repetitive peak power requirements increases considerably while the ripple compensation performance has degraded. In this case, the SDAF is only compensating for 76.6% of ripple when rated power is delivered to load. Furthermore, the low-load performance of the active filter has gotten worse. It has reduced from 78%, in case of 10% input inductance, to only 43% in case of 1% reactance. As the harmonic analysis of the MVDC-bus suggests, under low-load condition, the higher order harmonics are not only compensated but are also boosted when the SDAF is operated in series with the DC-link. As the above results suggest, for the case of 10% input reactance X_s , as the rated power is delivered to the load, the SDAF is able to compensate for as much as 96% of the ripple content with only 120 kVA of repetitive peak apparent power. The compensation of the SDAF degrades to only 78% as the output load power is dropped to 10% of its rated value.

III. Effect of Switching Frequency

In previous section parametric search over two different AC-side line reactances with different output loading conditions was carried out and it was shown that not only with a higher value of input inductance the MVDC-bus voltage ripple slew-rate reduces, but it also reduces as the output load increases. Thus, the larger the input inductance and load current, the smaller the voltage ripple slew-rate becomes and the better the SDAF inverter is able to compensate for the thyristor-bridge output voltage ripple with its limited bandwidth. The current regulator bandwidth of the inverter is approximately one tenth of the switching frequency. Considering the 7 kHz switching frequency of the inverter in the previous section, this will give rise to a current regulator bandwidth of around 720 Hz. That means that the PWM inverter is able to synthesize output voltage harmonics up to this frequency (12th) without introducing any phase or amplitude error. This is very important as it shows how much the SDAF can effectively compensate for the output voltage ripple. Assuming a constant switching frequency, the situation gets worse as the amplitude for higher frequency harmonics of the output ripple increases; and thus, the inverter is not able to compensate for all of them. This will not only affect the effective (rms) ripple compensation, but it will also reflect itself more in terms of peak ripple compensation and peak ripple stress on the SDAF. This suggests that to get a better compensation the switching frequency has to be increased; and hence, the current regulator bandwidth. Therefore, the new frequency is set to 20 kHz giving an effective current regulator bandwidth of 2.16 kHz which enables the SDAF to compensate effectively up to 36th harmonic of the output voltage ripple. Figure 36 and Figure 37 show the result for X_s of 10% when the switching frequency is set to 20 kHz and when

the load is set to 10% and 100% of rated value, respectively. Table 15 presented detailed DC voltage harmonics analysis and Table 16 provides detailed active filter power rating analysis as load is varied.

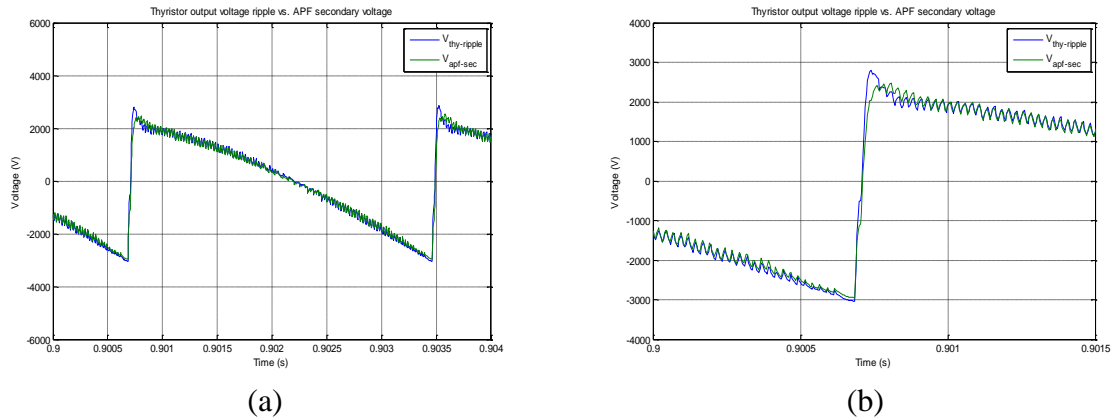


Figure 36 PCR (thyristor-bridge) output voltage ripple (blue) and SDAF injected voltage (green) for $X_s = 10\%$ and 10% rated load when $f_{sw} = 20$ kHz (a) and same quantities zoomed out (b).

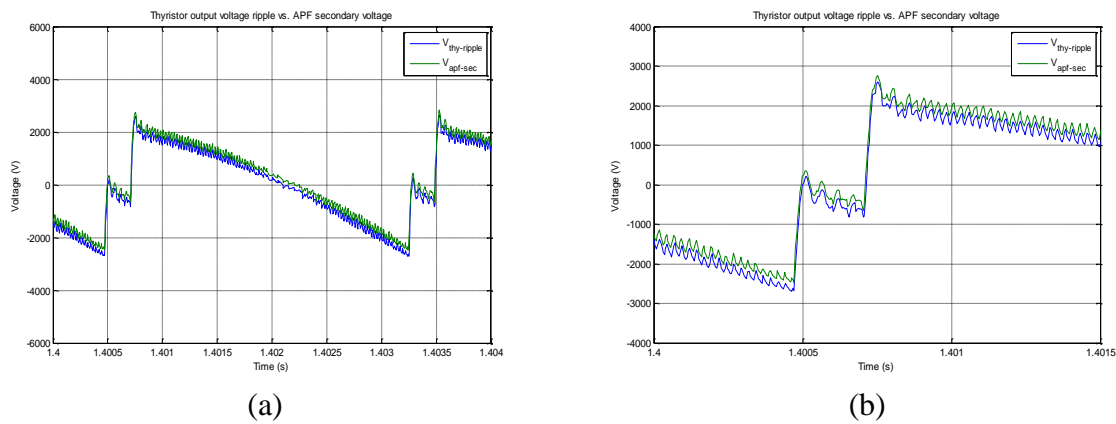


Figure 37 PCR (thyristor-bridge) output voltage ripple (blue) and SDAF injected voltage (green) for $X_s = 10\%$ and 100% rated load when $f_{sw} = 20$ kHz (a) and same quantities zoomed out (b).

Table 15 DC voltage harmonics at $X_s = 10\%$ and $f_{sw} = 20\text{ kHz}$

Load DC voltage harmonic analysis – $X_s=10\%$ and $f_{sw} = 20\text{kHz}$												
rated load (5MW)	APF	Harmonics									RF (%)	CMPF
		DC (V)	6 th (%)	12 th (%)	18 th (%)	24 th (%)	30 th (%)	36 th (%)	42 nd (%)	48 th (%)		
10%	w/o	5000	34.81	16.91	11.24	8.59	6.77	5.72	4.98	4.44	30.5	-
	with		0.57	0.54	0.25	0.88	0.76	0.83	0.87	0.86	2.6	0.915
100%	w/o		31.03	13.57	7.21	3.93	1.47	0.39	1.46	2.3	30.1	-
	with		0.28	0.16	0.02	0.07	0.03	0.02	0.03	0.06	0.37	0.986

Table 16 SDAF rating at $X_s = 10\%$ and $f_{sw} = 20\text{ kHz}$

SDAF power rating with $(N_2/N_1) = 4.5$ transformer ratio & DC-bus = 650V									
rated load (5MW)	$S_{peak} (V_p I_p)$ (kVA)	V_{rms} (V)		V_{peak} (V)		I_{rms} (A)		I_{peak} (A)	
		pri	sec	pri	sec	pri	sec	pri	Sec
10%	48	342	1539	710	3195	12	2.67	67.6	15
100%	40	294	1323	690	3105	17	3.77	57	12.7

IV. Effect of Circuit Topology

In previous sections, except for rating impact analysis of series coupling transformer, only a “pure” series DC active filter topology, as shown in Figure 11, was adopted. The studies carried out above suggest that with the limit in the current regulator bandwidth, due to practical switching frequency limitation, enhanced and desired filtering performance can only be achieved by deploying a “hybrid” series DC active filter approach, as shown in Figure 11, in which the high-frequency content of output ripple is filtered out by a passive filter and only the low-frequency content of output ripple is filtered out by SDAF. This is shown as damped passive filter in topology circuit diagram of Figure 22. A second-order,

damped low-pass LCR filter is used for this purpose. The passive filter will attenuate the high frequency components of ripple, as highlighted in Table 15, such that the overall hybrid active filter system requires less kVA rating to provide the same desired filtering and damping functions. The passive filter parameters for this study are chosen as below:

- $L_f = 2 \text{ mH}$
- $C_f = 30 \text{ uF}$
- $R_f = 16 \text{ } \Omega$ (in series with capacitor)

The passive filter magnitude and phase frequency responses are shown in Figure 38. Thyristor output voltages after output passive filter are shown Figure 38 for 10% and 100% of total load. It shows that the SDAF ripple tracking performance is very good comparatively. In fact, the SDAF compensation varies between 96.5 – 99% for the loading conditions. The peak apparent power rating of the filter in this hybrid approach comes to be only one-fifth (25 kVA) as compared to the previous system. The switching frequency is 20 kHz as before..

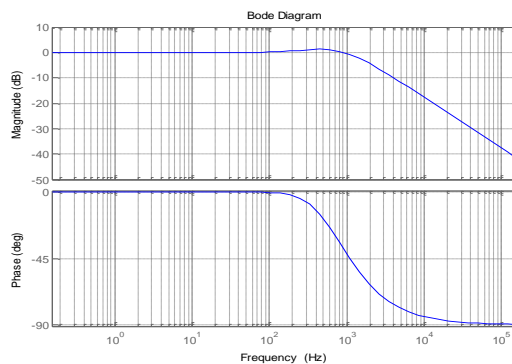
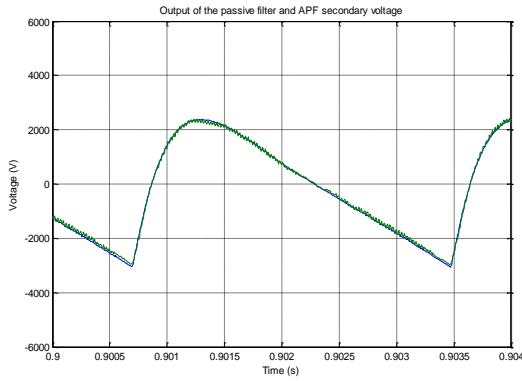
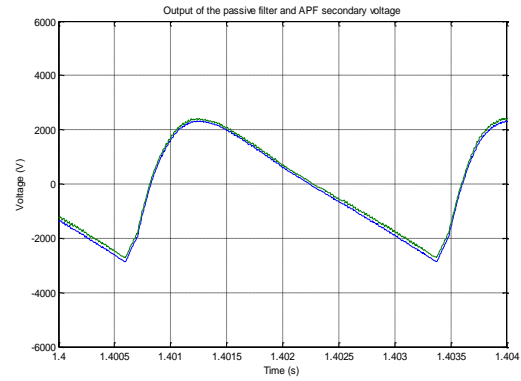


Figure 38 PCR output passive filter magnitude and phase frequency response.



(a)



(b)

Figure 39 PCR output voltage ripple (blue) after passive filter and hybrid SDAF series injected voltage (green) for $X_s = 10\%$ and 10% of load (a) and 100% of load (b).

2.5 MVDC Amplifier System

Florida State University's Center for Advanced Power Systems (FSU-CAPS) has established a unique power-hardware-in-the-loop (PHIL) experimental facility which allows electrical power hardware to be connected to and interact with a virtual power system. At the core of the facility is a real-time computer simulator capable of simulating electrical power systems networks and controls with typically 50s time steps. In addition, CAPS operates a 5 MW rated bidirectional power converter system as a large signal amplifier at AC voltages up to 4.16 kV and DC voltages up to 1 kV. Due to the high switching frequency of the IGBT based converter (effectively 10 kHz) the bandwidth of the amplifier is in the range of around 1 kHz. The primary circuit is fed from the adjacent substation:

- Input circuit voltage: 12.47 kV
- Feed transformer rating: 30 MVA, 5.4% impedance, Primary voltage 115 kV, secondary voltage 12.47 kV.

2.5.1 MVDC Amplifier Requirements

The desired basic requirements for the MVDC amplifier are summarized in Table 17. The unit should be capable to support power flow in both directions. To achieve this functionality at full power we can also consider mechanical reconfiguration of the converter. It is envisioned that the MVDC amplifier will support testing of numerous nouvelle apparatus, both loads and sources, with varied voltage ratings. For this reason we will consider the base rating of 5 MW at 5 kV with a voltage spectrum of 1.5 kV to 20 kV. The converter transformer will have a 12.47 kV primary rating. The transformer secondary may have corresponding taps for each operating voltage window. The proposed system shall provide the best capability of amplifying the waveforms from CAPS Real Time Digital Simulator (RTDS) with conventional converter topologies. Single topology solutions as well as hybrid topologies are solutions. The converter topology and the operating switching frequency of the semiconductor devices in this application as well as the maximum switching frequency considered possible under reduced power requirements (i.e. enhancing fidelity while reducing power).

Table 17 Desired basic requirements for the MVDC Amplifier

Quantity	Value	Unit	Comment
DC output voltage range VDC	1.5...20	kV	Not necessarily throughout the entire range without mechanical reconfiguration

Table 17 Continued

Polarity (voltage)	Positive and negative	-	For both voltage polarities and throughout the entire DC voltage range, two different operating conditions shall be possible: Ungrounded output (“floating”) Grounding one of the two MVDC output terminals in order to obtain plus or minus VDC with respect to ground
Short term voltage excursions	2.0	pu	10
Nominal DC power (bi-directional)	5.0	MW	For VDC = (1.5...20) kV.
Nominal DC current (bi-directional)	1.0	kA	Calculated from the nominal power at VDC = 5 kV. The current can be reduced for VDC > 5 kV.
Maximum overload current	(4...1)	kA	Corresponding to voltages between (5...20) kV for 1 s
Surge current	25	kA	For 10 ms into a bolted fault

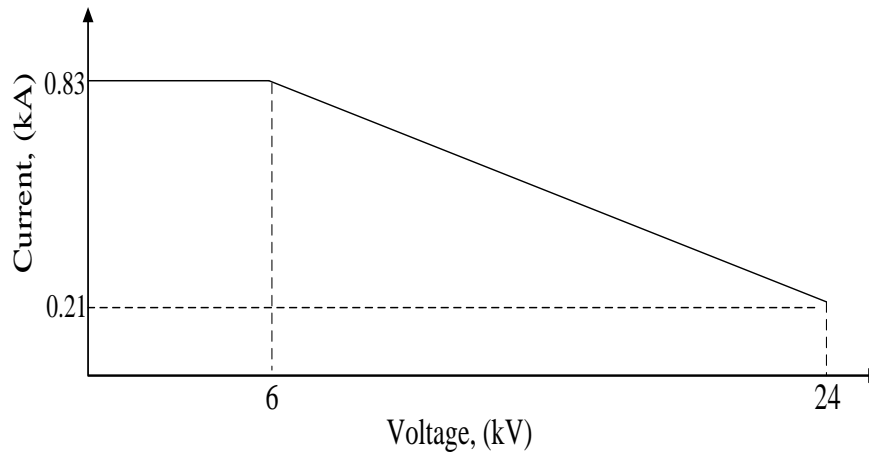


Figure 40 MVDC amplifier continuous current requirements.

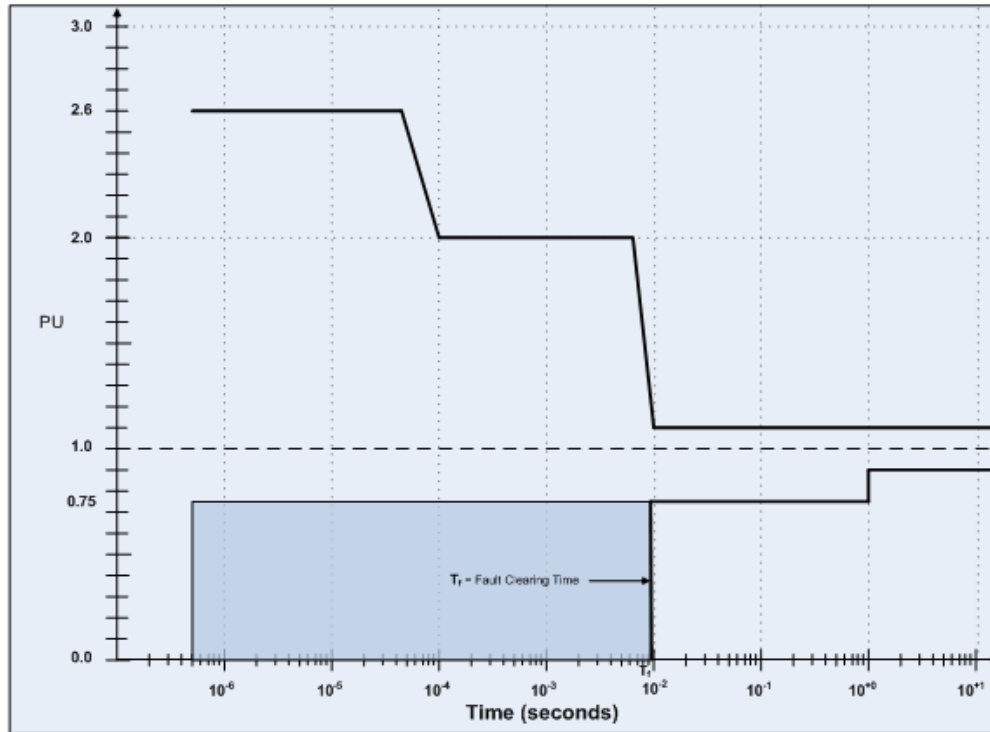


Figure 41 Example of short term voltage excursions on shipboard MVDC application.

2.5.2 Amplifier Operational Concept

The purpose of the MVDC amplifier to produce a voltage waveform with a DC bias as it is provided as a time varying signal reference by the CAPS real time simulator (RTDS). One of the applications for the MVDC converter system is to provide voltage waveforms of “arbitrary” shape to different types of loads. For example, such voltage waveforms may contain a DC bias plus steady state non-sinusoidal voltages or transient voltage excursions (e.g. similar to voltage steps with a higher slew rate). Typically, the RTDS will simulate a MVDC power system with simulation time steps as small as 2s. Therefore, the voltage of interest is generated with a bandwidth of DC to approximately 50 kHz. Consequently, the

ideal amplifier should have a corresponding bandwidth. However, the cost for such a high bandwidth is expected to be prohibitively high considering state-of-the-art power converters in the desired power range of 5 MW. Therefore technical solutions for establishing a power electronic based amplifier system with a bandwidth between DC and at least 3 kHz. Figure 42 illustrates the decomposition of the amplifier output voltage V_{out} into three components. Component 1 includes the undesired, but unavoidable, voltage ripple V_{ripple} , caused by the connection to the 60 Hz grid supply. Component 2 maps the reference voltage signals from the simulator into the desired output voltage. The RTDS can provide analog signals with a bandwidth between DC and approximately 3 kHz. The conventional part of the amplifier output is the DC voltage (V_{DC}), which is defined by V_{REF-DC} and the transfer function TF_{DC} . Additionally to the requested DC reference, the MVDC amplifier system must be capable of providing arbitrary shaped voltage waveforms, which is defined by V_{REF-AC} and the transfer function TF_{AC} . Component 2 illustrates the dependencies of the transfer functions upon the load characteristics. For example, the voltage ripple may be dependent upon the applied load and the actual quantity of the DC reference voltage.

1. Steady-state Performance and bandwidth

All steady-state and dynamic requirements stated below are worst case. The system should at least meet these requirements under all load condition. Table 18 defines the maximal voltage ripple and DC amplification accuracy of the MVDC system, when only a DC voltage is requested and the system operates in steady-state. In addition, Figure 43 shows the required bandwidth of the MVDC system for AC reference signals. For example, a 2 kV reference on top of the DC voltage output should be reproduced up to a frequency of 500 Hz

with a maximum amplitude error of 0.5% (10 V) and phase error of < 5 degrees. AC references at higher frequencies can/will have lower amplitudes as defined in Figure 43.

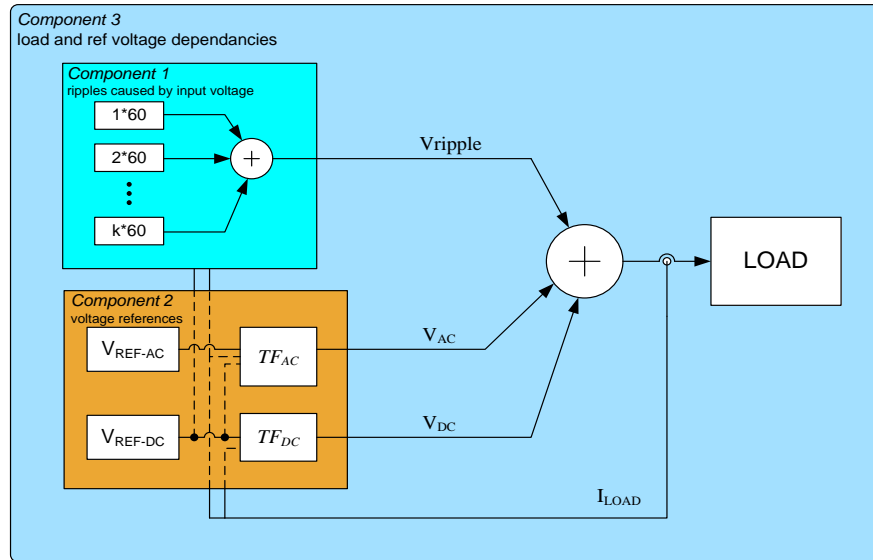


Figure 42 Amplifier output voltage decomposition.

Table 18 DC voltage ripple and error

Total DC voltage ripple $ \text{VRIPPLE-PP} / \text{VDC} *100\%$	1.0	%	Through entire DC output voltage range
Error of DC voltage component $ \text{VDC}- \text{VREFDC} / \text{VREFDC} *100\%$	< 0.5	%	Through entire DC output voltage range

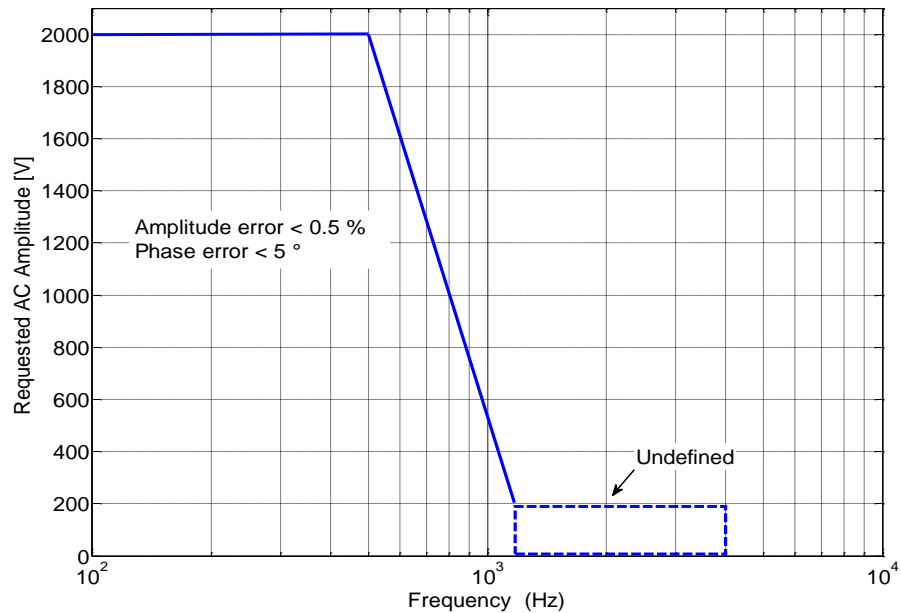


Figure 43 AC output voltage bandwidth specification.

II. Dynamic Performance

For the dynamic performance of the MVDC amplifier, four main parameters are defined: slew rate, rise and fall time, recovery from step load, and dead-time. The rate at which the DC voltage of the amplifier responds to a step change in requested output voltage is called the amplifier slew rate and is given in V/ μ sec (see Figure 44 and Figure 45 for illustration of parameters). The slew rate defines the ability of an amplifier to generate high voltage pulses with sharp rising and falling edges, but is also a bandwidth limiting factor for sine-wave or arbitrary signals. The rise time is the difference between the time when the output signal crosses the lower threshold (3% above pre-step reference) to the time when the signal crosses the upper threshold (3% below post-step reference) and stays within the defined 3 % band (see Figure 44). Correspondingly, the fall time is the difference between the time when the

signal crosses the upper threshold (3% below pre-step reference) to the time when the signal crosses the lower threshold (3% above post-step reference) and stays within the defined 3 % band (see Figure 45). The dead-time (ΔT in Figure 45) is defined as the delay between a commanded step-change and the actual change of the output voltage. The desired dynamic requirements for the MVDC amplifier are summarized in Table 19.

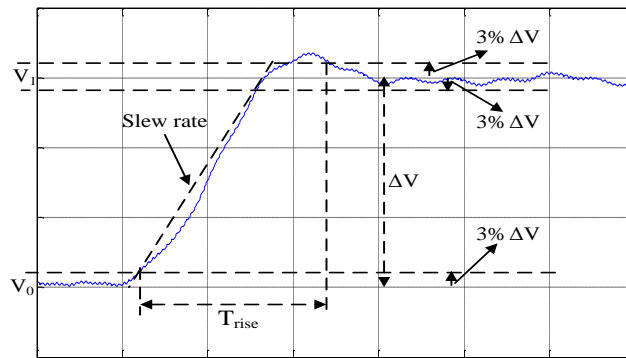


Figure 44 MVDC Amplifier Step-up Dynamic Characteristic.

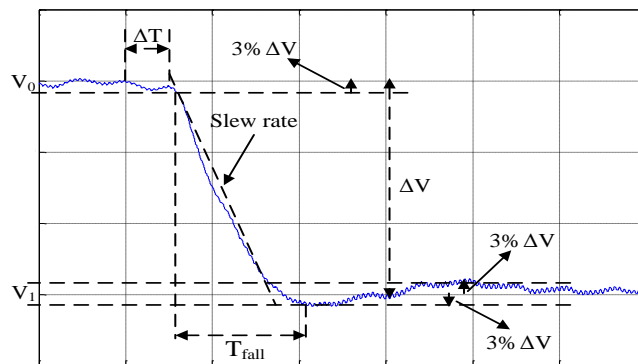


Figure 45 MVDC Amplifier Step-down Dynamic Characteristic.

Table 19 MVDC Amplifier dynamic specifications

Dynamic Specifications			
Rise time and fall time	1.5	msec	Maximum requirement: 0.3 pu step request
Slew rate	4.5	V/ μ sec	Maximum requirement: 0.3 pu step request
Recovery time after step load	2.0	msec	Maximum requirement: 0.4 pu load change request
Voltage excursion after step load	0.15	Pu	Maximum
ΔT dead-time	0.2	ms	

2.5.3 MVDC Amplifier Dynamic Study

I. System Architecture

A twelve-pulse phase-controlled thyristor front-end rectifier with Hybrid-SDAF (Hybrid Series DC Active Filter) makes the integrated MVDC amplifier system. The power stage of the system is shown in Figure 46 and the system control block diagram is shown in Figure 47. This is a case study of hybrid series active filtering solution and its impact on dynamic performance of the system. This is mainly because the hybrid series topology gives a better filtering solution for phase-controlled thyristor bridge rectifier than pure SDAF. In this case, not all the DC-link harmonics should be taken care of by SDAF but a portion of them and the rest are being filtered out by a passive filter which comes immediately after the thyristor-bridge, as shown in Figure 47. The goal of the study is to see how different components in the system affect the dynamic performance of MVDC amplifier and how well they compare with the specification in Table 19. The SDAF filter has a switching frequency of 20 kHz and

an effective bandwidth of 2.2 kHz and thus, the passive filter is basically filtering out frequencies which are higher than the bandwidth of SDAF.

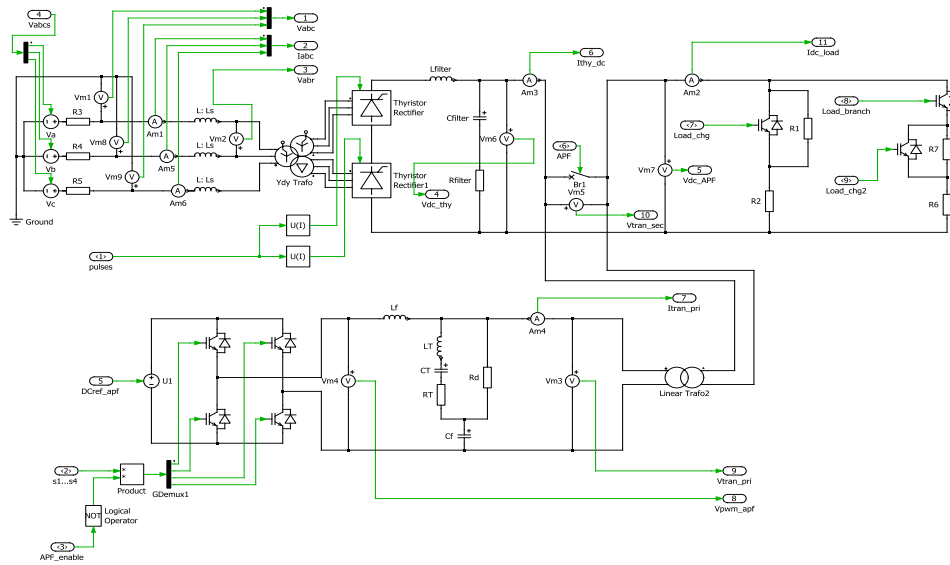


Figure 46 MVDC amplifier system power circuit.

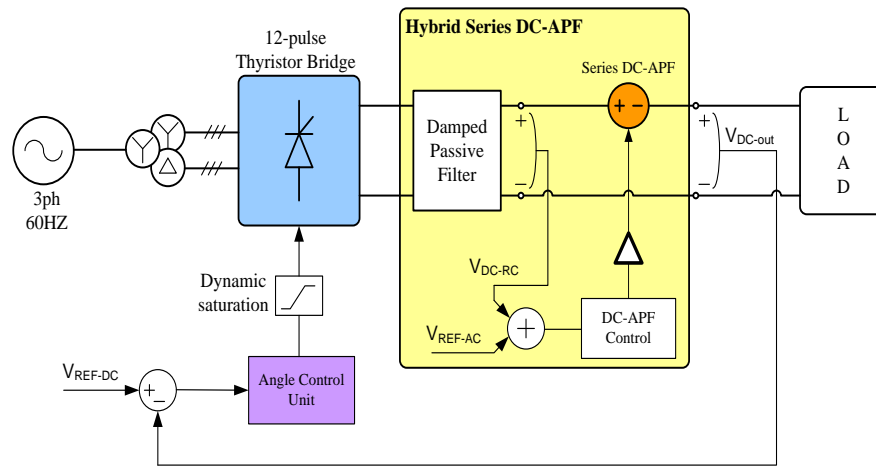


Figure 47 Twelve-pulse front-end MVDC amplifier system block diagram.

II. System Parameters

The dynamic performance of the active filter can be affected by the following system components:

- 1- *Thyristor bridge low-pass filter:* this filter inserts a certain amount of delay between at the output of the thyristor-bridge from the moment the firing angle is applied to the converter. The LPF filter parameters are restricted to certain range of values required by the filtering performance and thyristor bridge predictable behavior. For the thyristor bridge to behave predictably, the load that it sees on the DC-side should be dominantly inductive. This requires a minimum amount of inductance on the dc-side and therefore, the capacitor and damping resistor are chosen accordingly. Due to filtering requirements, the filter resonant frequency can only be varied over a narrow frequency band. In this case, it can vary from 500-1000 Hz.
- 2- *Angle control unit:* angle control PI controller affects the transient and steady-state error but is limited by the voltage-boost or –buck rate limit and dynamic saturation limits which vary according to the commanded reference DC-bus and load current.
- 3- *Voltage-boost or –buck rate limit and quantization:* This is the kind of limitation that is forced by the hardware which is firing the thyristors. The maximum rising and falling edge rate considered for this work is $4^\circ/\text{ms}$ and it's quantized with a sampling frequency of 2.5 kHz.
- 4- *Dynamic saturation:* the dynamic saturation helps to control and hold the voltage excursions within a certain predefined band around the commanded reference. This is actually done by dynamically limiting the angle within a band around the reference

value and it can be done in a symmetric or non-symmetric fashion. For the dynamic saturation to work hand in hand with the rate limit and PI controller there is a need for a good approximation of the actual firing angle. Since we're already forcing the dc-side to be highly inductive, the average dc voltage produced by the thyristor-bridge can be formulated in terms of the firing angle and from there, for a specific DC-link reference voltage we can find the required angle for firing thyristors. The non-accuracy in the angle approximation arises when the dc-link is not highly inductive and second, when the input inductance is rather large. In this case since there is a 10% of X_s at the input ac-side, then there is a certain dc voltage drop of the nominal average dc voltage which should be taken care of in the firing angle calculations:

$$V_{dc} = \left(\frac{3}{\pi}\right) [V_{ll,p} \cos(\alpha_f) - X_s] \cdot I_{dc} - (R_s + 2R_{ON}) \cdot I_{dc} \quad (4-1)$$

Therefore:

$$\alpha_f = \left(\frac{\pi}{3}\right) \frac{\cos^{-1} \left(V_{dc} + \frac{3}{\pi} X_s I_{dc} + (R_s + 2R_{ON}) I_{dc} \right)}{V_{ll,p}} \quad (4-2)$$

where in the above formula R_s is the resistance of input inductance and R_{ON} is the resistance of a thyristor when it's ON. The angle obtained in this way has shown to lead to better steady-state response of the system.

- 5- *System controllers*: these consist of two major components. The first one is the ac-ripple extraction for the SDAF and the second one is the dc extraction for the PI angle control unit. These two contribute mostly to the transient performance of the system

having set all the aforementioned parameters properly. Furthermore, it is seen that setting the cut-off frequency of the LPF associated with the dc extraction unit of PI angle controller of the thyristor-bridge to a value which is preferably not above the minimum harmonic frequency of the dc-link (in this case 360 Hz but it may be some other value depending on the specific system of converters designed), the bandwidth of the ac-ripple extraction unit of the SDAF dominates the rise-time and fall-time transient performance of the whole system. The bandwidth of the ac-ripple extraction unit is actually how fast the SDAF is able to smooth the dc-link assuming a certain rate-limited increase or decrease in firing angle. An important point to note here is that having a relatively high rate of change of angle, the bottleneck of the system transient behavior turns out to be caused by the active filter ac-reference extraction unit than any other component in the system. Other components in the system contribute more to delay (dead-time) than significantly affecting the rise-time or fall-time of the system.

All the aforementioned parameters are summarized in Table 20. According to the simulation plan, the system first is given a reference voltage of 3500 V and is delivering a power of 245 kW then at $t = 0.4\text{s}$ the reference voltage is risen to 5000 V (0.3pu increase) with the system delivering a power of 500 kW. At $t = 0.7\text{s}$ the output power demanded by the load is increased to 2.5 MW which is a 0.4 pu increase in power. At $t = 1\text{s}$ the reference voltage is again dropped to 3500 V which is equal to 0.3 pu decrease.

Table 20 MVDC amplifier system parameter set for dynamic performance study

Thyristor bridge passive filter	Resonant frequency (Hz):		800
	Bandwidth (kHz):		2
	L (mH)		4
	C (uF)		10
	R (Ω)		40
Angle control unit	PI controller	Kp	0.02
		Ki	0.75
	Rate limiter	Rise (deg/sec)	4000
		Fall (deg/sec)	-4000
	Dynamic saturation	Upper (%)	4
		Lower (%)	6
Quantization	ZOH with sampling frequency of 2.5 kHz		
System controllers	Thyristor bridge DC extraction BW (Hz)		100
	APF ac-ripple extraction BW (Hz)		80
			240

III. Simulation Results

The simulation results are shown for the two case of APF ac-ripple extraction bandwidth of 80 Hz and 240 Hz. Figure 48 shows the angle control unit performance when angle change rate is limited to $\pm 4^\circ$ deg/ms, quantization sampling frequency is 2.5 kHz, and SDAF AC-ripple extraction BW is 80Hz. The angle rate limit and quantization model set practical limits in the way these quantities would change. Figure 49 shows the reference voltage that is asked from the MVDC amplifier to produce and the actual output of the system. Also showed is the step-up and step-down dynamic performance of the MVDC-SDAF integrated system. It is seen from the simulation results that having set a proper value for the angle rising and falling rate limits and upper and lower bands of dynamic saturation, the limiting factor in reaching a desired rise/fall-time is the bandwidth of the ac-ripple extraction unit of SDAF.

With a bandwidth of 80Hz the rise/fall-time is almost 20ms but with a bandwidth of 240 Hz the rise/fall-time both are almost 10ms which is half the previous value. On the hand, we cannot afford to arbitrarily increase the bandwidth of this module since it will adversely affect the main job of SDAF which is canceling the ripples and disturbances rather than passing them through. This bandwidth is theoretically limited by the first dominant harmonics frequency of the dc-link ripple which in this case is 360 Hz. The higher the bandwidth of ac-ripple extraction unit, the higher ripple amplitude of the MVDC-link becomes even with the SDAF in operation. Table 21 compares obtained dynamics with the desired one.

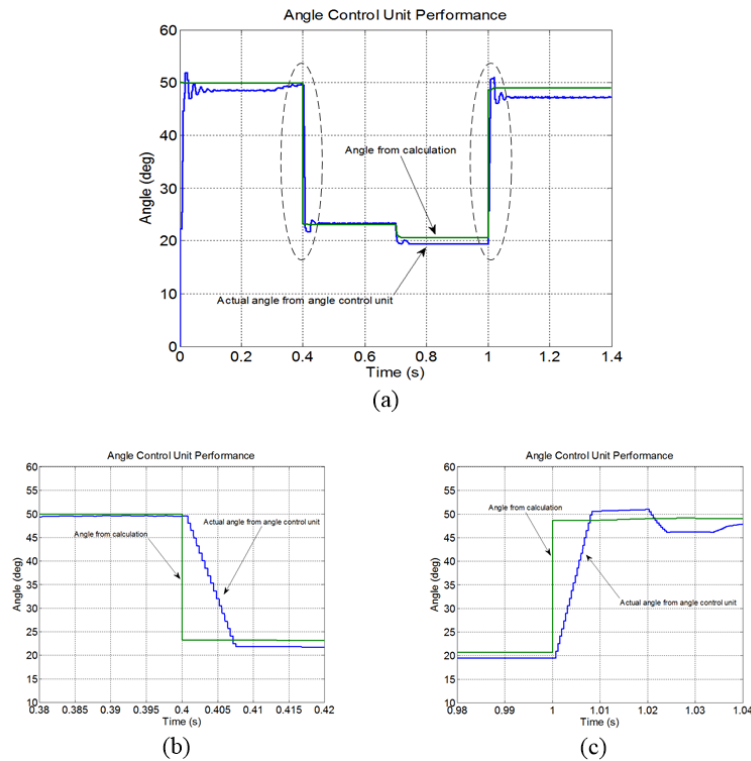
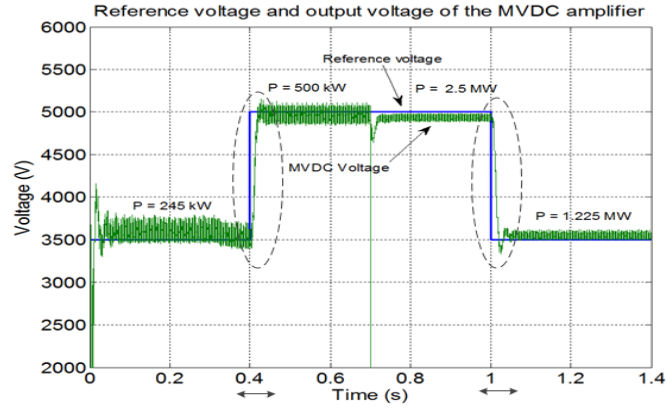
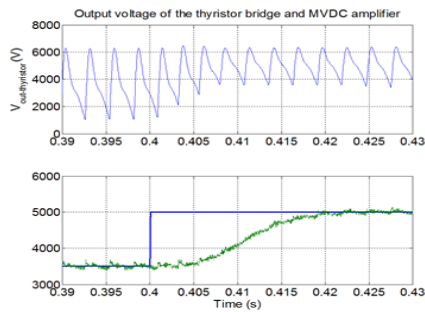


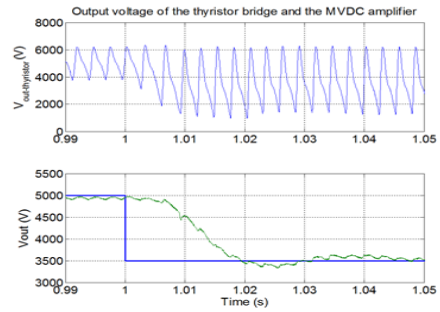
Figure 48 Angle control unit performance for SDAF AC-ripple extraction bandwidth of 80 Hz.



(a)

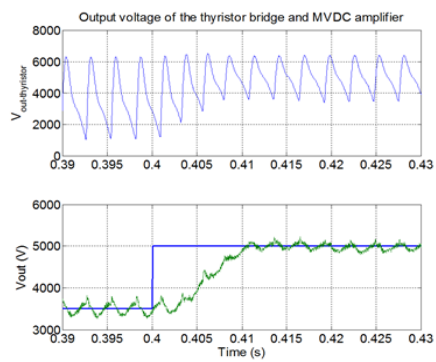


(b)

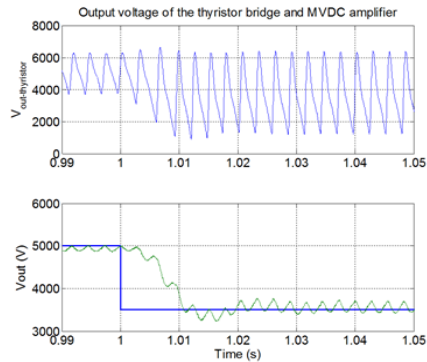


(c)

Figure 49 Reference voltage versus the output voltage of MVDC amplifier for SDAF AC-ripple extraction bandwidth of 80 Hz.



(a)



(b)

Figure 50 Output voltage of MVDC amplifier for SDAF AC-ripple extraction bandwidth of 240 Hz.

Table 21 Comparison of MVDC amplifier system dynamic performance studies

		ideal	80 Hz*	240 Hz	
Rise time and fall time	msec	1.5	16	8	Maximum requirement: 0.3 pu step request
Slew rate	V/ μ sec	4.5	0.093	0.186	Maximum requirement: 0.3 pu step request
Recovery time after step load	msec	2.0	13	8.5	Maximum requirement: 0.4 pu load change request
Voltage excursion after step load	Pu	0.15	0.32	0.32	Maximum
ΔT dead-time	msec	0.2	4	2	

*This is the bandwidth of the ac-ripple extraction unit of SDAF.

2.6 Design Issues in a MVDC Amplifier with a Multi-Pulse Thyristor Bridge Front-End

As it was mentioned in dynamic performance requirements, a high power medium-voltage dc amplifier system must have adequate bandwidth to reproduce the reference signal [41]. Active front-ends based on IGBT semiconductor technologies have limited converter bandwidth due to limited switching frequency at high power and are not suited for the application. There is also a concern that in using IGBTs, the allowable short circuit current may not be high enough for a robust system that has a significant or long duration short circuits on the load. In contrast, phase-controlled front-end rectifiers such as multi-pulse thyristor-bridges commutated at 50/60 Hz ac line frequency offer a viable solution to the operational requirements of MVDC amplifier system. They are based on mature and robust

thyristor technology, which allows for a higher symmetrical short circuit current up to around 50kA peak. Figure 51 shows the MVDC amplifier power circuit diagram comprising a multi-pulse thyristor bridge front-end and a series dc active filter. Figure 22 shows the proposed 12-pulse system for the design study.

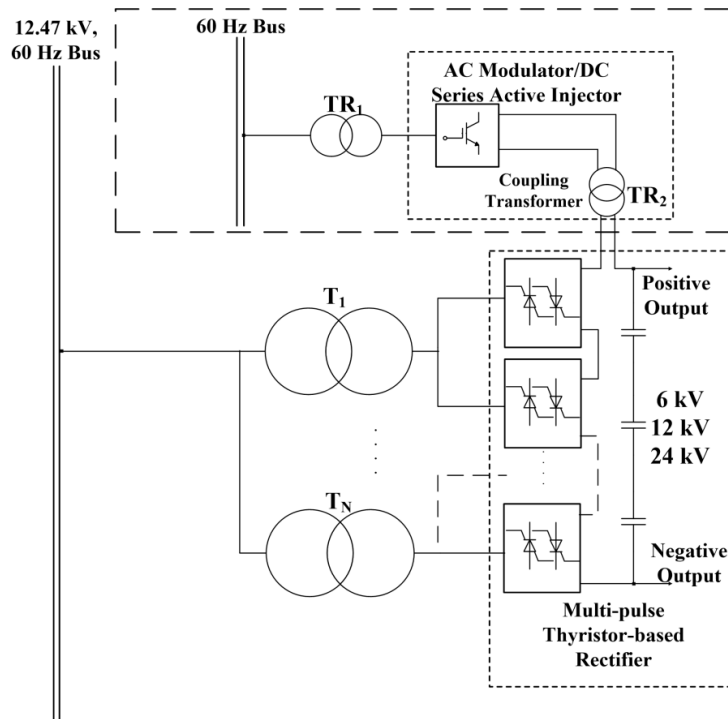


Figure 51 MVDC amplifier circuit diagram with multi-pulse circuit topology [40].

To meet the system dynamic requirements, the thyristor bridge response time is considered critical. The output dc voltage response time of a multi-pulse thyristor rectifier is determined by the firing pulse generator dynamics, and therefore it should be carefully examined for the MVDC amplifier system. In this regard, a general purpose 12-pulse firing

(gate delay) pulse generator board is characterized based on the thyristor firing circuit theory [42]. Following are the important observations from characterizing the firing board [43]:

2.6.1 Firing Angle Change Dynamic

It is necessary to determine this dynamic as it directly influences the MVDC amplifier dynamics. This is the transfer function from reference firing angle delay to the actual angle delay applied to all thyristors. Figure 52 shows the block diagram of the angle delay transfer function in which $\tau_1.. \tau_4$ are 2400 μ s, 1200 μ s, 23.9 μ s, 232 μ s respectively, and k_0 is 313s⁻¹. The transfer function $T_\alpha(s)$ step response and bode diagram are shown in Figure 53 and Figure 54. As it can be seen, the transfer function is approximately an over-damped 2nd-order system with 10% to 90% rise time of 4.09ms, 98% settling time of 8.58ms, and final value reach time of 14ms. The -3dB bandwidth is 562 rad/sec. This is the fastest dynamic the firing board can reach since decreasing the response time further would shorten the mandatory 15-20 μ s pulse width in thyristor gating pulse train more than the limit required for reliable firing of individual thyristors. Referring to Table 19, the firing angle change dynamic falls short of the desired dynamic spec of the amplifier.

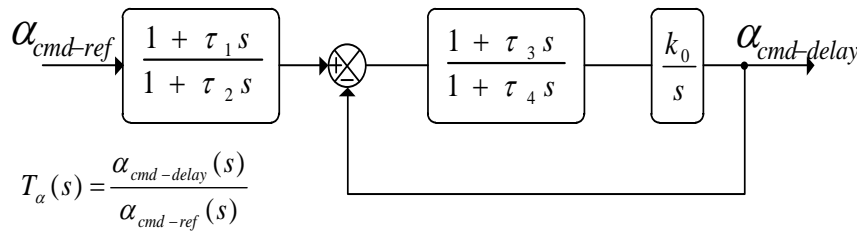


Figure 52 Block diagram of the firing angle controller transfer function.

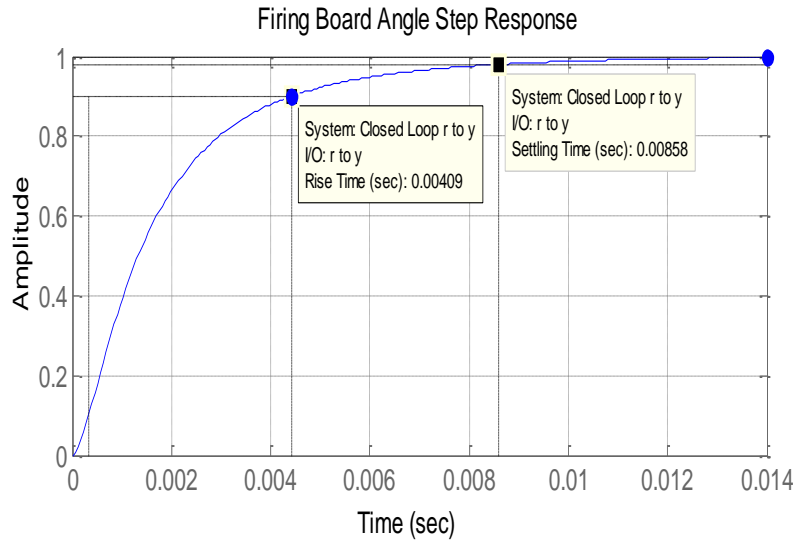


Figure 53 General purpose thyristor firing board angle delay step response.

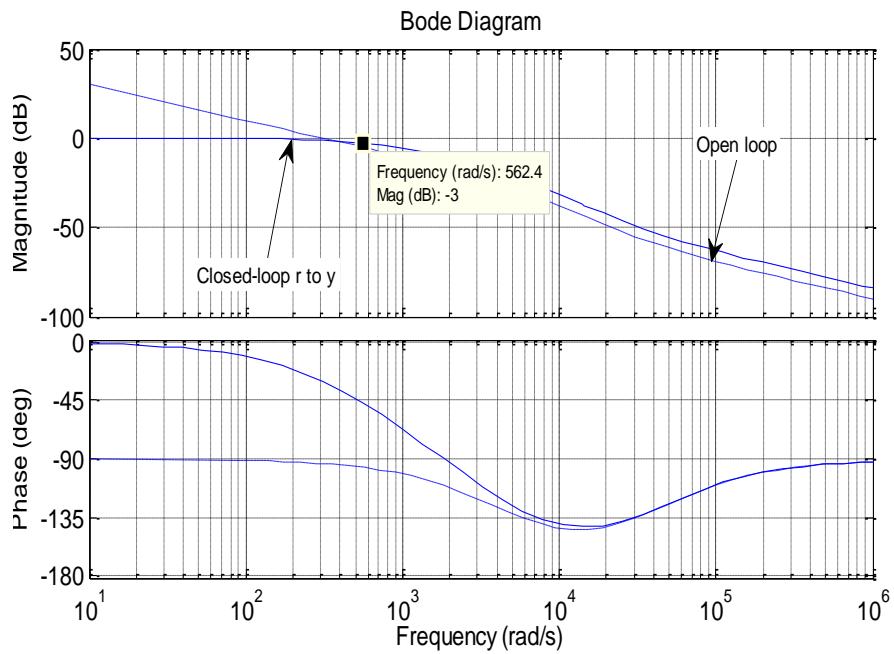


Figure 54 Thyristor firing board angle delay frequency response.

2.6.2 Firing Angle Inherent Sampling and Quantization

Another important observation of firing angle board is that there is an inherent sampling and quantization of the firing angle. This is caused by the discrete pulses in a multi-pulse thyristor rectifier circuit. For a 12-pulse rectifier, as in Figure 22, during each period of the input alternating line voltage, there are exactly 12 instants from which the gate pulses of thyristors could be delayed. Figure 55 shows the firing board step-down response to a step change in delay angle from 87° to 57° . As is can be seen the angle changes is non-uniformly sampled and changes in non-linear discrete steps. This intrinsic sampling of firing angle together with the non-linear angle dynamic causes the angle to change in a stepwise fashion and therefore, the average dc output voltage changes in a stepwise fashion. This will adversely affect the rating of the active filter system.

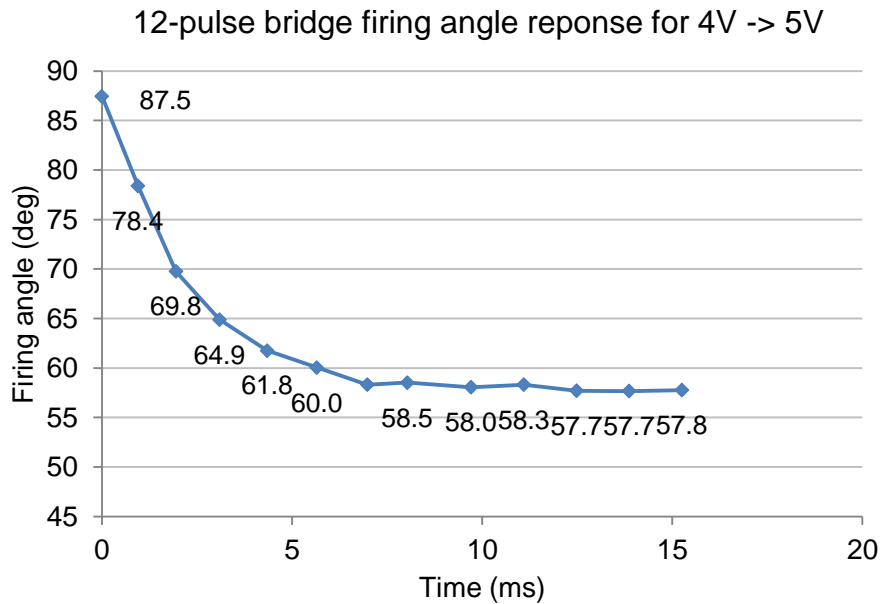


Figure 55 12-pulse thyristor bridge angle response to a step-down angle change from 87° to 57° .

2.6.3 Firing Angle Change Dead-Time

With the rectifier demanding a firing angle change from α_1 to α_2 , there are only p (pulse number of the rectifier) instants that this could happen during each period of ac line voltage. Therefore, there is a possible dead-time between the reference command voltage and actual angle change which only in the most favorable case is zero but otherwise in worst case for a 60Hz ac system could be:

$$0 < t_d \leq \frac{T_{ac}}{p} \rightarrow t_{d-12p-max} = 1.388ms$$

This way exceeds the $200\mu s$ threshold limit set in the dynamic specifications and therefore, the series dc active filter should compensate for that.

2.6.4 Series DC Active Filter in MVDC Amplifier

Considering all the benefits of a multi-pulse thyristor bridge front-end, the major drawback with this front-end topology is the slow dynamics of the MVDC-bus due to slow dynamics of the firing angle in the multi-pulse thyristor rectifier. Knowing this limitation, the only way to meet the target dynamics is by proper design and control of the series dc active filter. In the previously proposed solution [11], [41], the series dc active filter functioned merely as a static ripple compensator rather than improving system dynamics. If there is no control action by the series dc active filter, the filtered dc output voltage dynamic will only be determined by firing angle dynamics. Since the firing angle changes much slower than the target dynamic, the system dynamic specifications will never be satisfied.

The series dc active filter, as part of the amplifier system, will not only statically compensate for the harmonic ripples on the dc bus but also dynamically provide for the

difference between amplifier's target dynamic and the rectifier dc output dynamic. The design of series active filter is driven by *static volt-second (flux) injection*, accounting for static ripple compensation, and *dynamic volt-second (flux) injection*, accounting for the amplifier target dc-bus dynamic. The active filter controller is designed such that these two functional requirements are well performed. The 7.5kVdc nominal voltage MVDC amplifier system of Figure 22 is simulated in MATLAB/Simulink to achieve a $\tau=500\mu\text{s}$ 1st-order time response for the whole system. Figure 56 shows the step command to the amplifier, 12-pulse thyristor rectifier output before filtering, the 12-pulse rectifier dc output dynamic, the MVDC amplifier target dynamic, and the MVDC amplifier final output. The area between the MVDC amplifier target dynamic and the rectifier dc output dynamic represents the volt-second (flux) to be injected and has to be provided by series active filter. In order to design the active filter, the maximum change in flux, $\Delta\phi_{max}$, for the time interval $t_d+\Delta t_1$ is calculated (where t_d is firing angle change dead-time and Δt_1 is the first sampling period).

The active filter is coupled to the dc-link by an integral *series coupling transformer* shown in Figure 22. The active filter converter rating depends on both maximum flux injection and transformer magnetic core characteristic. The transformer is designed to have a linear core characteristic in the region of operation. Figure 57a and Figure 57b show *flux-current curve* of the transformer for 1kV step-up from 4kV to 5kV and 1kV step-down from 5kV to 4kV, respectively. The flux-current curves capture both the steady-state and transient phenomena. The non-closing end is the start of the transient period trajectory before ending in steady-state condition. The longer is the traversed trajectory, the higher the active filter rating would be. As can be seen, the worst case flux injection occurs for a step-down

dynamic and this is the determining factor for the filter rating. This fact is proved by experimental results. Figure 58 shows the required active filter rating for 1kV step-down command to achieve different time constants. It can be seen that a faster time response also requires more active filter rating.

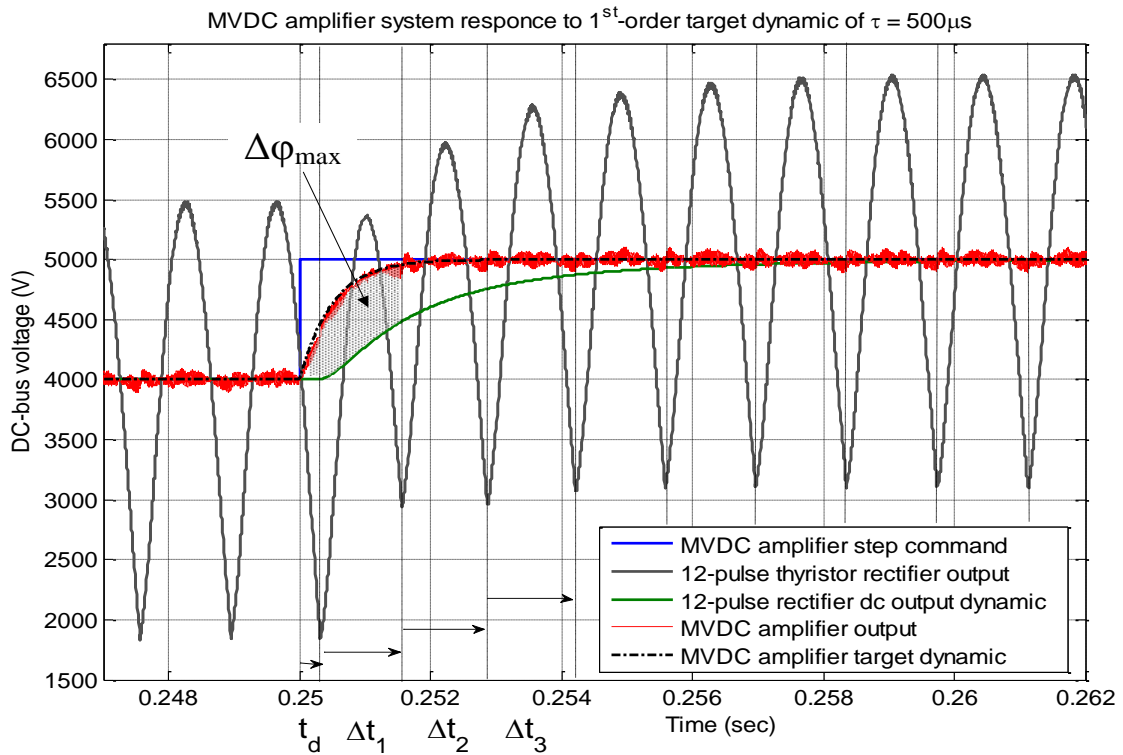
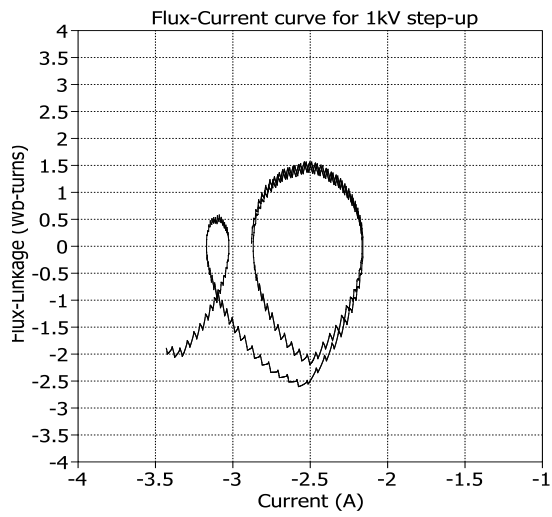
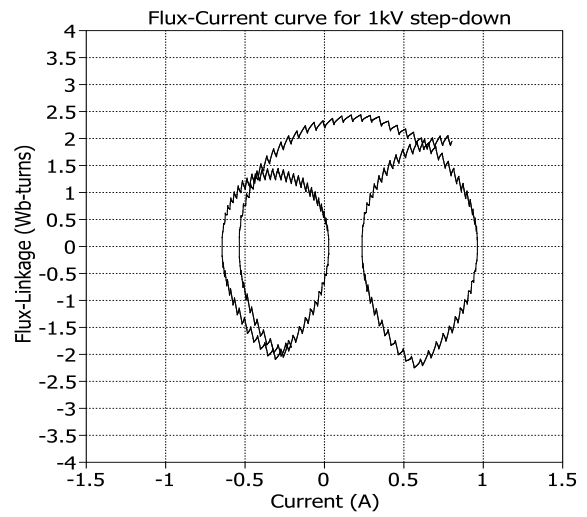


Figure 56 MVDC amplifier response to first-order target dynamic request with $\tau=500\mu\text{s}$.



(a)



(b)

Figure 57 Flux-current curve of series coupling transformer injection for: (a) 1kV step-up from 4kV to 5kV; (b) 1kV step-down from 5kV to 4kV.

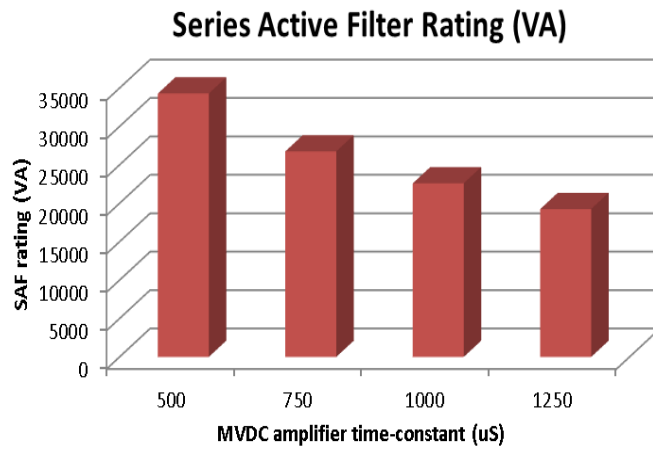


Figure 58 Required active filter rating at different MVDC amplifier dynamic time-constants.

2.7 MVDC Amplifier Laboratory-scale Test-bed Solution

2.7.1 Proposed Laboratory-scale Test-bed

In order to prove the concepts developed in this chapter for both DC active filters and MVDC amplifier system, develop controls, and consider real design considerations, a 12-kVA, 400-Vdc laboratory-scale MVDC amplifier test-bed is developed. Figure 59 shows power circuit diagram and different components in test-bed. At the input, there is a six-phase D/D/Y transformer which supplies the rectifier. The main supply rectifier is a 12-pulse thyristor-bridge that is controlled through a SCR firing board and voltage regulator board. The 12-pulse bridge is comprised of two 6-pulse bridges itself with thyristors in each bridge rated at 1800 V and 160 A. The rectifier could produce a nominal DC voltage of 550 V at the output for 3-ph, 208-V AC supply voltage. At the output of the rectifier a passive LCR filter is utilized to filter high frequency components of ripple voltage out. The series dc active filter consists of a full-bridge inverter, output switching ripple filter, DSP controller and electronic interfaces, and series dc coupling transformer. The full-bridge inverter is of APS IAP75T120 SixPac™ model, which is a three-phase bridge rectifier using 75A/1200V IGBTs. Two types of load are developed to be connected to dc-bus. The first type of load is a resistive load bank. The second type of load is programmable dc electronic load. This will enforce different kinds of load of power source, voltage source, current source, resistive, and/or pulsating nature upon dc-link. For this purpose, a 500-V, 4.5-kW Chroma high power dc electronic load is utilized. Two 5-kVA dual active-bridge (DAB) DC/DC converter are also projected for future developments. The combination these two type loads provides the opportunity to investigate how rectifier/load interactions and pulsating loads would disturb the dc-link. The

test-bed specifications and parameters are provided in Table 22. The components of the test-bed are accommodated in a cabinet which is shown in Figure 60. Different hardware components of series dc active filter are shown in Figure 61. Figure 62 shows the picture of series dc coupling transformer which has a 1:1 turns ratio. Details of transformer design specifications are given in Table 23.

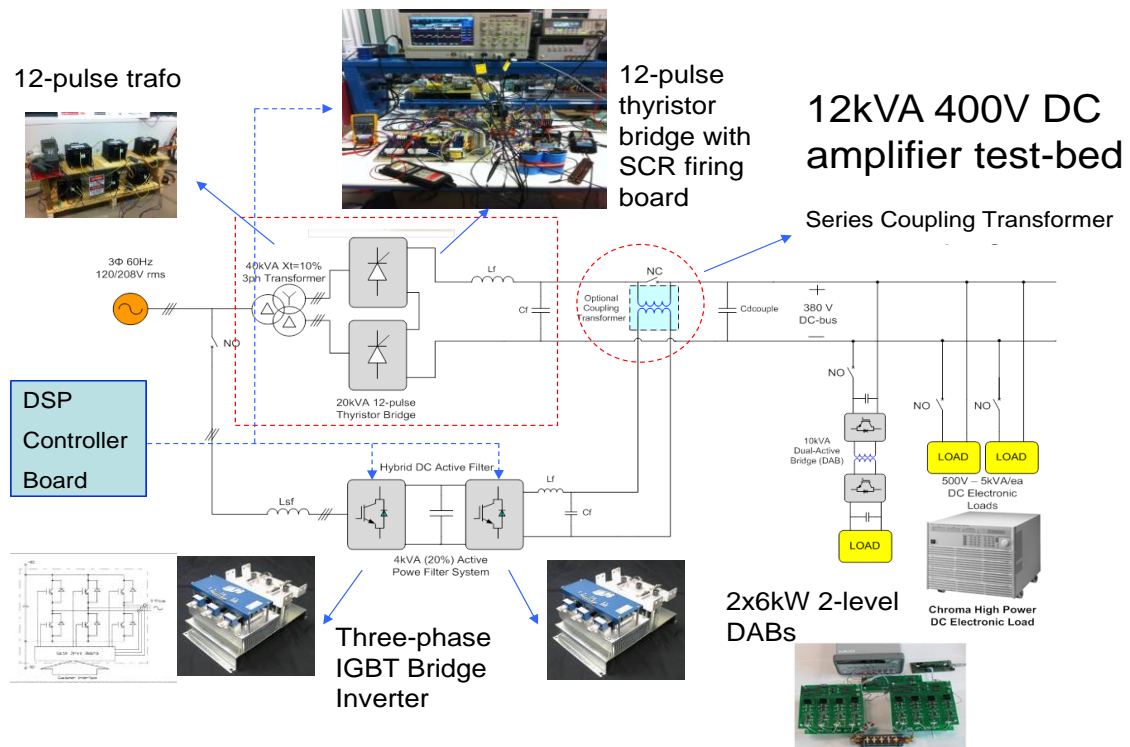


Figure 59 12-kVA, single-supply, 400-V DC test-bed with phase-controlled rectifiers (PCRs) and series dc active filter (SDAF).

Table 22 Test-bed specification and parameters

12-pulse Thyristor Bridge	
Input voltage	3ph/208Vrms
Output voltage range	0 - 550Vdc
Base output voltage	400Vdc
Input 6-phase D/Y/D transformer	6x2kVA at $X_t = 3\%$
Rated power	12kVA
Series DC Active Filter	
H-bridge IGBT inverter	4x1200V/75A IGBTs
DC-link	300Vdc
Switching frequency	21kHz
Output filter	Lf = 230 μ H Cf = 9 μ F Lt = 95 μ H Ct = 666nF Rt = 200m Ω Rd = 5 Ω
Series dc coupling transformer	n1/n2 = 0.998 Lm = 12.3mH Rs1=0.49 Ω , Ls1=1.69mH Rs2=0.12 Ω , Ls2=1.70mH

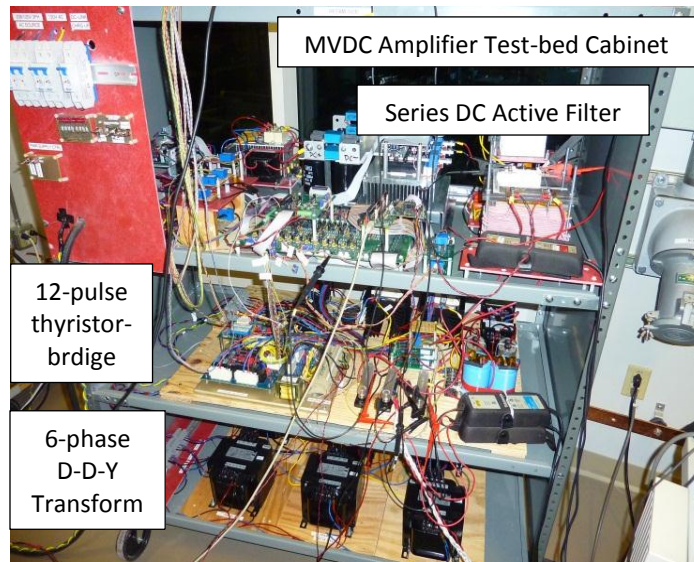


Figure 60 MVDC amplifier test-bed cabinet.

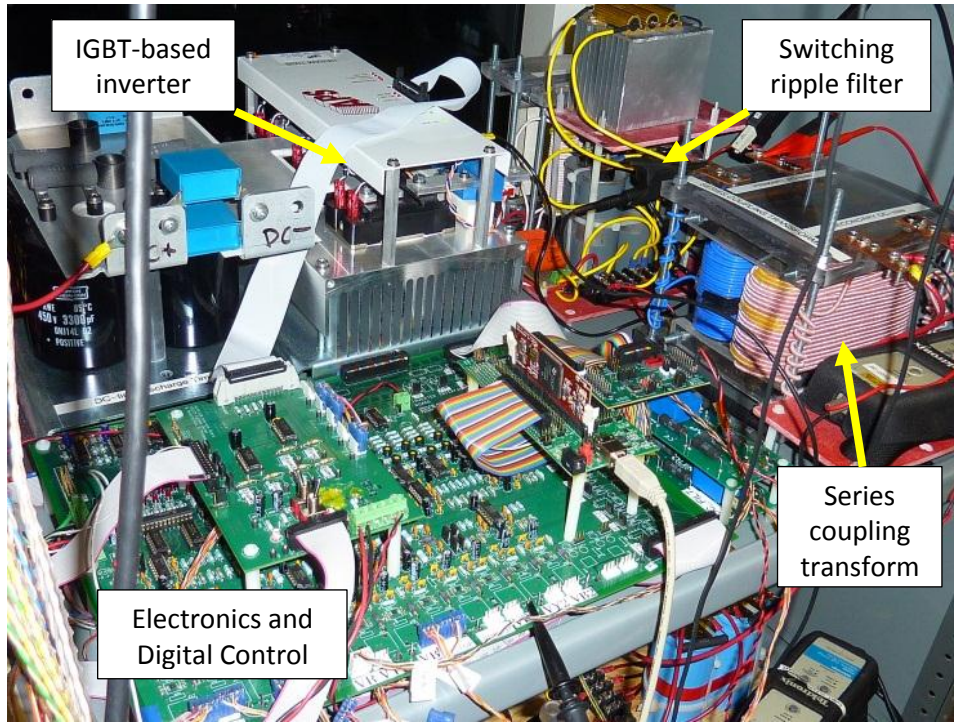


Figure 61 Series dc active filter hardware.

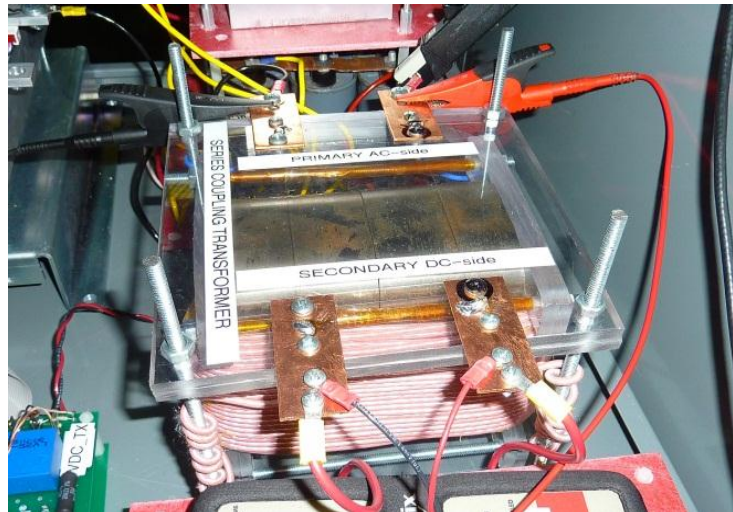


Figure 62 Series DC coupling transformer.

Table 23 Series coupling transformer specifications

Series dc coupling transformer (SDCT)	
Core material	Iron-based Metglas® amorphous alloy
Core type	AMCC-400 C-cores
Stacking number	2
Saturation flux density	1.56T
Core loss	8W/kg @ 0.1T at 20kHz
Switching frequency	21 kHz
Maximum secondary DC current	25A
Maximum primary AC voltage	250V @ 720Hz sinusoidal fundamental
Transformer parameters	n1/n2 = 0.998 Lm = 12.3mH Rs1=0.49Ω, Ls1=1.69mH Rs2=0.12Ω, Ls2=1.70mH
Transformer dimension (LxWxH)	18x15.5x18 cm

2.7.2 Experimental Results

Experiments are carried out to verify the steady-state and dynamic operation of the dc amplifier. The output of the dc amplifier is connected to a resistive load bank with nominal output power of 2.6kW at 400Vdc. Figure 63 shows the steady-state operation of the amplifier at 414Vdc. As it can be seen, the maximum peak-to-peak output ripple of the 12-pulse thyristor-bridge is reduced from 220V to almost 30V. This means peak-to-peak ripple has been reduced to 7.2% of total DC-bus which still needs to be further reduced to comply with requirements mentioned in [4]. Figure 64 shows the steady-state series active filter voltage, current, and power waveforms on the primary-side (AC-side) of the series coupling transformer. In this case the active filter requires only 160VA to filter out the ripple.

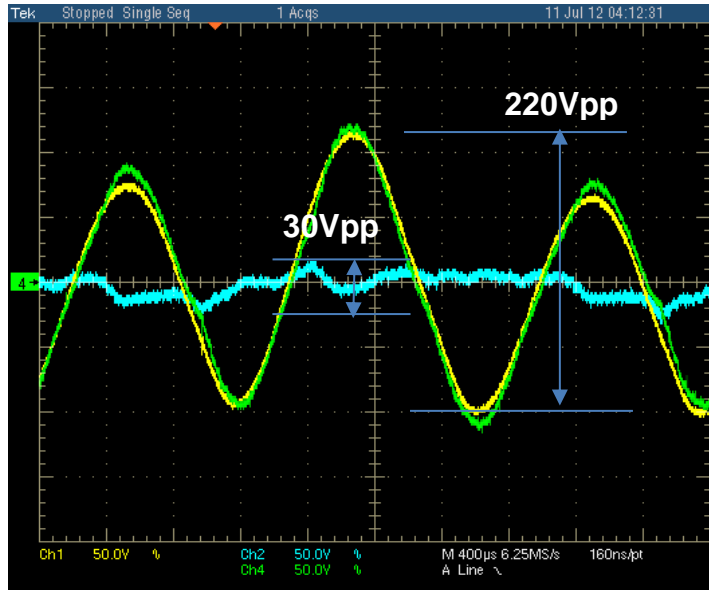


Figure 63 Steady-state compensation at 414Vdc (yellow=output ripple of thyristor bridge, green=active filter series injection, blue=final dc-bus).

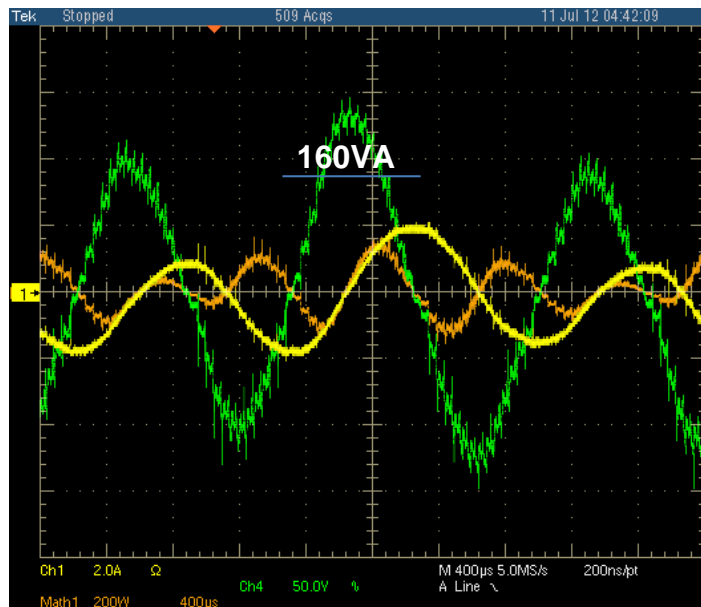
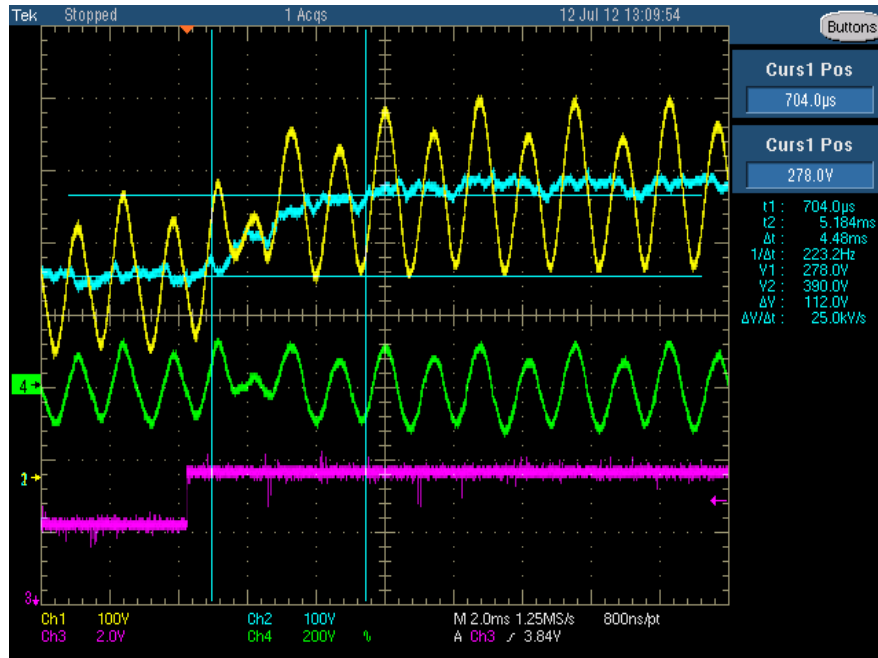


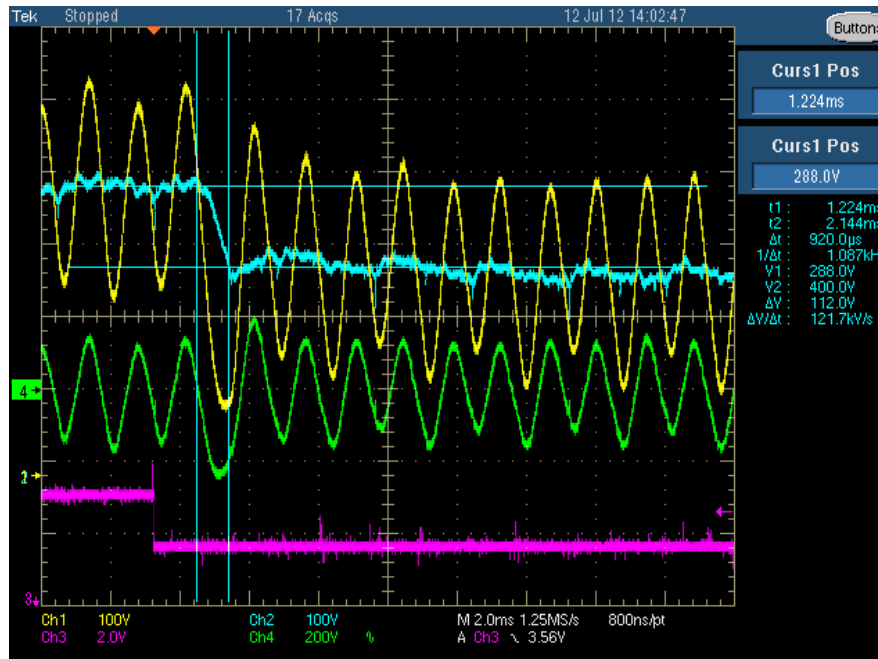
Figure 64 Steady-state primary (AC-side) series coupling transformer waveforms (green = primary voltage, yellow=primary current, brown=instantaneous active filter power).

The preliminary implemented dynamic results for 0.3pu step requests are demonstrated in Figure 65. The dynamic rise-time and fall-time measurements are done within 3% tolerance of the steady-state value. Figure 65a shows that the step-up dynamic dead-time is 704 μ s and rise time is 4.48ms. Comparing with the specifications in Table 19, it can be seen that in both cases the results are yet slower than the requirements. Figure 65b shows that the step-down dynamic dead-time is 1.22 ms and fall time is 920 μ s. It can be observed that the dead-time is still considerably large as compared to requirement but the fall time is fast and meets the specification requirements.

Figure 66 shows the voltage, current, and instantaneous power of the series active filter during the dynamic response. Knowing that the load is a resistive load of 2.6kW at 400Vdc, Figure 66a shows that the active filter requires an absolute maximum of 520W for the 0.3pu step-up dynamic response; and Figure 66b shows that the active filter requires an absolute maximum of 1.4kW for the step-down dynamic response. It can be seen that the active filter requires more rating in case of step-down dynamic response as compared to the step-up dynamic response. This difference in the required rating is also shown in Figure 67 in the voltage-current trajectory of the active filter on the primary-side of the series coupling transformer. The non-closed ends of the trajectories in Figure 67 are the starting point of the dynamic period. It can be seen that the trajectory in Figure 67b has to travel a longer path in the V-I plane beginning from the starting point rather than the shorter path in Figure 67a. This concludes that the required rating is higher in case of a step-down dynamic response as compared to step-up dynamic.

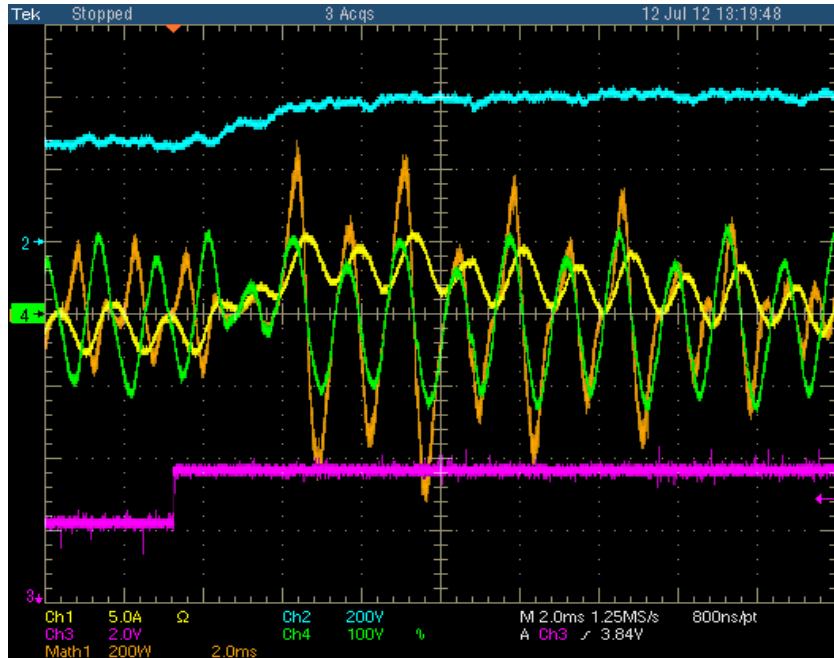


(a)

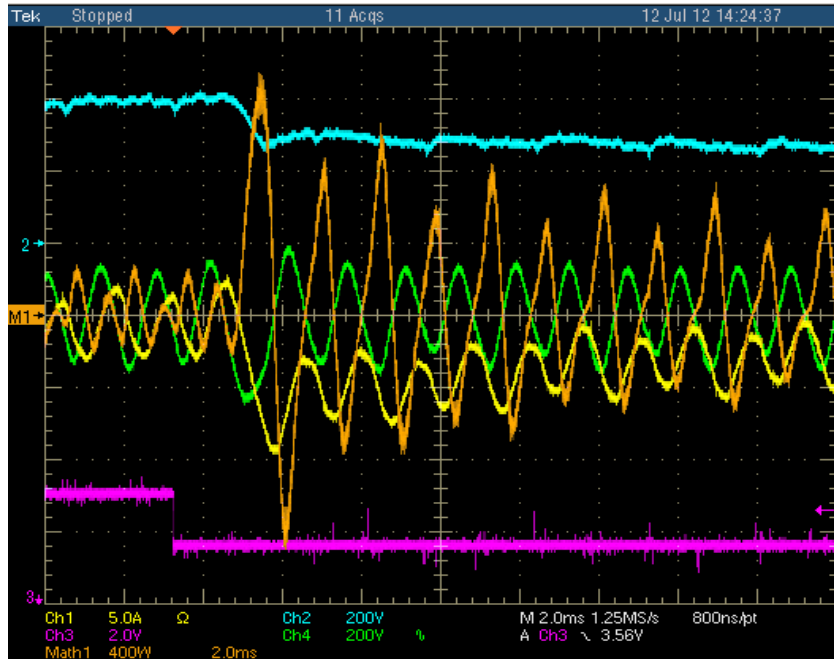


(b)

Figure 65 Dynamic response of dc amplifier test-bed to dc-bus reference change. (a) step-up from 277Vdc to 404Vdc. (b) step-down from 404Vdc to 277Vdc (yellow=thyristor output voltage, blue=final dc output, green=active filter injection).



(a)



(b)

Figure 66 Voltage, current, and instantaneous power of active filter during dynamic response. (a) step-up from 277Vdc to 404Vdc. (b) step-down from 404Vdc to 277Vdc (blue=final dc output, green=transformer primary voltage, yellow=transformer primary current, brown=instantaneous active filter power).

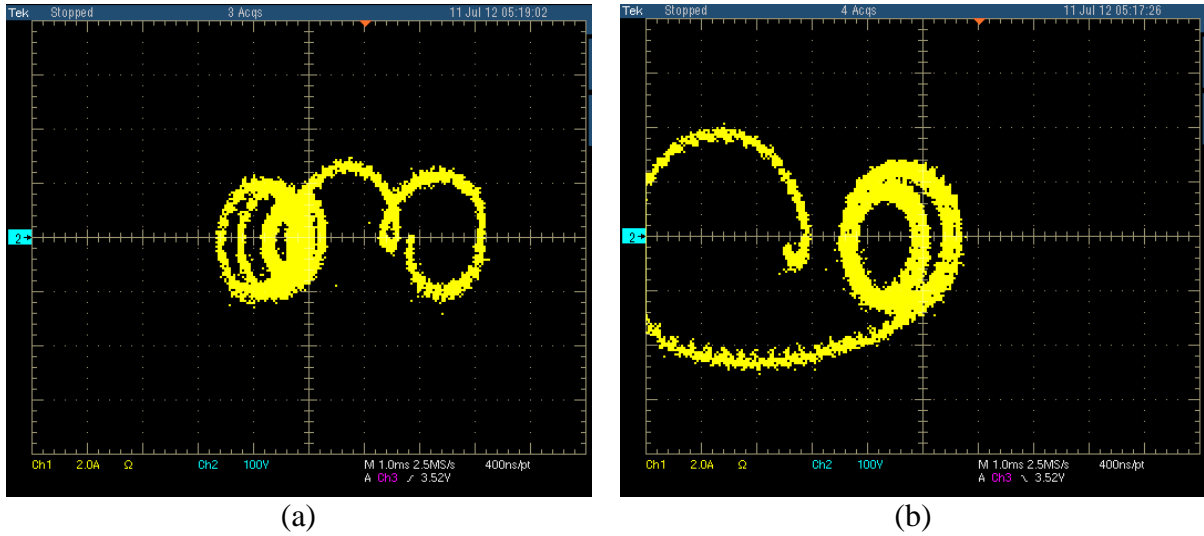


Figure 67 Voltage-current trajectory of series active filter on the primary-side (ac-side) of series coupling transformer during dynamic response. (a) step-up dynamic. (b) step-down dynamic (x-axis is current 2A/div and y-axis is voltage 100V/div).

2.8 Conclusion

In this chapter the issues in current MVDC system such as low front-end rectifier bandwidth, rectifier/load interactions, and emerging loads of very varying nature were investigated. It was shown that there is need to increase dc-link inertia and provide adequate damping during disturbances. The dc active power filter method was proposed to alleviate the problem. These active filters can be implemented in a number of different topologies of either pure -w/o passive filter- and/or hybrid – w/ passive filter- type. Each dc active filter is coupled to dc-link using coupling mechanism. They can also be part of an integrated MVDC amplifier system design.

Furthermore, this chapter introduces the concept and presents the specification of a medium-voltage DC amplifier for DC shipboard power system studies. Basic requirements of

the MVDC amplifier are derived and possible circuit topologies to implement the MVDC amplifier with the required voltage and power rating are reviewed. A multi-pulse thyristor-bridge front-end amplifier system incorporating a series dc active filter is proposed to meet the steady-state and dynamic performance requirements of the system. Proposed amplifier system control components design and their impact on system dynamics studied and verified by simulations. The impact of dc active power filter control and firing angle quantization on amplifier's steady-state and transient behavior are presented. This study provides the design and evaluation required towards a prototype testbed for MVDC amplifier system concept.

Finally, some design issues of a medium-voltage DC (MVDC) amplifier system based on a multi-pulse thyristor front-end technology was presented. Understanding the direct influence of the firing angle dynamics on the overall amplifier dynamics, a general purpose firing pulse generator has been characterized and key observations with regard to firing angle dynamic, sampling and quantization has been made. It is shown that the firing angle dynamic slows down the system and makes it impossible to meet the amplifier dynamic specification. In order to achieve the target MVDC amplifier dynamic, a new compensation method for the series dc active filter is proposed and the required active filter rating is simulated. The preliminary steady-state and dynamic results of a laboratory-scale implementation of a 12kVA/400V dc amplifier test-bed are presented. It is seen that the sizing of the active filter is driven by step-down dynamic response of the system. Further improvements of the test-bed to meet the full system specification requirements are considered for future research.

Chapter 3 Hybrid Front-End Converter System for Large Mobile Mining Machines

3.1 Introduction

In open-cut mining applications, economies of scale play the most important role by helping mine owners keep their mines productive and thus, stay competitive. Large mobile mining equipment such as big excavators, electric rope shovels, draglines, and big mining haul trucks are employed to move massive amount of surface material. The huge dipper (bucket) payload capacity of these loading machines when matched with the optimum haul truck size allows for increase in production rate with fewer loading passes. In this regard, 3-loading pass of mining haul trucks has been accepted as a benchmark by mining industry [44], [45]. Figure 68a shows different mechanical motions of an electric rope mining shovel and Figure 68b shows a 109-tonne nominal payload capacity shovel with 62 m³ dipper capacity which can load a 330-tonne mining haul truck in 3 loading passes [44].

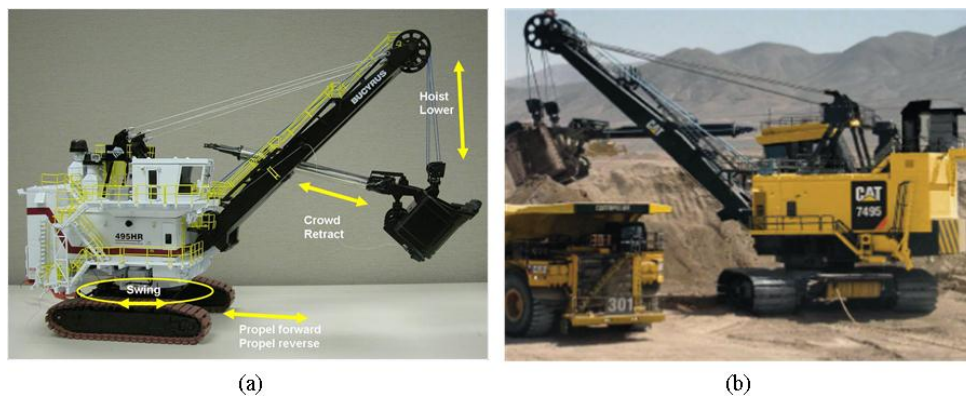


Figure 68 Electric rope mining shovel. (a) different mechanical motions. (b) a 109-tonne payload capacity electric shovel loading a 330-t haul truck [44].

Mine operators are constantly seeking ways to increase productivity and efficiency and reduce cost-per-ton of production in their mine to stay competitive in the market; they perform extensive planning and deploy all their resources in order to maximize removal rate of overburden during mining process while keeping the total cost of ownership (TCO) of the equipment to the lowest. These objectives necessarily require faster and higher capacity load cycles, lower meantime between failure and lower time to repair, higher machine uptime, and higher utilization for the mining equipment. Thus, to meet the needs of the mine operators, mining equipment manufacturers are continuously striving to make mining equipment which possesses higher safety, reliability and efficiency characteristics. Maximizing production rate generally means building equipment that are larger, faster and more powerful and can operate with higher reliability and less downtime. It is in this regard that the traditionally direct current (DC) static electric drive system – there is also a DC rotating drive system based on motor-generator (M-G) sets which is nearly an obsolete technology – for large mobile mining machines has increasingly been replaced with AC static electric drive system [46], [47]. The major advantage of AC drives stems from the squirrel-cage induction motor technology which eliminates the brush and commutator assembly in DC machines resulting in higher speed, increased power density, greater efficiency, higher reliability, and lower maintenance for AC motors [46], [48]. By utilizing AC motors for all of the mining dragline excavating motions (hoist, crowd, swing, and propel), a 20% increase in production rate and a system efficiency of 86%-89% was reported versus the 74% efficiency of DC drives, [49]. The benefits of AC drives over DC drives are summarized in Table 24.

Table 24 Summary of benefits of AC drive over DC drive for mobile mining application

Category	Influencing factor	Positive impact	AC drive	DC drive
High productivity	Speed	Faster Cycle time	+++	+
	Power density	Larger Equipment and increased payload	++	+
	Reliability	Extended mean time between failure (MTBF)	+++	+
	Availability	Higher equipment utilization and less down time	++	+
Low cost-per-ton	Efficiency	Lower losses and energy cost savings	++	+
	Maintenance	Reduced mean time to repair (MTTR) and spare parts inventory	+++	+

3.2 Current Front-End Converter Technologies for Mining Excavating Machines

The power circuit of AC drive system for large electric mining excavating machines (shovels and draglines) consists mainly of input transformer, front-end, inverter and AC induction motor, as it is shown in Figure 69. The front-end converter interfaces with the input transformer at the point of connection to grid and converts the three-phase input AC voltage to a regulated DC voltage to support the DC-bus. The inverters then draw power from DC-bus to drive the AC induction motors for different motions during a mechanical loading cycle. The DC-bus is supported by many DC capacitors, so that power can be easily exchanged between inverters independent of the front-ends, and is protected against unsafe voltage overshoots during regenerative mode by DC choppers and bleeding resistors.

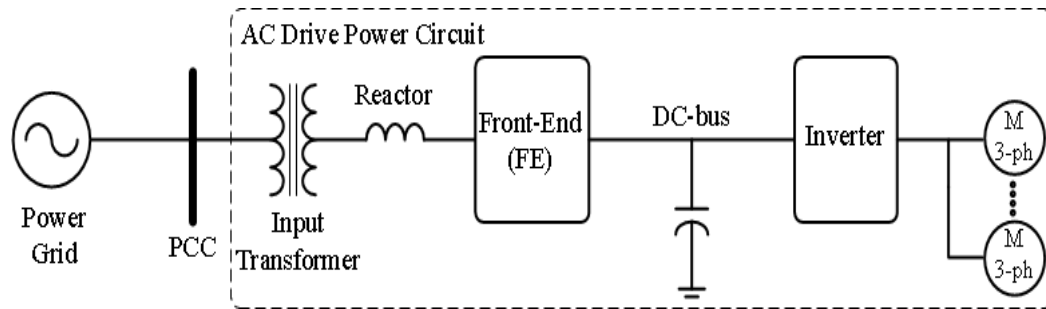


Figure 69 General power circuit diagram of an AC drive system for mining application.

3.2.1 Passive Front-End (PFE) – An Old Technology

Traditionally, the front-end technology of choice in drives has been the passive front-end technology of multi-pulse (6, 12, or higher number of pulses) diode- or thyristor-bridges based on diode and/or silicon-controlled rectifier (SCR) power switch technology. Since these power switches could not be actively turned off, they are only commutated by AC line voltage (line-commutated) and hence, they are named “passive front-end (PFE).” PFEs, due to line commutation, inherently produce a great amount of harmonic distortion and, in case of thyristor-bridges, a lagging power factor (PF) at the point of common connection (PCC) to grid. Total harmonic current distortion (THDi) could be as high as 54% in 6-pulse configuration and uncompensated lagging PF could be as low as 0.4 [46], [50]. Figure 70 shows the power circuit topology of a 12-pulse non-regenerative shovel AC drive system rated at 1.85 MVA, [50]. Each of the 4 inverters at the output is rated at 790 kVA and drives the motor(s) that power different motions during a mechanical loading cycle.

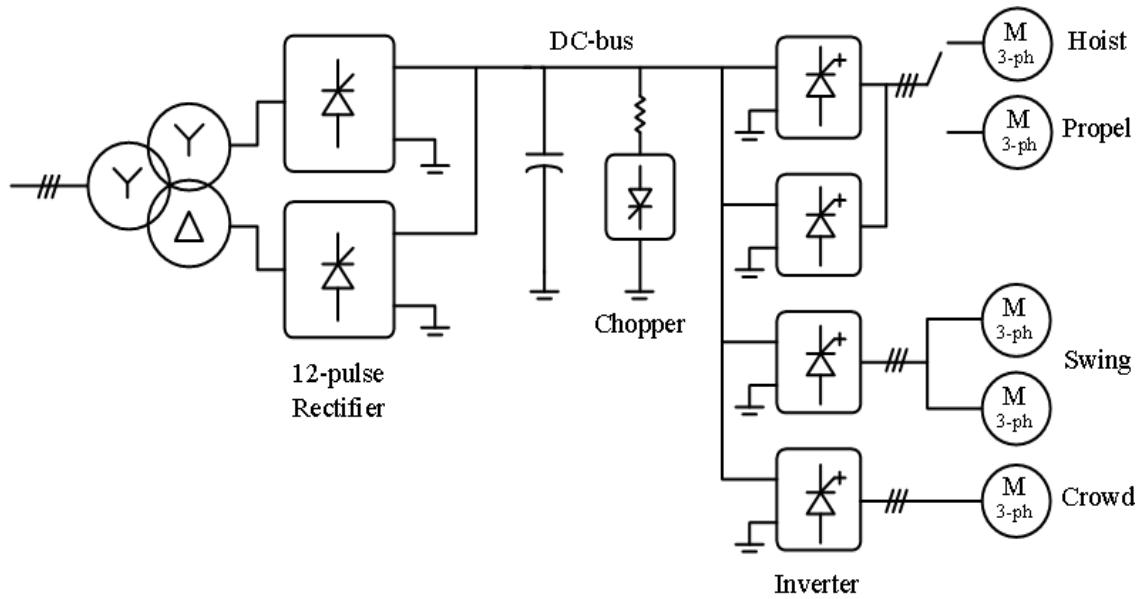


Figure 70 Power circuit topology of a 12-pulse non-regenerative shovel drive system rated at 1.85 MVA, as in [50].

Power quality, in terms of harmonic distortion and power factor, is an important factor in power grid compatibility, utilization and robustness of mine network. High current distortion at PCC increases losses in all power system components interfacing with grid, mainly distribution feeders and power transformers; and lagging reactive power at PCC requires much higher apparent power capacity to deliver the same amount of active power to loads (electric motors). Higher apparent power capacity means higher current capacity resulting in increased RI^2 losses and over-dimensioning of power system components. Moreover, the large lagging reactive power causes extra voltage drop that, especially in case of long distribution lines and/or weak mine network, can adversely affect system voltage at PCC and force expensive equipment downtime, [50]. In the traditional approach to alleviate power quality problems associated with PFEs, tuned passive filters, i.e., 5th- and 7th-harmonic tuned

filter for 6-pulse configuration, and reactive power compensator (RPC), consisting of switched capacitor banks with phase-controlled reactors, are typically employed at PCC to reduce harmonic current distortion and improve power factor, respectively. However, not only is the effectiveness of these approaches prone to changes in system configuration, as reported in [50], but also the add-on nature of it decreases system reliability and makes system troubleshooting and maintenance harder and more expensive.

3.2.2 Active Front-End (AFE) – A Modern Technology

Large mines are often located in remote areas with limited infrastructure and accessibility to utility power and consequently, in some cases, they have their own on-site power generation. High productivity, high efficiency and low maintenance of AC drive system requires a reliable front-end technology that is robust and independent of mine network, and meets mine's power quality requirements of low harmonic distortion and unity or leading power factor. In this regard, the preferred technology of choice for front-end converters in modern AC drives is the "active front-end" (AFE) technology. The AFE, utilizing the forced-commutated insulated gate bipolar transistor (IGBT) technology, boosts the output voltage beyond diode-bridge and actively modulates input voltages to control input current's shape, amplitude and phase angle.

To overcome the shortcomings of PFEs at input side, many high power active front-end (AFE) converters are utilized in staggered fashion (parallel with different phase shift) to produce low harmonic distortion and to provide VAR compensation at the grid-side of drive system [46], [47]. Utilizing the 3.3-kV/1700-A IGBT technology, 1-MVA-rated AFE units are achieved. Currently, mining shovels are manufactured up to 5 MW and walking draglines

are manufactured up to 24 MW. In high power draglines, as many as 24 (standard) or 32 (leading power factor) AFEs are put in parallel [47]. Draglines are often required to provide a leading PF (~2% P.U. VAR), whereas shovels usually operate under unity PF [47], [51]. Figure 71 shows an electric circuit diagram where two or more AFEs are staggered with phase shift to supply the AC drive system of a modern mining excavating machine. Table 25 gives the AFE-side parameter of modern AC drive system. Figure 72a shows simulation results for a 1.5-MW shovel in which 2 AFEs are staggered resulting in a THD of 4.87% at nominal current, and Figure 72b shows simulation results where 32 AFEs are staggered resulting in a THD of 0.2%. The improved THD performance of AFEs at PCC is achieved with no extra passive filtering on the input side as compared to PFEs where tuned filters are typically required. Thus, it increases system reliability and efficiency.

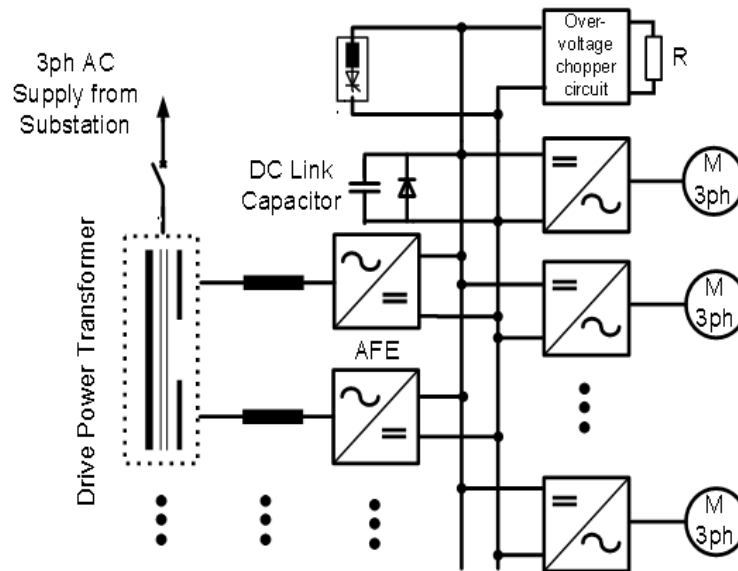


Figure 71 Power circuit diagram of a modern AC drive system for mining excavating machines [51].

Table 25 Active front-end (AFE)-side parameters [51]

Line-to-line voltage (AFE side)	E_d	900 V rms
Line frequency (grid)	f	60 Hz
Leakage inductance	L_s	16% PU
Interface resistance	R_s	0.4% PU
Each converter rated power	S_n	1 MVA
Number of AFEs	N_{AFE}	2, 4, 32
Nominal DC link voltage	V_{DC}	1.8 kV
Chopper circuit threshold	V_{ch}	2 kV
Crowbar circuit threshold	V_{cr}	2.2 kV
DC link capacitance	C_{DC}	12 mF
Switching frequency	f_s	540 Hz
Converter loss resistor (estimated)	R_p	1% PU
Absolute overcurrent capability	I_{max}	2 PU
Current regulator response time	τ_i	2~5 msec

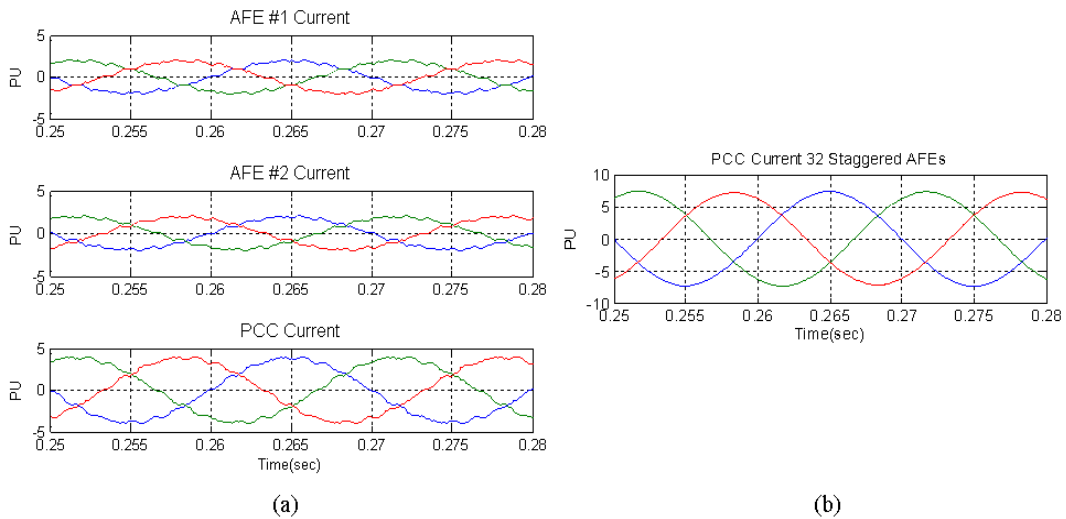


Figure 72 Simulation results of staggered AFEs in AC drive system. (a) 2 staggered AFEs in a 1.5-MW mining shovel. (b) 32 staggered AFEs [51].

3.3 Supplementary Energy Storage Integration

3.3.1 Motivation

A typical mining excavating process load cycle has major motoring and regenerative power regions [50], [51]-[53], as it is shown in Figure 73. The electric power regeneration, which occurs during swing motion deceleration and lowering of dipper in shovels, can amount up to 60% of motoring peak power demand, [54]. If this large regenerative power is not handled properly, it can lead to unsafe DC-bus voltages, and in extreme case, force a system shutdown in overvoltage protection. Thus, being able to handle this excess power safely and reliably is a technical requirement in mobile mining drive systems. Conventional non-regenerative drive systems based on PFEs employ chopper circuits with bleeding resistor to dissipate regenerative energy, whereas the PFE-based regenerative counterpart like 6-pulse dual converter topology can regenerate power but faces low reliability due to occurrence of thyristor commutation failure, [50]. Modern drive systems utilizing IGBT-based AFEs are advantageous to the conventional drive systems because of the inherent ability of AFEs to regenerate power reliably, [46].

However, mines are often located in remote areas where access to commercial electric power is not readily available and where deployment of local off-grid generation greatly limits the ability of mining distribution system to absorb regenerative power, like Pribbenow Mine located in Colombia S.A with a 24-MW generation capacity, [54]. Thus, the practical solution currently is simply to dissipate the excess energy into resistive load banks using chopper circuits to keep the DC-link of AFEs within safe operational margins, [47]-[54].

On the other hand, supplying peak power demand in large multi-motor mining machines is always challenging, especially in isolated, off-grid power systems. Load swings of active and reactive power during a load cycle and motor starting power are large relative to the power system's generation capacity. Because there is a limit to how quick a generator can pick up a load, keeping up with fast and dynamic load swings of large loads is particularly challenging. For example, a CAT 7495 electric shovel can switch from regenerating 2.5 MW of power to demanding 3.7 MW of power in less than a second which makes it very difficult for a generator to supply, [55]. Moreover, power generator sets supplying fluctuating loads have to be de-rated due to active governing and mismatches resulting in unequal power sharing during dynamics, [56]. The conventional solution for large electric shovels is to use multiple generators with a total of 8 MW capacity to achieve rapid load response when peak power is demanded, [55].

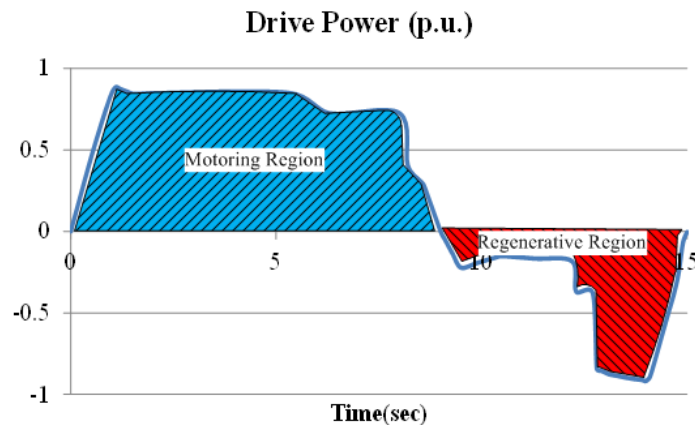


Figure 73 Drive power of a typical mining excavating process [51].

3.3.2 Energy Storage Technology

As it was explained, the standard practice to meet the needs of large mining loads, in terms of rapid load response and peak power demand, is simply to overdesign power system components. In addition to increased up-front capital investment, this leads to a system with higher fuel and energy consumption, higher carbon emission, lower efficiency and higher operating and maintenance costs. To solve the issues posed by peak power demand, better load power management, increase power system utilization and efficiency and reduce environmental impact, peak power shaving strategy is introduced, [52], [57]. In this load management scheme, the power regenerated in mining machine, as in during hoist lowering and swing deceleration of shovels, is stored in an energy storage system and is used to reduce peak power demand of the drive system. This results in savings not only in terms of energy costs but also in terms of extra capital investment which would otherwise be necessary to increase power system rating.

To choose the proper energy storage technology, several economic and technical criteria such as energy cost, weight, volume and temperature are considered and the results are presented in Figure 74 for 1.5-3 MW shovels, [51]. Based on the obtained results, ultra-capacitor has been selected as the technology of choice for shovels. Similar conclusion can be made about draglines.

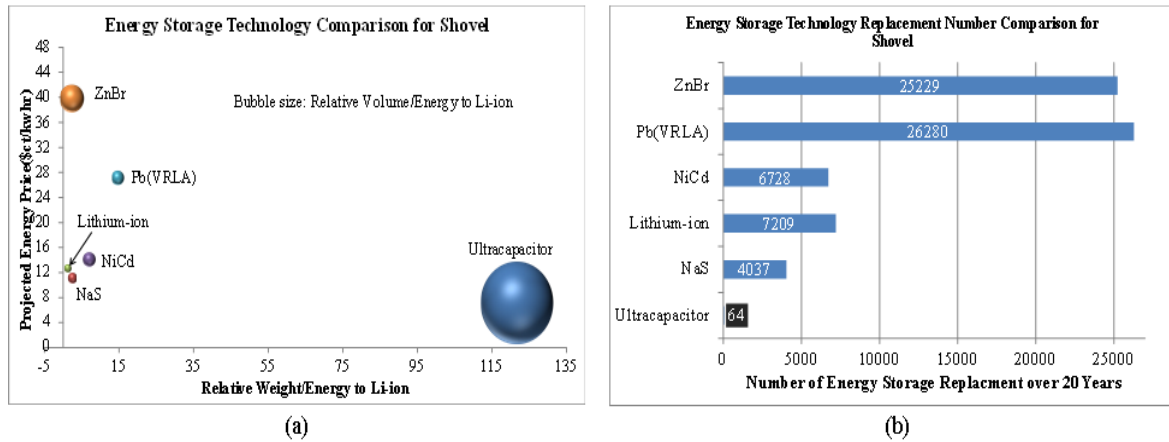


Figure 74 Energy storage technology comparison for shovel [51]. (a) projected cost with respect to relative weight/energy. (b) number of energy storage replacements.

3.3.3 Ultra-capacitor Integration to High Power Mining Converters

Ultra-capacitors can be integrated to dc-bus of AC drive system either directly or indirectly, through a separate DC-DC converter [51], [52], [58]. In the direct method, the drive-side inverter has to tolerate a flexible dc-bus, whereas in the indirect method the fast DC-DC converter helps with DC-bus control, though special care should be taken to avoid any conflict between AFE controller and DC-DC controller, [58]. Figure 75 shows power circuit diagram of modern drive system for mining excavating application with indirect (DC-DC) ultra-capacitor energy storage integration. Simulated performance of a 1.5-MW, AFE-based shovel indirectly integrated with 7-F stack of ultra-capacitors is shown in Figure 76. The excess regenerated power stored in ultra-capacitors when used according to peak-shaving strategy has been observed to reduce the required rating of the front-end equipment to 0.73 P.U., [51], [58].

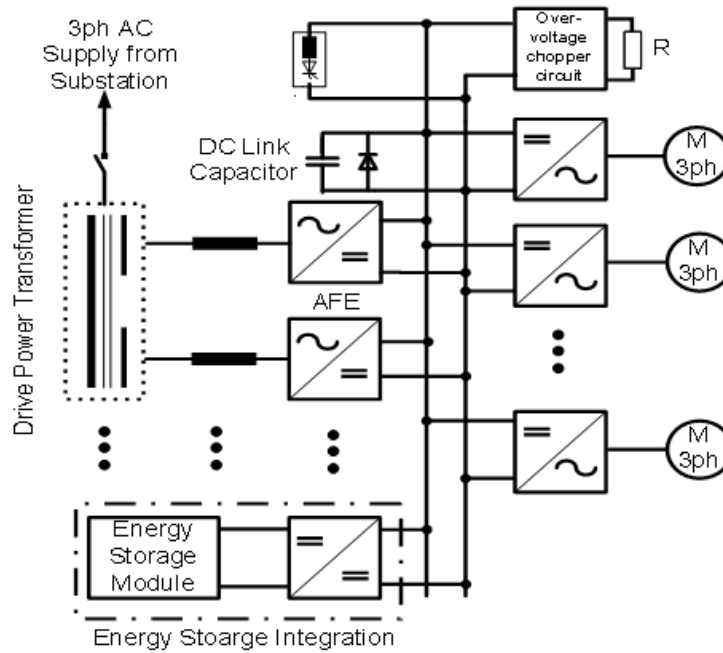


Figure 75 Power circuit diagram of electric drive system for mining excavating machine with indirect ultra-capacitor energy storage integration [51].

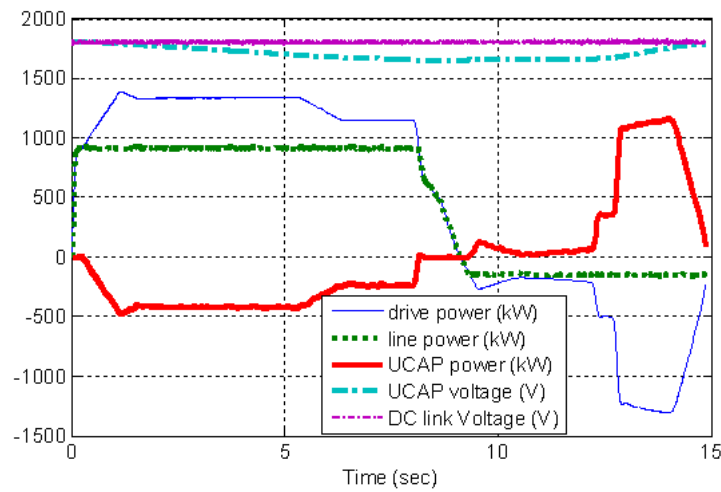


Figure 76 Simulated performance of 1.5-MW AFE-based shovel with indirect (DC-DC) integration 7-F stack of ultra-capacitors [51].

3.4 Hybrid Front-End (HFE) Converters for High-Power Mobile Mining Drives

Although the proposed ultra-capacitor energy storage integration has clear benefits to the mine network, especially in terms of power system utilization and energy management; however, converter components' rating of either electrical or mechanical parts, would not change significantly for large mining machines. It can be shown that the benefits from possible downsizing of components by ultra-capacitor integration cannot be realized for a dragline, and even a shovel, considering the desired harmonic and power quality performance, number of spare converters, weight and volume. Consequently, for the mining equipment manufacturer, the proposed energy storage integration into the current mining drive system, as depicted in Figure 75 can be seen as an add-on component which mostly increases equipment cost and complexity.

In order to truly exploit the benefits of energy storage integration for the mining equipment, two straightforward front-end converter topologies have been proposed for next generation of high-power, multi-motor mining machines such as draglines and shovels, [51]. In these front-end converter configurations, an ultra-capacitor is still used through a DC-DC converter to harvest the regenerative energy of the mining drive and harness it for peak power shaving during motoring mode. Thus, instead of bi-directional AFEs, unidirectional rectifiers based on high-power, mature and reliable technology of diode- or thyristor-bridges are used. As it was mentioned before, 6-pulse unidirectional rectifiers suffer from poor THD at PCC. To overcome the THD performance deficiency, a multi-pulse (12-pulse or higher), which drastically improves THD as compared to a simple 6-pulse bridge, is assisted with a

fractionally-rated (~3-5%) parallel active power filter (APF) to improve THD performance, and also provide partial VAR support (~2% P.U.) at PCC. The unidirectional rectifier is PFE-based and the active filter is AFE-based; hence, this new category of converters are called “hybrid front-end” (HFE) power converters.

In the first HFE topology (HFE-I), a 12-pulse diode-bridge is assisted with a fractionally-rated hybrid active power filter, as depicted in Figure 77. The selected simulation results for harmonic performance evaluation of this system at PCC are shown in Figure 78. As it can be seen, the current THD is less than 5% which also complies with IEEE 519-1992 standard for allowable harmonic distortion. This topology is projected for 1.5-MW shovels [51].

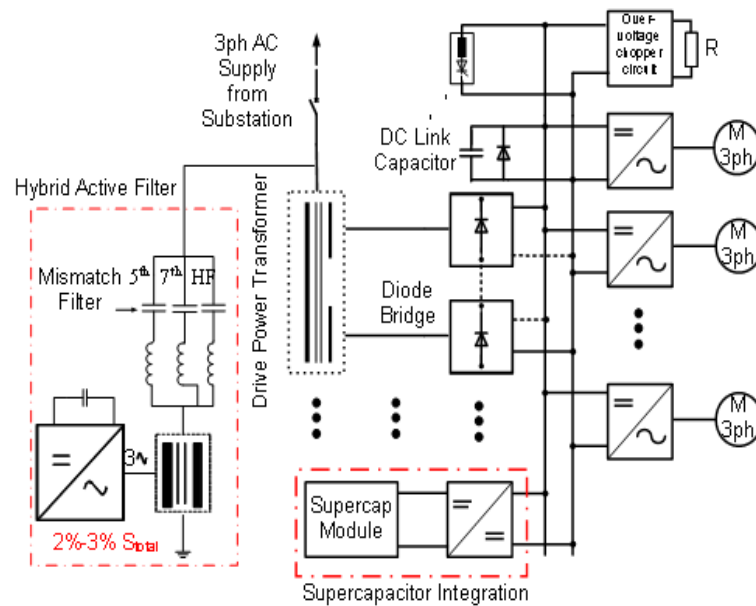


Figure 77 HFE-I topology — a unidirectional 12-pulse diode rectifier is assisted with partially-rated hybrid parallel active filter system.

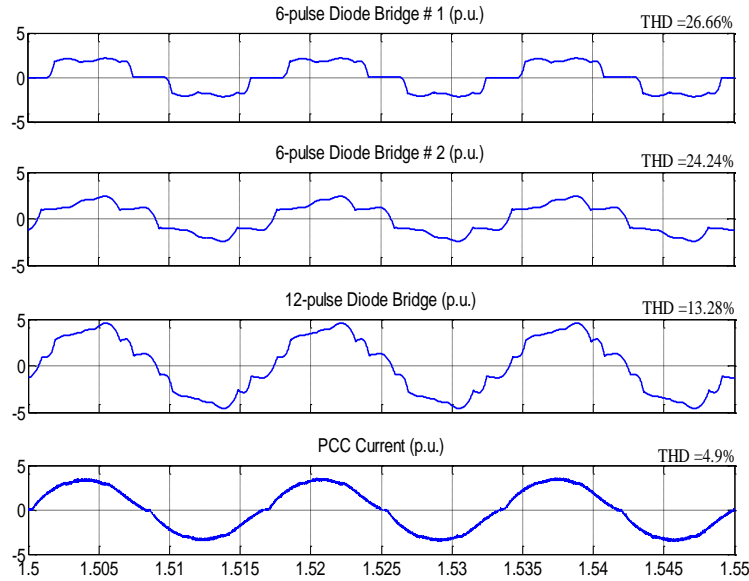


Figure 78 Simulated current THD performance of HFE-I topology at PCC.

In the second proposed HFE topology (HFE-II), a 12-pulse diode- or thyristor-bridge is still used to convert three-phase AC electric power to DC; however, an AFE-based converter is connected in parallel with the main rectifier at grid-side to PCC and at drive-side to DC-link, as shown in Figure 79. Although the converters in this topology share a common DC-link, only the main rectifier provides active power flow to drive-side inverters, whereas the fractionally-rated, AFE-based converter acts as an active power filter to reduce harmonic current distortion at PCC and also provide partial VAR support as needed to improve system power quality. The choice of thyristor-bridge as the main rectifier assures an adjustable and regulated DC-bus voltage on the drive-side; however, it introduces an input current with lagging PF that needs to be considered. The three-phase, multi-winding transformer used at the input of diode- or thyristor-bridge is not an additional component since it is already used

in staggered AFE topology. The active filter converter connected in parallel with the main rectifier is nothing but a spare AFE converter retrofitted for the hybrid topology. The bi-directionality of the AFE employed in HFE-II topology enhances system functionality and reliability, as compared to HFE-I, by providing a partial path for active power to and from the machines that could be used for pre-charging DC-bus or feeding some of regenerated power during load cycle back to the grid.

To develop the hybrid configuration, Figure 80 presents the proposed control structure for the hybrid architecture with specific attention to 12-pulse thyristor-bridge and the AFE. The pure parallel active filter control in the hybrid option is based on synchronous-reference-frame (SRF) controller structure used for harmonic load current extraction, [59].

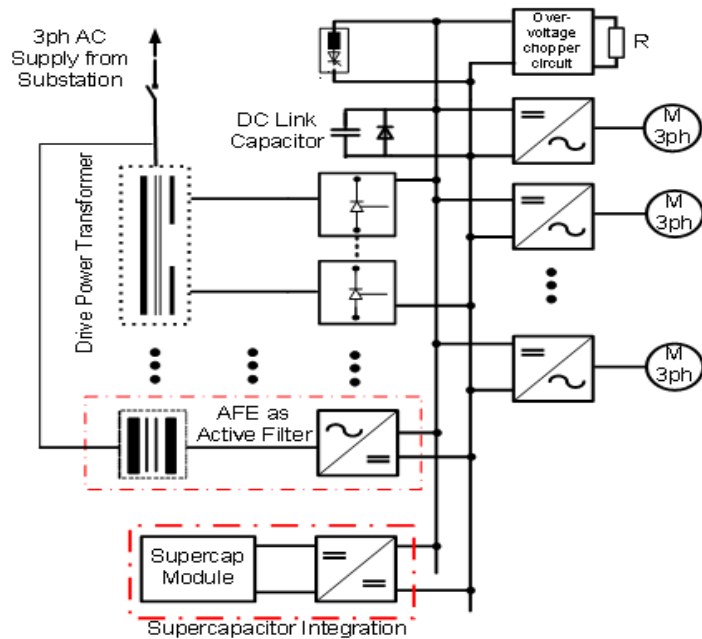


Figure 79 HFE-II topology — a 12-pulse thyristor-bridge is parallel connected with an AFE at PCC and DC-link.

Figure 81a shows the simulated currents for the proposed system at PCC, and Figure 81b shows the frequency spectrum and THD of the current at PCC before and after compensation. As can be seen, at the PCC, the current THD is less than 5%, and thus, IEEE519-1992 requirements are met.

In the SRF method, current controller proportional gain (K_{pc}) is important with regard to DC-link dynamics and power exchange between the converters, especially, when both share the same DC bus. Simulated results in Figure 82, for a constant gain of $K_{pc}=5$, shows dc-bus oscillations for step-down load condition from 8kW to 1kW. Since harmonic distortion requirements are for rated load condition, a load adaptive gain scheduling method is designed to control and smooth out dc-link oscillations. Figure 83 shows the simulation results when the gain is reduced to $K_{pc}=2$ for the same step-down loading condition but in this case, the dc-link oscillations are damped out. It is believed by the author that this is an important finding since common DC link for active filter and the main front-end has not been implemented as an integrated solution. In other words, DC link loading affects the dynamics of the active filter which results in uncontrolled or marginally stable operation of the whole system especially at light load conditions.

As final remarks, the benefits of HFE configurations over current state-of-the-art AFE technology can be listed as follows:

1. Hybrid front-end converters facilitate the integration of energy storage systems into high-power mining machines.

2. The proposed system uses high-power, highly efficient, reliable, and mature diode-based or thyristor-based technology.
3. The new systems still require the input transformer for isolation and phase shifting but will have fewer power switches leading to increased power density.
4. The hybrid diode-based front-end (HFE-I) configuration requires some passive filtering, and therefore, it is more suited for lower power mining equipment like shovels.
5. The hybrid thyristor-based front-end (HFE-II) technology, retrofitting an AFE unit as active filter for harmonic compensation and VAR support, is more suited for high-power draglines or larger shovels.
6. The active filter in both system configurations ensures that the THD is between ~3% and 5%.
7. The proposed systems' control complexity is much lower compared to state-of-the-art AFEs.

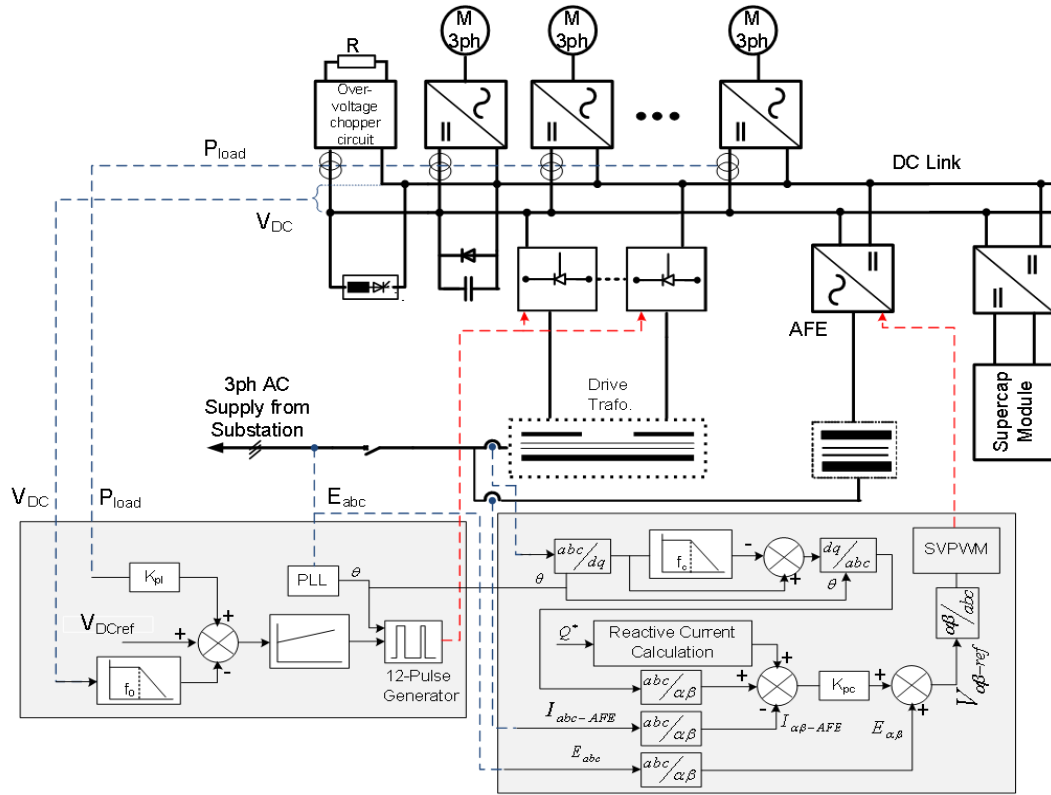


Figure 80 Control system for HFE-II topology based on 12-pulse thyristor-bridge.

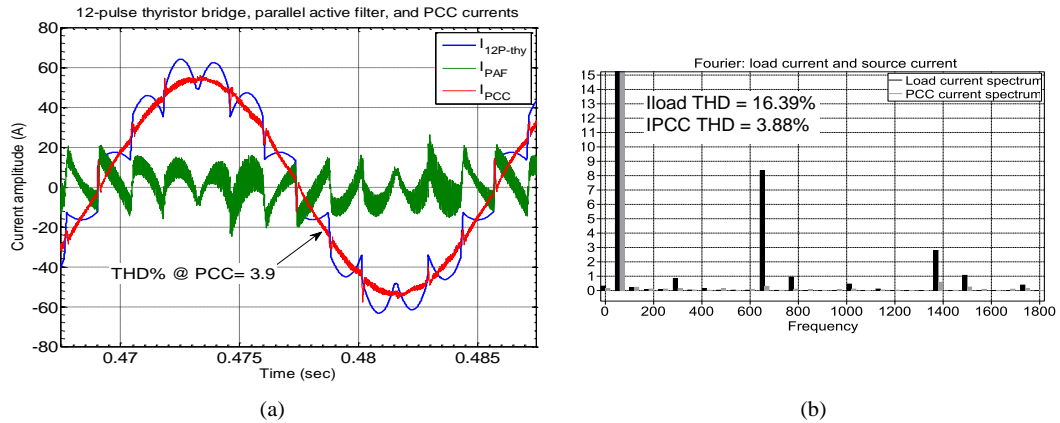


Figure 81 Simulated performance of HFE-II topology with 12-pulse thyristor-bridge. (a) grid-side current waveforms. (b) load and PCC current frequency spectrum.

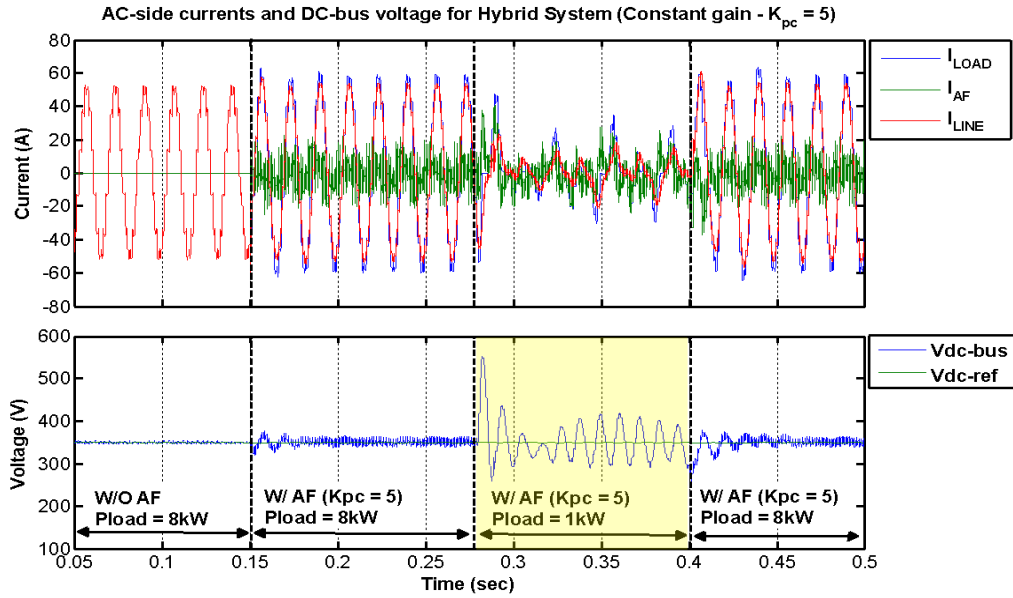


Figure 82 Simulated hybrid front-end waveforms without adaptive current compensation gain (K_{pc}).

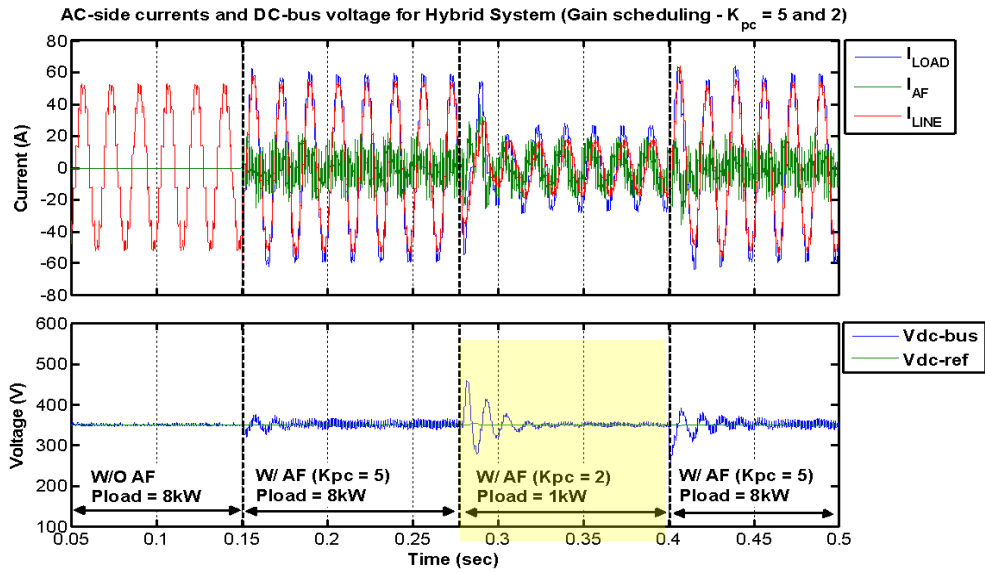


Figure 83 Simulated hybrid front-end waveforms with adaptive current compensation gain (K_{pc}).

3.5 The laboratory-scale hybrid front-end test-bed for mobile mining application

In order to test, further specify and experimentally verify performance characteristics of the proposed HFE configuration, a 3-ph/12-kVA grid-connected test-bed was designed and implemented in FREEDM Systems Center's high voltage laboratory. The following subsections provide further details on the test-bed hardware and system specification, modeling and control system, and experimental results and system performance evaluation.

3.5.1 HFE Test-bed Topology and System Parameters

The single-line circuit diagram of the three-phase HFE test-bed is presented in Figure 84. The test-bed is established by a 12-pulse (12-p) thyristor-bridge and an IGBT-based AFE which share a common DC-bus and are connected in parallel at PCC. The 12-pulse thyristor-bridge, which serves as the main AC-DC power rectifier, is comprised of two 6-pulse (6-p) thyristor-bridges connected in parallel at input through phase shifting transformers to input reactance and PCC and connected in series at output to smoothing reactors and output capacitors. A 3-ph D-Y transformer connects the top 6-p bridge to the same common point of connection to which a 3-ph D-D transformer connects the bottom 6-p bridge. Each input transformer is rated at 6 kVA and thus the whole system is rated at 12 kVA. Since the input transformers' series reactance is small, an extra line reactance, i.e., X_{in} (~ 10% P.U.) can be inserted per phase between PCC and the input of transformers to emulate higher input inductance condition. At the DC-bus, the filtered output of 12-p bridge is connected to DC-link of active power filter inverter, DC electronic load (DCEL) and resistive load bank. The resistive load bank is used for continuous high-power loading condition and DCEL is

intended for dynamic loading conditions. The AFE, in the hybrid configuration, is a 3-phase, 2-level, IGBT-based inverter which shares the same DC-bus as with 12-p bridge, as depicted in Figure 84. It connects to PCC through inverter inductor, i.e., X_{f1} , shunt impedance, i.e., Z_{sh} , and buffer inductor, i.e., X_{f2} . The active power filter injects harmonic currents and reactive power at the PCC of thyristor rectifier and AC source. Table 26 presents the system parameters for HFE test-bed. Figure 85 shows the 12-kVA, 550-VDC HFE test-bed system designed and built at NSF FREEDM Systems Center.

Table 26 HFE test-bed system parameters

Rated power	$S_b = 12 \text{ kVA}$
3-ph Input voltage	$V_{in} = 208 \text{ VAC}/60 \text{ Hz}$
Output voltage	$V_{out} = 0 - 550 \text{ VDC}$
Operating output voltages	$V_{out} = 360, 450 \text{ VDC}$
Input transformers	T1 = 3-ph, D-Y $S_{T1} = 6 \text{ kVA}$ $X_{T1} = 1.13\% \text{ P.U.}$ $N_{T1} = 1.07$
	T2 = 3-ph, D-D $S_{T2} = 6 \text{ kVA}$ $X_{T2} = 1\% \text{ P.U.}$ $N_{T2} = 1.03$
Input reactor	$X_{in} = 10.5\% \text{ P.U.}$
Output reactor	$L_d = 4.25 \text{ mH} (44.5\% \text{ P.U.})$
Output capacitor	$C_d = 3300 \text{ uF}$ Al-electrolytic parallel with 4 uF MKP film cap.
DC Electronic Load	$V_{DC} = 500 \text{ V}$ $P_{rated} = 4.5 \text{ kW}$ programmable
Inverter inductor	$X_{f1} = 2\% \text{ P.U.}$
Buffer inductor	$X_{f2} = 0.94\% \text{ P.U.}$
Inverter switching frequency	$f_{sw} = 20.9 \text{ kHz}$

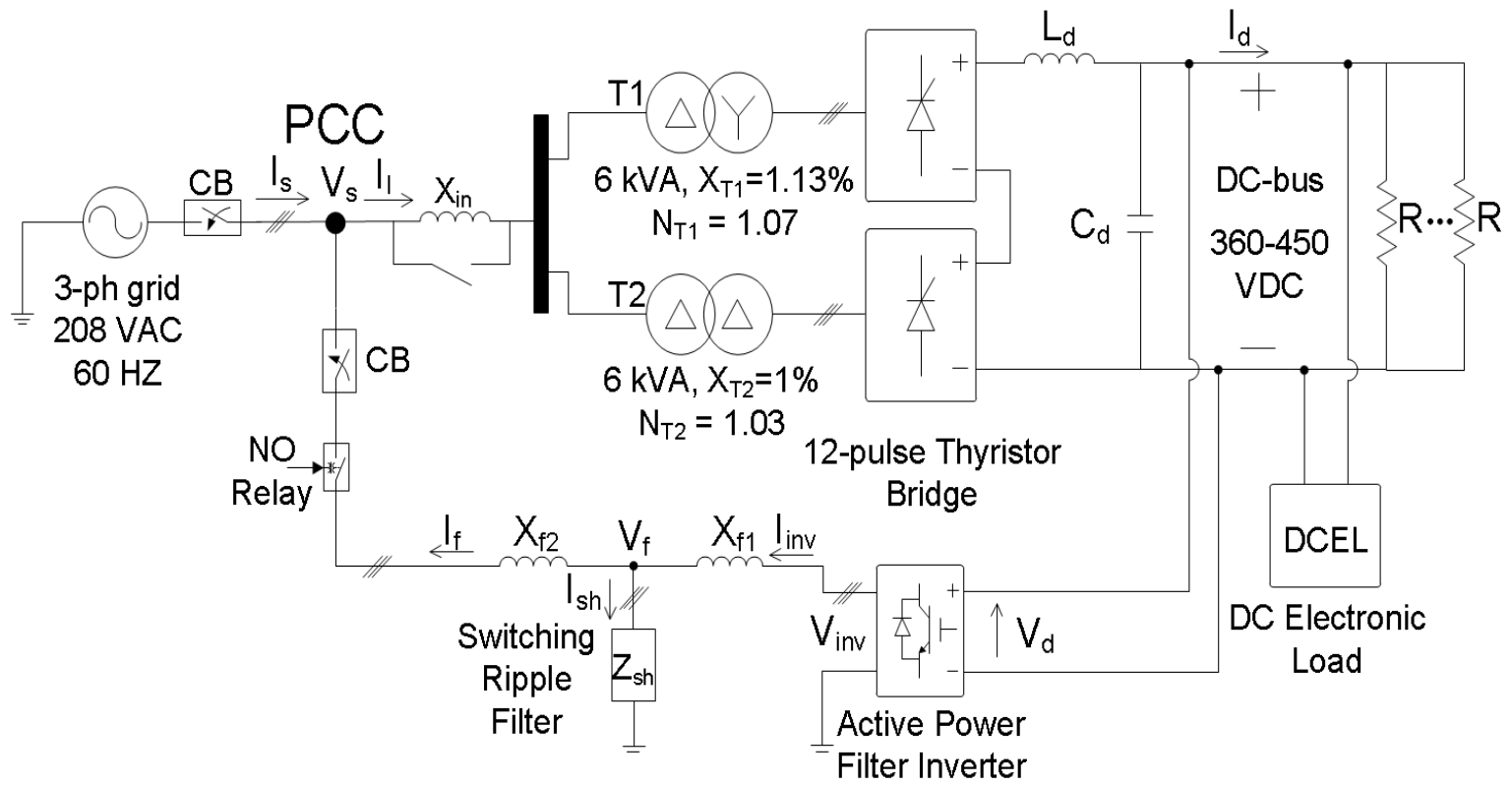
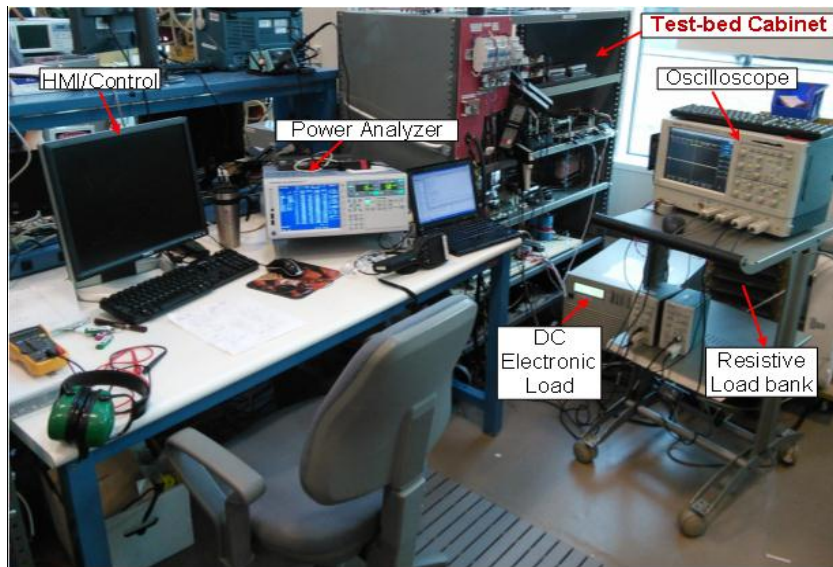
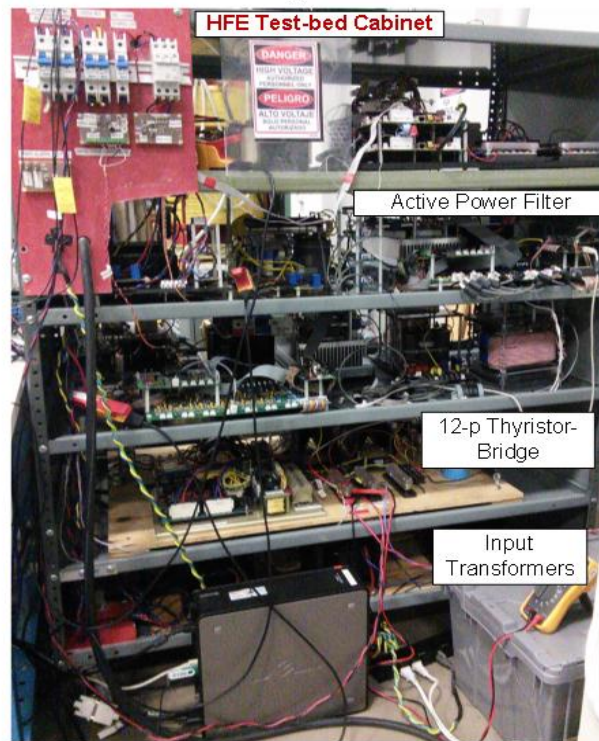


Figure 84 Single-line circuit diagram of the three-phase HFE test-bed.



(a)



(b)

Figure 85 12-kVA, 550-VDC HFE test-bed at FREEDM Systems Center. (a) complete system setup. (b) main power circuit components inside the test-bed cabinet.

3.5.2 Inverter Switching Ripple Filter Analysis

The active filter is a basic, full-bridge, IGBT-based inverter. As it is shown in Figure 84, it connects to PCC through X_{f1} , inverter inductor, Z_{sh} , shunt ripple filter, and X_{f2} , buffer inductor. X_{f1} and Z_{sh} work together to significantly reduce converter switching ripple resulting from pulse-width-modulated (PWM) output voltage of inverter, and X_{f2} (~50% of X_{f1}) serves as buffer inductor needed to provide the active filter voltage feedback signal, i.e., V_f . This feedback signal is necessary for proper synchronization of active filter to grid voltage because a simple voltage feed-forward is not enough and results in an active filter output voltage at a slight phase lag with respect to PCC voltage as it will be shown later.

The ideal objective of switching ripple filter is to thoroughly cancel out switching noise while passing the harmonic frequencies of interest totally unaffected. When the frequency separation between the harmonic frequencies and switching noise is not large enough, switching ripple filter design to meet those objectives becomes especially challenging. Due to 12-pulse nature of thyristor-bridge, it normally produces harmonics at $12n\pm 1$ multiples of ac line frequency with n being a positive integer; however, because of unbalances present in the system, it also produces some amount of harmonics at $6n\pm 1$ multiples of line frequency. The active filter inverter's switching frequency is 20.88 kHz and harmonic orders of 11th, 13th, 23rd and 25th effectively fall within the bandwidth of active filter. In order to have maximum attenuation at switching frequency while inflicting minimum phase delay on harmonics of interest, a "C-type" topology is chosen for Z_{sh} of switching ripple filter, as shown in Figure 86. Table 27 lists both calculated and field measured parameters for phase-a of 3-ph output switching filter designed and implemented for active power filter. A bode plot

of the calculated and measured shunt filter response with X_{f1} is shown below in Figure 87. Table 28 lists important points of magnitude and phase response in the bode plot. As it can be seen, the switching ripple filter attenuates switching noise by more than 36 dB (1.6% peak-to-peak ripple), whereas it barely amplifies the other important harmonics. However, it introduces a small amount of growing phase lag to the harmonics of interest which lie within active filter bandwidth. These phase lags have proven to negatively impact the harmonic compensation performance of active power filter. The larger the phase delay for a specific harmonic frequency, the worse the active filtering performance is for that harmonic.

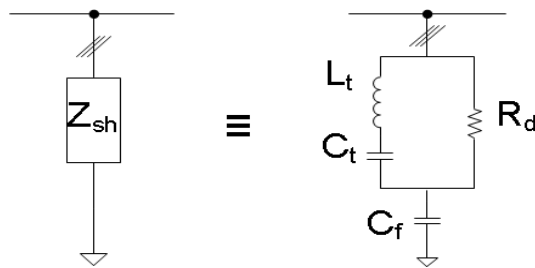


Figure 86 C-type filter topology for shunt branch of switching ripple filter.

Table 27 Phase-a parameters of the 3-ph output switching filter for active power filter

Impedance element	Parameter	Calculated	Measured
Inverter inductor	Lf1 (uH)	200	195.2
Shunt impedance	Ct (uF)	3	3
	Lt (uH)	25	25.34
	Rt (mΩ)	0	770
	Rd (Ω)	5	4
	Cf (uF)	10	8.16
Buffer inductor	Lf2 (uH)	86	88

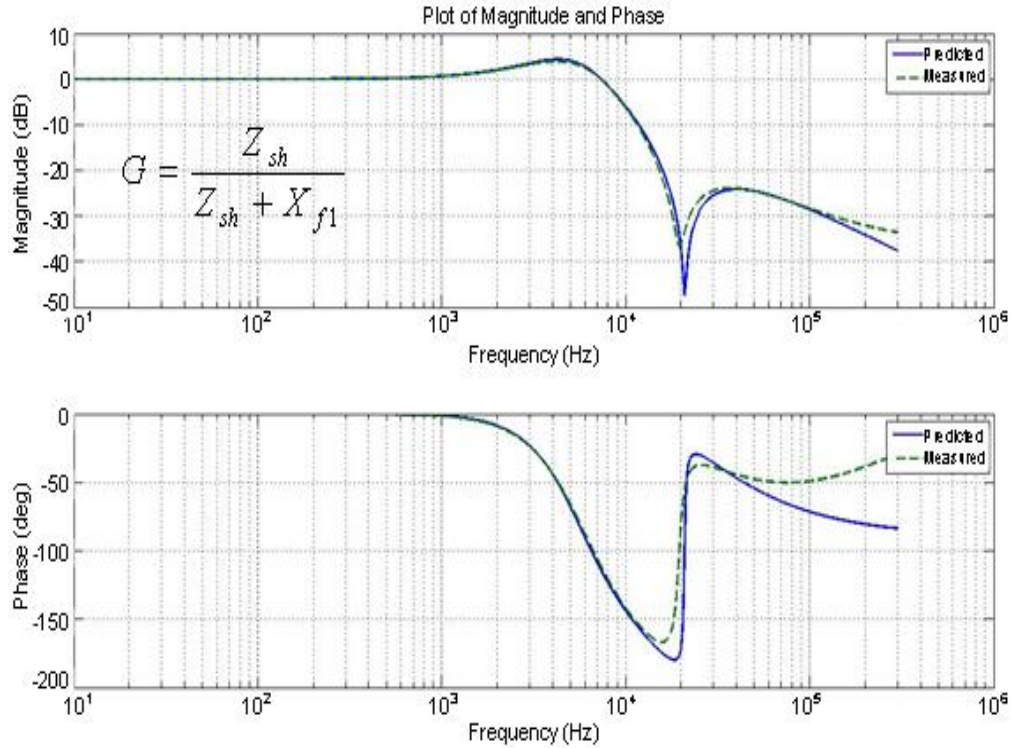


Figure 87 Predicted and measured frequency response of X_{f1} and Z_{sh} .

Table 28 Important points of switching ripple filter bode plot

Frequency (Hz)	Harmonic Order (n)	Magnitude Gain (dB)	Phase (Degree)
60	1 (fundamental)	0.0000	-0.0177
660	11	0.2806	-0.6084
780	13	0.3866	-0.9011
1380	23	1.0838	-3.7181
1500	25	1.2443	-4.5760
20880	348 (switching Frequency)	-36.1350	-81.2727

3.5.3 The HFE Control System

The controller structure for the active power filter in hybrid front-end is presented in Figure 88. The control system is based on synchronous-reference-frame (SRF) [REF], in which three-phase sinusoidal ac currents and/or voltages are transformed, via amplitude-preserving park transformation (1-3), to dc quantities in rotating direct (d)-quadrature (q) frame synchronized to sinusoidal PCC phase voltage by an enhanced phase-locked-loop (PLL) [REF]. Since in this control scheme the PLL is sine-based and because of the transformation, the fundamental active component of load current corresponding to active power transfer appears as dc on q-axis, and the fundamental reactive component of load current corresponding to reactive power appears as dc on the d-axis in Figure 88. In addition, harmonics currents of higher order than fundamental frequency also appear as higher frequency components on both d- and q-axes after the transformation. The SRF d-q quantities are then transformed back to stationary α - β frame, via dq-to- $\alpha\beta$ transformation (2-3), before going to the modulator.

$$\begin{bmatrix} d \\ q \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\omega t) & \cos\left(\omega t - \frac{2\pi}{3}\right) & \cos\left(\omega t + \frac{2\pi}{3}\right) \\ \sin(\omega t) & \sin\left(\omega t - \frac{2\pi}{3}\right) & \sin\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix} * \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad (1-3)$$

$$\begin{bmatrix} \alpha \\ \beta \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & \sin(\omega t) \\ -\sin(\omega t) & \cos(\omega t) \end{bmatrix} * \begin{bmatrix} d \\ q \end{bmatrix} \quad (2-3)$$

The control system is comprised of a proportional (p)-controlled current compensator and voltage compensator which together produce the reference stationary voltage vector, i.e., $V_{ref-\alpha\beta}$, to the space-vector pulse-width-modulator (SV-PWM) for producing switching commands to active filter inverter. The current compensator is based on load (thyristor-

bridge) harmonic current extraction and has two modes, ‘harmonics only’ and ‘harmonics & VAR support’, each of which are chosen by properly positioning a selector switch in the control system, as shown in Figure 88. In the harmonics only mode, the selector switch is positioned to 0 and harmonic content of load current is only extracted by just filtering the dc values on both d-axis and q-axis using high-pass filters (HPF) with very low cut-off frequency compared to first major load harmonic component. In the harmonics and VAR support mode, the selector switch is positioned to 1 which only changes control configuration on d-axis compared to harmonic only mode, to add a proportional gain, i.e., K_Q , to extracted dc component for providing VAR support in the HFE system. A simple proportional gain controller, i.e., K_p , controls the overall performance of the current compensator.

In the voltage compensation section of SRF controller, a simple feed-forward of the exact PCC voltages in stationary α - β frame assures that there is no undesired active power flow through the active filter path to shared DC-bus of hybrid front-end system. However, due to non-idealities present in the system such as converter losses, passive component losses and different phase delays, it is observed that the voltage produced at the output of active filter departs from PCC voltage causing undesired active power flow during steady-state and severe transients especially during system start-up. The latter is important during grid synchronization phase of HFE start-up where large transients could force the active filter converter to trip in overcurrent protection. Thus, a voltage correction feedback term represented by proportional gains K_{vd} and K_{vq} , is added in the voltage control loop to compensate for the phase mismatch between PCC voltage and active filter voltage. Figure 89 shows the phase lag between these voltages before and after implementation of feedback

correction term. As it can be seen from Figure 89a, with only voltage feed-forward control, the active filter voltage lags the PCC voltage by $252 \mu\text{s}$ or 5.5° , whereas with feed-forward augmented with feedback correction terms, tight voltages' zero-crossing with almost no phase lag is achieved, as it can be seen in Figure 89b.

The control system is implemented in TI's TMS320F28335 32-bit floating-point digital signal processor (DSP) with maximum clocking frequency of 150 MHz or clock period of 6.67 nS. The control loop is sampled every $T_s = 35.0877 \mu\text{s}$ time interval at a frequency of $f_s = 28.5 \text{ kHz}$. The sampling frequency corresponds to 475 samples or 0.477° resolution per 60-Hz ac line cycle. At the beginning of each control sampling period, a software command starts the analog-to-digital (ADC) conversion process. The 12-bit ADC converter in the DSP has 16 channels out of which 9 channels are utilized – only 2 channels for each three-phase measurement in Figure 88 because of the three-wire system and 1 channel for common dc-bus voltage measurement. The ADC which runs at 12.5 MHz maximum clock frequency has only two sample-and-hold (S/H) units that are utilized to synchronously – simultaneously – sample each pair of two analog channels in two ADC clock periods and in the same sequential order as displayed in Figure 88. Due to this physical limitation, an unavoidable phase delay/lag error occurs between the first sampled-pair and the last sampled-pair which decreases the maximum frequency that could be sampled without error. In order to reduce the impact from sampling phase lag, signals with high frequency harmonic content such as load currents and active filter currents are prioritized first and grouped together in the sampling sequence of ADC and voltage signals are sequenced afterwards.

Several types of digital filters are employed in the control algorithm for signal processing and filtering purposes. Low-pass filters (LPF) effectively are used to reject remaining high frequency noise on measurement signals inside controller; DC removal filters are used to effectively cancel out any remaining DC offset in the measurement signals resulting from signal conditioning board; and HPF and/or LPF filters are used to extract harmonic and/or fundamental frequency. Since the control sampling frequency is $f_s = 28.5$ kHz, the highest frequency in the discrete-domain signals is practically limited to Nyquist frequency $f_{nyq} = f_s/2 = 14.25$ kHz. Consequently, all filters' cut-off frequency, i.e., f_c , must be less than f_{nyq} and filters' magnitude response should be ideally zero beyond Nyquist frequency.

First- and second-order low-pass infinite-impulse-response (IIR) Butterworth digital filters are designed for LPFs. Discrete-domain Butterworth filters are advantageous because of their nearly flat frequency magnitude response in pass-band, high attenuation in stop-band, sharp transition period, and zero magnitude response beyond f_{nyq} . The higher the order of Butterworth filter, the better the magnitude response is; however, the higher the phase delay of filter is.

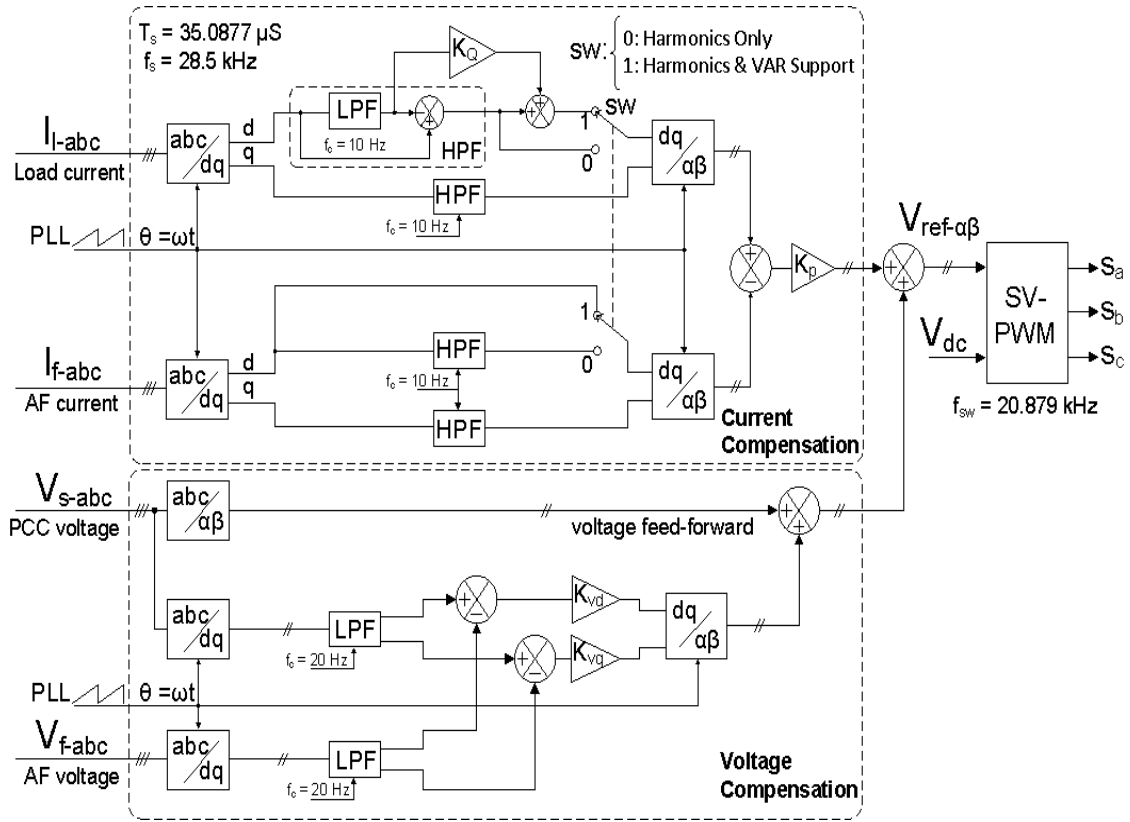


Figure 88 Synchronous-reference-frame (SRF) control system for active filter in hybrid front-end.

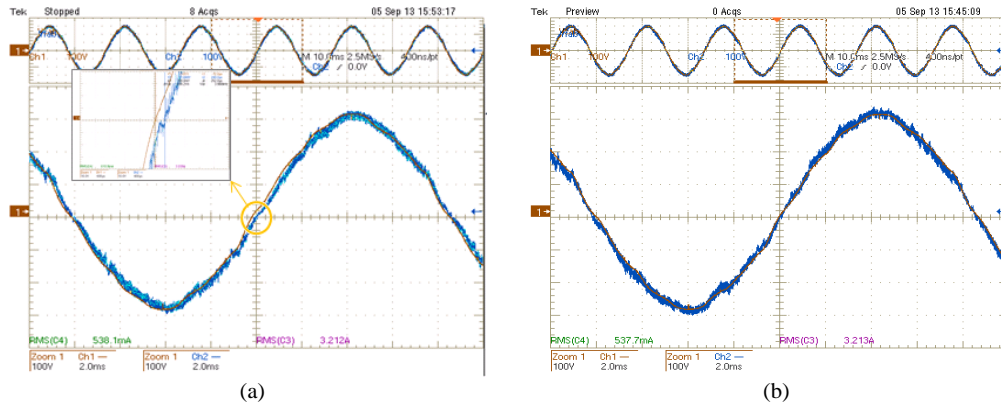


Figure 89 Phase lag between PCC and active filter line voltage, Ch1 (brown) is PCC voltage and Ch2 (blue) is active filter voltage. (a) with only voltage feed-forward (b) with feed-forward and feedback voltage correction.

Figure 90a shows frequency magnitude and phase response of 1st- and 2nd-order discrete Butterworth filter with $f_c = 13$ kHz, and Figure 90b shows the blown up phase response which is highlighted at some harmonic frequencies of interest. As it can be seen in Figure 90a, 2nd-order Butterworth filter has a better magnitude response than 1st-order Butterworth; however, 2nd-order Butterworth filter also has a higher phase delay than the latter. This fact is better demonstrated in Figure 90b where phase delay of the 2nd-order filter grows faster at increasing highlighted harmonic frequencies. These types of phase delay which are unavoidable due to digital filter implementation and limited sampling frequency, negatively impact harmonic compensation performance of active filter. Consequently, for noise filters on measurements with $f_c = 13$ kHz, 1st-order Butterworth LPFs are, and only for main control loop filters, 2nd-order HPF Butterworth filters with $f_c = 10$ Hz or 20 Hz are applied. Butterworth HPF filter is obtained by subtracting the corresponding LPF-filtered signal from whole signal, as depicted in Figure 88. Figure 91a and Figure 91b show the frequency magnitude and phase response of both 1st-order and 2nd-order HPF Butterworth with $f_c = 10$ Hz for harmonic extraction in controller. As it can be seen from Figure 91b, 1st-order Butterworth HPF has considerable phase lead at harmonic frequencies of interest, whereas 2nd-order Butterworth HPF has zero phase lead. Thus, 2nd-order Butterworth HPF is used for harmonic extraction in the control system.

The general discrete (z-domain) transfer function of digital filter is given in (3-3), where numerator and denominator coefficients are given by row matrices B and A , as in (4-3) and (5-3), respectively; and in all which n represents the order of discrete filter. Table 29 summarizes specifications of filters used in the control system.

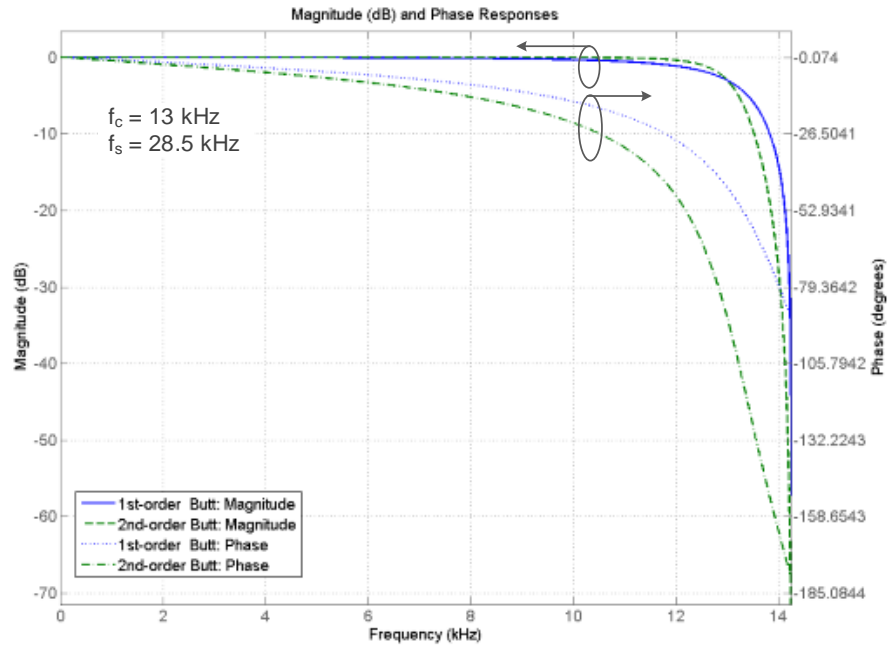
$$\frac{Y(z)}{X(z)} = \frac{b_0 + b_1z^{-1} + \dots + b_nz^n}{1 - a_1z^{-1} - \dots - a_nz^n} \quad (3-3)$$

$$B = [b_0, b_1, \dots, b_n] \quad \text{numerator coefficients} \quad (4-3)$$

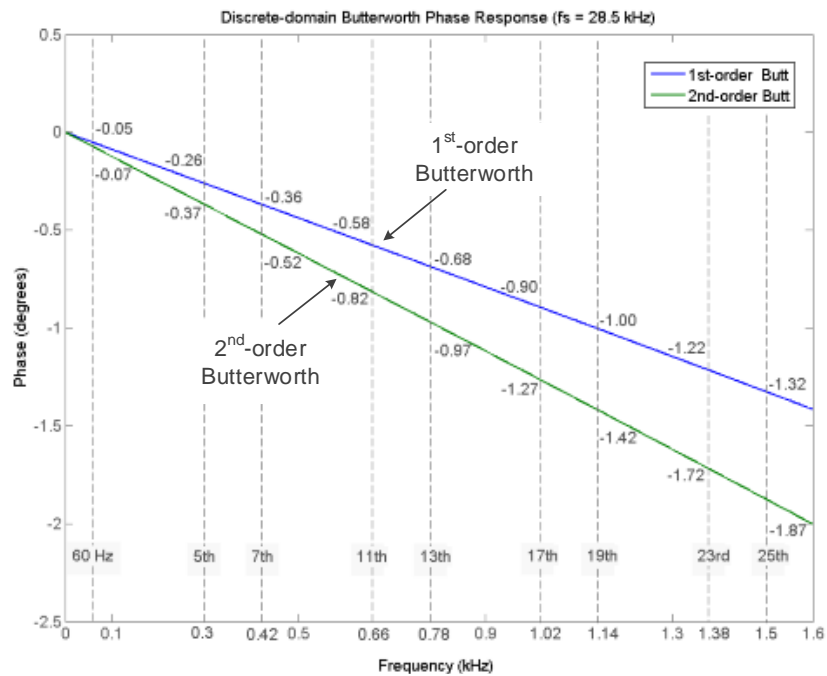
$$A = [1, -a_1, \dots, -a_n] \quad \text{denominator coefficients} \quad (5-3)$$

Table 29 Specification of discrete-time IIR filters used in control system

Type	Application	Cut-off freq. (fc) and sampling freq. (fs)	Filter coefficients – B (numerator) & A (denominator)	Filter structure	Implementation cost
1 st -order Butterworth LPF	Noise filtering	fc = 13 kHz; fs = 28.5 kHz;	B = [0.878218, 0.878218]; A = [1, 0.756437];	Direct-Form II Transposed	3 multiplier 2 adders 1 state
2 nd -order Butterworth LPF	Harmonic extraction – current control loop	fc = 10 Hz; fs = 28.5 kHz;	B = [0.00000121, 0.00000242, 0.00000121]; A = [1, -1.99688219, 0.99688704];		5 multipliers 4 adders 2 states
	Harmonic extraction – voltage control loop	fc = 20 Hz; fs = 28.5 kHz;	B = [0.00000484, 0.00000969, 0.00000484]; A = [1, -1.99376439, 0.99378377];		

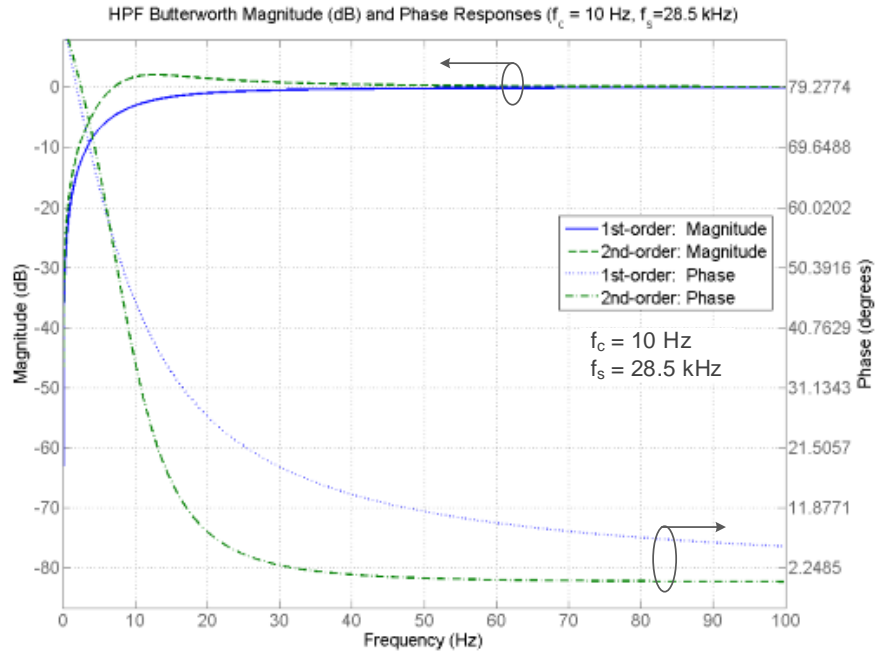


(a)

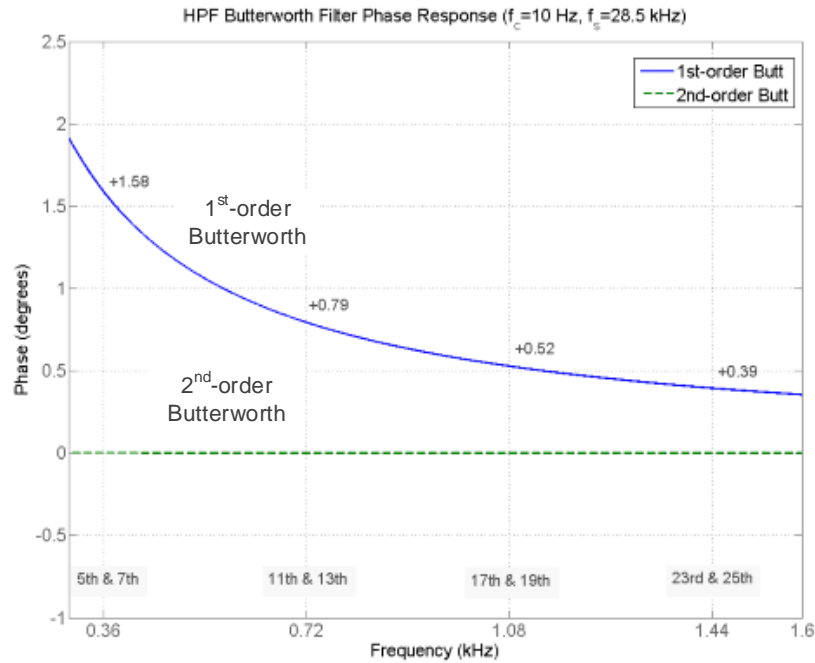


(b)

Figure 90 Frequency response of 1st- and 2nd-order discrete-domain low-pass Butterworth filter with $f_c = 13$ kHz and $f_s = 28.5$ kHz. (a) magnitude and phase response over $[0, f_s/2]$ frequency range (b) zoomed up and highlighted phase response at some harmonic frequencies of interest.



(a)



(b)

Figure 91 Frequency response of 1st-order and 2nd-order high-pass Butterworth filter with $f_c = 10 \text{ Hz}$ and $f_s = 28.5 \text{ kHz}$. (a) magnitude and phase response. (b) blown up phase response at harmonic frequencies of interest.

Figure 92 presents waveforms of some important quantities inside controller, with reference to control system diagram in Figure 88, when the system is only compensating for harmonic currents in ‘harmonics-only’ mode with $sw = 0$ and where harmonic compensation gain $K_p = 5$. The controller waveforms are recorded at nominal line-to-line input voltage $V_s = 208$ Vrms, load power factor $PF = 0.68$, output power $P_{out} = 1500$ W and dc-bus voltage $V_{dc} = 450$ V. The PLL is implemented on phase-a line-to-neutral voltage and is dead on sinusoidal voltage zero-crossing, as it is shown in Figure 92a. Figure 92b shows three-phase PCC voltages with 2.5% to 2.7% total harmonics distortion (THD), Figure 92c shows three-phase load currents with 25% THD.

The d-q rotating frame – synchronous frame – load currents are shown in Figure 92d, where active power appears as d-c value in q (ch2) component; reactive power appears as d-c value in d (ch1) component; and load harmonics appears as a-c component on both d and q components. In the harmonics only mode, d-c values are high-pass filtered which is demonstrated in Figure 92e. The filtered d-q current is transformed to stationary α - β frame from which the feedback filter current is subtracted and then multiplied with current compensation gain K_p to produce current reference in α - β frame, as shown in Figure 92f. The output of current and voltage control loops in α - β frame are added together to produce the final reference voltage to SV-PWM. Figure 92h shows α - β reference voltages along time-axis; and Figure 92g and Figure 92i show trajectory of PCC voltage vector and final reference voltage vector in stationary α - β frame, respectively.

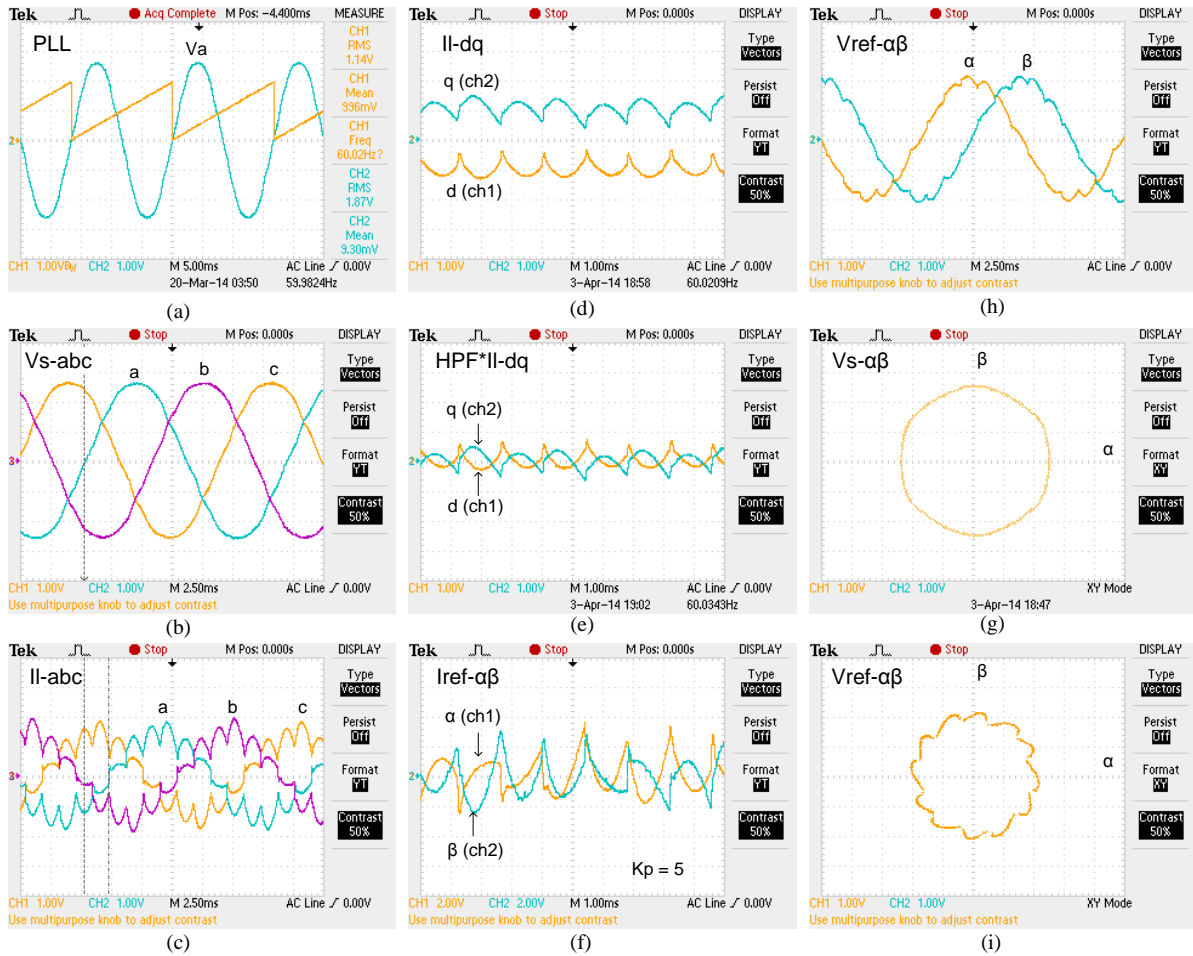


Figure 92 Controller waveforms in harmonics-only mode with $K_p = 5$. (a) PLL on phase a voltage. (b) 3-ph PCC voltage. (c) 3-ph load current. (d) d-q transformed load current. (e) HP filter d-q load currents. (f) α - β transformed reference current. (h) α - β transformed reference voltage. (g) PCC voltage in stationary α - β frame. (i) reference voltage in stationary α - β frame.

Figure 93 shows some important controller waveforms when the system is also providing reactive power support in ‘harmonics-and-VAR-support’ mode with $sw = 1$, where reactive power compensation gain $K_Q = 1$. In this mode, the d (ch1) component not only contains the high-pass filtered harmonics, but it also contains a proportionally-controlled d-c value for providing VAR support, as shown in Figure 93a. The α and β reference voltages are

shown in Figure 93b in which the α -component voltage zero crossing is compared against that of harmonics-only mode. Figure 93c shows stationary α - β frame voltage vector trajectories for both compensation modes, where the phase rotation due to addition of d-c component on rotating d-component for providing VAR support is demonstrated.

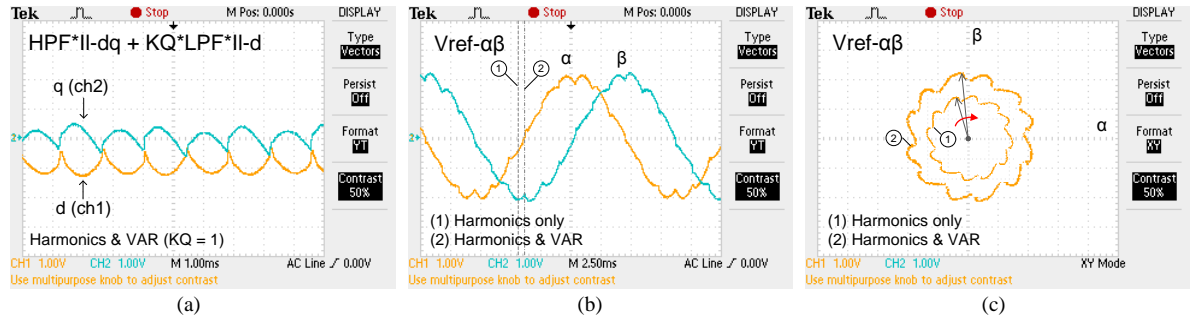


Figure 93 Controller waveforms in harmonics-and-VAR-support mode with $KQ = 1$. (a) HP filtered d-q load currents plus LP filtered d load current. (b) α - β transformed reference voltage compared against harmonics only mode. (c) reference voltage in stationary α - β frame compared versus harmonics-only mode.

3.5.4 The HFE equivalent circuit modeling

In order to better understand the HFE system, a modeling analysis based on single-phase equivalent circuit is performed. The single-phase equivalent circuit of HFE system is shown in Figure 94 where load is ideally modeled as a current source and active filter inverter as voltage source. The objective is to find how active filter current, i.e., I_f , influences source current, i.e., I_s , which is found by applying Kirchhoff's current law (KCL) at PCC to be:

$$I_s = I_l - I_f \quad (6-3)$$

where I_l is load current representing 12-p thyristor-bridge current. In (6-3), I_f needs to be found in terms of active filter reference current, i.e., I_f^* . For easier modeling analysis, inverter voltage, i.e., V_{inv} , inverter reactance, i.e., X_{f1} , and shunt ripple impedance, i.e., Z_{sh} , are replaced with their corresponding Thevenin equivalent circuit, as shown in Figure 95. The Thevenin voltage and impedance, i.e., V_{th} and Z_{th} , are defined as below:

$$V_{th} = G * V_{inv} \quad (7-3)$$

$$Z_{th} = G * X_{f1} \quad (8-3)$$

where G is the output filter transfer function plotted in Figure 87 and is defined as below:

$$G = \frac{Z_{sh}}{Z_{sh} + X_{f1}} \quad (9-3)$$

From Figure 95, the active filter current can be found as follows:

$$I_f = \frac{V_{th} - V_s}{Z_{eq}} \quad (10-3)$$

$$Z_{eq} = Z_{th} + X_{f2} \quad (11-3)$$

where V_s is PCC phase voltage, and Z_{eq} is the active filter equivalent impedance marked in Figure 95 and given in (11-3). Z_{eq} magnitude and phase frequency response is plotted in Figure 96. It can be seen that at 60 Hz the equivalent impedance is purely capacitive with relatively small dB magnitude of -19.4.

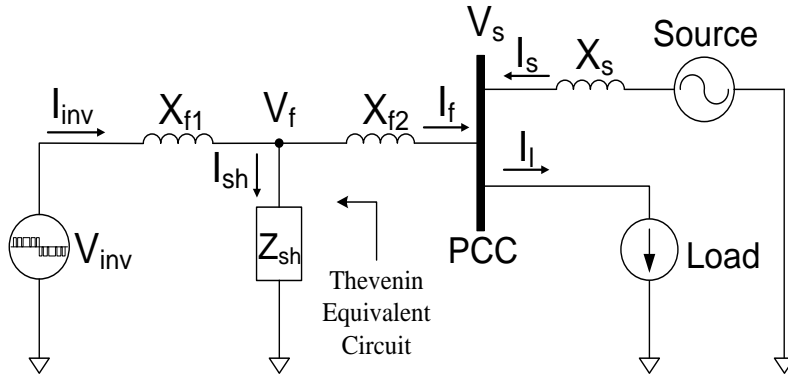


Figure 94 Single-phase equivalent circuit of HFE system.

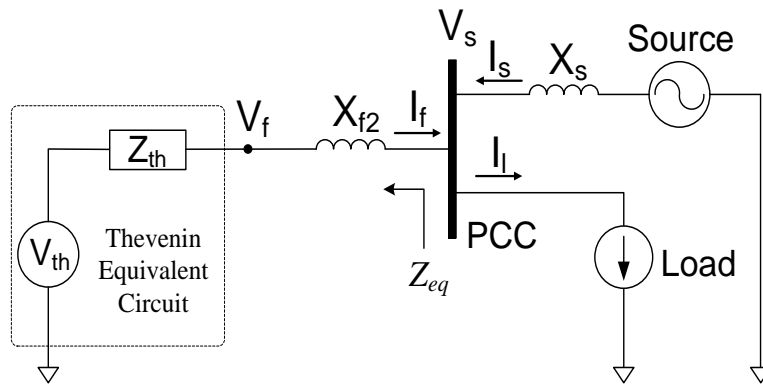


Figure 95 Single-phase Thevenin equivalent circuit of HFE system.

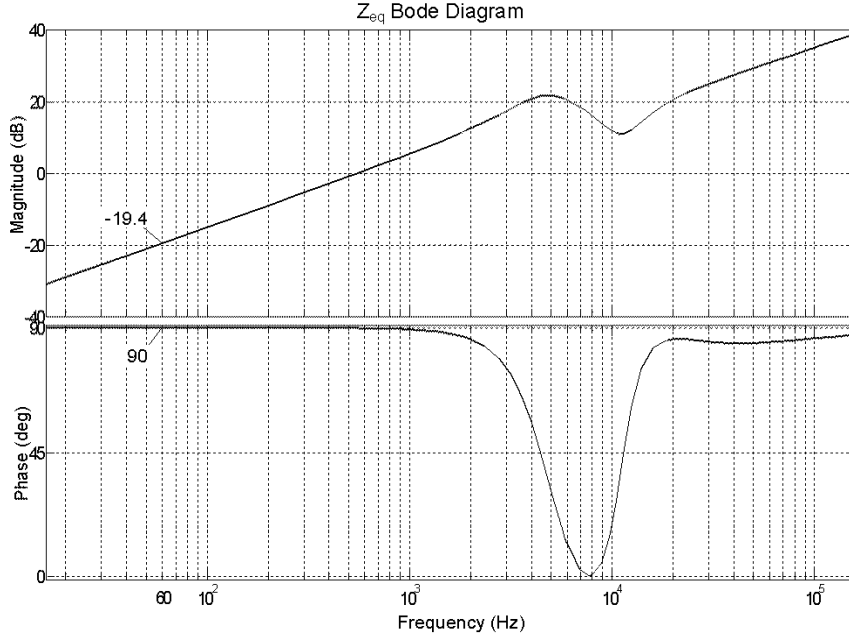


Figure 96 Magnitude and phase frequency response of Z_{eq} .

To further expand (10-3), V_{th} is expanded in terms of V_{inv} which is found from control system as follows:

$$V_{inv} = V_s + K_p \cdot (I_f^* - I_f) \quad (12-3)$$

where I_f^* is reference current command to current compensator in control system. Inserting in (10-3) from (7-3) and (12-3) and then simplifying, yields (13-3):

$$I_f = \frac{(G - 1)V_s}{Z_{eq} + GK_p} + \frac{GK_p}{Z_{eq} + GK_p} \cdot I_f^* \quad (13-3)$$

It can be seen from Figure 87 that at fundamental frequency $f_1 = 60$ Hz, $G = 1$ which then omits the first term in (13-3). However, at other non-fundamental harmonic frequencies $f_h \neq 60$ Hz, PCC voltage is approximately zero, i.e., $V_s \approx 0$. Thus, it can be well

approximated that the first term in (13-3) is always zero since the numerator is approximately zero at all frequencies, which reduces (13-3) to the following:

$$I_f = \frac{GK_p}{Z_{eq} + GK_p} \cdot I_f^* \quad (14-3)$$

Eqn. (14-3) is very important because it relates I_f to I_f^* , which on the other hand is related to load current, I_l . The load current can be decomposed to fundamental and harmonic components as follows:

$$I_l = I_{l1P} + I_{l1Q} + \sum_h I_{lh} \quad (15-3)$$

where I_{lh} is harmonic load current phasor; and I_{l1P} and I_{l1Q} are active and reactive fundamental load current phasors, respectively, which are defined as below:

$$I_{l1P} = \sqrt{2} \cdot \hat{I}_1 \cdot \cos(\alpha) \angle 0^\circ \quad (16-3)$$

$$I_{l1Q} = \sqrt{2} \cdot \hat{I}_1 \cdot \sin(\alpha) \angle -90^\circ \quad (17-3)$$

$$\hat{I}_1 = \frac{6}{\pi} \sqrt{\frac{2}{3}} \cdot I_{d-12p} \quad (18-3)$$

where \hat{I}_1 is peak fundamental current; I_{d-12p} is d-c load (12-pulse bridge) current; and α is firing angle (phase delay) of 12-pulse Thyristor-bridge. The harmonics in (15-3) ideally should occur at $(12k \pm 1)$ non-zero integer multiples of a-c line frequency; however, due to presence of unbalances in three-phase input voltage and input transformer, some amount of harmonics also occur at $(6k \pm 1)$ non-zero integer multiples of line frequency.

1. *The harmonics-only (Ih-only) mode*

When the active filter is only compensating for harmonic content of load, the active filter reference current is:

$$I_f^* = \sum_h I_{lh} \quad (19-3)$$

From (6-3), (14-3) and (19-3), the ratio of source harmonic current content to load harmonic current is obtained as below:

$$\frac{I_{sh}}{I_{lh}} = \frac{Z_{eq}}{Z_{eq} + GK_p} = G_h(s) \quad (20-3)$$

where $G_h(s)$ is defined as harmonic compensation transfer function. In (20-3), current compensator gain K_p is the enforcing factor in reducing source current harmonics. As K_p approaches infinity, source current harmonics reduce to zero as it is shown in (21-3):

$$\lim_{K_p \rightarrow \infty} \left(G_h(s) = \frac{Z_{eq}}{Z_{eq} + GK_p} \right) = 0 \rightarrow \lim_{K_p \rightarrow \infty} (I_{sh}) = 0 \quad (21-3)$$

From (21-3), it is implied that the active filter will compensate the harmonic current of the load completely. However, due to practical limitations, the active filter saturates well before K_p gets to infinity. In fact, experimental results suggest that K_p saturates around 6. Figure 97 shows frequency magnitude response plots of harmonic compensation transfer function $G_h(s)$ for $K_p = 1, 3, 6$. As it can be seen from Figure 97a, both dB harmonic attenuation at a specific frequency and compensation range increase with increasing K_p ; however, a maximum 50% attenuation limit is reached at around 2.2 kHz frequency with

$K_p = 6$. The change in absolute magnitude attenuation with K_p at $h = 5^{\text{th}}, 7^{\text{th}}, 11^{\text{th}}, 13^{\text{th}} \dots$ harmonics of a-c line frequency is shown in Figure 97b.

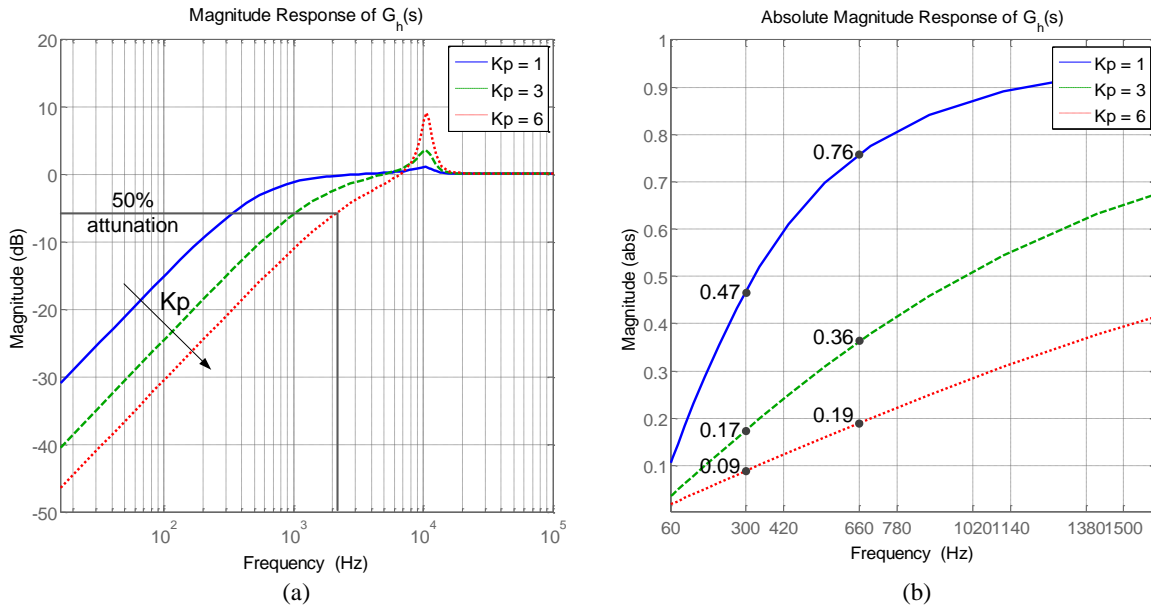


Figure 97 Frequency magnitude response plot of harmonic compensation transfer function $G_h(s)$ at $K_p = 1, 3, 6$. (a) dB magnitude response with increasing K_p . (b) zoomed-in absolute magnitude response at critical harmonic frequencies with $h = 5, 7, 11, 13, 17, 19, 23, 25$.

II. The harmonics-and-VAR-support (Ih&VAR) mode

When the active filter is compensating for both harmonic and fundamental reactive load currents, the active filter reference current is:

$$I_f^* = K_Q \cdot I_{l1Q} + \sum_h I_{lh} \quad (22-3)$$

From (6-3), (14-3) and (22-3), source current can be written as:

$$I_s = I_{l1P} + G_Q(s)I_{l1Q} + G_h(s) \sum_h I_{lh} \quad (22-3)$$

where $G_h(s)$ is harmonic compensation transfer function as in (20-3); and $G_Q(s)$ is the reactive power compensation transfer function as follows:

$$G_Q(s) = \frac{Z_{eq} + (1 - K_Q)K_p G}{Z_{eq} + K_p G} \quad (23-3)$$

Since only fundamental reactive power is concerned, (23-3) only needs to be evaluated at fundamental frequency $f_1 = 60$ Hz. Moreover, it is known that (23-3) is a complex quantity; and since I_{l1Q} as fundamental load reactive current is pure imaginary, only the real part of (23-3), i.e., $Re(G_Q(s))$, influences source reactive current. On the other hand, the imaginary part of (23-3), i.e., $Im(G_Q(s))$, changes the fundamental active current. Thus, from (17-3) and (22-3), fundamental component of (22-3) can be written as:

$$I_{s1} = I_{l1P} + A \cdot |I_{l1Q}| - jB \cdot |I_{l1Q}|$$

$$A = \text{Im} \left(G_Q(s) \right) \Big|_{s=j2\pi \cdot 60} \quad (24-3)$$

$$B = \text{Re} \left(G_Q(s) \right) \Big|_{s=j2\pi \cdot 60}$$

Furthermore, (24-3) can be written in terms of source complex power and load (12-pulse Thyristor-bridge) active and reactive powers as in the following:

$$S_{1s} = P_l + A \cdot Q_l - jB \cdot Q_l$$

$$P_l = V_{di} I_{d-12p} \cdot \cos(\alpha)$$

$$Q_l = V_{di} I_{d-12p} \cdot \sin(\alpha) \quad (25-3)$$

$$V_{di} = \frac{6}{\pi} \cdot V_{sll-pk}$$

where P_l is fundamental load (12-pulse bridge) active power; Q_l is fundamental load reactive power; V_{di} is the maximum uncontrolled voltage of 12-pulse bridge; and V_{sll-pk} is peak value of line-to-line source voltage. Imaginary and real parts of G_Q , A and B as in (24-3), are plotted with respect to K_Q for different values of K_p in Figure 98a and Figure 98b, respectively. As it can be seen, magnitude of A increases with K_Q , whereas magnitude of B decreases with K_Q . Moreover, for the same values of K_Q , increasing K_p greatly decreases magnitude of A , whereas it almost doesn't change magnitude of B . The experimental results, though, have shown a much greater degree of dependency of B on current compensation gain K_p , with higher values of K_p producing larger VAR support.

As it can be seen in (25-3), decreasing magnitude of B decreases lagging reactive power at PCC; and decreasing magnitude of A reduces fundamental active power flow through active filter path. In fact, Figure 98a shows for $K_Q = 1$, magnitude of B is zero for high values of K_p and nearly zero for other values which implies unity power factor operation of HFE system. Figure 99 shows the per unit change in active filter VAR support, fundamental apparent power and displacement (fundamental) PF with respect to K_Q , where the system is initially operating at $S = 0.3$ P.U. and $K_p = 6$. It can be seen from Figure 99 that for values of K_Q less than 1, DPF is lagging; and for values of K_Q greater than 1, DPF is leading. It should be noted, though, that reactive power compensation only takes place in harmonics-and-VAR-support; and as such, it is bound by the saturation limits of the system. Additionally, it is very important to bear in mind that true PF (fraction of active power over total apparent power) is also proportional to distortion factor (DF); and it is equal to DPF only when $DF = 1$ – or when THD is 0; and it is smaller than DPF in all other cases, depending on degree of harmonic compensation and whether or not saturation limits of the system are reached.

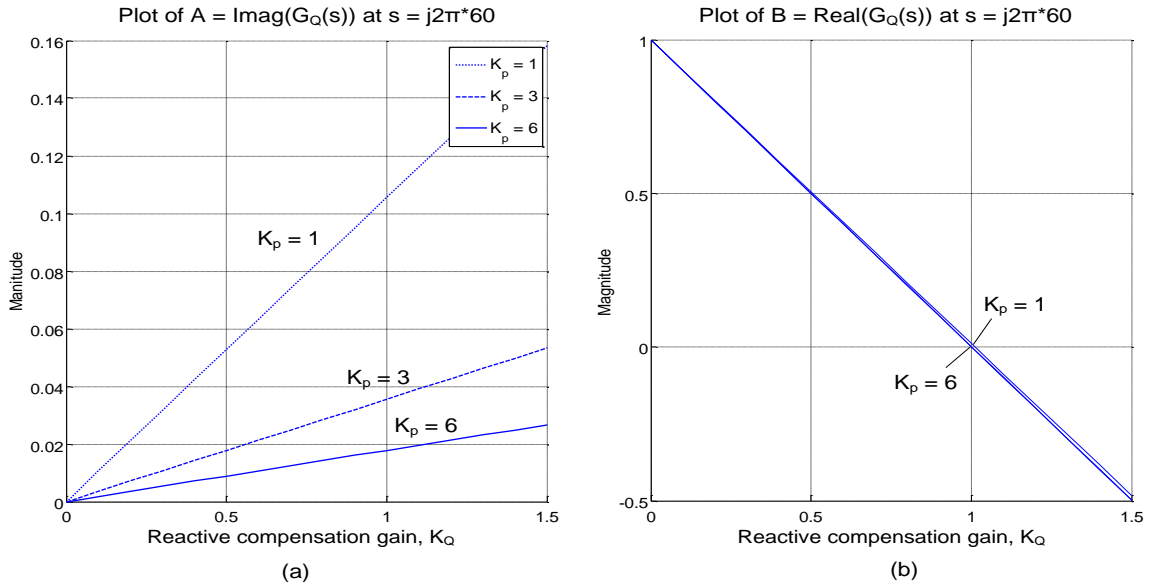


Figure 98 Magnitude plot of real and imaginary parts of reactive compensation transfer function $G_Q(s)$ at $s = j2\pi \cdot 60$ with respect to reactive compensation gain K_Q . (a) $A = \text{Imag}(G_Q(s))$. (b) $B = \text{Real}(G_Q(s))$.

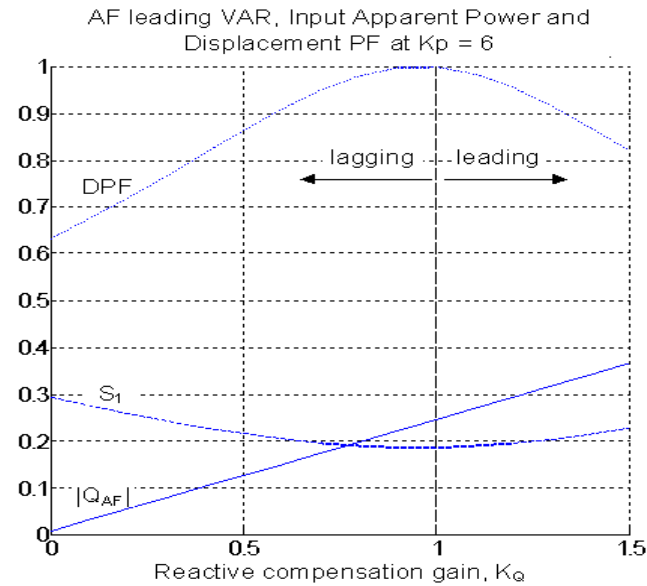


Figure 99 Per unit active filter leading VAR, per unit fundamental apparent power and displacement power factor change with respect to reactive compensation gain K_Q at $K_p = 6$.

3.5.5 Load characteristic and DC-link Voltage of Active Filter

In order to better define the limitations of the active filter for HFE system, the harmonic current of the load is investigated. In particular, it is desired to see di/dt of the harmonic current for the worst case. This occurs at lower load situations as load current approaches discontinuity. From this analysis, the required DC-link voltage of active filter – and thus DC-bus voltage of HFE system – can be estimated. From Figure 94, it is assumed that source impedance is comparatively high with respect to active filter path impedance; and therefore, all harmonic content of load current is supplied by active filter. Consequently, the output voltage of inverter is approximately equal to sum of voltage drops across reactances, X_{f1} and X_{f2} effectively in series, and PCC voltage, V_s . Two cycles of load harmonic current at 662-W output power that are extracted by the controller are shown in Figure 100. The maximum di/dt of this reference current is 83234 amps/second. Computing the voltage across series inductors, this leads to a needed 24-V voltage difference that must be provided by active filter. If load harmonic current lags sinusoidal source voltage by 90° , the required maximum output voltage of inverter will be sum of worst-case reactance voltage drop and peak source voltage. Therefore, for 170 V peak fundamental source voltage in HFE test-bed, a total of 194 V is required at the output of inverter, whereas a DC-link voltage of 360 V only allows for 180 V. Although the aforementioned 90-degree phase shift is not usually the case, it is better to have DC-link voltage at least double the worst-case output voltage of inverter. A minimum DC-link voltage of 400 V meets this condition.

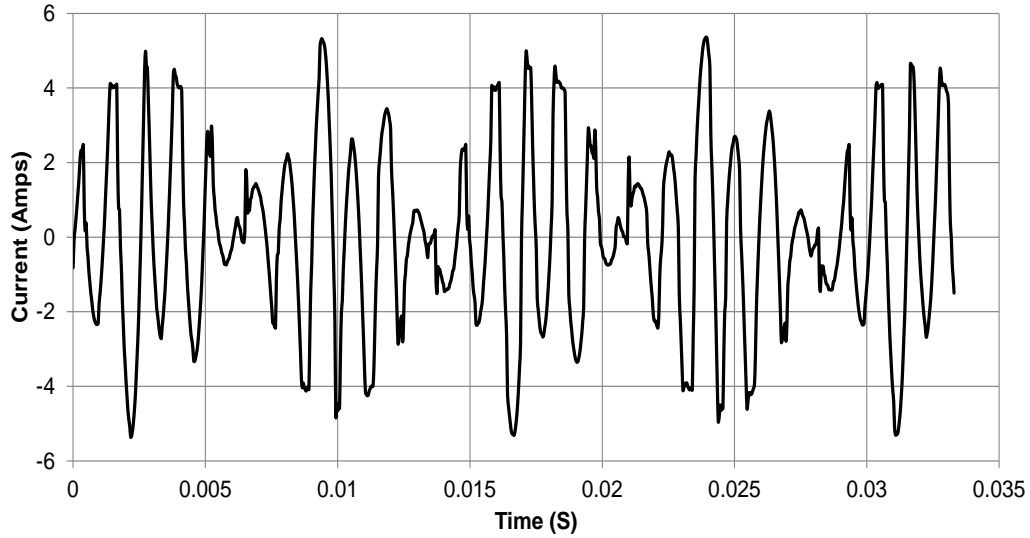


Figure 100 Extracted load harmonic current at 662 W.

3.6 Experimental results

The experiments were carried out on the 12-kVA, 550-VDC HFE test-bed, as shown in Figure 85, at different resistive load level. Initially, the tests were performed at output DC-bus voltage of 360 V and with no external line reactance at the input side ($X_{in} = 0$ in Figure 84). This was due to safety considerations as all the experiments were done while the HFE system was on-line and connected to the three-phase power grid. Thus, many of system operational characteristic analysis was originally performed at 360 VDC. However, after confidence was gained in the system, the operating DC-bus voltage was raised to 450 VDC. Furthermore, with the acquisition of 1 mH power inductors, the external line reactance of the HFE system was increased to more than 10% ($X_{in} = 10\%$ in Figure 84) which, though, still not high enough, it more closely emulates the real situation of total input line reactance in

front-ends for high power mobile mining machines. For the loading conditions, a combination of resistive load bank and Chroma 63804 DC electronic/programmable load was utilized. Due to hardware limitations, the system could be tested only up to 70% (0.7 P.U.) of its nominal capacity. For comprehensive system power quality analysis, the WT3000 Yokogawa precision power analyzer was used.

3.6.1 Harmonics-only Compensation Mode

The results presented in this section are system waveforms that are captured in harmonics-only compensation mode under steady-state operating condition. The test conditions are summarized in Table 30. Figure 101 shows three-phase PCC phase (line-to-neutral) voltages together with dc-bus voltage, and Table 31 lists some important power quality indices three-phase PCC line voltages. As it can be seen, PCC voltages are unbalanced and have an average total harmonic distortion of 2.6%. Figure 102 shows source phase voltage and current of phase-a when only the 12-pulse bridge is operating. As it can be seen there is a phase lag between voltage and current which is due to time delayed firing of thyristors for regulating DC-bus at the reference value of 450V. The phase lag amounts for a lagging power factor of 0.7718. The FFT frequency spectrum of source current in 12-pulse thyristor-bridge operating mode is shown in Figure 103. As it can be observed at $S_{in} \approx 0.5 PU$, among major non-fundamental harmonic orders of 5, 7, 11, 13, 23 and 25, the 11th harmonic multiple of fundamental frequency is dominant with an amplitude of 2.11 A relative to 15.2 A fundamental current. This makes harmonic distortion factor of of 11th harmonic source current (ratio of harmonic current amplitude to fundamental current

amplitude), i.e., $I_{s11,df}$, equal to 13.9%. The harmonics in 12-pulse mode comprise a source current THD of 16.17%.

Table 30 Harmonics-only mode experiment test condition

Input line voltage	Vin (V)	215
Output DC voltage	Vdc (V)	450
Input line reactance	Xin (%)	10.5 %
Load resistance	RL (Ω)	53
Output power of 12-p bridge	Pout (W)	3976 (0.33 PU)
Input powers of 12-p bridge	Pin (W)	4369 (0.36 PU)
	Qin (Var)	3592 (0.3 PU)
	Sin (VA)	5655 (0.47 PU)
Power factor of 12-pulse bridge	PF	0.7718 lagging
Compensation mode	Harmonics-only	
Current compensation gain	Kp	1, 5

Table 31 PCC line voltages amplitude and harmonics distortion

Function	Element1 (VAC)	Element2 (VBC)	Element3 (VAB)
Urms (V)	216.08	215.38	215.08
U+peak (V)	312.75	311.59	311.67
U-peak (V)	-312.72	-311.64	-311.74
CFU	1.447	1.447	1.449
Uthd (%)	2.535	2.631	2.593

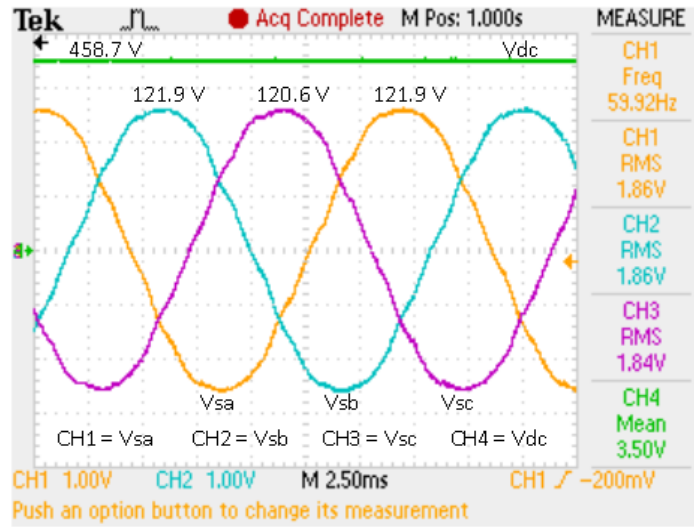


Figure 101 Three-phase input phase voltage and dc-bus voltage.

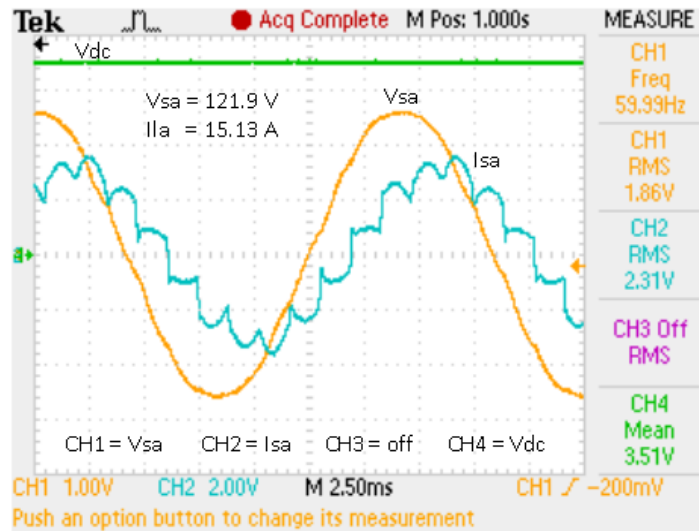


Figure 102 Source phase voltage and current of phase-a together with dc-bus voltage when only 12-pulse bridge is on.

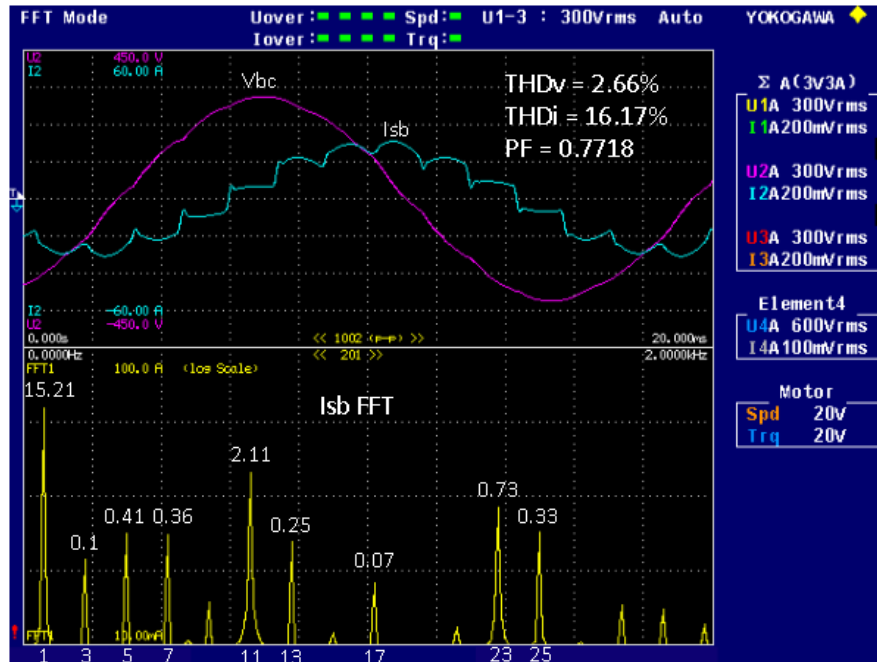


Figure 103 12-pulse thyristor-bridge mode - top plot shows phase-b source voltage and current and bottom plot shows source current FFT.

The input waveforms of HFE when it is operating in harmonics-only compensation mode with current compensation gain of $K_p = 1$, are shown in Figure 104 and Figure 105 for inside digital controller and actual field measurements, respectively. In these, source phase/line voltage, source current, load (12-pulse thyristor-bridge) current and active filter current are shown. The FFT of load current and active filter current in this mode is shown in Figure 106. The objective of active filter is to only compensate for harmonics and thus the fundamental component of its current is small and constitute only 6 % (0.86 A) of fundamental current. The load current harmonics in Figure 106 are mainly occurring at $12n \pm 1$ multiples of line frequency but due to presence of unbalance in the system, there are also some amount of harmonics at $6n \pm 1$ multiples of line frequency of which 5th and 7th

harmonic are really important. The frequency spectrum shows that active filter injects harmonics up to 49th order; however, the effective bandwidth of active filter is less than 2 kHz due to ~20 kHz switching frequency which makes up for ‘effective’ compensation up to 25th harmonic order. When $K_p = 1$, active filter injects only 87 % (0.36 A) of load current 5th-harmonic amplitude, only 16.3 % (0.33 A) of load current 11th-harmonic amplitude, only 12.8 % (0.09 A) of load current 23rd-harmonic amplitude. Important power quality information of HFE source, load, active filter and d-c currents are listed in Table 32. As it can be seen for $K_p = 1$, where active filter current THD is 78%, source current THD is reduced from 16.5 % of load to 13.6 % at HFE input.

Table 32 HFE input current amplitude and distortion in harmonics-only mode ($K_p = 1$)

Function	Element1 (Isb)	Element2 (Ilb)	Element3 (Ifb)	Element4 (Idc)
Irms (A)	15.05	14.41	1.11	8.81
I+peak (A)	23.54	22.56	2.22	8.86
I-peak (A)	-22.72	-22.56	-2.49	8.76
CFI	1.564	1.566	2.240	1.005
Ithd (%)	13.662	16.511	78.113	NAN
Idf (%)	99.07	98.66	78.80	NAN

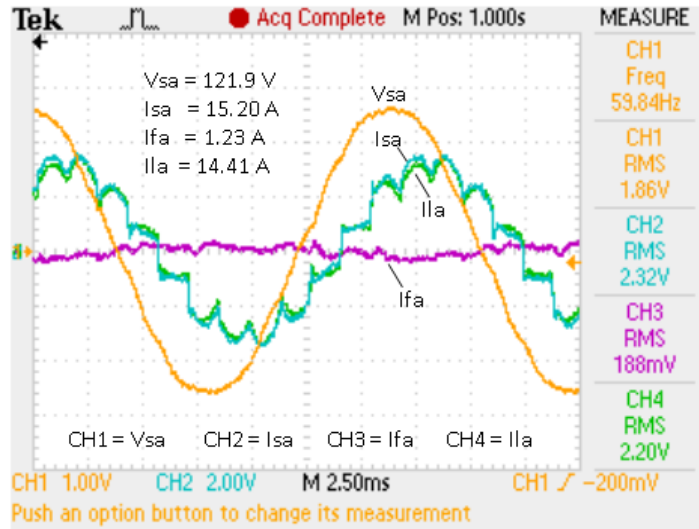


Figure 104 Source phase voltage, source current, load current and active filter current of phase-a when HFE is in harmonic-only compensation mode with $K_p = 1$.

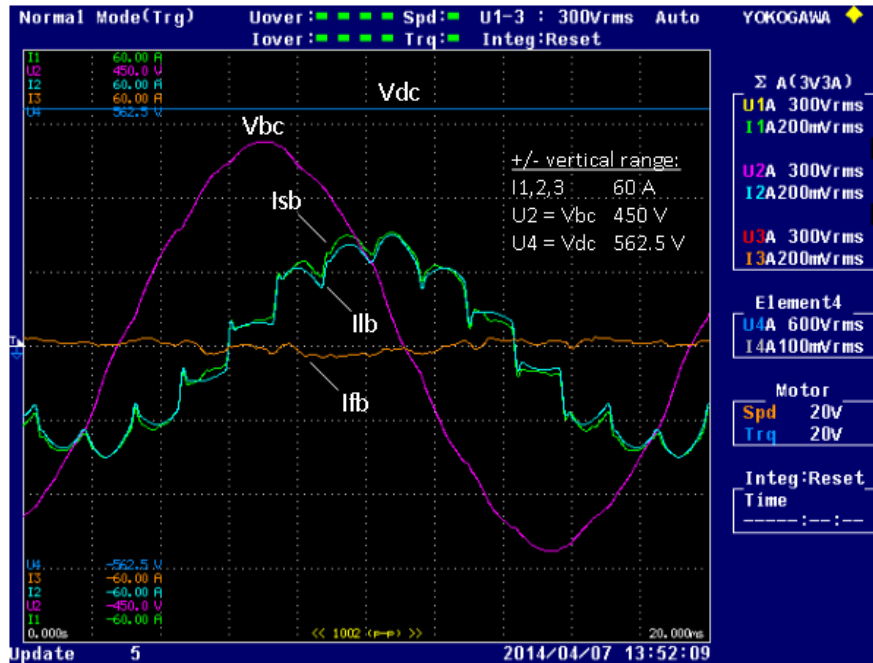


Figure 105 HFE waveforms when the system is operating in harmonisc-only compensation mode with $K_p = 1$.

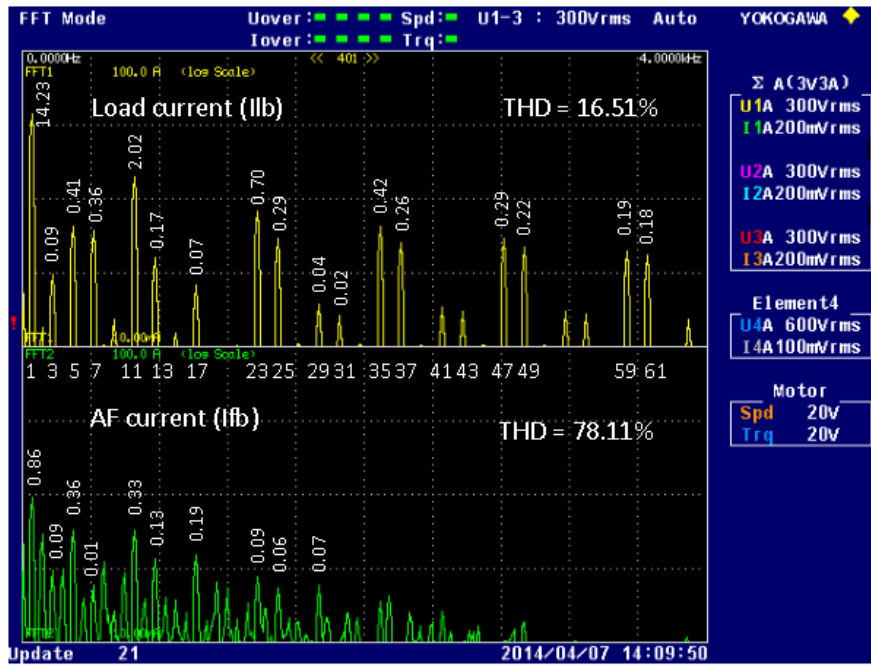


Figure 106 Phase-b load current and active filter current FFT in harmonics-only mode with $K_p = 1$.

The input waveforms of HFE when it is operating in harmonics-only compensation mode with current compensation gain of $K_p = 5$, are shown in Figure 107 and Figure 108 for inside digital controller and actual field measurements, respectively. The FFT of HFE load current and active filter current is shown in Figure 109. As it can be seen the increase in K_p from 1 to 5, not only increases the amplitude of characteristic harmonics injected by active filter, but it also increases the frequency band of harmonic injection. Furthermore, the active filter also produces an increasing amount of non-characteristic – integer or non-integer multiple order - harmonics which of all them, it is observed that harmonics happening between 3.1 KHz to 3.3 kHz could create a disruptive resonance condition especially at

higher K_p gain values. Nevertheless, it can be seen that for $K_p = 5$, active filter injects 83 % (0.35 A) of load current 5th-harmonic amplitude, 47 % (0.97 A) of load current 11th-harmonic amplitude, 37 % (0.26 A) of load current 23rd-harmonic amplitude, and 63 % (0.19 A) of load current 25th-harmonic amplitude. Figure 110 shows the HFE input waveforms and the FFT of HFE input current. Important power quality information of HFE system currents are provided in Table 33. As it can be seen for $K_p = 5$, where active filter current THD is 242 %, source current THD is reduced from 16.4 % of load to 10.5 % at HFE input. It can also be noted from Figure 110 that system power factor has slightly increased. This is purely due to the fact that input current distortion factor (fraction of fundamental current to rms current) has increased by reduction of input current THD, as it can be noted from Table 33.

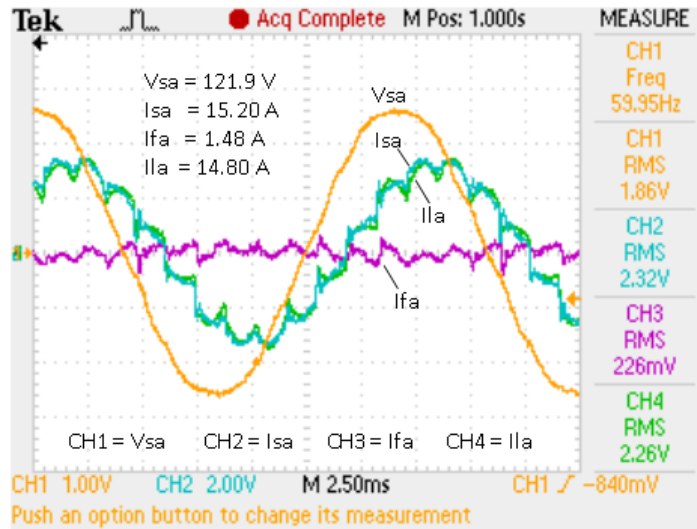


Figure 107 Source phase voltage, source current, load current and active filter current of phase-a when HFE is in harmonic-only compensation mode with $K_p = 5$.

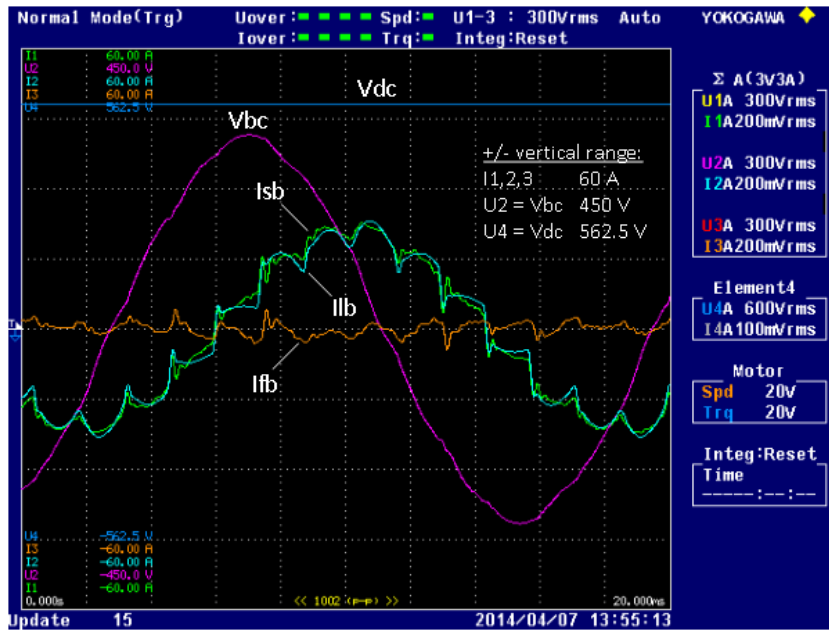


Figure 108 HFE waveforms when the system is operating in harmonics-only compensation mode with $K_p = 5$.

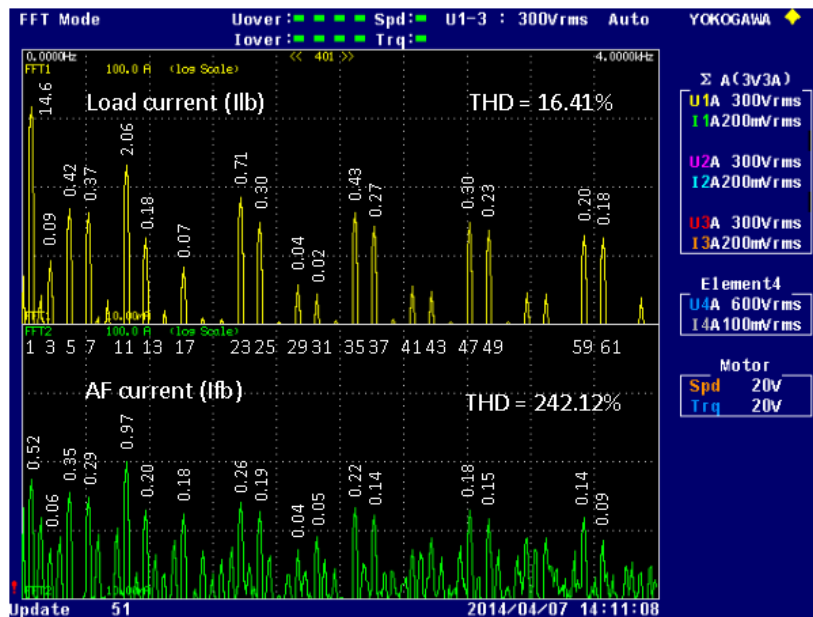


Figure 109 Phase-b load current and active filter current FFT in harmonics-only mode with $K_p = 5$.

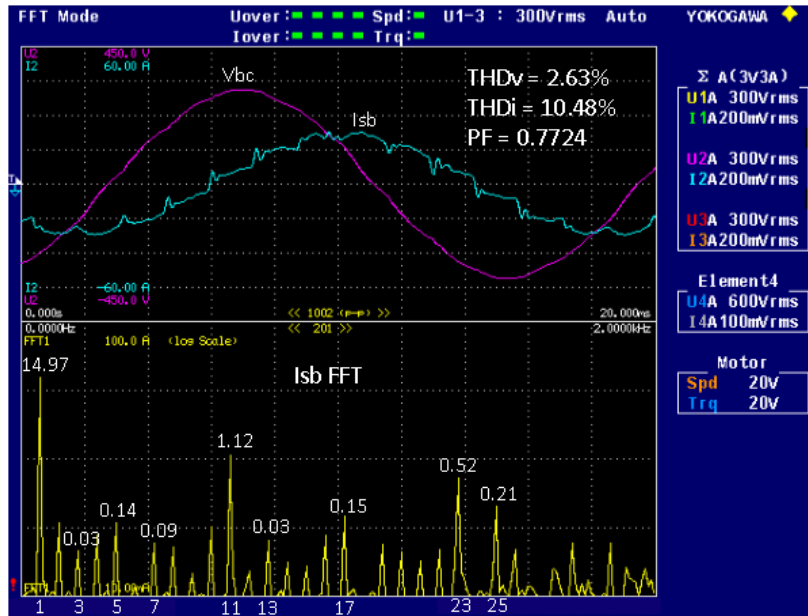


Figure 110 HFE harmonics-only comp. mode with $K_p = 5$ – top plot shows phase-b line voltage and source current and bottom plot shows source current FFT.

Table 33 HFE input current amplitude and distortion in harmonics-only mode ($K_p = 5$)

Function	Element1 (Isb)	Element2 (Ilb)	Element3 (Ifb)	Element4 (Idc)
Irms (A)	15.06	14.79	1.40	8.81
I+peak (A)	23.30	23.14	4.52	8.86
I-peak (A)	-22.68	-23.14	-4.97	8.77
CFI	1.547	1.565	3.554	1.006
Ithd (%)	10.482	16.415	242.129	NAN
Idf (%)	99.45	98.68	38.17	NAN

3.6.2 System THD Analysis in Harmonics-only Mode

For complete THD analysis of input current in HFE, the HFE is run at 4 output power operating points: 1000 W (0.09 PU), 2000 W (0.18 PU), 3000 W (0.26 PU) and 4000 W (0.33 PU). The output d-c voltage is 450 V and input line inductance is 10.5 %. In the first test, the 12-pulse thyristor-bridge is run; and in the second test, the HFE is run in harmonics-only compensation mode with harmonic current compensation gain $K_p = 5$. Due to hardware limitations, the full-load tests could not be carried out. Therefore, the THD results are recorded at all partial-load operating points and are then utilized to predict current THD values at full-load condition. Figure 118 shows the input power flow of HFE at different output power operating points during experimental tests. The data points and associated fitted curve for THD% of current with respect to per unit of input power are shown in Figure 112 and Figure 113 for 12-pulse thyristor-bridge and HFE in harmonics-only mode, respectively. It can be seen that at $S_{in} = 0.5 PU$, THD of input current reduces from 16 % for 12-pulse to 10.5 % for HFE; and at $S_{in} = 1.0 PU$, THD of input current reduces from 11.9 % for 12-pulse to 8.4 % for HFE. The actual THD values are predicted to be in the lower prediction band of the fitted curves, especially for HFE. Thus, the full-load THD of HFE is predicted to be less than 8 % and within the limits of IEEE 519-1992 harmonics standard.

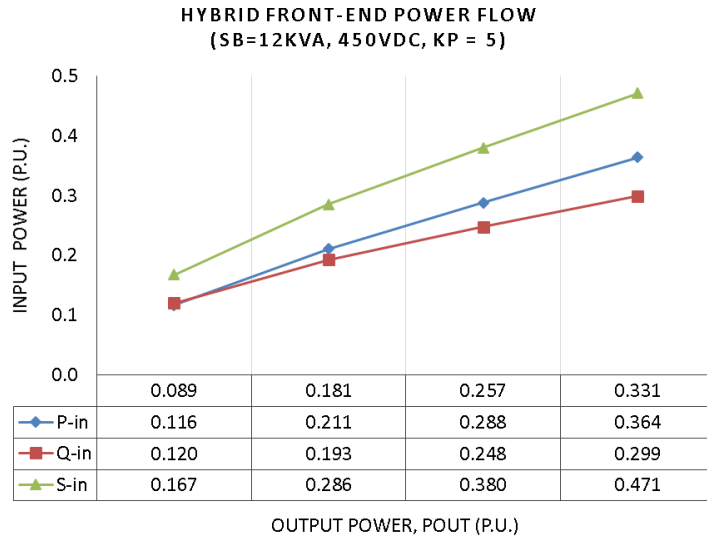


Figure 111 HFE input power flow with respect to output power operating points.

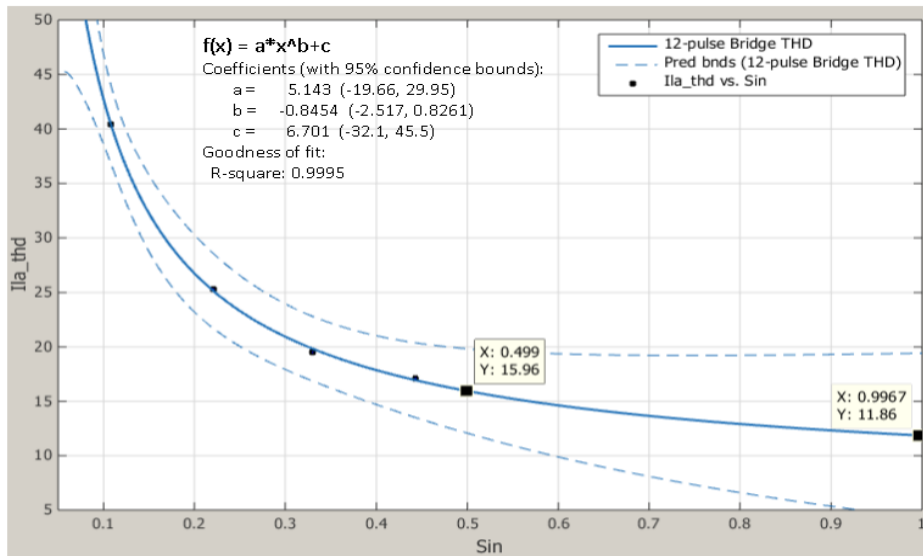


Figure 112 12-pulse bridge data points and fitted curve for THD% of current with respect to per unit of input power.

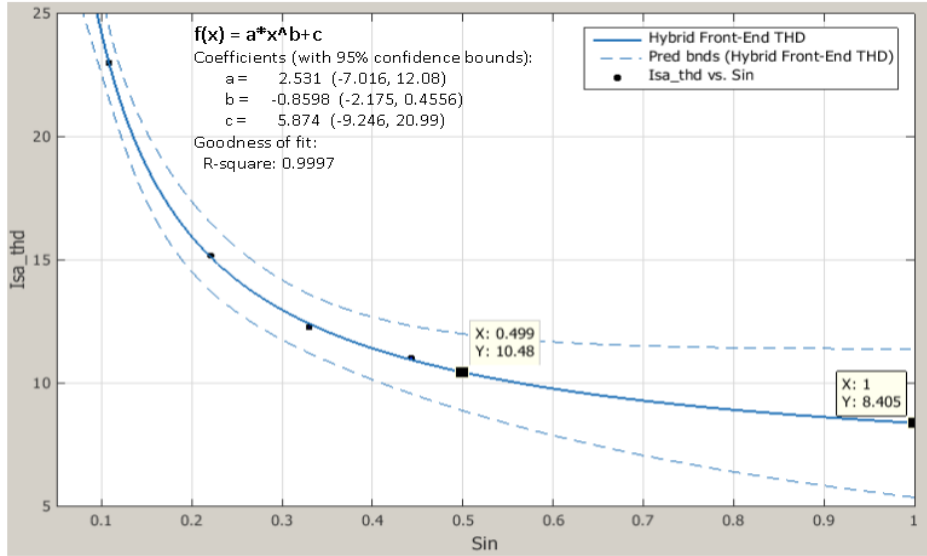


Figure 113 HFE data points and fitted curve for THD% of current with respect to per unit of input power ($K_p = 5$).

3.6.3 Active Filter Power Rating and HFE System Efficiency Analysis

In this section, the required active filter power rating and HFE system efficiency are analyzed for harmonics-only compensation mode. These two important criteria influence the overall sizing and dimensioning of the HFE system. The test operating conditions are the same as for system THD analysis. Figure 114 shows the HFE and active filter apparent power flow in harmonics-only mode with respect to output power when current compensation gain $K_p = 5$. With 12 kVA amounting to 100 % of system rating, it can be observed from Figure 114 that active filter requires only 2-3 % of system rating, at low load condition, and only 1-2 % of system rating, at high-load condition, to perform harmonic compensation. The 12-pulse thyristor-bridge and HFE efficiency curves at operating load conditions are shown in Figure 115. Furthermore, fitted curves on efficiency data points are

utilized to evaluate system efficiency at full-load condition. As it can be seen, the 12-pulse thyristor-bridge efficiency is 94.8 % at full-load condition in Figure 116, whereas HFE efficiency is 94.1 % at full-load condition in Figure 117. The majority of power loss is contributed by equivalent series resistance of input line reactance and, especially, series resistance of input transformers ($R \approx 1\%$ per input phase). The rather large power loss share of input transformer is due to the fact that industrial control transformers with rather high resistive loss are utilized in test-bed. In actual HFE system for mobile mining application power transformers will be utilized and thus, the system efficiency would be even higher.

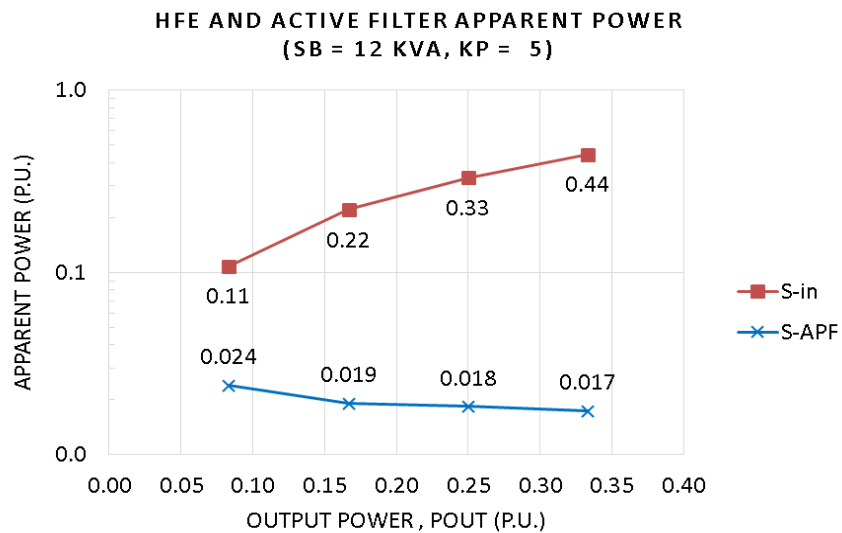


Figure 114 HFE and active filter apparent power flow in harmonic-only mode with respect to output power ($K_p = 5$).

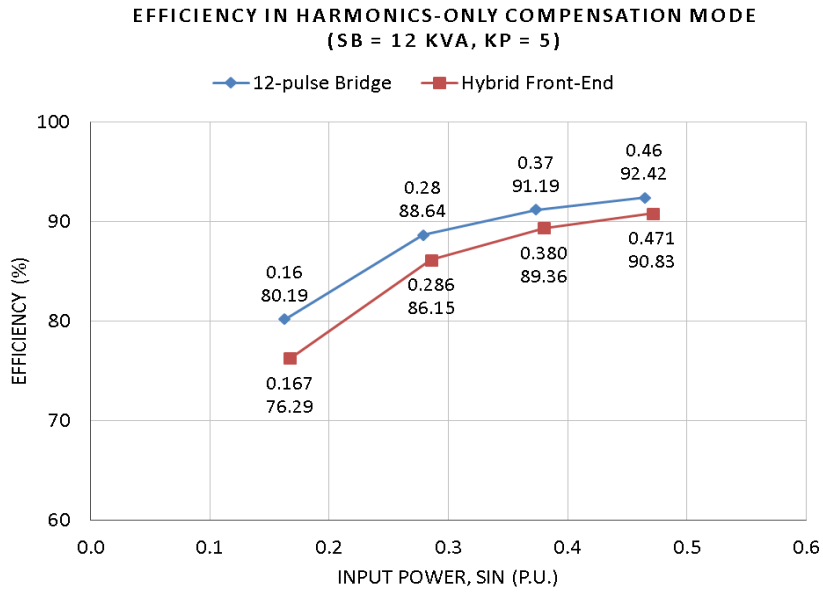


Figure 115 12-pulse thyristor-bridge and HFE efficiency in harmonics-only compensation mode ($K_p = 5$).

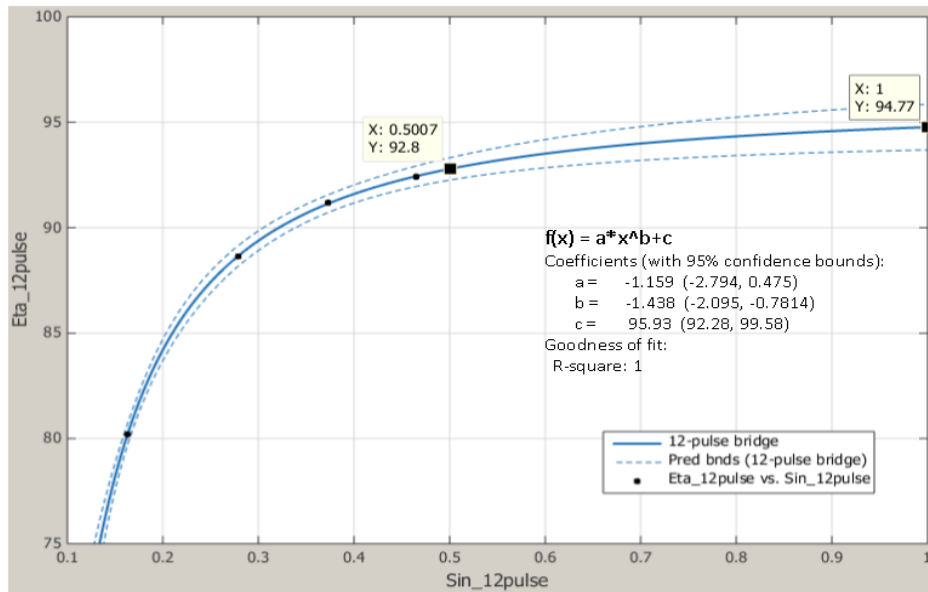


Figure 116 12-pulse thyristor-bridge efficiency percentage data points and fitted curve with respect to per unit of input power.

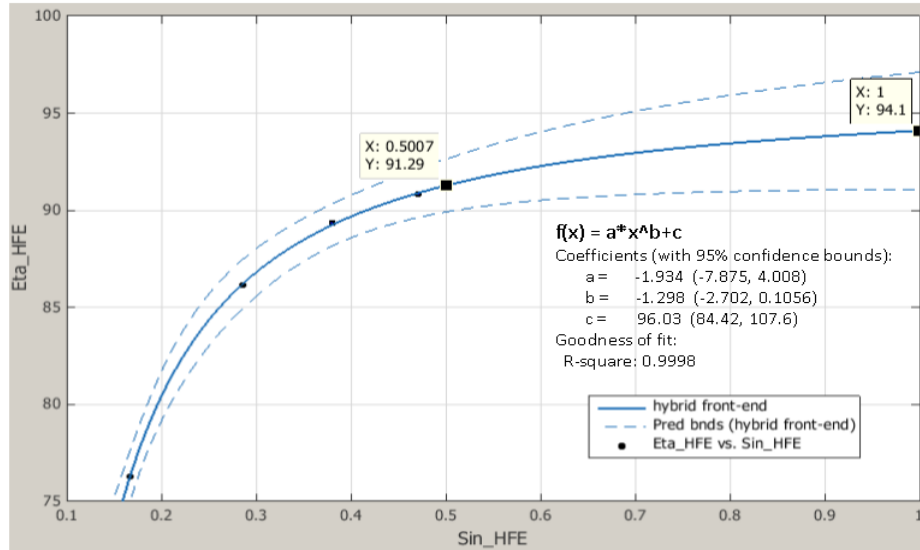


Figure 117 HFE efficiency percentage data point and fitted curve with respect to per unit of input power in harmonics-only compensation mode ($K_p = 5$).

3.6.4 Harmonics-and-VAR-support Compensation Mode

In this compensation mode of HFE, the active filter simultaneously provides harmonics compensation for load current THD reduction and VAR support for input PF improvement. The experimental test operating conditions are given in Table 34. The HFE system input voltage and current waveforms when $k_p = 1$ and $K_Q = 1$ are shown in Figure 118 and Figure 119 for inside the digital controller and actual field measurements, respectively. Table 35 provides HFE system currents amplitude and harmonic distortion information. As it can be seen, the input current THD is only slightly improved – reduced from 16.53 % to 16.18 %; however, as it will be seen in Table 37, input power factor has improved from 0.77 of 12-pulse thyristor-bridge to 0.84 at input of HFE system. The minimal harmonic compensation is also evident from FFT of active filter current, as shown in Figure 120. It can be seen that

active filter only provides 7 % (0.14 A) of amplitude of load current 11th-harmonic which is the dominant harmonic of load current – ~14 % of amplitude of load fundamental current. To further enhance both harmonic compensation and VAR support, the current compensation gain is increased to $K_p = 5$ while reactive power gain is kept at $K_Q = 1$. The HFE input voltage and current waveforms for $K_p = 5$ and $K_Q = 1$ are shown in Figure 121 and Figure 122 for inside digital controller and actual field measurement, respectively. It is noticeable that power factor and current THD are markedly improved at input of HFE. The improvement in harmonic compensation is further demonstrated in Figure 122 where the FFT of active filter current is shown with respect to the FFT of load current. For $K_p = 5$ and $K_Q = 1$, Figure 124 shows input voltage and current waveforms of HFE and input current spectrum, and Table 36 provide current amplitude and harmonic distortion information. It can be seen that power factor has increased to 0.9037 for HFE compared to 0.7718 for 12-pulse thyristor-bridge, and current THD has reduced from 16.05 % for load to 12.41 % for HFE. The power factor information for different compensation modes are summarized in Table 37.

Table 34 Operating test condition of harmonics-and-VAR-support mode

Input line voltage	Vin (V)	215
Output DC voltage	Vdc (V)	450
Input line reactance	Xin (%)	10.5 %
Load resistance	RL (Ω)	53
Output power of 12-p bridge	Pout (W)	3976 (0.33 PU)

Table 34 Continued

Input powers of 12-p bridge	Pin (W)	4369 (0.36 PU)
	Qin (Var)	3592 (0.3 PU)
	Sin (VA)	5655 (0.47 PU)
Power factor of 12-p bridge	PF	0.7718 lagging
Compensation mode	Harmonics-and-VAR-support	
Current compensation gain	Kp	1, 5
Reactive power compensation gain	KQ	1

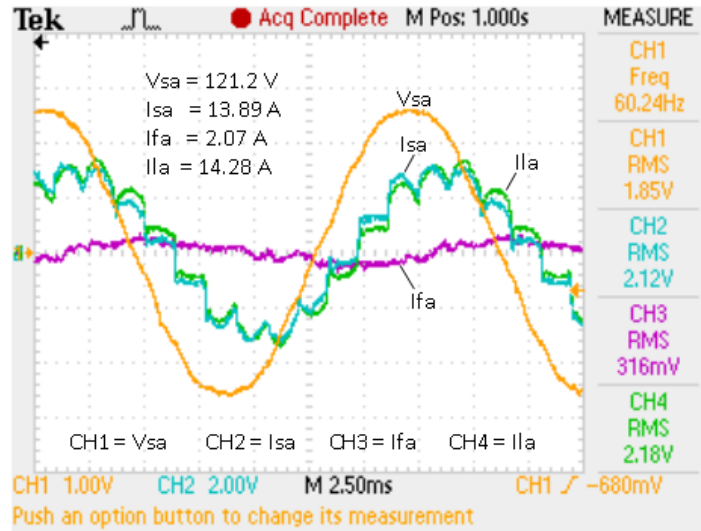


Figure 118 Source phase voltage, source current, load current and active filter current of phase-a when HFE is in harmonics-and-VAR-support mode with K_p = 1 and K_Q = 1.

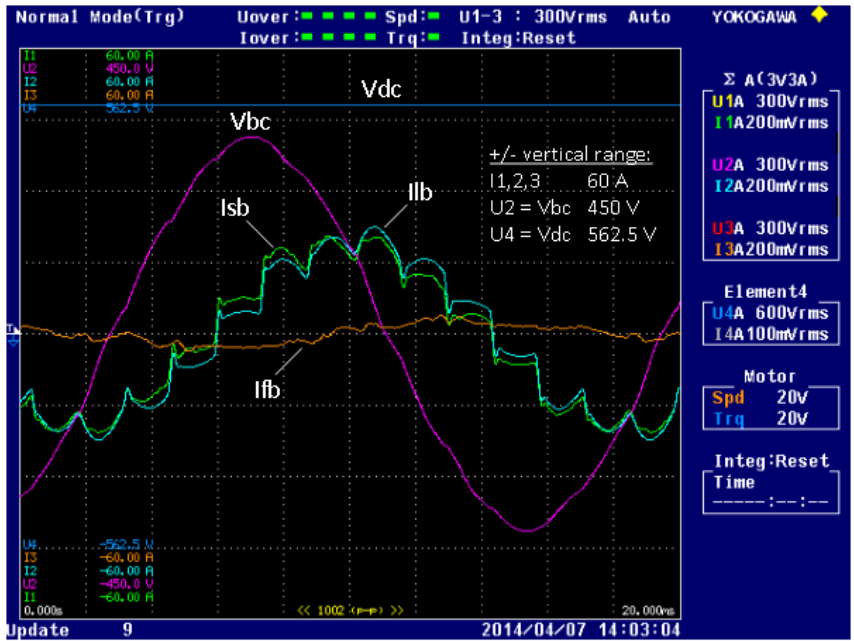


Figure 119 HFE waveforms when the system is operating in harmonics-and-VAR-support mode with $K_p = 1$ and $K_Q = 1$.

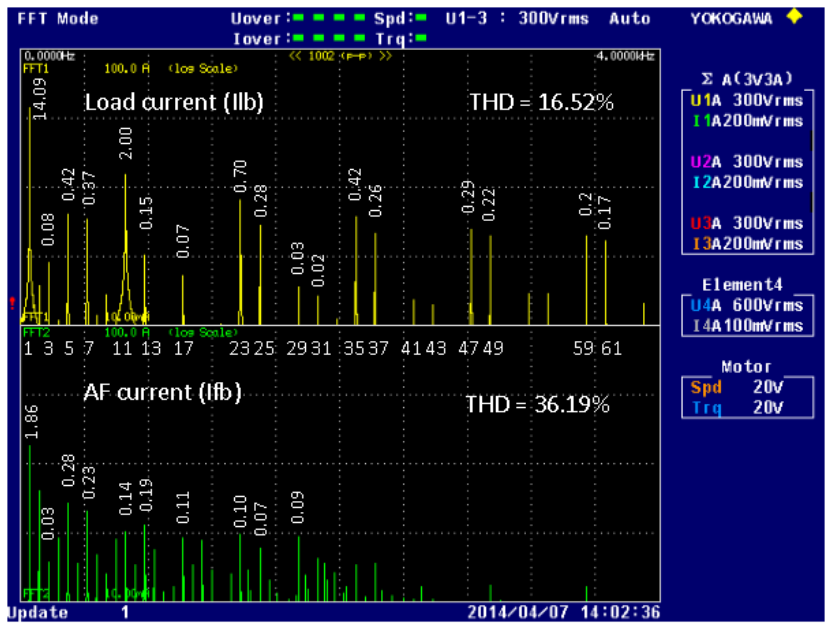


Figure 120 Phase-b load current and active filter current FFT in harmonics-and-VAR-support mode with $K_p = 1$ and $K_Q = 1$.

Table 35 HFE input current amplitude and distortion in harmonics-and-VAR mode ($K_p = 1$, $K_Q=1$)

Function	Element1 (Isb)	Element2 (Ilb)	Element3 (Ifb)	Element4 (Idc)
I_{rms} (A)	13.90	14.28	1.98	8.81
I_{+peak} (A)	21.52	22.42	4.11	8.86
I_{-peak} (A)	-21.31	-22.39	-4.27	8.77
CFI	1.548	1.570	2.157	1.006
I_{thd} (%)	16.184	16.529	36.191	NAN
I_{df} (%)	98.71	98.66	94.03	NAN

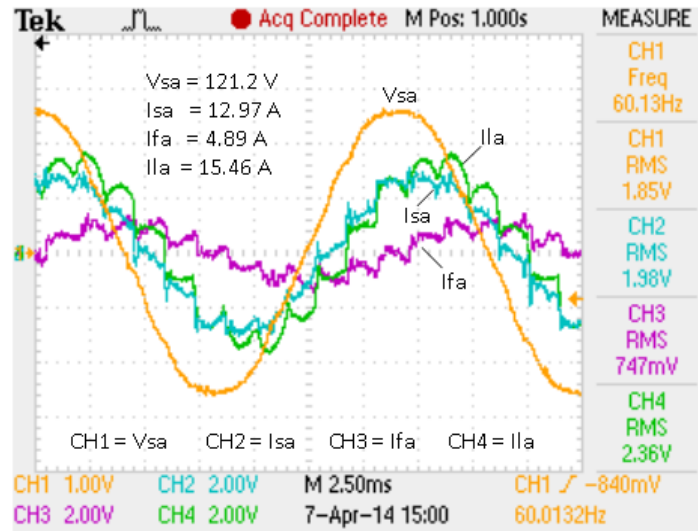


Figure 121 Source voltage, source current, load current and active filter current of phase-a when HFE is in harmonics-and-VAR-support mode with $K_p = 5$ and $K_Q = 1$.

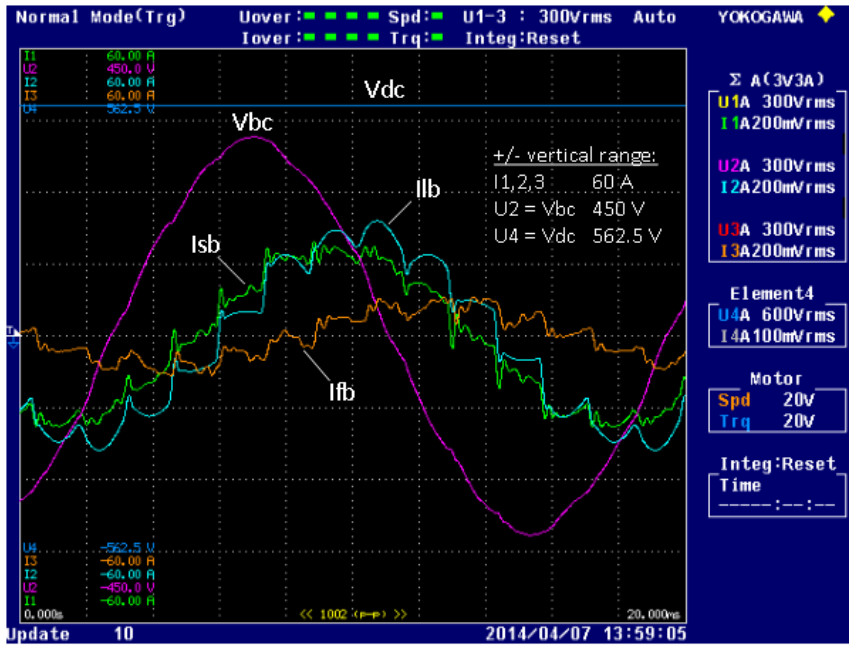


Figure 122 HFE waveforms when the system is operating in harmonics-and-VAR-support mode with $K_p = 5$ and $K_Q = 1$.

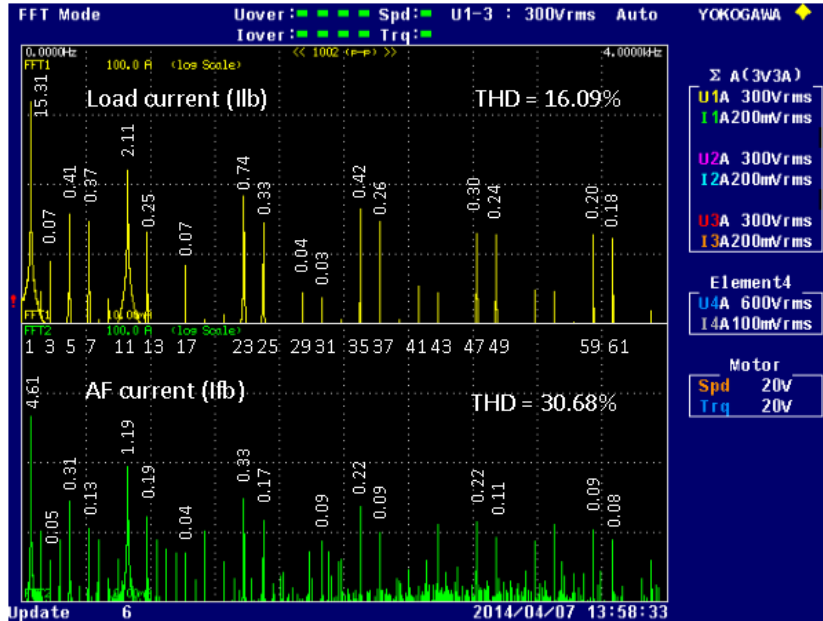


Figure 123 Phase-b load current and active filter current FFT in harmonics-and-VAR-support mode with $K_p = 5$ and $K_Q = 1$.

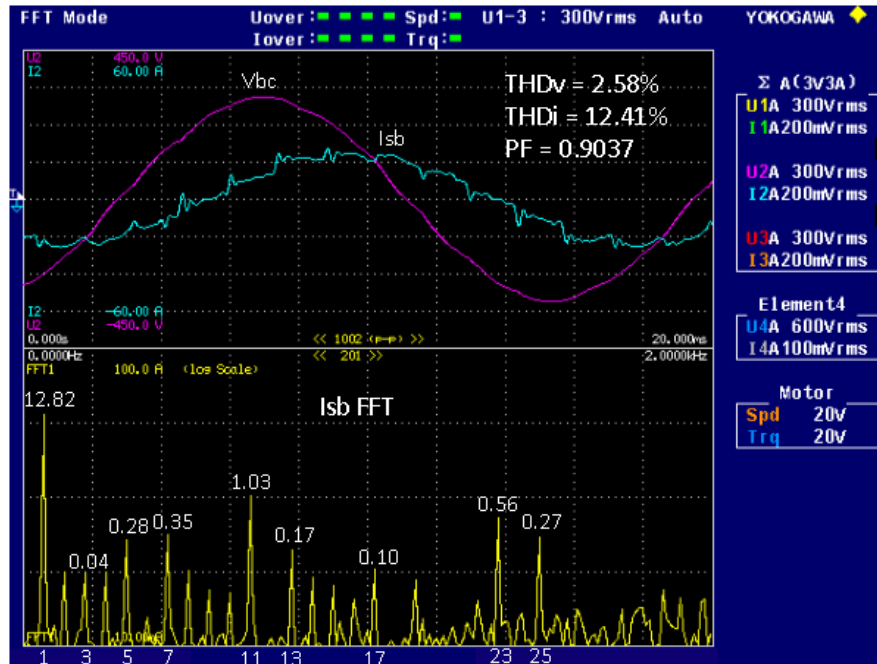


Figure 124 HFE harmonics-and-VAR comp. mode with $K_p = 5$ and $K_Q = 1$ – top plot shows phase-b line voltage and source current and bottom plot shows source current FFT.

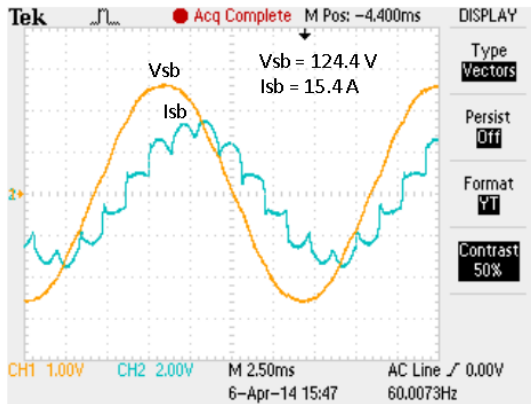
Table 36 HFE input current amplitude and distortion in harmonics-and-VAR mode ($K_p = 5$, $K_Q = 1$)

Function	Element1 (Isb)	Element2 (Ilb)	Element3 (Ifb)	Element4 (Idc)
Irms (A)	12.91	15.51	4.84	8.81
I+peak (A)	20.99	24.14	10.03	8.86
I-peak (A)	-19.62	-24.06	-10.71	8.76
CFI	1.626	1.557	2.212	1.006
Ithd (%)	12.418	16.095	30.688	NAN
Idf (%)	99.23	98.73	95.60	NAN

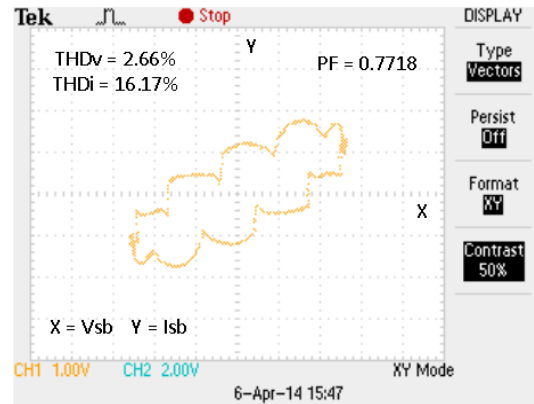
Table 37 Input power factor in different compensation modes

Mode	PF
12-pulse Thyrsitor-Bridge	0.7718
Harmonics-and-VAR-support (Kp = 1, KQ=1)	0.8409
Harmonics-and-VAR-support (Kp = 5, KQ=1)	0.9037

Figure 125 to Figure 127 show input phase voltage and current of phase-b of HFE in both time-domain and X-Y domain for different operating modes. This is to better visually demonstrate how harmonic compensation and power factor correction influence reflect themselves in system quantities. The harmonic distortion and phase lag of 12-pulse thyristor-bridge current along time-axis in Figure 125a translate, respectively, to ripples on the perimeter and area of the shape produced in Figure 125b in X-Y domain. When harmonics of input current are reduced, as in Figure 126a for HFE operating in harmonics-only mode with $K_p = 5$, an oval-like shape is produced in X-Y domain, as in Figure 126b, which has essentially the same area as in Figure 125b. In ideal case of no harmonic distortion, the shape produced in Figure 126b would exactly be an oval. When both harmonic distortion of current and power factor are improved, as in Figure 127a for HFE operating in harmonics-and-VAR-support mode with $K_p = 5$ and $K_Q = 1$, an oval-like shape is again produced in X-Y domain, as in Figure 127b, but the area of the shape is reduced compared to the aforementioned cases. In the ideal case of no harmonic distortion and unity power factor operation, the shape produced in X-Y domain would exactly be a straight line.

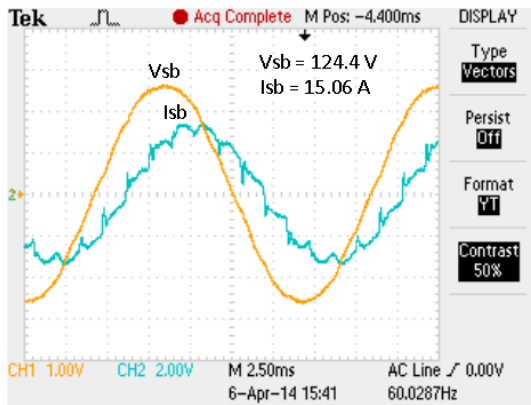


(a)

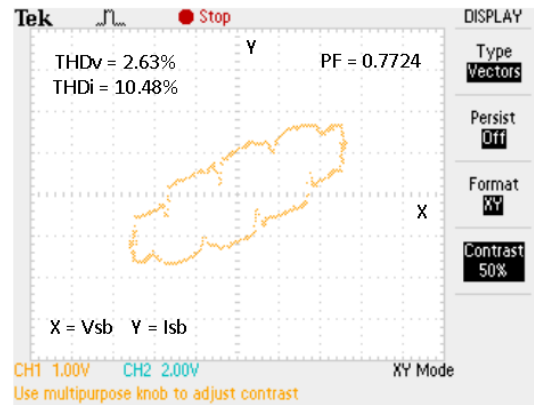


(b)

Figure 125 Phase-b phase voltage and current waveforms in 12-pulse thyristor-bridge mode. (a) time-domain display. (b) XY-domain display.



(a)



(b)

Figure 126 Phase-b phase voltage and current waveforms in harmonics-only compensation mode with $K_p = 5$ and $K_Q = 0$. (a) time-domain display. (b) XY-domain display.

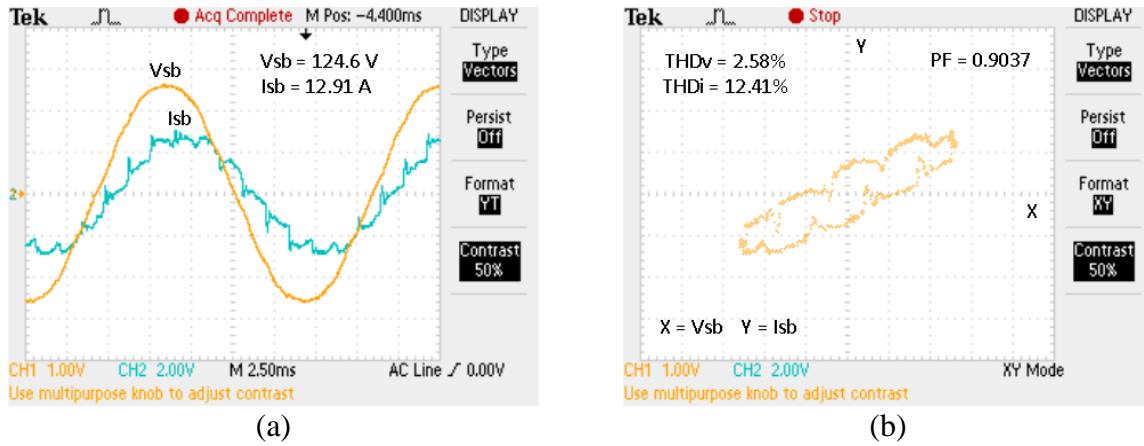


Figure 127 Phase-b phase voltage and current waveforms in harmonics-and-VAR compensation mode with $K_p = 5$ and $K_Q = 1$. (a) time-domain display. (b) XY-domain display.

3.6.5 Unity Power Factor Operation

In order to further demonstrate the harmonics-and-VAR-support mode of operation, a unity power factor test was carried out. The test operating conditions are provided in Table 38. During the test, DC-bus voltage is set to 450 V and output power is set at 1500 W (0.125 PU); current gain value is kept constant at $K_p = 5$; and reactive compensation gain value is sequentially set to $K_Q = 0, 1, 1.5, 2.2$.

Table 38 Unity power factor test operating conditions

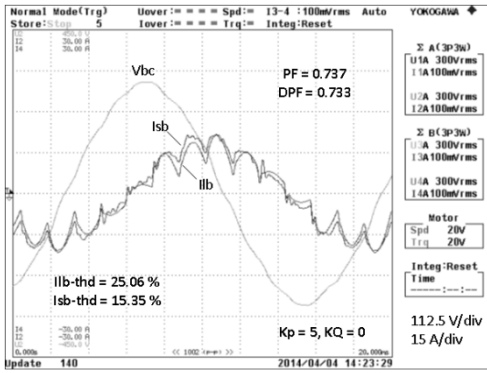
Line voltage	V_{in} (V)	213.32
Line current	I_{in} (A)	6.05
Input line reactance	X_{in} (%)	10.5
DC-bus voltage	V_{dc} (V)	450
Load resistance	R_l (Ω)	136
Output power	P_{out} (W)	1490 (0.124 PU)

Table 38 Continued

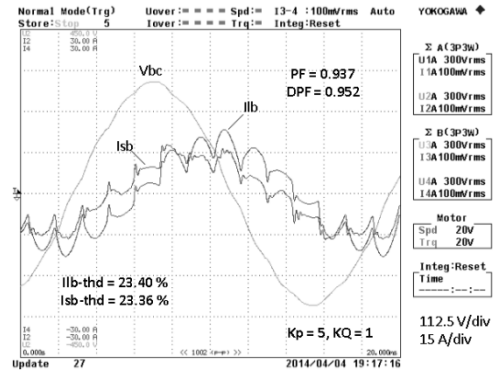
Input power(s)	Pin (W)	1531 (0.127 PU)
	Sin (VA)	2236 (0.186 PU)
	Qin (Var)	1728 (0.144 PU)
Power factor	PF	0.685 lagging (true)
	DPF	0.703 lagging (fund.)
Compensation mode	Harmonics-and-VAR	
Current comp. gain	Kp	5
Reactive comp. gain	KQ	0, 1, 1.5, 2.2

The HFE input voltage and current waveforms are shown in Figure 128 in which THD values of current, power factor (PF) and displacement power factor (DPF) values are also given. DPF is the fundamental power factor resulting from fundamental component of current. PF is always lower than DPF because of harmonic current distortion. It can be seen in Figure 128a that for $K_p = 5$ and $K_Q = 0$ only THD of current is improved from 25 % to 15 % but PF of HFE is not basically changed from 0.73. At $K_p = 5$ and $K_Q = 1$, Figure 128b shows PF is improved to 0.937, however, THD performance is degraded as THD of HFE current is almost the same as THD of load current which is 23 %. By further increasing reactive compensation gain, both THD performance and system PF and DPF are improved. Figure 128c shows that for $K_p = 5$ and $K_Q = 1.5$, DPF is improved to 0.990; PF is improved to 0.981; and THD of current is reduced from 23 % to 18 %. Ultimately, for $K_p = 5$ and $K_Q = 2.2$, Figure 128d shows a true unity PF operation of HFE during which input current THD is also reduced from 23 % to 16 %.

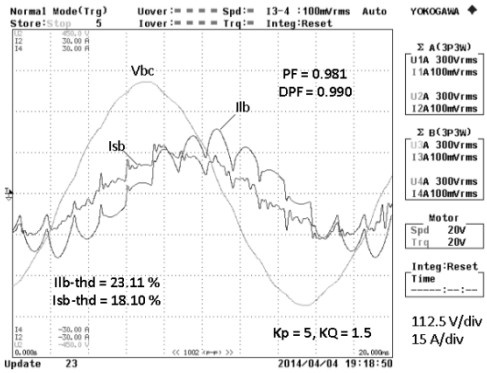
In order to better visually demonstrate the power factor correction operation in HFE, input phase voltage and current are shown in time-domain and X-Y domain in Figure 129 and Figure 130 for 12-pulse thyristor-bridge and unity PF operation, respectively. An oval-like shape is produced in X-Y domain, as shown in Figure 129b, in which ripples on its perimeter and the area enclosed by it are representations of current harmonics and current phase lag, respectively, as shown in Figure 129a. As THD of current and power factor are improved both ripples on the perimeter and area of the oval-like shape are reduced. In the ideal case of zero harmonic distortion and unity PF, the uncompensated oval-like shape would reduce down to a straight line. A close approximation of this condition is shown in Figure 130b for time-domain waveforms of Figure 130a. Even though the current waveform in Figure 130a still has some amount of distortion (16 % THD), however, unity PF is evident from near perfect match of phase voltage and current zero-crossings.



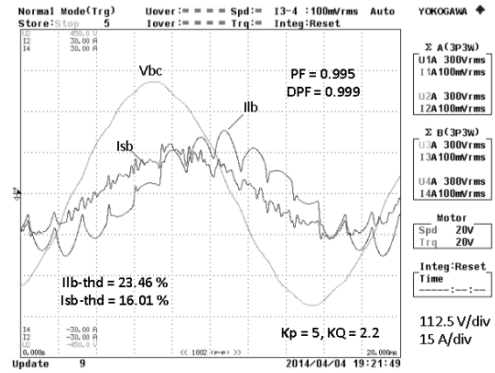
(a)



(b)

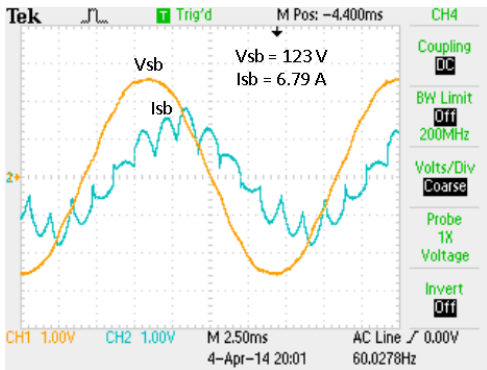


(c)

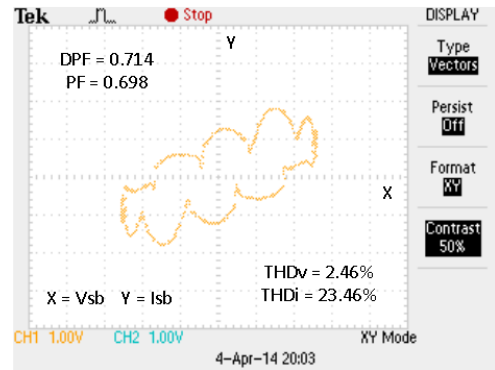


(d)

Figure 128 Input phase-b waveforms of HFE in unity power factor correction test in harmonics-and-VAR-support mode ($K_p = 5$). (a) $K_Q = 0$. (b) $K_Q = 1$. (c) $K_Q = 1.5$. (d) $K_Q = 2.2$.



(a)



(b)

Figure 129 Load (12-pulse thyristor-bridge) phase-b phase voltage and current waveforms in HFE unity PF test. (a) time-domain display. (b) XY-domain display.

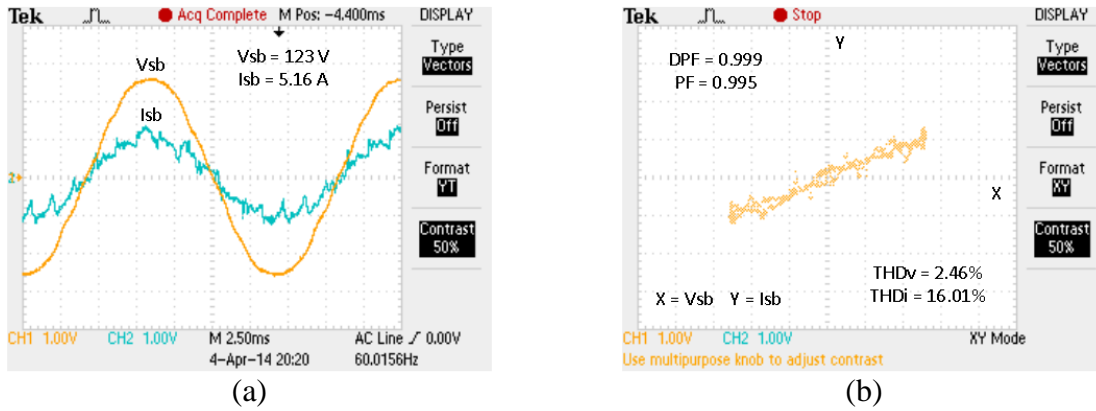


Figure 130 HFE input phase-b phase voltage and current waveforms in unity PF test. (a) time-domain display. (b) XY-domain display.

3.7 Conclusion

In this chapter, a new front-end topology for large mobile mining machines is proposed. The new front-end which is a hybrid topology of 12-pulse thyristor-bridge and IGBT-based active power filter is, thus, called ‘hybrid front-end’ (HFE). It is explained how the simple, reliable, efficient and mature technology of high power thyristors when combined with highly-controllable IGBT switches in HFE enables more power dense and larger equipment by reducing the number of components in the system and easier integration of energy storage by providing more controllability. The steady-state and dynamic simulation results of the system are presented. Furthermore, a 3-ph/208-Vac, 550-Vdc, 12-kVA laboratory-scale HFE test-bed circuit is proposed, developed and tested in FREEDM Systems Center. A proposed digital control system is presented for HFE which allows configuring the system for harmonics-only mode (just compensating harmonic distortion of current) or harmonics-and-VAR-support mode (compensating both harmonic distortion of current and providing partial

VAR support). Complete experimental results for both operational modes are presented at DC-bus voltage of 450 V and different load operating points. It is shown that in harmonics-only mode the active power filter requires only 2-3 % of total system rating to perform harmonic compensation. It is shown that the system has a promising performance in reducing total harmonic distortion (THD) of current with the current test-bed predicted to achieve less than 8 % of THD at full-load condition. Moreover, efficiency measurements of the system verify high efficiency performance of the system by predicting total efficiency at full-load to be higher of 94 %. Finally, the experimental results for harmonics-and-VAR-support compensation mode are presented at output power 4 kW (0.33 PU). Partial VAR support in the system is validated through improving lagging power factor (PF) at input of HFE; and furthermore, unity PF operation of the system is demonstrated.

Chapter 4 **Design Comparison of High Power Medium-Voltage Converters based on Si- and SiC-based Power Devices**

4.1 Introduction

In this chapter, a comparative design study of high power medium-voltage three-level neutral-point-clamped (3L-NPC) converter with 6.5 kV Si-IGBT/Si-PiN diode, 6.5 kV Si-IGBT/SiC-JBS diode and 10 kV SiC-MOSFET/SiC-JBS diode is presented. A circuit model of a 100 A power module, including packaging parasitic inductances, is developed based on device die SPICE-based circuit models for each power device. Switching waveforms, characteristics and switching power and energy loss measurements of the power modules including symmetric/asymmetric parasitic inductances are presented. High power converter designs and SPICE circuit simulations are carried out, and power loss and efficiencies are compared for: (1) A PWM 1 MW power converter at 1 kHz, 5 kHz and 10 kHz switching frequencies for application in shipboard power system (SPS), and (2) A PWM vector-controlled and line frequency angle-controlled 20-40 MVA power converter at 60 Hz, 540 Hz and 1 kHz switching frequencies for active mobile substation (AMS) application. It is shown that the 6.5 kV Si-IGBT incorporating an anti-parallel SiC-JBS diode, with its high efficiency performance up to 5 kHz switching frequency, is a strong candidate for MW-range power converters. The 10 kV SiC-MOSFET/SiC-JBS diode remains an option for higher switching frequency (5-10 kHz) high power converters.

In recent years, the need for power semiconductor devices with high-voltage, high frequency and high-temperature operating capabilities have been growing fast, especially, in military and power transmission/distribution applications, as the enabling technology for more efficient and compact power conversion [60]. In marine and shipboard military applications, size and weight are critical constraints in the design of shipboard power system (SPS), and thus, high switching frequency and high power density operation is required [1]. According to the office of naval research technology roadmap [5], the navy is embarking on the development of a medium-voltage dc (MVDC) system of 6-8 kV voltage class in the next generation of integrated power system for future surface ships and submarines as a means of providing better fuel economy and architectural flexibility for high energy mission systems. The MVDC system will accommodate increased power capacity onboard by taking into consideration the ship's limited available space and weight constraints.

In the power transmission and distribution sectors, with the new smart grid application enabling large integration of renewable and distributed energy resources, 60 Hz distribution class transformers are envisioned to be replaced by more versatile, compact solid-state-based transformers (SSTs) [62]. On the other hand, knowing that high power, high voltage transformers are the single most valuable asset in power transmission grid, concerns about enhancing the security of electricity in case of natural and man-made disasters in the 21st century, has led to research and development of emerging technologies such as solid-state transmission/distribution “recovery” transformer and active mobile substation (AMS) [63], [63]. These new technologies have to meet all functional requirements of standard 60 Hz

transformers and, additionally, have to feature small size, weight and volume for transportability and ease of installation.

High voltage power semiconductors are at the core of any high power, power electronic conversion system. High voltage Silicon IGBTs (Si-IGBTs) with Silicon PiN (Si-PiN) anti-parallel diodes, namely 6.5 kV Si-IGBT/Si-PiN diodes, are commercially available at different current ratings [65], and are used due to ease of driving, low drive power and low conduction loss. Due to the design objectives and economic operation considerations, silicon power semiconductors at high voltage are designed to have enhanced conductivity and low losses during on-state [66]. However, this causes increased switching loss in high voltage Si-IGBT and reverse recovery loss in high voltage Si-PiN diode under hard switching conditions. In fact, it is shown in [67] that anti-parallel Si-PiN diode reverse recovery loss (E_{rec}) comprises the major portion of turn-on energy loss (E_{on}) in high current 6.5 kV Si-IGBTs. In inverters with high voltage rating, the combination of turn-on loss of the switch and reverse recovery loss of the diode make up 40 to 60 percent of total inverter losses [68].

It is shown that wide bandgap Silicon-Carbide (SiC) devices versus Si-based devices possess superior properties like 10 times higher breakdown electric field, higher thermal conductivity and much lower intrinsic carrier concentration [69]. These properties indicate that SiC is a superior material over Si in high frequency, high voltage and high temperature applications. High voltage SiC devices, namely 10 kV SiC MOSFETs and 10 kV Junction-Barrier-Schottky (JBS) diodes, have been developed by Cree [78]. High voltage SiC-JBS diodes are especially advantageous due to minimum reverse recovery phenomenon at turn

off. It is because of this fact that a hybrid power module incorporating a 6.5 kV Si-IGBT and a 6.5 kV SiC-JBS diode can also be a viable semiconductor technology solution for high power, power converter applications. In [71], comparative design of the power devices in mega-watt (MW) power converters for application in shipboard power system (SPS) was presented but the effect of packaging and stray parasitic inductances on power loss, especially at higher switching frequency, was not investigated.

In this chapter a comparative design study of high power three-level neutral-point-clamped (3L-NPC) converter with 6.5 kV Si-IGBT/Si-PIN diode, 6.5 kV Si-IGBT/SiC-JBS diode and 10 kV SiC-MOSFET/SiC-JBS diode has been carried out to provide a technology roadmap for high power and medium-voltage applications. Section 4.2 presents the equivalent circuit model, switching characteristics and loss measurements for 100 A power device modules including inductive parasitics. Section 4.3 discusses the impact of kelvin-emitter inductance on current distribution and power loss of IGBT power modules. In section 4.4.1, NPC-based power converter design for SPS application is presented and simulation results are used to evaluate losses and efficiency at different switching frequencies for a PWM 1 MW power converter. In section 4.4.2, a complete power loss and efficiency evaluation for AMS as a power transmission class power conversion system is presented. Finally, in section 4.4.1, thermal limit and switching frequency capability of power converters are investigated.

4.2 Power Module Modeling and Switching Characteristics

In this section, power device die SPICE-based models are used to construct equivalent circuit models of 100 A power device modules which also include different parasitic inductances. The power module models are then used in an inductive-clamped load test circuit to measure and compare switching characteristics and power losses under hard switching condition. For that purpose, the inductive-clamped switching circuit of Figure 131 is considered. This circuit emulates the hard switching condition under which power devices in most high power converters operate. As compared to the ideal test circuit in [70], this circuit includes gate loop parasitic inductance (L_g), kelvin-emitter inductance (L_{ke}), lead connection inductance (L_s) and dc-link stray inductance (L_d), the values of which are all shown in Figure 131. In what follows, a gate resistance (R_g) of 11 ohms is considered for the Si-IGBTs and R_g of 3.7 ohms is considered for SiC-MOSFET. A double gate-pulse voltage of LOW (0 V) and HIGH (20 V) is applied to the device under test (DUT) in such a way that the switching action occurs at rated current of 100 A.

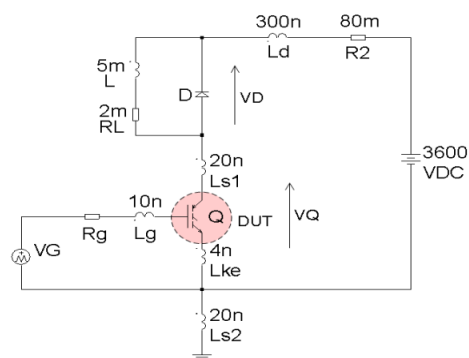


Figure 131 Inductive-clamped load test circuit for simulating power devices under hard switching condition at junction temperature (T_j) of 27°C.

4.2.1 Silicon IGBT Power Module Modeling and Switching Waveforms

For the 6.5 kV/100A IGBT power modules, a chip layout arrangement similar to one section of EUPEC 3.3 kV IGBT layout, as shown in [72], has been adopted. Figure 132a shows the 6.5 kV/100A Si-IGBT power module chip layout incorporating anti-parallel diodes, and Figure 132b shows the equivalent circuit model thereof. For the 6.5 kV Si-IGBT/Si-PiN diode power module, each section in the layout consists of 4x25 A IGBT dies in parallel and 2x50 A anti-parallel diode dies in parallel [73]. For the 6.5 kV Si-IGBT hybrid power module co-packed with 6.5 kV SiC-JBS diode, the IGBT subsections remain the same and only 10x10 A SiC-JBS diode dies are put in parallel. The die circuit models for 6.5 kV Si-IGBT and Si-PiN diodes are based on the modeling approach in [74], and the circuit model for 6.5 kV SiC-JBS diode is based on modeling approach in [78].

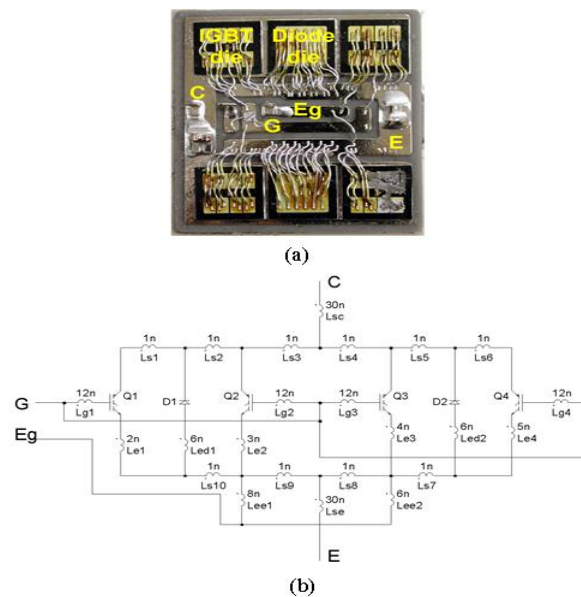


Figure 132 6.5 kV/100A Si-IGBT/Si-PiN diode power module: (a) one section chip layout consisting of 4xIGBTs in parallel and 2 anti-parallel diodes as in [72], (b) equivalent circuit model.

The parasitics included in the modeling are wire-bond inductances, trace inductances and terminal lead connection inductances. According to [76], self-inductance of a 24-mm long, 20-mil thick wire bond is between 10-16 nH; therefore, accordingly, the inductance of several of them in parallel can be estimated. The substrate conductor trace inductance is within a range of a few nH, and terminal leads inductance from substrate to mounting joints is about 30 nH. Based on these values, the equivalent circuit model for both 6.5 kV Si-IGBTs and 10 kV SiC-MOSFET are created. To evaluate switching turn-on and turn-off waveforms, simulations are carried out in SIMetrix/SIMPLIS advanced SPICE circuit simulator [77]. In test circuit of Figure 131, gate resistance R_g is set to 11 ohms and a double gate pulse voltage of 0 V (LOW) and 20 V (HIGH) is applied to each DUT. Figure 133 shows the switching waveforms for 6.5 kV/100A Si-IGBT/Si-PiN diode power module, and Figure 134 shows switching waveforms for the 6.5 kV/100A Si-IGBT/SiC-JBS diode power module.

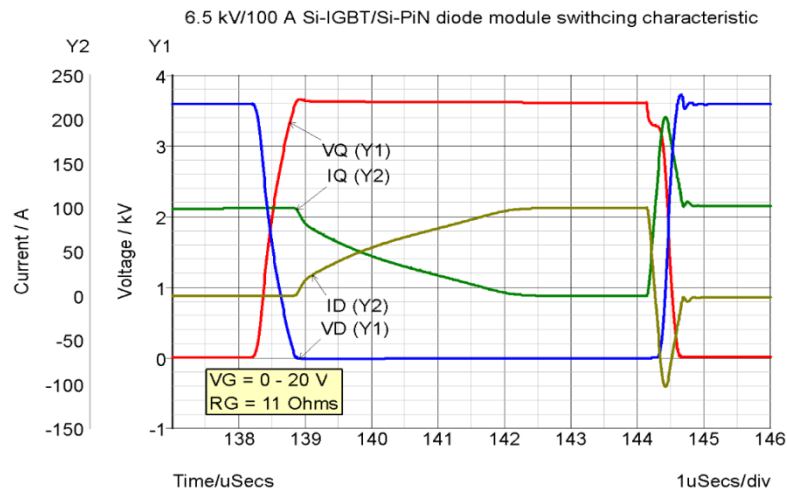


Figure 133 6.5 kV/100A Si-IGBT/Si-PiN diode power module switching characteristics.

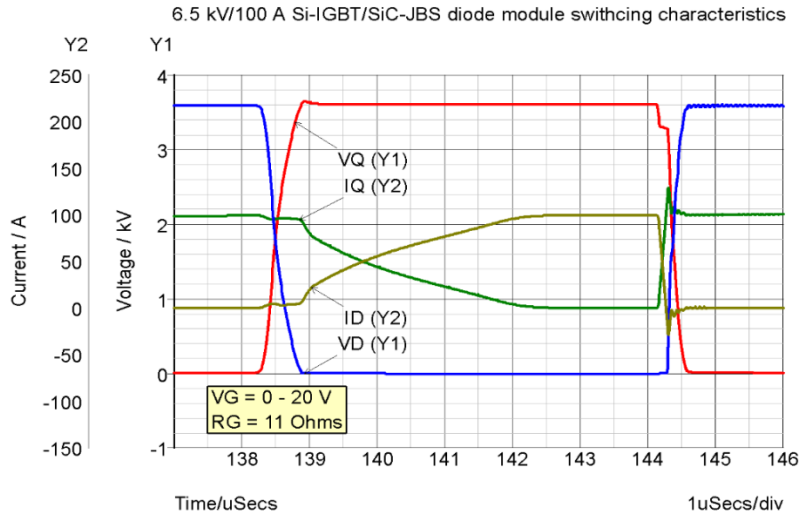


Figure 134 6.5 kV/100 A Si-IGBT/SiC-JBS diode power module switching characteristics.

4.2.2 Silicon Carbide MOSFET Power Module Modeling and Switching Waveforms

For the SiC-MOSFET power module, an internal chip layout similar to that of 10 kV/50A SiC MOSFET dual switch module [78], also shown in Figure 135a, is considered. Similarly, the 10 kV/100A power module consists of twenty 10 kV/5A SiC-MOSFET dies and twenty 10 kV/5A SiC-JBS diode dies that are paralleled per switch. Figure 135b shows the equivalent SPICE circuit model of the power module. A Si Schottky diode is put in series with SiC-MOSFET in order to cancel out any effect of internal body diode. Nevertheless, it should be pointed out that the anti-parallel SiC-JBS diode has a turn-on voltage of 1 V, whereas the internal Si body diode has a turn-on voltage of about 3 V, and thus, it is effectively bypassed [79]. The die circuit models for SiC-MOSFET and SiC-JBS diode are based on modeling approach in [70] and [78]. Figure 136 shows the switching waveforms of the power module.

4.2.3 Switching Energy and Power Loss Analysis and Comparison

In this subsection, comparative analysis of switching energy and power loss of the aforementioned power devices is presented. The analysis includes the impact of increase in switching speed on all loss components through measurements at four different gate resistances that are decreased, in a logarithmic base of 3, from 100 ohms to 3.7 ohms. The same gate resistance is used for both turn-on and turn-off conditions.

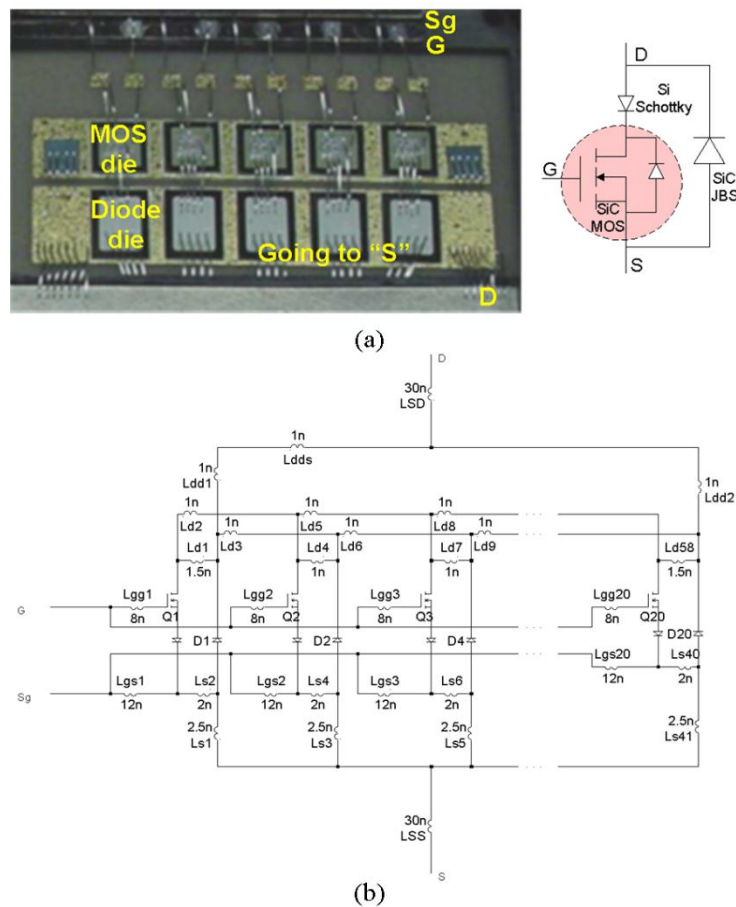


Figure 135 10 kV/100A SiC-MOSFET/SiC-JBS diode power module: (a) one section layout of 10 kV/50A module as in [78], (b) equivalent circuit model.

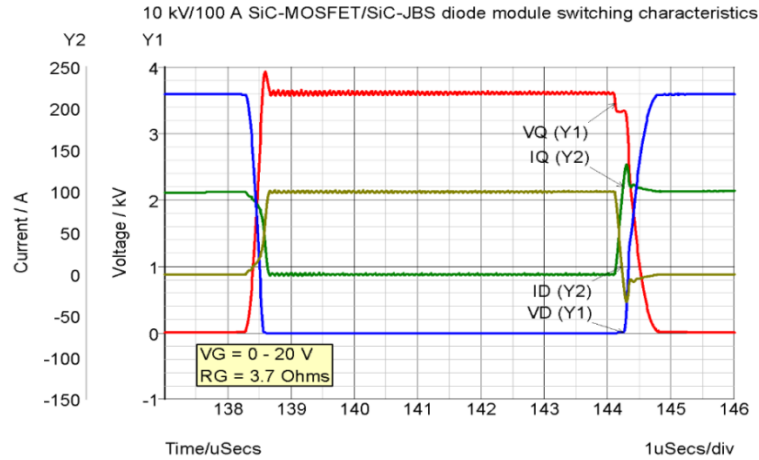


Figure 136 10 kV/100A SiC-MOSFET/SiC-JBS diode power module switching characteristics.

Since all devices considered in this paper are MOS-controlled devices, decreasing gate resistance leads to faster turn-on which, in turn, results in lower turn-on energy loss. This fact is shown in Figure 137 where, among all power devices, the Si-IGBT/SiC-JBS diode hybrid module possesses the lowest turn-on energy loss for all gate resistances. Under hard switching conditions, turn-on of the main switch is simultaneous with turn-off of the anti-parallel diode when current starts commuting from the diode to the switch. The faster the turn-on condition, the higher the current slew-rate and thus, the higher reverse recovery loss (E_{rec}) is in Si-PiN diode and turn-on loss (E_{on}) is in Si-IGBT. At $R_g = 3.7$ ohms, turn-on energy loss of 6.5 kV Si-IGBT/Si-PiN diode is almost 3.5 times higher than that of 6.5 kV Si-IGBT/SiC-JBS diode.

Figure 138 shows E_{rec} for all power diodes with respect to R_g . For 6.5 kV Si-PiN diode, E_{rec} is much higher as compared to other devices, due to removal of dense charge built-up and charge carrier recombination process [66]. It also increases steadily with decreasing gate

resistance, whereas it remains negligible and almost constant for the other two SiC-JBS diodes. At $R_g = 3.7$ ohms, 6.5 kV Si-PiN diode has a reverse recovery loss which is almost 37 times higher than that of 6.5 kV SiC-JBS diode.

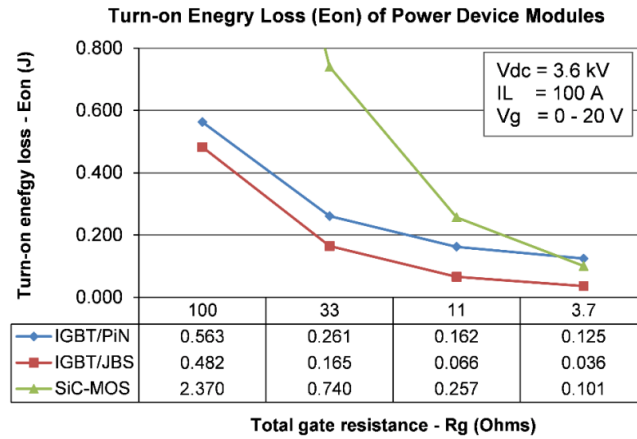


Figure 137 Turn-on energy loss (E_{on}) curves for all power device modules with respect to total gate resistance (R_g).

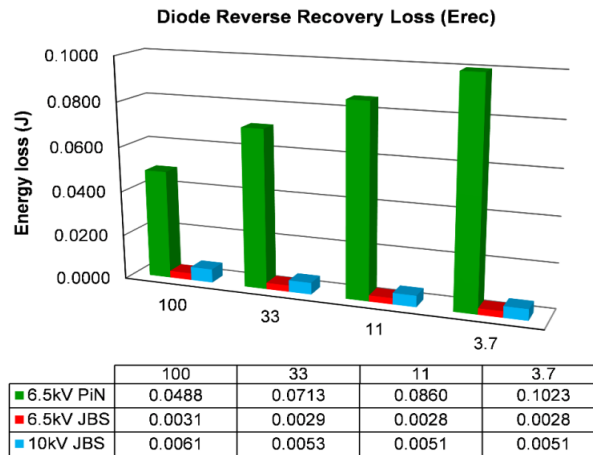


Figure 138 Diode reverse recovery loss (E_{rec}) with respect to gate resistance (R_g).

Figure 139 shows turn-on power loss (P_{on}) of power device modules. For 6.5 kV Si-IGBT/Si-PiN diode, P_{on} is higher compared to other devices and increases considerably with increase in switching speed, whereas it remains almost constant for the other two devices. This means that if the same thermal design and maximum junction temperature ($T_{j,max}$) has to be considered for those power devices with all operating within their safe operating area (SOA) boundary, 6.5 kV Si-IGBT/Si-PiN diode power module has to operate at much lower switching frequency and/or rated output power, comparatively.

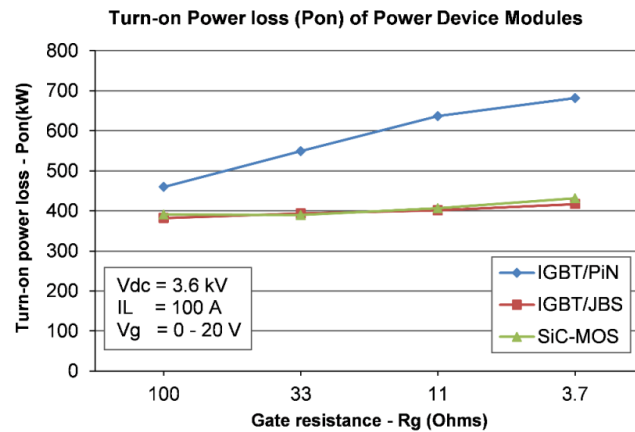


Figure 139 Turn-on power loss (P_{on}) curves for all power device modules with respect to total gate resistance (R_g).

Turn-off energy loss for high voltage Si-IGBTs is mainly due to two mechanisms: turn-off of MOS channel in the device, and removal of charge built up in the n-base region of the device during on-state [80]. The energy loss associated with MOS-channel turn-off decreases remarkably with decrease in gate resistance; however, removal of the dense charge, which is

mainly dependent on the recombination process and charge carrier lifetime [66][80] ,, is not affected by change in gate resistance and remains almost constant. This manifests itself through a relatively long current tailing segment during turn-off for both of the Si-IGBTs, as it is shown in Figure 133 and Figure 134.

Figure 140 shows the overall turn-off energy loss for all of the power devices. It can be seen that turn-off energy loss for both Si-IGBTs reaches an almost steady, and relatively high, value even as the gate resistance is decreased to a very low value of 3.7 ohms. As mentioned earlier, this is because of recombination process within device and charge carrier lifetime which is mainly independent of gate resistance. In contrast, it is seen that turn-off loss of the SiC-MOSFET decreases significantly with decrease of gate resistance. This is mainly due to unipolar nature of this device [66]. It can be seen from Figure 140 that both Si-IGBTs have a turn-off loss more than 12 times higher than that of the SiC-MOSFET at $R_g = 3.7$ ohms.

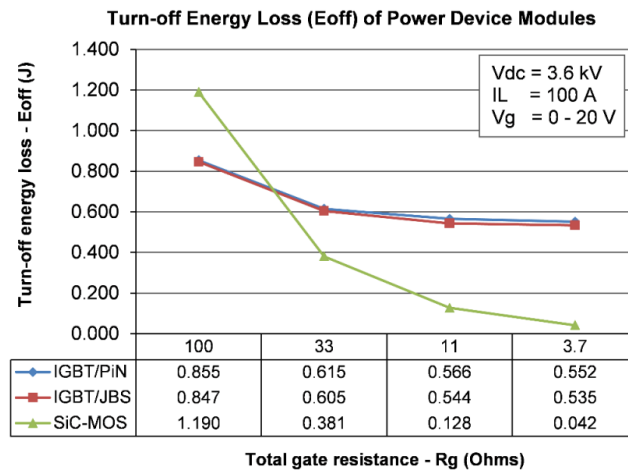


Figure 140 Turn-off energy loss (E_{off}) curves for all power device modules with respect to gate resistance (R_g).

Figure 141 shows turn-off power loss (P_{off}) for all the power devices with respect to gate resistance. It is seen, expectedly, that turn-off power loss for the Si-IGBT devices remains almost constant with decrease in gate resistance, whereas turn-off power loss of the SiC-MOSFET decreases. It is also important to note from comparison of Figure 141 with Figure 139 that, under hard switching condition, turn-on power loss is always higher than turn-off power loss; thus, it should be considered as the driving factor in thermal design of power converter.

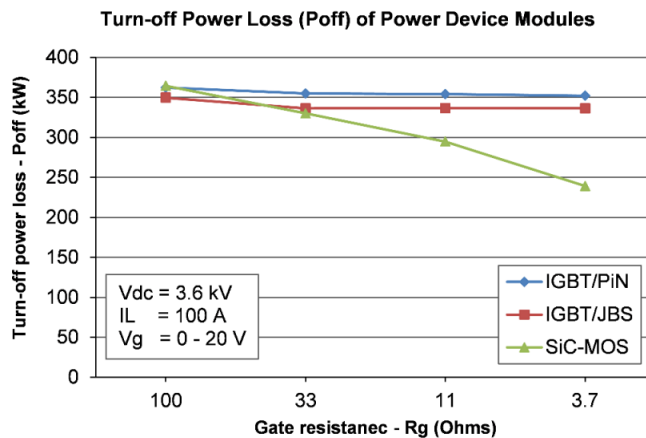


Figure 141 Turn-off power loss (P_{off}) curves for all power device modules with respect to total gate resistance (R_g).

The total switching energy loss (E_{tot}) comparison and evaluation for power device modules, including turn-on and turn-off losses of both switch and anti-parallel diode, is presented in Figure 142. For 6.5 kV Si-IGBTs, at high gate resistance, the total energy loss is

high due to both turn-on and turn-off losses being high. As gate resistance is decreased, even though turn-on energy loss decreases, turn-off energy loss remains almost constant, and thus, it dominates the total loss. Hence, the total energy loss reaches an almost constant value. The Si-IGBT/SiC-JBS diode hybrid module has a lower total energy loss compared to the Si-IGBT/Si-PiN diode module mainly due to avoidance of loss mechanisms induced by the Si-PiN diode's reverse recovery phenomenon. The resultant efficiency improvement in high voltage, high power converters will become evident in Section IV where numerical simulation results are presented. For 10 kV SiC-MOSFET/SiC-JBS diode power module, both turn-on and turn-off losses reduce considerably with decrease in gate resistance value. This leads to lowest total energy loss for the SiC-MOS/SiC-JBS diode among all the power devices at R_g equal to 11 ohms and 3.7 ohms, respectively.

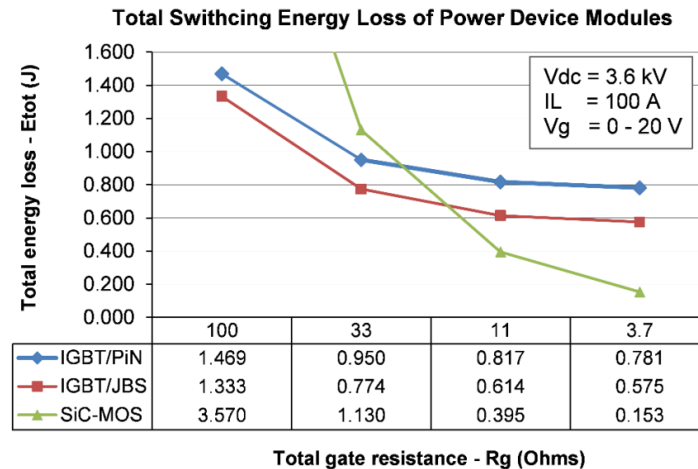


Figure 142 Total switching energy loss (E_{tot}) curves for power device modules with respect to total gate resistance (R_g).

4.3 IGBT Module Parasitics Impact on Current Distribution and Power Loss

In this section, the impact of kelvin-emitter inductance (L_{ke}) unbalance in the circuit model of Figure 132b, on current distribution among the Si-IGBT dies, and on total power loss of both Si-IGBT modules, is investigated. To study the effect of unbalance, simulations are carried out in SIMetrix SPICE circuit simulator for two consecutive switching events. As it is shown in Table 39, four cases are considered: case I represents the reference balanced condition with nominal kelvin-emitter inductance of 4 nH; case II and case III represent symmetric unbalance conditions; case IV represents an asymmetric unbalance condition. Figure 143 and Figure 144 show the internal current distribution between 4x25 A IGBT dies (chips) in case III for both Si-IGBT power modules. From simulation results for all unbalanced cases, it is seen that it is case III that results in worst unbalanced current distribution between Si-IGBT chips inside the Si-IGBT/SiC-JBS diode module, whereas the internal chip current distribution of the Si-IGBT/Si-PiN diode module remains approximately balanced. This suggests that a revised internal chip layout design may be needed to guarantee safe and reliable operation of the Si-IGBT/SiC-JBS diode hybrid module under real hard switching conditions.

Table 39 IGBT kelvin-emitter inductance unbalance cases

Case	Condition	L_{e1} (nH)	L_{e2} (nH)	L_{e3} (nH)	L_{e4} (nH)
I	balanced	4	4	4	4
II	unbalanced	4	3	3	4
III		3	4	4	3
IV		2	3	4	5

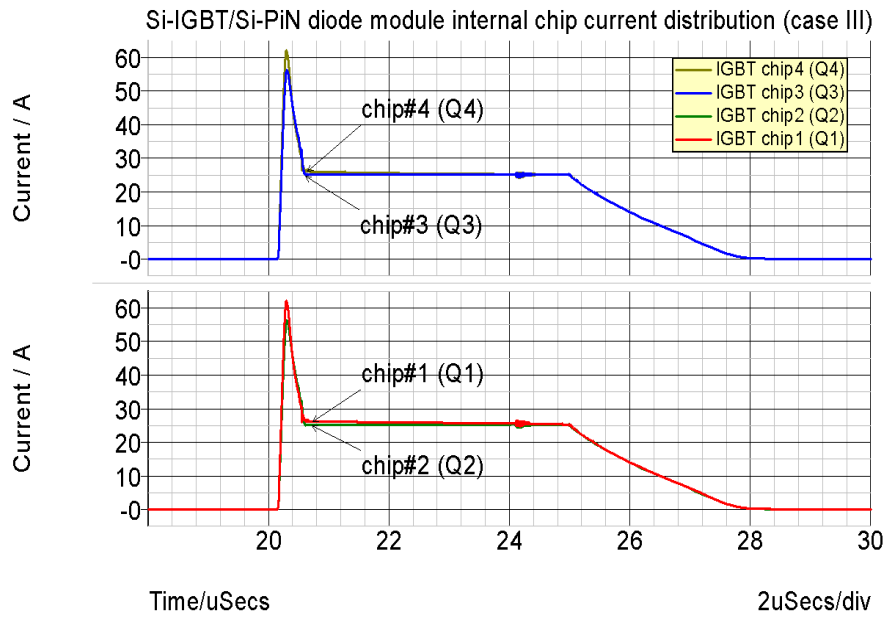


Figure 143 Si-IGBT/Si-PiN diode module IGBT dies current (Case III).

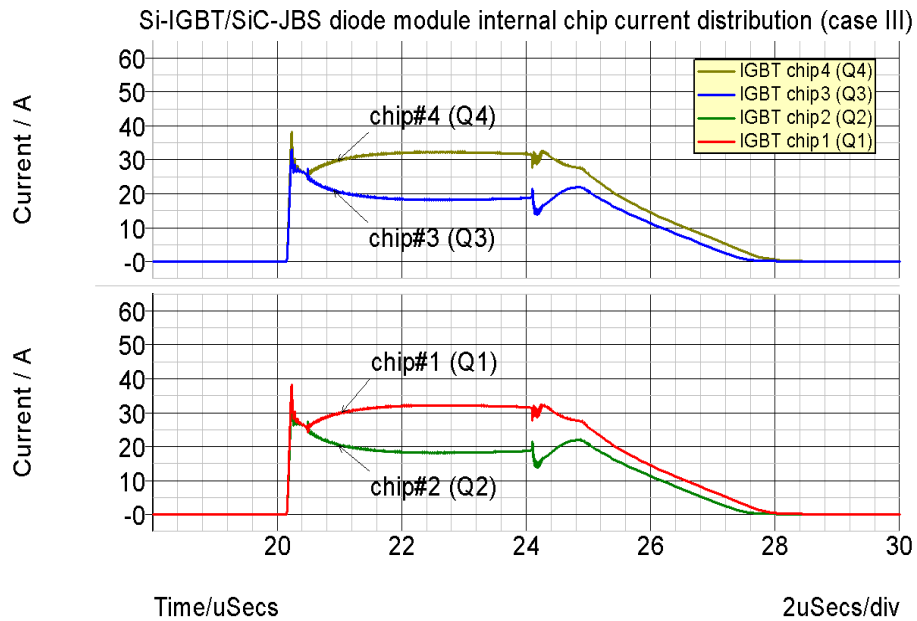


Figure 144 Si-IGBT/SiC-JBS diode module IGBT dies current (Case III).

Figure 145 and Figure 146 show turn-on energy loss (E_{on}) for both Si-IGBT power modules under all cases. As for the 6.5 kV Si-IGBT/Si-PiN diode module, turn-on energy loss almost doubles at second pulse with case II having the highest loss among all. However, for 6.5 kV Si-IGBT/SiC-JBS diode module, turn-on loss at first and second pulse remains approximately the same. This implies that the 6.5 kV Si-IGBT/SiC-JBS diode hybrid module, overall, can potentially perform better with respect to energy loss under such unbalanced parasitics when compared to the 6.5 kV Si-IGBT/Si-PiN diode; however, as mentioned before in case of the hybrid power module, a possible rearrangement of IGBT chips inside power module, resulting in minimization of kelvin-emitter inductance unbalance, may be needed to even out current distribution for reliable operation. A close look at turn-off energy loss for the two-pulse switching test has revealed that both power modules show similar losses.

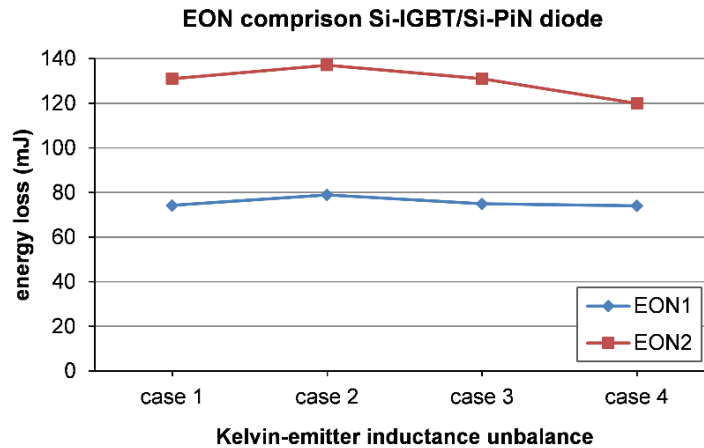


Figure 145 Double-pulse turn-on energy loss (E_{on}) comparison of Si-IGBT/Si-PiN diode under unbalanced condition.

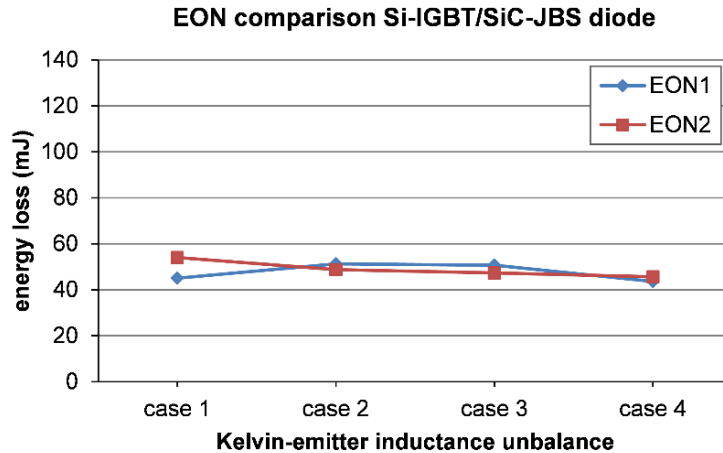


Figure 146 Double-pulse turn-on energy loss (Eon) comparison of Si-IGBT/SiC-JBS diode under unbalanced condition.

4.4 High Power Converter Design and Simulation

When designing power converter systems for space-limited applications, such as in shipboard and active mobile substation applications, many details have to be considered to meet the main design objectives of high power density (low weight and volume) and high efficiency. Different power losses occur within the power converter, and it is the thermal management and cooling system design that ultimately sets the physical limits of the design and the maximum deliverable output power. In this regard, proper selection of the following greatly affects the outcome of the design:

- Power semiconductor technology, type and rating (blocking voltage and turn-off current)
- Power converter topology (two-level or multi-level)

- Power converter switching frequency
- Power converter control and modulation (hard-switching and soft-switching)
- Power converter design layout (parasitics and stray inductances)

In this section, high power medium-voltage three-level neutral-point-clamped (3L-NPC) converters, topology of which is shown in Figure 147, are designed and simulated using: (a) 6.5 kV/100A Si-IGBT/Si-PiN diode, (b) 6.5 kV/100A Si-IGBT/SiC-JBS diode, and (c) 10 kV/100A SiC-MOSFET/SiC-JBS diode. In section 4.4.1, NPC-based power converter design methodology for medium-voltage SPS application is presented and simulation results are used to analyze power losses and efficiency; in section 4.4.2, NPC-based power conversion efficiency simulation results for high voltage AMS application is presented. Finally, power switch thermal limit consideration and switching frequency capability of power converters are discussed in section 4.4.1.

4.4.1 Power Conversion for Shipboard Application

In the proposed next generation medium-voltage dc power system for shipboard application, there is a multi-MW front-end converter that converts the ac power generated by ship's power plant into medium-voltage dc. This is then, through other power converter units, converted to the required ac or dc form of electricity to be used by ship's electric propulsion and high energy mission and service type of loads. A NPC-based circuit topology, as depicted in Figure 147, is selected for the main power conversion unit. This converter is especially advantageous because of its three-level topology that allows each power switch to block only half of total dc-link voltage. Based on selection of power semiconductor

technologies considered in this paper, four NPC-based converters are designed that can be divided into two groups based on the medium-voltage dc-link voltage of 7.5 kV or 15 kV. Table 40 shows the converter designs that are considered for medium-voltage shipboard power system application.

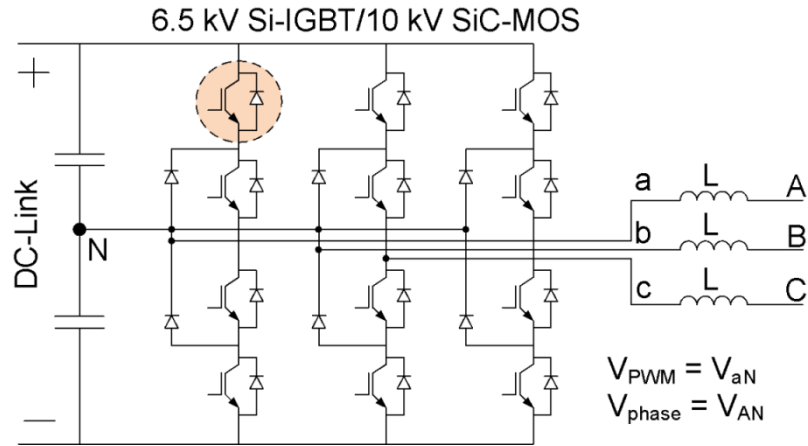


Figure 147 Three-level neutral-point-clamped (3L-NPC) converter circuit topology.

Table 40 3L-NPC converter designs for medium-voltage shipboard power system application

Converter	Power module	DC-link (kV)	Vout (kV)
3L-NPC1	6.5 kV/100A Si-IGBT/ Si-PiN diode	7.5	4.16
3L-NPC2	6.5 kV/100A Si-IGBT/ SiC-JBS diode	7.5	4.16
3L-NPC3	10 kV/100A SiC-MOS/ SiC-JBS diode	7.5	4.16
3L-NPC4		15	8.33

An important and practical safety design factor for hard-switching power converters is the voltage safety design factor ($K_{v,sf}$) defined as the ratio of forward blocking-voltage to half of the total dc-link voltage:

$$K_{v,sf} = \frac{V_{FW-BD}}{\frac{V_{DC}}{2}} \quad (4-1)$$

where V_{FW-BD} (V) is the forward breakdown voltage of the power switch, and V_{DC} (V) is the total dc-link voltage. This safety design factor must be greater than one to account for over-voltages caused by stray inductances in the circuit. Moreover, each power switch in the converter is modulated using a three-level carrier-based sinusoidal pulse-width-modulation (SPWM) technique. For that reason, the output voltage is related to dc-link voltage as in the following:

$$V_{AB} = \frac{\sqrt{3} \cdot m \cdot V_{DC}}{2 \sqrt{2}} \quad (4-2)$$

where V_{AB} (V) is rms value of fundamental output line-to-line voltage in Figure 147, and m is the converter modulation index. Maximum modulation index value for SPWM is 1 ($m = 1$); however, in certain modulation schemes such as SPWM with 3rd-harmonic injection and Space-Vector-Modulation (SVM), it can be increased to 1.15 ($m = 1.15$). On the other hand, each power switch can only conduct a maximum half-cycle of the total output sinusoidal current; thus, the rated output current of power converter is obtained in terms of the switch current as:

$$I_A = \frac{2 \cdot K_{i,sf} \cdot I_F}{\sqrt{2}} \quad (4-3)$$

where $I_A(A)$ is rms value of fundamental output line current in Figure 147, $K_{i,sf}$ is the current safety design factor, and $I_F(A)$ is the rated continuous forward dc current of the switch. The current safety design factor is less than 1, and is determined by comparing switching transients against safe operating area (SOA) of the switch. The output power of the converter can be defined as follows:

$$P_{out} = \sqrt{3} \cdot V_{AB} I_A \cdot PF \quad (4-4)$$

where PF is the output power factor. Assuming a unity power factor mode of operation ($PF = 1$) and substituting for (4-4) from (4-1)-(4-3), the rated output power is obtained as in (4-5):

$$P_{out-rated} = \frac{3 \cdot m \cdot K_{i,sf} \cdot I_F \cdot V_{FW-BD}}{K_{v,sf}} \quad (4-5)$$

where $P_{out-rated}(W)$ is the converter rated output power. Equation (4-5) relates rated output power, directly, to voltage and current rating of the power device, and indirectly, to SOA boundary of the power device through safety design factors.

The goal is to design converter units that can deliver at least 1 MW nominal power utilizing the 100 A power modules; thus, only the number of power modules in parallel per converter switch and current safety design factor need to be determined since all the other variables in (4-5) are known. This is done through SOA analysis of switching I-V curves of 100 A power modules in each 3L-NPC converter design. Figure 148 shows switching I-V

curves for converters at 5 kHz switching frequency, approximately 500 kW output power for NPC1-3 and 1 MW output power for NPC4. For all converter designs, the voltage spikes at turn-off are well inside the SOA; however, current spikes need to be carefully examined. During turn-on, current spike for NPC1 is considerably larger than other converters and it also slightly exceeds the SOA boundary; current spikes for NPC2-NPC4, even though inside SOA, indicate that $K_{i,sf}$ must be carefully chosen for each converter to achieve the required power rating. The switching I-V curves also show that 2x100 A power modules in parallel should be deployed per power switch in all power converters. Table 41 summarizes the final converter design specifications and resultant rated output power.

Circuit simulations of all converters, using SPICE-based circuit models of the power device modules, are carried out in SIMetrix/SIMPLIS advanced SPICE circuit simulator [76]. Figure 149 shows one converter leg implementation of the NPC converter circuit, as shown in Figure 147, including stray and dc-link inductances.

Table 41 Converter design specifications and rated output power

➤ Number of 100A modules in parallel = 2 ($I_F = 2 \times 100$ A) ➤ Maximum modulation index = 0.905 ($m = 0.905$)				
Converter	V_{FW-BD} (kV)	$K_{v,sf}$	$K_{i,sf}$	P_{rated} (MW)
3L-NPC1	6.5	1.73	0.50	1.0
3L-NPC2			0.75	1.5
3L-NPC3	10	2.66	0.80	1.6
3L-NPC4			1.33	0.60

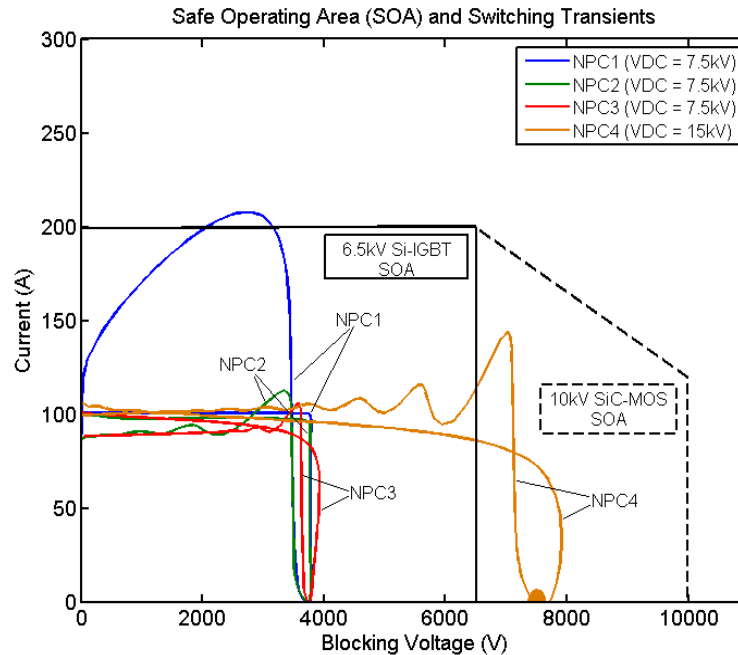


Figure 148 SOA of 100 A power modules and switching I-V curves at $f_{sw} = 5$ kHz and P_{out} approximately 500 kW for NPC1-3 and 1 MW for NPC4.

The output inductors are chosen to achieve a peak-to-peak output current ripple of 26 A ($\Delta i_{pp} = 26 A$) at peak current and maximum modulation index. Because converter simulations are carried out at 1 kHz, 5 kHz and 10 kHz switching frequencies, the value of inductor (L) per output ac phase is chosen to be 10 mH, 2.8 mH and 1.7 mH for each switching frequency, respectively. The gate-drive voltage has a 0-20 V pulse pattern. For the IGBT-based converters, gate resistance is 12 ohms, and for MOSFET-based converters, gate resistance is 5 ohms. This is due to the fact that input gate capacitance is 12 nF for the IGBT and is 31 nF for the MOSFET. Figure 150 shows half-cycle output waveforms of the 3L-NPC at switching frequency of 5 kHz and modulation index (m) of 0.905.

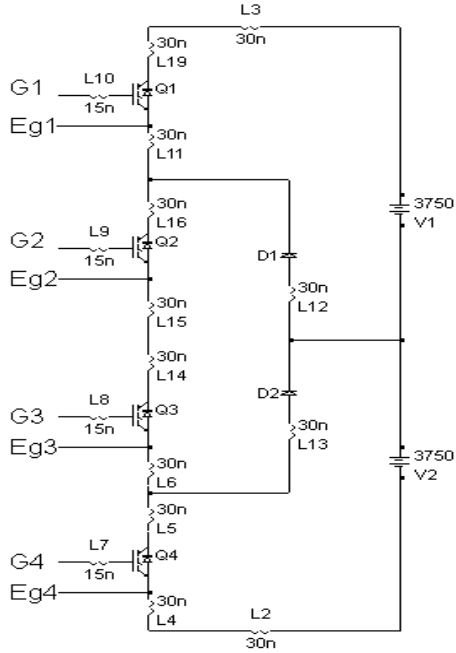


Figure 149 NPC converter leg implementation including different stray and dc-link inductances.

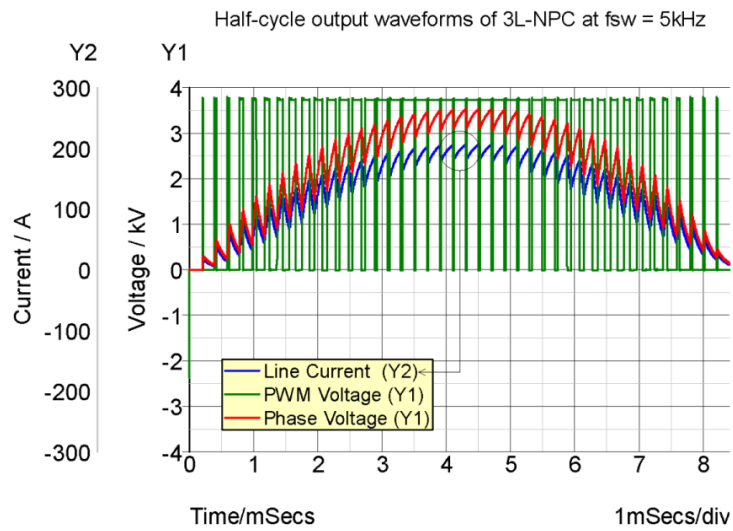


Figure 150 Half-cycle simulation waveforms of 3L-NPC at $f_{sw} = 5\text{ kHz}$.

Figure 151 to Figure 153 show percentages of turn-on and turn-off switching power losses, conduction power loss, parasitic power loss and efficiency for all converters at 1 kHz, 5 kHz and 10 kHz switching frequency, respectively. From those figures, it can be seen for NPC1, with 6.5 kV/100A Si-IGBT/Si-PiN diode power switch, that both switching and conduction power losses are major loss components at 1 kHz, whereas at 5 kHz and 10 kHz, switching power loss becomes dominant with turn-on loss making the major portion. For NPC2, with 6.5 kV/100A Si-IGBT/SiC-JBS diode power switch, switching and conduction are major power losses at 1 kHz, whereas at 5 kHz and 10 kHz switching frequencies, switching power loss is dominant with major turn-off loss share. For NPC3, with 10 kV/100A SiC-MOSFET/SiC-JBS diode power switch, conduction power loss is always important; however, as switching frequency increases to 5 kHz and 10 kHz, turn-on switching loss prevails, whereas turn-off loss remains almost negligible. For NPC4, with the same power switch as in latter, turn-on loss is always the main loss component and shares a significant portion of total power loss as switching frequency is increased.

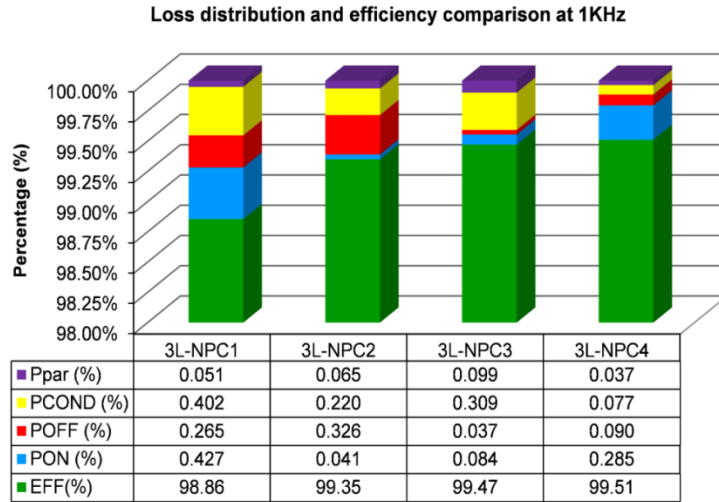


Figure 151 Power loss distribution and efficiency percentage comparison at 1 kHz switching frequency and output power of 1 MW.

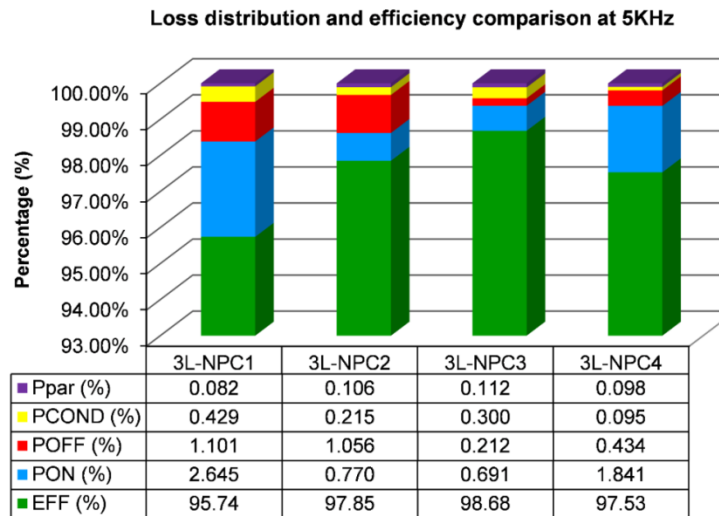


Figure 152 Power loss distribution and efficiency percentage comparison at 5 kHz switching frequency and output power of 995 kW.

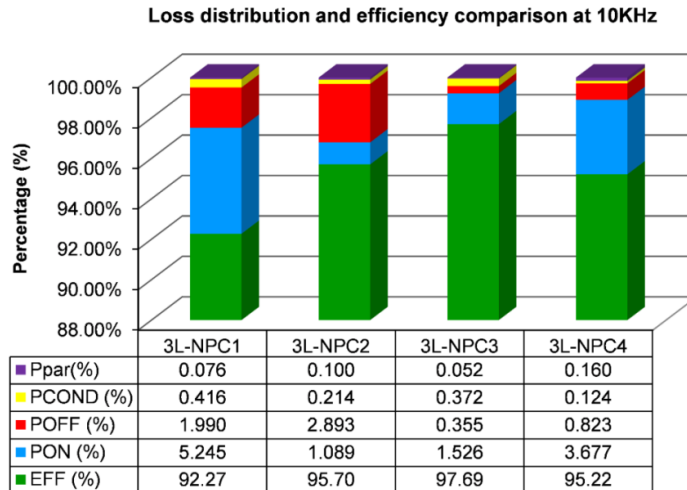


Figure 153 Power loss distribution and efficiency percentage comparison at 10 kHz switching frequency and output power of 986 kW.

Figure 154 shows turn-on loss percentage curves for converters. It can be seen that NPC1 has a fast increasing turn-on power loss that is also the highest among all. This is mainly because of losses induced by large reverse recovery phenomenon that occurs at turn-off of 6.5 kV Si-PiN diode. Power converters NPC2 and NPC3 possess very low turn-on losses, and NPC2 has the lowest turn-on loss of all at 10 kHz switching frequency. Converter NPC4 has nearly double the turn-on loss of NPC3 at 10 kHz; that is due to surge effect and double voltage stress caused by double dc-link voltage.

Figure 155 shows turn-off loss percentage curves for converters. Comparison of curves for NPC3 and NPC4 shows that both have really low turn-off loss, which is due to 10 kV SiC MOSFET technology. This is especially beneficial at higher switching frequencies (> 5 kHz)

compared to NPC2 converter where, at switching frequencies greater than 5 kHz, turn-off loss becomes the major switching loss.

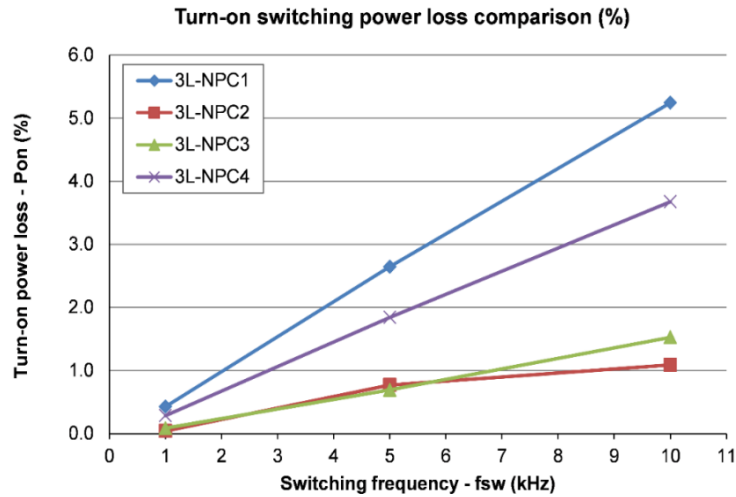


Figure 154 Turn-on power loss percentage curves for 3L-NPC converters.

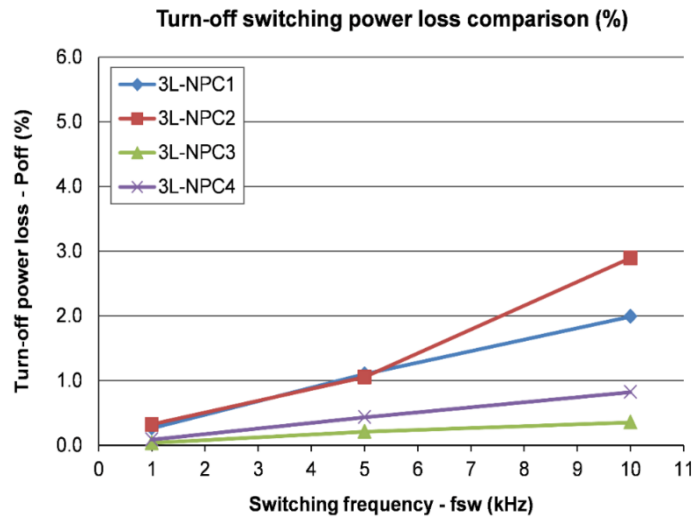


Figure 155 Turn-off power loss percentage curves for 3L-NPC converters.

Figure 156 shows efficiency percentage curves for converters. It is seen that NPC3 has the highest efficiency performance, and therefore, it is always an option especially at higher switching frequencies (> 5 kHz) where it would clearly perform better than other converters. However, from efficiency point of view, NPC2 and NPC4 are also strong candidates up to 5 kHz switching frequency.

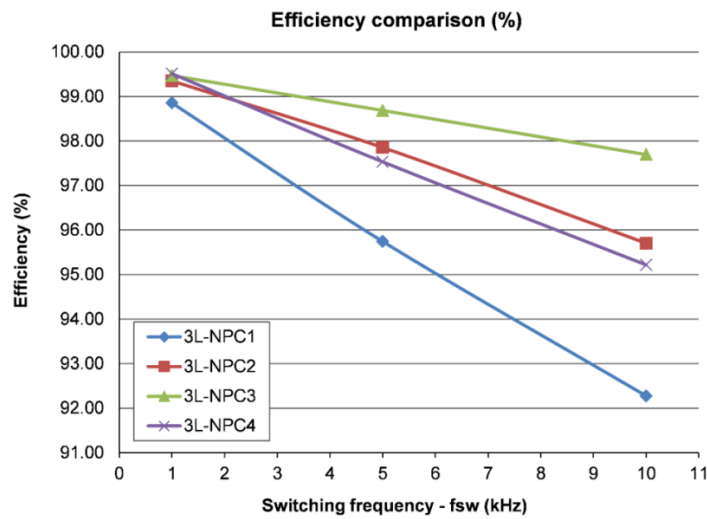


Figure 156 Efficiency percentage curves for 3L-NPC converters.

4.4.2 Power Conversion for Active Mobile Substation (AMS)

Mobile substations are used in power system to temporarily replace/bypass the main substation in case of damage or required maintenance of the high voltage power transformer. On the other hand, an *active* mobile substation (AMS) is a 20-40 MVA transmission-level (69 kV/138-245 kV) power electronics integrated solution that functions as a power router under normal conditions and as a recovery transformer under contingencies [63], [64]. The

main building block in the system is a mega-watt range NPC-based AC/AC modular transformer converter (MTC) [63]. This converter system is considered for power loss and efficiency analysis as a very high power application of NPC-based converter systems. The voltage-sourced converter (VSC) can be controlled using PWM vector-control method ($f_{sw} \sim 540 \text{ Hz} - 1 \text{ kHz}$) and/or angle-control method ($f_{sw} = 50/60\text{Hz}$). To achieve the same THD performance, vector-controlled VSCs need to operate at much higher switching frequencies than ac line frequency. Since efficiency is a key factor in the transportability of the AMS, power loss and efficiency calculations are carried out using SPICE circuit simulation of the 6.5 kV Si-IGBT/Si-PiN diode and 6.5 kV Si-IGBT/SiC-JBS diode power devices for three different control strategies: (1) angle control (60 Hz), (2) hybrid control [63] (540 Hz and 1 kHz), and (3) vector control (540 Hz and 1 kHz). The maximum switching frequency of 1 kHz is chosen due to very high voltage and high power considerations in the system. Figure 157 shows full comparative illustration of power loss distribution and efficiency results of AMS converter system for the aforementioned control methods at different switching frequencies. It can be seen that regardless of the choice of semiconductor technology, the vector-control strategy results in lower converter efficiency due to higher switching frequency application. Further analysis of the results reveals that 6.5 kV Si-IGBT/SiC-JBS diode hybrid power module compared to 6.5 kV Si-IGBT/Si-PiN diode power module, has a better efficiency performance at both high (1 kHz in AMS application) and low (60 Hz) switching frequencies.

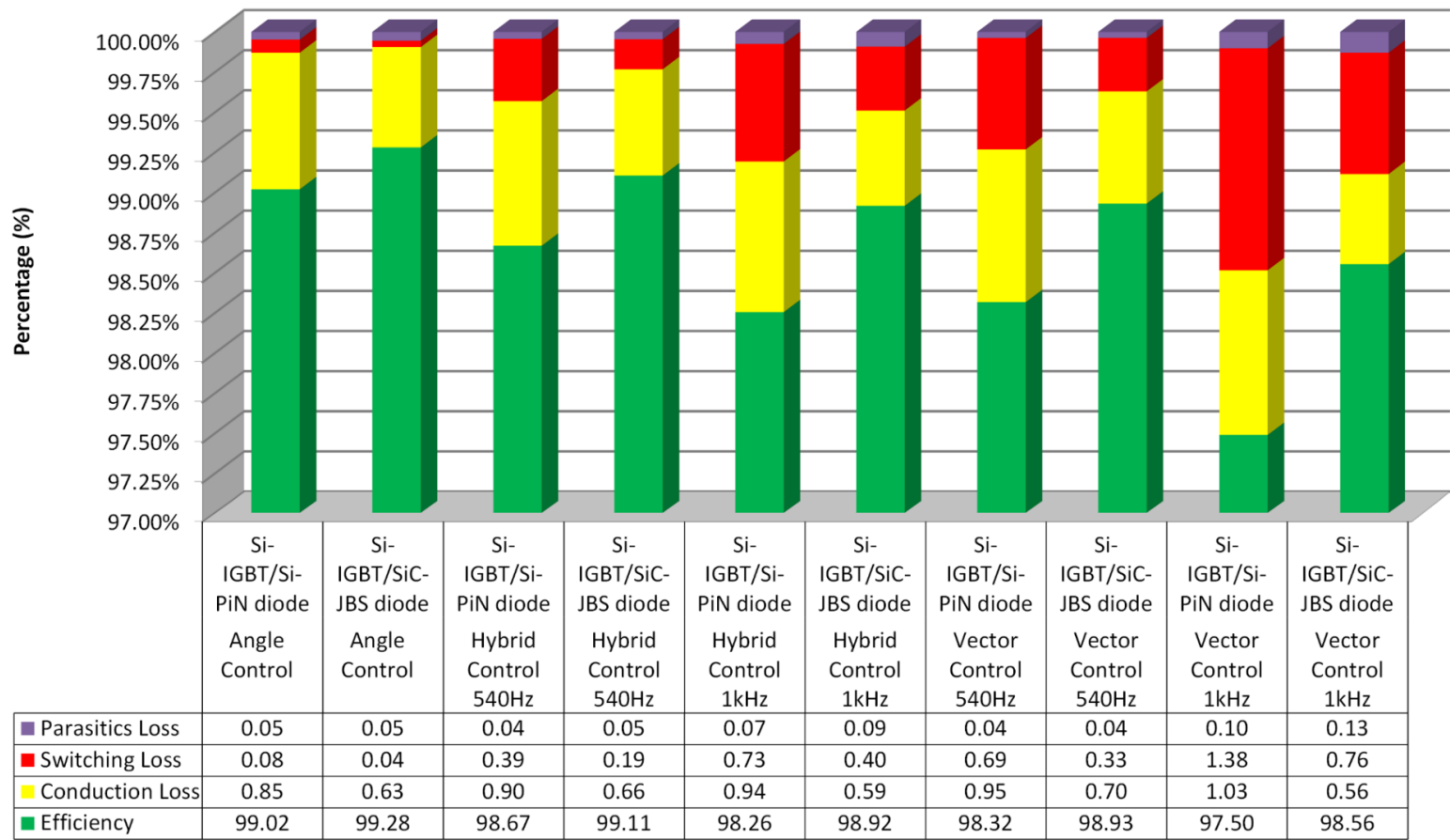


Figure 157 Efficiency and power loss comparison of NPC-based AC/AC power converters for AMS application.

4.4.1 Thermal Limit and Switching Frequency Capability of Power Converters

The output power of a converter is proportional to power loss density (P_{loss}) of the power switch, which is defined as:

$$P_{loss} = \frac{T_j - T_a}{R_{th,ja}} \quad (4-6)$$

where T_j (K) is the junction temperature, T_a (K) is the ambient temperature, and $R_{th,ja}$ (K/W.cm²) is the junction to ambient thermal resistance. Different losses in power converter increase the power semiconductor junction temperature (T_j) and thus, the maximum deliverable output power is ultimately limited by maximum junction temperature ($T_{j,max}$) of power device and cooling system design. Semiconductor physics and device reliability issues limit $T_{j,max}$ to 400° K for Si-based power switches, whereas SiC-based power switches can potentially operate at much higher maximum junction temperatures, i.e. 500° K. This is very advantageous for SiC-based converters since the maximum deliverable output power can be proportionally increased for the same switching frequency as compared to Si-based power converters. Unfortunately, the current insulated packaging technology sets the thermal limit for both Si- and SiC-based devices at $T_j = 400^\circ$ K [81]. For a thermal resistance of 0.33 K/W.cm² ($R_{th,ja} = 0.33$), the maximum power loss density for all converters is 300 W/cm². Figure 158 shows switching power loss density for all converters versus the current and future thermal limit of insulated housing technology. It can be concluded that, at rated output power, NPC1 converter is capable to operate up to about 2 kHz switching frequency; NPC2 and NPC3 are capable to operate up to 5 kHz switching frequency, and NPC4 is capable to operate well up to 10 kHz switching frequency. If the converters are required to

operate beyond their switching frequency capability, the nominal output power has to be de-rated as a fraction of total rated power with respect to switching frequency. Figure 159 shows output power de-rating curves for all converter designs.

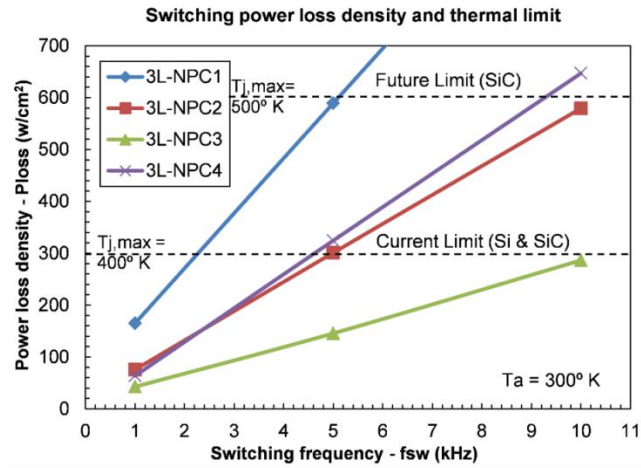


Figure 158 Switching power loss density of 3L-NPC power converters versus thermal limit of power switches.

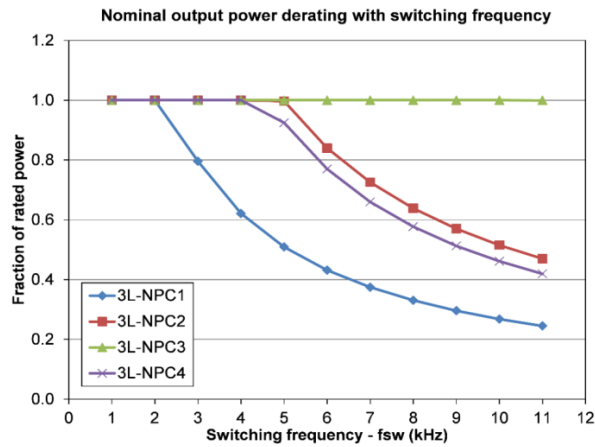


Figure 159 Nominal output power de-rating curves considering power converter frequency capability and power device thermal limit.

4.5 Conclusion

This chapter presents a comparative design study of high power medium-voltage three-level neutral-point-clamped (3L-NPC) converters based on three device technologies: (1) 6.5 kV Si-IGBT with Si-PiN anti-parallel diode, (2) 6.5 kV Si-IGBT co-packed with 6.5 kV SiC-JBS anti-parallel diode, and (3) 10 kV SiC-MOSFET with 10 kV SiC-JBS diode. SPICE-based circuit models for dies of these power semiconductor devices are used to create 100 A power module models, which includes parasitic inductances, to investigate switching characteristics. It is shown that 6.5 kV Si-IGBT/SiC-JBS diode has a better switching energy loss performance than 6.5 kV Si-IGBT/Si-PiN diode, especially at higher switching speeds and lower gate resistances, due to prevention of reverse recovery induced loss mechanisms. It is also shown that 10 kV SiC-MOSFET/SiC-JBS diode has a better efficiency performance at higher switching frequencies compared to both Si-IGBT power devices, due to really low turn-off energy loss of MOSFET. A practical power converter design methodology based on switching I-V curves and power device SOA is presented. Complete comparative power loss distribution and efficiency analysis of power converters at different switching frequencies is presented for shipboard and AMS applications. Switching frequency capability curves of power converters versus power device thermal limit and also, output power de-rating curves of power converters beyond nominal switching frequency are presented. It is shown that the Si-IGBT/Si-PiN diode module's efficiency performance degrades remarkably with increasing switching frequency, whereas the Si-IGBT/SiC-JBS diode hybrid module retains high efficiency performance up to 5 kHz; hence, it is a strong candidate for medium-voltage

mega-watt high power converters. The SiC-MOSFET/SiC-JBS diode remains an option for higher switching frequency (5-10 kHz) high power converters.

Chapter 5 Conclusion and Future Work

In chapter 2, the issues in current MVDC system such as low front-end rectifier bandwidth, rectifier/load interactions, and emerging loads of very varying nature, it was shown that there is need to increase dc-link inertia and provide adequate damping during disturbances. The dc active power filter method was proposed to alleviate the problem. These active filters can be implemented in a number of different topologies of either pure -w/o passive filter- and/or hybrid – w/ passive filter- type. Each dc active filter is coupled to dc-link using coupling mechanism. They can also be part of an integrated MVDC amplifier system design.

Furthermore, this chapter introduces the concept and presents the specification of a medium-voltage DC amplifier for DC shipboard power system studies. Basic requirements of the MVDC amplifier are derived and possible circuit topologies to implement the MVDC amplifier with the required voltage and power rating are reviewed. A multi-pulse thyristor-bridge front-end amplifier system incorporating a series dc active filter is proposed to meet the steady-state and dynamic performance requirements of the system. Proposed amplifier system control components design and their impact on system dynamics studied and verified by simulations. The impact of dc active power filter control and firing angle quantization on amplifier's steady-state and transient behavior are presented. This study provides the design and evaluation required towards a prototype testbed for MVDC amplifier system concept.

Finally, some design issues of a medium-voltage DC (MVDC) amplifier system based on a multi-pulse thyristor front-end technology was presented. Understanding the direct

influence of the firing angle dynamics on the overall amplifier dynamics, a general purpose firing pulse generator has been characterized and key observations with regard to firing angle dynamic, sampling and quantization has been made. It is shown that the firing angle dynamic slows down the system and makes it impossible to meet the amplifier dynamic specification. In order to achieve the target MVDC amplifier dynamic, a new compensation method for the series dc active filter is proposed and the required active filter rating is simulated. The preliminary steady-state and dynamic results of a laboratory-scale implementation of a 12kVA/400V dc amplifier test-bed are presented. It is seen that the sizing of the active filter is driven by step-down dynamic response of the system. Further improvements of the test-bed to meet the full system specification requirements are considered for future research. This chapter has culminated in research papers [11][39][41][43].

In chapter 3, a new front-end topology for large mobile mining machines is proposed. The new front-end which is a hybrid topology of 12-pulse thyristor-bridge and IGBT-based active power filter is, thus, called ‘hybrid front-end’ (HFE). It is explained how the simple, reliable, efficient and mature technology of high power thyristors when combined with highly-controllable IGBT switches in HFE enables more power dense and larger equipment by reducing the number of components in the system and easier integration of energy storage by providing more controllability. The steady-state and dynamic simulation results of the system are presented. Furthermore, a 3-ph/208-Vac, 550-Vdc, 12-kVA laboratory-scale HFE test-bed circuit is proposed, developed and tested in FREEDM Systems Center. A proposed digital control system is presented for HFE which allows configuring the system for harmonics-only mode (just compensating harmonic distortion of current) or harmonics-and-

VAR-support mode (compensating both harmonic distortion of current and providing partial VAR support). Complete experimental results for both operational modes are presented at DC-bus voltage of 450 V and different load operating points. It is shown that in harmonics-only mode the active power filter requires only 2-3% of total system rating to perform harmonic compensation. It is shown that the system has a promising performance in reducing total harmonic distortion (THD) of current with the current test-bed predicted to achieve less than 8 % of THD at full-load condition. Moreover, efficiency measurements of the system verify high efficiency performance of the system by predicting total efficiency at full-load to be higher of 94%. Finally, the experimental results for harmonics-and-VAR-support compensation mode are presented at output power 4 kW (0.33 PU). Partial VAR support in the system is validated through improving lagging power factor (PF) at input of HFE; and furthermore, unity PF operation of the system is demonstrated. This chapter has culminated in research papers [51][58].

Finally, chapter 4 presents a comparative design study of high power medium-voltage three-level neutral-point-clamped (3L-NPC) converters based on three device technologies: (1) 6.5 kV Si-IGBT with Si-PiN anti-parallel diode, (2) 6.5 kV Si-IGBT co-packed with 6.5 kV SiC-JBS anti-parallel diode, and (3) 10 kV SiC-MOSFET with 10 kV SiC-JBS diode. SPICE-based circuit models for dies of these power semiconductor devices are used to create 100 A power module models, which includes parasitic inductances, to investigate switching characteristics. It is shown that 6.5 kV Si-IGBT/SiC-JBS diode has a better switching energy loss performance than 6.5 kV Si-IGBT/Si-PiN diode, especially at higher switching speeds and lower gate resistances, due to prevention of reverse recovery induced loss mechanisms. It

is also shown that 10 kV SiC-MOSFET/SiC-JBS diode has a better efficiency performance at higher switching frequencies compared to both Si-IGBT power devices, due to really low turn-off energy loss of MOSFET. A practical power converter design methodology based on switching I-V curves and power device SOA is presented. Complete comparative power loss distribution and efficiency analysis of power converters at different switching frequencies is presented for shipboard and AMS applications. Switching frequency capability curves of power converters versus power device thermal limit and also, output power de-rating curves of power converters beyond nominal switching frequency are presented. It is shown that the Si-IGBT/Si-PiN diode module's efficiency performance degrades remarkably with increasing switching frequency, whereas the Si-IGBT/SiC-JBS diode hybrid module retains high efficiency performance up to 5 kHz; hence, it is a strong candidate for medium-voltage mega-watt high power converters. The SiC-MOSFET/SiC-JBS diode remains an option for higher switching frequency (5-10 kHz) high power converters. This chapter has culminated in research papers [9][71].

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