Abstract

Mattos, Leonardo Serra. The EvBot II: An Enhanced Evolutionary Robotics Platform Equipped with Integrated Sensing for Control. (Under the direction of Edward Grant.)

The research presented in this thesis describes the design and development of the EvBot II, a small, computationally powerful, and robust evolutionary robotics platform equipped with an acoustic array system. The EvBot II represents the next generation of autonomous robots for distributed robot-colony research, and its design has expanded the sensing capabilities and the overall performance of the EvBot robots by the incorporation of two microcontroller units, shaft encoders and a complete acoustic array system for tracking and navigation purposes. The design, development and test of this new robot is described in detail throughout this thesis, including the design of an USB data acquisition system capable of simultaneously sampling eight audio channels as required for the realization of the added acoustic array system. Experiments designed to evaluate the performance of this new robot and its components are also described in this thesis, as well as experimental results showing that it is a well-suited platform for the study of evolutionary robotics, distributed robot-colonies and sensors technologies.

THE EVBOT II
AN ENHANCED EVOLUTIONARY ROBOTICS PLATFORM EQUIPPED WITH INTEGRATED SENSING FOR CONTROL

by

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Biography

Leonardo Serra de Mattos was born December 17, 1974 in Red Bank, New Jersey, and shortly after moved to Brazil with his family. From education received there he earned his Technical degree in Electronics from the State University of Campinas (UNICAMP) in 1992, and a Bachelor of Science degree in Electrical Engineering from the University of São Paulo (USP) in 1998. Once again living in the United States, he received his Master of Science degree in Electrical Engineering from the North Carolina State University in 2003. Leonardo is a member of the IEEE society.

Acknowledgments

I wish to thank my wife Daniela and my parents José Carlos and Theresinha for their love, long support and patience. Together with my brothers and sisters and the rest of my family, they are the ones that give me the strength to grow and always try to do my best.

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List of Abbreviations

ADC = Analog to Digital Converter

AI = Artificial Intelligence

ATA = Advanced Technology bus Attachment

CRIM = Center for Robotics and Intelligent Machines

DIP = Dual Inline Package

DOC = DiskOnChip

GPS = Global Positioning System

GUI = Graphical User Interface

I/O = Input/Output

IEEE = Institute of Electrical and Electronics Engineers

MCU = Microprocessor Control Unit / microcontroller

NCSU = North Carolina State University / NC State

PCB = Printed Circuit Board

PCMCIA = Personal Computer Memory Card International Association

PnP = Plug-and-Play

PWM = Pulse Width Modulation

RF = Radio Frequency

RSTA = Reconnaissance, Surveillance and Target Acquisition

SAR = Search and Rescue

SDRAM = Synchronous Dynamic Random Access Memory

SONAR = Sound Navigation and Ranging

UGS = Unattended Ground Sensors

USB = Universal Serial Bus

Chapter 1 – Introduction

Researchers in the areas of distributed and evolvable robotics have recently started to use physical platforms to validate concepts developed in simulation, but one of the problems that they have been facing is to overcome limitations imposed by unsuited robotic systems. We believe that the current need in this area is for robot platforms that are small enough to be used within research laboratories, yet robust and computationally power enough to implement complex machine-learned controllers in the real world. The EvBot robots were developed to bridge the gap that exists between cumbersome commercial platforms featuring powerful central processing units (CPUs) and extensive sensing capabilities, and small inexpensive robots with limited capabilities. The original EvBot measures only eight inches in diameter and is an autonomous system equipped with a Pentium class microcomputer system. This robot has proven to be an extremely useful platform for advanced experimentation in robot colony behaviors and evolutionary robotics, but experimentation also indicated that the original EvBot platform still needed additional sensor capabilities to improve position and velocity control. The research reported upon in this thesis concentrates on specifying the design of, and the implementation of, an improved and flexible hardware architecture for hosting and integrating data from a variety of sensor types, such as vision, sound and position. The end result is the EvBot II robot, a platform with the improved position and velocity accuracy that is required for interacting

robots acting as part of a colony. To support this effort, circuitry was designed to enable the incorporation of shaft encoders and the closed loop control of up to three motors. A USB hub was also introduced to allow uncomplicated incorporation of extra sensors if and when such sensors are required. The USB hub allows "plug and play" sensor addition, and was used for the integration of an acoustic array system specially developed for this robot. The development of the mentioned acoustic array system was the second major focus of the research described in this thesis, and it involved the design of a custom data acquisition system (the USB-DAQ8) and several associated software programs. The EvBot II autonomous robot that emerged from this research work extends the possible application areas of EvBots, e.g., evolutionary and distributed robotics to undertake surveillance, reconnaissance and security applications. Experimentation with the EvBot II robotic platform demonstrated that, in addition to be completely compatible with the original EvBot, it is able to make successful use of the shaft encoders to control its traveling speed. Experiments also confirmed that the developed data acquisition system can effectively perform the simultaneous sampling of eight audio channels at a rate of 9600 samples per second per channel, thus successfully enabling the use of the acoustic array system for tracking and navigation purposes.

Section 1.1 – Thesis Outline

The design and development of the EvBot II platform and its custom acoustic array system are described in this thesis. Chapter 2 presents a review of the literature, including a summary of autonomous robots currently in use in the areas of distributed and evolutionary robotics, and an overview of past and current research focused on the use of acoustics by mobile robots. The development of the new hardware and software for the EvBot II, including the design of the encoder systems and the new circuitry to drive the motor, is presented in Chapter 3. The following chapter presents an introduction to acoustic arrays and describes software developed for simulation and use on such systems. Chapter 5 provides an in depth description of the data acquisition system USB-DAQ8, which was developed to realize the acoustic array. The experimental results from tests of the robot platform and acoustic array system are presented in Chapter 6. Lastly, Chapter 7 presents some ideas for further improvements of the EvBot platform, as well as ideas for future experiments with the robot.

Section 1.2 – Thesis Goals

The objectives of this thesis are to describe the:

- Design and construction of the EvBot II, a small but computationally powerful autonomous robot created as an enhanced version of the original EvBot.
- Development of the software used to design and make use of the acoustic array system implemented on the EvBot II.
- Design of the USB-DAQ8, a data acquisition system custom developed to realize the EvBot's acoustic array system.
- Demonstration of the robot's enhanced performance and use of the acoustic array system for tracking and navigation.

Chapter 2 – Literature Review

The concept of robots is a very old one in our society and has always been related to automatic machines that can perform tasks in the manner of a human. Although their history is frequently said to have started around 270 BC with the water clocks and organs made by the Greek engineer Ctesibus, it was only in the early 1920's that term "robot" appeared. It was introduced by the Czech writer Karel Capek, who derived the term from the Czechoslovakian word for slave (robotnik) and used it in the play "Rossum's Universal Robots".

From the beginnings, one of the main functions of robots in our society has been to free humans from repetitive, difficult or harmful tasks. Industrial robots were the first ones to appear in large scale and, since their first demonstration in 1959 by the M.I.T. Servomechanisms Lab, they have been improving the quality of life of humans across the globe. In recent times mobile robots have also started to be designed to help humans in a diverse quantity of tasks, from household work to exploration of hazardous environments. However, unlike industrial robots, mobile robots are required to have intelligence, the capability to adapt to different environments or tasks, and are also often required to be autonomous. Several examples of such robots can be found in the recent literature and the main uses include reconnaissance, surveillance and target acquisition (RSTA) for military forces

[4] [8], security monitoring [24] [27] [32] and search and rescue (SAR) in disaster areas [6] [23].

The first autonomous robots appeared in the research community in the early 1950's when the neurophysiologist W. Grey Walter [29] introduced his "Machina Speculatrix", which was a three wheeled vehicle equipped with a two vacuum tube analog computer. This robot had the tendency to wonder around exploring the environment and this was the first proof that intelligent and autonomous robots can evolve and develop practical functions. Though it was only it the late 1980s that researchers would expand that idea to groups of robots that evolve together, originating in what is now known as distributed robotics [10] [2] [1] [30]. About that same time the artificial intelligence (A.I.) research community was introduced to the subsumption architecture proposed by Rodney Brooks [3] and started using its essence to build physical platforms to realize and test intelligent systems that previously had only existed in simulations.

From the early work up to recent days, many of the physical autonomous robots developed to test evolvable and distributed systems were unsophisticated and carried little onboard processing, such as the common Kephera robot [35], which has been used by innumerous research groups as mentioned in [21]. Even though these robots proved to be very useful for research, their lack of processing power imposes limitations, so they often rely on an external computer for high-level processing when the implementation of complex controllers are desired [9] [15].

Recently autonomous robots with large processing capabilities have appeared in the distributed robotics literature, such as the Urban II and the ATRV-2 developed by iRobot Corporation and used by Hogg *et al.* [12] and Budulas *et al.* [4]. These robots use powerful hand-held computers for processing of sensor data and control, but are relatively large, heavy and expensive. Another example of a powerful robot is the RATLER, which is a medium-sized all-electric vehicle containing a PC104 stack for computation, control and sensing. The RATLER was originally developed at the Sandia National Laboratories as a prototype vehicle for lunar missions, and some of these robots are currently in distributed robotics research [8] [16].

Other research groups are experimenting with evolvable and distributed systems using small and inexpensive robots, like the GROWBOT from Parallax [39], which was used in the Idaho National Engineering and Environmental Laboratory (INEEL) by a research group working on large-scale micro-robotic forces [7]. Even with the limited processing power and limited sensorial capabilities provided by GROWBOT's Basic Stamp 2 microcontroller, the researchers were able to demonstrate evolution and interaction between robots.

The robot EvBot developed in the Center for Robotics and Intelligent Machines (CRIM) at the NC State University [11] fits well into the mid-range of autonomous robots being used for the study of evolvable systems. Although it has compatible processing power as most of the newest robots found in the literature, the CRIM's EvBot has the advantage of reduced size (twelve by ten inches) and low price (about $1400.00 for parts per unit). Similar to the RATLER and to the Koala

robots [35], the EvBot uses a PC104 stack equipped with a Pentium class processor, and it also features low power consumption, being able to continuously operate for more than two hours on a single 7.2V/3000mAh Ni-MH battery.

In general, it is seen that the research community in the area of distributed and evolvable robotics requires robotic platforms that allow the implementation of computationally complex controllers from a wealth of data. This is especially true when the robots are designed to leave the research laboratories and undertake "real-world" tasks. In the "real-world" the usefulness of such robots is usually directly proportional to the diversity of their onboard sensors, i.e. the larger the variety of sensors one robot has, the higher is the number of possible tasks it can perform, or the higher is the precision of the tasks it can perform. For that reason, this research area needs robot platforms whose architecture is open and expandable, thus providing a capability for the addition of new sensors as needed. Robots being developed for military applications, such as urban warfare, are very good examples of systems with these needs [16] [19]. They are usually required to have video camera, radar, GPS, RF transceivers and other specialized sensors, like chemical detectors or acoustic sensors.

Recently the researchers in the area of robotic RSTA started to revisit the acoustic field and the use of sound as tactical information has been regaining importance. This field started to become very popular by the end of the World War I, when the first sonar devices were developed to detect submarines. Since them the sonar technology has been greatly developed and along came the development of

acoustic arrays and related technologies, such as systems that perform spatial filtering by beamforming [28], target localization and classification [13] and estimation of sound source location [5] [18]. Acoustic array research is still active and producing knowledge, especially in the area of sensor array data processing [14] [25].

Recent trends in security and in RSTA are also bringing the attention back to passive acoustic array systems due to the fact that such systems can provide important strategic information without being easily detected. For that reason, acoustic array systems are being studied as part of RSTA robots [31] and as unattended ground sensors (UGS) [17].

In conclusion, it is seen that the research in the area of autonomous mobile robotics is growing substantially and strengthening in the area of distributed robotics. This is particularly the case where a team of robots may contribute cooperatively and overperform an individual robot. As a result, small and sophisticated robot platforms capable of carrying multiple sensors, implement complex controllers, and provide a wealth of data are being needed to support experimental tests.

Chapter 3 – The EvBot II Platform

The original Evolutionary Robots (EvBots) [11] have always performed well, but they needed more on-board sensors to increase their perception and control. For example, they needed the addition of shaft encoders to ensure closed-loop speed control. Without encoders it is not possible for the robot to perform precise movements, or move at a constant speed, or realize that it is not moving at all. Without shaft encoders each EvBot has to go through a difficult and time-consuming calibration process to ensure the robot controller makes precise decisions related to desired actions, e.g., turning a desired amount or moving at a desired speed.

So, the addition of shaft encoders became the first priority in the design of the new EvBot robot platform, the EvBot II. The encoders along with their associated circuitry were the first major design change initiated for expanding the robot colony. Because the EvBot II colony was to be based on the Radio Shack™ Bedlam product (see Figure 3.1), a certain amount of redesign was needed to its hardware, e.g., replacement of the driving motors and the removal of the extra gears. Only then could the new circuit design required for motor control and enhanced sensing be specified. To expand the connectivity of the original EvBot systems, a USB hub was also included on the EvBot II robot platform. Doing this ensured that the new system could implement a diverse number of commercially available or custom designed sensor systems, e.g., an acoustic array system that will be discussed later.

The specification and the design of all hardware and software for the new generation of EvBots will be fully described in the remaining sections of this chapter.

Section 3.1 – The EvBot II Base

The base used for the EvBot II came from the radio-controlled car Bedlam, from Radio Shack™. Driving the car showed that it operated at high speeds, using its tank-like traction system for forward and backward motion, and spins. However, this vehicle also includes a third axis that can provide transverse motion, which makes an interesting platform for studying the use of biologically inspired actions, subsumption architectures, and evolutionary robotics.

Figure 3.1: The Bedlam, used as the EvBot II base.

To create the new robot, the Bedlam platform was first striped of all unnecessary parts. It was reduced to its drive system, the motors and gear systems,

which were kept as the basis of the EvBot II platform. The shaft encoders were then installed in the base using a custom designed support (Figure 3.2) and the motor wire loom were extended to ensure that they would be able to connect to the newly designed driver board.

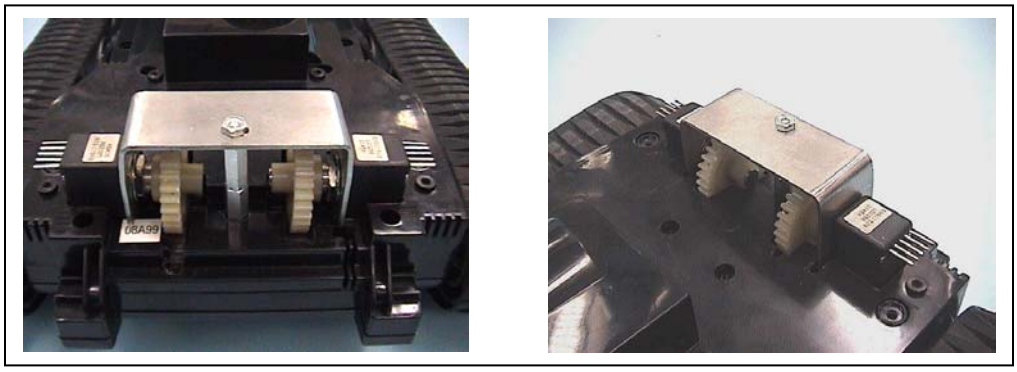


Figure 3.2: Encoders installed on the EvBot II base using a custom designed bracket.

After the changes to the mechanical drive system were made to the Bedlam vehicle, it now became the basis of the EvBot II robot platform. Speed control tests carried out with the Bedlam drive system showed that the original motors operated too fast for all practical purposes. It therefore became necessary to reduce the speed of the drive system, which the tests showed could not be solely achieved by simply reducing the motor's voltage. Because the radio-controlled car was design to move at high speed, the gearing does not provide a sufficient enough reduction to keep the motor in its operating range, particularly when the robot is required to move slowly. New motors having built-in reduction gears were specified to overcome this problem. The selected motor was the HS-300BB made by Hitec (Appendix A3.8). Once these were sourced and delivered, they were installed in the EvBot II platform. However,

they could not be installed without another design alteration being made to the Bedlam body. The final design of the bracket supported the drive motors and the encoders, and is shown in Figure 3.3.

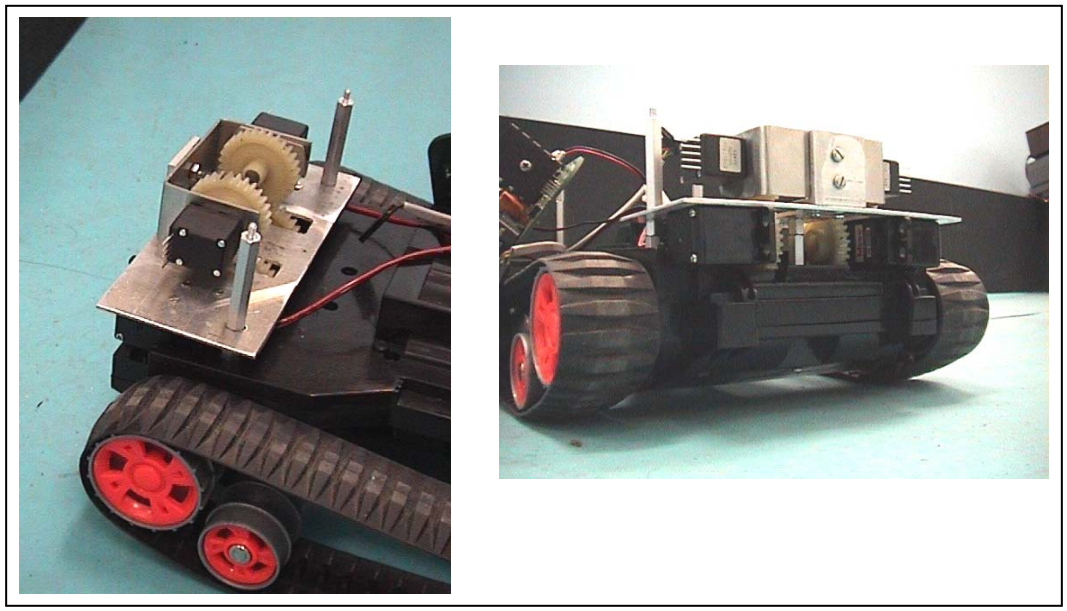


Figure 3.3: Motor-Encoder Assemblage.

Section 3.2 - The Encoder Circuitry

The addition of shaft encoders to each of the robot's motors required the development of dedicated hardware and software capable of handling the data from these two sensors. To achieve this, encoder circuitry was specially designed, tested and implemented on the new generation of EvBots. The design specification of the encoder circuitry is descried in this section.

The encoder circuit is based on the integrated circuit HCTL-2016 from Agilent, see the data sheet in Appendix A3.7. This integrated circuit (IC) is a quadrature decoder/counter set up to be directly controlled by a microcontroller chip, which in this case is the BasicX24. The data sheet of the HCTL-2016 shows that the chip outputs a 16-bit word to an 8-bit parallel bus. This is achieved by breaking the 16-bit word into two 8-bit bytes, i.e., a high byte and a low byte. The output byte is selected by control lines of the microcontroller, but due to the limited number of I/O pins on the BasicX a parallel to serial converter had to be employed to get the appropriate data control action. A shift register, IC MM74HC165, was selected for this task. Adopting this design means that only one control line is now required from the BasicX microcontroller.

The encoders selected for this application are the optical encoder ENS-1J-B28 from Bourn, see Appendix A3.6. This encoder provides a 2-bit gray code as output and its the maximum shaft speed is 3000 RPM. After the encoders, the only other required component for the new circuitry is a clock oscillator. This needs to be connected to the decoder and it should be fast enough to allow proper functioning of the system at the maximum desired speed. Given the maximum operating speed of the encoder, the selected clock oscillator was an ECS100AC, which is a 1.22MHz oscillator from ECS International Inc.

The BasicX microcontroller is equipped with internal timers and circuitry that is capable of driving two simultaneous pulse width modulation (PWM) outputs. However, two quadrature decoders are also needed to get feedback data from the two

shaft encoders on the EvBot platform. The final circuit design for the shaft encoders, see Figure 3.4, has the two shaft encoder systems working in parallel to ensure maximum operating efficiency.

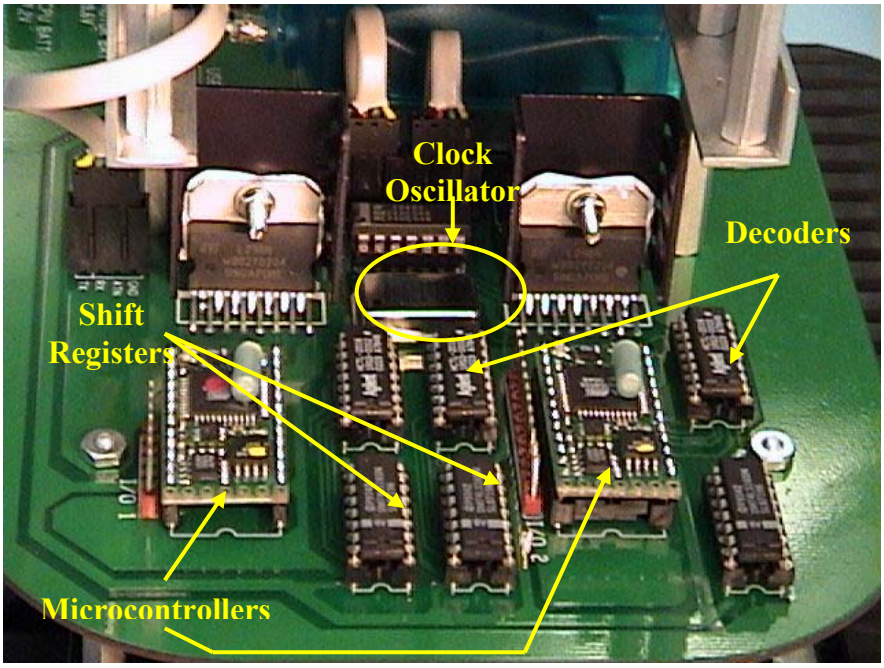


Figure 3.4: Encoder circuitry in the utility board.

Section 3.3 - The Motor Driver Circuitry

This part of the EvBot II system design deals with the speed control of a DC motor using pulse width modulation (PWM). The PWM signals, which are a train of square waves where the aspect ratio can be altered, are generated in the EvBot II by the BasicX microcontroller and are used to control the speed of the DC motors. By introducing an H-Bridge driver into the circuit for power amplification, power can be supplied to drive the DC motors and the control of forward/reverse direction of rotation of the motor is easily implemented.

To make use of the BasicX microcomputer's capability of producing two simultaneous PWM outputs, the Dual Full Bridge Driver L298 was selected. This is a compact but powerful IC capable of driving two DC motors with current up to 4A, see Appendix A3.9. Each of the two halves of the L298 driver has an enable pin and two input pins that can accept the TTL level signals produced by the BasicX. The input pins are used to select the direction of rotation and the enable pin receives the PWM pulses to determine the speed of rotation. The control sequence is shown in Table 3.1.

Table 3.1: Control signals for the motor driver L298.

Input 1	Input 2	Enable A	Motor
X	X	Low	Free running
High	Low	High	Turn clockwise
Low	High	High	Turn counter-clockwise
Low	Low	Illegal / Not Possible	
High	High		

To ensure that the signal on the Input 2 pin is always the inverted signal of the Input 1 pin, the inverter IC 7404 was used. DC motor back-EMF protection was also included in the circuit through the addition of the small signal Schottky diodes encapsulated on the IC UC3610 chip from Texas Instruments, see Appendix A3.10.

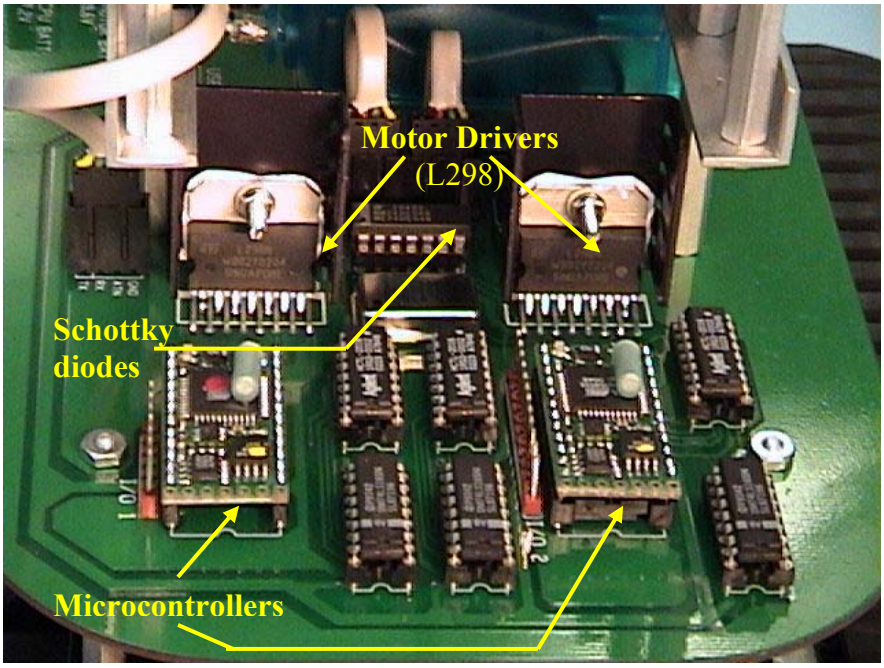


Figure 3.5: Motor driver circuit in the utility board.

Section 3.4 – Design of the Utility Printed Circuit Board

The utility board in the EvBot II integrates several functions. First, it is responsible for powering the PC/104 stack, which contains the central processing unit (CPU). Second, it is responsible for all interface connections, such as the mouse, keyboard, speaker, reset button and a USB port access to the CPU. Other than these utility functions, the board design also incorporates two BasicX microcontrollers and all the necessary circuitry for driving the DC motors and interfacing to the shaft encoders.

The utility board was designed to conform to the geometry of the Bedlam vehicle's base, to the extent that it uses the pre-existing holes in the vehicle for attachment. The board has two wiring layers and was drawn using the software CirCAD. Images of the CAD design of top and bottom layers of the utility board are shown in Figure 3.6 and Figure 3.7 respectively. Images of the top and bottom of the manufactured utility board are shown in Figure 3.8.

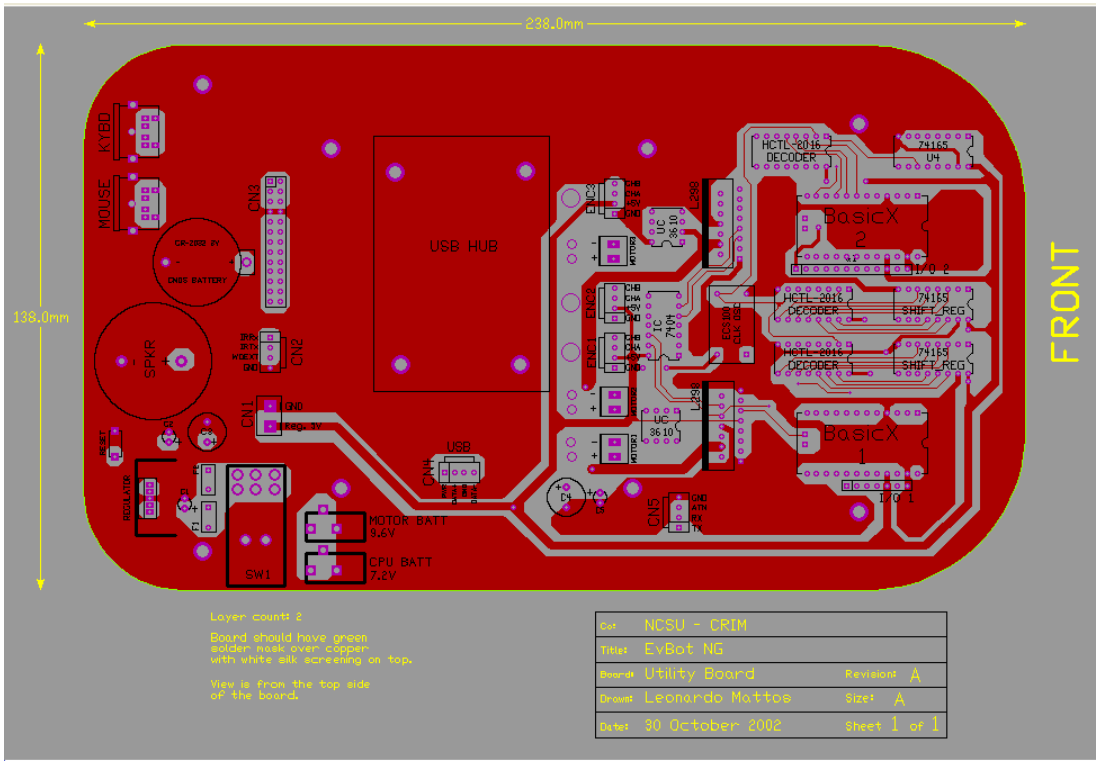


Figure 3.6: Top layer of the utility board.

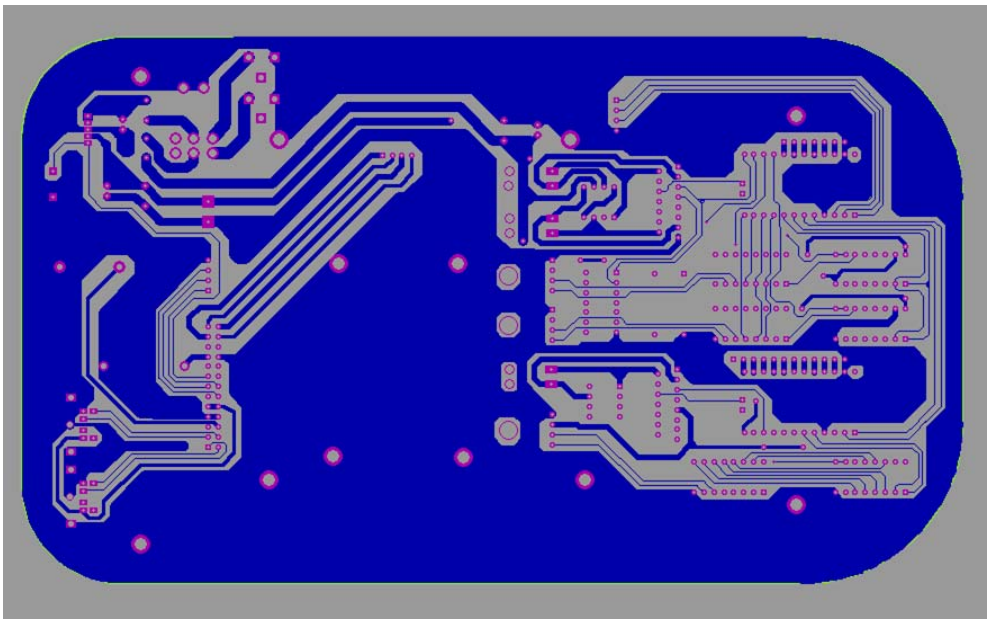


Figure 3.7: Bottom layer of the utility board.

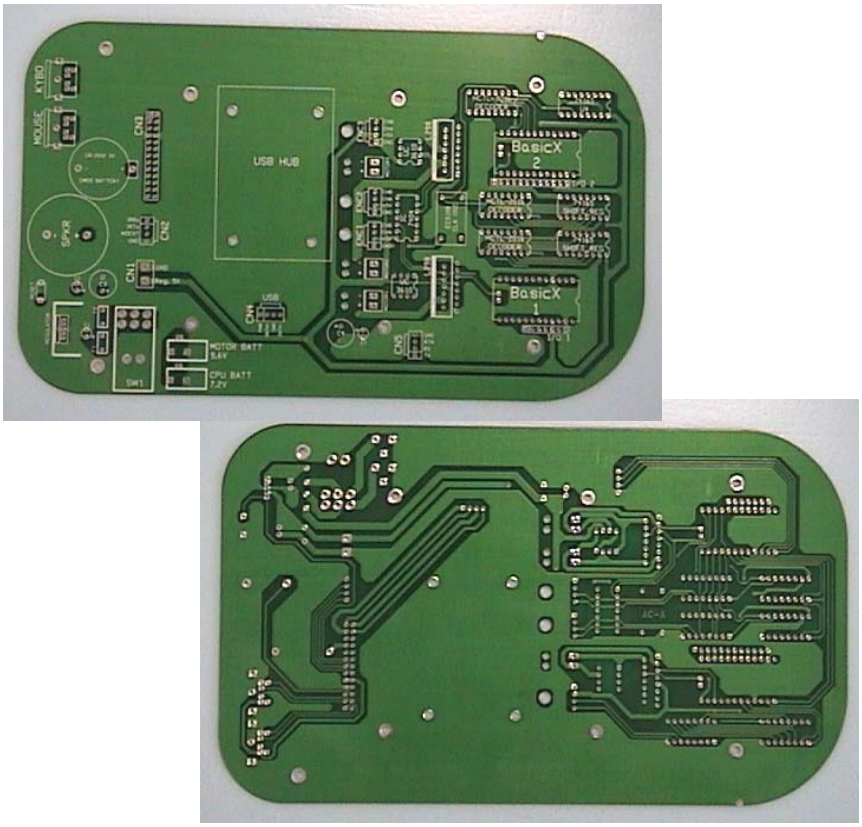


Figure 3.8: The manufactured utility board.

Section 3.5 –CPU to Microcontroller Communication System

As in the original EvBot design, all communications between the CPU (PC/104-based) and the microcontrollers (BasicX-based) in the EvBot II design are made using the RS232 communications standard. The main difference between the communications system design between the original and the new systems is that there are now two microcontrollers on-board instead of one. However, to ensure economy

of design it was decided to use only one of the serial ports in the CPU for data transfers. To solve this problem a communications chain was developed.

The communications system starts on the serial port 1 of the PC/104 stack. That port is directly connected to the first BasicX microprocessor, which is called the Master BasicX. The second link is made using the BasicX chip to support and handle extra serial ports. A second RS232 port is thus defined in the Master BasicX and I/O pins are allocated to communicate serially to the second microcontroller, called the Slave BasicX.

All the commands in this communication system originate in the CPU and are sent to the Master BasicX. This microcontroller is responsible for determining if received commands should be executed locally or if they should be forwarded to the Slave BasicX for execution. All system commands are one-byte in length, which can be extended to include arguments if necessary (see Appendix 2). All system commands produce a return value, which is a command byte followed by the return argument, again if necessary. Exceptions are error bytes, which are returned to the CPU when the last command has not been successfully executed.

Section 3.6 - The PC/104 Stack

The PC/104 stack contains the MZ104, the central processing unity (CPU) of all EvBot's. It is based on the integrated circuit ZFx86, a Pentium-class processors whose main features include: 32 bit CPU core with 100 MHz operation; Full desktop AT compatibility; 64 MB of SDRAM; Fail-safe boot ROM; Dual watchdog timer; Two serial ports; One parallel port; One USB port; Drive interfaces and support for a solid state flash memory device (DiskOnChip).

The second component in the PC/104 stack is a PC/104 interface module with two built-in PCMCIA card slots. It is used to hold additional memory (128 MB in a flash card) and a wireless network card.

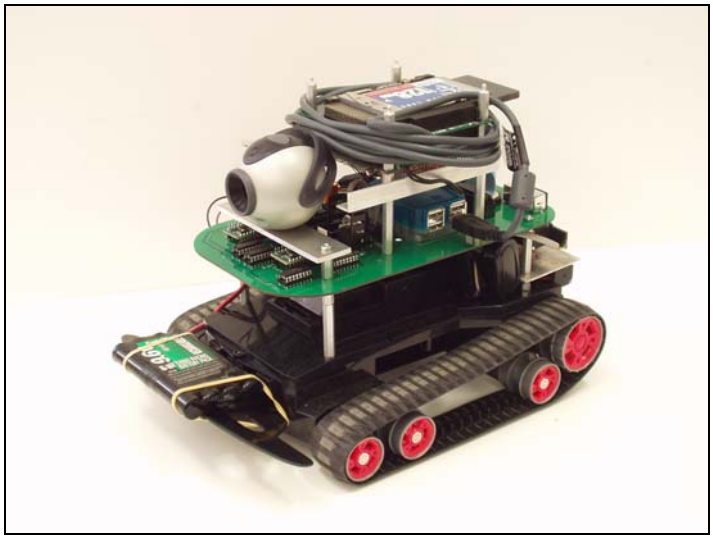


Figure 3.9: The EvBot II completely assembled, showing the utility board and the PC/104 stack mounted on the top the threaded base.

A detailed description of the hardware and custom software developed for the PC/104 system for the EvBots's can be found in [11]. That work also presents the configuration of the network environment were the EvBot's operate and the Infinity Atom Linux, the custom operational system developed for the EvBot platform.

The only improvements on the PC/104 system implemented in the EvBot II were the expansion of memory size. The flash memory card was upgraded from 96MB to 128MB and the DiskOnChip size was increased from 8MB to 32MB. The remainder of the PC/104 system was kept as specified for the original EvBot's platform.

Section 3.7 – Calibration of the Motion System

Although the EvBot II incorporates shaft encoders, calibrations of the motion system were necessary to guarantee a reliable performance of the robot. The calibrations were performed for the open-loop and closed-loop control modes and will be detailed in Chapter 6 along with other experimentations involving the EvBot II platform.

Chapter 4 – Acoustic Array Sensor

Acoustic arrays are passive sensor systems that can have several uses with a robot platform [4] [13]. They are composed by a group of acoustic sensors placed in known geometrical locations that can, in connection with a processing unit, perform a number of audio related functions. Just like our ears, acoustic arrays can be used for communications, for navigation purposes, or as passive sonar for monitoring, tracking, object identification and triangulation.

One of the advantages of acoustic arrays is that they offer increased acoustical sensitivity when compared to single sensor systems, but the main reason to use such an array of sensors is the possibility to perform beamforming and triangulation with the acquired audio data. Both of these functions are based on phase differences between the multiple audio signals. Beamforming provides a way to implement spatial filtering and directional listening, while triangulation can be used to pinpoint the coordinates of a sound source with respect to the sensors array. Both functions will be detailed later in this chapter.

Acoustic arrays started to gain importance when the first sonar devices were developed by the end of the World War I. Since then they have been widely used in the field of surveillance and target acquisition. Recently the use of acoustic arrays started to be extended to autonomous mobile robots being designed for applications in urban warfare and other complex battlefields, and researchers are trying to show their

usefulness for target detection and situation awareness, such as location of snipers or detection of door slam [31].

The goal of the development of an acoustic array for the EvBot II is to expand its sensorial capabilities and to enable the investigation of the uses of sound as another source of information about the robot's surrounding world. With this objective, a small area acoustic array with eight microphones was designed in simulation and later implemented as a shield that can be attached to the robot body.

This chapter briefly presents the background theory involved in acoustic array systems, and presents simulation programs developed to help the understanding and design of such arrays. The programs include software to analyze acoustic array configurations for beamforming and triangulation purposes, and programs developed to use and analyze real acoustic arrays. As a group the developed programs provide the means to validate simulation data and to demonstrate the usefulness of an acoustic array system to the EvBot II.

Section 4.1 – Quick Background

Section 4.1.1 – Background on Sound

The word "sound" usually means sound which can be perceived by the human ear, i.e., it is used as a synonym for pressure waves with frequency between 20 Hz and 20,000 Hz.

Sound propagates through air as a longitudinal wave, which is characterized by the medium being displaced in parallel to the propagation of the wave. As an example, "a single-frequency sound wave traveling through air will cause a sinusoidal pressure variation in the air. The air motion which accompanies the passage of the sound wave will be back and forth in the direction of the propagation of the sound" [38].

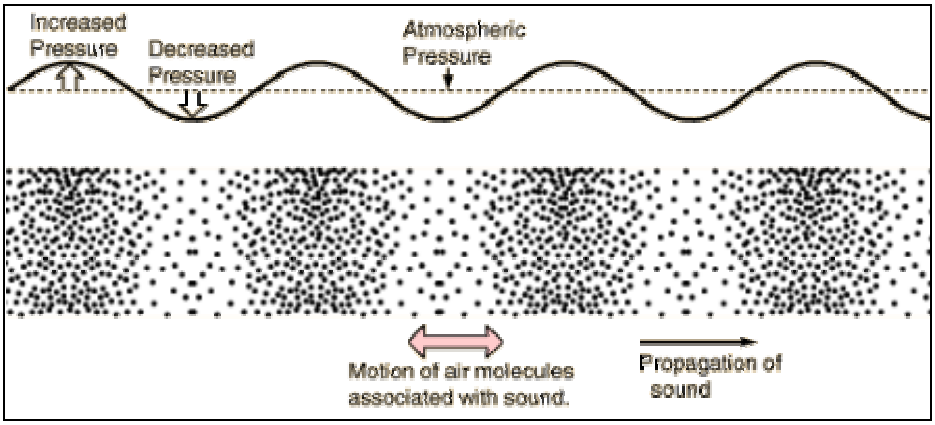


Figure 4.1: Sound waves in air (reproduced from [38]).

The propagation speed of sound is determined by the properties of the medium and, as most other types of waves, follows the relationship $v = f\lambda$, where v is the propagation velocity, f is the wave frequency and λ is the wavelength. In the case of dry air, the speed of sound can be approximated by $v_{sound} \approx 331.4 + 0.6\,\mathrm{T}$ m/s, where T is the Celsius temperature. As an example, for dry air at 21°C the sound speed is 344 m/s and the audible sound waves have wavelengths from 0.0172 meters to 17.2 meters.

Section 4.1.2 – Background on Beamforming

Beamforming is a method used to implement spatial filtering of signals in an array of sensors. It is realized by beamformer systems that collect spatially propagating waves and exploit the principle of interference in order to receive a signal radiating from a specific location and attenuate signals from other locations.

Interference is a phenomenon that can occur between waves propagating in the same medium, and may be constructive or destructive. Constructive interference occurs when the interfering waves are "in phase" and their amplitudes add. If the waves are "out of phase" and the amplitudes subtract the interference is called destructive.

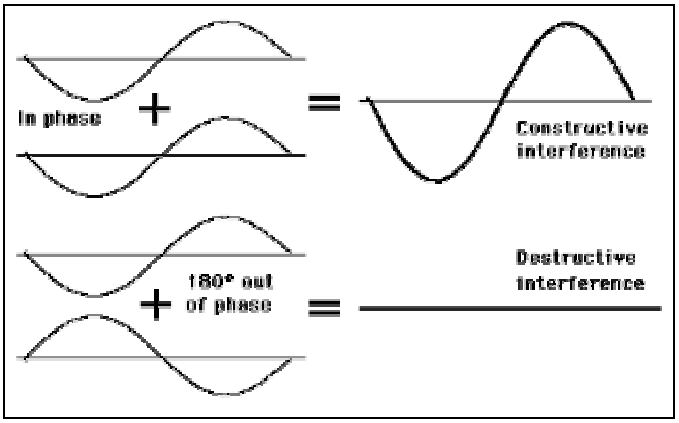


Figure 4.2: Constructive and destructive interference (reproduced from [38]).

Beamformers make use of interference by adding delays and linearly combining the signals collected from the sensors in the array. Such delays cause the signals coming from the listening direction to interfere constructively, and cause the

signals coming from other directions to interference destructively. This effectively amplifies the signals coming from the listening direction and attenuates signals from other directions.

Typically a beamformer is a digital processing system that contains a data acquisition system to translate the analog input data into digital information by means of a sampling process. In such a beamformer the sampled time series obtained from each sensor is shifted and linearly combined to generate a single output time series, which is taken as the signal coming from the specific listening direction.

Section 4.1.3 – Background on Triangulation

Triangulation is a term used to indicate the calculation of the coordinates of a signal source based on multiple sensors' data (or the coordinates of the receiver based on multiple sources' signals). In the case of acoustic arrays, the coordinates of the sound source can be calculated based on the coordinates of each sensor in the array and on the time delays between the signals received by each sensor. Different algorithms can be used to perform such calculation, and they usually provide different precisions and number of singular points. Two triangulation methods will be presented in the following subsections.

Section 4.1.3.1 – Triangulation by Solving Simultaneous Equations

The triangulation method described in this section was called "Matrix Method" and its formulation is relatively simple. As described in [18], the solution can be developed from the case where there is one signal transmitter and four receivers (sensors):

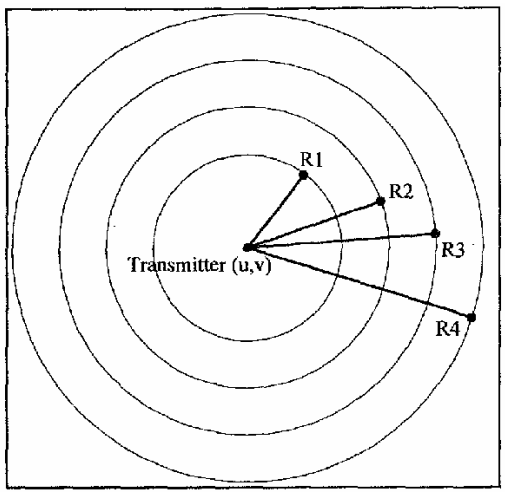


Figure 4.3: Setup for formulation of the triangulation problem (reproduced from [18]).

To start the formulation, consider that the position of the sound source (u,v) is unknown, but the coordinates of the sensors are known and have the values R_1 (x_1,y_1), R_2 (x_2,y_2), R_3 (x_3,y_3) and R_4 (x_4,y_4). Also consider that we can measure time delays between the received signals and assume sensor number 1 as the reference. So the time delays are given by ΔT_{12}, ΔT_{13} and ΔT_{14}. Now, considering that the sound travels in circular waves from the transmitter, four concentric circles can be draw as in Figure 4.3: one with radius d through R_1 and the others with radius ($d + c\Delta T_{12}$), (d

+ $c\Delta T_{13}$) and (d + $c\Delta T_{14}$), where c is the speed of the sound. At this point we already have a set of equation, which is:

$$\begin{cases} (x_1 - u)^2 + (y_1 - v)^2 = d^2 \\ (x_2 - u)^2 + (y_2 - v)^2 = (d + c\Delta T_{12})^2 \\ (x_3 - u)^2 + (y_3 - v)^2 = (d + c\Delta T_{13})^2 \\ (x_4 - u)^2 + (y_4 - v)^2 = (d + c\Delta T_{14})^2 \end{cases}$$

Now, by solving the first equation for d^2 and performing some substitutions, the final set of equations can be written:

$$\begin{bmatrix} 2x_1 - 2x_2 & 2y_1 - 2y_2 & -2c\Delta T_{12} \\ 2x_1 - 2x_3 & 2y_1 - 2y_3 & -2c\Delta T_{13} \\ 2x_1 - 2x_4 & 2y_1 - 2y_4 & -2c\Delta T_{14} \end{bmatrix} * \begin{bmatrix} u \\ v \\ d \end{bmatrix} = \begin{bmatrix} c^2\Delta T_{12}^2 + x_1^2 + y_1^2 - x_2^2 - y_2^2 \\ c^2\Delta T_{13}^2 + x_1^2 + y_1^2 - x_3^2 - y_3^2 \\ c^2\Delta T_{12}^2 + x_1^2 + y_1^2 - x_4^2 - y_4^2 \end{bmatrix}$$

These simultaneous equations can be solved for the sound source coordinates (u,v) and for the distance d between the transmitter and the sensor number 1 provided that we know the velocity of the sound. If that velocity also needs to be calculated, the addition of a fifth sensor can provide an extra equation and a new set of equations can be found and solved. This formulation can also be extended to three-dimensional arrangements (see [18] for details).

This algorithm was tested in simulation and it was found that it is sensitive to errors in the sensors coordinates and in the time delays measurements. It also presents many singular points for planar arrays, so a new algorithm was developed to try to solve these problems by using a voting scheme.

Section 4.1.3.2 – Triangulation by the Voting Method

This algorithm was developed to approximately determine the azimuth angle of an emitting sound source and can be applied to arrays of arbitrary number of sensors and arbitrary configurations. The formulation of the triangulation problem for this method can be better understood by analyzing an acoustic array composed of 3 microphones positioned on the same plane:

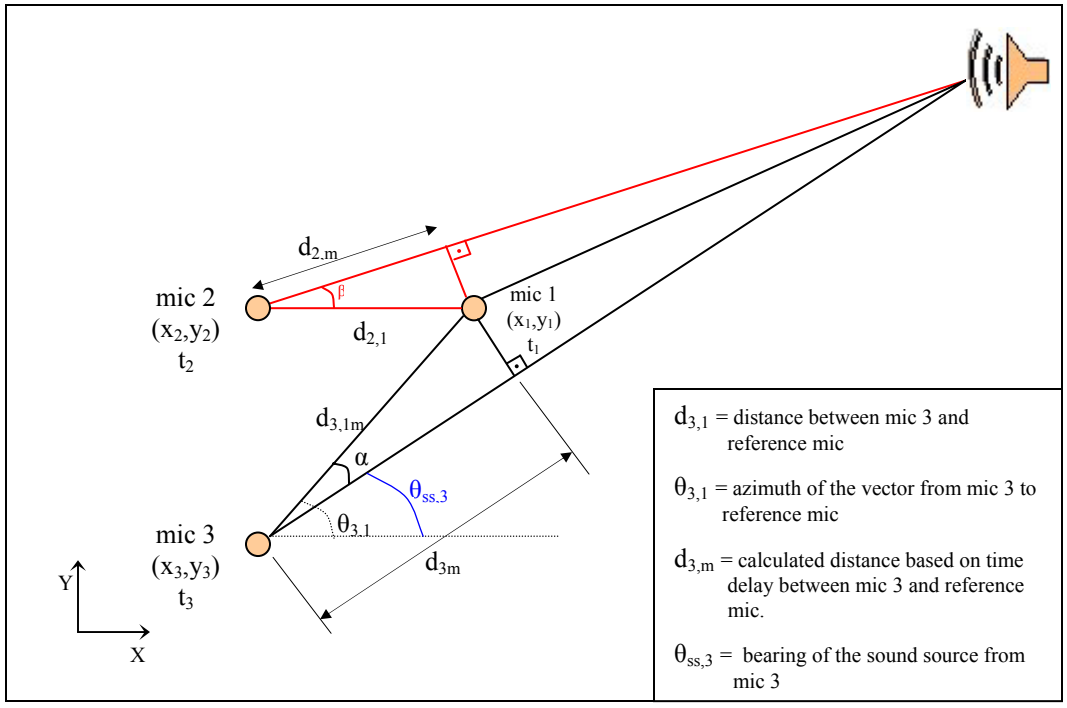


Figure 4.4: Setup for formulation of the triangulation problem.

For the development of the equations, consider the reference microphone to be the mic 1, the microphone with the smallest measured time delay. Now, remembering that we know the distances between the reference and the other microphones ($d_{2,1}$ and

$d_{3,1}$), as well as the azimuth of the vectors from each microphone to the reference ($\theta_{3,1}$ and $\theta_{2,1}$), relative time delay measurements can be used to calculate the distances $d_{2,m}$ and $d_{3,m}$. The formula for these calculations are based on the speed of the sound and given by:

$$d_{2,m} = V_{sound} * (t_2 - t_1)$$

$$d_{3,m} = V_{sound} * (t_3 - t_1)$$

If we consider that the acoustic array is in the far field of the sound source, square angles can be assumed as shown in Figure 4.4, and using geometrical relations we can get to the following equations:

$$d_{3,1} = \sqrt{(x_3 - x_1)^2 + (y_3 - y_1)^2} \qquad d_{2,1} = \sqrt{(x_2 - x_1)^2 + (y_2 - y_1)^2}$$

$$\alpha = \cos^{-1}\left(\frac{d_{3,m}}{d_{3,1}}\right) \qquad \beta = \cos^{-1}\left(\frac{d_{2,m}}{d_{2,1}}\right)$$

$$\theta_{3,1} = \tan^{-1}\left(\frac{y_1 - y_3}{x_1 - x_3}\right) \qquad \theta_{2,1} = \tan^{-1}\left(\frac{y_1 - y_2}{x_1 - x_2}\right)$$

$$\theta_{ss,3} = \theta_{3,1} \pm \alpha \qquad \theta_{ss,2} = \theta_{2,1} \pm \beta$$

The above equations can be used to solve for the azimuth of the sound source as viewed from each microphone, but ambiguities arise. The approach taken by this algorithm to solve this problem is to implement a voting scheme where each microphone "votes" for two possible sound source azimuths. This means that, if the

array has n microphones, the total number of votes will be 2*(n-1), from which (n-1) votes will go to angles that are close to the correct bearing of the sound source. At he end of the voting process, the algorithm selects the angle with more votes as the most probable azimuth of the sound source.

This algorithm was tested in simulation and proved to work well, see Section 4.2.5. Although it does not provide the precise resolution obtained by the solution of simultaneous equations, it does not generate singularities and provide a reliable estimate of the sound source bearing by using data from all sensors available.

Section 4.2 – Acoustic Array Software

The beamforming processing in acoustic arrays is realized in the digital world, using digital signal processing techniques. Therefore one of the main parts of acoustic array systems is the processing computer and the code running on it.

The use of software code for simulation is also very important for acoustic arrays analysis. Simulations can help in the design of array geometry by providing an easy way to change parameters and test new configurations. It also provides graphical representations that can help us understand better the intricate characteristic of such systems.

During the research performed in this area simulation and application programs were developed. The main characteristic of these programs is that they are general in respect to the acoustic array geometry, enabling any two-dimensional or three-dimensional array configurations to be analyzed. Each of the developed software is a MATLAB program and will be presented in the following sections.

Section 4.2.1 – Creating a Representation of the Array Geometry

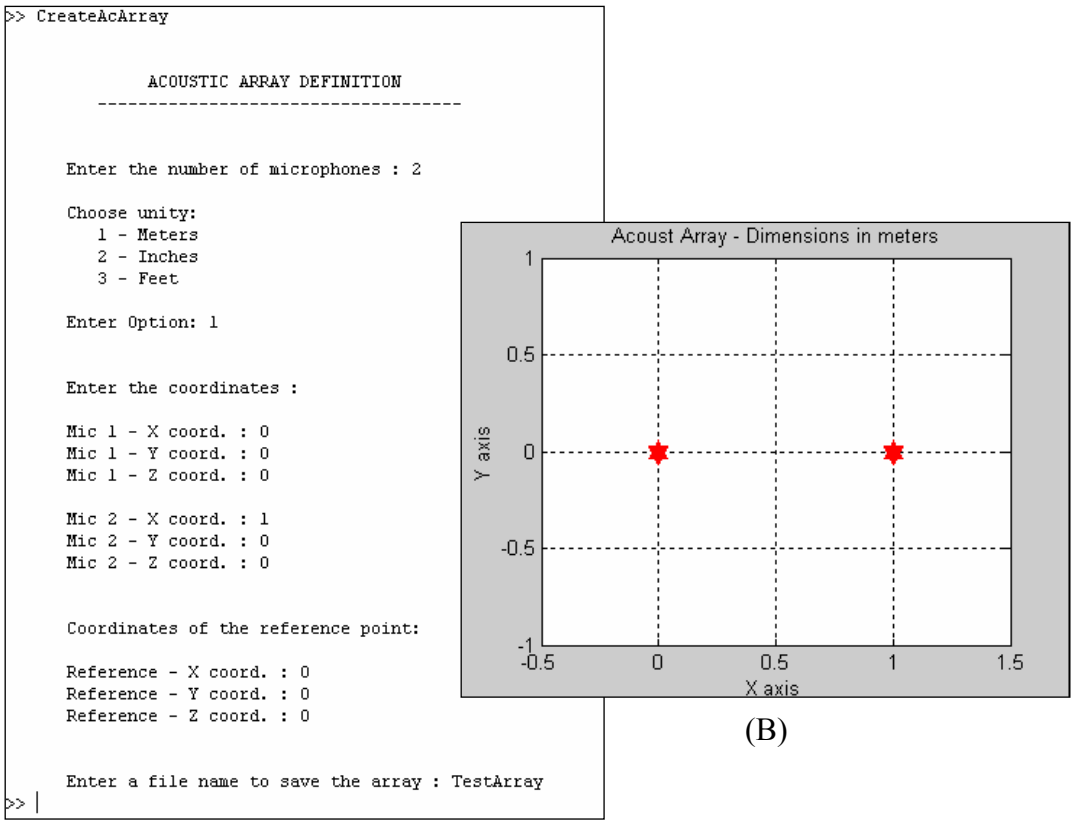
The program *CreateAcArray.m* was developed to gather geometrical information about a new acoustic array configuration and create a file containing the configuration data of that array. The main objective is the generation of a computational representation of the desired acoustic array to be used for simulation and data analysis.

CreateAcArray.m was developed to accommodate for 2-D and 3-D array configurations and accepts parameters in inches, feet or meters. The program gathers the necessary information by questioning the user, starting with the number of sensors in the array. From there, the geometrical coordinates of each microphone relative to a user-defined origin of a cartesian coordinate system are requested.

When *CreateAcArray.m* finishes the information gathering, it plots a representation of each microphone in a 2-D or 3-D figure so the user can easily confirm the correctness of the array configuration. The program also creates a

configuration text file with the sensors coordinates, saving the entered information so other programs can use it.

A view of the MATLAB window running the *CreateAcArray.m* program is shown in Figure 4.5(A) and an example of plot generated is shown in Figure 4.5(B).



(A) (B)

Figure 4.5: (A) MATLAB running the program *CreateAcArray.m* and (B) created array.

Section 4.2.2 – Simulating the Directional Sound Intensity Sensed by an Acoustic Array

After the geometrical configuration of an acoustic array is created, one of the main questions that arise is: How well does it work in terms of beamforming? The MATLAB program *ArrayPolarPlot.m* was created to answer this question through simulation.

The *ArrayPolarPlot.m* program simulates the directional sound intensity sensed by a general acoustic array for a specific sound source location and frequency, which are user defined. To perform that task, the program uses the azimuth and elevation angles of the sound source to generate simulated sound signals with appropriate delays at the microphones and then calculates the directional sound intensity for every look-angle.

In the *ArrayPolarPlot.m* program the look-angles consist of a combination of azimuth and elevation angles having a pre-specified resolution of one degree. For every look-angle, ideal delays that would put signals coming from that direction in phase are calculated and added to the sound signals at the microphones. Those signals are then added together and, due to the included delays, constructive or destructive interference occurs. The result is a signal whose RMS value is proportional to the magnitude of the sound sensed as coming from that direction.

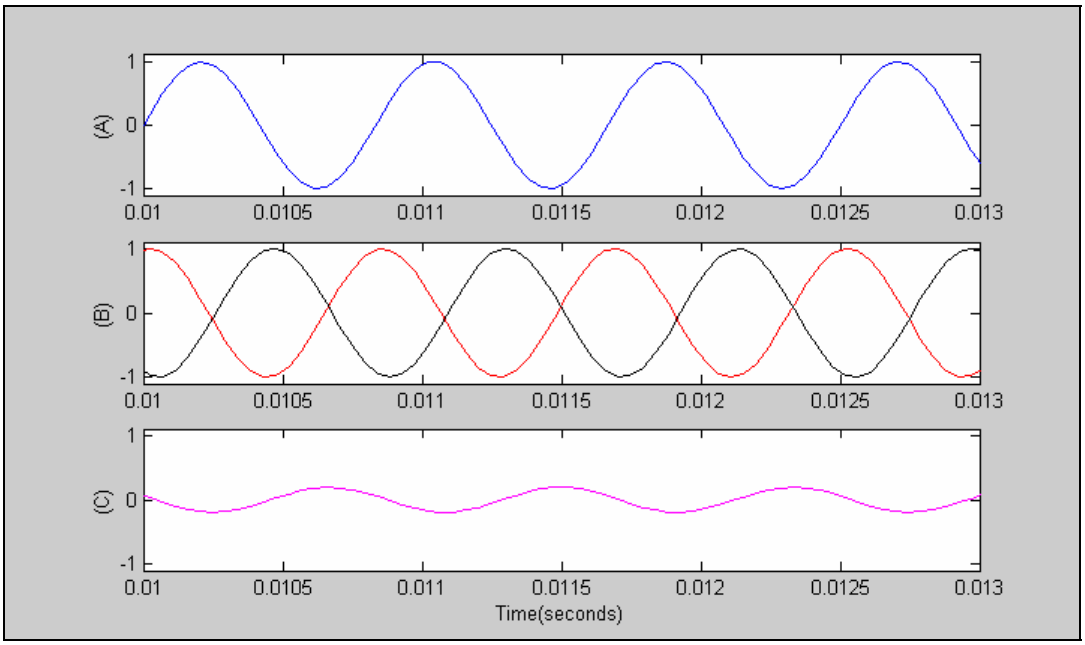


Figure 4.6: Example of simulated acoustic signals. (A) Signal at the sound source. (B) Delayed signals arriving at the microphones. (C) Resulting signal showing destructive interference cause by linear combination of the sensors' signals.

The output of this simulation program is a figure with two plots, each representing the RMS value of the sum-signal at the look-angles. The values are normalized and understood as gains, so the plots are described as directional gain plots for the acoustic array.

The first plot in the created figure is a surface plot representing the gain of the acoustic array in a 3-D space. The second plot is a polar plot that shows the gain data only for the zero-elevation angles. An example of the generated plots is shown next.

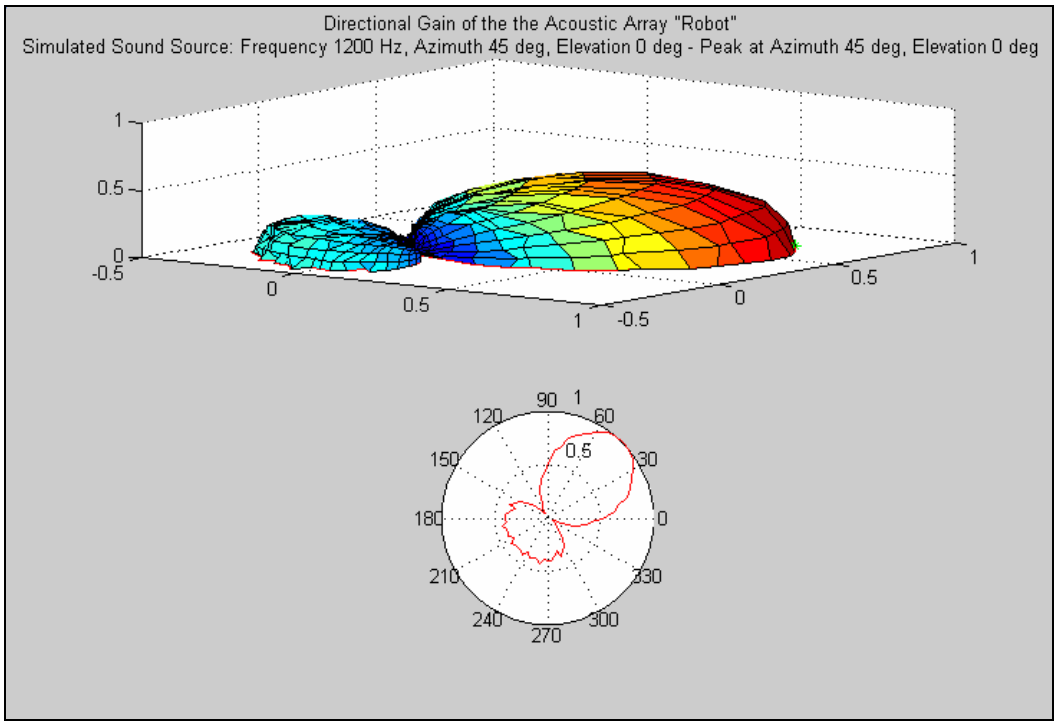


Figure 4.7: Example of directional gain plots generated by the *ArrayPolarPlot* program.

This program also outputs the azimuth and elevation angles of the direction that corresponds to the maximum RMS value of the sum-signal, offering an easy way to check that the maximum value corresponds to the direction of the sound source.

Section 4.2.3 – Simulating Beamforming

A simulation program was created as a variation of the *ArrayPolarPlot.m* program with the objective of generating of similar plots by maintaining the look-

angle fixed and varying the position of the simulated sound source. This program was called *ArrayBeamformer.m* and it allows the user to define the sound source frequency and the acoustic array's look-angle. An example of the plots generated by the *ArrayBeamformer.m* is shown on Figure 4.8.

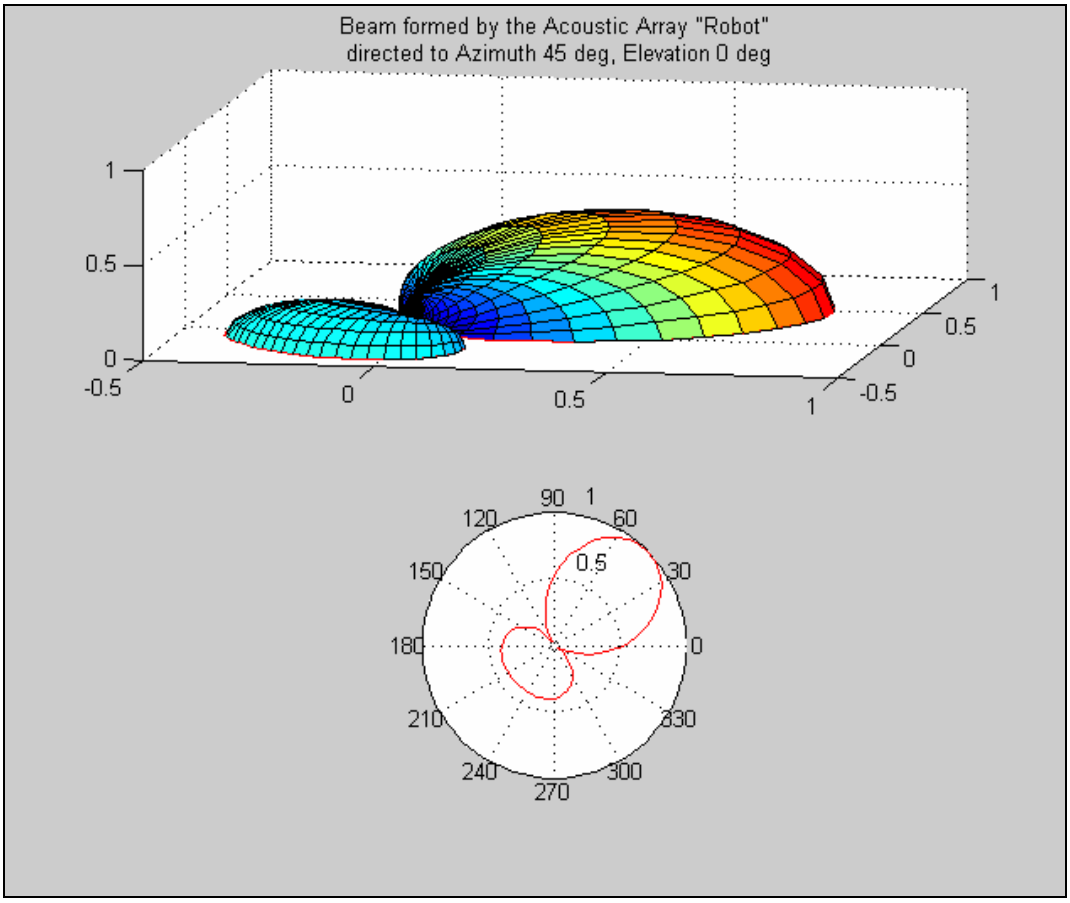


Figure 4.8: Simulated image of a beam that was formed for a look-angle of 45° azimuth and 0° elevation.

Section 4.2.4 – Passive Sonar Simulation and Waterfall Plot

With the objective of implementing more sophisticated and realistic simulations, a program that simulates the use of acoustic arrays as sonar devices was developed. The program was called *TrackingSonar.m* and was developed by extending the program *ArrayPolarPlot.m* to introduce of a moving simulated sound source. A waterfall plot of the directional sound intensities and a waterfall plot of the signal's frequency components were also included in this program.

The *TrackingSonar.m* lets the user specify the sound source frequency and them it rotates the source around the array. For each position of the sound source, the program scans all azimuth angles and calculates the sensed directional sound intensities, using the data to produce two plots: (1) A polar plot as described in the previous sections, and (2) a flat surface plot of the sound intensities versus azimuth angle versus time, which is called waterfall plot. In this plot different colors are used to represent the various intensity levels and the time is implicit in the scan cycle index.

The same idea is used to create a waterfall plot of the frequency components of the sound signals received by the array. In this case, the plot is a flat surface of frequency components magnitude versus frequency versus time. The main use of a plot like this includes object identification by analysis of the frequency signatures, but it can also provide complimentary information about the movement of the sound source by measurements of the Doppler effect.

The *TrackingSonar.m* program also creates a movie of each simulation, making it easy to store the analysis and simulation results for different combinations of acoustic array configuration and sound frequency. An example of the generated output is show in Figure 4.9.

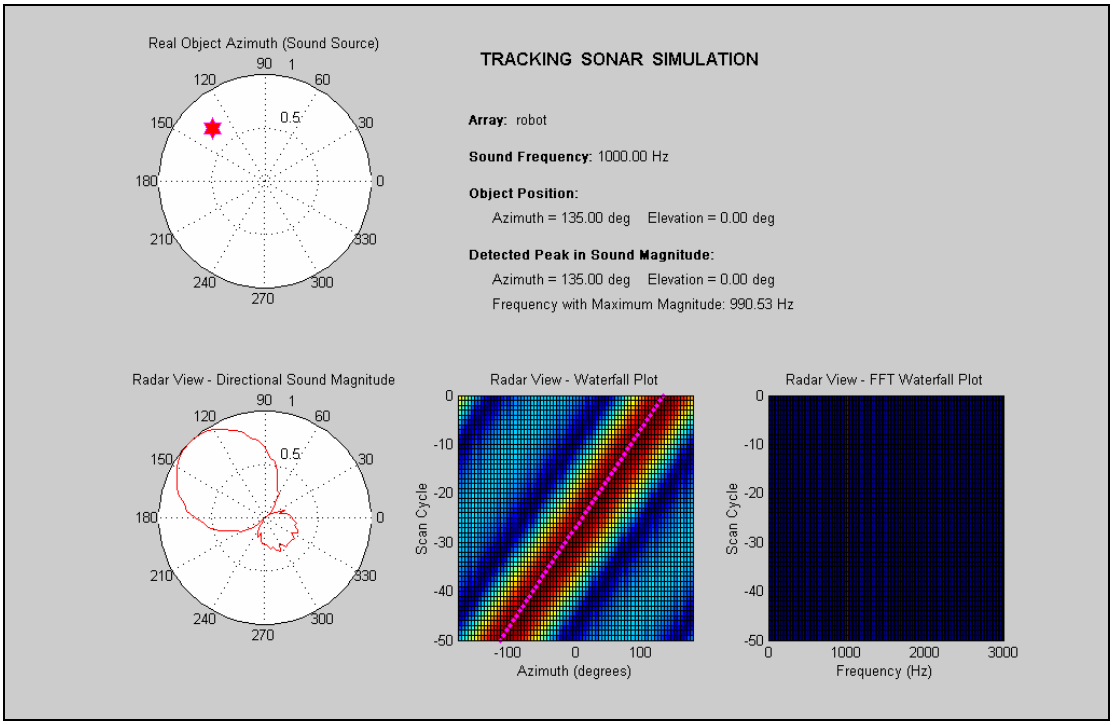


Figure 4.9: Graphics generated by the program *TrackingSonar*.

Section 4.2.5 – Simulating Triangulation – Error Plots

The simulations of the triangulation methods presented in Section 4.1.3 were performed by the programs *Triang_Matrix.m* and *Triang_Voting.m*. Both programs

allow the user to specify the sampling rate of a simulated data acquisition system, and both implement a moving sound source in order to generate plots of the errors in position estimation.

The error plots were used to compare the performance of the triangulation algorithms and it was found that the precision of the time delay measurements is the key factor for obtaining correct estimates. This is especially noticeable in the case of the matrix method, where lower-resolution time measurements cause the appearance of larger errors in the position estimations. Examples of the error plots are shown in Figures 4.10. The poor simulation performance of both algorithms at the sampling frequency used by the EvBot's data acquisition system (9600 Hz) discouraged further developments of triangulation software, so no actual implementation of the triangulation methods was realized.

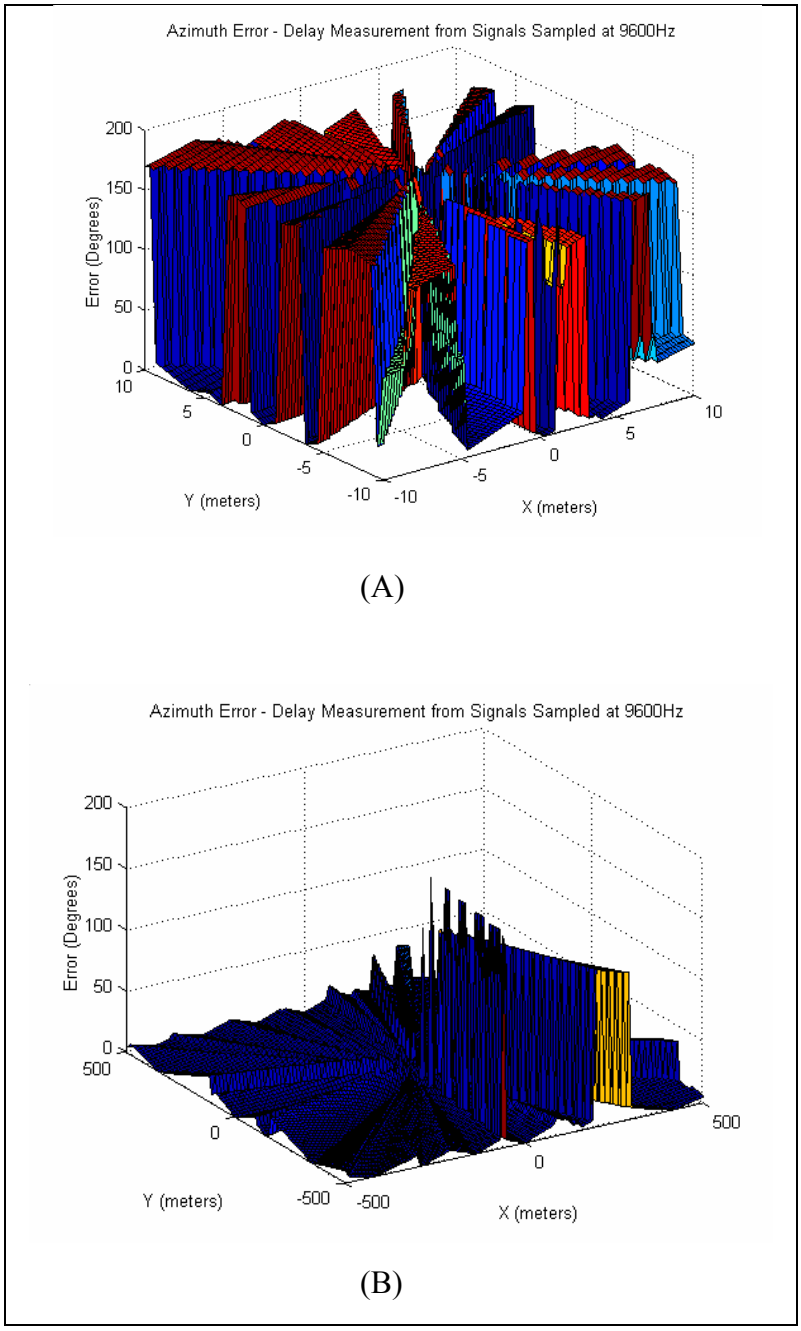


Figure 4.10: Simulated Error plots from the use of the EvBot's acoustic array to estimate the direction of a sound source. (A) Matrix method. (B) Voting method.

Section 4.2.6 – Testing the EvBot's Tracking Sonar

The program *EvBot_TrackingSonar.m* was developed to test the acoustic array installed on the EvBot II by commanding the robot to turn and move towards a sound source. It works like the *TrackingSonar.m*, but instead of simulating the sound signals it gathers real data from the microphones in the array. The data is then processed and after the direction with maximum magnitude is found, the program sends commands to move the robot. This program was tested successfully and some results from experimentation can be found in Chapter 6.

With the objective of better testing the acoustic array system, a second version of the program *EvBot_TrackingSonar.m* was developed to generated graphics of what the robot was actually seeing. Due to the fact that the EvBot doesn't have a display, the control of the robot was transferred to a desktop computer programmed to act as its CPU, thus enabling the generation of plots from real data gathered from the array. The figures created by this new version of *EvBot_TrackingSonar.m* are comparable to the simulation plots generated by the programs *ArrayPolarPlot.m* and *TrackingSonar.m*. Examples are shown in Figures 4.11 and 4.12.

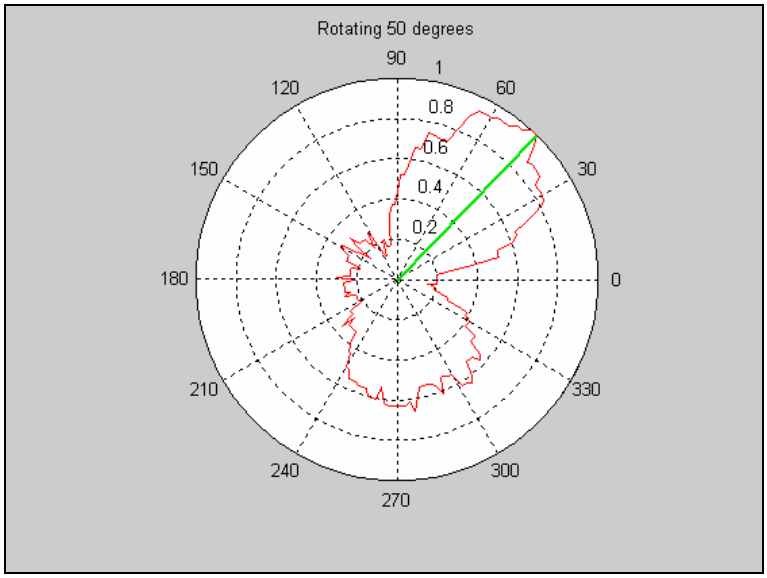


Figure 4.11: Directional sound magnitude as viewed by the EvBot. The green line marks the azimuth of maximum magnitude. The plot's title displays the generated movement command.

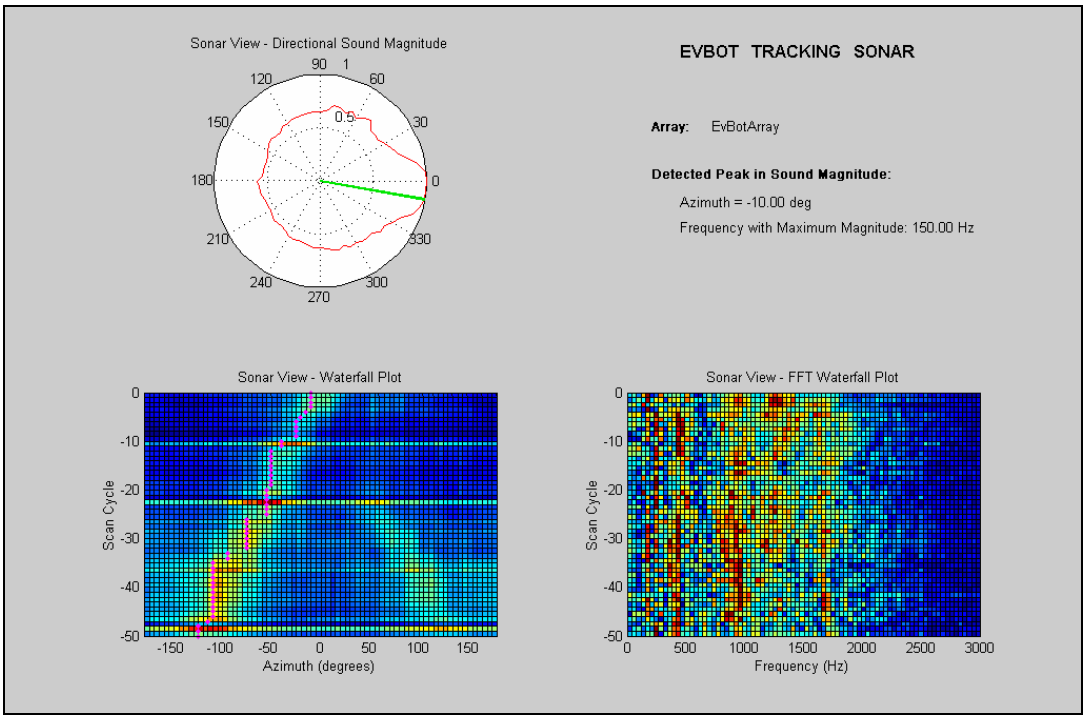


Figure 4.12: Graphics generated by the program EvBot_TrackingSonar when a helicopter's sound was being reproduced near the robot.

Section 4.3 – The EvBot's Acoustic Array Configuration

The design of the acoustic array configuration for the EvBot II was mostly empirical and based on the developed simulation programs described in the previous section. During this design process a decision was made to install the microphone on the robot's shield (see Figure 4.15), so some constraints were imposed by the size of the robot body and the shield itself. The use of simulation programs enabled the analysis of beamforming characteristics for different array configurations, resulting in the decision to implement a 3-D arrangement of the sensors. The selected array configuration is shown in Figure 4.13 and the expected beam formed for a sound frequency of 1 KHz is shown in Figure 4.14. A comparison of the simulated performance obtained for this array configuration along with its measured performance will be later considered and is presented in Chapter 6.

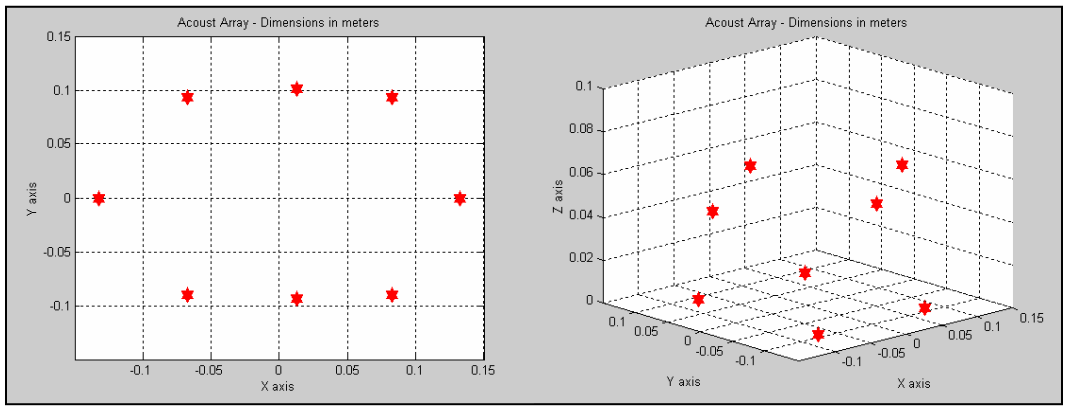


Figure 4.13: Acoustic array configuration for the EvBot II.

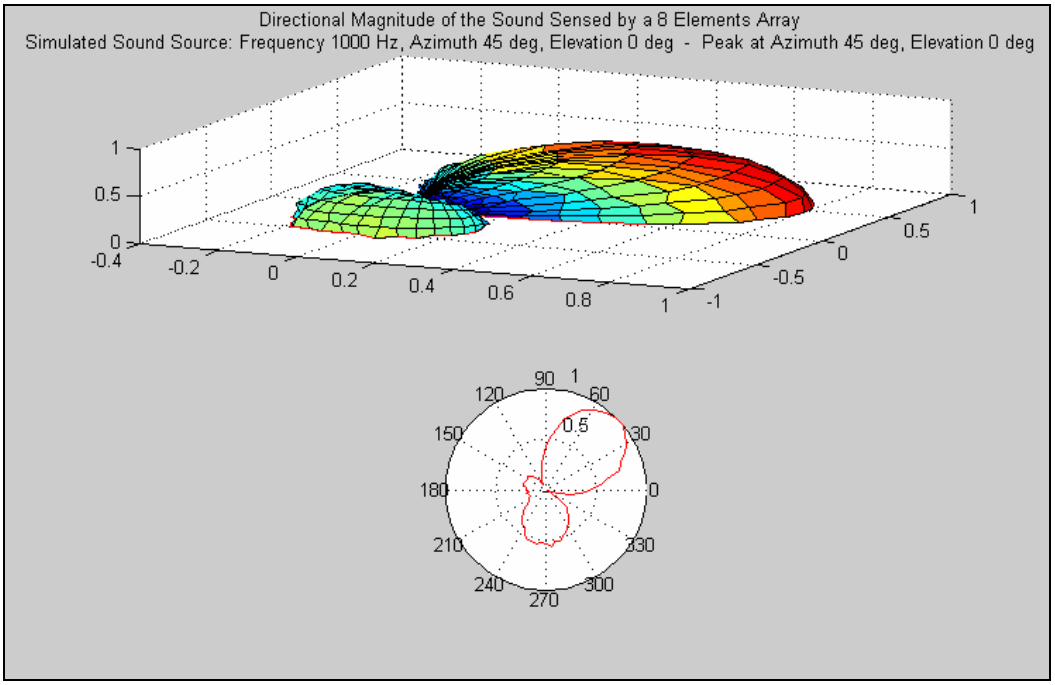


Figure 4.14: Simulation of the directional sound magnitude sensed by the EvBot's acoustic array due to a 1 KHz sound source at azimuth 45°.

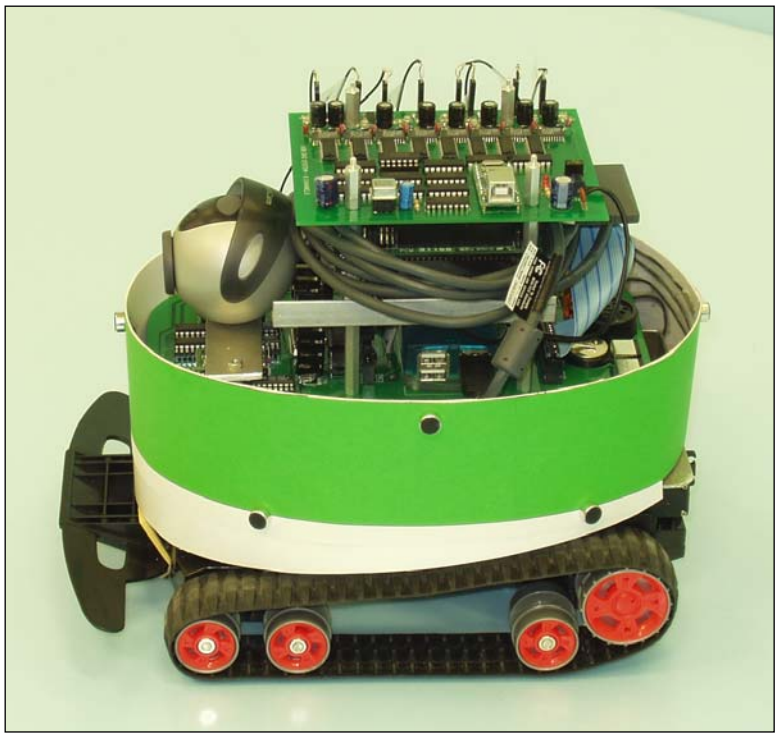


Figure 4.15: The EvBot II equipped with its acoustic array and data acquisition board.

Chapter 5 – The USB-DAQ8 Data Acquisition System

A data acquisition system is the equipment responsible for collecting data from the exterior world sensors, translating that data into a structure, and linking it to a computer where digital processing turns it into useful information. To perform sensor data capture and data organization tasks, a data acquisition system is commonly designed to accommodate the type of data coming from external world and to accomplish specific requirements of the data collection process. It is an important link in the intelligent connection of perception to action. The manner of the connection to the processing computer and the communications parameters are two very important design characteristics of any data acquisition system because they must accommodate for hardware limitations and guarantee mutual understanding.

The need for the development of a data acquisition system for the EvBot II came from the necessity to collect audio signals from an acoustic array of microphones, which is included on the new robot as part of an enhanced sensory capability, so that processing and analysis could be performed. Possible benefits seen from including an acoustic array of sensors are: increased sensor sensitivity, beamforming and triangulation capabilities, and frequency-time analysis. Increasing the sensor count would not be possible without a data acquisition system capable of acquiring and linking all the microphones' acoustic data to the processing unit. In the

long-term an increased sensory capability was intended to give the EvBot II better localization and control capabilities.

The designed data acquisition system was named USB-DAQ8 and it is capable of receiving the analog signals coming from the eight audio microphones to be mounted on the EvBot II. The USB-DAQ8 can simultaneously sample those eight audio channels, what is very important to preserve inter-channel phase relationships. The necessary connection to the CPU is made via a USB link, because of its plug-and-play capabilities and the physical availability of a USB communication's port. USB was chosen over the RS232C serial ports for this task based solely on communication speed requirements.

So, the circuitry developed for acoustic array data acquisition consisted of eight input channels equipped with signal amplifiers and anti-aliasing low-pass filters. Each input channel has its own track-and-hold (T/H) and analog-to-digital converter (ADC) circuit, which are activated simultaneously, thus providing simultaneous sampling of all eight channels. The sampling frequency selected for the task was 78.125 KHz, resulting in 5 million bits of data being sent to the CPU every second (5 Mb/s). Knowing that the EvBot II would generate a large amount of data from its enhanced sensory capability a USB link became a natural choice, after all it is designed to handle such large volume of data with relative ease.

Section 5.1 – Commercially Available Data Acquisition Systems

Data acquisition systems are a huge market and out-of-the-self systems can be easily found for any type of application one might think of. The only problem is that those systems tend to be expensive and most of the times require to be connected to a desktop computer as the CPU host. Most of the systems on the market are also too large and consume too much power to be useful for the EvBot II application. A study of commercially available data acquisition systems indicated that not a single one had the required size, capability, e.g., eight channels with simultaneous sampling, and Linux operating system (OS) compatibility to comply with the EvBot II specification.

A review of the literature indicated that the data acquisition systems that would be most suited to the EvBot II specification are manufactured by National Instruments, Quatech, and MicroDAQ. National Instruments has the SCXI-1140 module that has eight simultaneously sampled input channels, and it is easily programmed and controlled by LabView programs. Although this system has been used by other research groups working in the area of acoustic arrays [22], it is not applicable to the EvBot II project because: the price of the system is prohibitive, and it has large dimensions and large power consumption. A fully functioning system based on SCXI-1140 would cost in excess of US$ 2,000.00, and this was considered excessive for the EvBot II.

The second company mentioned above, Quatech, produces compact PCMCIA data acquisition cards with good specifications, like the DAQP-208. However, this device was discounted for the intended application because it did not offer

simultaneous sampling nor did it support the Linux operating system, two key design requirements for all EvBot robot platforms.

The third company mentioned above, MicroDAQ, produces a data acquisition systems that uses a USB connection, and this attracted attention to the product during the search phase. The USB-30 model was considered first of all, but once again there was a problem with a lack of: support for the Linux OS, simultaneous sampling, and economic price (US$ 570.00/unit). Lastly, it's power requirements were also a factor in the decision to discount this device, since they consume typically 1A at 9 VDC.

After the search of the commercially available data acquisition systems was completed, and found to be unsuccessful, the obvious conclusion was that it would be necessary to design a customized data acquisition system for the EvBot II. It is this design specification that will be discussed in the following sections of this chapter.

Section 5.2 – USB-DAQ8 Overview

As briefly mentioned earlier, the data acquisition system specification to be used for data collection of the acoustic array of sensors includes:

- The amplification of sensors signals
- A low-pass filter, to allow audio signals only to be processed and to serve as an anti-aliasing filter
- The simultaneous track-and-hold of eight channels
- Fast analog-to-digital conversions, to enable ideally 40K samples per second per channel
- An ADC resolution of at least 8 bits per sample
- A USB link to the data processing CPU
- Low power consumption

The developed USB-DAQ8 system accomplishes the requirements above by having eight complete analog-to-digital converter circuits working in parallel and consuming only 1 Watt (200mA at 5V). Unlike typical multi-channel ADC's that use an input multiplexer and convert one input channel at a time, the designed system implements multiple ADC's and performs parallel conversions on all the channels simultaneously. This design specification that was selected due to the fact that no single component was found to offer both a reasonable price and the capability to simultaneously sample 8 channels at the minimum required speed.

A block diagram showing the functionality of the USB-DAQ8 system as specified is shown in Figure 5.1.

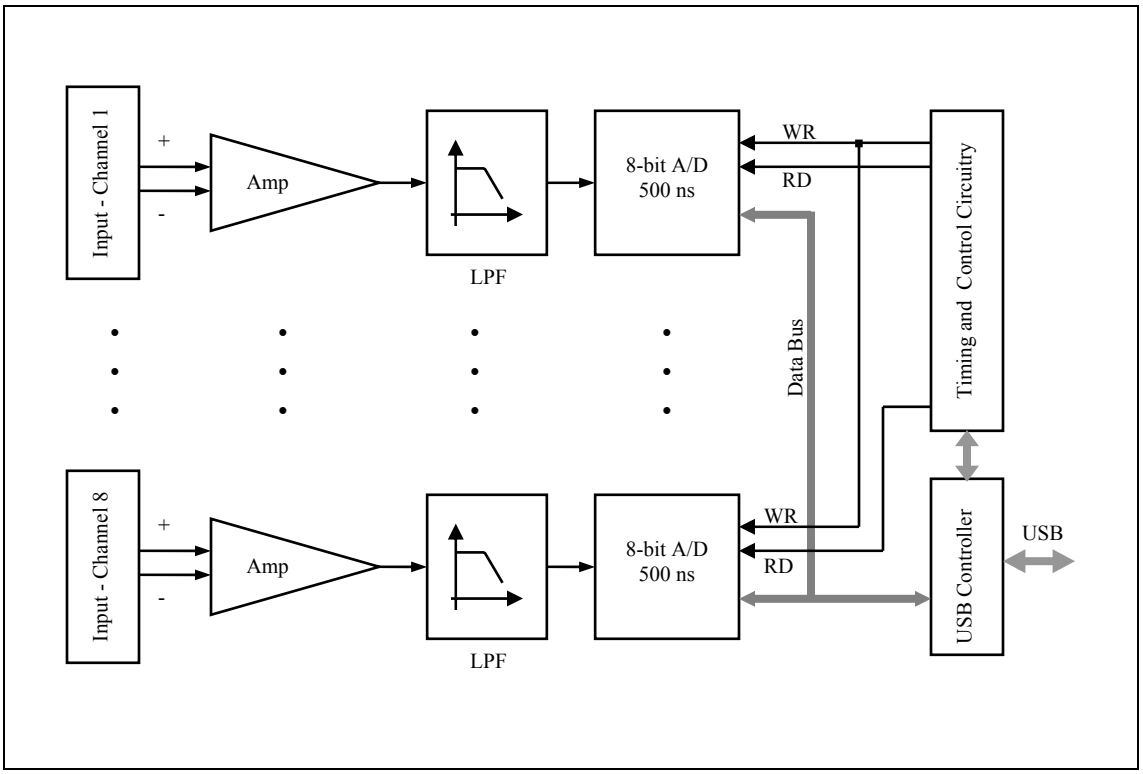


Figure 5.1: The USB-DAQ8 block diagram.

The amplifiers implemented on the USB-DAQ8 provide adjustable gain settings with a minimum gain of 46dB and low-pass filters that have a cut-off frequency set to 20 KHz, which is typically the maximum frequency in the audible range. The sampling speed of the system is 78.125 KHz and it uses 8-bit resolution over the range of 0 to 5 volts. These values translate into a precision of ±0.02 volts and the generation of 5 million bits of data every second (5 Mb/s).

The sampling process in the USB-DAQ8 is controlled by a timing and control digital circuit specifically developed to sequentially read the data from the ADC's and

transfer it directly to the USB controller. From there, the generated digital data is transferred to the processing CPU via a USB link that is capable of transmitting data at a maximum data rate of 8 Mb/s.

Section 5.3 – USB-DAQ8's Amplifier Circuit

The amplifier circuits designed for the USB-DAQ8 are used to couple the electrical signals coming from the sensing microphones into the data acquisition system. They were designed to provide the required gain on the input signals' power and to add a DC level to those signals, enforcing an output signal ranging from 0 to 5 volts.

The amplifier circuits on the USB-DAQ8 are basically AC coupled non-inverting amplifiers that are based on the LMX324 series of operational amplifiers from Maxim Integrated Products (Appendix A3.15). This integrated circuit contains four operational amplifiers, each featuring rail-to-rail output and single supply voltage range, thereby eliminating the need for a (non-available) negative voltage power supply and increasing the swing range of the amplified audio signals. The designed amplifier circuit also provides a variable gain capability, which can be adjusted through an incorporated potentiometer. The minimum gain setting possible is 46dB but usually larger gain values are necessary with the EvBot II acoustic array because of the very low power characteristic of the microphone's signals. This

variable gain setting feature is also useful to accommodate for any slight differences in microphone sensitivity and to set the proper gain value necessary in specific experiments.

An image showing three amplifier circuits on a section of the manufactured and populated USB-DAQ8's printed circuit board is presented in Figure 5.2. Each of the eight input channels of the USB-DAQ8 uses an amplifier circuit like the one described here, always remembering that the gain settings are independent for each channel.

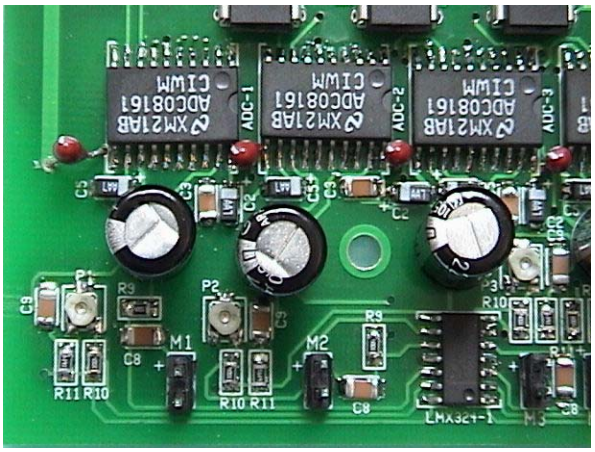


Figure 5.2: Amplifier circuits on the USB-DAQ8's printed circuit board

The Figure 5.3 below shows typical waveforms seen at the input and output of the amplifier circuit. The input signal is a typical audio signal generated from speech and it was measured directly from a microphone's terminals.

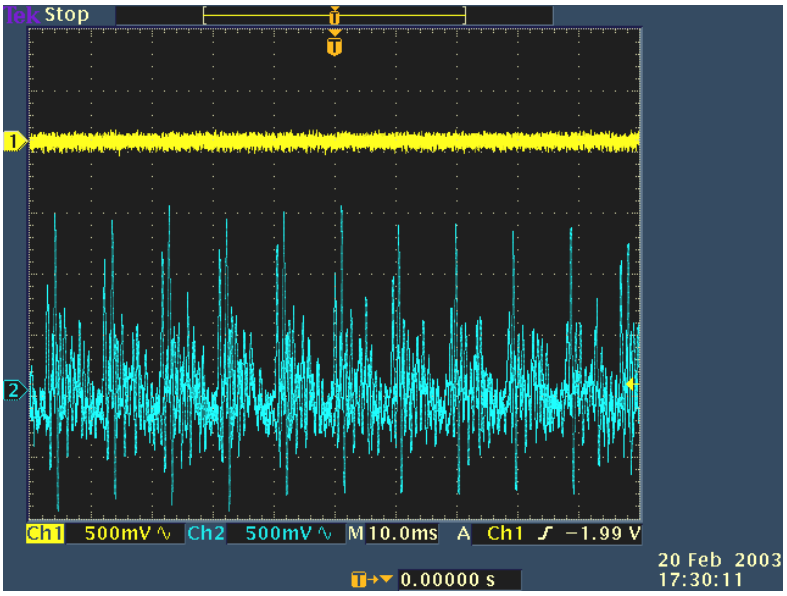


Figure 5.3: Waveforms at the input (Ch 1) and output (Ch 2) of the amplifier circuit.

Section 5.4 – USB-DAQ8's Low-Pass Filter

Frequency filters are used in electronic circuits to select the frequencies of interest or to reject undesired frequency components. In the case of data acquisition systems, filters are a fundamental requirement to prevent any aliasing problems that may arise during the sampling process [26].

The developed data acquisition system uses filters for two tasks, to simultaneously: act as low-pass filters to reject frequency components of noise above 20 KHz; thus selecting only the frequencies in the audible range, and, to act as anti-aliasing filters. The audible frequency range for humans is typically from 20 Hz to 20

KHz, but the band-pass of the filters also include frequency components between 0 and 20 Hz. These very low frequencies (especially DC) are later filtered out using software techniques.

The implementation of the filters for the EvBot II are based on the integrated circuit LTC1563-3 from Linear Technologies, see Appendix A3.16. This device implements a 4th order active RC low-pass filter that approximates a Bessel response. It also features rail-to-rail operation and an internal architecture that enables the selection of any desired cutoff frequency using a single resistor value. The formula used to calculate the value of the resistor for a unit gain filter configuration is given by:

$$R = 10k(256kHz / f_c)$$

where, f_c is the desired cutoff frequency.

The equation above was used to calculate the desired cutoff frequency of the USB-DAQ8's filters, which was previously selected to be 20 KHz. The calculated resistor value was 128 KΩ, which was approximated to 130 KΩ due to the preferred numbers of available resistors. The filter circuit was tested successfully after its construction and provided a cutoff frequency of 20.07 KHz. Typical frequency response plots for the filters are shown on Figure 5.4, where both the gain (db) and phase (degrees) characteristics of the filter are seen plotted against a base of frequency (Hz).

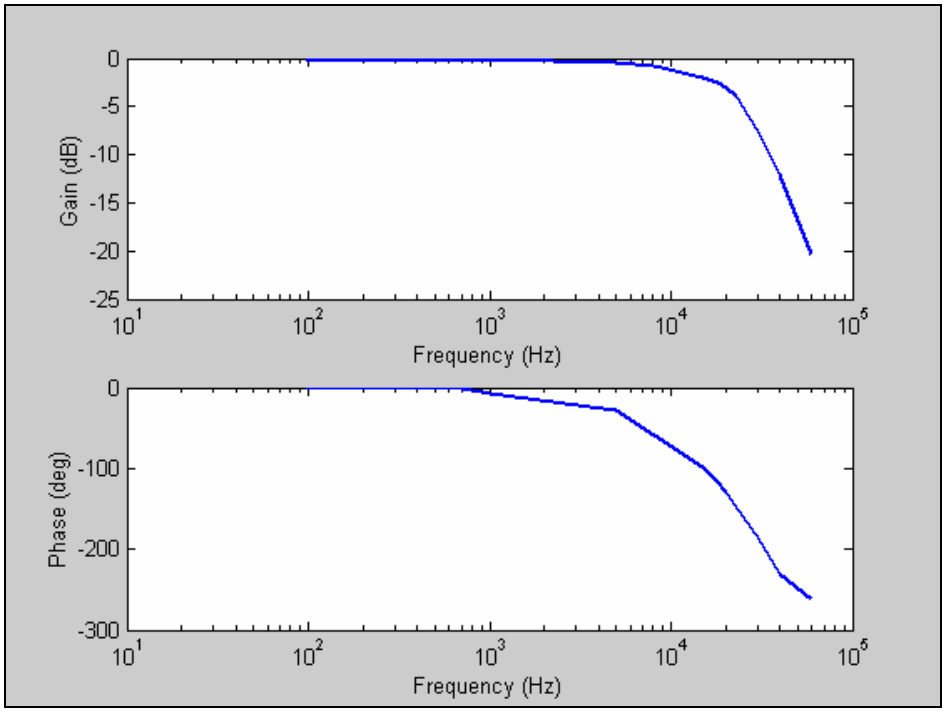


Figure 5.4: Gain and phase frequency response of the USB-DAQ8's active filter.

Figure 5.5 below shows an image of a section of the USB-DAQ8 board that contains one of the filters.

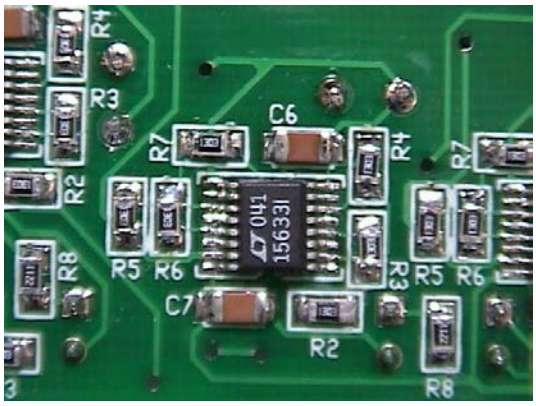


Figure 5.5: A single low-pass filter seen on a section of the USB-DAQ8 printed circuit board.

Section 5.5 – USB-DAQ8's Analog-to-Digital Converter

The analog-to-digital (ADC) converter modules on the USB-DAQ8 are the most important components of the data acquisition system. The ADC's are responsible for converting the continuous time electrical signals generated by the acoustic array sensor microphones into sequences of zeros and ones that can be interpreted and used by the processing CPU. Like data acquisition systems, ADC's can be found for virtually any type of application. The large number of ADC integrated circuits available commercially creates a large variety of specifications, including resolution, speed, approximation techniques, number of input channels and price options.

As usual, the selection of an adequate ADC for the USB-DAQ8 started by a comprehensive search based on the desired characteristics of performance. Certain potential candidate ADC's where easily excluded from consideration due to price, eventually leaving only two components to decide from: Maxim's MAX155, and, National Semiconductor's ADC08161. Now, although the MAX155 offers an 8-Channel ADC with simultaneous track-and-hold, it does not support the minimum sampling frequency of 40 KHZ required by the USB-DAQ8. So, the final choice was made in favor of the very fast National Semiconductor ADC08161 (Appendix A3.14).

The National Semiconductor ADC08161 is an 8-bit ADC with internal sample-and-hold and conversion time of only 500ηs. It also features a convenient 2.5V reference output and supports sample rates up to 300 KHz. These features, added to the low price of $3.47 per unit, made this IC the perfect choice for our EvBot II data acquisition system. Because the selected IC is a single channel analog-to-digital converter, eight ADC08161 are required to be used in the USB-DAQ8. Simultaneous sampling is achieved by starting the conversion process at the same time in all eight ADC's, and this is guaranteed by hardwiring a parallel connection to all eight ADC08161 $\overline{WR}$ pins.

The interfacing of the ADC's to the USB controller was also made easy due to the fact that the selected IC had a parallel data bus featuring tri-state buffers and control lines. This feature made possible to connect all ADC's to the same parallel data bus and to design a relatively simple logic circuit for timing and data control. Figure 5.6 is an image of a section of the designed printed circuit board showing one of the installed analog-to-digital converters (ADC's).

Figure 5.6: Analog-to-digital converter on a section of the USB-DAQ8 board.

Section 5.6 – USB Interface and Controller

From the design requirements, all data generated by the USB-DAQ8 needs to be uploaded to the processing CPU via a USB link. This was accomplished on the USB-DAQ8 by the incorporation of the USBMOD2, a low-cost integrated module for transferring data between an 8-bit parallel bus and a USB channel. The USBMOD2 (Appendix A3.13) is based on the FTDI FT8U245 USB FIFO – Fast Parallel Data Transfer IC, which can transfer data at speeds up to 8 Megabits per second. This technology makes the USB connection very easy by having flag pins for data received and busy, and a control pin to send data. A picture of the USBMOD2 is shown in Figure 5.7.

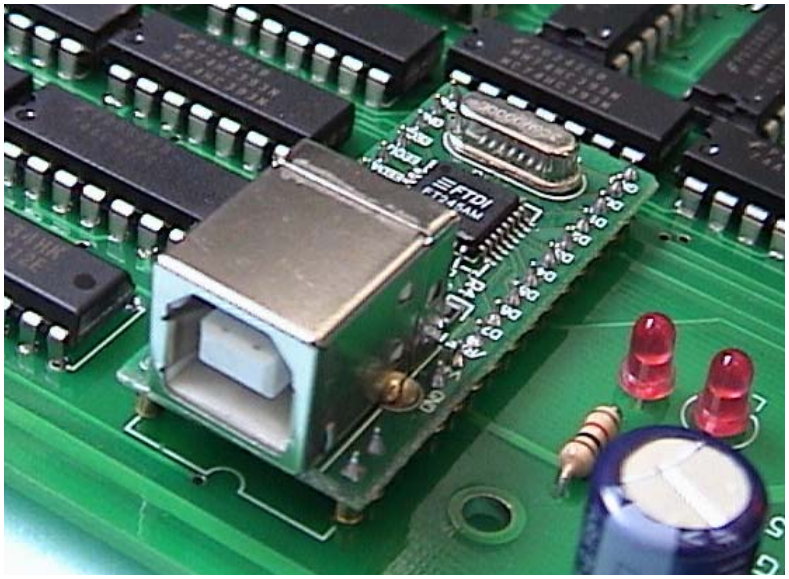


Figure 5.7: The USBMOD2.

The USBMOD2 is viewed by the processing CPU as a standard COM port when FTDI's virtual COM port drivers are used. This was done in the design of the EvBot II so that the data gathering by the processing CPU follows similar procedures as a regular RS232 communications system. Once the required drivers are installed, the USBMOD2 becomes plug-and-play and hot swappable, making it easy for the complete data acquisition system to be connected and disconnected from the EvBot II as required.

Section 5.7 – The USB-DAQ8's Timing and Control Circuit

To ensure the proper functioning of the developed data acquisition system for the EvBot II platform, the components and modules described on the Sections 5.3 to 5.6 had to be connected together using a timing and control circuit. The design and operation of this circuit is described in this section.

The main tasks undertaken by the timing and control circuit include: starting and stopping the simultaneous sampling process in all eight channels, the control of a sequential reading of the ADCs' values, and the transfer of data from the ADC's to the processing CPU. A logic circuit was designed for this purpose, thereby eliminating the need for a local microcontroller system dedicated for this task in the USB-DAQ8.

A general overview of how the timing and control circuit works and interacts with the other components in the USB-DAQ8 can be better understood after the analysis of the functional block diagram presented in Figure 5.8. On the USB-DAQ8, the sampling process is started when it receives any one data byte from the CPU. When that occurs, the USBMOD2 automatically flags the presence of data available for reading by pulling the pin $\overline{\text{RXF}}$ low. This is the signal to start the analog-to-digital conversions and the ADC's are all simultaneously triggered. A demultiplexer controlled by a main counter selects the channel to be read and the system waits for the end of the analog-to-digital conversions. When the selected ADC pulls the pin $\overline{\text{INT}}$ low to flag that data is ready, the logical control circuit enables the parallel bus and the data is loaded to the USBMOD2, which automatically uploads the data to the CPU. At this point, the main counter is incremented and another channel is read following the same process as just described. The system is reset and restarted at the end of reading of the eighth analog-to-digital converter data, provided it did not receive a stop byte from the CPU.

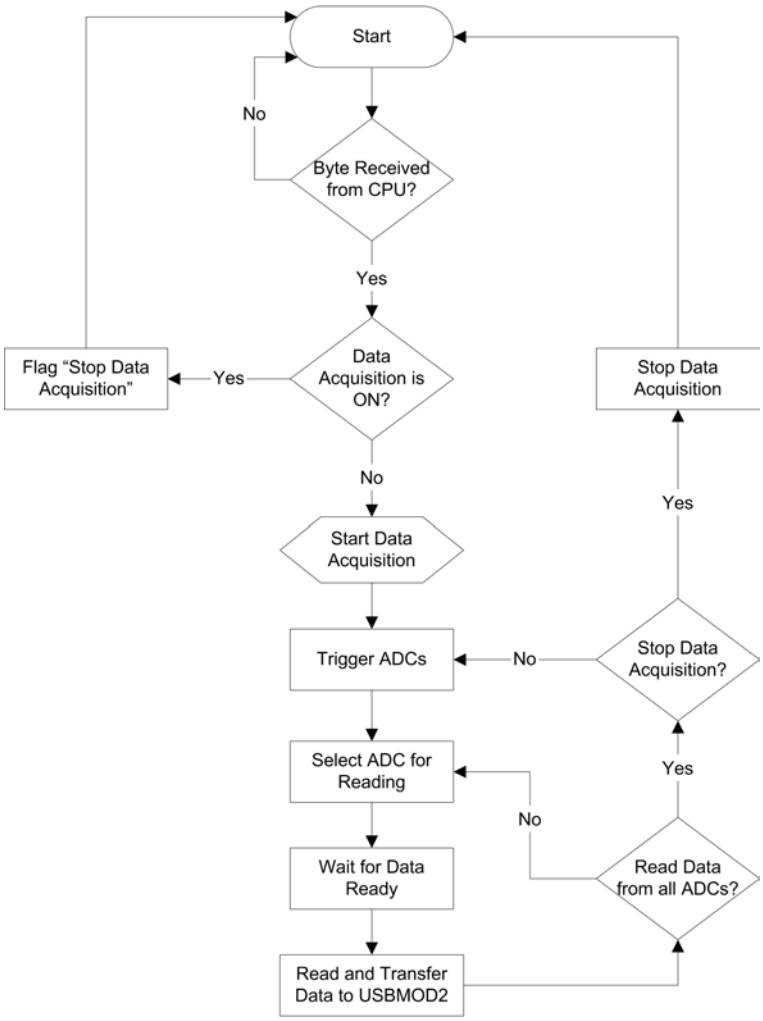


Figure 5.8: USB-DAQ8's functional block diagram

A simplified timing diagram showing the sequences of operations that occur on the data acquisition system is presented in Figure 5.9. Note in the diagram that most of the operations require a minimum processing time.

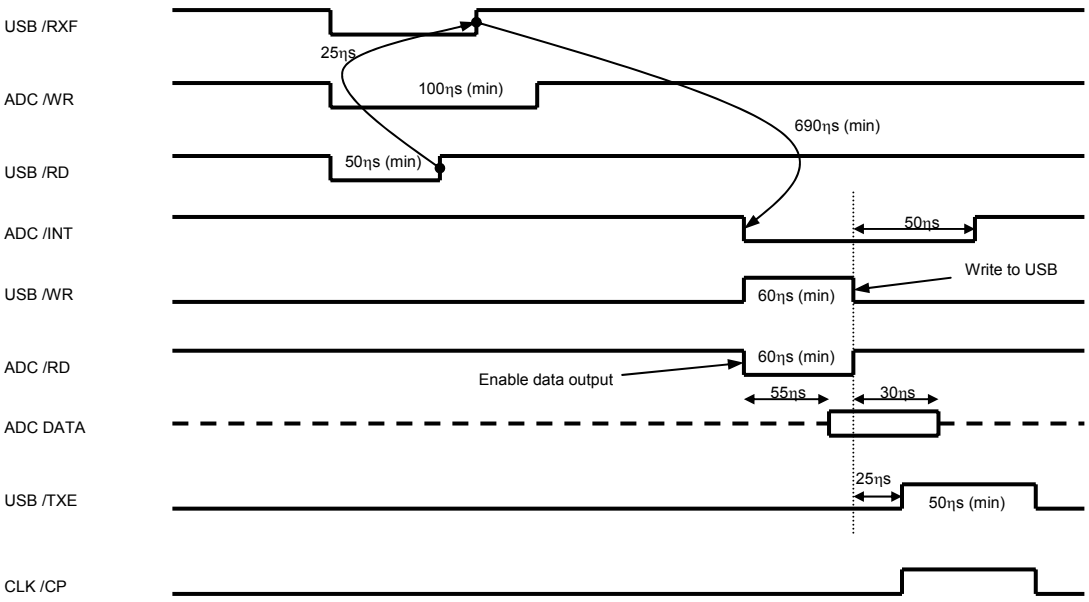


Figure 5.9: Timing diagram for the USB-DAQ8 data acquisition system.

The timing circuitry incorporated into the logic control circuit guarantees a constant sampling frequency of 78.125 KHz for all eight channels for as long as it is required to gather data. It also provides a sufficient amount of time necessary for each signal, and it accommodates for maximum possible delays to guarantee the correct operation of the system. The implementation of the timing and control circuit on the printed circuit board designed for the USB-DAQ8 is shown in Figure 5.10.

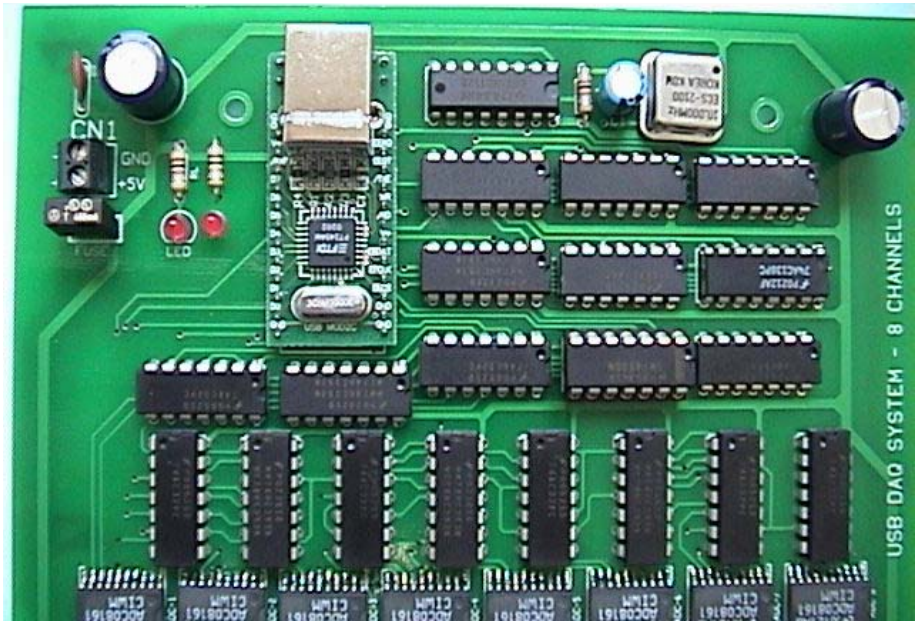


Figure 5.10: Logic circuit for timing and control on the USB-DAQ8 board.

Section 5.8 – USB-DAQ8's Circuit Board

The circuit board created for the USB-DAQ8 was designed to fit the PC104 stack, enabling an easy attachment to any EvBot robot platform. The circuit board has two wiring layers and was created using the software CirCAD. Images of the top and bottom layers are shown in Figures 5.11 and 5.12, along with pictures of the populated circuit board, Figure 5.13.

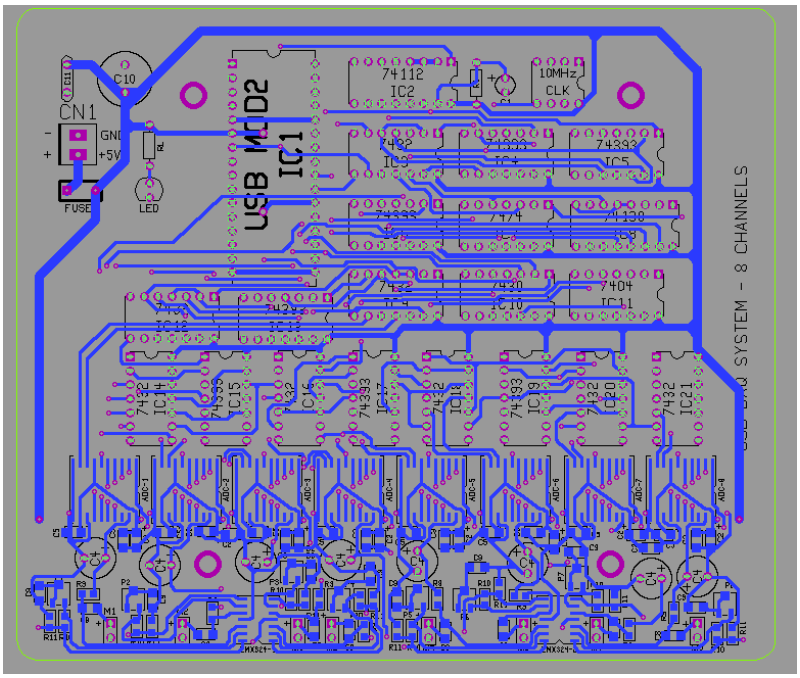


Figure 5.11: CirCAD drawing of the USB-DAQ8's top layer.

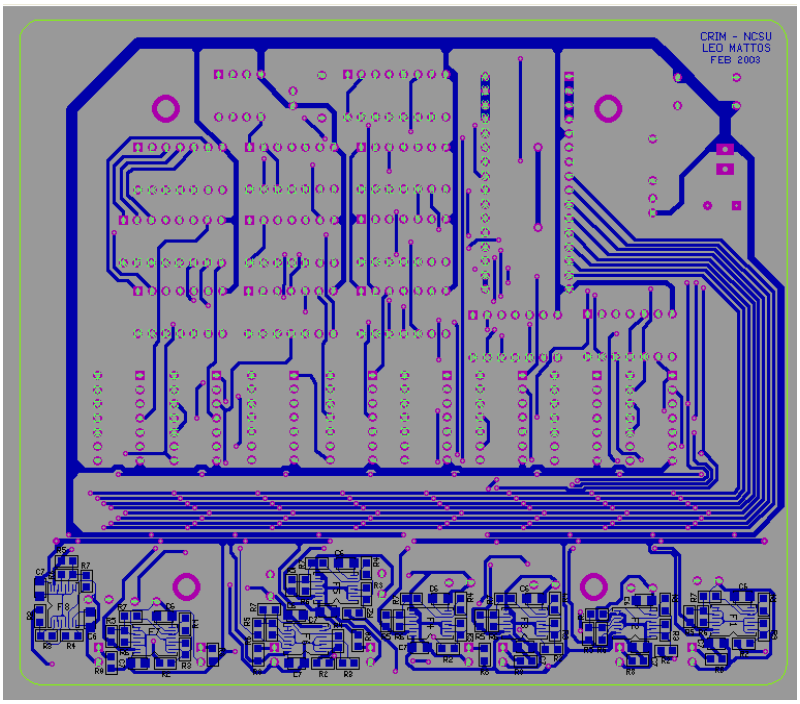


Figure 5.12: CirCAD drawing of the USB-DAQ8's bottom layer.

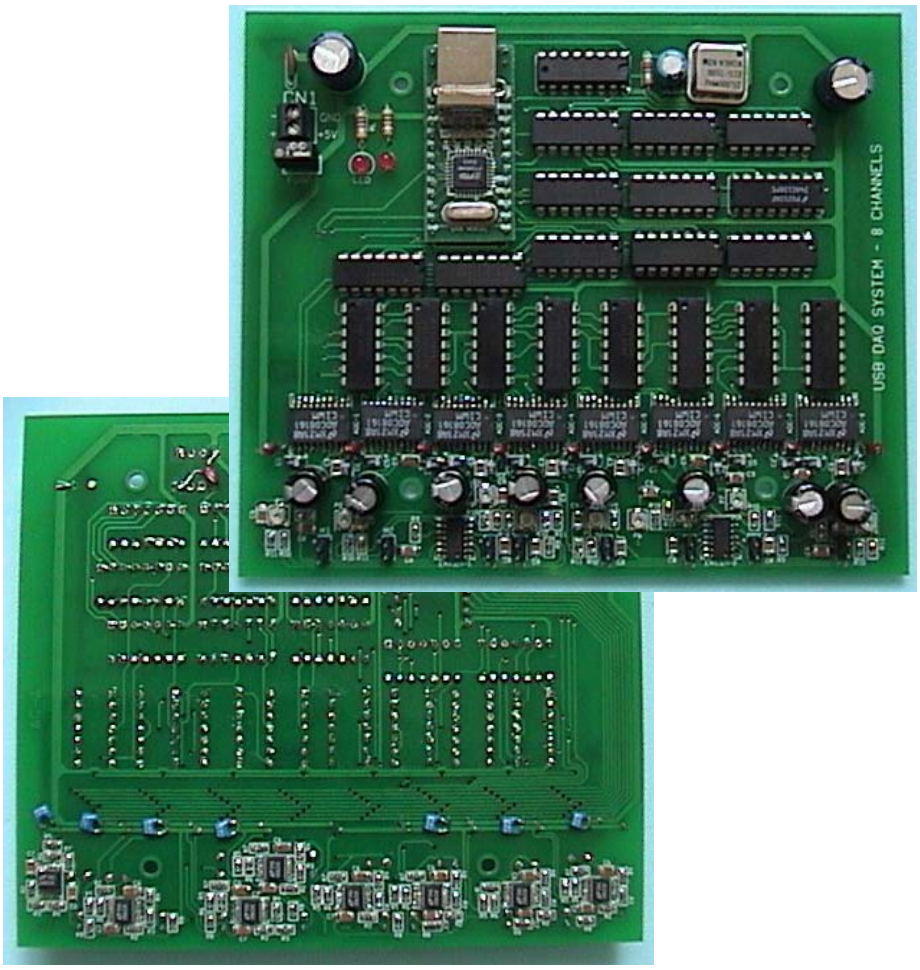


Figure 5.13: The USB-DAQ8's printed circuit board.

Section 5.9 – Design Fault and Solution

After the completion of the USB-DAQ8 implementation several tests were conducted to evaluate its performance, and one of the tests pointed to a design fault related to the data transfer rate on the USB connection. The experiment, which is

described in detail in Chapter 6, made clear that the assumption of an 8 MBps connection was a mistake. It was found that the EvBot's USB port only supports low-speed USB, which works at a maximum 1.5 MBps. Therefore, even though the USB-DAQ8 works fine at higher speeds, it had to be modified to accommodate this parameter change. This problem was addressed by reducing the sampling frequency of the USB-DAQ8 to 9600 samples per second per channel, thus reducing the total amount of data generated from 625 KBps to 76.8 KBps. After this modification experiments were performed and proved that this new sampling rate results in a reliable communication speed.

The consequence of this design change was, as mentioned, a reduced sampling frequency used by the USB-DAQ8 and this reflected on the maximum sound frequency that the system is able to sample, reducing it from 39 KHz to 4.8 KHz. This change was initially thought to be bad, but experimentation proved that this sampling speed is reasonable to the desired application and can provide good results.

Chapter 6 – Experimentation and Results

In this chapter some of the experiments performed during the research are described. These experiments were designed to test the functionality of the individual parts of the new EvBot II architecture, to calibrate them, and to test them in application. The calibration and performance measurements of the EvBot II platform are explained first, followed by descriptions of experimentation involving the USB-DAQ8 data acquisition system. The third section in this chapter presents the experiments performed with the acoustic array system, mainly comparing real results and simulations to evaluate the system. Lastly, an experiment demonstrating the EvBot use of the acoustic array sensor to navigate towards a sound source is presented.

Section 6.1 – Experiments with the EvBot II Platform

The most significant experiments performed on the EvBot II's platform were related to testing of the modules of the new architecture and calibration of the locomotion system. Experiments were also conduct to evaluate the compatibility between the two generations of EvBots. These experiments are described in the next subsections.

Section 6.1.1 – Calibration of the Open Loop Speed Control

Although the EvBot II incorporates shaft encoders, it is required to have a motor control system capable of operation in an open-loop configuration to maintain full compatibility with the existing EvBot's. This means that each robot must perform within a pre-specified error margin when commanded to move or turn. To reach this goal a precise calibration was necessary.

The calibration procedure consisted of adjustments of the PWM duty cycles so the motors turn at the desired speed. To reach such goals, measurements were taken for commands with an active time of one second, what facilitated the calibration process by allowing the measurement of the average speeds by measuring the distance travelled. The entire range of speeds supported by the EvBot II was tested and the PWM values were adjusted to reduce the measured errors to less than ±5%. This process generated the specific PWM values necessary for speed values ranging from zero to 8.5 inches/second, the maximum linear speed of the robot. Such information was used to generate the plot seen in Figure 6.1, from which the linear relationship between the PWM values and the linear speed was calculated.

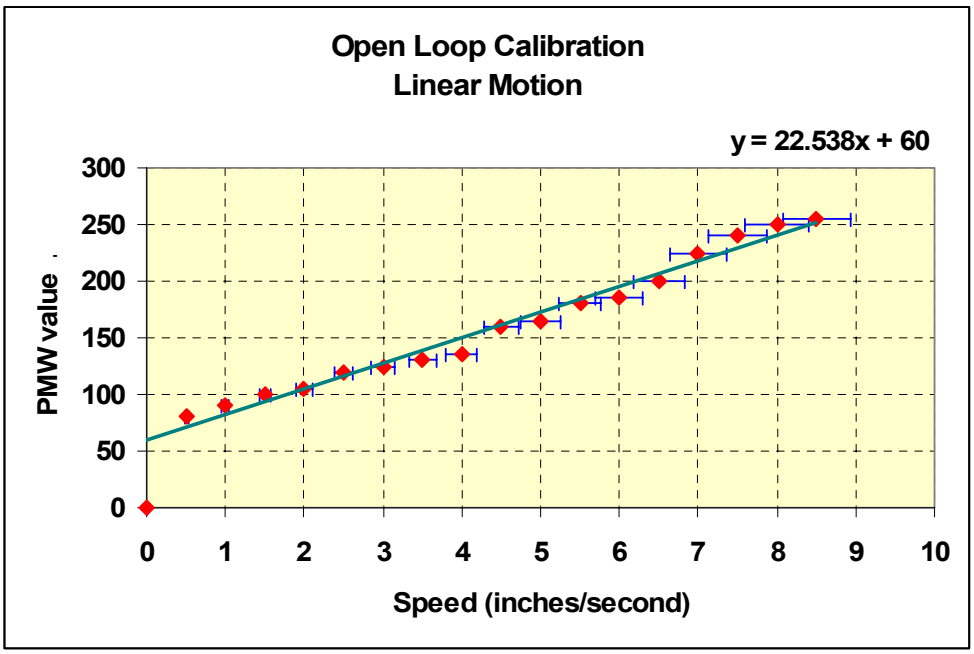


Figure 6.1: Open loop calibration points for linear motion. Error bars show ±5% error at each calibrated speed.

A similar procedure was followed to calibrate the robot rotation. In this case angular displacements were measured and compared to a desired value. The PWM duty cycles and the active time of the commands were then adjusted to generate the desired rotation. This process of calibration was performed for rotation angles ranging from -180° to +180°, and the resulting values are shown in the next figures as the product of the two parameters varied during calibration.

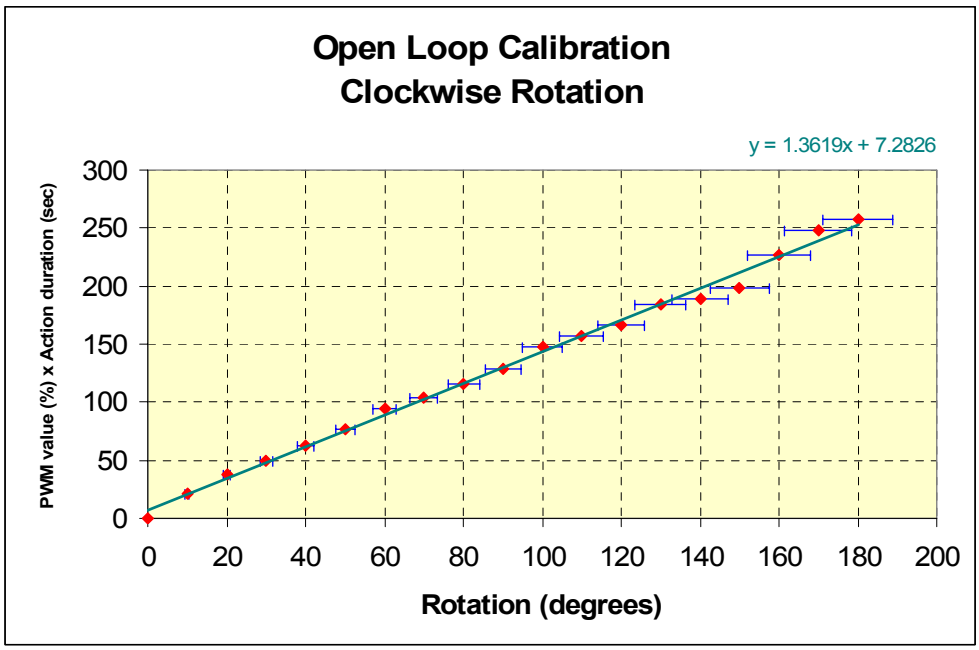


Figure 6.2: Open loop calibration points for clockwise rotations. The y axis represents the product of PMW values and active time of the rotation commands. The error bars show ±5% error at each calibrated point.

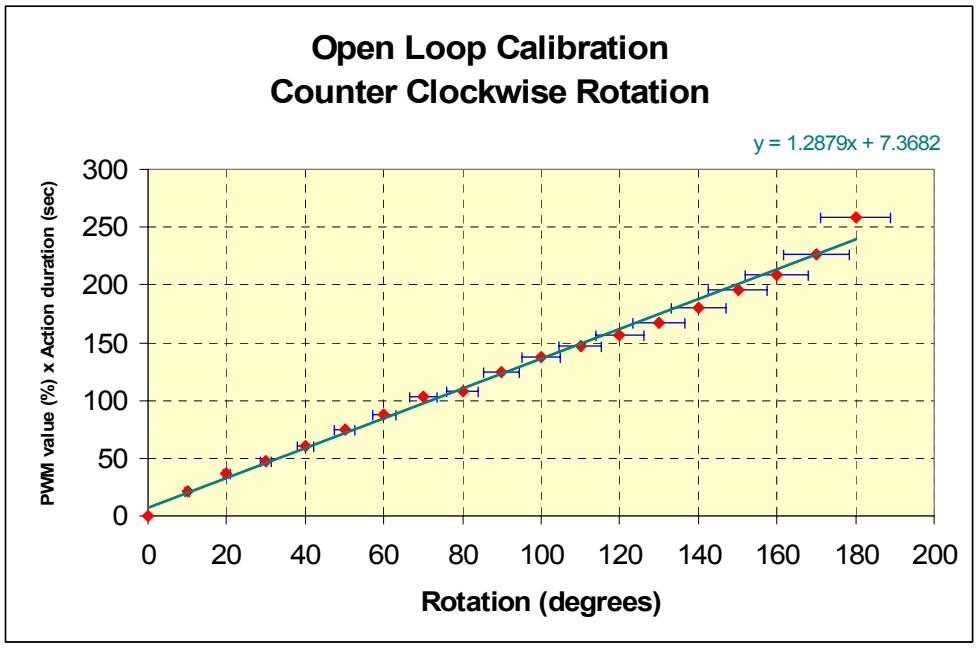


Figure 6.3: Open loop calibration points for counter clockwise rotations. The y axis represents the product of PMW values and active time of the rotation commands. The error bars show ±5% error at each calibrated point.

From the plots above a linear relationship between the rotation angles and the product PMW-Time can be observed and is made explicit by the formulas shown. Such formulas will be implemented in the EvBot II's software and are used to produce the correct commands when rotations are desired.

Section 6.1.2 – Calibration of the Closed Loop Speed Control

The closed-loop speed control system developed for the EvBot II was implemented using PID controllers running on the BasicX microcontroller. Each motor has its own control system, which receives speed commands generated at the EvBot's CPU and feedback signals from optical shaft encoders. The microcontroller is responsible for evaluating the data from the encoders and measuring the motor angular velocities, obtaining values in encoders-counts per second. It also translates the unit of the received commands from inches/second to encoder-counts/second, and imposes a limit of 2550 encoder-counts/second. This limit translates to a maximum linear speed of approximately 6.5 inches/second.

The calibration procedure for the closed-loop speed control systems consisted of basically two phases: Initially the PID controllers were experimentally calibrated to provide relatively fast rise-time and low oscillation on the steady-state phase; later the scaling factors for the speed commands were calibrated to provide compensation for slight differences between the two driving motors. The calibrations of the PID

controllers were very qualitative but the results show a good performance of the system, as can be noticed from Figure 6.5.

The calibrations of the scaling factors for the commanded speeds were necessary to make the EvBot II move on a straight line when the same speed value is commanded for both driving motors. These factors are basically the maximum speed of the robot's treads and are used for normalization of the speed commands. As a consequence, the calibrations were performed experimentally by measuring the robot motion in a straight line.

After the calibrations were performed, experiments were conducted to evaluate the quality of the speed control system. Satisfactory results were obtained and are summarized by the following plots. The data collected during the experiments can be found in Appendix A1.2.

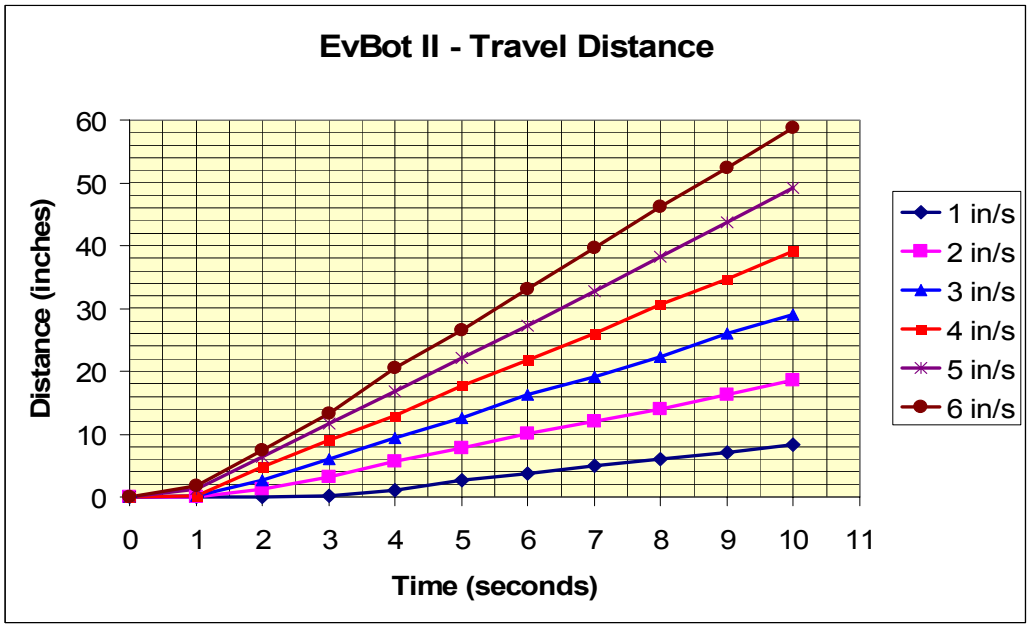


Figure 6.4: Distance traveled by the EvBot II for different speed commands when using closed-loop speed control.

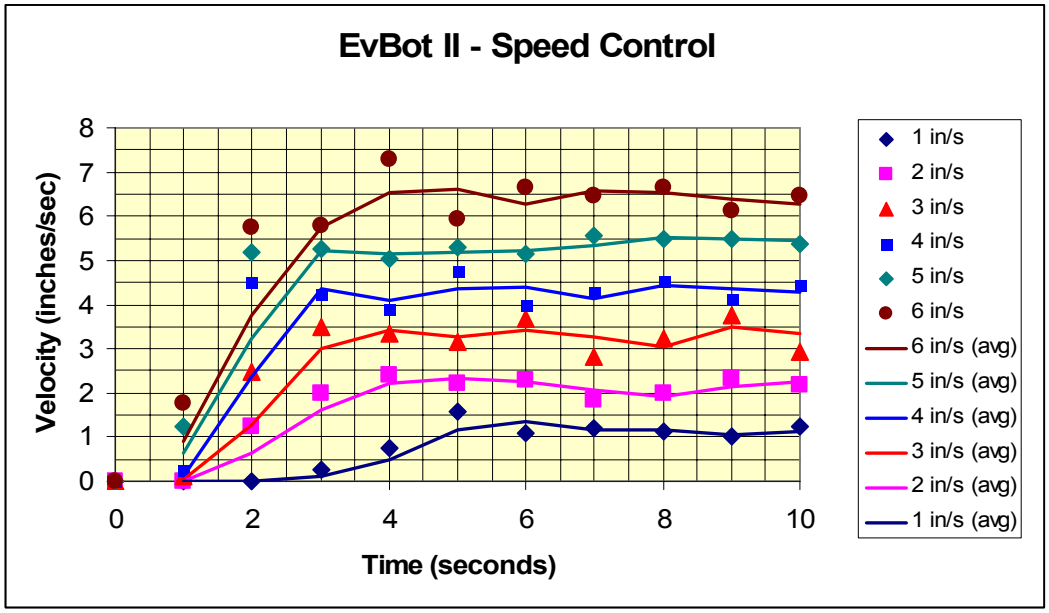


Figure 6.5: Response of the speed control system to different commanded speeds obtained from experimental data.

Section 6.1.3 – EvBot II in Action

The EvBot II platform was developed to be completely compatible with the original EvBot, so a major indicator of how well the EvBot II performed was obtained by testing it against the EvBot. To test compatibility the EvBot II was given the same neural network controller as used by other EvBots, then tested in a maze environment. The results obtained showed that the EvBot II operates in a similar matter to the original EvBots and also to the simulated EvBots under similar conditions. This performance can be seen in Figure 6.6, which shows two images of

the tracks followed by the EvBot II while searching for the red goal in the maze environment.

A performance comparison of the two generation of EvBots during one of the experimental runs is shown in Figure 6.7, and an image of simulated EvBots in the simulated world used to evolve the neural networks controllers is shown in Figure 6.8. By observing those two figures we can see that both generations perform closely to that obtained in simulations. Furthermore it is clear that when the two generations of EvBots operate in the real world they avoid colliding with walls, in a similar fashion to their simulated counterparts.

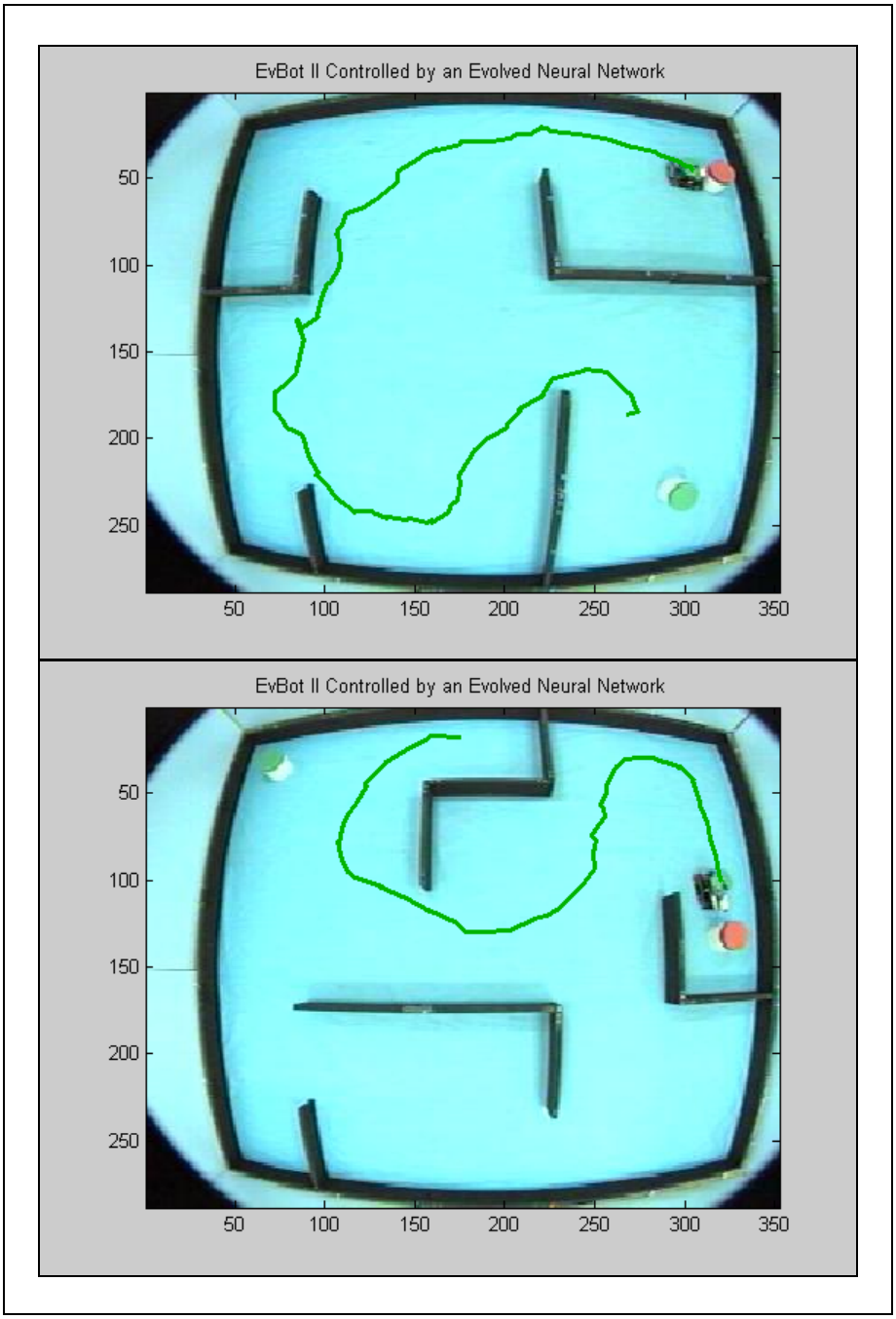


Figure 6.6: EvBot II traveling through the maze in search of the red goal (two trials).

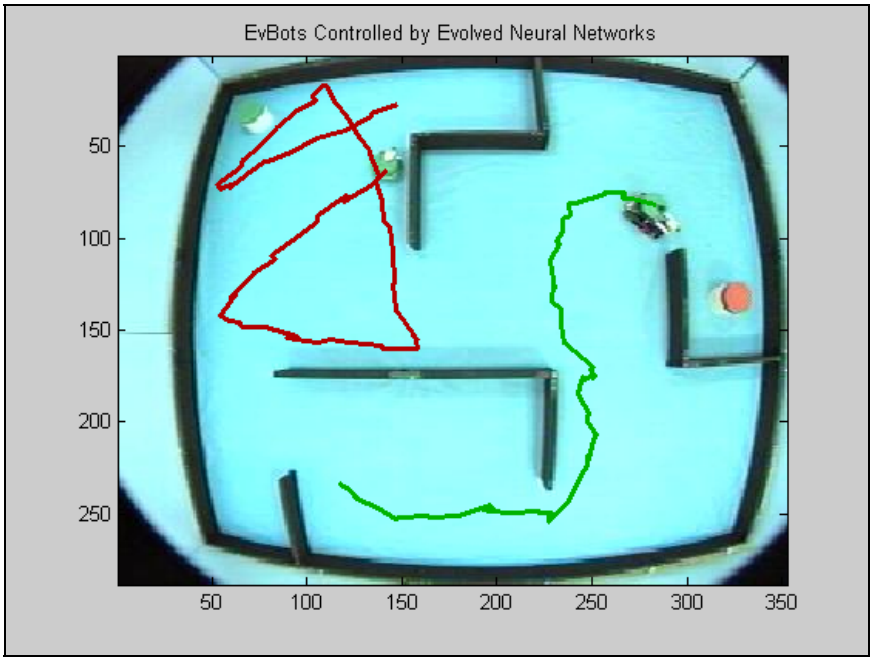


Figure 6.7: Two generations of EvBots playing together.

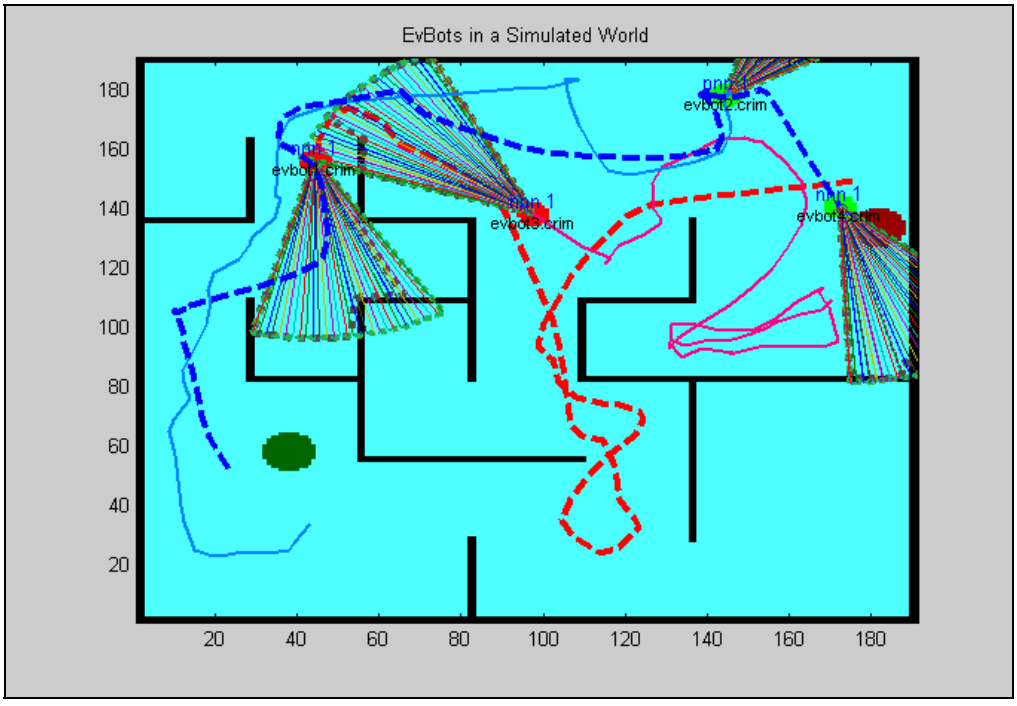


Figure 6.8: Simulated world with simulated EvBots running the same neural network controllers as the one used by the real robots (courtesy of Andrew Nelson, CRIM).

Section 6.2 – Experiments with the Data Acquisition System

In this section experiments designed to detect faults and to evaluate the performance and capabilities of the USB-DAQ8 data acquisition system were carried out. The first two experiments described here deal with the evaluation of subsystems and components used in the USB-DAQ8 board. First, the frequency response measurement of the implemented low-pass filters is presented. Second, a description of experimentation to test the quality of the analog to digital converter IC is given. Thirdly, experiments that test the data acquisition system as a whole are described, starting from the evaluation of achievable data transfer rates and ending with the demonstration of the capabilities and possible uses of the USB-DAQ8 system.

Section 6.2.1 – Test of the Low Pass Filter Frequency Response

The frequency response of the low-pass filters embedded in the USB-DAQ8 were measured experimentally to verify the designed cutoff frequency of 20 KHz. The obtained data validated design calculations and the quality of the integrated circuit LTC1563-3 by showing that the actual cutoff frequency is 20.07 KHz. This experimental data is summarized in the Figure 6.9 and can be found in Appendix A1.3.

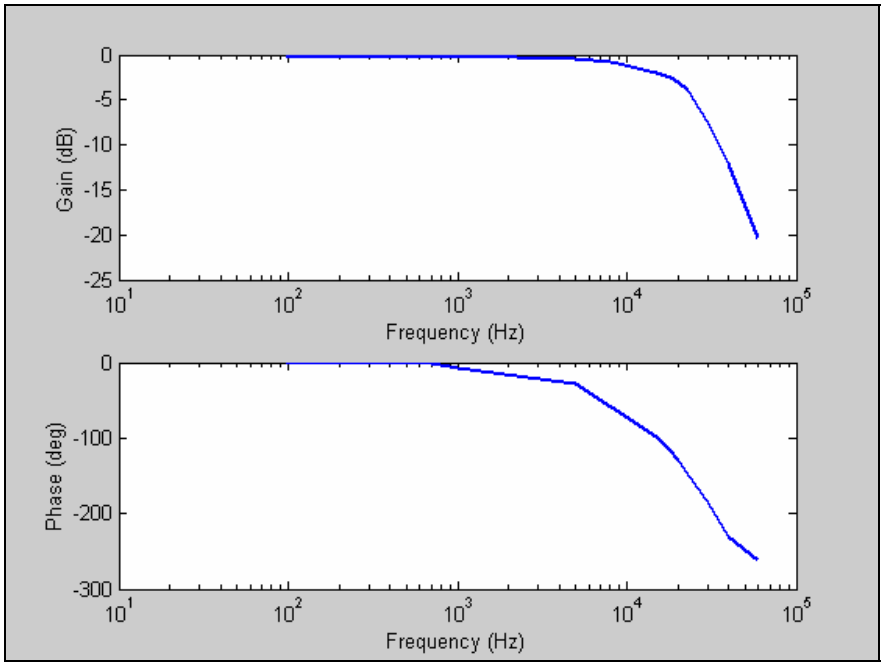


Figure 6.9: Frequency response USB-DAQ8's low-pass filter.

Section 6.2.2 – Test of the ADC Linearity and Frequency Distortion

As a way of testing the quality and reliability of the USB-DAQ8, tests were performed to analyze the main component in that system: the analog to digital converter integrated circuit. This was done by performing experiments designed to measure its linearity and frequency distortion. For the linearity tests, known input voltages were applied to the ADC's and the outputted digital values were recorded. The performance of the ADC08161C was good and the measured errors remained close to the specified resolution (±0.02V). The results obtained during this experiment are shown in Figure 6.10 and Figure 6.11.

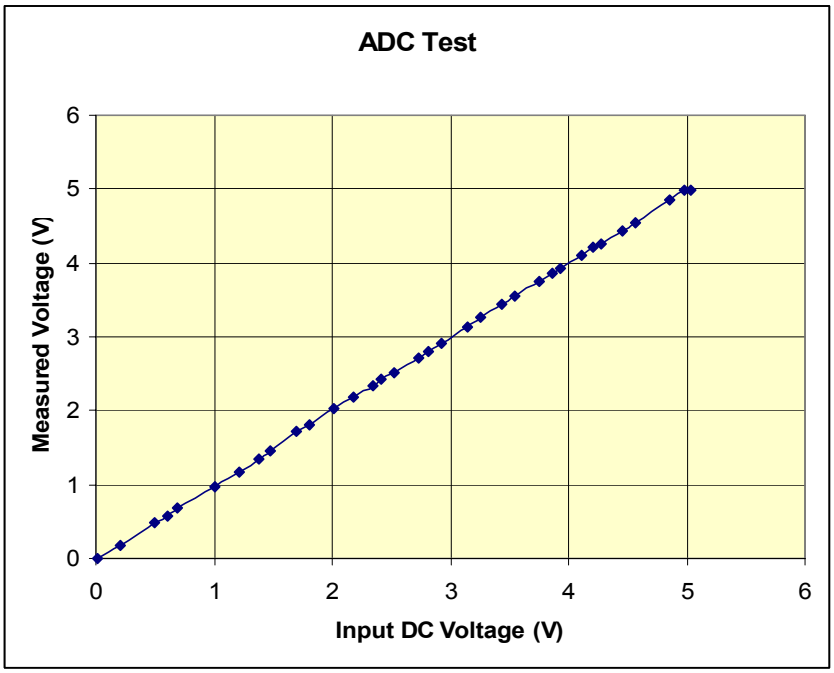


Figure 6.10: Results from the linearity test performed on the IC ADC08161C.

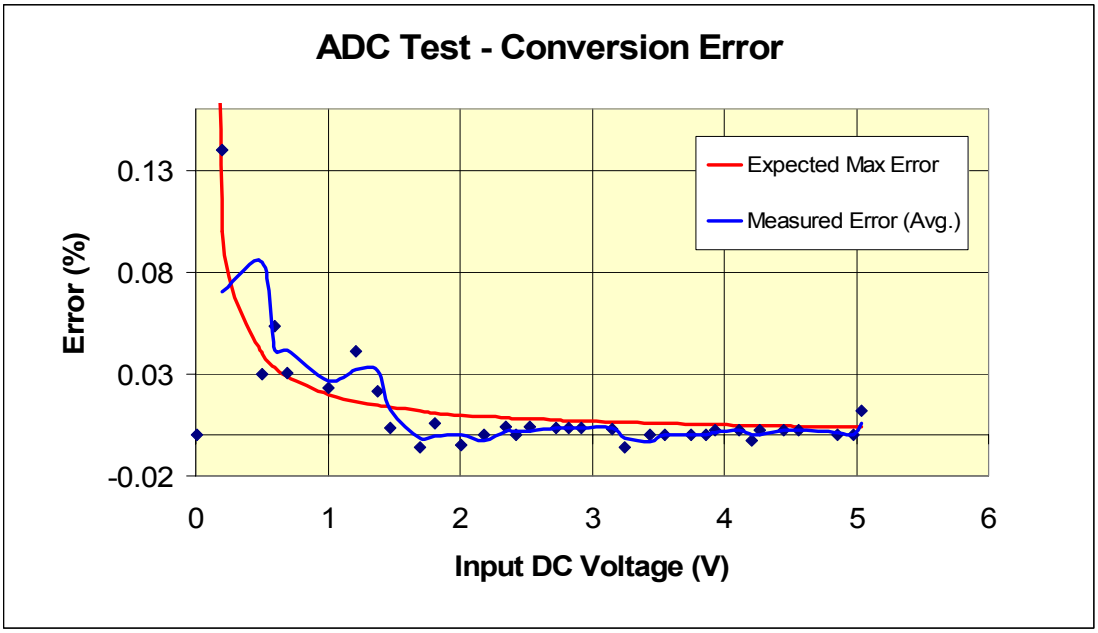


Figure 6.11: Results from the linearity test performed on the IC ADC08161C. The expected error reflects the ±0.02V resolution (5V / 256 levels).

The frequency distortion test performed on the ADC08161C consisted of the application of signals of known frequency to the IC's input, followed by the sampling process and later calculation of the signal's frequency components based on the Fourier transform of the obtained series. The obtained results are shown on the next figures and are positive, exhibiting a maximum measured frequency distortion of 1%.

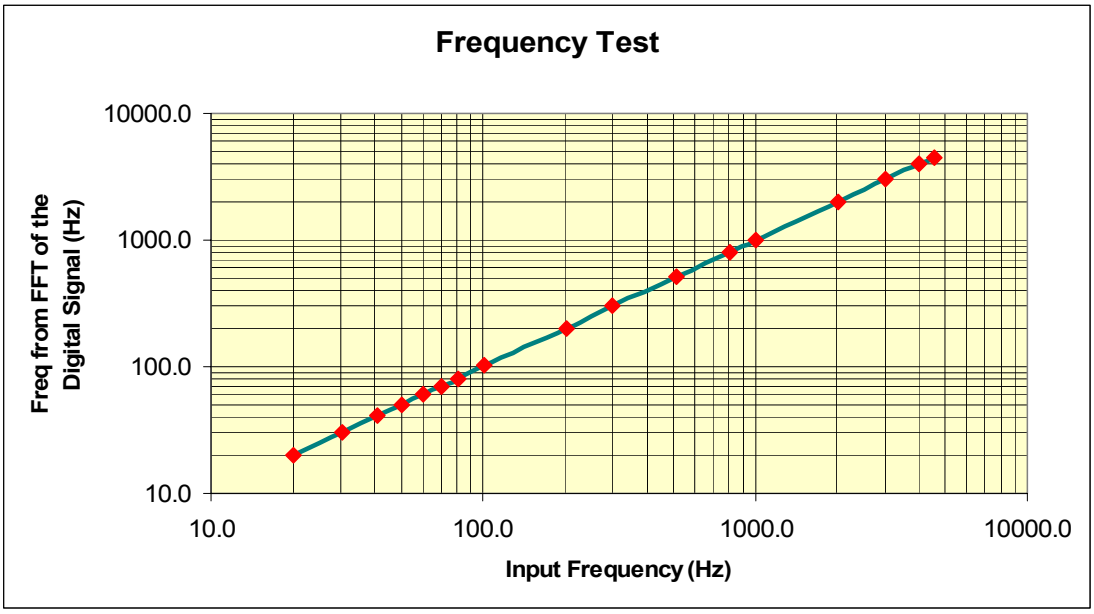


Figure 6.12: Results from the frequency distortion test performed on the IC ADC08161C and data acquisition system.

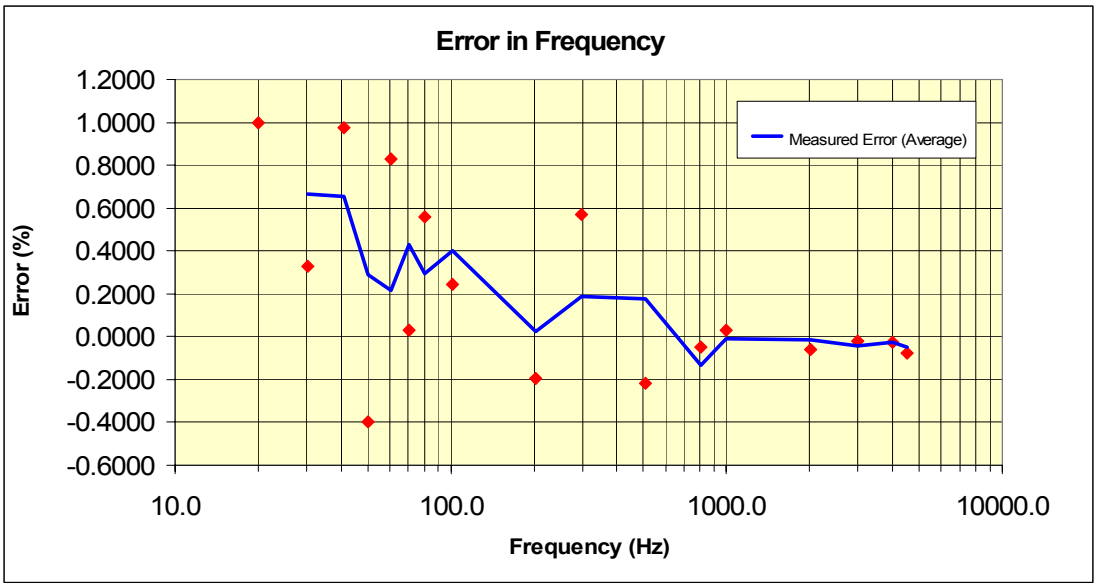


Figure 6.13: Errors measured during the frequency distortion test performed on the IC ADC08161C and data acquisition system.

Even though the tests were not performed using high-accuracy nor recently calibrated instruments, the obtained results were very consistent and demonstrated that the integrated circuit ADC08161C is a reliable component.

Section 6.2.3 – Test of the Data Transfer Speed

The sampling speed of the data acquisition system was originally designed to be 78.125 KHz per channel and use a resolution of 8 bits per sample. This corresponds to a data transfer speed greater than of 5 million bits per second (5 Mb/s) when control bits are considered, which was assumed to be feasible based on

datasheets information [A3.13]. After completion of the USB-DAQ8 implementation that assumption was put to a test and a design fault was found. The experiment described in this section showed that, although the USB-DAQ8 is capable of managing such baud rates, the computer's USB port used for the experiment is not. The problem is that the EvBot's USB port is also limited and can only support low-speed USB (1.5 Mbps from USB Rev. 1.1 specifications). This design problem was addressed by reducing the sampling frequency of the USB-DAQ8 to 9600 samples per seconds per channel, requiring 614.4 Kbps for the data bits only. Experiments proved that this new sampling rate results in a reliable communication speed.

The data obtained from the experiments performed to measure data transfer speed between the USB-DAQ8 and a host computer are summarized in the next plots. Figure 6.14 and Figure 6.15 present the data obtained for the original sampling rate of 78.125 KHz per channel, and respectively show plots of the total number of bytes transferred and average transfer rate of data bytes as a function of the sampling time. The figures 6.16 and 6.17 present corresponding data for a sampling rate of 9600 Hz per channel. Each data point obtained from these experiments is an average of 100 trials.

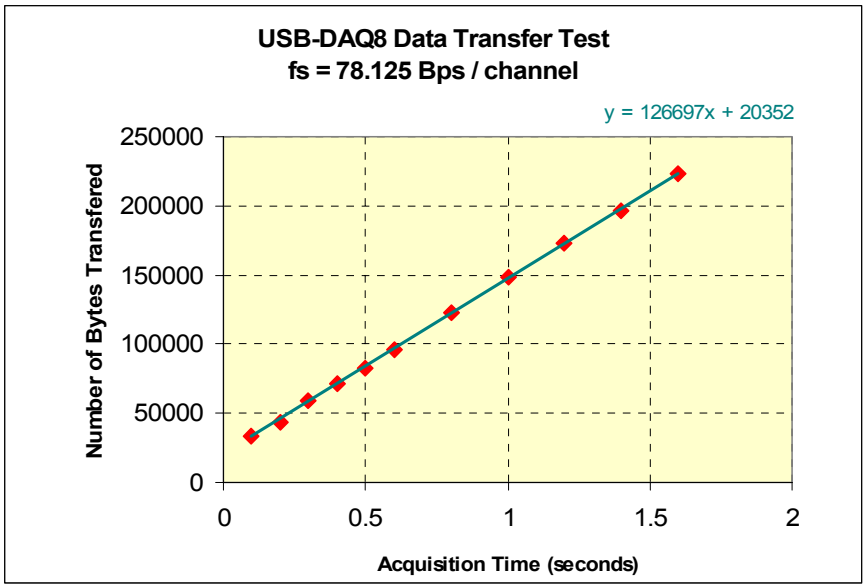


Figure 6.14: Total number of bytes transferred as a function of sampling time.

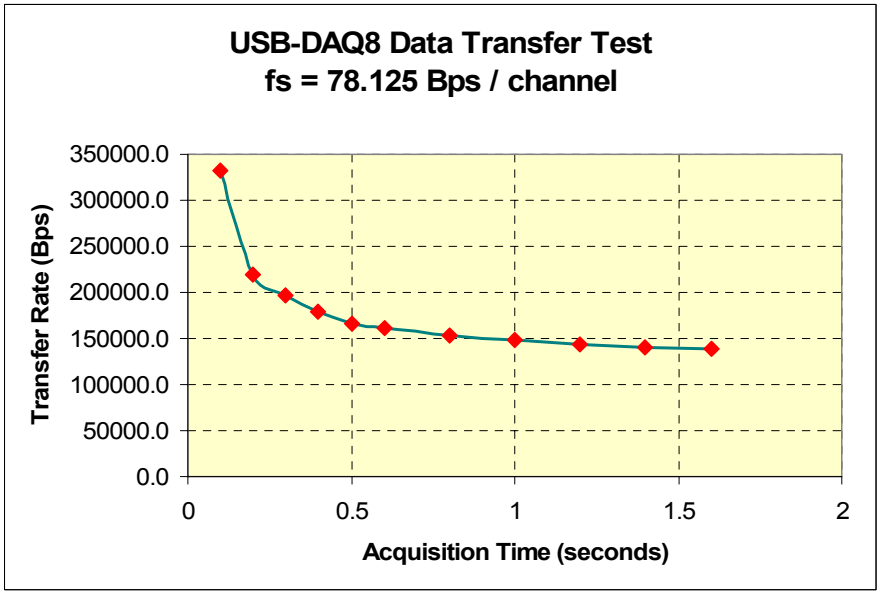


Figure 6.15: Transfer rate in bytes per second as a function of the sampling time.

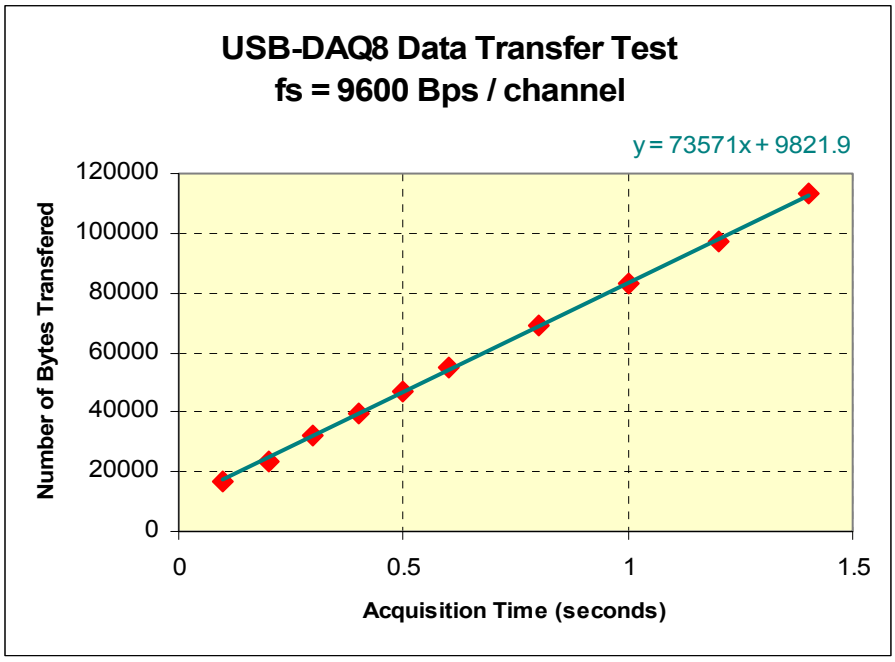


Figure 6.16: Total number of bytes transferred as a function of sampling time.

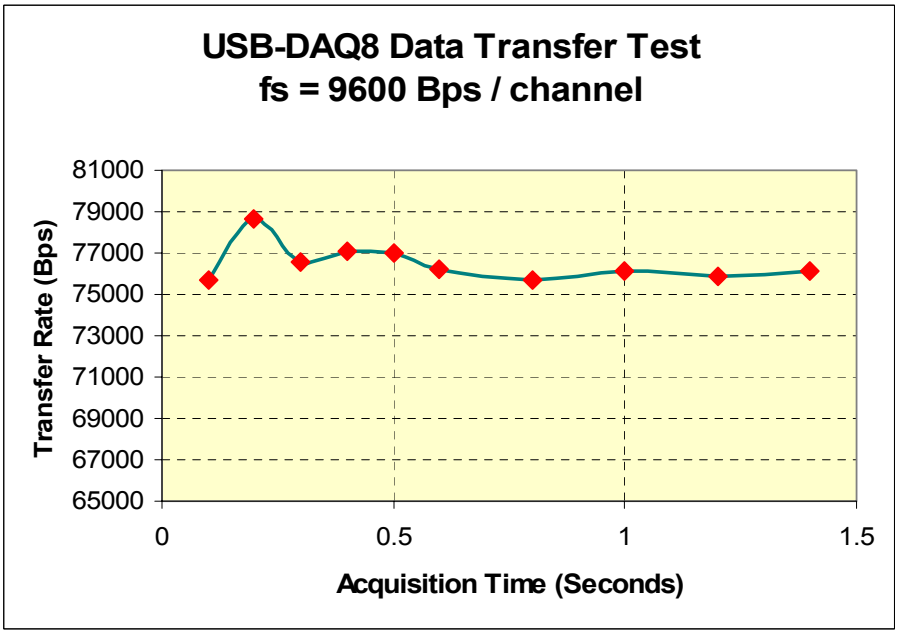


Figure 6.17: Transfer rate in bytes per second as a function of the sampling time.

Section 6.2.4 – Acquiring Data with the USB-DAQ8

After finalizing the assembly of the USB-DAQ8, its overall performance and functioning had to be tested, so software code was developed for this purpose. The created programs enabled the communications between the data acquisition system and a desktop computer, allowing for on/off control, data logging and data analysis. Innumerous experiments were performed and three of them were selected to be shown as examples in this section. The first two experiments consisted of sampling analog sine waves with known frequencies, followed by analysis of the collected data in the digital domain. In the first experiment a 202 Hz sine wave with 4.08 Vpp was sample using the USB-DAQ8, and in the second experiment the sine wave frequency was changed to 4.53 KHz. The obtained results, as well as a screen shot of the analog waves obtained from an oscilloscope, are shown in Figures 6.18 and 6.19. Note that the sampling frequency used by the USB-DAQ8 during these experiments was set to 9600 samples/sec/channel.

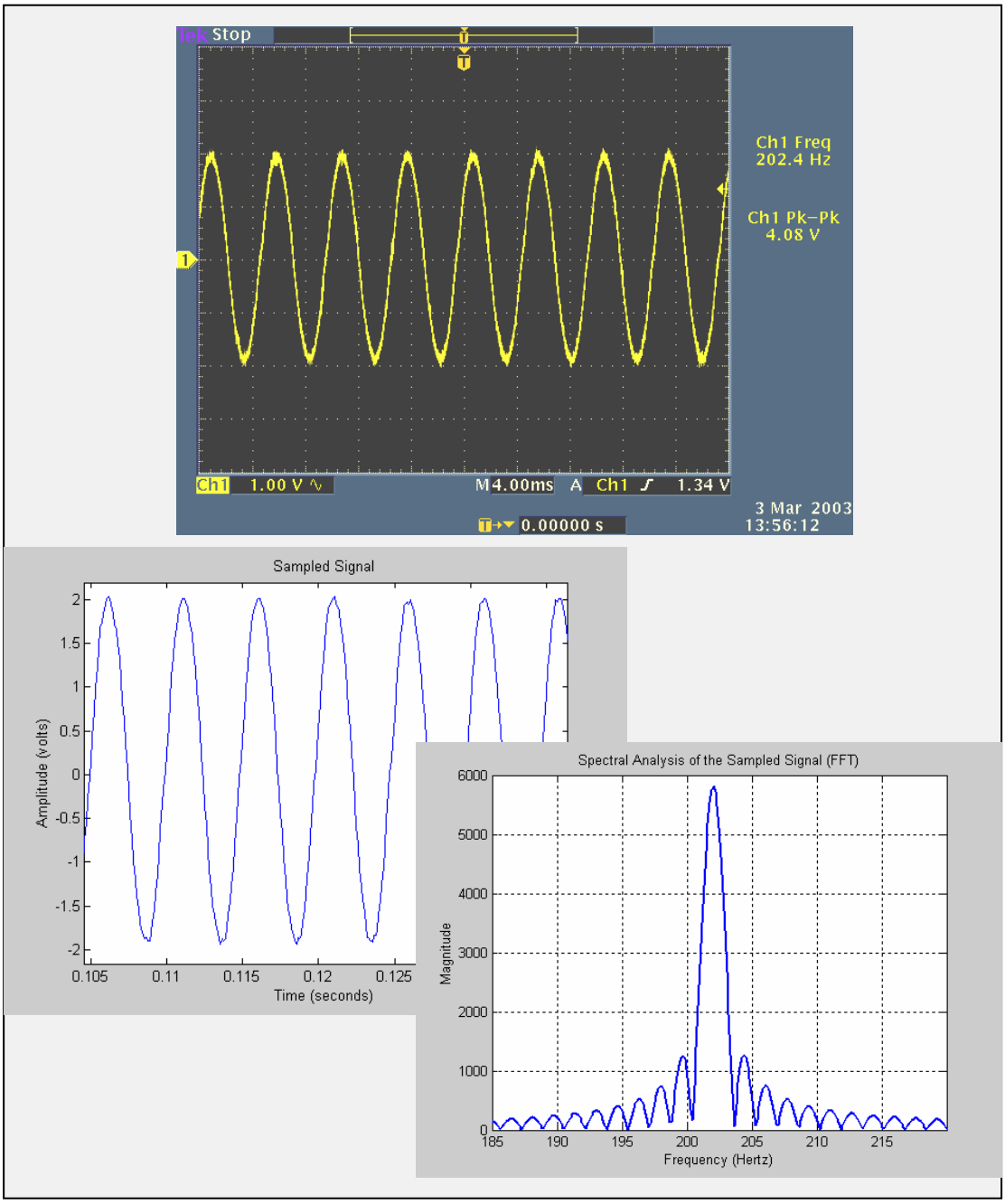


Figure 6.18: USB-DAQ8 acquiring a 202 Hz signal.

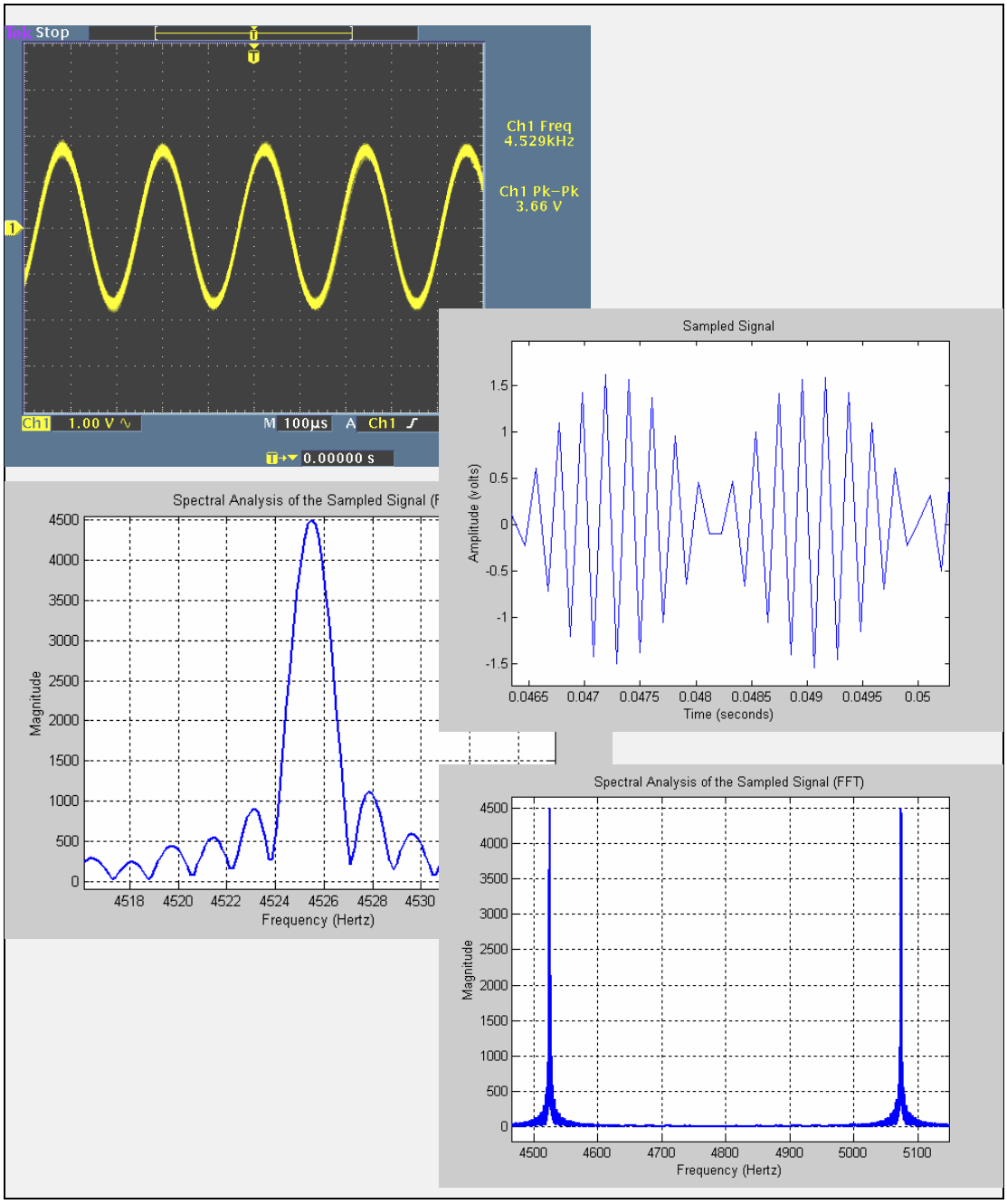


Figure 6.19: USB-DAQ8 acquiring a 4.53 KHz signal.

From the results presented in the above figures we can see that the data acquisition system works as expected, introducing little noise and frequency distortion.

The third experiment mentioned earlier consisted of simultaneously sampling and displaying the signals from all eight input channels of the USB-DAQ8. This function was implemented by a program developed to continuously gather and display data from the channels in eight separate plots, creating a quasi eight-channel digital oscilloscope. The program was called *USBscope* and a screen shot of it is shown in Figure 6.20.

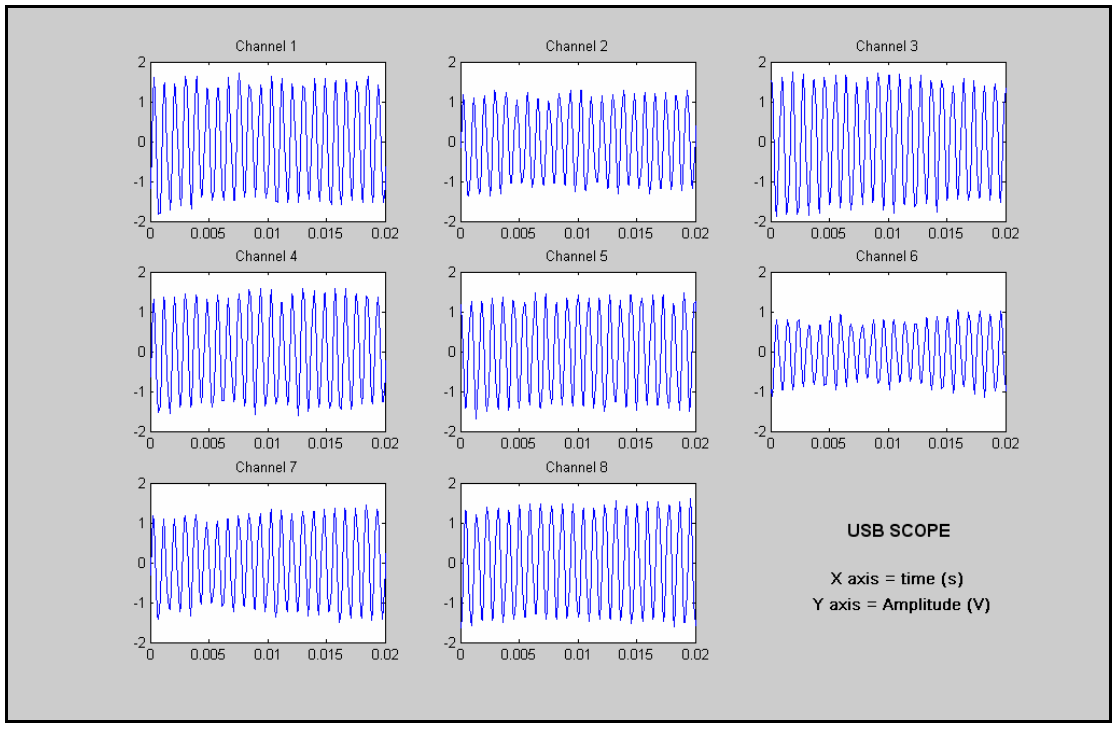


Figure 6.20: The program *USBscope* displaying data simultaneously sampled from all eight input channels of the USB-DAQ8.

Section 6.3 – Experiments with the Acoustic Array

The experimentation carried out on the acoustic array area consisted of systems simulations and analysis of the implemented array. The simulations were initially performed as a mean to select the desired acoustic array configuration for the EvBot, and later used to evaluate its performance through comparisons between obtained and expected results. Initially the experimentation with different configurations of acoustic arrays is presented. This is followed by the performance analysis of the implemented system. Finally experiments demonstrating the use of the acoustic array as a tracking sonar system are presented.

Section 6.3.1 – Beamforming by Different Array Configurations

The final design of the EvBot's acoustic array configuration was empirically performed by the use of the simulation software described in Chapter 4. During this process several configurations were analyzed, from which two were selected to be presented here as representative examples. Similar plots for the final acoustic array configuration have already been presented in Chapter 4 but are reproduced here for comparisons purposes.

One of the acoustic array configurations considered for the EvBot II consisted of a planar configuration that would fit on the top of the PC/104 stack. It was called *Planar10x10* in reference to its dimension of 10 cm^2, and the beam pattern obtained from that array is presented in Figure 6.21.

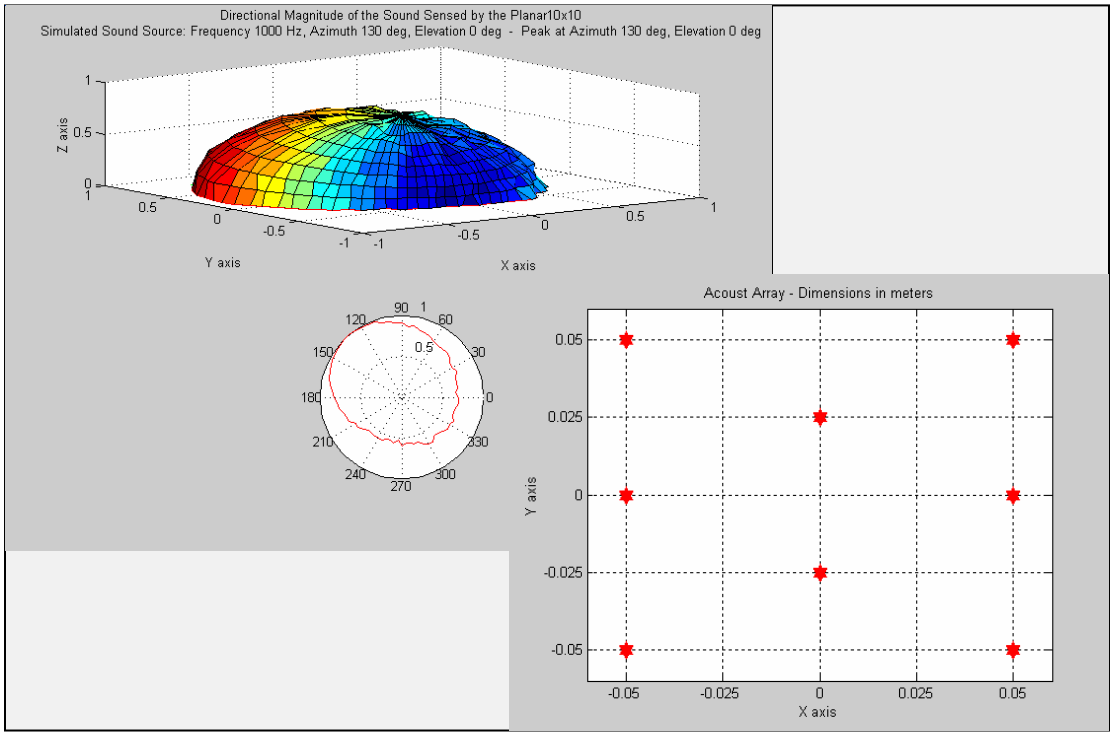


Figure 6.21: Beamforming simulation for a frequency of 1 KHz using a planar array that would fit on the top of the PC/104 stack.

The second simulated array configuration presented here consists of a three dimensional configuration resembling a pyramid. For that reason it was called *PyramidArray* and it was also designed to fit the EvBot II body. The obtained beam pattern from this array configuration for a sound frequency of 1 KHz is presented in Figure 6.22.

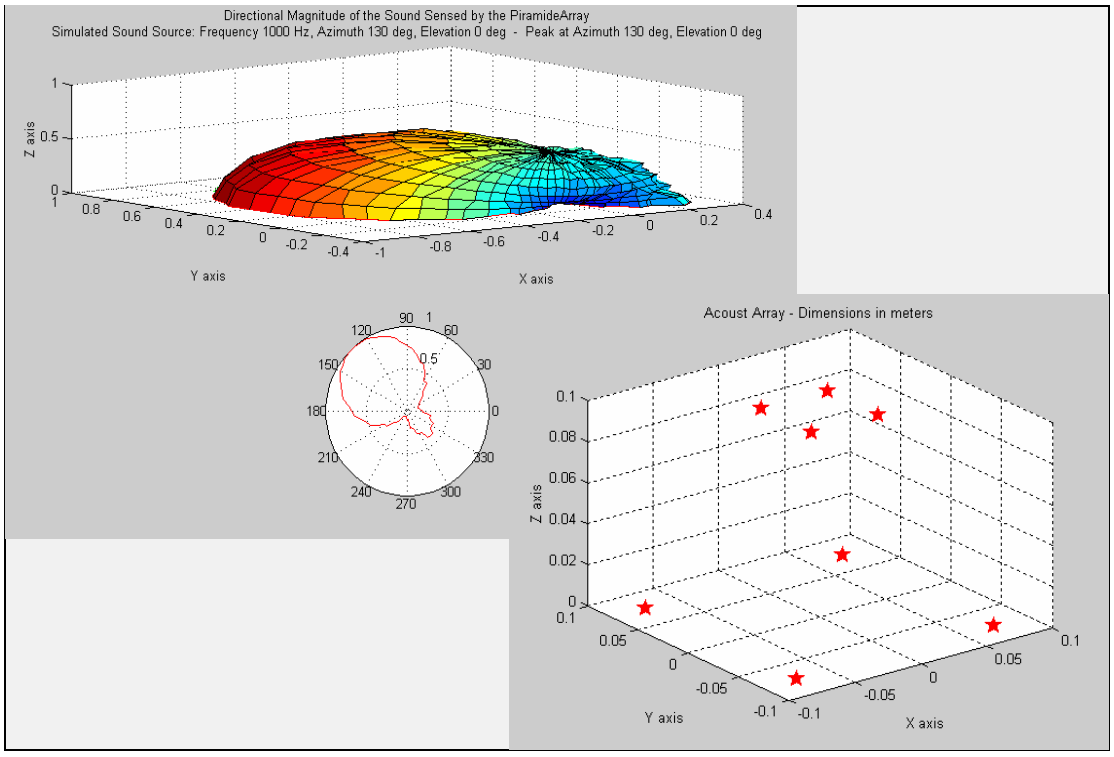


Figure 6.22: Beamforming simulation for a frequency of 1 KHz using a 3-D array configuration that could fit on the EvBot II body.

From the figures above it can be seen that the larger size of the *PyramidArray* improved the directional resolution for the selected frequency, presenting a narrower beam when compared to the one produced by the *Planar10x10* array. This phenomenon shows the proportional relationship that exists between the sound wavelength and the ideal distances among sensors when beamforming is desired, i.e., the longer the sound wavelength, the larger the distances between the microphones should be to produce an effective interference pattern. This will be further noticed by examination of the beamforming characteristics of the *EvBotArray*, which is an even larger array configuration. The *EvBotArray* is the array configuration selected for implementation on the EvBot II.

The comparison of the beam pattern plots in Figures 6.21 and 6.22 also shows that the beam size was reduced as a whole, reflecting on increased resolution for both azimuth and elevation angles.

The beam pattern generated by the *EvBotArray* is presented in Figure 6.23 and shows that a larger array configuration provided further improvements on the directional resolution of azimuth angles at the 1 KHz frequency range. This array was designed to fit the EvBot II shield and also uses a 3-D configuration.

The observation of the beam pattern plot for the *EvBotArray* also shows that the elevation angle resolution was somewhat decreased from the one obtained by the use of the *PyramidArray*. This change is believed to be result of a reduction on the height of the array but this phenomenon wasn't deeply studied because the research focus was on a system capable of good azimuth resolution.

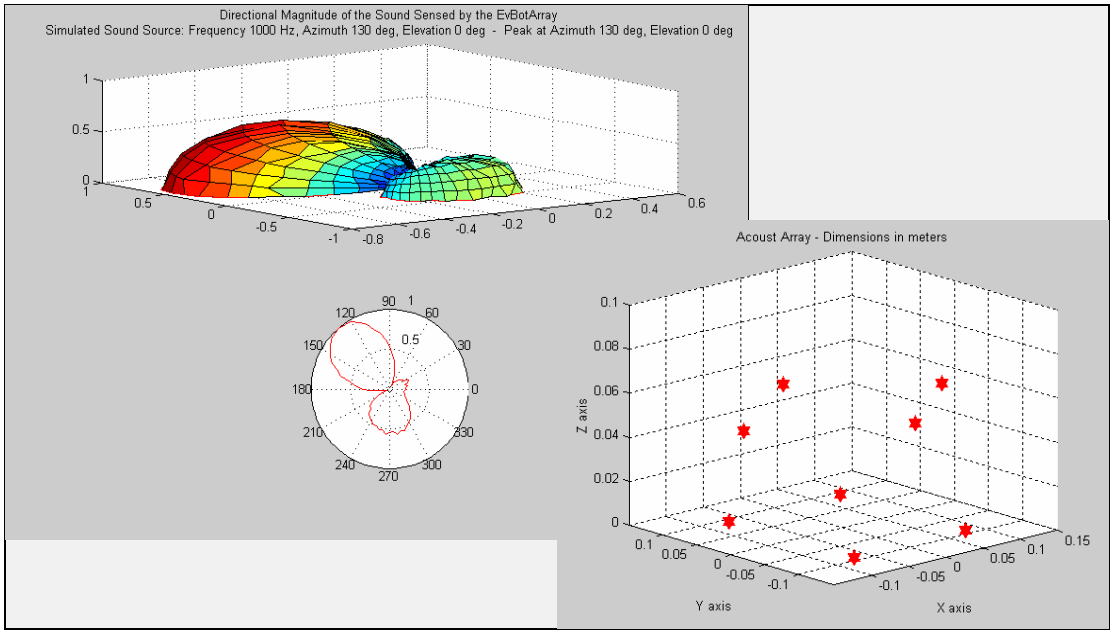


Figure 6.23: Beamforming simulation for a frequency of 1 KHz using the final array configuration selected for the EvBot II.

Section 6.3.2 – Evaluation of the EvBot's Acoustic Array System

The experiments realized to evaluate the performance of the implemented acoustic array system consisted of using real data to perform beamforming. Several trials were carried out for a diverse number of sound frequencies and sound source positions, but only a few examples were selected to be presented in this section. In such examples the sound source was kept on a fixed position and data was collected for sound frequencies ranging from 200 Hz to 1500 Hz. The acquired data was then used to generate plots of the directional sound intensities which were compared to similar plots generated by simulated data.

The plots created during this experiment are displayed in the figures 6.24 through 6.25, and clearly show that the performance of the implemented acoustic array system is very similar to what was expected from simulations, but only up to frequencies around 1500 Hz. For higher sound frequencies the actual beam pattern starts to deviate from the simulated ones, but no conclusion was reach about this effect, only that further investigation is necessary.

Another interesting note about the plots created during this experimentation is that they clearly show the changes in the beam pattern formed for different sound frequencies. From the plots we can see that at low frequencies the beam patterns are very broad, but as the sound frequency increases the beams get narrower. From these observations it was noted that the best directionality for the implemented acoustic

array occurs for frequencies around 1200 Hz. In that frequency range the beam formed is relatively narrow and the secondary beams are relatively small.

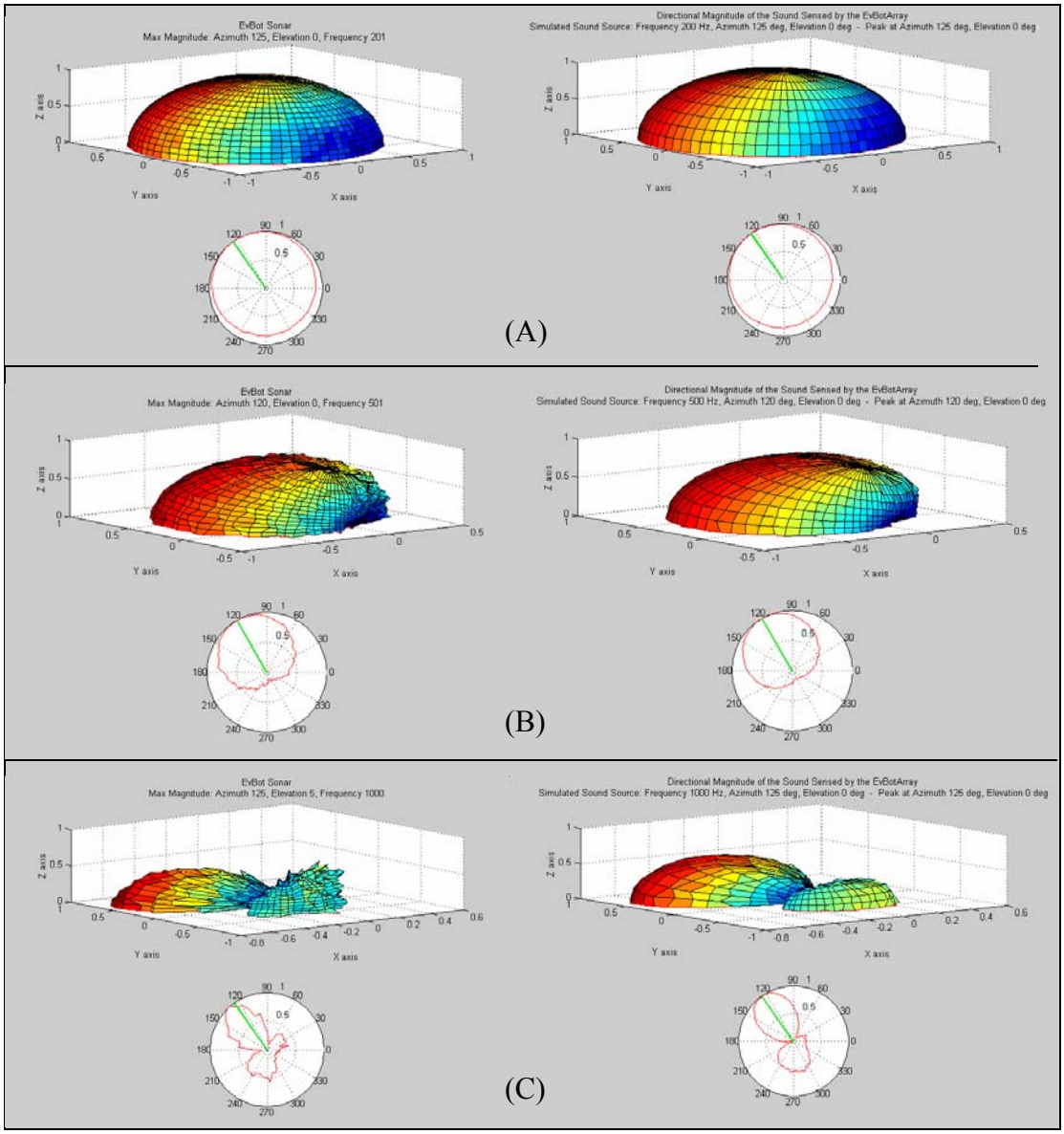


Figure 6.24: Comparisons between beam patterns obtained from real data (right) and simulated data (left) for the following sound frequencies: (A) 200 Hz. (B) 500 Hz. (C) 1000 Hz.

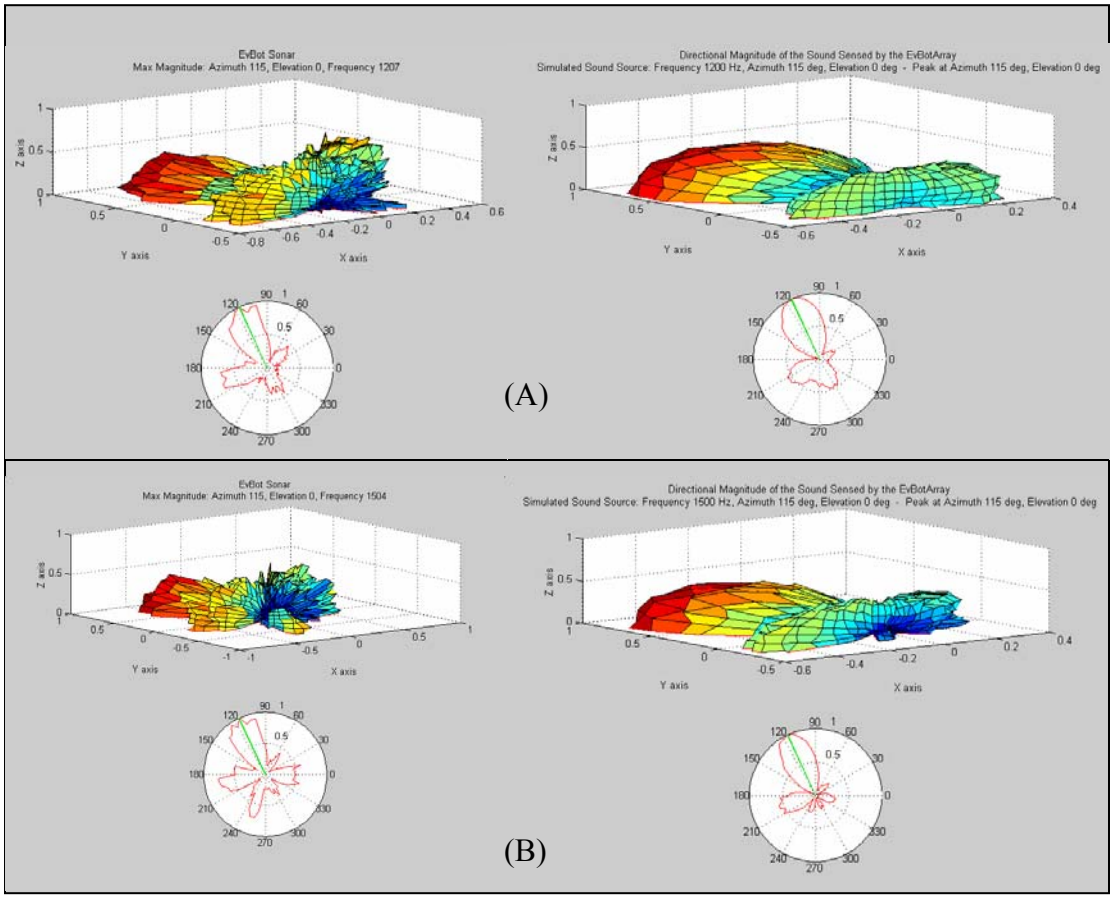


Figure 6.25: Comparisons between beam patterns obtained from real data (right) and simulated data (left) for the following sound frequencies: (A) 1200 Hz. (B) 1500 Hz.

Section 6.3.3 –Using the Acoustic Array as a Tracking Sonar

The usefulness of the developed acoustic array as a tracking sonar device was studied through experiments based on the program *EvBot_TrackingSonar.m*. As described in Chapter 4, this program makes use of regularly sampled acoustical data to generate waterfall plots of the directional sound intensities and frequency

components, so the performed experiments consisted of the generation and analyzes of such plots. Experiments were performed for several real-object sounds, such as helicopters, trucks and airplanes, which were played back on a speaker. Some single-tone sounds were also tested by the use of a function generator. A sample of the obtained plots is shown on the next figures.

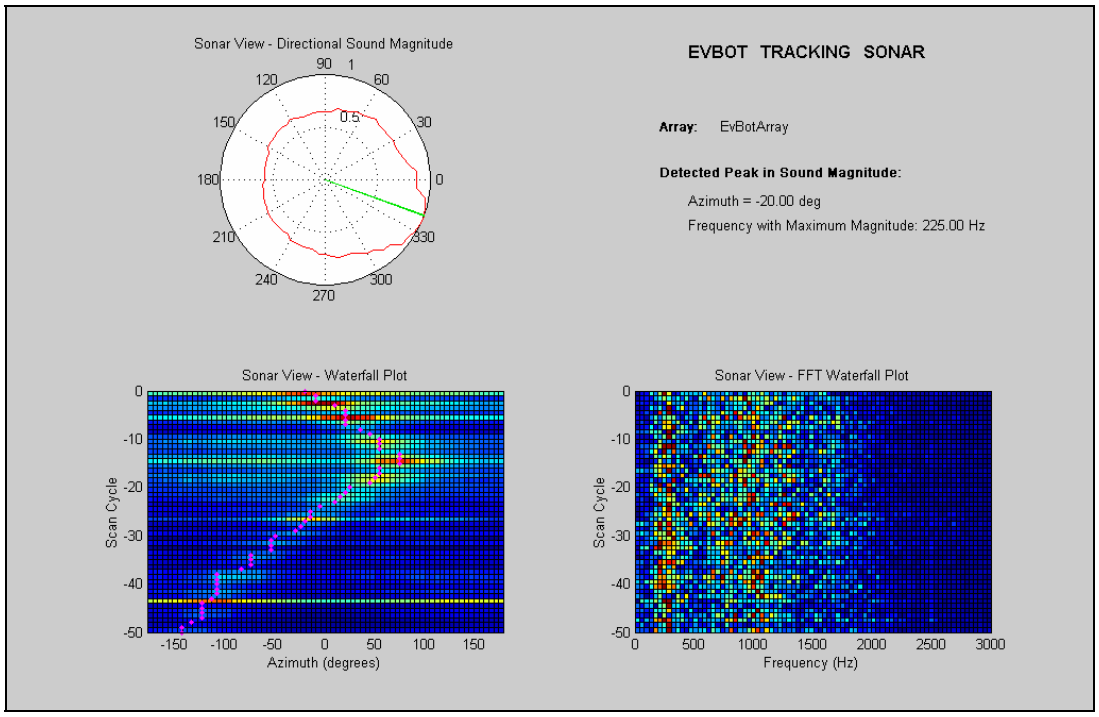


Figure 6.26: Acoustic array system being used to track the sound of truck reproduced by a nearby moving speaker.

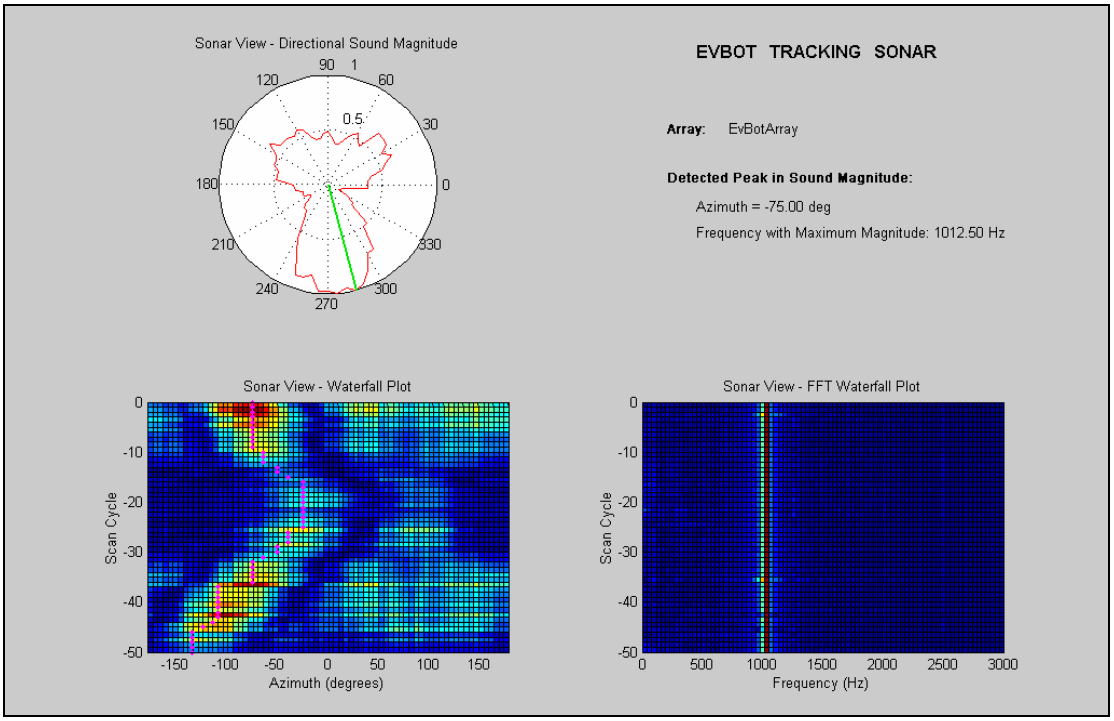


Figure 6.27: Acoustic array system being used to track a single-tone sound source.

From the observation of the plots in Figures 6.26 and 6.27 it can be noticed that the acoustic array system works well as a tracking device. It was able to successfully track all played-back sounds tested and shows that the waterfall plots are a fine way to keep a history of surrounding sound events. Furthermore, the visualization of the frequency components provided by the FFT waterfall plot can be very useful for object identification and speed estimation through the analysis of the sound signatures and Doppler effects.

Section 6.4 – EvBot's Navigation by Sound

The final set of experiments performed during this research consisted of testing the capabilities the EvBot to use its acoustic array to navigate towards a sound source. This was performed by the development of a controller program responsible to gather and process the data from the array of sensors, generating movement commands as a result. This program is described in Chapter 4 and is the first version of the *EvBot_TrackingSonar.m*.

The performed experiments proved that the design of this new sensor system for the EvBot was successful and able to provide reliable data. A screen shot showing the track followed by the EvBot II in one of the experiments is displayed in Figure 6.28, and clearly shows that the robot is able to turn and precisely move towards the sound source by correcting its bearing in the way.

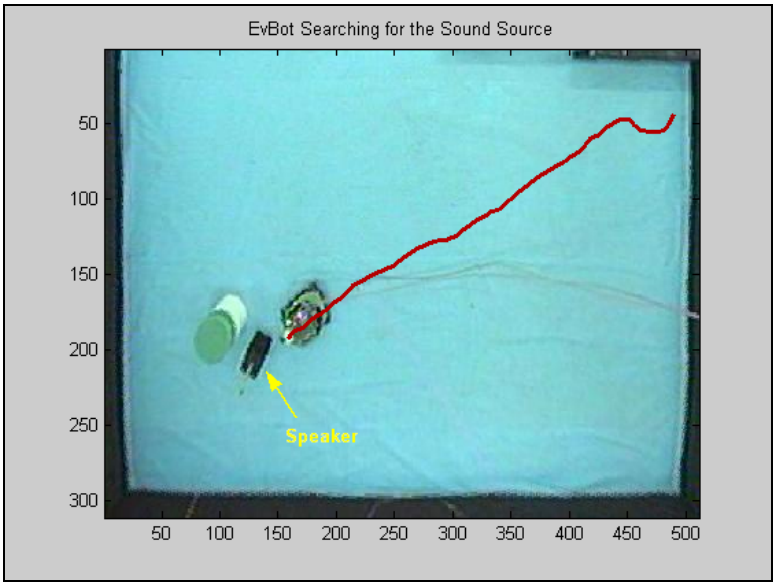


Figure 6.28: Path taken by the EvBot II to find the sound source.

Chapter 7 – Conclusion and Future Research

Section 7.1 – Concluding Remarks

The research work presented in this thesis has resulted in the development of a small and computationally powerful robotic platform for studying distributed and evolutionary robotics. Such robots are suited to application areas such as surveillance, reconnaissance and security. This robot, called EvBot II, was successfully created to enhance the sensing, mobility and intelligent control capabilities of its predecessor.

The EvBot II's high level processing was kept with the same configuration as in the previous generation, a PC/104 computer system which is able to host intelligent control software developed entirely in a MATLAB environment. On the other hand, the low level processing system was redesigned to make use of two microcontroller units serially connected to the CPU. These microcontrollers are able to effectively handle the closed loop control of up to three motors through the use of custom designed circuitry, and can also provide the input channels for several additional sensors if necessary. Sensor integration is seen as an important element of evolutionary robotics.

The efforts put into the expansion of the EvBot's sensing capabilities also resulted in the development and successful implementation of an acoustic array system. Such system is able to perform beamforming based on data collected from

eight microphones, and can be used by the EvBot on tasks like object identification or object tracking, as demonstrated by performed experiments. As part of the development of this acoustic array system a number of simulation and application software programs were created, generating a very useful resource for the study and development of other acoustic array configurations.

The successful design and realization of a data acquisition system with simultaneous sampling of eight audio channels was also part of the development of the acoustic array system, and created a very versatile plug-and-play device that can be used on any computer system equipped with an USB port.

In summary, the research presented in this thesis created the next generation of autonomous mobile robots, one that is small, robust and computationally powerful enough to provide integrated sensor feedback for intelligent control. In addition, experimentation demonstrated that all of the hardware and software designs were successful, and that the EvBot II and its subcomponents function within specifications.

Section 7.2 – Future Research

There are innumerous experiments in the areas of evolvable robotics, SAR and RSTA in which the EvBot II could be applied. Its capabilities could be very useful, for example, to test evolved systems designed to perform two tasks with different priorities, such as “go to sound source” and “avoid walls”, or to study the implementation of triangulation systems based on the use of two or more robots. Even completely different experiments than the ones mentioned in this thesis can be supported by the EvBot II platform, such as experimentation involving rule based controllers or remote control functionality.

Although the EvBot II platform has proven to be a remarkable robotic platform, there are still grounds for enhancements. The odometer system is an example of an area that still needs some work, so is the speed control system, where improvements are expected to reduce the inherent delay of the data gathering process, thus enabling a higher quality control. Modifications to the USB-DAQ8 system are also foreseen, especially to make it able to sample at higher frequencies while still transmitting data through slow USB channels.

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APPENDICES

Appendix 1 – Experimental Data

The following sections present tables and figures containing experimental data collected during the development and testing of the EvBot II platform, the USB-DAQ8 data acquisition system and the acoustic array system.

Section A1.1 – Calibration of the Open Loop Control System

The following tables contain the experimental data acquired while calibrating the open loop control of the EvBot II. Each value in the tables is an average of five trials.

Table A1.1: Calibration values obtained for linear motion.

Distance traveled in one second (inch)	Required PWM value
0.0	0
0.5	80
1.0	90
1.5	100
2.0	105
2.5	120
3.0	125
3.5	130
4.0	135
4.5	160
5.0	165
5.5	180
6.0	185
6.5	200
7.0	225
7.5	240
8.0	250
8.5	255

Table A1.2: Calibration values obtained for rotations.

Rotation angle	Time step (seconds)	LEFT PWM Value	RIGHT PWM Value	Product PWM x Time
0	0	0	0	0.00
10	0.3	-180	180	21.18
20	0.5	-190	190	37.25
30	0.6	-200	200	47.06
40	0.7	-220	220	60.39
50	0.8	-240	240	75.29
60	0.9	-250	250	88.24
70	1.1	-240	240	103.53
80	1.1	-250	250	107.84
90	1.3	-245	245	124.90
100	1.4	-250	250	137.25
110	1.5	-250	250	147.06
120	1.6	-250	250	156.86
130	1.7	-250	250	166.67
140	1.8	-255	255	180.00
150	2	-250	250	196.08
160	2.1	-253	253	208.35
170	2.3	-251	251	226.39
180	2.6	-253	253	257.96
-170	2.5	253	-253	248.04
-160	2.3	251	-251	226.39
-150	2	253	-253	198.43
-140	1.9	254	-254	189.25
-130	1.9	248	-248	184.78
-120	1.7	250	-250	166.67
-110	1.6	250	-250	156.86
-100	1.5	250	-250	147.06
-90	1.3	253	-253	128.98
-80	1.2	245	-245	115.29
-70	1.1	242	-242	104.39
-60	1	240	-240	94.12
-50	0.8	244	-244	76.55
-40	0.7	230	-230	63.14
-30	0.6	212	-212	49.88
-20	0.5	195	-195	38.24
-10	0.3	180	-180	21.18

Section A1.2 – EvBot II Speed Control Experiments

The following tables contain experimental data obtained during calibration and testing of the closed loop speed control system for the EvBot II. Each value in the tables is an average of five trials.

Table A1.3: Measured speed versus time for different commanded speeds

Commanded Speed	1	2	3	4	5	6
Time	**Speed (inches/sec)**					
0	0	0	0	0	0	0
1	0	0	0.1	0.25	1.25	1.77
2	0	1.25	2.483	4.5	5.1875	5.75
3	0.25	2	3.5	4.25	5.2625	5.77
4	0.75	2.42	3.334	3.917	5.05	7.28
5	1.58	2.205	3.166	4.783	5.31	5.93
6	1.09	2.292	3.667	4	5.13	6.65
7	1.205	1.833	2.833	4.3	5.56	6.47
8	1.125	2	3.247	4.56	5.5	6.63
9	1	2.3125	3.753	4.14	5.5	6.125
10	1.25	2.1875	2.917	4.425	5.375	6.45
11	0.91					
15	1.1675		3.325	4.375		6.303
20		2.1583		4.2		

Table A1.4: Measured distance traveled versus time for different commanded speeds

Commanded Speed	1	2	3	4	5	6
Time	Distance Traveled (inches)					
0	0	0	0	0	0	0
1	0	0	0.1	0.25	1.25	1.77
2	0	1.25	2.583	4.75	6.4375	7.52
3	0.25	3.25	6.083	9	11.7	13.29
4	1	5.67	9.417	12.917	16.75	20.57
5	2.58	7.875	12.583	17.7	22.06	26.5
6	3.67	10.167	16.25	21.7	27.19	33.15
7	4.875	12	19.083	26	32.75	39.62
8	6	14	22.33	30.56	38.25	46.25
9	7	16.3125	26.083	34.7	43.75	52.375
10	8.25	18.5	29	39.125	49.125	58.825
11	9.16					
15	13.83		45.625	61		90.34
20		40.083		82		

The data shown in the above tables was used to generate plots of the distance traveled versus time and speed versus time for each speed command value. These plots are shown in Figures A1.1 to A1.12.

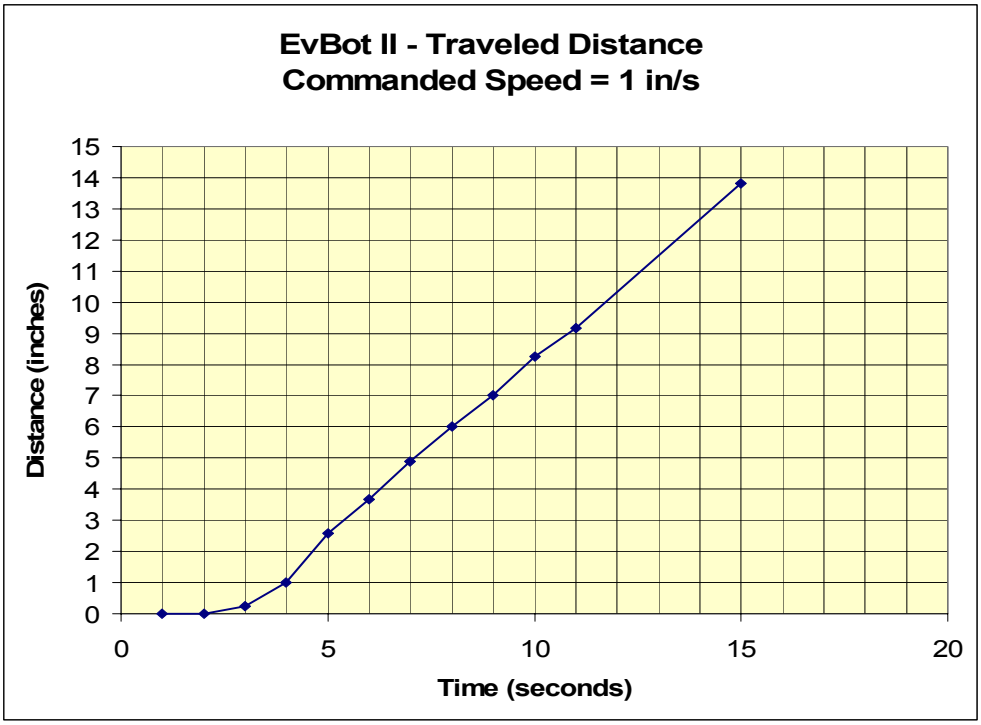


Figure A1.1: Measured distance traveled versus time for a commanded speed of one inch/second.

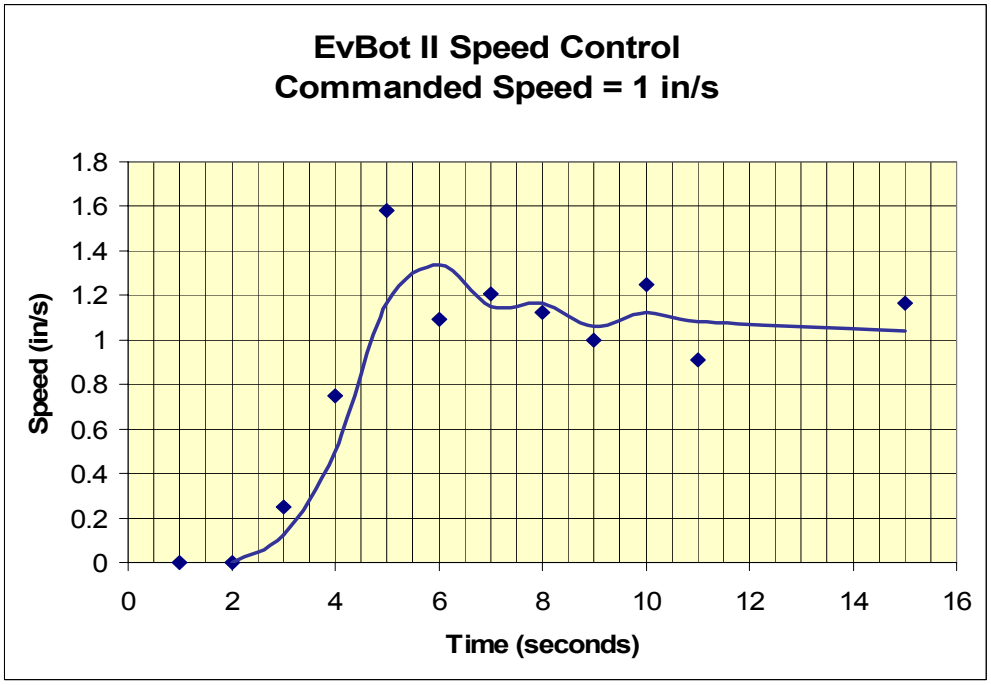


Figure A1.2: Plot of velocity versus time for a commanded speed of one inch/second.

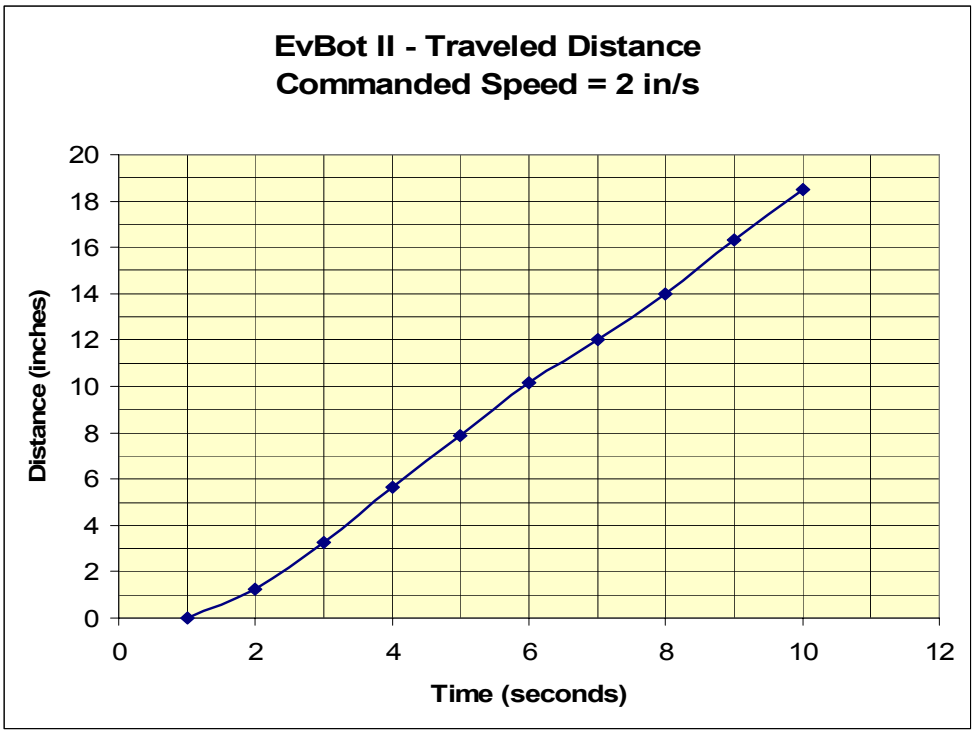


Figure A1.3: Measured distance traveled versus time for a commanded speed of two inches/second.

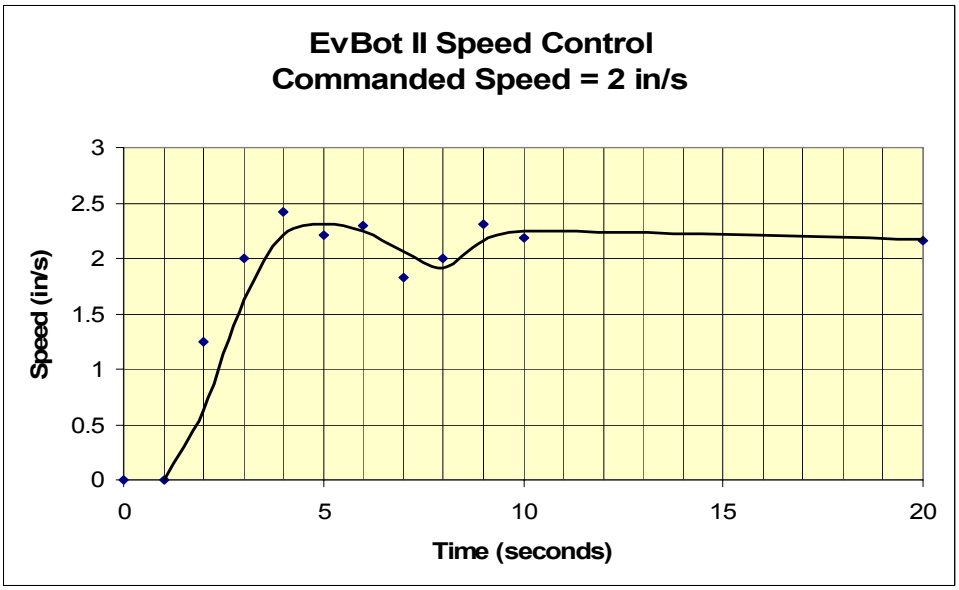


Figure A1.4: Plot of velocity versus time for a commanded speed of two inches/second.

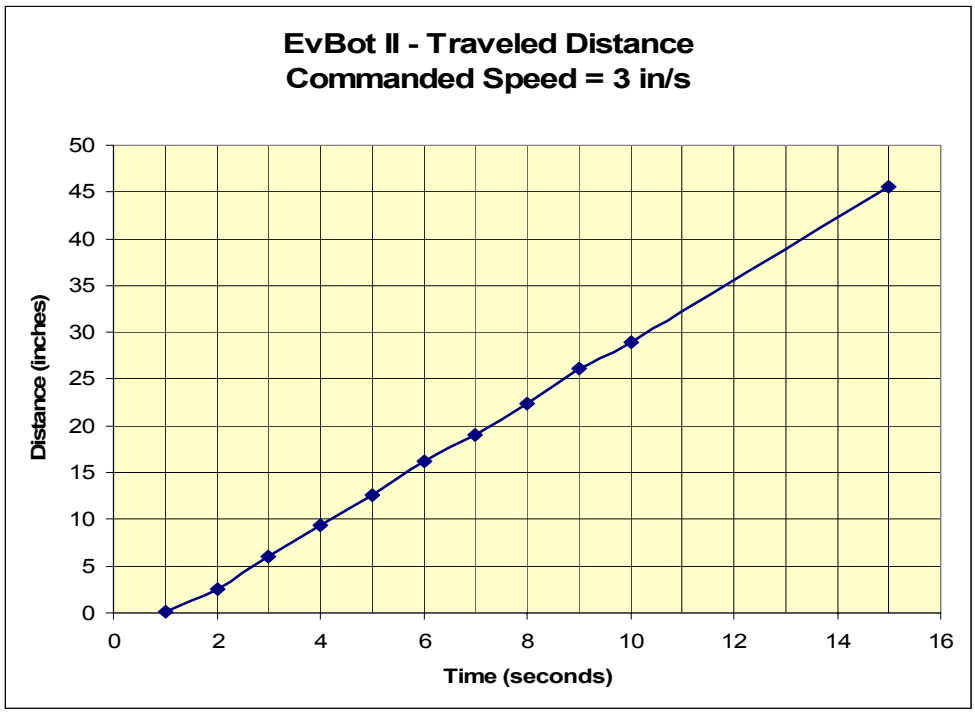


Figure A1.5: Measured distance traveled versus time for a commanded speed of three inches/second.

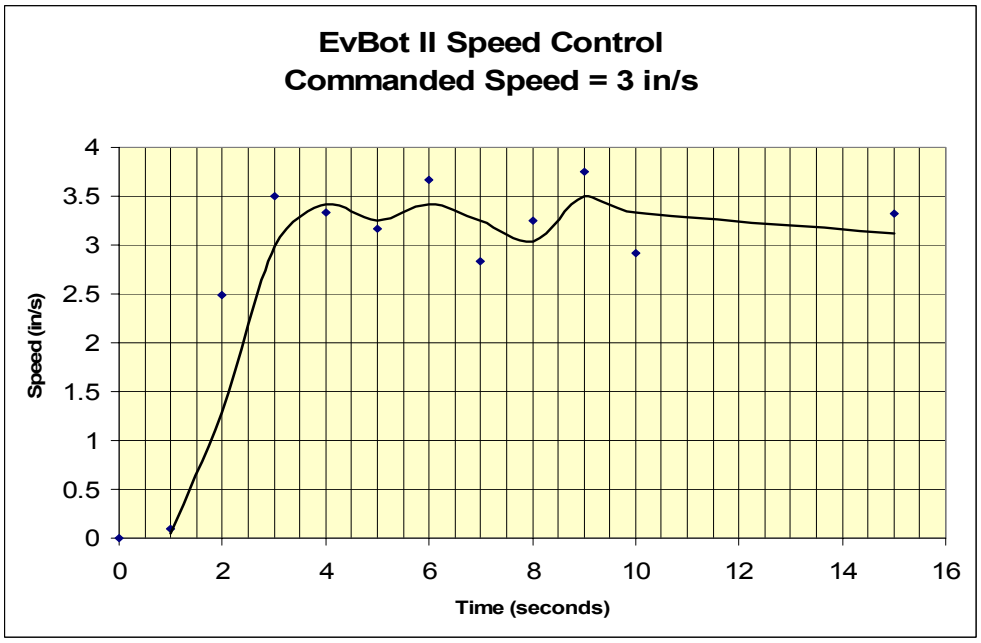


Figure A1.6: Plot of velocity versus time for a commanded speed of three inches/second.

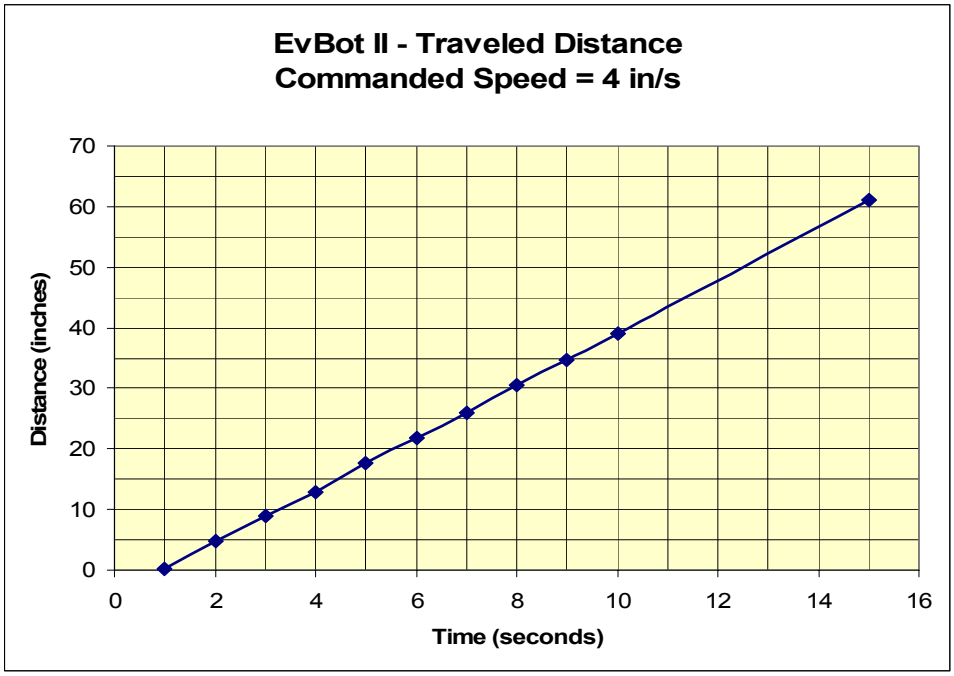


Figure A1.7: Measured distance traveled versus time for a commanded speed of four inches/second.

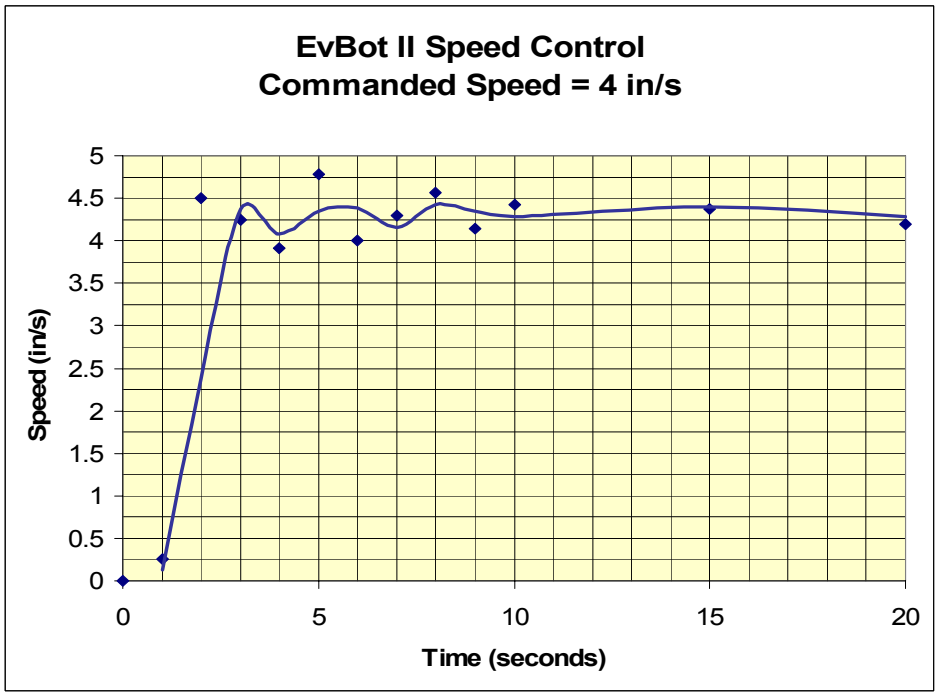


Figure A1.8: Plot of velocity versus time for a commanded speed of four inches/second.

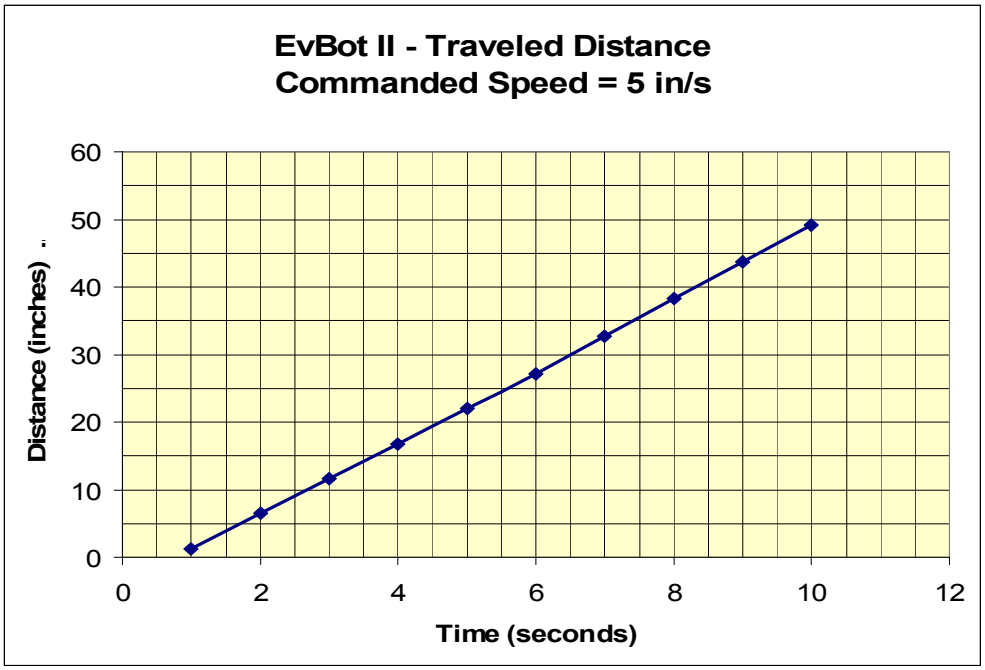


Figure A1.9: Measured distance traveled versus time for a commanded speed of five inches/second.

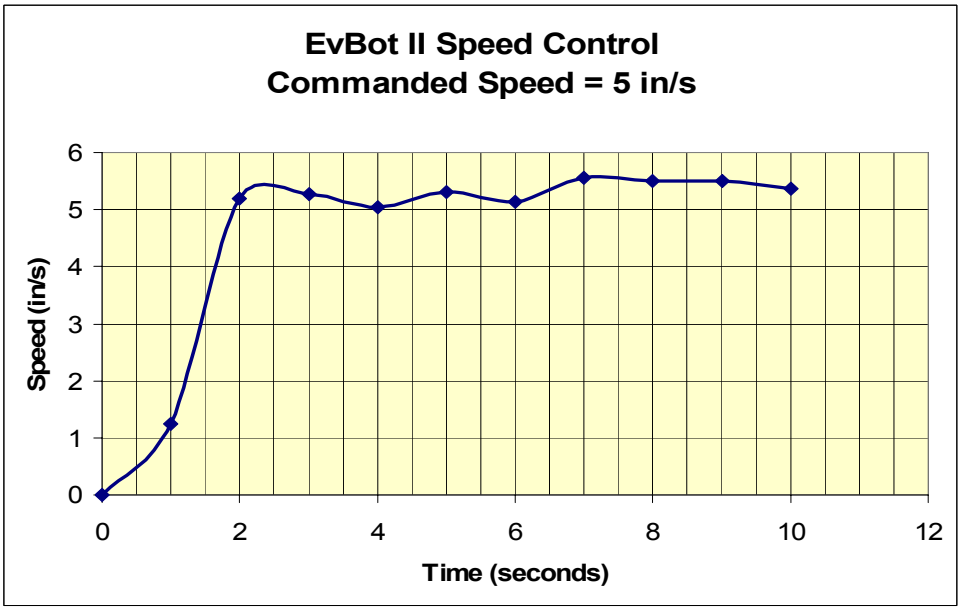


Figure A1.10: Plot of velocity versus time for a commanded speed of five inches/second.

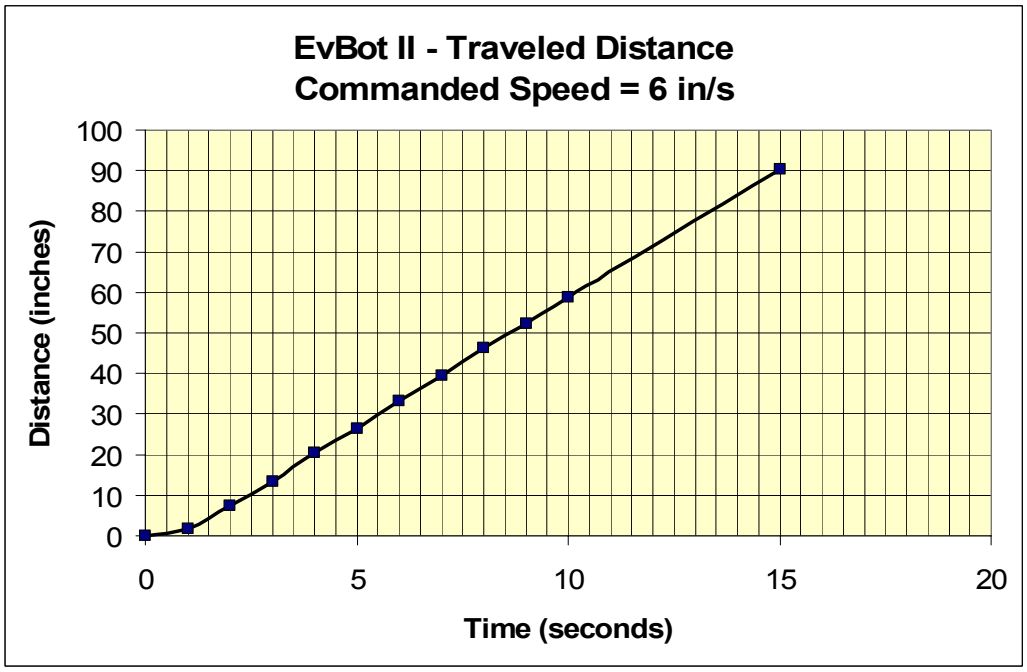


Figure A1.11: Measured distance traveled versus time for a commanded speed of six inches/second.

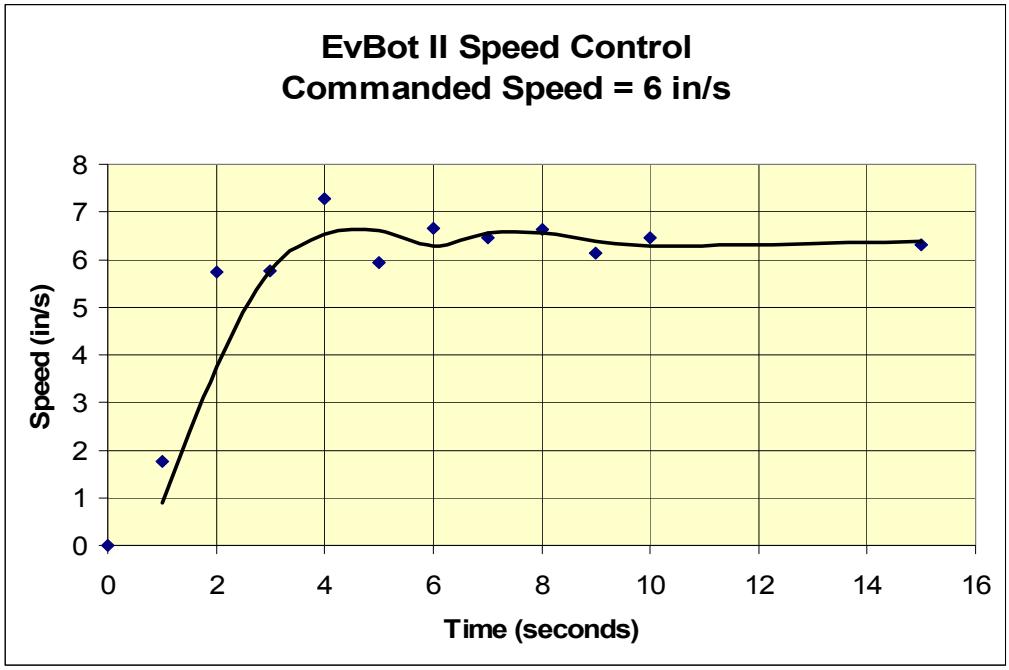


Figure A1.12: Plot of velocity versus time for a commanded speed of six inches/second.

Section A1.3 – Low-Pass Filter Characterization

The low-pass filters implemented on the USB-DAQ8 were experimentally tested and the following data was obtained.

Table A1.5: Measured values for gain and phase as a function of frequency.

Frequency	Gain	Phase
98	1	0
195	0.9798	0
390	0.9903	0
707	0.9709	0
1000	1	-7.2
4950	0.9533	-28.5
8160	0.9135	-58.75
15120	0.7961	-98
17960	0.7525	-116.38
20090	0.7075	-130.18
22940	0.6321	-148.6
30090	0.4227	-184.2
40000	0.2476	-230.4
60000	0.0947	-261.9

Section A1.4 – ADC Linearity and Frequency Distortion

The experimental data obtained from experiments with the analog to digital converter ADC08161C are shown in the next tables. Table A1.6 presents the data from the linearity tests. Table A1.7 presents data from the frequency distortion tests.

Table A1.6: Values obtained during the linearity test performed on the IC ADC08161C.

Input DC voltage	Measured DC voltage	Error (%)	Expected Error (from ±0.02V resolution)
0.01	0.01	0.000	2.000
0.20	0.17	0.140	0.100
0.50	0.49	0.030	0.040
0.60	0.57	0.053	0.033
0.70	0.67	0.030	0.029
1.00	0.98	0.023	0.020
1.21	1.16	0.041	0.017
1.38	1.35	0.022	0.014
1.47	1.47	0.003	0.014
1.70	1.71	-0.006	0.012
1.81	1.80	0.006	0.011
2.01	2.02	-0.005	0.010
2.18	2.18	0.000	0.009
2.35	2.34	0.004	0.009
2.42	2.42	0.000	0.008
2.53	2.52	0.004	0.008
2.73	2.72	0.004	0.007
2.82	2.81	0.004	0.007
2.92	2.91	0.003	0.007
3.15	3.14	0.003	0.006
3.25	3.27	-0.006	0.006
3.44	3.44	0.000	0.006
3.55	3.55	0.000	0.006
3.75	3.75	0.000	0.005
3.86	3.86	0.000	0.005
3.93	3.92	0.003	0.005
4.11	4.10	0.002	0.005
4.21	4.22	-0.002	0.005
4.27	4.26	0.002	0.005
4.45	4.44	0.002	0.004
4.56	4.55	0.002	0.004
4.86	4.86	0.000	0.004
4.98	4.98	0.000	0.004
5.04	4.98	0.012	0.004

Table A1.7: Values obtained during the frequency distortion test performed on the IC ADC08161C.

Analog Signal Frequency	Digital Signal Frequency (from FFT)	Error (%)
20.0	20.2	1.0000
30.3	30.4	0.3300
41.1	41.5	0.9732
50.3	50.1	-0.3976
60.4	60.9	0.8278
70.4	70.5	0.0284
80.5	81.0	0.5590
101.4	101.7	0.2465
202.4	202.0	-0.1976
298.1	299.8	0.5703
510.1	509.0	-0.2156
805.9	805.5	-0.0496
997.9	998.2	0.0301
2016.0	2014.8	-0.0620
2998.0	2997.3	-0.0233
3993.0	3992.0	-0.0250
4529.0	4525.5	-0.0773

Section A1.5 – USB-DAQ8 Data Transfer Rate Test

The data collected from performed experiments designed to measure the data transfer rates between the USB-DAQ8 and a host computer are show next. Table A1.6 presents data from the USB-DAQ8 trying to sample at 78.125 KHz, and Table A1.7 presents data for the reduced sampling rate.

Table A1.8: Results from data transfer tests performed while using a sampling frequency of 78.125 KHz. The values in the table represent and average of 100 trials performed for each acquisition time.

Sampling frequency = 78.125 KHz		
Acquisition Time (seconds)	Average Number of Bytes Received	Calculated Rate (Bps)
0.1	33259	332590.0
0.2	43982	219910.0
0.3	58898	196326.7
0.4	71883	179707.5
0.5	82899	165798.0
0.6	96305	160508.3
0.8	122683	153353.8
1.0	148255	148255.0
1.2	172555	143795.8
1.4	196224	140160.0
1.6	223181	139488.1

Table A1.9: Results from data transfer tests performed while using a sampling frequency of 9600 Hz. The values in the table represent and average of 100 trials performed for each acquisition time.

Sampling frequency = 9600 Hz		
Acquisition Time (seconds)	Average Number of Bytes Received	Calculated Rate (Bps)
0.1	16552	75670.1
0.2	23686	78626.3
0.3	32312	76589.6
0.4	39559	77049.3
0.5	47003	77036.6
0.6	54803	76231.6
0.8	69358	75727.2
1.0	82889	76137.5
1.2	97279	75864.1
1.4	112993	76091.8

Appendix 2 – Commands for the BasicX MCU's

This appendix presents the commands used for motion control and to gather data from the EvBot's BasicX microcontroller units. The commands must follow the described formats for proper functioning of the robot's motion system.

The BasicX MCU's have the following commands available:

Motion Commands

P	Set the PWM duty-cycle for motor 1 and motor 2
M	Set the speed for motor 1 and motor 2 (use feedback control)
T	Set the PWM duty-cycle for motor 3
N	Set the speed for motor 3 (use feedback control)
S	Stop all motors and return speed control errors

Speed Control Setup Commands

K	Set the control proportional gain for motor 1 or motor 2
C	Set the control proportional gain for motor 3

I/O Commands

R	Read a digital input pin from the master BasicX
I	Read a digital input pin from the slave BasicX

P command

Description

Set the PWM duty-cycle for motor 1 (right motor) and motor 2 (left motor).

Syntax

[P] [LeftDir|RightDir] [LeftPWM] [RightPWM] or

[p] [LeftDir|RightDir] [LeftPWM] [RightPWM]

Arguments Description

Item	Type	Description
[P] or [p]	Byte	ASCII(P) = 80 ASCII(p) = 112
[LeftDir|RightDir]	Byte	Bit 0: Right direction Bit 1: Left direction 0 = Forward 1 = Backward
[LeftPWM]	Byte	PWM duty-cycle for the left motor 255 = 100%
[RightPWM]	Byte	PWM duty-cycle for the right motor 255 = 100%

Return Value

If success, return [P].

Related MatLab file

setpwm.m

M command

Description

Set the speeds for motor 1 (right motor) and motor 2 (left motor). The motor speed is controlled using feedback from wheel encoders.

Syntax

[M] [LeftDir|RightDir] [LeftSpeed] [RightSpeed] or

[m] [LeftDir|RightDir] [LeftSpeed] [RightSpeed]

Arguments Description

Item	Type	Description
[M] or [m]	Byte	ASCII(M) = 77 ASCII(m) = 109
[LeftDir|RightDir]	Byte	Bit 0: Right direction Bit 1: Left direction 0 = Forward 1 = Backward
[LeftSpeed]	Byte	Left motor speed 255 = maximum speed
[RightSpeed]	Byte	Right motor speed 255 = maximum speed

Return Value

If success, return [M].

Related MatLab file

setspeed.m

T command

Description

Set the PWM duty-cycle for third motor.

Syntax

[T] [TransverseDir] [TransversePWM] or

[t] [TransverseDir] [TransversePWM]

Arguments Description

Item	Type	Description
[T] or [t]	Byte	ASCII(T) = 84 ASCII(t) = 116
[TransverseDir]	Byte	Bit 0: Direction 0 = Rightward 1 = Leftward
[TransversePWM]	Byte	PWM duty-cycle for the transverse motor (255 = 100%)

Return Value

If success, return [T].

Related MatLab file

setpwm3.m

N command

Description

Set the speeds for motor 3 (transverse motor). The motor speed is controlled using feedback from a wheel encoder.

Syntax

[N] [TransverseDir] [TransverseSpeed] or

[n] [TransverseDir] [TransverseSpeed]

Arguments Description

Item	Type	Description
[N] or [n]	Byte	ASCII(N) = 78 ASCII(n) = 110
[TransverseDir]	Byte	Bit 0: Direction 0 = Rightward 1 = Leftward
[TransverseSpeed]	Byte	Transverse motor speed 255 = maximum speed

Return Value

If success, return [N].

Related MatLab file

setspeed3.m

R command

Description

Read a digital input pin from the master BasicX (BasicX 1).

Syntax

[R] [I/O pin number] or

[r] [I/O pin number]

Arguments Description

Item	Type	Description
[R] or [r]	Byte	ASCII(R) = 82 ASCII(r) = 114
[I/O pin number]	Byte	0 = 0 ... 9 = 9, A = a = 10 ... z = Z = 35

Return Value Syntax

[R] [pin value]

Return Arguments Description

Item	Type	Description
[R]	Byte	ASCII(R) = 82
[pin value]	Byte	0 or 1 in ASCII ASCII(0) = 48 ASCII(1) = 49

Related MatLab file

readpin.m

I command

Description

Read a digital input pin from the slave BasicX (BasicX 2).

Syntax

[I] [I/O pin number] or

[i] [I/O pin number]

Arguments Description

Item	Type	Description
[I] or [i]	Byte	ASCII(I) = 73 ASCII(i) = 105
[I/O pin number]	Byte	0 = 0 ... 9 = 9, A = a = 10 ... z = Z = 35

Return Syntax

[I] [pin value]

Return Arguments Description

Item	Type	Description
[I]	Byte	ASCII(I) = 73
[pin value]	Byte	0 or 1 in ASCII ASCII(0) = 48 ASCII(1) = 49

Related MatLab file

readpinbx2.m

K command

Description

Set the proportional gain of the feedback control of the motor 1 (right motor) or of the motor 2 (left motor). The decimal number corresponding to the 16-bit word is divided by 1000.0, so the range of the proportional gain is from 0.000 to 32.767.

Syntax

[K] [Left_K|Right_K] [HighByte] [LowByte] or

[k] [Left_K|Right_K] [HighByte] [LowByte]

Arguments Description

Item	Type	Description
[K] or [k]	Byte	ASCII(K) = 75 ASCII(k) = 107
[Left_K|Right_K]	Byte	Bit 0 : select right motor or left motor 0 = Right motor 1 = Left motor
[HighByte]	Byte	High byte of a 16 bit number (bit 8 to bit 15)
[LowByte]	Byte	Low byte of a 16 bit number (bit 0 to bit 7)

Return Value

If success, return [K].

Related MatLab file

setpgain.m

C command

Description

Set the proportional gain of the feedback control of the motor 3 (transverse motor). The decimal number corresponding to the 16-bit word is divided by 1000.0, so the range of the proportional gain is from 0.000 to 32.767.

Syntax

[C] [HighByte] [LowByte] or

[c] [HighByte] [LowByte]

Arguments Description

Item	Type	Description
[C] or [c]	Byte	ASCII(C) = 67 ASCII(c) = 99
[HighByte]	Byte	High byte of a 16 bit number (bit 8 to bit 15)
[LowByte]	Byte	Low byte of a 16 bit number (bit 0 to bit 7)

Return Value

If success, return [C].

Related MatLab file

setpgain3.m

S command

Description

Stop all motors and return error codes when on closed-loop control mode.

Syntax

[S] or [s]

Arguments Description

Item	Type	Description
[S] or [s]	Byte	ASCII(S) = 83 ASCII(s) = 115

Return Values

If successful stop and errors on the speed control are less than 10%, return [S].

If only the error on the speed control of the motor 1 is greater than 10%, return [A][S].

If only the error on the speed control of the motor 2 is greater than 10%, return [B][S].

If errors on the speed control of the motors 1 and 2 are greater than 10%, return [A][B][S].

Related MatLab file

stopmotors.m

Appendix 3 – Datasheets

The following sections present copies of the datasheets of the components used in the EvBot II and in the USB-DAQ8. The datasheets presented here are mere copies of the first two pages of datasheets found on the world wide web.

A3.1 – MZ104 computer

MZ104

PC/104 Computer with ZFx86 Single Chip PC

Features

- Low power low cost 100% x86 architecture compatible
- Dual watchdog timers, Phoenix BIOS and FailSafe Boot ROM
- Dual RS-232 serial, dual EIDE and floppy support, USB, parallel port
- Compatible with most operating systems including RTOS
- DiskOnChip socket

Specifications

ZFx86, Embedded PC-on-a-Chip
- 32 bit CPU core with 33, 66, 100, and 133*MHz
- Full Desktop AT compatibility
- Phoenix embedded PC BIOS
- SDRAM support, 8MB to 64MB SO-DIMM

Fail-safe Boot ROM
- Total system recovery
- Recover easily from the corruption or loss of CPU boot data

Dual Watchdog Timer
- Programmable tickle sources

PC/104 Bus
- Compliant with standard PC/104 expansion bus with an IRQ and DMA channel subset

Serial Ports
- Two 16550-compatible serial ports, RS232

Parallel Ports
- One bi-directional AT-compatible printer port

USB Port
- One USB root hub interface

* 133MHz is overclocking (additional cooling required)

Drive Interfaces
- Supports up to two EIDE drives (master/slave)
- Floppy Disk Controller

Solid State Flash Memory Device
- Supports M-Systems DiskOnChip Millennium and DiskOnChip 2000 - 8MB to 244MB

Software Compatibility
- Phoenix embedded PC BIOS - 100% x86 compatible, DOS, MSDOS, DRDOS, LINUX, VxWorks, and most other PC compatible RTOS
- Windows™ 9x, and Windows NT™

Electrical Specifications
- Single 5V DC Operation

Mechanical/Environmental
- Size: 3.6" x 3.8" x 0.9"
- Operating temperature: 133MHz @ -20°C to 70°C
- 33MHz, 66MHz, 100C @ -40°C to 85°C (Estimated)

High Efficiency
Up to 95%
Energy Efficiency

Ordering Information

Part Number	Description
MZ104-1MB	PC/104 Computer with 1MB BIOS Flash
MZ104-4MB	PC/104 Computer with 4MB BIOS Flash
Options	
MZ104 KIT	MZ104 Starter Kit
CABLESET1-MZ104	Cables only solution - dual serial, parallel, dual floppy, dual IDE, Utility with Keyboard
CABLESET2-MZ104	Cables (dual floppy, dual IDE, 3 interconnect cables) with Utility board
MEM-8MB-MZ	8MB SDRAM SO-DIMM for MZ104 series
MEM-16MB-MZ	16MB SDRAM SO-DIMM for MZ104 series
MEM-32MB-MZ	32MB SDRAM SO-DIMM for MZ104 series
MEM-64MB-MZ	64MB SDRAM SO-DIMM for MZ104 series

Tri-M Systems and Engineering
1407 Kebet Way, Unit 100 • Port Coquitlam, BC V3C 6L3 • Canada
Tel: 604.945.9565 Fax: 604.945.9566 www.Tri-M.com

A3.2 – DiskOnChip 2000

DiskOnChip® 2000

The Industry-Standard Local Storage Solution

- Single-chip flash disk
- Easy to use interface
- Up to 288 Mbyte capacities (Future capacities: 576 Mbytes and up)
- Pinout & S/W Compatible with 8 Mbyte DiskOnChip Millennium
- 32-pin DIP JEDEC standard
- EPROM/FLASH compatible electrical interface
- High performance - 1.4/0.5 Mbytes/sec sustained Read/Write
- EDC/ECC for maximum data reliability
- Full boot capability
- Built-in TrueFFS® provides full hard disk emulation
- Broad CPU and O/S support
- Optimal Windows CE persistant storage solutions
- 8 Kbyte memory window
- Cost effective solution
- Low power consumption

DiskOnChip Product Family

Overview

M-Systems DiskOnChip® 2000 is a high performance single-chip flash disk in a standard 32-pin DIP package. This unique data storage solution offers cost effective data storage beyond that of traditional hard disks. Perfect for applications with limited space and varying capacity requirements. The DiskOnChip 2000 is simply inserted into a 32-pin DIP socket on your CPU board and you have a bootable flash disk.

Optimal Solution for Internet Appliances, Thin Clients & Embedded Mother Boards

The DiskOnChip 2000 has become the standard modular flash disk for Internet Appliances (such as set-top-boxes) and embedded single board computers.

TrueFFS

The DiskOnChip 2000 includes M-Systems proprietary TrueFFS® (True Flash File System) technology built-in, providing complete read/write capability and hard disk emulation. TrueFFS provides hard disk compatibility at both the sector and file level. The DiskOnChip 2000 works in all major operating systems including DOS, Windows 2000/CE/Embedded NT, pSOS+, VxWorks and QNX. It is also relatively easy to customize to work in O/S-less and non-x86 environments.

Reliability

The use of TrueFFS, in conjunction with the built-in EDC/ECC, provides maximum data reliability, even under harsh operating conditions such as power failures. Advanced wear leveling ensures long flash life for maximum usage.

M-Systems
Flash Disk Pioneers

Tri-M Systems Inc., 6-1301 Ketch Court, Coquitlam, B.C., V3K 6X7, Canada
Phone: (604) 527-1100, (800) 665-5600 Fax: (604) 527-1110
Email: info@tri-m.com Web: www.tri-m.com

DiskOnChip 2000 Specifications

Compatibility
Full hard disk emulation

Host O/S Support[1]
DOS 3.3 and higher, Windows 2000, WinCE, WinNT, Linux, FreeBSD, VxWorks, QNX, pSOS+
(Can be customized for other environments)

Capacity
16, 24, 32, 48, 64, 72, 80, 96, 112, 144, 160, 192, 288 Mbytes

Performance[2]
Sustained Read Speed: 1.4 Mbytes/sec
Sustained Write Speed: 500 Kbytes/sec
Burst Transfer Read Rate: 5 Mbytes/sec
Burst Transfer Write Rate: 5 Mbytes/sec

Package Type
32-pin DIP, 600 mil. width, JEDEC standard

Dimensions in Millimeters
Low profile: 43.75 x 18.10 x 5.80
High profile: 43.75 x 18.10 x 12.80

Current Consumption
Standby 60µA (typical), 100µA (maximum)
Read 25mA (typical), 40mA (maximum)
Write 30mA (typical), 40mA (maximum)

Supply Voltage
3.3V or 5V (single supply)

Operating Temperature
0°C - +70°C (Commercial)
-40°C - +85°C (Extended)

Storage Temperature
-50°C - +100°C (Commercial)

Humidity
10% - 90% relative, non-condensing

EDC/ECC
The enhanced Reed-Solomon EDC/ECC logic provides the following detection and correction capability for each 512-byte block of data:

- Corrects up to two 10-bit symbols, including two random bit errors
- Corrects single bursts up to 11 bits
- Detects single bursts up to 31 bits and double bursts up to 11 bits
- Detects up to 4 random bit errors

Ordering Information

MD220y-Dxxx-xx-t

Package
0 - Low profile (16, 24 Mbytes)
1 - High profile (72 Mbytes)
2 - Low profile (32, 48, 64, 96 Mbytes)
3 - High profile (80, 112, 144, 160, 199, 288 Mbytes)

Capacity
16 - 16 Mbytes
•
•
•
288 - 288 Mbytes

Supply Voltage
V3 - 3.3V
Blank - 5V

Temperature Range
X - Extended -40°C - +85°C
Blank - Commercial 0°C - +70°C

DiskOnChip System Interface

[1] Contact M-Systems for availability
[2] Performance measured in an ISA bus system with no wait states and a Pentium 133 MHz

M-Systems
Flash Disk Pioneers

01-MN-100-00 400

A3.3 – PCM-3115B PCMCIA Module

PC-104 MODULES

PCM-3115B

PCMCIA Module (Two-slot)

Introduction

- PCMCIA socket (with ejector) accepts:
  Type I: FLASH/DRAM/ROM memory
  Type II: Fax/modem/network
  Type III: ATA mass storage
- Complies with PCMCIA v.2.10 and JEIDA v.4.2
- 16-bit data bus
- Features two PCMCIA drives
- Programmable 8KB SMD-type boot FLASH BIOS
- Busy status LED
- Supports bootable function from linear Flash Card, ATA hard disk drives, ATA Flash cards, and SRAM cards
- Power requirement: +5V @ 70mA

A3.4 – PCMCIA Wireless Card

LINKSYS®

Instant Wireless™ Network PC Card

The Freedom to Work Where You Want,
The Flexibility to Work How You Want.

Maximize Your Notebook PC!

INSTANT WIRELESS™ NETWORK PC CARD
(WPC11)

Attention Notebook PC Users: Put the "mobile" back into mobile computing! Whether you're at your desk or in the boardroom, the Linksys Instant Wireless Network PC Card allows you to share printers, files, and more anywhere within your wireless LAN infrastructure; increasing your productivity and keeping you "in touch."

The Instant Wireless Network PC Card gives you the freedom to work your way, from where you want--letting you take full advantage of your notebook PC's portability, while providing you with access to all your network resources. A high-powered built-in Diversity antenna means that you're covered--at a distance of up to 800 feet. And since it occupies only one Type II PCMCIA slot, you're free to use your other slots for additional accessories.

Ready to run in any PCMCIA-equipped notebook PC, and compatible with virtually all major operating systems, the Instant Wireless Network PC Card from Linksys is truly a "must-have" for all notebook PC users.

Benefits

- Wireless Technology Offers Unsurpassed Flexibility--Perfect For Notebook PCs
- Long Operating Range Allows You to Easily Configure Your Workspace
- Compatible With Virtually All PCMCIA-Equipped Notebook Computers
- Runs With Virtually All Major Network Operating Systems
- Free Technical Support
- 1-Year Limited Warranty

Features

- 11 Mbps High-Speed Transfer Rate
- Interoperable with IEEE 802.11b (DSSS) 2.4GHz-compliant Equipment
- Plug-and-Play Operation Provides Easy Set Up
- Long Operating Range (up to 120m indoor)
- Advanced Power Management Features Conserve Valuable Notebook PC Battery Life
- Rugged Metal Design with Integrated Antenna
- Compatible with Virtually All Major Operating Syatems
- Works with All Standard Internet Applications
- Automatic Load Balancing and Scale Back
- Technical Support - 24 Hours a Day, 7 Days a Week
- Full 1-Year Warranty

Specifications

Standards	IEEE 802.11b
Configuration	DHCP
Wired Standard	TCIP/IP, IPX, NDIS4
Ethernet Interface	RF/MAC
Operating Range	100' to 350' from Access Point (indoor)
Data Rate	up to 11Mbps (w/ automatic scale back)
LEDs	Wireless. LAN Activity

Environmental

Dimensions	4.3" x 2.1" x 0.2"
Unit Weight	1.8 oz.
Power	*Input:* 3.3/5V (w/ advanced power management) *Output*: EIRP max +14 dBm
Certifications	CE, FCC Class B, ETS 300 328, ETS 300 826
Operating Temp.	-10ºC to 55ºC (14ºF to 131ºF)
Storage Temp.	-20ºC to 70ºC (-4ºF to 158ºF)
Operating Hum.	10% to 85% Non-Condensing
Storage Hum.	5% to 95% Non-Condensing

Package Contents

Instant Wireless™
Network PC Card

- One Instant Wireless Network PC Card
- One Driver Disk
- User Guide and Registration Card

(Model No.: WPC11)

Sales (800) 546-5797
Support (800) 326-7114
Fax (949) 261-8868
Email sales@linksys.com
Web www.linksys.com

LINKSYS®

A3.5 – BasicX24 Microcontroller

BasicX-24

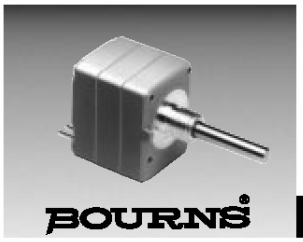
BasicX-24 is the World's most powerful BASIC programmable Microcontroller. It's all-in-one design provides a power-packed module capable of fitting in the smallest of applications. The BX-24s powerful feature set and low cost make it the perfect choice for any application or project.

$49.95 Qty 1 1 Qty Add to Cart

BasicX-24 Quick Specs:

Speed	65,000 instructions per second
EEPROM	32K bytes (User program and data storage)
Max program length	8000+ lines of Basic code
RAM	400 bytes
Available I/O pins	21 (16 standard + 2 serial only + 3 accessed outside standard dip pin area)
Analog Inputs (ADCs)	8 (8 of the 16 standard I/O pins can individually function as 10bit ADCs or standard digital I/Os or a mixture of both)
Serial I/O speed	1200 - 460.8K Baud
Programming interface	High speed Serial
Physical Package	24 pin DIP module

A3.6 – ENS-1J-B28 Rotary Optical Encoder



Features

- Two channel quadrature output
- Bushing or servo mount
- Square wave signal
- Index channel available
- Small size
- Resolution to 256PPR
- CMOS and TTL compatible
- Long life
- High operating speed

EN - Rotary Optical Encoder

Electrical Characteristics

Output	2-bit gray code, Channel A leads Channel B by 90° (electrical) with clockwise rotation
Supply Voltage	5.0 VDC ±0.25 VDC*
Supply Current	26 mA maximum
Output Voltage	
Low Output	0.8V maximum
High Output	4V minimum
Output Current	
Low Output	25mA minimum
Insulation Resistance (500 VDC)	1,000 megohms
Rise/Fall Time	200ns (typical)
Shaft RPM (Ball Bearing)	3,000 rpm maximum
Power Consumption	136 mW maximum
Pulse Width (Electrical Degrees, Each Channel)	180° ±45° TYP.
Pulse Width (Index Channel)	360° ±90°
Phase (Electrical Degrees, Channel A to Channel B)	90° ±45° TYP.
Index Channel Centered on 1-1 State Combination of A and B Channels	0° ±45°

**Consult factory for other voltages up to 15 VDC.*

Environmental Characteristics

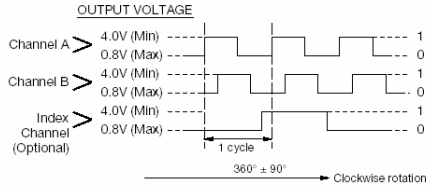
Operating Temperature Range (Standard)	-40°C to +85°C
Vibration	5G
Shock	50G
Humidity	MIL-STD-202, Method 103B, Condition B

Mechanical Characteristics

Torque (Starting and Running)	
A & C Bushings (Spring Loaded for Optimum Feel)	1.5 oz-in. maximum
W, S & T Bushings (Ball Bearing Shaft Support)	0.1 oz-in. maximum
Mechanical Rotation	Continuous
Shaft End Play	0.012" T.I.R. maximum
Shaft Radial Play	0.005" T.I.R. maximum
Rotational Life	
A & C Bushings (300 rpm maximum)**	10,000,000 revolutions
W, S & T Bushings (3,000 rpm maximum)**	200,000,000 revolutions
Weight	0.4 oz.

**For resolutions ≤ 128 quadrature cycles per shaft revolution.

OUTPUT TABLE



STANDARD RESOLUTIONS AVAILABLE

(Full quadrature output cycles per shaft revolution)

25*	125
50*	128
64	200
100	256

For Non-Standard Resolutions—Consult Factory

* Channel B leads Channel A

Specifications are subject to change without notice.

ROTARY OPTICAL

The Bourns® EN model is a self-contained rotary optical encoder. It produces a 2-bit quadrature signal which is suitable for digital systems where both magnitude and direction of adjustment must be provided. The EN encoder is ideal for use as a digital panel control or as a position sensing device in applications where long life, reliability, high resolution and precise linearity are critical.

The EN series encoder converts rotary input into electrical signals which can be used by microprocessors without A/D conversion.

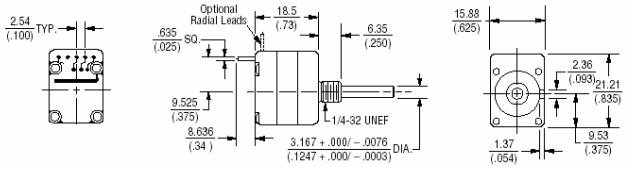
Bourns encoder output signals are square wave digital pulses which do not require debounce circuitry. Both features make it possible to significantly reduce the memory overhead, wiring and wiring interconnects required by other types of control devices.

EN optical encoders offer a useful rotational life of from 10 million to 200 million shaft revolutions, making them ideal for extended service applications. The Bourns encoder is also compact and well suited for situations where the available space is limited.

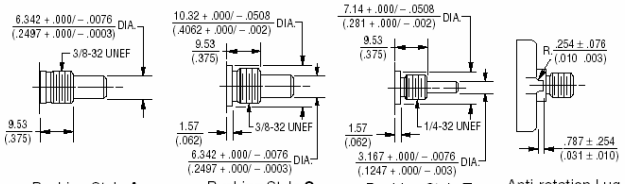
EN - Rotary Optical Encoder

BOURNS®

Dimensional Drawings



Bushing Style **C**



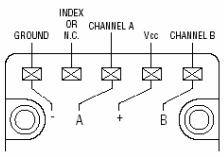
Bushing Style **A**

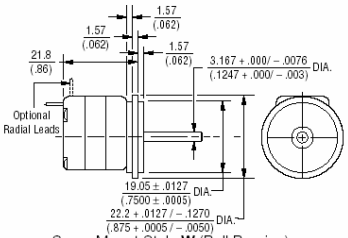
Bushing Style **S** (Ball Bearing)

Bushing Style **T** (Ball Bearing)

Anti-rotation Lug View

TERMINATION DIAGRAM





Servo Mount Style **W** (Ball Bearing)

Consult factory for options not shown, including:

- Wire lead or cable options
- Connectors
- Non-standard resolutions
- Special shaft/bushing sizes and features
- Special performance characteristics
- PCB mounting bracket

How To Order

BOURNS EN SERIES OPTICAL ENCODER

E	N	C	1	J	D	2	8	L	0	0	1	2	8

ANTI-ROTATION LUG POSITION

Code	Description
D	None
J	9:00 Position
P	Rear Mounting Bracket

SHAFT LENGTH*

Code	Description
16	1/2" Long
20	5/8" Long
28	7/8" Long

SWITCHING CONFIGURATION

Code	Description
1	Channel A Leads Channel B By 90 (Clockwise Rotation)**
2	Code 1 Switching With Index Channel

TERMINAL* CONFIGURATION**

Code	Description
L	Axial, Multi-Purpose Pin
R	Radial, Multi-Purpose Pin
M	Rear Ribbon Cable with Connector
N	Side Ribbon Cable with Connector
W	Rear Ribbon Cable - No Connector
Y	Side Ribbon Cable - No Connector

RESOLUTION

Code	Cycles Per Revolution
00025	25
00050	50
00064	64
00100	100
00125	125
00128	128
00200	200
00256	256

SHAFT STYLE

Code	Description	Use With Bushings (Code)
B	1/4" Dia., Plain End	A, S
D	1/8" Dia., Plain End	C, T, W
C	1/4" Dia., Single Flatted	A, S

BUSHING CONFIGURATION

Code	Description
A	3/8"D X 3/8"L Threaded
C	1/4"D X 1/4"L Threaded
S	3/8"D X 3/8"L Threaded (Ball Bearing)
T	1/4"D X 3/8"L Threaded (Ball Bearing)
W	Servo Mount 7/8"D (Ball Bearing)

* Shaft length measured from mounting surface.
** 25 and 50ppr is reversed (Channel B leads Channel A)
*** Standard ribbon cable is 10" long
Consult factory for other lengths.

Specifications are subject to change without notice.

A3.7 – HCTL-2016 Quadrature Decoder

Agilent Technologies
Innovating the HP Way

Quadrature Decoder/Counter Interface ICs

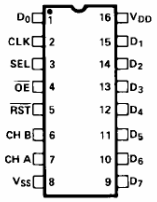
Technical Data

HCTL-2000
HCTL-2016
HCTL-2020

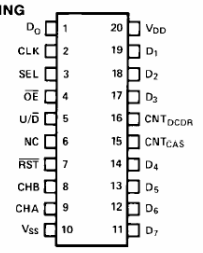
Features

- **Interfaces Encoder to Microprocessor**
- **14 MHz Clock Operation**
- **Full 4X Decode**
- **High Noise Immunity:** Schmitt Trigger Inputs Digital Noise Filter
- **12 or 16-Bit Binary Up/ Down Counter**
- **Latched Outputs**
- **8-Bit Tristate Interface**
- **8, 12, or 16-Bit Operating Modes**
- **Quadrature Decoder Output Signals, Up/Down and Count**
- **Cascade Output Signals, Up/ Down and Count**
- **Substantially Reduced System Software**

DIGITAL MOTION ENCODING



PINOUT A



PINOUT B

Applications

- **Interface Quadrature Incremental Encoders to Microprocessors**
- **Interface Digital Potentiometers to Digital Data Input Buses**

Description

The HCTL-2000, 2016, 2020 are CMOS ICs that perform the quadrature decoder, counter, and bus interface function. The HCTL-20XX family is designed to improve system performance

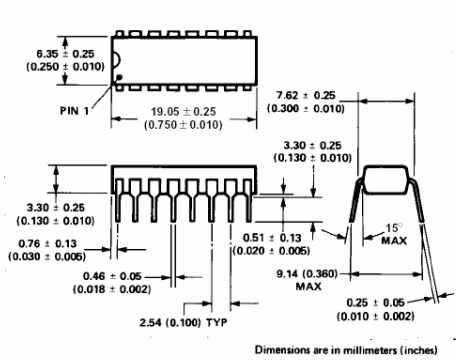
Devices

Part Number	Description	Package Drawing
HCTL-2000	12-bit counter. 14 MHz clock operation.	A
HCTL-2016	All features of the HCTL-2000. 16-bit counter.	A
HCTL-2020	All features of the HCTL-2016. Quadrature decoder output signals. Cascade output signals.	B

ESD WARNING: Standard CMOS handling precautions should be observed with the HCTL-20XX family ICs.

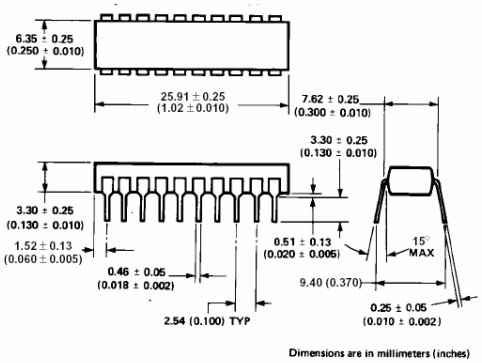
in digital closed loop motion control systems and digital data input systems. It does this by shifting time intensive quadrature decoder functions to a cost effective hardware solution. The entire HCTL-20XX family consists of a 4x quadrature decoder, a binary up/down state counter, and an 8-bit bus interface. The use of Schmitt-triggered CMOS inputs and input noise filters allows reliable operation in noisy environments. The HCTL-2000 contains a 12-bit counter. The HCTL-2016 and 2020 contain a 16-bit counter. The HCTL-2020 also contains quadrature decoder output signals and cascade signals for use with many standard counter ICs. The HCTL-20XX family provides LSTTL compatible tri-state output buffers. Operation is specified for a temperature range from -40 to +85°C at clock frequencies up to 14 MHz.

Package Dimensions



PACKAGE A LEAD FINISH: SOLDER DIPPED

PACKAGE A



PACKAGE B LEAD FINISH: SOLDER DIPPED

PACKAGE B

Operating Characteristics

Table 1. Absolute Maximum Ratings

(All voltages below are referenced to V_{SS})

Parameter	Symbol	Limits	Units
DC Supply Voltage	V_{DD}	-0.3 to +5.5	V
Input Voltage	V_{IN}	-0.3 to V_{DD} +0.3	V
Storage Temperature	T_S	-40 to +125	°C
Operating Temperature	T_A[1]	-40 to +85	°C

Table 2. Recommended Operating Conditions

Parameter	Symbol	Limits	Units
DC Supply Voltage	V_{DD}	+4.5 to +5.5	V
Ambient Temperature	T_A[1]	-40 to +85	°C

A3.8 – HS-300BB Servo Motor

HS-300BB ***Economy Ball Bearing Servo***

Manual | Spec Sheet

Hitec RCD's best selling servo, the HS-300BB has precise heavy-duty resin gears a top ball bearing and SMT circuitry. The HS-300 presents a remarkable value in today's R/C market.

Connector :	Hitec\JR\Airt-Z	Futaba™
Stock #'s	31305S	31305J

Specifications

Motor Type :	3 Pole Ferrite
Bearing Type :	Top Ball Bearing

	English	Metric
Torque 4.8/6.0v :	42 / 51 oz.	3.0 / 3.7 kg.
Speed 4.8/6.0v :	0.19 / 0.15 second	
Size :	1.6"x 0.8"x 1.4"	40 x 20 x 37mm
Weight :	1.7 oz.	48.5 g.

Replacement Parts (SKU#)

Gear Set :	56325
Case Set :	56329
Horn Set :	56315

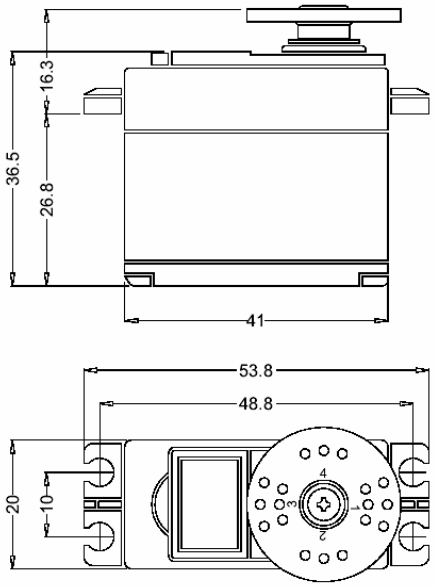
The HS-300,HS-303 and HS300BB share similar cases

Servo Chart | Hitec Home | FAQ's

ANNOUNCED SPECIFICATION OF HS-305BB STANDARD SUPER SPORT BALL BEARING SERVO

1.TECHNICAL VALUES

CONTROL SYSTEM	: +PULSE WIDTH CONTROL 1500usec NEUTRAL	
OPERATING VOLTAGE RANGE	: 4.8V TO 6.0V	
OPERATING TEMPERATURE RANGE	: -20 TO +60°C	
TEST VOLTAGE	: AT 4.8V	AT 6.0V
OPERATING SPEED	: 0.19sec/60° AT NO LOAD	0.15sec/60° AT NO LOAD
STALL TORQUE	: 3kg.cm(41.66oz.in)	3.7kg.cm(51.38oz.in)
OPERATING ANGLE	: 45°/ONE SIDE PULSE TRAVELING 400usec	
DIRECTION	: CLOCK WISE/PULSE TRAVELING 1500 TO 1900usec	
CURRENT DRAIN	: 8mA/IDLE AND 150mA/NO LOAD RUNNING	
DEAD BAND WIDTH	: 8usec	
CONNECTOR WIRE LENGTH	: 300mm(11.81in)	
DIMENSIONS	: 41x20x36.5mm(1.61x0.78x1.43in)	
WEIGHT	: 47.5g(1.67oz)	



2.FEATURES
3-POLE FERRITE MOTOR
DIRECT POTENTIOMETER DRIVE
ONE BALL BEARING

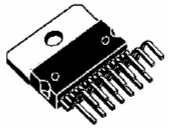
3.APPLICATIONS
SPORT/TRAINER AIRCRAFT
CARS
TRUCKS
BOATS

A3.9 – L298 Dual Full-Bridge Driver

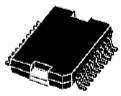
L298

DUAL FULL-BRIDGE DRIVER

- OPERATING SUPPLY VOLTAGE UP TO 46 V
- TOTAL DC CURRENT UP TO 4 A
- LOW SATURATION VOLTAGE
- OVERTEMPERATURE PROTECTION
- LOGICAL "0" INPUT VOLTAGE UP TO 1.5 V (HIGH NOISE IMMUNITY)



Multiwatt15



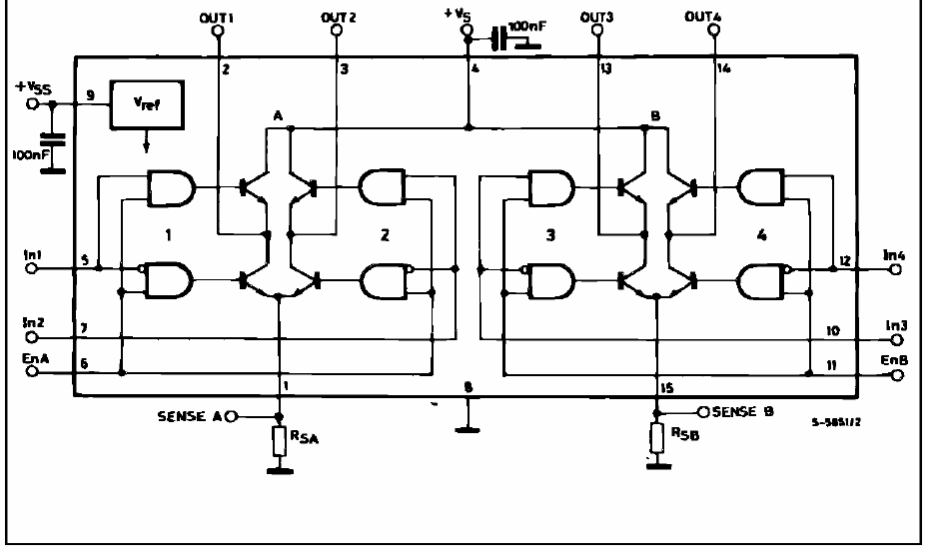
PowerSO20

ORDERING NUMBERS : L298N (Multiwatt Vert.)
L298HN (Multiwatt Horiz.)
L298P (PowerSO20)

DESCRIPTION

The L298 is an integrated monolithic circuit in a 15-lead Multiwatt and PowerSO20 packages. It is a high voltage, high current dual full-bridge driver designed to accept standard TTL logic levels and drive inductive loads such as relays, solenoids, DC and stepping motors. Two enable inputs are provided to enable or disable the device independently of the input signals. The emitters of the lower transistors of each bridge are connected together and the corresponding external terminal can be used for the connection of an external sensing resistor. An additional supply input is provided so that the logic works at a lower voltage.

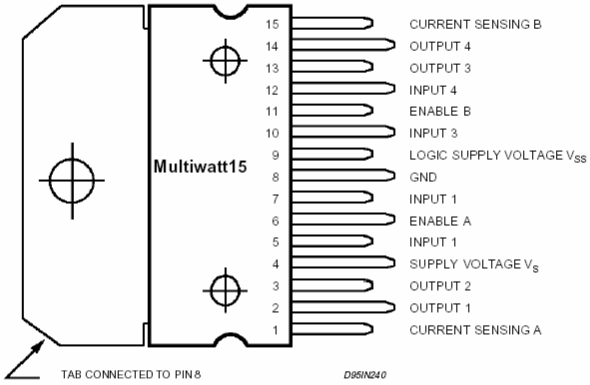
BLOCK DIAGRAM

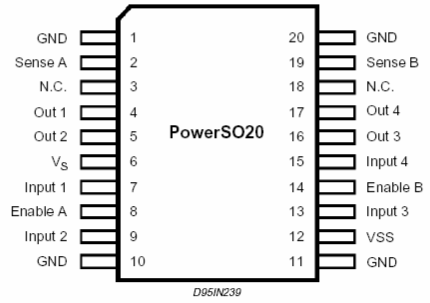


ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Power Supply	50	V
V_{SS}	Logic Supply Voltage	7	V
V_i,V_{en}	Input and Enable Voltage	–0.3 to 7	V
I_O	Peak Output Current (each Channel) – Non Repetitive (t = 100µs) –Repetitive (80% on –20% off; t_{on} = 10ms) –DC Operation	 3 2.5 2	 A A A
V_{sens}	Sensing Voltage	–1 to 2.3	V
P_{tot}	Total Power Dissipation (T_{case} = 75°C)	25	W
T_{op}	Junction Operating Temperature	–25 to 130	°C
T_{stg}, T_j	Storage and Junction Temperature	–40 to 150	°C

PIN CONNECTIONS (top view)





THERMAL DATA

Symbol	Parameter		PowerSO20	Multiwatt15	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max.	–	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	13 (*)	35	°C/W

(*) Mounted on aluminum substrate

A3.10 – UC3610 Dual Schottky Diode Bridge

TEXAS INSTRUMENTS

UC1610
UC3610

SLUS339A – JUNE 1993 – REVISED MAY 2001

DUAL SCHOTTKY DIODE BRIDGE

FEATURES

- **Monolithic Eight-Diode Array**
- **Exceptional Efficiency**
- **Low Forward Voltage**
- **Fast Recovery Time**
- **High Peak Current**
- **Small Size**

DESCRIPTION

This eight-diode array is designed for high-current, low duty-cycle applications typical of flyback voltage clamping for inductive loads. The dual bridge connection makes this device particularly applicable to bipolar driven stepper motors.

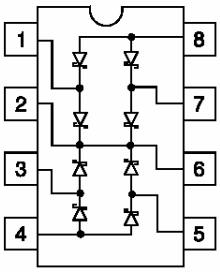
The use of Schottky diode technology features high efficiency through lowered forward voltage drop and decreased reverse recovery time.

This single monolithic chip is fabricated in both hermetic CERDIP and copper-leaded plastic packages. The UC1610 in ceramic is designed for –55°C to 125°C environments but with reduced peak current capability. The UC2610 in plastic and ceramic is designed for –25°C to 125°C environments also with reduced peak current capability; while the UC3610 in plastic has higher current rating over a 0°C to 70°C temperature range.

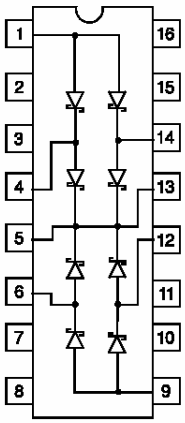
AVAILABLE OPTIONS

$T_A = T_J$	Packaged Devices		
	SOIC Wide (DW)	DIL (J)	DIL (N)
–55°C to 125°C	UC1610DW	UC1610J	UC1610N
–25°C to 125°C	UC2610DW	UC2610J	UC2610N
0°C to 70°C	UC3610DW	UC3610J	UC3610N

N OR J PACKAGE
TOP VIEW



DW PACKAGE
TOP VIEW



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Peak inverse voltage (per diode) . . . . . 50 V
Peak forward current
UC1611 . . . . . 1 A
UC2610 . . . . . 1 A
UC3611 . . . . . 3 A
Power dissipation at T_A = 70°C . . . . . 1 W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature (soldering, 10 seconds) . . . . . 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ Consult packaging section of databook for thermal limitations and considerations of package.

electrical characteristics, all specifications apply to each individual diode, T_J = 25°C, $T_A = T_J$, (except as noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward voltage drop	I_F = 100 mA	0.35	0.5	0.7	V
	I_F = 1 A	0.8	1.0	1.3	V
Leakage current	V_R = 40 V		0.01	0.1	mA
	V_R = 40 V, T_J = 100°C		0.1	1.0	mA
Reverse recovery	0.5 A forward to 0.5 A reverse		15		ns
Forward recovery	1 A forward to 1.1 V recovery		30		ns
Junction capacitance	V_R = 5 V		70		pF

NOTE: At forward currents of greater than 1.0 A, a parasitic current of approximately 10 mA may be collected by adjacent diodes.

A3.11 – 74HC165 Parallel-in / Serial-out Shift Register

FAIRCHILD SEMICONDUCTOR™

September 1983
Revised February 1999

MM74HC165
Parallel-in/Serial-out 8-Bit Shift Register

General Description

The MM74HC165 high speed PARALLEL-IN/SERIAL-OUT SHIFT REGISTER utilizes advanced silicon-gate CMOS technology. It has the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

This 8-bit serial shift register shifts data from Q_A to Q_H when clocked. Parallel inputs to each stage are enabled by a low level at the SHIFT/LOAD input. Also included is a gated CLOCK input and a complementary output from the eighth bit.

Clocking is accomplished through a 2-input NOR gate permitting one input to be used as a CLOCK INHIBIT function. Holding either of the CLOCK inputs high inhibits clocking, and holding either CLOCK input low with the SHIFT/LOAD input high enables the other CLOCK input. Data transfer occurs on the positive going edge of the clock. Parallel loading is inhibited as long as the SHIFT/LOAD input is HIGH. When taken LOW, data at the parallel inputs is loaded directly into the register independent of the state of the clock.

The 74HC logic family is functionally as well as pin-out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns (clock to Q)
- Wide operating supply voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent supply current: 80 μA maximum (74HC Series)
- Fanout of 10 LS-TTL loads

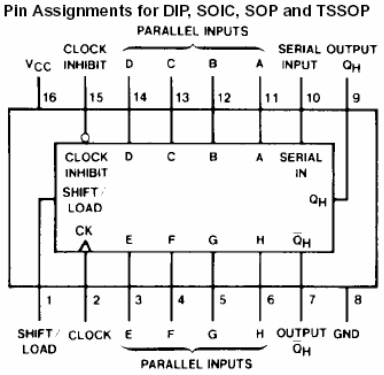
Ordering Code:

Order Number	Package Number	Package Description
MM74HC165M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC165SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC165MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC165	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP



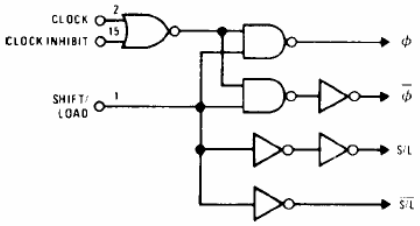
Top View

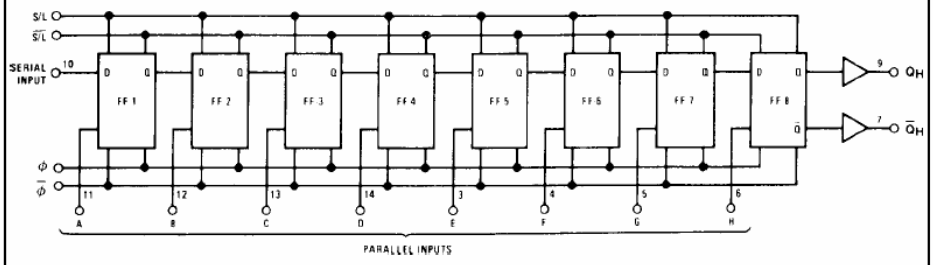
Function Table

Inputs					Internal Outputs		Output
Shift/ Load	Clock Inhibit	Clock	Serial	Parallel A. . .H	Q_A	Q_B	Q_H
L	X	X	X	a. . .h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{AN}	Q_{GN}
H	L	↑	L	X	L	Q_{AN}	Q_{GN}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = HIGH Level (steady state), L = LOW Level (steady state)
X = Irrelevant (any input, including transitions)
↑ = Transition from LOW-to-HIGH level
Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{AN}, Q_{GN} = The level of Q_A or Q_G before the most recent ↑ transition of the clock; indicates a one-bit shift.

Logic Diagrams





A3.12 – MIC29501 Voltage Regulator

The Infinite Bandwidth Company™

MIC29150/29300/29500/29750 Series

High-Current Low-Dropout Regulators

Final Information

General Description

The MIC29150/29300/29500/29750 are high current, high accuracy, low-dropout voltage regulators. Using Micrel's proprietary Super ßeta PNP™ process with a PNP pass element, these regulators feature 300mV to 370mV (full load) dropout voltages and very low ground current. Designed for high current loads, these devices also find applications in lower current, extremely low dropout-critical systems, where their tiny dropout voltage and ground current values are important attributes.

The MIC29150/29300/29500/29750 are fully protected against overcurrent faults, reversed input polarity, reversed lead insertion, overtemperature operation, and positive and negative transient voltage spikes. Five pin fixed voltage versions feature logic level ON/OFF control and an error flag which signals whenever the output falls out of regulation. Flagged states include low input voltage (dropout), output current limit, overtemperature shutdown, and extremely high voltage spikes on the input.

On the MIC29xx1 and MIC29xx2, the ENABLE pin may be tied to V_{IN} if it is not required for ON/OFF control. The MIC29150/29300/29500 are available in 3- and 5-pin TO-220 and surface mount TO-263 packages. The MIC29750 7.5A regulators are available in 3- and 5-pin TO-247 packages.

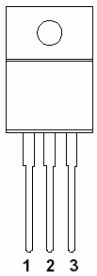
Features

- High Current Capability
  - MIC29150/29151/29152/29153 ..... 1.5A
  - MIC29300/29301/29302/29303 ..... 3A
  - MIC29500/29501/29502/29503 ..... 5A
  - MIC29750/29751/29752 ..... 7.5A
- Low-Dropout Voltage ..... 350mV at Full Load
- Low Ground Current
- Accurate 1% Guaranteed Tolerance
- Extremely Fast Transient Response
- Reverse-battery and "Load Dump" Protection
- Zero-Current Shutdown Mode (5-Pin versions)
- Error Flag Signals Output Out-of-Regulation (5-Pin versions)
- Also Characterized For Smaller Loads With Industry-Leading Performance Specifications
- Fixed Voltage and Adjustable Versions

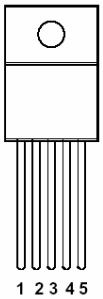
Applications

- Battery Powered Equipment
- High-Efficiency "Green" Computer Systems
- Automotive Electronics
- High-Efficiency Linear Power Supplies
- High-Efficiency Post-Regulator For Switching Supply

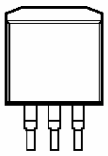
Pin Configuration



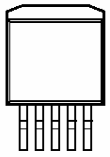
MIC29150/29300/ 29500BT and MIC29750BWT



MIC29151/29152/29153BT MIC29301/29302/29303BT MIC29501/29502/29503BT MIC29751/29752BWT



MIC29150/29300BU



MIC29151/29152/29153BU MIC29301/29302/29303BU MIC29501/29502/29503BU

Pinout **On all devices, the Tab is grounded.**

MIC29150/29300/29500/29750 Three Terminal Devices:
Pin 1 = Input, 2 = Ground, 3 = Output

MIC29151/29301/29501/29751 Five Terminal Fixed Voltage Devices:
Pin 1 = Enable, 2 = Input, 3 = Ground, 4 = Output, 5 = Flag

MIC29152/29302/29502/29752 Adjustable with ON/OFF Control
Pin 1 = Enable, 2 = Input, 3 = Ground, 4 = Output, 5 = Adjust

MIC29153/29303/29503 Adjustable with Flag
Pin 1 = Flag, 2 = Input, 3 = Ground, 4 = Output, 5 = Adjust

Micrel, Inc. • 1849 Fortune Drive • San Jose, CA 95131 • USA • tel + 1 (408) 944-0800 • fax + 1 (408) 944-0970 • http://www.micrel.com

Ordering Information

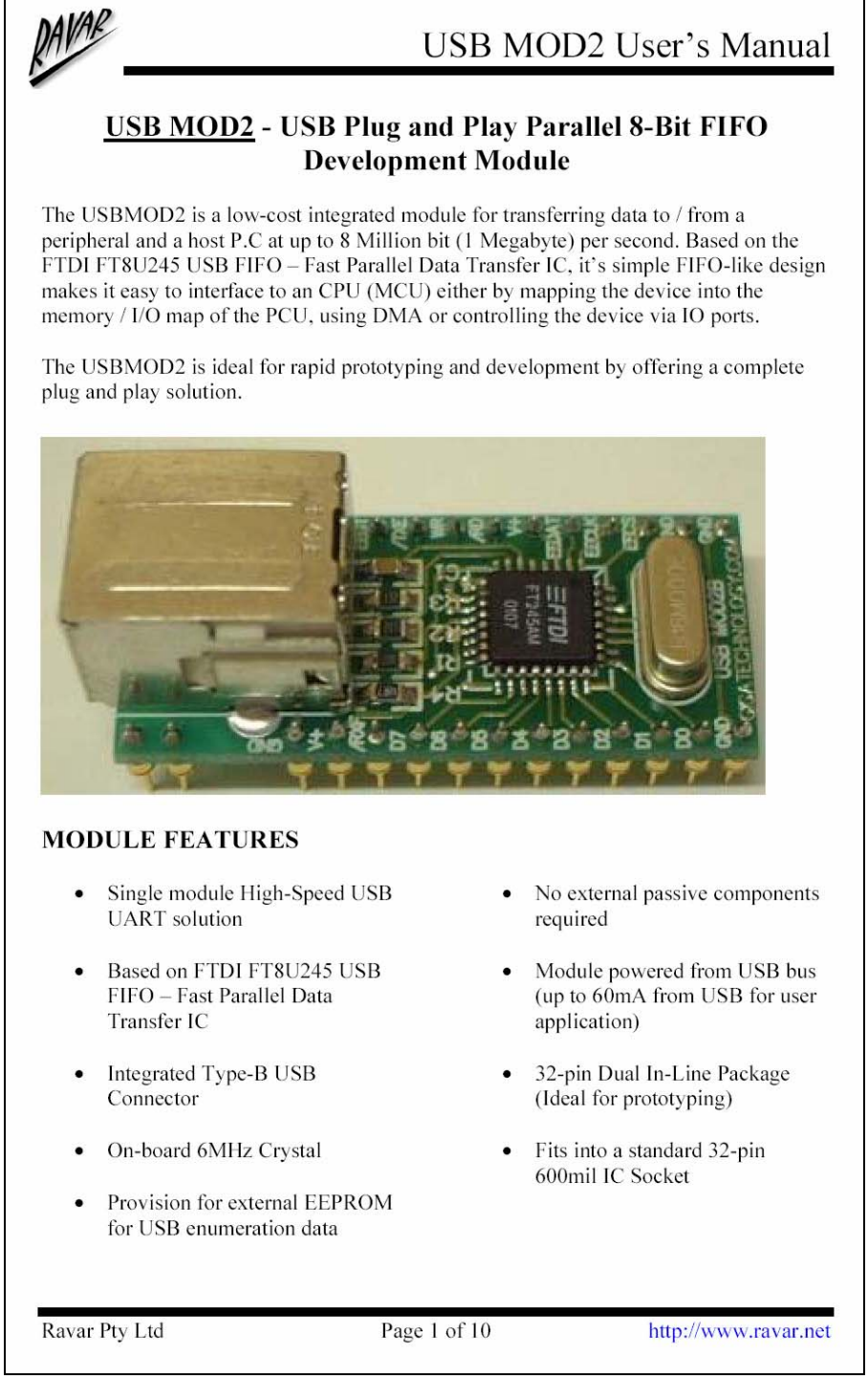
Part Number	Temp. Range*	Volts	Current	Package
MIC29150-3.3BT	–40 to +125°C	3.3	1.5A	TO-220
MIC29150-4.2BT	–40 to +125°C	4.2	1.5A	TO-220
MIC29150-5.0BT	–40 to +125°C	5.0	1.5A	TO-220
MIC29150-12BT	–40 to +125°C	12	1.5A	TO-220
MIC29150-3.3BU	–40 to +125°C	3.3	1.5A	TO-263
MIC29150-5.0BU	–40 to +125°C	5.0	1.5A	TO-263
MIC29150-12BU	–40 to +125°C	12	1.5A	TO-263
MIC29151-3.3BT	–40 to +125°C	3.3	1.5A	TO-220-5
MIC29151-5.0BT	–40 to +125°C	5.0	1.5A	TO-220-5
MIC29151-12BT	–40 to +125°C	12	1.5A	TO-220-5
MIC29151-3.3BU	–40 to +125°C	3.3	1.5A	TO-263-5
MIC29151-5.0BU	–40 to +125°C	5.0	1.5A	TO-263-5
MIC29151-12BU	–40 to +125°C	12	1.5A	TO-263-5
MIC29152BT	–40 to +125°C	Adj	1.5A	TO-220-5
MIC29152BU	–40 to +125°C	Adj	1.5A	TO-263-5
MIC29153BT	–40 to +125°C	Adj	1.5A	TO-220-5
MIC29153BU	–40 to +125°C	Adj	1.5A	TO-263-5
MIC29300-3.3BT	–40 to +125°C	3.3	3.0A	TO-220
MIC29300-5.0BT	–40 to +125°C	5.0	3.0A	TO-220
MIC29300-12BT	–40 to +125°C	12	3.0A	TO-220
MIC29300-3.3BU	–40 to +125°C	3.3	3.0A	TO-263
MIC29300-5.0BU	–40 to +125°C	5.0	3.0A	TO-263
MIC29300-12BU	–40 to +125°C	12	3.0A	TO-263
MIC29301-3.3BT	–40 to +125°C	3.3	3.0A	TO-220-5
MIC29301-5.0BT	–40 to +125°C	5.0	3.0A	TO-220-5
MIC29301-12BT	–40 to +125°C	12	3.0A	TO-220-5
MIC29301-3.3BU	–40 to +125°C	3.3	3.0A	TO-263-5
MIC29301-5.0BU	–40 to +125°C	5.0	3.0A	TO-263-5
MIC29301-12BU	–40 to +125°C	12	3.0A	TO-263-5
MIC29302BT	–40 to +125°C	Adj	3.0A	TO-220-5
MIC29302BU	–40 to +125°C	Adj	3.0A	TO-263-5
MIC29303BT	–40 to +125°C	Adj	3.0A	TO-220-5
MIC29303BU	–40 to +125°C	Adj	3.0A	TO-263-5

* Junction Temperature

Part Number	Temp. Range*	Volts	Current	Package
MIC29500-3.3BT	–40 to +125°C	3.3	5.0A	TO-220
MIC29500-5.0BT	–40 to +125°C	5.0	5.0A	TO-220
MIC29501-3.3BT	–40 to +125°C	3.3	5.0A	TO-220-5
MIC29501-5.0BT	–40 to +125°C	5.0	5.0A	TO-220-5
MIC29501-3.3BU	–40 to +125°C	3.3	5.0A	TO-263-5
MIC29501-5.0BU	–40 to +125°C	5.0	5.0A	TO-263-5
MIC29502BT	–40 to +125°C	Adj	5.0A	TO-220-5
MIC29502BU	–40 to +125°C	Adj	5.0A	TO-263-5
MIC29503BT	–40 to +125°C	Adj	5.0A	TO-220-5
MIC29503BU	–40 to +125°C	Adj	5.0A	TO-263-5
MIC29750-3.3BWT	–40 to +125°C	3.3	7.5A	TO-247-3
MIC29750-5.0BWT	–40 to +125°C	5.0	7.5A	TO-247-3
MIC29751-3.3BWT	–40 to +125°C	3.3	7.5A	TO-247-5
MIC29751-5.0BWT	–40 to +125°C	5.0	7.5A	TO-247-5
MIC29752BWT	–40 to +125°C	Adj	7.5A	TO-247-5

MIC29xx0 versions are 3-terminal fixed voltage devices. MIC29xx1 are fixed voltage devices with ENABLE and ERROR flag. MIC29xx2 are adjustable regulators with ENABLE control. MIC29xx3 are adjustables with an ERROR flag.

A3.13 – USB MOD2



USB MOD2 User's Manual

USB MOD2 - USB Plug and Play Parallel 8-Bit FIFO Development Module

The USBMOD2 is a low-cost integrated module for transferring data to / from a peripheral and a host P.C at up to 8 Million bit (1 Megabyte) per second. Based on the FTDI FT8U245 USB FIFO – Fast Parallel Data Transfer IC, it's simple FIFO-like design makes it easy to interface to an CPU (MCU) either by mapping the device into the memory / I/O map of the PCU, using DMA or controlling the device via IO ports.

The USBMOD2 is ideal for rapid prototyping and development by offering a complete plug and play solution.

MODULE FEATURES

- Single module High-Speed USB UART solution
- Based on FTDI FT8U245 USB FIFO – Fast Parallel Data Transfer IC
- Integrated Type-B USB Connector
- On-board 6MHz Crystal
- Provision for external EEPROM for USB enumeration data
- No external passive components required
- Module powered from USB bus (up to 60mA from USB for user application)
- 32-pin Dual In-Line Package (Ideal for prototyping)
- Fits into a standard 32-pin 600mil IC Socket

FT8U245 IC FEATURES

- Single Chip Multi-Function Data Transfer Solution
- Send / Receive Data over USB at up to 1 Mb / Sec
- 384 byte receive buffer / 128 byte transmit buffer for high data throughput
- Simple interface to CPU or MCU bus
- No in-depth knowledge of USB required as all USB Protocol is handled automatically within the I.C
- FTDI's Virtual COM port drivers eliminate the need for USB driver development in most cases.
- Compact 32 pin (7mm x 7mm) MQFP package
- Integrated 6Mhz – 48Mhz Clock Multiplier aids FCC and CE compliance
- Integrated 3.3v Regulator – No External Regulator Required
- UHCI / OHCI Compliant
- USB 1.1 Specification Compliant
- USB VID, PID, Serial Number and Product Description Strings in external E2PROM.

VIRTUAL COM PORT (VCP)
DRIVERS for

- Windows 98 and Windows 98 SE
- Windows 2000 / ME / XP
- Windows CE **
- MAC OS-8 and OS9
- MAC OS-X
- Linux 2.40 and greater

[** = In the planning or under development]

D2XX
(USB Direct Drivers + DLL S/W Interface)

- Windows 98 and Windows 98 SE
- Windows 2000 / ME / XP

For further information regarding the FTDI FT8U245AM USB FIFO – Fast Parallel Data Transfer IC please refer to the FT8U245AM Datasheet. This datasheet can be found on the Ravar website at **http://www.ravar.net**

A3.14 – ADC8161 Analog to Digital Converter

National Semiconductor

June 1999

ADC08161
500 ns A/D Converter with S/H Function and 2.5V Bandgap Reference

General Description

Using a patented multi-step A/D conversion technique, the 8-bit ADC08161 CMOS A/D converter offers 500 ns conversion time, internal sample-and-hold (S/H), a 2.5V bandgap reference, and dissipates only 100 mW of power. The ADC08161 performs an 8-bit conversion with a 2-bit voltage estimator that generates the 2 MSBs and two low-resolution (3-bit) flashes that generate the 6 LBSs.

Input signals are tracked and held by the input sampling circuitry, eliminating the need for an external sample-and-hold. The ADC08161 can perform accurate conversions of full-scale input signals at frequencies from DC to typically more than 300 kHz (full power bandwidth) without the need of an external sample-and-hold (S/H).

For ease of interface to microprocessors, this part has been designed to appear as a memory location or I/O port without the need for external interfacing logic.

Key Specifications

- Resolution — 8 Bits
- Conversion time (t_{CONV}) — 560 ns max ($\overline{WR}$-$\overline{RD}$ Mode)
- Full power bandwidth — 300 kHz (typ)
- Throughput rate — 1.5 MHz min
- Power dissipation — 100 mW max
- Total unadjusted error — ±½ LSB and ±1 LSB max

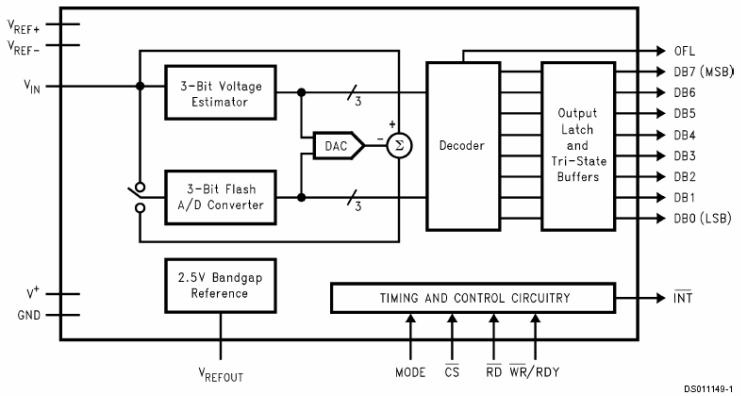
Features

- No external clock required
- Analog input voltage range from GND to V^+
- 2.5V bandgap reference

Applications

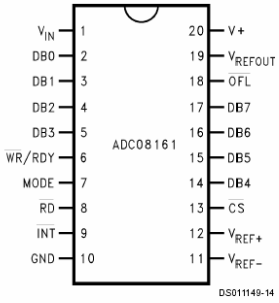
- Mobile telecommunications
- Hard-disk drives
- Instrumentation
- High-speed data acquisition systems

Block Diagram



Connection Diagram

Wide-Body Small-Outline Package



See NS Package Number M20B

Ordering Information

Industrial ($-40^{\circ}C \le T_A \le 85^{\circ}C$)	Package
ADC08161CIWM	M20B

Pin Description

V_{IN} — This is the analog input. The input range is GND–50 mV ≤ V_{INPUT} ≤ V^+ + 50 mV.

DB0–DB7 — TRI-STATE data outputs—bit 0 (LSB) through bit 7 (MSB).

$\overline{WR}$ /RDY — **$\overline{WR}$-$\overline{RD}$ Mode** (Logic high applied to MODE pin)

$\overline{WR}$: With $\overline{CS}$ low, the conversion is started on the rising edge of $\overline{WR}$. The digital result will be strobed into the output latch at the end of conversion (*Figures 2, 3, 4*).

$\overline{RD}$ Mode (Logic low applied to MODE pin)

RDY: This is an open drain output (no internal pull-up device). $\overline{RDY}$ will go low after the falling edge of $\overline{CS}$ and returns high at the end of conversion.

MODE — **Mode:** Mode (**$\overline{RD}$ or $\overline{WR}$-$\overline{RD}$**) selection input– This pin is pulled to a logic low through an internal 50 µA current sink when left unconnected.

$\overline{RD}$ Mode is selected if the MODE pin is left unconnected or externally forced low. A complete conversion is accomplished by pulling $\overline{RD}$ low until output data appears.

$\overline{WR}$-$\overline{RD}$ Mode is selected when a high is applied to the MODE pin. A conversion starts with the $\overline{WR}$ signal's rising edge and then using $\overline{RD}$ to access the data.

$\overline{RD}$ — **$\overline{WR}$-$\overline{RD}$ Mode** (logic high on the MODE pin)

This is the active low Read input. With a logic low applied to the $\overline{CS}$ pin, the TRI-STATE data outputs (DB0–DB7) will be activated when $\overline{RD}$ goes low (*Figures 2, 3, 4*).

$\overline{RD}$ Mode (logic low on the MODE pin)

With $\overline{CS}$ low, a conversion starts on the falling edge of $\overline{RD}$. Output data appears on DB0–DB7 at the end of conversion (*Figures 1, 5*).

$\overline{INT}$ — This is an active low output that indicates that a conversion is complete and the data is in the output latch. $\overline{INT}$ is reset by the rising edge of $\overline{RD}$.

GND — This is the power supply ground pin. The ground pin should be connected to a "clean" ground reference point.

V_{REF-}, V_{REF+} — These are the reference voltage inputs. They may be placed at any voltage between GND − 50 mV and V^+ + 50 mV, but V_{REF+} must be greater than V_{REF-}. Ideally, an input voltage equal to V_{REF-} produces an output code of 0, and an input voltage greater than V_{REF+} − 1.5 LSB produces an output code of 255.

For the ADC08161 an input voltage that exceeds V^+ by more than 100 mV or is below GND by more than 100 mV will create conversion errors.

$\overline{CS}$ — This is the active low Chip Select input. A logic low signal applied to this input pin enables the $\overline{RD}$ and $\overline{WR}$ inputs. Internally, the $\overline{CS}$ signal is ORed with $\overline{RD}$ and $\overline{WR}$ signals.

$\overline{OFL}$ — Overflow Output. If the analog input is higher than V_{REF+}, $\overline{OFL}$ will be low at the end of conversion. It can be used when cascading two ADC08161s to achieve higher resolution (9 bits). This output is always active and does not go into TRI-STATE as DB0–DB7 do. When $\overline{OFL}$ is set, all data outputs remain high when the ADC08061's output data is read.

V^+ — Positive power supply voltage input. Nominal operating supply voltage is +5V. The supply pin should be bypassed with a 10 µF bead tantalum in parallel with a 0.1 ceramic capacitor. Lead length should be as short as possible.

V_{REFOUT} — The internal bandgap reference's 2.5V output is available on this pin. Use a 220 µF bypass capacitor between this pin and analog ground.

A3.15 – LMX324 Quad Operational Amplifiers

19-2103; Rev 0; 8/01

MAXIM

Single/Dual/Quad, General-Purpose, Low-Voltage, Rail-to-Rail Output Op Amps

General Description

The LMX321/LMX358/LMX324 are single/dual/quad, low-cost, low-voltage, pin-to-pin compatible upgrades to the LMV321/LMV358/LMV324 family of general purpose op amps. These devices offer Rail-to-Rail® outputs and an input common-mode range that extends below ground. These op amps draw only 105µA of quiescent current per amplifier, operate from a single +2.3V to +7V supply, and drive 2kΩ resistive loads to within 40mV of either rail. The LMX321/LMX358/LMX324 are unity-gain stable with a 1.3MHz gain-bandwidth product capable of driving capacitive loads up to 400pF. The combination of low voltage, low cost, and small package size makes these amplifiers ideal for portable/battery-powered equipment.

The LMX321 single op amp is available in ultra-small 5-pin SC70 and space-saving 5-pin SOT23 packages. The LMX358 dual op amp is available in the tiny 8-pin SOT23 package. The LMX324 quad op amp is available in 14-pin TSSOP and SO packages.

Applications

Cellular Phones

Laptops

Low-Power, Low-Voltage Applications

Portable/Battery-Powered Equipment

Cordless Phones

Active Filters

Features

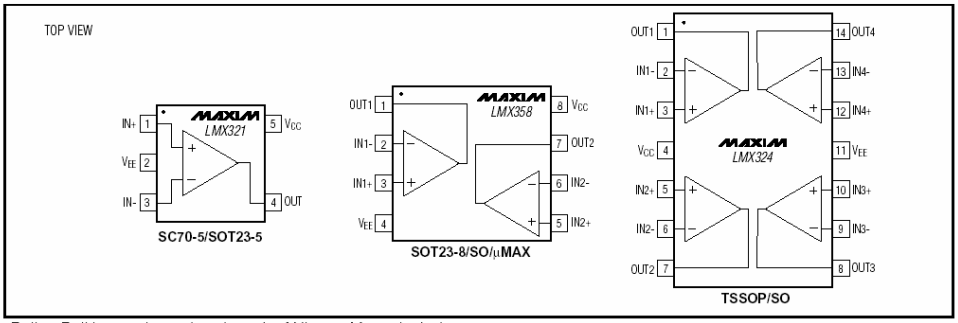
- **Upgrade to LMV321/LMV358/LMV324 Family**
- **Single +2.3V to +7V Supply Voltage Range**
- **Available in Space-Saving Packages**
  5-Pin SC70 (LMX321)
  8-Pin SOT23 (LMX358)
  14-Pin TSSOP (LMX324)
- **1.3MHz Gain-Bandwidth Product**
- **105µA Quiescent Current per Amplifier (V_{CC} = +2.7V)**
- **No Phase Reversal for Overdriven Inputs**
- **No Crossover Distortion**
- **Rail-to-Rail Output Swing**
- **Input Common-Mode Voltage Range: V_{EE} - 0.2V to V_{CC} - 0.8V**
- **Drives 2kΩ Resistive Loads**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
LMX321AXK-T	-40°C to +125°C	5 SC70-5
LMX321AUK-T	-40°C to +125°C	5 SOT23-5
LMX358AKA-T	-40°C to +125°C	8 SOT23-8
LMX358ASA	-40°C to +125°C	8 SO
LMX358AUA	-40°C to +125°C	8 µMAX
LMX324ASD	-40°C to +125°C	14 SO
LMX324AUD	-40°C to +125°C	14 TSSOP

Selector Guide appears at end of data sheet.

Pin Configurations



Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.

Single/Dual/Quad, General-Purpose, Low-Voltage, Rail-to-Rail Output Op Amps

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to V_{EE}) ..... -0.3V to +8V
Differential Input Voltage (V_{IN+} - V_{IN-}) ..... V_{EE} to V_{CC}
OUT_ to V_{EE} ..... -0.3V to (V_{CC} + 0.3V)
Output Short-Circuit Duration
  OUT_ Shorted to V_{CC} or V_{EE} ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
  5-Pin SC70-5 (derate 3.1mW/°C above +70°C) 247mW
  5-Pin SOT23-5 (derate 7.1mW/°C above +70°C) 571mW
  8-Pin SOT23-8 (derate 7.52mW/°C above +70°C) 602mW
  8-Pin SO (derate 5.9mW/°C above +70°C) 471mW
  8-Pin µMAX (derate 4.5mW/°C above +70°C) 362mW
  14-Pin TSSOP (derate 9.1mW/°C above +70°C) 727mW
  14-Pin SO (derate 8.3mW/°C above +70°C) 667mW
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V, V_{EE} = 0, V_{OUT} = V_{CC}/2, V_{CM} = 1V, R_L > 1MΩ, **T_A = +25°C**, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC Characteristics							
Input Offset Voltage	V_{OS}				1	6	mV
Input Offset Voltage Average Drift	TCV_{OS}				6		µV/°C
Input Bias Current	I_B				18	50	nA
Input Offset Current	I_{OS}				1	8	nA
Common-Mode Rejection Ratio	CMRR	-0.2V < V_{CM} < 1.8V		72	92		dB
Power-Supply Rejection Ratio	PSRR	2.3V ≤ V_{CC} ≤ 7V, V_{OUT} = 1V		82	96		dB
Input Common-Mode Voltage Range	V_{CM}	For CMRR ≥ 72dB	Limit	-0.2		1.8	V
			Typ	-0.2		1.9	
Large-Signal Voltage Gain	A_{VOL}	R_L = 2kΩ to V_{EE}, 0.3V < V_{OUT} < 2.4V		20	120		V/mV
Output Voltage Swing	V_{OUT}	R_L = 10kΩ to 1.35V	V_{CC} - V_{OH}		12	50	mV
			V_{OL}		10	40	
		R_L = 2kΩ to 1.35V	V_{CC} - V_{OH}		40	110	
			V_{OL}		25	60	
Supply Current	I_{CC}	LMX321 (Single)			105	150	µA
		LMX358 (Dual)			210	300	
		LMX324 (Quad)			420	600	
AC Characteristics							
Slew Rate	SR	1V step Input			1		V/µs
Gain-Bandwidth Product	GBW	C_L = 200pF			1.3		MHz
Phase Margin	ϕ_M				64		degrees
Gain Margin	GM				24		dB
Input Noise Voltage Density	e_n	f = 1kHz			66		nV/√Hz
Input Current Noise Density	i_n	f = 1kHz			0.13		pA/√Hz

A3.16 – LTC 1563-3 Active Lowpass Filter

LINEAR TECHNOLOGY

LTC1563-2/LTC1563-3

Active RC, 4th Order Lowpass Filter Family

FEATURES

- **Extremely Easy to Use—A Single Resistor Value Sets the Cutoff Frequency (256Hz < f_C < 256kHz)**
- **Extremely Flexible—Different Resistor Values Allow Arbitrary Transfer Functions with or without Gain (256Hz < f_C < 256kHz)**
- Supports Cutoff Frequencies Up to 360kHz Using FilterCAD™
- LTC1563-2: Unity-Gain Butterworth Response Uses a Single Resistor Value, Different Resistor Values Allow Other Responses with or without Gain
- LTC1563-3: Unity-Gain Bessel Response Uses a Single Resistor Value, Different Resistor Values Allow Other Responses with or without Gain
- Rail-to-Rail Input and Output Voltages
- Operates from a Single 3V (2.7V Min) to ±5V Supply
- Low Noise: 36µV_{RMS} for f_C = 25.6kHz, 60µV_{RMS} for f_C = 256kHz
- f_C Accuracy < ±2% (Typ)
- DC Offset < 1mV
- Cascadable to Form 8th Order Lowpass Filters

APPLICATIONS

- **Replaces Discrete RC Active Filters and Modules**
- Antialiasing Filters
- Smoothing or Reconstruction Filters
- Linear Phase Filtering for Data Communication
- Phase Locked Loops

DESCRIPTION

The LTC®1563-2/LTC1563-3 are a family of extremely easy-to-use, active RC lowpass filters with rail-to-rail inputs and outputs and low DC offset suitable for systems with a resolution of up to 16 bits. The LTC1563-2, with a single resistor value, gives a unity-gain Butterworth response. The LTC1563-3, with a single resistor value, gives a unity-gain Bessel response. The proprietary architecture of these parts allows for a simple resistor calculation:

R = 10k (256kHz/f_C); f_C = Cutoff Frequency

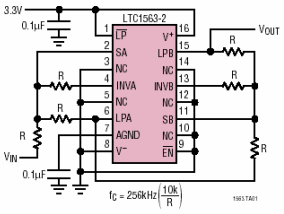
where f_C is the desired cutoff frequency. For many applications, this formula is all that is needed to design a filter. By simply utilizing different valued resistors, gain and other responses are achieved.

The LTC1563-X features a low power mode, for the lower frequency applications, where the supply current is reduced by an order of magnitude and a near zero power shutdown mode.

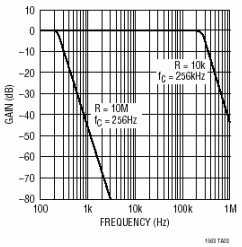
The LTC1563-Xs are available in the narrow SSOP-16 package (SO-8 footprint).

TYPICAL APPLICATION

Single 3.3V, 256Hz to 256kHz Butterworth Lowpass Filter



Frequency Response

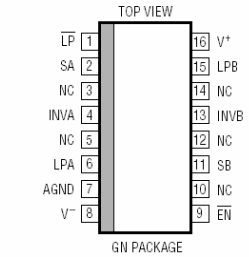


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to V^-) 11V
Maximum Input Voltage at
Any Pin ..... $(V^- - 0.3V) \leq V_{PIN} \leq (V^+ + 0.3V)$
Power Dissipation 500mW
Operating Temperature Range
LTC1563C ..... 0°C to 70°C
LTC1563I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
16-LEAD PLASTIC SSOP

T_{JMAX} = 150°C, θ_{JA} = 135°C/W

NOTE: PINS LABELED NC ARE NOT CONNECTED INTERNALLY AND SHOULD BE CONNECTED TO THE SYSTEM GROUND

ORDER PART NUMBER
LTC1563-2CGN LTC1563-3CGN LTC1563-2IGN LTC1563-3IGN
GN PART MARKING
15632 15633 15632I 15633I

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_S = Single 4.75V, $\overline{EN}$ pin to logic "low," Gain = 1, R_{FIL} = R11 = R21 = R31 = R12 = R22 = R32, specifications apply to both the high speed (HS) and low power (LP) modes unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Specifications for Both LTC1563-2 and LTC1563-3						
Total Supply Voltage (V_S), HS Mode		●	3		11	V
Total Supply Voltage (V_S), LP Mode		●	2.7		11	V
Output Voltage Swing High (LPB Pin) HS Mode	V_S = 3V, f_C = 25.6kHz, R_{FIL} = 100k, R_L = 10k to GND	●	2.9	2.95		V
	V_S = 4.75V, f_C = 25.6kHz, R_{FIL} = 100k, R_L = 10k to GND	●	4.55	4.7		V
	V_S = ±5V, f_C = 25.6kHz, R_{FIL} = 100k, R_L = 10k to GND	●	4.8	4.9		V
Output Voltage Swing Low (LPB Pin) HS Mode	V_S = 3V, f_C = 25.6kHz, R_{FIL} = 100k, R_L = 10k to GND	●		0.015	0.05	V
	V_S = 4.75V, f_C = 25.6kHz, R_{FIL} = 100k, R_L = 10k to GND	●		0.02	0.05	V
	V_S = ±5V, f_C = 25.6kHz, R_{FIL} = 100k, R_L = 10k to GND	●		–4.95	–4.9	V
Output Swing High (LPB Pin) LP Mode	V_S = 2.7V, f_C = 25.6kHz, R_{FIL} = 100k, R_L = 10k to GND	●	2.6	2.65		V
	V_S = 4.75V, f_C = 25.6kHz, R_{FIL} = 100k, R_L = 10k to GND	●	4.55	4.65		V
	V_S = ±5V, f_C = 25.6kHz, R_{FIL} = 100k, R_L = 10k to GND	●	4.8	4.9		V
Output Swing Low (LPB Pin) LP Mode	V_S = 2.7V, f_C = 25.6kHz, R_{FIL} = 100k, R_L = 10k to GND	●		0.01	0.05	V
	V_S = 4.75V, f_C = 25.6kHz, R_{FIL} = 100k, R_L = 10k to GND	●		0.015	0.05	V
	V_S = ±5V, f_C = 25.6kHz, R_{FIL} = 100k, R_L = 10k to GND	●		–4.95	–4.9	V
DC Offset Voltage, HS Mode (Section A Only)	V_S = 3V, f_C = 25.6kHz, R_{FIL} = 100k	●		±1.5	±3	mV
	V_S = 4.75V, f_C = 25.6kHz, R_{FIL} = 100k	●		±1.0	±3	mV
	V_S = ±5V, f_C = 25.6kHz, R_{FIL} = 100k	●		±1.5	±3	mV
DC Offset Voltage, LP Mode (Section A Only)	V_S = 2.7V, f_C = 25.6kHz, R_{FIL} = 100k	●		±2	±4	mV
	V_S = 4.75V, f_C = 25.6kHz, R_{FIL} = 100k	●		±2	±4	mV
	V_S = ±5V, f_C = 25.6kHz, R_{FIL} = 100k	●		±2	±5	mV
DC Offset Voltage, HS Mode (Input to Output, Sections A, B Cascaded)	V_S = 3V, f_C = 25.6kHz, R_{FIL} = 100k	●		±1.5	±3	mV
	V_S = 4.75V, f_C = 25.6kHz, R_{FIL} = 100k	●		±1.0	±3	mV
	V_S = ±5V, f_C = 25.6kHz, R_{FIL} = 100k	●		±1.5	±3	mV
DC Offset Voltage, LP Mode (Input to Output, Sections A, B Cascaded)	V_S = 2.7V, f_C = 25.6kHz, R_{FIL} = 100k	●		±2	±5	mV
	V_S = 4.75V, f_C = 25.6kHz, R_{FIL} = 100k	●		±2	±5	mV
	V_S = ±5V, f_C = 25.6kHz, R_{FIL} = 100k	●		±2	±6	mV

A3.17 – WM-52B Omnidirectional Electret Microphone

Panasonic Microphone Cartridges

Omnidirectional Electret Condenser Microphone Cartridge

Series: **WM-52B/54B** (pin type)

■ Features

- High-cost performance, electret condenser microphone cartridge
- WM-52B series are low-voltage, 1.5V operation microphones and suitable for all telephone applications, intercoms, and computers.
- WM-54B series are low-voltage 2.5V operation microphones and suitable for tape recorders, telephone devices, and toys

■ Sensitivity

WM-52B

Vs = 1.5V
RL = 3.0kΩ

T	−44±3dB
Y	−42±3dB
U	−40±3dB
M	−44±2dB
H	−42±2dB
P	−40±2dB

WM-54B

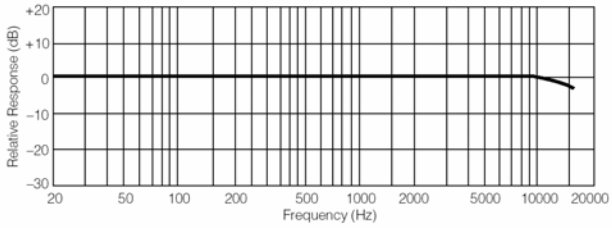
Vs = 2.5V
RL = 2.2kΩ

X	−46±3dB
T	−44±3dB
Y	−42±3dB
U	−40±3dB
M	−44±2dB
H	−42±2dB

■ Specifications

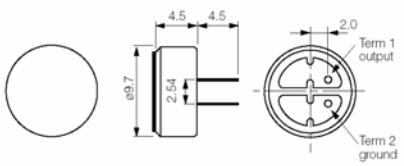
Sensitivity	See next page (0dB = 1V/pA, 1kHz)
Impedance	Less than 3.0kΩ [2.2kΩ]
Directivity	Omnidirectional
Frequency	20–16,000 Hz
Max. operation voltage	10V
Standard operation voltage	1.5V [2.5V]
Current consumption	Max. 0.3mA [0.6mA]
Sensitivity reduction	Within −3 dB at 1.1V [2V]
S/N ratio	More than 60dB

■ Typical Frequency Response Curve

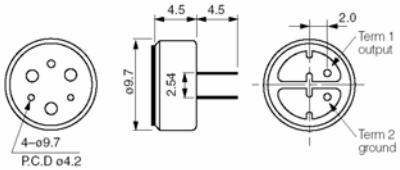


■ Dimensions in mm (not to scale)

WM-52B



WM-54B



Design and specifications are subject to change without notice. Ask factory for technical specifications before purchase and/or use.
Whenever a doubt about safety arises from this product, please contact us immediately for technical consultation.

A3.18 – 74VHC112 J-K Flip-Flop

FAIRCHILD SEMICONDUCTOR™

September 1995
Revised April 1999

74VHC112
Dual J-K Flip-Flops with Preset and Clear

General Description

The VHC112 is an advanced high speed CMOS device fabricated with silicon gate CMOS technology. It achieves the high-speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The VHC112 contains two independent, high-speed JK flip-flops with Direct Set and Clear inputs. Synchronous state changes are initiated by the falling edge of the clock. Triggering occurs at a voltage level of the clock and is not directly related to transition time. The J and K inputs can change when the clock is in either state without affecting the flip-flop, provided that they are in the desired state during the recommended setup and hold times relative to the falling edge of the clock. The LOW signal on PR or CLR prevents clocking and forces Q and $\overline{Q}$ HIGH, respectively.

Simultaneous LOW signals on PR and CLR force both Q and $\overline{Q}$ HIGH.

An input protection circuit ensures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

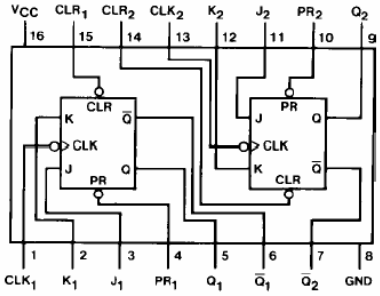
- High speed: f_{MAX} = 200 MHz (typ) at V_{CC} = 5.0V
- Low power dissipation: I_{CC} = 2 µA (max) at T_A = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
- Power down protection is provided on all inputs
- Pin and function compatible with 74HC112

Ordering Code:

Order Number	Package Number	Package Description
74VHC112M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74VHC112SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC112MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC112N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Pin Descriptions

Pin Names	Description
J_1, J_2, K_1, K_2	Data Inputs
CLK_1, CLK_2	Clock Pulse Inputs (Active Falling Edge)
CLR_1, CLR_2	Direct Clear Inputs (Active LOW)
PR_1, PR_2	Direct Preset Inputs (Active LOW)
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs

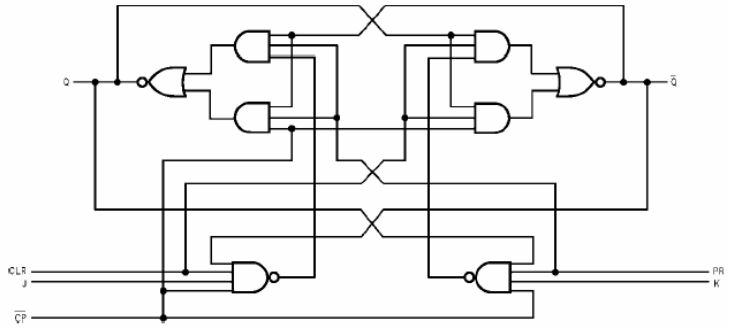
Truth Table

Inputs					Outputs	
PR	CLR	$\overline{CP}$	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	⌐	h	h	$\overline{Q}_0$	Q_0
H	H	⌐	l	h	L	H
H	H	⌐	h	l	H	L
H	H	⌐	l	l	Q_0	$\overline{Q}_0$

H (h) = HIGH Voltage Level
L (l) = LOW Voltage Level
X = Immaterial
⌐ = HIGH-to-LOW Clock Transition
Q_0 ($\overline{Q}_0$) = Before HIGH-to-LOW Transition of Clock
Lower case letters indicate the state of the referenced input or output one setup time prior to the HIGH-to-LOW clock transition.

Logic Diagram

(One Half Shown)



A3.19 – 74AC74 D-Type Flip-Flop

FAIRCHILD SEMICONDUCTOR™

November 1988
Revised November 1999

74AC74 • 74ACT74
Dual D-Type Positive Edge-Triggered Flip-Flop

General Description

The AC/ACT74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q, $\overline{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

Asynchronous Inputs:

LOW input to $\overline{S}_D$ (Set) sets Q to HIGH level

LOW input to $\overline{C}_D$ (Clear) sets Q to LOW level

Clear and Set are independent of clock

Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

Features

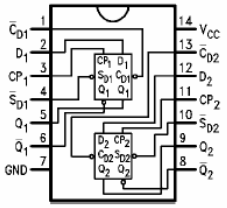
- I_{CC} reduced by 50%
- Output source/sink 24 mA
- ACT74 has TTL-compatible inputs

Ordering Code:

Order Number	Package Number	Package Description
74AC74SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Body
74AC74SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC74MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC74PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT74SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Body
74ACT74SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT74MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT74PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagram



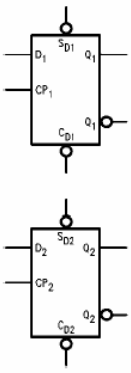
Pin Descriptions

Pin Names	Description
D_1, D_2	Data Inputs
CP_1, CP_2	Clock Pulse Inputs
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs
Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$	Outputs

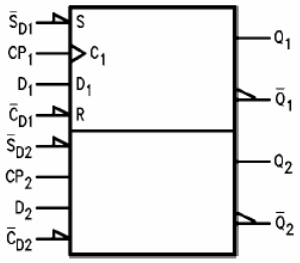
FACT™ is a trademark of Fairchild Semiconductor Corporation.

 DS009920

Logic Symbols



IEEE/IEC



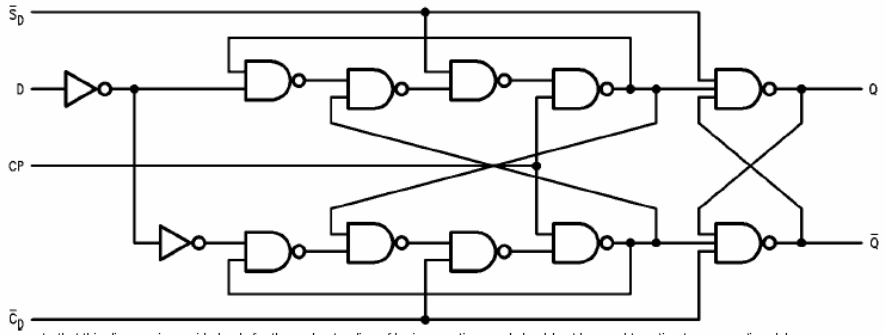
Truth Table

(Each Half)

Inputs				Outputs	
$\overline{S}_D$	$\overline{C}_D$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	⌐	H	H	L
H	H	⌐	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Clock Transition
Q_0 ($\overline{Q}_0$) = Previous Q ($\overline{Q}$) before LOW-to-HIGH Transition of Clock

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

A3.20 – 74VHC393 Dual 4-Bit Binary Counter

FAIRCHILD SEMICONDUCTOR™

March 1993
Revised March 1999

74VHC393
Dual 4-Bit Binary Counter

General Description

The VHC393 is an advanced high speed CMOS 4-bit Binary Counter fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. It contains two independent counter circuits in one package, so that counting or frequency division of 8 binary bits can be achieved with one IC. This device changes state on the negative going transition of the CLOCK pulse. The counter can be reset to "0" (Q_0–Q_3 = "L") by a HIGH at the CLEAR input regardless of other inputs.

An input protection circuit ensures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

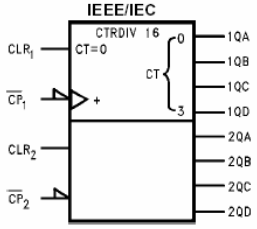
- High Speed: f_{MAX} = 170 MHz (typ) at T_A = 25°C
- Low power dissipation: I_{CC} = 4 μA (max) at T_A = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
- Power down protection is provided on all inputs
- Pin and function compatible with 74HC393

Ordering Code:

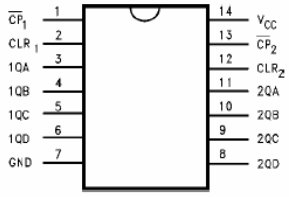
Order Number	Package Number	Package Description
74VHC393M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
74VHC393SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC393MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC393N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
CLR1, CLR2	Clear Inputs
$\overline{CP}_1$, $\overline{CP}_2$	Clock Pulse Inputs
QA, QB, QC, QD	Outputs

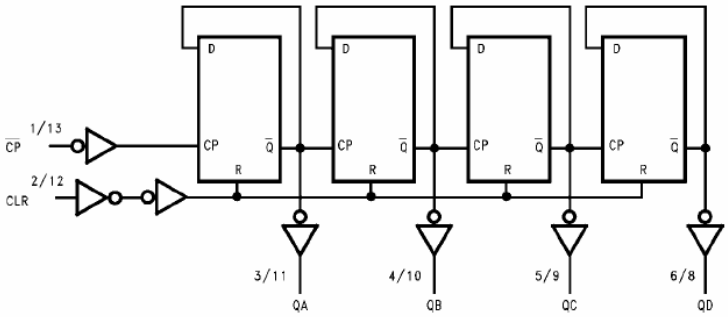
 DS011571.prf www.fairchildsemi.com

Truth Table

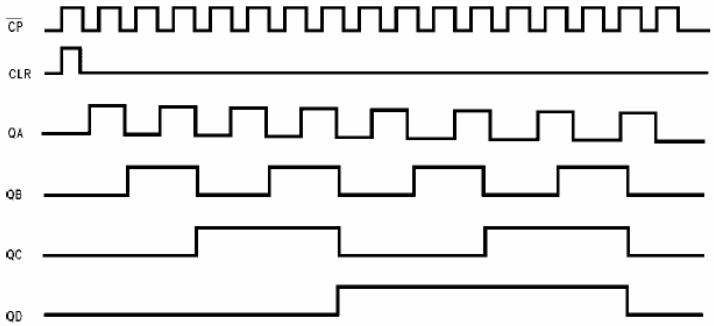
Inputs		Outputs			
$\overline{CP}$	CLR	QA	QB	QC	QD
X	H	L	L	L	L
↓	L	Count Up			
↑	L	No Change			

X: Don't Care

System Diagram



Timing Chart



A3.21 – 74AC32 Quad 2-Input OR Gate

FAIRCHILD SEMICONDUCTOR™

November 1988
Revised November 1999

74AC32 • 74ACT32
Quad 2-Input OR Gate

General Description

The AC/ACT32 contains four, 2-input OR gates.

Features

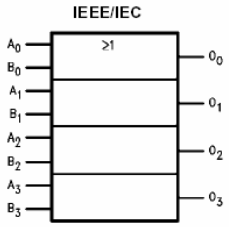
- I_{CC} reduced by 50% on 74AC only
- Outputs source/sink 24 mA
- ACT32 has TTL-compatible inputs

Ordering Code:

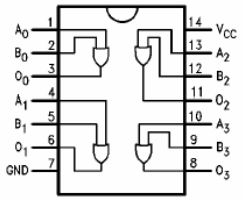
Order Number	Package Number	Package Description
74AC32SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Body
74AC32SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC32MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC32PC	N14A	14-Lead Plastic Dual-In-Line (PDIP), JEDEC MS-001, 0.300" Wide
74ACT32SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Body
74ACT32MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT32PC	N14A	14-Lead Plastic Dual-In-Line (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
A_n, B_n	Inputs
O_n	Outputs

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Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source	
or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current	
per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
PDIP	140°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
AC	2.0V to 6.0V
ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V)	T_A = +25°C Typ	T_A = −40°C to +85°C Guaranteed Limits		Units	Conditions
V_{IH}	Minimum HIGH Level Input Voltage	3.0	1.5	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum LOW Level Input Voltage	3.0	1.5	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum HIGH Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 µA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
							V_{IN} = V_{IL} or V_{IH}
		3.0		2.56	2.46		I_{OH} = −12 mA
		4.5		3.86	3.76	V	I_{OH} = −24 mA
		5.5		4.86	4.76		I_{OH} = −24 mA (Note 2)
V_{OL}	Maximum LOW Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 µA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
							V_{IN} = V_{IL} or V_{IH}
		3.0		0.36	0.44		I_{OL} = 12 mA
		4.5		0.36	0.44	V	I_{OL} 24 mA
		5.5		0.36	0.44		I_{OL} = 24 mA (Note 2)
I_{IN} (Note 4)	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	µA	V_I = V_{CC}, GND
I_{OLD}	Minimum Dynamic Output Current (Note 3)	5.5			75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−75	mA	V_{OHD} = 3.85V Min
I_{CC} (Note 4)	Maximum Quiescent Supply Current	5.5		2.0	20.0	µA	V_{IN} = V_{CC} or GND

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

A3.22 – 74AC138 1-of-8 Decoder

FAIRCHILD SEMICONDUCTOR™

November 1988
Revised August 2000

74AC138 • 74ACT138
1-of-8 Decoder/Demultiplexer

General Description

The AC/ACT138 is a high-speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high-speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three AC/ACT138 devices or a 1-of-32 decoder using four AC/ACT138 devices and one inverter.

Features

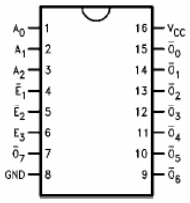
- I_{CC} reduced by 50%
- Demultiplexing capability
- Multiple input enable for easy expansion
- Active LOW mutually exclusive outputs
- Outputs source/sink 24 mA
- ACT138 has TTL-compatible inputs

Ordering Code:

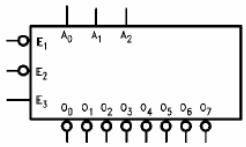
Order Number	Package Number	Package Description
74AC138SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74AC138SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC138MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC138PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
74ACT138SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74ACT138SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT138PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

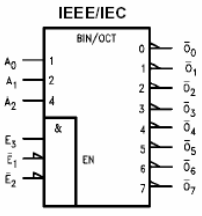
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagram



Logic Symbols





Pin Descriptions

Pin Names	Description
A_0–A_2	Address Inputs
$\overline{E}_1$–$\overline{E}_2$	Enable Inputs
E_3	Enable Input
$\overline{O}_0$–$\overline{O}_7$	Outputs

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Truth Table

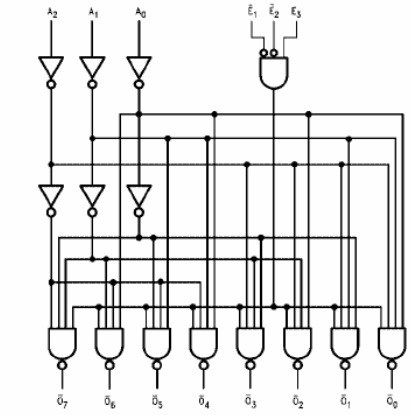
Inputs						Outputs							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial

Functional Description

The AC/ACT138 high-speed 1-of-8 decoder/demultiplexer accepts three binary weighted inputs (A_0, A_1, A_2) and, when enabled, provides eight mutually exclusive active-LOW outputs ($\overline{O}_0$–$\overline{O}_7$). The AC/ACT138 features three Enable inputs, two active-LOW ($\overline{E}_1$, $\overline{E}_2$) and one active-HIGH (E_3). All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four AC/ACT138 devices and one inverter (see Figure 1). The AC/ACT138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active-HIGH or active-LOW state.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

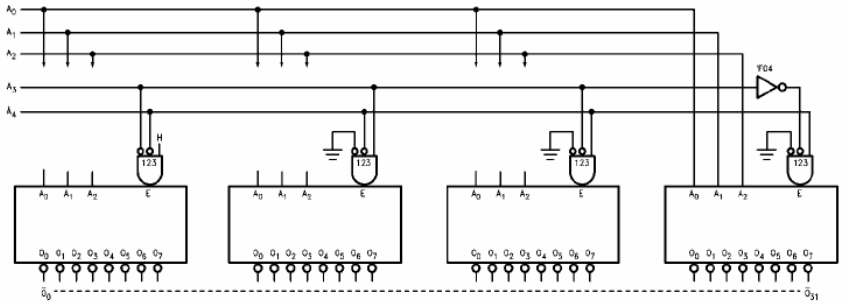


FIGURE 1. Expansion to 1-of-32 Decoding

A3.23 – 74HC30 8-input NAND Gate

TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS121B

August 1997 - Revised March 2002

CD54/74HC30, CD54/74HCT30

High Speed CMOS Logic 8-Input NAND Gate

Features

- **Buffered Inputs**
- **Typical Propagation Delay: 10ns at V_{CC} = 5V, C_L = 15pF, T_A = 25°C**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55°C to 125°C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}**

Description

The 'HC30 and 'HCT30 each contain an 8-input NAND gate in one package. They provide the system designer with the direct implementation of the positive logic 8-input NAND function. Logic gates utilize silicon gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LSTTL loads. The HCT logic family is functionally pin compatible with the standard LS logic family.

Ordering Information

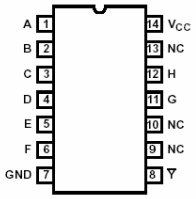
PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC30F	-55 to 125	14 Ld CERDIP
CD54HC30F3A	-55 to 125	14 Ld CERDIP
CD74HC30E	-55 to 125	14 Ld PDIP
CD74HC30M	-55 to 125	14 Ld SOIC
CD54HC30NSR	-55 to 125	14 Ld SOP
CD54HCT30F3A	-55 to 125	14 Ld CERDIP
CD54HCT30H	-55 to 125	Die
CD74HCT30E	-55 to 125	14 Ld PDIP
CD74HCT30M	-55 to 125	14 Ld SOIC

NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Die for this part number is available which meets all electrical specifications. Please contact your local TI sales office or customer service for ordering information.

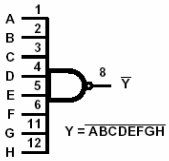
Pinout

CD54HC30, CD54HCT30 (CERDIP)
CD74HC30 (PDIP, SOIC, SOP)
CD74HCT30 (PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Functional Diagram

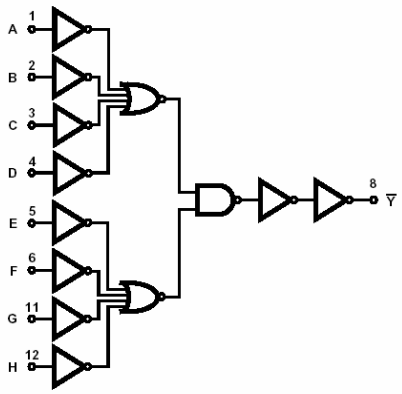


TRUTH TABLE

INPUTS								OUTPUT
A	B	C	D	E	F	G	H	
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L

NOTE: H = HIGH Voltage Level, L = LOW Voltage Level, X = Irrelevant

Logic Symbol



A3.24 – 74AC04 Hex Inverter

FAIRCHILD SEMICONDUCTOR™

November 1988
Revised November 1999

74AC04 • 74ACT04
Hex Inverter

General Description

The AC/ACT04 contains six inverters.

Features

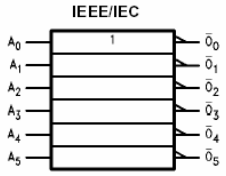
- I_{CC} reduced by 50% on 74AC only
- Outputs source/sink 24 mA
- ACT04 has TTL-compatible inputs

Ordering Code:

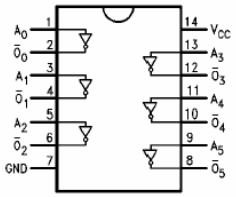
Order Number	Package Number	Package Description
74AC04SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Body
74AC04SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC04MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC04PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT04SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Body
74ACT04MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT04PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code. (PC not available in Tape and Reel.)

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
A_n	Inputs
$\overline{O}_n$	Outputs

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Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	−20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
PDIP	140°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
AC	2.0V to 6.0V
ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$ Typ	$T_A = -40°C$ to $+85°C$ Guaranteed Limits		Units	Conditions
V_{IH}	Minimum HIGH Level Input Voltage	3.0	1.5	2.1	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum LOW Level Input Voltage	3.0	1.5	0.9	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum HIGH Level Output Voltage	3.0	2.99	2.9	2.9	V	$I_{OUT} = -50\ \mu A$
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
							$V_{IN} = V_{IL}$ or V_{IH}
		3.0		2.56	2.46		$I_{OH} = -12$ mA
		4.5		3.86	3.76	V	$I_{OH} = -24$ mA
		5.5		4.86	4.76		$I_{OH} = -24$ mA (Note 2)
V_{OL}	Maximum LOW Level Output Voltage	3.0	0.002	0.1	0.1	V	$I_{OUT} = 50\ \mu A$
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
							$V_{IN} = V_{IL}$ or V_{IH}
		3.0		0.36	0.44		$I_{OL} = 12$ mA
		4.5		0.36	0.44	V	$I_{OL} = 24$ mA
		5.5		0.36	0.44		$I_{OL} = 24$ mA (Note 2)
I_{IN} (Note 4)	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	$V_I = V_{CC}$, GND
I_{OLD}	Minimum Dynamic Output Current (Note 3)	5.5			75	mA	$V_{OLD} = 1.65V$ Max
I_{OHD}		5.5			−75	mA	$V_{OHD} = 3.85V$ Min
I_{CC} (Note 4)	Maximum Quiescent Supply Current	5.5		2.0	20.0	μA	$V_{IN} = V_{CC}$ or GND

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

A3.25 – TU–400E USB Hub

4 Port USB Mini Hub, Bus–Powered USB Hub 4 Ports (TU–400E)

The TU-400E is a highly integrated 4-port USB hub. It consists of one upstream and four downstream ports and was designed to bridge USB interfaced peripherals to your desktop or notebook computer. The TU-400E complies with USB 1.0/1.1 specifications and supports both full (12Mbps) and low (1.5Mbps) data rate speeds. With Plug-and-Play and Hot-Swap, you can easily connect/disconnect USB equipped camera, network adapter, modem, and joystick to your computer. Connect each port to another USB hub for limited expansion. Compact, light-weighted, and requiring no external power, the TU-400E is ideal for SOHO and mobile computing. Compatible with Universal Serial Bus Rev. 1.0 and 1.1 Specification

- Plug-and-Play (PnP) and Hot-Swappable
- Supports Windows 98 / ME/2000 and iMAC / Macintosh
- Easy expansion with other USB Hubs, allows the use of up to 127 devices
- Supports 1 upstream and 4 downstream USB ports
- All downstream ports support high-speed (12Mbps) and low-speed (1.5Mbps) operations mode
- Power control/overload detection on each individual USB port
- Single status LED
- Bus-Powered; does not require AC Power Adapter
- 5-Year Warranty

Movies

1. EvBot II exploring the maze

2. EvBot II exploring the maze (2)

3. Two generations of EvBots in the maze

4. EvBot II moving towards a sound source

5. Simulation of the EvBot sonar for a sound frequency of 1 KHz

6. EvBot sonar tracking a 1 KHz sound source

7. EvBot sonar tracking the sound of an airplane reproduced by a nearby speaker