Capacitive Micromachined Ultrasonic Transducers: Fabrication Technology

Arif Sanlı Ergun, Member, IEEE, Yongli Huang, Student Member, IEEE,

Xuefeng Zhuang, Student Member, IEEE, Ömer Oralkan, Member, IEEE, Göksen G. Yarahoğlu, Member, IEEE, and Butrus T. Khuri-Yakub, Fellow, IEEE

Abstract-Capacitive micromachined ultrasonic transducer (cMUT) technology is a prime candidate for next generation imaging systems. Medical and underwater imaging and the nondestructive evaluation (NDE) societies have expressed growing interest in cMUTs over the years. Capacitive micromachined ultrasonic transducer technology is expected to make a strong impact on imaging technologies, especially volumetric imaging, and to appear in commercial products in the near future. This paper focuses on fabrication technologies for cMUTs and reviews and compares variations in the production processes. We have developed two main approaches to the fabrication of cMUTs: the sacrificial release process and the recently introduced wafer-bonding method. This paper gives a thorough review of the sacrificial release processes, and it describes the new wafer-bonding method in detail. Process variations are compared qualitatively and quantitatively whenever possible. Through these comparisons, it was concluded that waferbonded cMUT technology was superior in terms of process control, yield, and uniformity. Because the number of steps and consequent process time were reduced (from six-mask process to four-mask process), turn-around time was improved significantly.

I. INTRODUCTION

APACITIVE micromachined ultrasonic transducers $\mathcal{I}(\text{cMUTs})$ were introduced to the ultrasound community about a decade ago. Initially, the interest in cMUTs was for airborne applications such as nondestructive evaluation (NDE), mainly because at the time the cavity could not be sealed. Once techniques were developed to seal their cavity, cMUTs began to appear in immersion applications, first in underwater imaging and later in medical imaging. Consequently, research interest has increased for both technology development and modeling. Early on, the Office of Naval Research (ONR) approached cMUT technology aggressively to build underwater ultrasound imaging cameras. Recently, the medical imaging community has taken the lead in commercialization of cMUT technology. This paper focuses on the fabrication technology of cMUTs, comparing variations in the fabrication techniques for output, process control, and yield.

The first versions of capacitive ultrasonic transducers were built using conventional machining tools [1]. A rough metal surface was used as the back plate of the capacitor, and a metallized mylar membrane made up the top electrode. Later versions of these capacitive ultrasonic transducers used micromachining instead of conventional machining to define the cavities on silicon [2], [3]. Although micromachining allowed precise control over the gap size, these devices did not fully use micromachining techniques: metallized dielectric films (kapton, mylar, or polyester) were used as the membrane material, which did not allow vacuum sealing. Fully micromachined versions of capacitive ultrasonic transducers were introduced in 1994 [4] and were called capacitive micromachined ultrasonic transducers (later abbreviated as cMUT to clarify the distinction between piezoelectrically and capacitively actuated transducers).

The first cMUTs were built using a sacrificial release process that has become the standard cMUT fabrication method. Numerous variations of the sacrificial release process have been published, all based on the same basic principle. The cavity underneath the membrane is created by depositing or growing a sacrificial layer on the carrier substrate. After the membrane deposition, the sacrificial layer is removed with an etchant, specifically chosen to etch the sacrificial layer material but not to etch the membrane layer material. A number of sacrificial layer, membrane, and substrate material combinations can be used to fabricate cMUTs. Although the fabrication method remains more or less the same, the combination of materials makes a difference in the design, process control, and overall device yield.

Because the highest temperature in the process determines whether cMUTs can be processed on the same wafer with the electronics, cMUT processes can be categorized as low and high temperature processes. If the cMUTs are built on the same silicon substrate with the CMOS electronic circuitry, the highest temperature throughout the process cannot exceed 400°C. Such low-temperature processes often are called CMOS compatible. All other types are simply called high-temperature processes. The advantages and disadvantages of each type will be discussed later. In Section II, we will briefly describe the hightemperature sacrificial release process developed at Stanford University. Low-pressure chemical vapor deposited (LPCVD) silicon nitride (Si_3N_4) is the membrane, and LPCVD poly-silicon is the sacrificial layer material in this process. Potassium hydroxide (KOH), which has very good selectivity between LPCVD silicon nitride and poly-silicon

Manuscript received September 29, 2004; accepted June 29, 2005. The authors are with the Edward L. Ginzton Laboratory, Stanford University, Stanford, CA 94305-4088 (e-mail: sanli@stanford.edu).

(>400,000:1), removes the sacrificial layer. In Section III, we will discuss variations of the sacrificial release processes, and compare them qualitatively. In Section IV, we will give our perspective on the two-dimensional array fabrication and on electronic integration in general.

The wafer-bonding method is a new cMUT fabrication technique, based on a different approach to cavity formation that uses a combination of bulk and surface micromachining techniques [5]. Section V will describe this recently developed wafer-bonded cMUT process. By comparing the basic number of steps used in the wafer-bonding method to the number of steps in the sacrificial release method, we will show that the wafer-bonding method simplifies cMUT fabrication considerably, offering many advantages over the sacrificial-release processes. Section VI will discuss these advantages, together with possible process variations to further improve acoustical output and reliability.

II. SACRIFICIAL-RELEASE PROCESS

The sacrificial-release process begins with a conductive silicon wafer. The silicon wafer is doped to achieve high conduction at its surface, which is the back electrode in cMUT operation. Silicon nitride is then deposited at 785°C with LPCVD. The composition of the gases is adjusted to obtain a low-stress Si_3N_4 film [dichlorosilane (DCS) to ammonia (NH_3) ratio of 14:1]. Typically, the Si₃N₄ films deposited with such conditions have < 100 MPa tensile stress and a refractive index of 2.4. This layer—also called the etch-stop layer—must be sufficiently thick to protect the silicon wafer from the etchant during the long, wet sacrificial layer etch. Because the capacitance of this layer comes in series with the active gap capacitance, it should not be arbitrarily thick. In principle, a few hundred Angstroms of Si_3N_4 is sufficient; however, typically, over 1000 Å thick etch-stop layer is used to avoid problems with possible pin holes (common in thin Si_3N_4 layers).

Sacrificial-layer deposition and patterning is done in two steps, so that the channels KOH uses to remove the sacrificial layer are thinner than the cavity thickness. In the first step, a layer of LPCVD poly-silicon is deposited, and regions of reduced channel height are defined by photolithography. The subsequent dry etch removes all the poly-silicon in the defined regions, but it stops at the Si_3N_4 layer underneath [Fig. 1(a)]. Another thin layer of poly-silicon deposition follows the first [Fig. 1(b)]. The thickness of the second poly-silicon layer determines the thickness of the channels; total poly-silicon thickness from the first and second depositions determines the initial cavity height. Low temperature depositions are preferred for better thickness control.

Another photolithography and dry etch step follows the second poly-silicon deposition, defining the cavity and the membrane shape, together with the etch channels [Fig. 1(c)]. In general, the membrane can be any shape, but circles and hexagons are easier to model and are used most often. Both the shape and the size of the membrane



Fig. 1. Sacrificial-release process with LPCVD Si_3N_4 membrane. (a) Substrate doping, etch-stop layer deposition, first sacrificial layer deposition and patterning. (b) Reduced etch channel height regions. (c) Active area definition. (d) Membrane deposition. (e) Sacrificial layer etch hole definition and Si_3N_4 etch. (f) Membrane release in KOH. (g) Membrane sealing with more Si_3N_4 deposition. (h) Top electrode deposition and patterning.

are critical cMUT design parameters that determine the frequency response of the element.

The next step is the critical membrane deposition [Fig. 1(d)]. Like the etch-stop layer, the membrane is composed of low-stress Si_3N_4 deposited by LPCVD at 785°C. Because another layer of Si_3N_4 will be added during the sealing step, the Si_3N_4 thickness at this time is not the final membrane thickness.

Next, a lithography and dry etch step opens small holes through the Si_3N_4 layer [Fig. 1(e)]. The etch holes are located on the etch channels, so that when the wafer is immersed in KOH solution, KOH etches its way to the cavity through the channels and releases the membrane [Fig. 1(f)]. The poly-silicon etch rate of KOH is highly dependent on temperature [6]. At room temperature, the etch may take several days, depending on the membrane size. This slow rate is due, in part, to the narrow and thin etch channels, which limit the diffusion of KOH. During the long KOH etch, the etch-stop layer protects the silicon wafer. Near boiling point, the wet release may be as fast as several hours. However, because the etch selectivity worsens at high temperatures, this fast release process is not always preferred.

The next step in the process seals the holes with another layer of LPCVD Si_3N_4 [Fig. 1(g)]. Because Si_3N_4 is deposited at low pressure, the cavity is considered vacuumsealed for practical purposes. In immersion applications, including medical imaging, the cavity must be sealed; otherwise, fluid fills the cavity and hinders proper cMUT operation. Squeeze film damping will load the membrane vibrations, making the transducer inefficient. For the same reason (but with less effect), it also is undesirable to leave air inside the cavity while sealing [7], [8].

The rest of the process establishes the electrical connections from the bond pads to the top and bottom electrodes. A lithography and etch step opens connections to the ground plane through the Si_3N_4 layers. Subsequently, aluminum is sputtered over the whole wafer and patterned by lithography and wet etch [Fig. 1(h)]. Because it provides conformal coverage, sputtering is preferred for this step. This final lithography and etch step defines the top electrode coverage over the membrane. After depositing the metal, it is best to anneal the wafer to establish good ohmic contact to ground. However, annealing generates high tensile stress in the aluminum electrode (~ 500 MPa), which alters both the static deflection under atmospheric pressure and the mechanical resonance frequency of the membranes. Because a sufficiently good ohmic contact still may be obtained, it is possible to skip the annealing step. Otherwise, high tensile stress must be accounted for in designing the cMUT.

III. VARIATIONS AND ISSUES OF THE SACRIFICIAL-RELEASE PROCESSES

A. Substrate Material and Back Electrode

Although its electronic properties are rarely used, silicon is the most popular substrate material for cMUT fabrication. The silicon substrate is, in essence, both a mechanical platform on which the membranes are built and an electrical ground plane. In general, it may be replaced by any other substrate material, provided that material has a conductive surface. Quartz is an attractive alternative. Although quartz is an insulator, it can be coated with a conductive layer of poly-silicon or metal to form the ground plane. The choice of conductive layer depends on the subsequent processing steps. For low temperature processes, this layer can be any of the common metals. For high temperature processes (similar to the one described above), this layer must be either doped poly-silicon or a metal with a high melting point, such as tungsten. Quartz is a perfect insulator, and it is optically transparent. The bottom electrode can be patterned to reduce parasitic capacitance, or it can be patterned in the form of fingers, creating a diffraction grating with the membrane so that optical sensing methods can be used [9]. The patterned back electrode concept can be implemented on very high resistive silicon wafers as well [10].

In variations in which the cMUT is integrated with the electronics, the substrate material is silicon, and the back electrode is either an n-well or aluminum, both of which are patterned to reduce parasitic capacitance [11]–[13]. When patterned, the surface topology of the back electrode is transferred to the membrane. Although selectively doped poly-silicon layers and n-wells in silicon wafers do not have significant topology, the profile of the metal back electrodes can be problematic, especially when the gap height is comparable to or thinner than the thickness of the back electrode metal.

B. Sacrificial Layer Deposition and Cavity Definition

The sacrificial poly-silicon has high compressive stress (-400 to -500 MPa, depending on the thickness), which poses a problem for releasing large membranes (>~100 μ m in diameter for circular membranes). When high compressive stress is released by the sacrificial layer etch, large membranes tend to break. Rectangular membranes experience worse problems as the aspect ratio increases. Depositing a buffer layer of LPCVD phospho-silicide-glass (PSG, phosphorus doped low-temperature silicon dioxide) between poly-silicon and Si₃N₄ is a partial solution. If the sacrificial layer is deposited as a composite layer of polysilicon and PSG, it is possible to fabricate membranes as large as 160 μ m in diameter. The down side of this process is the lack of uniformity in the PSG deposition.

C. Membrane Deposition and Wet Release

Ideally, the initial membrane deposition thickness would be the final membrane thickness minus the amount added during sealing. However, there is a constraint on the initial membrane thickness: it must be thicker than a critical value to avoid sticktion. The sticktion problem arises during the drying process, after the removal of the sacrificial layer. As the water in the cavity evaporates, capillary forces from surface tension pull the membrane toward the substrate. If the membrane is not sufficiently stiff, these forces may overcome the restoring force of the membrane and stick the membrane to the substrate, a process that generally is irreversible [14]–[17].

Sticktion is a common issue associated with all wetrelease processes, but there are ways of avoiding it: freeze drying [18], supercritical drying [19], and dry release [20]– [22]. In freeze drying, deionized (DI) water left in the cavity after the wet release is replaced by another chemical, which is subsequently frozen and sublimed at low pressure. Supercritical drying is a similar method in which the DI water is replaced with liquid carbon dioxide. At the critical temperature and pressure, carbon dioxide is in the supercritical phase in which there is no liquid-vapor interface, and therefore no capillary forces. If appropriate membrane and sacrificial-layer materials are used, a dry-release process is most convenient. Dry release works in the same way as wet release, except that, instead of a wet chemical, a plasma removes the sacrificial layer. For example, when silicon dioxide is used as the membrane material, xenon difluoride (XeF_2) is commonly used to selectively etch silicon.

There are a number of variations to consider when choosing the sacrificial layer and the membrane material. One example is to chose LPCVD silicon dioxide as the sacrificial layer, and LPCVD deposited and doped polysilicon as the membrane material [11], [12], [23]. Liquid or vapor hydrofluoric acid (HF), which has excellent selectivity between silicon dioxide and poly-silicon, can be used to remove the sacrificial silicon dioxide layer. Because the poly-silicon membrane is conductive, an insulation layer is required between the membrane and the silicon back electrode. Etch rate selectivity of HF between silicon dioxide and Si_3N_4 is only ~100 to 1. Hence, the thickness of the insulation layer and the wet release of the membranes require careful design so as not to etch the insulation layer completely. The high-stress levels of the LPCVD polysilicon also must either be eliminated with additional steps, or taken into account in the design. The LPCVD Si_3N_4 also can be used as the membrane material, but it suffers from poor etch selectivity and results in radially varying membrane thicknesses. In a similar variation, plasmaenhanced chemical vapor deposition (PECVD) is used to deposit the sacrificial silicon dioxide and Si_3N_4 layers [24]. The reported etch rate selectivity between PECVD silicon dioxide and Si_3N_4 is 200:1, which is not adequate for membrane-to-membrane thickness uniformity. In general, wet etching of the sacrificial layer requires very good etch rate selectivity to avoid problems with etch uniformity.

Whether LPCVD or PECVD is used in depositing the Si_3N_4 membrane, the problem of stress in the membrane remains. By changing the composition of the gasses in the LPCVD reactor, it is possible to control the stress in the Si_3N_4 film. The radio frequency (RF) frequency and the power of PECVD reactors also can be tuned to reduce the film stress. However, in both cases, the quality of the Si_3N_4 film will deteriorate. The selectivity of the wet etchant drops greatly, and makes the sacrificial release impossible. A compromise between stress and quality usually can be achieved where the stress is low tensile or low compressive and the quality is moderate. For PECVD deposited Si₃N₄ films, the sacrificial release process remains a problem due to poor selectivity between Si₃N₄ and silicon dioxide or poly-silicon. However, other films such as polymide [25], [26] and chromium [9] have been successfully used as sacrificial layers in conjunction with low-stress PECVD Si₃N₄ membranes. Because polymide is spun-coated and etched to final thickness, and chromium is deposited to the final



Fig. 2. Optical pictures of several cMUT elements with different membrane shapes and sizes to show its relation to the active area coverage. (a) The 24 μ m diameter circular membranes has approximately 50% active area coverage. (b) The 80 μ m diameter circular membranes has 72% active area coverage. (c) The 80 μ m diameter hexagonal membranes has 86% active area coverage. (d) Tented membranes in which the etch holes are located on the post have over 90% active area coverage.

thickness, chromium is the better choice for gap thickness control.

Numerous combinations of materials and processes can be used to fabricate membranes. Although each has advantages and disadvantages, the issues of uniformity, repeatability, and controllability are common to all. Traditionally, LPCVD has been the preferred deposition method for uniformity [27], but there is not sufficient data on waferto-wafer uniformity, process repeatability, and control to make a strong statement about these issues.

D. Membrane Sealing and Thickness Control

The LPCVD Si₃N₄ has a very low sticking coefficient, which means that a molecule will not stick to the wafer surface immediately. Consequently, while sealing the etch holes, some amount of Si₃N₄ will deposit into the cavity. Because past experience shows that approximately onethird of the initial cavity height will remain after the etch holes are completely sealed [28], [29], narrow etch channels are needed for more efficient sealing. By defining the cavity and channel heights separately (in two steps), it is possible to reduce Si_3N_4 deposition into the cavity. Fig. 2(a) is an optical picture that shows circular membranes and etch channels (i) leading to the membranes from the etch holes (*ii*). The reduced channel height can be as low as 0.04 μ m, which means quick sealing of the etch holes, minimal deposition inside the cavity, elimination of the etch-back step to finalize the membrane thickness, and consequently better control of gap height and membrane thickness.

The problem with Si_3N_4 sealing is that it requires long etch channels, reduced channel height, or both. In each case, the price of efficient sealing and good thickness control is loss of active area, which eventually translates into loss of output pressure and receive sensitivity. For large membranes, the fractional loss is not that significant. However, as the membrane size decreases for high-frequency applications, the fractional active area loss becomes an issue. Fig. 2 shows optical pictures of four membranes where Fig. 2(a) has 24 μ m, and Fig. 2(b), (c), and (d) have 80 μ m diameter membranes. In the case of the small membrane, it is evident that half of the active area is lost. For the 80 μ m circular membrane, the active area coverage is considerably better (72%). Using hexagonal membranes as shown in Fig. 2(c), it is possible to reduce the size of the etch channels and increase the active area coverage to 86%. It is also possible to remove the posts between the hexagonal membranes to create tented membranes [shown in Fig. 2(d) with more than 90% active area coverage. A previous version of this process used e-beam lithography to open tiny holes through the Si_3N_4 membrane [30], instead of using long etch channels defined by g-line lithography. The reduction in cost obtained by using g-line lithography comes at the expense of loss of active area.

The LPCVD deposited low temperature silicon dioxide (LTO) is an alternate solution to Si_3N_4 to seal the etch holes [12], [23], [28]. Because LPCVD LTO has a higher sticking coefficient than Si_3N_4 , it is possible to seal the etch holes without long etch channels, and the active area coverage can be improved, even for small membranes. There is one minor issue with LTO sealing. Because of its high sticking coefficient, LTO is not capable of sealing very small holes, so the etch hole size must be larger than 2 μ m in diameter; [28] and [29] provide details on LTO sealing. The PECVD Si₃N₄ works in the same manner, sealing the holes locally without the need for long channels [9], [24].

E. Top Electrode Definition and Coverage

The electrode coverage determines the electromechanical transformer ratio and the parasitic capacitance, consequently, both the efficiency with which the electrical energy is transformed into mechanical energy and the frequency bandwidth. Past work on this subject has shown that, with coverage greater than half-metallization of the membrane radius, while there is not much improvement in the electromechanical transformation ratio, the parasitic capacitance increases almost linearly with the electrode area [31], [32]. However, if there are other dominant parasitic capacitance sources, coverage area can be larger without effecting the bandwidth.

Aluminum is the most common electrode material used in cMUT fabrication, mostly for historical reasons. As long as their mechanical properties are taken into account, other metals are equally suitable. Chromium and gold have been used successfully [9], [33], [34], and other possible alternatives are tungsten and copper.

F. Embedding the Top Electrode and Passivation

One optional process variation is to embed the top electrode inside the membrane, thereby reducing the dielectric thickness below the top electrode. Ideally, it is best to have no dielectric layer (other than vacuum) between the two electrodes of the capacitor. This arrangement is not practical because it is likely to cause an electrical short between the electrodes. By reducing the dielectric thickness under the electrode as much as possible, without changing the overall membrane thickness, the E-field share of the gap and the capacitance increase, and the impedance matching to the electronics improves. When aluminum is the top electrode, the top membrane layer must be a material deposited at low temperature ($< 500^{\circ}$ C). LTO commonly has been used for this purpose [27], [29], [35]; in this case, the membrane becomes a compound membrane composed of three layers (including the metal layer), and must be modeled accordingly.

Other options are to use a suitable metal with high melting point or doped poly-silicon rather than aluminum, then bring the membrane to the right thickness with LPCVD Si_3N_4 , so that the membrane is a monolayer. These are better options for process control, uniformity, and modeling. When phosphorus-doped poly-silicon is used as an embedded electrode, the diffusion time and temperature are chosen to minimize the stress in the polysilicon film [36]–[38]. Because doped poly-silicon has lower conductivity than aluminum, creating a monolayer membrane of Si_3N_4 in this way requires compromise in series resistance.

An optional final step in cMUT fabrication is passivation of the top electrode. Because the top electrode is the hot electrode, it is necessary to isolate it from the surrounding medium in most cases. Embedding the electrode inside the membrane, as described above, readily solves this issue. One-dimensional medical imaging arrays always are covered with a lens to focus the acoustic beam in the elevation direction. Such lenses are insulating, and isolate the top electrode from the outside. However, twodimensional arrays do not use a lens; applying a thinner coating with minimal attenuation is the best solution for a two-dimensional array. For example, parylene coating can be as thin as a few micrometers and provide adequate conformal coverage. When the cMUT is covered with a passivation layer, the membrane becomes a compound structure. Although the coating usually is much softer than the membrane material (smaller Young's modulus), it also might be thicker than the membrane and must be taken into account in such cMUT designs.

G. LPCVD versus PECVD

As described in detail in the previous subsections, the main issues with the sacrificial-release processes include: control over the mechanical properties of the membrane material, control over the thicknesses, repeatability, and limited design space [very large (>160 μ m in diameter)

and thick membranes are impossible to realize, due to residual stress of the films].

Whether it is a LPCVD or a PECVD reactor, control over the mechanical properties of the membrane material actually is equivalent to control over the deposition conditions of the films (that is, how a particular piece of equipment is maintained and calibrated). Because thermal excitation of the molecules increases the likelihood of making appropriate bonds, high-temperature processes, in general, are better for the quality of the film. Therefore, PECVD films have relatively more vacant bond sites, resulting in a relatively more porous film than LPCVD films. The quality of the film affects dielectric breakdown, dielectric charging, mechanical fatigue, uniformity, and chemical etch properties.

In general, LPCVD reactors are large tubes that can take more than 100 wafers at a time; PECVD reactors are much smaller in size and can handle only a handful of wafers. The LPCVD reactors are slow in terms of deposition and operation; PECVD reactors are easy to operate and have high-deposition rates. Deciding which technology to use depends on volume, availability of resources, and device specifications. Cost, the determining factor for production, is best judged by the industry according to these criteria. The LPCVD seems to be slightly favored for volume production, but wafer-to-wafer uniformity, repeatability, and predictability remain issues of concern.

H. Process Temperature and Electronic Integration

In comparison to piezoelectric transducers, cMUTs have low device capacitance, making them more vulnerable to parasitic capacitance. In two-dimensional arrays, the element size is limited by the Nyquist criterion and the desired viewing angle. Consequently, the device capacitance is so small that any cable connecting the cMUT to the electronics is unacceptable. Parasitic capacitance is an issue even in one-dimensional arrays, and is best handled by bringing the receiving electronics as close to the array as possible. Processing cMUTs on a CMOS or a BiCMOS chip has received substantial interest. In this method, the cMUT is processed directly on a CMOS (or BiCMOS) chip monolithically integrated with the electronics, thus minimizing the parasitics between the cMUT and the electronics. Because the electronic circuitry puts a limit on the highest temperature allowed, the highest temperature in the process becomes an important parameter for this type of integration.

There are three main approaches to the monolithic integration of the electronics with cMUTs: preprocessing, coprocessing, and postprocessing. In preprocessing, cMUTs are fabricated on the silicon substrate before the electronics. Because of the difficulty of carrying on an integrated circuit process on a substrate with cMUTs, this approach received no interest. Eccardt *et al.* [11] were the first to integrate the electronics with cMUTs on the same chip using the coprocessing method, by adding a few steps

to a standard BiCMOS process line. This approach provided a simple and cost-effective integration, but it was limited to small integrated sensors because it did not allow any control over the gap, the membrane thickness, or the residual stress of the membrane. The electronics and the cMUTs also shared the same area, making this approach unsuitable for two-dimensional arrays. The third monolithic integration method, postprocessing of cMUTs on CMOS electronics using a low-temperature cMUT fabrication method, is the most viable monolithic solution. Initially, the electronics were laid out by reserving areas for cMUT fabrication [39]. The low-temperature process, described in [25], followed the electronic integration, allowing much better control over the dimensions. A newer version of this process [40] did not reserve an area on the electronic circuit layout, but instead fabricated the cMUTs directly on top of the electronics by depositing a passivation layer in between. Thus, the entire process was carried out on the same wafer. This third solution is the best monolithic approach for packing density, and it allows the fabrication of two-dimensional cMUT arrays integrated with the transmit/receive electronics on the same wafer. However, such a two-dimensional cMUT array (monolithically integrated with the full transmit/receive electronics) has not yet been reported. Up to date, the electronics underneath the cMUT array have been limited to receive-only electronics [40], or to switches [41] for reconfigurable array applications.

In general, monolithic integration of microelectromechanical systems (MEMS) devices with the driving electronics has significant performance advantages due to reduced parasitics. However, because of the large number of steps involved, monolithic processes are highly complex, and therefore have low yield (a strong function of device area and number of steps). The duration of the overall process is fairly long, and the generic difficulties of monolithic integration of electronics with MEMS remain the same [42]–[44]. Unless the devices are very small (which is not the case for most ultrasonic transducer arrays), the cost of monolithic integration is not justified by the performance improvement. Flip-chip bonding of MEMS devices on electronics combines the performance advantages of monolithic integration with the flexibility of hybrid integration in the design and fabrication of MEMS devices and their electronics [45], [46]. Our approach to electronic integration is based on flip-chip bonding of cMUT arrays to the electronics chips, in combination with electrical throughwafer interconnects that bring the electrical connections of cMUT elements to the back side of the silicon wafer. The front side of the silicon wafer is populated with the cMUT elements; the back side of the silicon wafer has the corresponding signal and ground pads. The cMUT chip is flip-chip bonded onto a physically matching electronics array. The electrical through-wafer interconnect process is capable of producing low-capacitance ($\sim 0.05 \text{ pF}$) and lowresistance ($\sim 20 \Omega$) electrical connections from the back side to the front side of the silicon wafer [47]. In this way, the integration between the electronics and the transducer

array is established efficiently and without any significant parasitics. The flip-chip bonding integration allows us to independently fabricate the cMUT arrays and the electronics, gaining full flexibility in both processes. In addition, because neither of the processes is as complex as monolithic integration, the yield increases and the fabrication turn-around time shortens significantly. These advantages come at the expense of additional fabrication steps to generate the electrical through-wafer interconnects.

IV. TWO-DIMENSIONAL ARRAYS AND ELECTRICAL THROUGH-WAFER INTERCONNECTS

In two-dimensional array fabrication, before the actual cMUTs are fabricated, electrical through-wafer interconnects are preprocessed onto the silicon substrate. There are three elements of through-wafer interconnects: the front side pads on which the cMUT membranes are built, the through-wafer vias filled with conductive material, and the back-side pads used to connect to the electronics. The process starts with etching 20:1 aspect ratio holes through the silicon substrate, followed by thermal oxidation to isolate the silicon substrate from the vias and pads. Next, LPCVD poly-silicon deposition and doping create a conductive path through the via, and additional poly-silicon depositions fill in the vias. Excess poly-silicon on the front and back side surfaces is etched back, and the conductive poly-silicon layers on the front and back are patterned in the form of front and back side pads to create the electrical through-wafer interconnect structure (Fig. 3). The regular cMUT structures now can be processed on this wafer. Fig. 4 shows an optical picture of an array element from a 128×128 element two-dimensional array. This process, developed at Stanford University, is capable of producing high-density, high-yield, low parasitic capacitance interconnects [35], [47]–[51].

The pads and the vias described in the process flow have metal-insulator-semiconductor (MIS) junction relation with the silicon substrate. In variations of this process, the MIS relation is replaced with a PN junction relation, in order to reverse-bias the PN junction, create a large depletion region, and reduce the parasitic capacitance to negligible levels [47]. However, silicon wafer foundries are now capable of producing very high resistivity (> 20,000 $\Omega \cdot \text{cm}$) float zone wafers. When such high-resistivity wafers are used, the depletion width achieved with reverse-biased MIS junctions is sufficient to obtain very low-parasitic capacitance; electrical through-wafer interconnects in PN junction relation with the silicon substrate are no longer necessary.

The through-wafer via process consists of standard oxidation, LPCVD poly-silicon depositions, and dry etch steps. The through-wafer vias and the front and back-side pads all can be defined using only five masks. Thus, the electrical through-wafer interconnect process is a simple and well-developed process, and when combined with flip-



Fig. 3. Schematic of a two-dimensional array element showing the front side, populated with membranes, the backside pad for flip-chip bonding, and the conductive through-wafer via.

chip bonding, provides efficient and low-parasitic integration of the transducer arrays with the electronics. The first examples of such an integration have been reported in [52] with volumetric imaging results soon to be published.

V. CMUT FABRICATION WITH WAFER-BONDING METHOD

Wafer-bonding, considered as a bulk process, is widely used in micromachining, and it is older than surface micromachining techniques. There are three basic wafer-bonding techniques: anodic bonding, fusion bonding, and adhesive bonding. Although the physics behind each of these techniques is different, the purpose and outcome are the same: the permanent bonding of two similar or two different substrates.

Silicon fusion bonding has earned a stable position in today's technology, and it is now used for various applications: bond-and-etchback silicon-on-insulator (SOI) wafers, SMART-CUTTM SOI wafers (SOITEC, Bernin, France) [53], power devices, and many silicon microstructures such as pressure sensors and accelerometers [54]–[56]. Silicon fusion bonding is a direct bond between two silicon surfaces that takes place at high temperatures, forming strong covalent bonds between the silicon wafers. The bond is hermetic, and exceptionally stable both mechanically and electrically [55]. Measurements and observations indicate that the yield strength of the bond is close to the



400 µm

Fig. 4. An optical picture of a two-dimensional array element from the top. The small circle is the through-wafer via that connects the front-side pad to the back-side pad.

yield strength of single-crystal silicon [54]. This level of stability is crucial for extreme applications such as highpressure and high-temperature sensing environments. The bond is equally stable, even when one of the wafers is thermally oxidized.

Today, there are successful commercial MEMS products based on surface micromachining. Integrated accelerometers [57], pressure sensors [58], and microphones [59] are examples for miniature sensors. Grating light values [60] and digital micromirror devices [61] are examples of large actuator arrays that have digital control over the path of the light. Analog control over the path and intensity of light with very good reliability (analog control requires very tight reliability specifications) also has been demonstrated recently by Silicon Light Machines [62]. When compared to these examples, because of the relatively larger size of the transducer arrays in most cases, and very high electric field strengths involved in cMUT operation, there are tighter constraints on the yield and uniformity of the cMUT processes. In addition, the sensitivity and the frequency response of cMUTs are determined by the physical dimensions and material properties. Therefore, precise process control is crucial for cMUT fabrication. Silicon fusion bonding has been shown to have important advantages over surface micromachining techniques in making pressure sensors [55]. Along with stability, wafer-bonding allows easier fabrication of complex structures (e.g., membranes) from single crystal silicon, a material that has been extensively studied as a mechanical material and is very well characterized [63]. Its mechanical and electrical properties are consistent on a wafer, from wafer to wafer, and over time—important characteristics that are more difficult to achieve with surface micromachining. Although surface micromachining has been very successful for fabricating cMUTs (and many MEMS products), a cMUT process line may further benefit from the advantages of silicon fusion bonding.

The fabrication of cMUTs using the wafer-bonding technique begins with two wafers: a prime quality silicon wafer and a SOI wafer. In its simplest form, the waferbonded cMUT process can be summarized as follows: the cavity is defined on the prime wafer and fusion-bonded to the active side of the SOI wafer. The handle portion and the buried oxide layer of the SOI wafer are later removed, leaving a silicon membrane stretched over the cavities. The following sections describe this fabrication process in detail and discuss advantages, issues of concern, and possible variations.

A. Cavity Definition

The membrane size and the gap height are delineated in the cavity definition step. The prime quality silicon wafer is thermally oxidized to a predetermined thickness, followed by a photolithography step to define the cavity shape. The thermally grown silicon dioxide layer is etched with hydrofluoric acid solution (or dry etched) through the photoresist pattern all the way to the silicon, as shown in Fig. 5(a). After the photoresist is removed, another layer of silicon dioxide is thermally grown [Fig. 5(b)]. Because the membrane is silicon, which is not an insulator, the second oxidation isolates the conductive silicon substrate from the top electrode to avoid shorting.

B. Membrane Formation

Following the second oxidation, the SOI wafer and the prime wafer (after being RCA-cleaned and surface-activated) are brought together in vacuum, as shown in Fig. 5(c). As soon as the two wafers come in close contact, short-range van der Waals forces attract the two wafers and weak hydrogen bonds develop between them. The wafers are immediately annealed/oxidized at 1100°C to form strong covalent bonds.

After bonding and annealing, the handle of the SOI wafer (including the buried oxide layer) is removed to release the membranes [Fig. 5(d)], either by wet etching or dry etching. Wet etching of silicon, a well-known process, can be done with a solution of either KOH or tetra-methylammonium-hydroxide (TMAH). It is critical to ensure that the silicon dioxide layer on the back of the prime wafer holds off the wet etchant during this step. A better method is to grind/polish the handle portion of the SOI wafer down to $\sim 50 \ \mu m$ before the wet etch step, which relaxes the constraint on the thickness of the silicon dioxide layer on the back of the prime wafer. Because both KOH and TMAH have very slow etch rates for silicon dioxide, once the silicon etch is complete, the wet etch process will practically stop at the buried oxide (BOX) laver. The BOX laver then can be removed with hydrofluoric acid, which stops at the silicon membrane. If the handle wafer is dry etched with deep reactive ion etching (DRIE), the BOX layer serves as the etch-stop layer. Using recently developed DRIE equipment, this etch step may be 25 times faster than wet etch,



Fig. 5. Wafer-bonding technique for fabricating cMUTs. (a) First thermal oxidation step and cavity definition with photolithography and etch. (b) Second thermal oxidation to create the insulation layer. (c) Silicon direct bonding of the patterned prime wafer to the unpatterned SOI wafer. (d) Removal of the handle and the BOX layer of the SOI wafer to release the membranes. (e) Ground contact definition, top electrode deposition, and patterning. (f) Element definition by photolithography and silicon etch.

eliminating concerns about the serial nature (one wafer at a time) of the DRIE process.

C. Electrical Connections and Element Definition

The remaining steps of the wafer-bonded cMUT process are very similar to the surface micromachined cMUT process, with the exception of element definition. Openings through the silicon and silicon dioxide layers are defined with photolithography and dry etch steps to access the bottom silicon layer and make the ground connection. The top electrode is sputtered then patterned by another photolithography and wet etch step [Fig. 5(e)]. Because there is no surface topology in the wafer-bonded cMUTs at this step to cause discontinuity, the top electrode can also be evaporated.

The elements are defined by etching isolating trenches, as shown in Fig. 5(f). Because the active silicon layer is not a good insulator, it must be etched all the way to the oxide layer to electrically isolate the elements. The trenches are defined with photolithography, and then dry etched into the silicon.

VI. DISCUSSION ON THE WAFER-BONDED CMUT PROCESS

The wafer-bonded cMUT process (as evident from the above description) substantially reduces the complexity of cMUT fabrication. The number of essential masks is reduced from six to four, and the five deposition steps are replaced by two oxidation steps. Consequently, processing time is reduced substantially. The wafer-bonding technique also adds many design flexibilities that improve device efficiency. Because the cavity and the membrane are defined on separate wafers, it is possible to optimize both of them at the same time. There are no wet-release processes to limit the size of the membranes that can be fabricated, virtually eliminating any limit on the low frequency end. All of these advantages come with expensive SOI wafers (\approx \$250 per 100 mm wafer), the cost of which is still a small fraction of the total process cost of a wafer [64]. Then, the reduced number of steps and complexity justify the use of expensive SOI wafers in cMUT fabrication. The following sections describe examples that show the capabilities of the wafer-bonding technique, some of which are not possible with the sacrificial release process.

A. Cavity Definition, Cavity Height Control, and Uniformity

Thermal oxidation, a well-understood, well-characterized, and well-controlled process used extensively in very large scale integrated (VLSI) circuits processes, determines the cavity depth. The thickness of the thermally grown silicon dioxide is precise, as is the on-wafer and waferto-wafer thickness uniformity. Such accuracy allows excellent control over the cavity height and the insulation layer thickness. In dry thermal oxidation, typical on-wafer and wafer-to-wafer thickness uniformities are better than 1%, for which uniformity is defined as the ratio of the standard deviation to the mean of the thickness measurements. On average, the on-wafer uniformity is 0.64% (measured over 20 100-mm wafers in five separate runs), and the wafer-to-wafer uniformity is 0.81% (measured over a total of 46 100-mm wafers in 11 runs). For wet oxidation, the on-wafer uniformity is 1.07% (measured over 18 wafers in four separate runs), and wafer-to-wafer uniformity is 0.53% (measured over a total of 30 wafers in five runs). Moreover, the thickness control (defined as the ratio of the difference between measured and target thickness to the target thickness) is measured as low as 0.6%.

B. Wafer-Bonding, Membrane Thickness Control, and Uniformity

The direct bonding of the prime wafer (on which the cavity is defined) and the SOI wafer is the most critical step. Both wafers must be ultra-clean, free from particles, and ultra-smooth. The number of bonds—and therefore the strength of the bond—depends on the smoothness (inverse of surface roughness) of the wafers. It is estimated that the root mean square micro-roughness must be less than ~ 5 Å [53] for wafer-bonding to occur—an objective readily achieved by prime quality silicon and SOI wafers. As quoted by [54], the yield strength of bonded wafers is close to that of single crystal silicon, which assures the quality of the bond. The quality of the wafer bonding also depends on surface flatness. Both surface roughness and flatness define the surface profile. Roughness refers to microscopic variations (high spatial frequency variations); flatness refers to macroscopic (low spatial frequency) variations. Because of the elasticity of the wafer, the requirement for surface flatness is looser than the requirement for smoothness. Nonuniformity in the macroscopic flatness of the wafers results in macroscopic gaps between the two wafers. Under the right conditions, the wafers go through elastic deformation to make conformal contact, and eventually bond.

Because the membranes are made from the active silicon layer of the SOI wafer, the membrane thickness and thickness uniformity are determined by the SOI wafer. For SMART-CUTTM thin SOI wafers (< 1.5 μ m active silicon thickness), the thickness variation is less than 10 nm for 100-mm wafers. In addition, the membrane is single crystal silicon, which has well-known mechanical and electrical properties with no residual stress. Consequently, the control over the membrane thickness and its mechanical properties, as well as the on-wafer and wafer-to-wafer thickness uniformity, is excellent in comparison to any of the deposited membranes. Fig. 6(a) shows the resonance frequency at a fixed bias voltage and Fig. 6(b) shows capacitance variation over 76 elements in a one-dimensional array measured at 12 V. The array elements are 585 μ m by 4.7 mm in size. Each element consists of 288 square membranes, which are 84 μ m on the side. The membrane thick-



Fig. 6. The variation in the (a) resonance frequency and (b) capacitance of a one-dimensional array over 76 elements.

ness is 1 μ m, the gap height is 1 μ m before atmospheric deflection, and the insulation layer thickness is 0.15 μ m. The uniformity of the resonance frequency over 76 elements is 0.65%, including the variations in the mechanical resonance frequency, the parasitic capacitance, and the electromechanical transformation ratio at the bias voltage. The uniformity of the device capacitance over 76 elements is 2.6%, which, in effect, includes all the geometrical variations and the parasitic capacitance variation of the test setup (which is actually the dominant factor). This uniformity is approximately twice as good as previously reported results for surface micromachined cMUTs [27]. In contrast to surface micromachined cMUTs, the uniformity of wafer-



Fig. 7. Electrical model of a silicon membrane with (a) full top electrode coverage and (b) partial top electrode coverage.

bonded cMUTs is readily achieved without extra effort; [5] offers more data on process control issues.

C. Effect of the Resistivity of the Silicon Membrane

In all cMUT fabrication processes (with the exception of the wafer-bonding method), the membrane is either an insulating material, such as Si_3N_4 , or a conductive material, such as doped poly-silicon. The electrical properties of the membrane material have a significant impact on the cMUT's operation. The electrical equivalent of the membrane (not the electromechanical model) is shown in Fig. 7(a). When the membrane is insulating— R_{mem} is infinite and the membrane is a capacitor (C_{mem}) in series with the active gap capacitance (C_{gap}) —the applied alternating current (AC) voltage is divided among the membrane, the gap, and the insulating layer. Keeping a minimum insulation layer and embedding the top electrode inside the membrane as described in Section III-F, minimize the loss. However, an insulating membrane allows the patterning of the top electrode to optimize the trade-off between parasitic capacitance and transduction efficiency [31]. When the membrane is conductive—the membrane reduces to a small resistor in series with the active gap capacitancethere is no voltage drop across the membrane. However, unless the membrane is selectively made conductive, the top electrode cannot be patterned.

In the wafer-bonding method, the membrane is composed of single crystal silicon, which is really a semiconductor. Unless heavily doped, it is neither an insulator nor a conductor. Electrically, it corresponds to the case in which R_{mem} is comparable to the impedance of C_{mem} at the frequencies of interest, and the composite effect of R_{mem} and C_{mem} must be calculated. In the simple case of a square membrane with a 24 μ m side length (where for simplicity, the posts are not included and the top electrode is assumed to cover the whole membrane), the resistance of the membrane is:

$$R_{mem} = \frac{\rho t}{A},\tag{1}$$

where ρ is the resistivity, t is the thickness, and A is the area of the membrane. The capacitance of the membrane is:

$$C_{mem} = \frac{A\epsilon_0\epsilon_r}{t},\tag{2}$$

where $\epsilon_0 = 8.854 \times 10^{-12}$ F/m is the permittivity of free space and $\epsilon_r = 11.7$ is the relative dielectric constant of silicon. The critical frequency f_c , at which R_{mem} is equal to the impedance of C_{mem} , is:

$$f_c = \frac{1}{2\pi\rho\epsilon_0\epsilon_r},\tag{3}$$

where the resistivity of the silicon membrane, ρ , is the determining parameter. For high-resistivity silicon membranes (~2000 $\Omega \cdot cm$), the critical frequency occurs at 76.8 MHz. For typical cMUT applications, the silicon membrane should be considered as a conductor (i.e., drop C_{mem} from the electrical model). In usual cMUT designs, because the gap capacitance is smaller than the membrane capacitance and much smaller than the insulation layer capacitance, it becomes the dominant capacitance. Thus, the time constant resulting from the series combination of the membrane (R_{mem}) and the gap capacitance (C_{gap}) is even higher than we had calculated for the membrane. For the membrane parameters listed above, the frequency at which the resistance of the membrane is equal to the impedance of the gap capacitance is ~ 135 MHz. Below this frequency. the membrane resistance is negligible compared to the reactance of the gap. The membrane behaves like a conductor at the frequencies of interest, which puts it in the class of conductive membranes. Although the top electrode is deposited on top of the membrane, it effectively appears to be on the bottom of the membrane.

When the top electrode is patterned, however, the electrical behavior of the membrane becomes more complex, and the model must include the lateral resistance of the membrane (R_S) , shown in Fig. 7(b). Because the membrane is thin, the path from the top electrode to the periphery of the membrane is a high-resistance path; at some distance away from the center, the resistance, R_S , dominates the gap capacitance. The electrode is effectively larger than the actual metal pattern by a percentage that is a function of both the resistivity and the frequency of the membrane. In the above example of patterned top electrode, shown in Fig. 8(a), the active membrane is 20 μ m on the side that includes the supporting posts. The electrical behavior of the membrane is quantified by solving the problem numerically, using an electromagnetic field solver. For the above example and for several other scenarios, the



Fig. 8. (a) The schematic cross section of a square membrane, 20 μ m on the side, supported with a post width of 2 μ m on all sides. (b) EM simulation results for various scenarios of membrane resistivity and electrode location. The membrane thickness is 1 μ m, the gap height is 0.2 μ m, and the silicon dioxide insulation layer thickness is 0.15 μ m.

results of the simulations carried out with the EM simulator of Sonnet Software Inc. (Syracuse, NY) are shown in Fig. 8(b). When the membrane is highly conductive, the top electrode appears at the bottom of the membrane and covers it fully, resulting in the highest capacitance. When the membrane is insulating, the capacitance of the membrane is strictly defined by the electrode pattern, resulting in the lowest capacitance. When the membrane is resistive (as in our case), the capacitance versus frequency curve shows a transition between the two extremes, from a conductive membrane at low frequencies to an insulating membrane at high frequencies [solid line in Fig. 8(b)].

Measurements verify the above-mentioned behavior. Fig. 9 compares the measured capacitance of a unit cell to simulation results, for which the unit cell is a hexagon with an inscribed diameter of 24 μ m and a post width of 2 μ m. For the two simulation cases, the membrane thickness is 1 μ m, gap height is 0.2 μ m, the insulation thickness is 0.3 μ m, and the resistivity of the silicon membrane is 2000 Ω ·cm and 20,000 Ω ·cm. All three plots share two distinctive features that agree very well: the increase in the capacitance at low frequencies, and the asymptotic behav-



Fig. 9. Capacitance of a hexagonal membrane with 20 μ m inscribed diameter and 2 μ m post width, comparing the EM simulation results to measurement results. The membrane thickness is 1 μ m, the gap height is 0.2 μ m, the silicon dioxide insulator thickness is 0.3 μ m, and the silicon membrane resistivity is 2000 Ω ·cm.

ior at high frequencies. When compared to the simulation results, measurements indicate that the resistivity of the membrane is greater than 2000 Ω ·cm, probably closer to 20,000 Ω ·cm.

In conclusion, when the membrane is silicon, its electronic properties affect its behavior and complicate the analysis and design of cMUTs. The simulation and measurement results show that there is a frequency range at which the top electrode is effectively at the bottom of the membrane and patterned—the ideal case for cMUT operation. One remaining issue is the lack of accurate control over the resistivity of the silicon membrane. At low frequencies (around and less than 1 MHz), control is not an issue because the membrane behaves conductively even with highly resistive silicon. Nor is the resistivity of silicon an issue at high frequencies (around and above 5 MHz), as shown by simulations and measurements. However, for the frequency range between low and high ends, extra care is required in choosing the starting materials and in designing the cMUTs.

D. Dielectric Breakdown and Charging

In wafer-bonded cMUTs, the membrane and the substrate are separated by a layer of thermally grown silicon dioxide, which isolates the top electrode from the bottom electrode electrically. Both the thickness of the post that supports the membranes and the thickness of the insulation layer in the cavity must accommodate the highest voltage of operation. The nominal value for the intrinsic dielectric breakdown of silicon dioxide is 1200 V/ μ m, with a variation of ± 200 V/ μ m. The breakdown voltage of silicon dioxide normally depends on area as well (because of the weak point concentration) and can be as low as 600 V/ μ m. Because of major defects such as pinholes in

10 1 element 2 elements 10 3 elements 4 elements 10 10 Current (A) 10 10 10 10 10 20 60 200 0 40 80 100 120 140 160 180 Voltage (V)

Fig. 10. I-V curve of 0.15 μ m thick thermally grown silicon dioxide showing the dielectric breakdown. The measurement is done over four devices with different areas.

the growth process, there is also extrinsic breakdown at very low electric fields (100–200 V/ μ m). The quality of the silicon dioxide film, which depends largely on growth conditions and contamination levels, is measured by the narrowness of breakdown field distribution over a large area. Fig. 10 shows the results of breakdown voltage measurements over varying areas for thermally grown silicon dioxide. The measurement is done on the elements of a one-dimensional array, whose dimensions are given in Section VI-B. Measurement over four elements equals a measurement over an area of 2.34 mm by 4.68 mm. In this experiment, all membranes are collapsed, so that only the breakdown voltage of the 0.15 μ m thick insulation layer is measured. The I-V plot shows that the breakdown occurs consistently at 130 V, which corresponds to a breakdown field of 870 V/ μ m.

Silicon dioxide has a slightly higher breakdown field than Si₃N₄. Because it is thermally grown, silicon dioxide usually has fewer defects to cause extrinsic breakdown, and fewer weak points to widen the breakdown field distribution. In that sense, silicon dioxide is a better insulator. However, dielectric charging remains a major issue for silicon dioxide. The silicon dioxide surface easily traps slow charges, which do not respond to the AC signals used in cMUT operation, and therefore do not contribute to the capacitance. However, these charges may drift the direct current (DC) operating point in time. The cross-sectional view of a membrane, shown in Fig. 8, can be divided into two regions: the post region where the silicon dioxide layer has silicon interface on both sides, and the cavity where the silicon dioxide has silicon on one side and a vacuum on the other. Because the charges trapped in the postregion do not apply any force on the membrane, they do not affect the operating point. In the cavity, however, the charges trapped in the insulation layer alter both the electric field in the gap and the static force on the membrane, thus changing the operating point. The effect of

charge-trapping can be minimized by patterning the insulation layer in the cavity (easily possible with the waferbonding technique) to minimize the silicon dioxide area, while keeping silicon dioxide posts in certain locations to avoid shorting. The silicon dioxide in the cavity can be patterned in various shapes and sizes. To verify the concept, we used nine silicon dioxide posts, 0.3 μ m thick and 3 μ m in size, which covered only 1.2% of the total cavity area. The effect of charging is determined by measuring the capacitance-voltage (C-V) curve of the cMUT over several voltage sweep cycles; the shift in the C-V curve is compared to the control case, in which the insulation layer in the cavity is not patterned. In the control case, a voltage shift of ~ 35 V was observed in the C-V curve after several biasing and pulsing cycles; for the device with insulation posts there was no shift in the C-V curve [65].

E. Fill Factor and Parasitic Capacitance

In contrast to sacrificial-release processes, the waferbonding method has no wet-release step. Because of the absence of stress in the silicon membrane, together with the absence of a wet-release process, the wafer-bonding method has the unique capability to fabricate large membranes with a sealed cavity. The frequency range of cMUTs is thereby extended to 10 kHz on the low frequency side [66]. Wafer-bonded cMUTs have a distinctive advantage on the higher side of the frequency range as well: because they do not require etch holes and channels, the active area can be used very efficiently by leaving only 2 μ (or less) of post region between membranes.

The active area use, also called the fill factor, has significant implications on cMUT performance. It directly scales the output pressure and receive sensitivity, affects the acoustical load seen by the transducer (low fill factor implies narrower bandwidth), and determines the acoustical reflection coefficient of the cMUT on receive. The parasitic capacitance of a cMUT refers to the capacitance that does not contribute to the acoustical output. Although parasitic capacitance usually is not a problem on transmit, it adversely affects the signal-to-noise ratio on receive. Increasing the fill factor, by definition, reduces the parasitic capacitance while increasing the active capacitance. In summary, the fill factor has a threefold effect on overall device efficiency: increased output pressure and receive sensitivity because of area gain, and increased signal-tonoise ratio because of reduced parasitic capacitance.

Wafer-bonded cMUTs have other features that contribute to the fill factor, including the ability to fabricate high-aspect ratio rectangular membranes. Rectangular membranes increase both the fill factor and the average displacement over the membrane, compared to circular or hexagonal membranes. Recent work [67] revealed that rectangular membranes are superior to square membranes in both transmit efficiency and receive sensitivity by 46% and 43%, respectively. Using the wafer-bonded cMUT process, the membrane also can be fabricated with a mass in the middle for more piston-like movement, which creates





Fig. 11. Cross-sectional view of a cMUT membrane with a silicon mass at the center of the membrane.

higher average displacement over the membrane and less parasitic capacitance. The mass at the center of the membrane in this process also is made of single crystal silicon and is self-aligned to the cavity (Fig. 11).

VII. CONCLUSIONS

Capacitive micromachined ultrasonic transducers have been an attractive alternative to piezoelectric transducers for some time, showing performance benefits such as impedance match in air and low-pressure applications, wide frequency bandwidth in immersion applications [27], and higher coupling efficiency [68]. A major handicap for cMUTs has been the low output pressure capability of cMUTs in their normal mode of operation in immersion applications. Substantial research has been conducted to increase output pressure capability by operating cMUTs in different modes, has produced very promising results [69], [70]. The cMUTs also offer significant technological benefits. By using micromachining techniques, derived from integrated circuit technologies, cMUTs benefit from batch fabrication capability and scalability, the two factors that drove down the cost of integrated circuit fabrication. The most important technological benefit of cMUT technology is the electronic integration possibilities it offers, monolithic integration and integration with flip-chip bonding. Between the two, flip-chip bonding best combines performance with flexibility and yield.

In this paper, we also reviewed and qualitatively compared the two main cMUT fabrication techniques: the more traditional sacrificial-release processes and the waferbonding technique. The sacrificial-release processes, based on the method of depositing a sacrificial layer and removing it after the membrane deposition (described in Section I), vary with the materials and deposition techniques used. In comparing materials, tools, and methods used to fabricate cMUTs, we found the sacrificial processes to be more or less equal, with no definite winner. Because both the material science and semiconductor tools industries are evolving rapidly, new materials, tools, and methods may change today's conclusions. However, we can draw conclusions about fundamental principles. The recently introduced, wafer-bonded cMUT process uses a totally different fabrication approach from the sacrificial-release processes. Wafer-bonding simplifies the process, reduces the number of steps and the turn-around time, eliminates problems with membrane release processes, high stress, and porous films, and increases the yield, uniformity, and process control. Because of design and manufacturing flexibility, wafer-bonded cMUT technology is open to further improvement, and presents a clear, simple, reliable technology for cMUT fabrication.

References

- M. Rafiq and C. Wykes, "The performance of capacitive ultrasonic transducers using v-grooved backplates," *Meas. Sci. Tech*nol., vol. 2, pp. 168–174, 1991.
- [2] K. Suzuki, K. Higuchi, and H. Tanigawa, "A silicon electrostatic ultrasonic transducer," *IEEE Trans. Ultrason., Ferroelect., Freq. Contr.*, vol. 36, no. 6, pp. 620–627, 1989.
- [3] D. W. Schindel, D. A. Hutchins, L. Zou, and M. Sayer, "The design and characterization of micromachined air-coupled capacitance transducers," *IEEE Trans. Ultrason.*, *Ferroelect.*, *Freq. Contr.*, vol. 42, pp. 42–50, 1995.
- [4] M. I. Haller and B. T. Khuri-Yakub, "A surface micromachined electrostatic ultrasonic air transducer," in *Proc. IEEE Ultrason.* Symp., 1994, pp. 1241–1244.
- [5] Y. Huang, A. S. Ergun, E. Hægström, M. H. Badi, and B. T. Khuri-Yakub, "Fabricating capacitive micromachined ultrasonic transducers with wafer-bonding technology," *J. Microelectromech. Syst.*, vol. 12, pp. 128–137, Apr. 2003.
- [6] H. Seidel, L. Csepregi, A. Heuberger, and H. Baumgärtel, "Anisotropic etching of crystalline silicon in alkaline solutions," J. Electrochem. Soc., vol. 13, no. 11, pp. 3612–3625, 1990.
- [7] J. J. Blech, "On isothermal squeeze films," J. Lubrication Technol., vol. 105, pp. 615–621, 1983.
- [8] M. Andrews, I. Harris, and G. Turner, "A comparison of squeezefilm theory with measurements on a microstructure," Sens. Actuators A, vol. 36, pp. 79–87, 1993.
- [9] J. G. Knight and F. L. Değertekin, "Fabrication and characterization of cMUTs for forward looking intravascular ultrasound imaging," in *Proc. IEEE Ultrason. Symp.*, 2003, pp. 1175–1178.
- [10] S. T. Hansen, A. S. Ergun, W. Liou, B. A. Auld, and B. T. Khuri-Yakub, "Wideband micromachined capacitive microphones with radio frequency detection," *J. Acoust. Soc. Amer.*, vol. 116, pp. 828–842, Aug. 2004.
- [11] P. Eccardt, K. Niederer, T. Scheiter, and C. Hierold, "Surface micromachined ultrasound transducers in CMOS technology," in *Proc. IEEE Ultrason. Symp.*, 1996, pp. 959–962.
- [12] O. Ahrens, D. Hohlfeld, A. Buhrdorf, O. Glitza, and J. Binder, "A new class of capacitive micromachined ultrasonic transducers," in *Proc. IEEE Ultrason. Symp.*, 2000, pp. 939–942.
- [13] R. A. Noble, R. J. Bozeat, T. J. Robertson, D. R. Billson, and D. A. Hutchins, "Novel silicon nitride micromachined wide bandwidth ultrasonic transducers," in *Proc. IEEE Ultrason. Symp.*, 1998, pp. 1081–1084.
- [14] C. H. Mastrangelo and C. H. Hsu, "Mechanical stability and adhesion of microstructures under capillary forces–Part I: Basic theory," J. Microelectromech. Syst., vol. 2, pp. 33–43, Mar. 1993.
- [15] C. H. Mastrangelo and C. H. Hsu, "Mechanical stability and adhesion of microstructures under capillary forces–Part II: Experiments," J. Microelectromech. Syst., vol. 2, pp. 44–55, Mar. 1993.
- [16] N. Tas, T. Sonnenberg, H. Jansen, R. Legtenberg, and M. Elwenspoek, "Sticktion in surface micromachining," J. Micromech. Microeng., vol. 6, pp. 385–397, 1996.
- [17] R. Maboudian and R. T. Howe, "Critical review: Adhesion in surface micromechanical structures," J. Vac. Sci. Technol. B, vol. 15, no. 1, pp. 1–20, 1997.
- [18] H. Guckel, J. J. Sniegowski, T. R. Christenson, S. Mohney, and T. F. Kelly, "Fabrication of micromechanical devices from polysilicon films with smooth surfaces," *Sens. Actuators*, vol. 20, pp. 117–122, 1989.

- [19] G. T. Mulhern, D. S. Soane, and R. T. Howe, "Supercritical carbon dioxide drying of microstructures," in *Proc. 7th Int. Conf. Solid-State Sens. Actuators*, 1993, pp. 296–299.
- [20] J. H. Lee, H. H. Chung, S. Y. Kang, J. T. Baek, and H. J. Yoo, "Fabrication of surface micromachined polysilicon actuators using dry release process of hf gas-phase etching," in *Proc. Electron Devices Meeting*, 1996, pp. 761–764.
- [21] T. Hirano, T. Furuhata, and H. Fujita, "Dry releasing of electroplated rotational and overhanging structures," in *Proc. MEMS IEEE*, 1993, pp. 278–283.
- [22] R. Fritschi, C. Dehollain, M. J. Declercq, A. M. Ionescu, C. Hibert, P. Fluckiger, and P. Renaud, "A novel rf mems technological platform," in *Proc. 28th Annu. Conf. IEEE Indust. Electron. Soc.*, 2002, pp. 3052–3056.
- [23] X. C. Jin, I. Ladabaum, F. L. Değertekin, S. Calmes, and B. T. Khuri-Yakub, "Fabrication and characterization of surface micromachined capacitive ultrasonic immersion transducers," J. Microelectromech. Syst., vol. 8, pp. 100–114, 1999.
- [24] G. Caliano, F. Galanello, A. Caronti, R. Carotenuto, M. Pappalardo, V. Foglietti, and N. Lamberti, "Micromachined ultrasonic transducers using silicon nitride membrane fabricated in PECVD technology," in *Proc. IEEE Ultrason. Symp.*, 2000, pp. 963–968.
- [25] R. A. Noble, A. D. R. Jones, T. J. Robertson, D. A. Hutchins, and D. R. Billson, "Novel, wide bandwidth, micromachined ultrasonic transducers," *IEEE Trans. Ultrason., Ferroelect., Freq. Contr.*, vol. 48, pp. 1495–1507, Nov. 2001.
- [26] D. Memmi, V. Foglietti, E. Cianci, G. Caliano, and M. Pappalardo, "Fabrication of capacitive micromechanical ultrasonic transducers by low-temperature process," *Sens. Actuators A*, vol. 99, pp. 85–91, 2002.
- [27] Ö. Oralkan, A. S. Ergun, J. A. Johnson, M. Karaman, U. Demirci, K. Kaviani, T. H. Lee, and B. T. Khuri-Yakub, "Capacitive micromachined ultrasonic immersion transducers: Next-generation arrays for acoustic imaging?," *IEEE Trans. Ultrason., Ferroelect., Freq. Contr.*, vol. 49, pp. 1596–1610, Nov. 2002.
- [28] X. C. Jin, I. Ladabaum, and B. T. Khuri-Yakub, "The microfabrication of capacitive ultrasonic transducers," J. Microelectromech. Syst., vol. 7, pp. 295–302, 1998.
- [29] X. C. Jin, "Micromachined capacitive ultrasonic immersion transducer array," Ph.D. dissertation, Stanford University, Stanford, CA, Jan. 2002.
- [30] I. Ladabaum, X. C. Jin, H. T. Soh, A. Atalar, and B. T. Khuri-Yakub, "Surface micromachined capacitive ultrasonic transducers," *IEEE Trans. Ultrason., Ferroelect., Freq. Contr.*, vol. 45, pp. 678–690, 1998.
- [31] A. Bozkurt, I. Ladabaum, A. Atalar, and B. T. Khuri-Yakub, "Theory and analysis of electrode size optimization for capacitive microfabricated ultrasonic transducers," *IEEE Trans. Ultrason., Ferroelect., Freq. Contr.*, vol. 46, pp. 1364–1374, 1999.
- [32] B. Bayram, G. G. Yaralioglu, A. S. Ergun, and B. T. Khuri-Yakub, "Influence of the electrode size and location on the performance of a cMUT," in *Proc. IEEE Ultrason. Symp.*, 2001, pp. 949–952.
- [33] I. Ladabaum, B. T. Khuri-Yakub, and D. Spoliansky, "Micromachined ultrasonic transducers: 11.4 MHz transmission in air and more," *Appl. Phys. Lett.*, vol. 68, pp. 7–9, 1996.
- [34] H. T. Soh, I. Ladabaum, A. Atalar, C. F. Quate, and B. T. Khuri-Yakub, "Silicon micromachined ultrasonic immersion transducers," *Appl. Phys. Lett.*, vol. 69, pp. 3674–3676, 1996.
- [35] Ö. Oralkan, A. S. Ergun, C.-H. Cheng, J. A. Johnson, M. Karaman, T. H. Lee, and B. T. Khuri-Yakub, "Volumetric ultrasound imaging using 2-D cMUT arrays," *IEEE Trans. Ultrason., Ferroelect., Freq. Contr.*, vol. 50, pp. 1581–1594, Nov. 2003.
- [36] M. Orpana and A. O. Korhonen, "Control of residual stress of polysilicon films by heavy doping in surface micromachining," in *Proc. IEEE Transducers*, 1991, pp. 957–960.
- [37] R. T. Howe and R. S. Muller, "Stress in polycrystalline and amorphous silicon thin films," J. Appl. Phys., vol. 54, no. 8, pp. 4674–4675, 1983.
- [38] H. Guckel, D. W. Burns, C. C. G. Visser, H. A. C. Tilmans, and D. Deroo, "Fine-grained polysilicon films with built-in tensile strain," *IEEE Trans. Electron. Devices*, vol. 35, pp. 800–801, June 1988.
- [39] R. A. Noble, R. R. Davies, M. M. Day, L. Koker, D. O. King, K. M. Brunson, A. R. D. Jones, J. S. McIntosh, D. A. Hutchins, T. J. Robertson, and P. Saul, "Cost-effective and manufac-

turable route to the fabrication of high-density 2D micromachined ultrasonic transducer arrays and (CMOS) signal conditioning electronics on the same silicon substrate," in *Proc. IEEE Ultrason. Symp.*, 2001, pp. 941–944.

- [40] R. A. Noble, R. R. Davies, D. O. King, M. M. Day, A. R. D. Jones, J. S. McIntosh, D. A. Hutchins, and P. Saul, "Low-temperature micromachined cMUTs with fully-integrated analogue front-end electronics," in *Proc. IEEE Ultrason. Symp.*, 2002, pp. 1045–1050.
- [41] C. Daft, S. Calmes, D. da Graca, K. Patel, P. Wagner, and I. Ladabaum, "Microfabricated ultrasonic transducers monolithically integrated with high voltage electronics," in *Proc. IEEE Ultrason. Symp.*, 2004, pp. 493–496.
- [42] J. M. Bustillo, R. T. Howe, and R. S. Muller, "Surface micromachining for microelectromechanical systems," *Proc. IEEE*, vol. 86, pp. 1552–1574, Aug. 1998.
- [43] M. B. Cohn, K. F. Böhringer, J. M. Noworolski, A. Singh, C. G. Keller, K. Y. Goldberg, and R. T. Howe, "Microassembly technologies for mems," in *Proc. SPIE Micromach. Microfab.*, vol. 3515, 1998, pp. 2–16.
- [44] U. Srinivasan, M. A. Helmbrecht, C. Rembe, R. S. Muller, and R. T. Howe, "Fluidic self-assembly of micromirrors onto microactuators using capillary forces," *IEEE J. Select. Topics Quantum Electron.*, vol. 8, no. 1, pp. 4–11, 2002.
- [45] K. W. Markus, V. Dhuler, D. Roberson, A. Cowen, M. Berry, and S. Nangalia, "Smart mems: Flip-chip integration of mems and electronics," in *Proc. SPIE Smart Materials Conf.*, 1995, pp. 82–92.
- [46] A. Singh, D. A. Horsley, A. P. Pisano, and R. T. Howe, "Batch transfer of microstructures using flip-chip solder bonding," *IEEE J. Microelectromech. Syst.*, vol. 8, no. 1, pp. 27–33, 1999.
- [47] C. H. Cheng, A. S. Ergun, and B. T. Khuri-Yakub, "Electrical through-wafer interconnects with 0.05 picofarads parasitic capacitance on 400 μm thick silicon substrate," in *Proc. Solid-State Sensor, Actuator and Microsystems Workshop*, 2002, pp. 157–160.
- [48] S. Calmes, C. Cheng, F. L. Değertekin, X. C. Jin, A. S. Ergun, and B. T. Khuri-Yakub, "Highly integrated 2-D capacitive micromachined ultrasonic transducers," in *Proc. IEEE Ultrason. Symp.*, 1999, pp. 1163–1166.
- [49] Ö. Oralkan, X. C. Jin, F. L. Değertekin, and B. T. Khuri-Yakub, "Simulation and experimental characterization of a 2-D, 3-MHz capacitive micromachined ultrasonic transducer (cMUT) array element," in *Proc. IEEE Ultrason. Symp.*, 1999, pp. 1141–1144.
- [50] C. H. Cheng, E. M. Chow, X. C. Jin, S. Ergun, and B. T. Khuri-Yakub, "An efficient electrical addressing method using throughwafer vias for two-dimensional ultrasonic arrays," in *Proc. IEEE Ultrason. Symp.*, 2000, pp. 1179–1182.
- [51] C. H. Cheng, A. S. Ergun, and B. T. Khuri-Yakub, "Electrical through silicon wafer interconnects for high frequency photodetector arrays," in *Proc. Photonic Devices and Systems Packaging*, 2002, pp. 54–57.
- [52] I. O. Wygant, D. T. Yeh, X. Zhuang, A. Nikoozadeh, Ö. Oralkan, A. S. Ergun, M. Karaman, and B. T. Khuri-Yakub, "A miniature real-time volumetric ultrasonic imaging system," in *Proc. SPIE*, *Medical Imaging*, vol. 5750, 2005, pp. 26–36.
- [53] S. S. Iyer and A. J. Auberton Hervé, Eds. Silicon Wafer Bonding Technology for VLSI and MEMS Applications. London: IN-SPEC, The Institution of Electrical Engineers, 2002.
- [54] P. W. Barth, "Silicon fusion bonding for fabrication of sensors, actuators and microstructures," *Sens. Actuators A*, vol. A21, pp. 919–926, 1990.
- [55] K. Petersen, J. Brown, T. Vermuelen, P. Barth, J. Mallon, Jr., and J. Bryzek, "Ultra-stable, high-temperature pressure sensors using silicon fusion bonding," *Sens. Actuators A*, vol. A21, pp. 96–101, 1990.
- [56] L. Christel, K. Petersen, P. Barth, F. Pourahmadi, J. Mallon, Jr., and J. Bryzek, "Single-crystal silicon pressure sensors with 500× overpressure protection," *Sens. Actuators A*, vol. A21–A23, pp. 84–88, 1990.
- [57] R. S. Payne, S. Sherman, S. Lewis, and R. T. Howe, "Surface micromachining: From vision to reality to vision," in *Proc. IEEE Int. Solid State Circuits Conf.*, 1995, pp. 164–165.
- [58] H. Dudaicevs, M. Kandler, Y. Manoli, W. Mokwa, and E. Spiegel, "Surface micromachined pressure sensors with integrated CMOS read-out electronics," *Sens. Actuators A*, vol. 43, pp. 157–163, 1994.

- [59] M. Pedersen, W. Olthuis, and P. Bergveld, "An integrated silicon capacitive microphone with frequency-modulated digital output," Sens. Actuators A, vol. 69, pp. 267–275, 1998.
- [60] O. Solgaard, F. S. A. Sandejas, and D. M. Bloom, "Deformable grating optical modulator," *Opt. Lett.*, vol. 17, pp. 688–690, May 1992.
- [61] L. J. Hornbeck, T. Howell, R. Knipe, and M. Mignardi, "Digital micromirror device—commercialization of a massively parallel mems technology," in *Proc. ASME Int. Mech. Eng. Congr. Expo.*, 1997, vol. 62, pp. 3–8.
- [62] J. I. Trisnadi, C. B. Carlisle, and R. Monteverde, "Overview and applications of grating light valve based optical write engines for high-speed digital imaging," in *Proc. SPIE-MOEMS Display Imag. Syst. II*, 2004, vol. 5348, pp. 52–64.
- [63] K. E. Petersen, "Silicon as a mechanical material," Proc. IEEE, vol. 70, pp. 58–95, May 1982.
- [64] T. Chi, M. G. Heaton, and A. Mirza, personal communication, Oct. 2004.
- [65] Y. Huang, E. Hægström, X. Zhuang, A. S. Ergun, and B. T. Khuri-Yakub, "A solution to the charging problems in capacitive micromachined ultrasonic transducers," *IEEE Trans. Ultrason., Ferroelect., Freq. Contr.*, vol. 52, pp. 578–580, Apr. 2005.
- [66] A. S. Ergun, Y. Huang, C.-H. Cheng, Ö. Oralkan, J. Johnson, H. Jagannathan, U. Demirci, G. G. Yarahoğlu, M. Karaman, and B. T. Khuri-Yakub, "Broadband capacitive micromachined ultrasonic transducers ranging from 10 kHz to 60 MHz for imaging applications and more," in *Proc. IEEE Ultrason. Symp.*, 2002, pp. 1039–1043.
- [67] Y. Huang, E. Hægström, X. Zhuang, A. S. Ergun, and B. T. Khuri-Yakub, "Optimized membrane configuration improves cMUT performance," in *Proc. IEEE Ultrason. Symp.*, 2004, pp. 505–508.
- [68] G. G. Yarahoğlu, A. S. Ergun, B. Bayram, E. Hægström, and B. T. Khuri-Yakub, "Calculation and measurement of electromechanical coupling coefficient of capacitive micromachined ultrasonic transducers," *IEEE Trans. Ultrason., Ferroelect., Freq. Contr.*, vol. 50, pp. 449–456, Apr. 2003.
- [69] B. Bayram, E. Hægström, G. G. Yarahoğlu, and B. T. Khuri-Yakub, "A new regime for operating capacitive micromachined ultrasonic transducers," *IEEE Trans. Ultrason., Ferroelect.*, *Freq. Contr.*, vol. 50, pp. 1184–1190, Sep. 2003.
- [70] B. Bayram, Ö. Oralkan, A. S. Ergun, E. Hægström, G. G. Yaralioglu, and B. T. Khuri-Yakub, "Capacitive micromachined ultrasonic transducer design for high power transmission," *IEEE Trans. Ultrason., Ferroelect., Freq. Contr.*, vol. 52, no. 2, pp. 326–339, 2005.



Arif Sanlı Ergun (S'96–M'99) was born in Ankara, Turkey, in 1969. He received his B.Sc., M.Sc., and Ph.D. degrees in 1991, 1994, and 1999, respectively, all in electrical and electronics engineering, from Bilkent University, Ankara, Turkey.

He was a research assistant in Bilkent University between 1991 and 1999. He is now an engineering research associate at E. L. Ginzton Laboratory, Stanford University, Stanford, CA. His research interests are microwave electronics, ultrasonics, MEMS, and specifi-

cally CMUTs. He is a member of the IEEE and the Electron Devices Society.



Yongli Huang received the B.S. and M.S. degrees in physics from Fudan University, Shanghai, China, in 1987 and 1990, respectively, and the M.S. degree in electrical engineering from University of Hawaii at Manoa in 1996. He is currently working toward the Ph.D. degree in electrical engineering at Stanford University, Stanford, CA.

He worked as a research associate in the Department of Material Science and Engineering at University of Electronic Science and Technology of China, Chengdu, Sichuan, China, from 1990 to 1992. He joined SiTek, Inc., a subsidiary of BEI Electronics, Inc., Campbell, CA, in 1997 as a member of the technical staff and was promoted to a principal engineer in 1999. His research interests include MEMS technology, micromachined ultrasonic devices, inertial sensors, and optical devices.



Xuefeng Zhuang received the B.S. degree from Louisiana State University, Baton Rouge, LA, in 2002, and the M.S. degree from Stanford University, Stanford, CA, in 2004, both in electrical engineering. He is currently pursuing a Ph.D. degree in electrical engineering at Stanford University, Stanford, CA. His research interests include the design, fabrication, and packaging of capacitive micromachined ultrasonic transducer arrays and their integration with medical imaging systems.



Ömer Oralkan (S'93, M'05) received the B.S. degree from Bilkent University, Ankara, Turkey, in 1995, the M.S. degree from Clemson University, Clemson, SC, in 1997, and a Ph.D. degree from Stanford University, Stanford, CA, in 2004, all in electrical engineering.

Currently, he is an engineering research associate at the Edward L. Ginzton Laboratory at Stanford University. His past and present research interests include analog and digital circuit design, micromachined sensors and ac-

tuators, and semiconductor device physics and fabrication. His current research focuses on the design and implementation of integrated ultrasonic imaging systems.

Dr. Oralkan received the 2002 Outstanding Paper Award of the IEEE Ultrasonics, Ferroelectrics, and Frequency Control Society. He is a member of the IEEE.



Göksenin G. Yarahoğlu (S'92, M'99) was born in Akhisar, Turkey, on May 13, 1970. He received his B.S., M.S., and Ph.D. degrees from Bilkent University, Ankara, Turkey, in 1992, 1994, and 1999, respectively, all in electrical engineering.

He is now working as an engineering research associate in E. L. Ginzton Laboratory, Stanford University, Stanford, CA. His current research interests include design, modeling, and applications of micromachined ultrasonic transducers and atomic force mi-

croscopy at ultrasonic frequencies.



Butrus T. Khuri-Yakub (S'70–S'73–M'76–SM'87–F'95) was born in Beirut, Lebanon. He received the B.S. degree in 1970 from the American University of Beirut, the M.S. degree in 1972 from Dartmouth College, and the Ph.D. degree in 1975 from Stanford University, Stanford, CA, all in electrical engineering.

He joined the research staff at the E. L. Ginzton Laboratory of Stanford University in 1976 as a research associate. He was promoted to a senior research associate in 1978, and to a

Professor of Electrical Engineering (Research) in 1982. He has served on many university committees in the School of Engineering and the Department of Electrical Engineering. Presently, he is the Deputy Director of the E. L. Ginzton Laboratory. Dr. Khuri-Yakub has been teaching both at the graduate and undergraduate levels for over 15 years, and his current research interests include in situ acoustic sensors (temperature, film thickness, resist cure, etc.) for monitoring and control of integrated circuits manufacturing processes, micromachining silicon to make acoustic materials, and devices such as airborne and water immersion ultrasonic transducers and arrays, fluid ejectors, and in the field of ultrasonic nondestructive evaluation and acoustic imaging and microscopy.

Dr. Khuri-Yakub is a Fellow of the IEEE, a senior member of the Acoustical Society of America, and a member of Tau Beta Pi. He is associate editor of *Research in Nondestructive Evaluation*, a Journal of the American Society for Nondestructive Testing. He has authored over 300 publications and has been principal inventor or coinventor of 52 issued patents. He received the Stanford University School of Engineering Distinguished Advisor Award, June 1987, and the Medal of the City of Bordeaux for contributions to NDE, 1983.