A Three-Mask Process for Fabricating Vacuum-Sealed Capacitive Micromachined Ultrasonic Transducers Using Anodic Bonding

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***Abstract*—This paper introduces a simplified fabrication method for vacuum-sealed capacitive micromachined ultrasonic transducer (CMUT) arrays using anodic bonding. Anodic bonding provides the established advantages of wafer-bonding-based CMUT fabrication processes, including process simplicity, control over plate thickness and properties, high fill factor, and ability to implement large vibrating cells. In addition to these, compared with fusion bonding, anodic bonding can be performed at lower processing temperatures, i.e., 350°C as opposed to 1100°C; surface roughness requirement for anodic bonding is more than 10 times more relaxed, i.e., 5-nm root-mean-square (RMS) roughness as opposed to 0.5 nm for fusion bonding; anodic bonding can be performed on smaller contact area and hence improves the fill factor for CMUTs. Although anodic bonding has been previously used for CMUT fabrication, a CMUT with a vacuum cavity could not have been achieved, mainly because gas is trapped inside the cavities during anodic bonding. In the approach we present in this paper, the vacuum cavity is achieved by opening a channel in the plate structure to evacuate the trapped gas and subsequently sealing this channel by conformal silicon nitride deposition in the vacuum environment. The plate structure of the fabricated CMUT consists of the single-crystal silicon device layer of a silicon-on-insulator wafer and a thin silicon nitride insulation layer. The presented fabrication approach employs only three photolithographic steps and combines the advantages of anodic bonding with the advantages of a patterned metal bottom electrode on an insulating substrate, specifically low parasitic series resistance and low parasitic shunt capacitance. In this paper, the developed fabrication scheme is described in detail, including process recipes. The fabricated transducers are characterized using electrical input impedance measurements in air and hydrophone measurements in immersion. A representative design is used to demonstrate immersion operation in conventional, collapse-snapback, and collapse modes. In collapse-mode operation, an output pressure of 1.67 MPa_{pp} is shown at 7 MHz on the surface of the transducer for 60-V_{pp}, 3-cycle sinusoidal excitation at 30-V dc bias.**

Manuscript received October 21, 2014; accepted February 21, 2015. This work was supported by the Defense Advanced Research Projects Agency under contract D13AP00043, by the National Science Foundation under grant 1160483, and by the National Institutes of Health under grant HL117740.

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DOI http://dx.doi.org/10.1109/TUFFC.2014.006794

I. Introduction

Capacitive micromachined ultrasonic transducers (CMUTs) have become an attractive candidate for next-generation ultrasonic imaging and therapy systems [1]. CMUTs are fabricated using standard micromachining techniques, which facilitate realization of densely populated transducer arrays with a broad operating frequency range and various array configurations. The efficiency of this electrostatic transducer mainly depends on the ability to maintain an electric field in the gap with the strength on the order of 10^8 V/cm or higher. For that reason, microfabrication technology has been the principal enabler for CMUTs.

Two main fabrication approaches used for CMUTs are sacrificial release and wafer bonding processes [2]. The sacrificial release method is based on the basic principle of forming a cavity underneath a thin plate by first depositing and patterning a sacrificial layer on the substrate followed by the deposition of the plate layer and then selectively removing the sacrificial layer with a wet chemical etchant [3]. The wet etchant in this process is introduced through holes opened between the cells to reach the sacrificial layer under the plate material. As this is a wet chemical process, the cavities must be dried after the removal of the sacrificial material. Drying the cavities is a critical step, which can lead to collapse of the structure due to capillary forces, a phenomenon referred to as stiction [4]. In the sacrificial release process, the insulation layer, sacrificial layer, and thin plate are usually formed using chemical vapor deposition (CVD), and hence the control over the layer thickness, uniformity, and stress is not very precise. The plate thickness is limited by the CVD process, which makes it difficult to achieve CMUTs with thick plates. In sacrificially released CMUTs, the low-resistivity silicon substrate often serves as the bottom electrode resulting in overlap of top and bottom electrodes in the post area between active cells. This overlap increases the parasitic capacitance and can adversely affect the dielectric reliability of the device. Another shortcoming of the sacrificial release process is that the fill factor is limited due to the inactive region between cells that is used for sealing. Achieving high fill factor is especially critical to realize broadband operation at high frequencies [5].

The other main fabrication method for CMUTs is based on wafer bonding. This approach simplifies the fabrication by transferring a plate with precise mechanical properties over predefined cavities with a single bonding step [6]. The basic process flow in this approach is as follows. A conductive silicon substrate is first thermally oxidized. The resulting silicon dioxide layer is patterned and etched down to the silicon substrate to define the active region of the transducer. A second thermal oxidation is used to grow the insulating layer on the bottom surface of the active region. A silicon-on-insulator (SOI) wafer is fusion-bonded on the processed wafer in vacuum. The wafers are annealed at high temperature (i.e., 1100°C), to form strong covalent bonds. The handle portion and the buried oxide (BOX) layer of the SOI wafer are removed to realize a thin single-crystal silicon plate suspended over the cavities. Individual elements are defined by etching isolation trenches in the silicon plate. The major advantage of the wafer bonding approach is the improved control over the thickness, uniformity, and mechanical properties of the vibrating plate, thanks to the single-crystal silicon device layer of the SOI wafer. The fill factor is improved by eliminating the dead space between cells. In this process, dielectric reliability and parasitic capacitance continue to be issues as the dielectric post structure cannot be made thick if a thin gap is desired for good electromechanical efficiency. In a variant of this process, an extended insulation layer structure is formed in the post area by local oxidation of silicon (LOCOS) to address the low breakdown voltage and high parasitic capacitance issues associated with the described basic wafer bonding process [7], [8]. In this approach, because the LOCOS process also results in lateral oxide growth, the thickness and width of the post structure are coupled, which could be a limitation to implement high-frequency arrays with high fill factor. Other approaches such as using a thick BOX layer to form completely insulated silicon bottom electrodes below the active plate region in each CMUT cell are proposed [9]. All of these approaches introduce additional complexities in the fabrication process and result in increased cost and degradation of the yield.

In the summarized conventional CMUT structures, usually, a low-resistivity silicon substrate is used as the bottom electrode. The parasitic capacitance is mainly caused by the overlap of the substrate and the top electrode in the post region. It has been previously shown that a patterned metal bottom electrode on a quartz substrate results in reduced parasitic capacitance [10]. However, this process, being based on sacrificial release, suffers from poorer control over thickness, uniformity, and stress of deposited layers compared with wafer-bonding-based approaches.

Anodic bonding comes across as an appealing way of combining the benefits of wafer bonding and an insulating substrate. One can define a patterned metal bottom electrode on cavities etched in a glass substrate and anodically bond a silicon or SOI wafer on top to realize a CMUT [11], [12]. However, one major shortcoming of previously demonstrated anodically bonded CMUTs is the lack of vacuum cavity due to outgassing during bonding. In these devices, either the cavities were pressurized with the trapped oxygen gas under a thick plate [11] or the cavities were exposed to the outside, making the transducer unsuited for immersion operation [12].

In this paper, we present a fabrication process flow based on anodic bonding to make CMUTs with vacuum-sealed, sub-micrometer cavities suitable for implementing high-frequency imaging arrays. In this process, we evacuate the trapped gas by opening a channel to the cavities and then we seal that channel in vacuum. This anodic bonding-based process has several advantages compared with previously demonstrated CMUT fabrication approaches. The plate is implemented using the device layer of an SOI wafer, and hence good control over plate thickness and uniformity can be achieved. Anodic bonding is a cost-effective, low-temperature bonding process that allows use of patterned metal bottom electrodes to potentially minimize the parasitic series resistance and the parasitic shunt capacitance. Anodic bonding tolerates 10 times higher surface roughness compared with fusion bonding, which requires a root-mean-square (RMS) roughness smaller than 0.5 nm [13], [14]. Anodic bonding does not require any special surface activation before bonding. Furthermore, high fill factor can be achieved as compared with fusion, thermo-compression, and eutectic bonding methods. The overall complexity of the presented process is low as cavities on a borosilicate glass substrate can be easily achieved by either dry or wet chemical etching using photoresist as a mask [15]–[17].

In the next section, we present a detailed description of the developed fabrication process. In Section III, static surface deflection and electrical input impedance characterization of the resulting devices are presented and transmit pressure measurements in immersion are shown for different operating modes. Section IV discusses some important aspects of the presented fabrication process and proposes further improvements.

II. Fabrication Process

The realized CMUT structure consists of a thin single-crystal silicon plate with a thin silicon nitride insulation layer and a patterned metal bottom electrode deposited inside a vacuum-sealed, sub-micrometer cavity (Fig. 1). The vibrating plate is formed by depositing a layer of silicon nitride on the device layer of an SOI wafer before bonding. The silicon nitride layer is mainly to prevent electrical shorting when the plate comes in contact with the metal bottom electrode following pull-in and also acts as an intermediate bonding layer. Anodic bonding of borosilicate glass to thin-film coated silicon wafers was demonstrated previously [18]–[20]. The device layer is chosen to be highly doped conductive silicon as it is used as the top electrode. The bottom electrode is deposited on the surface of the cavities so that the overall parasitic capaci-

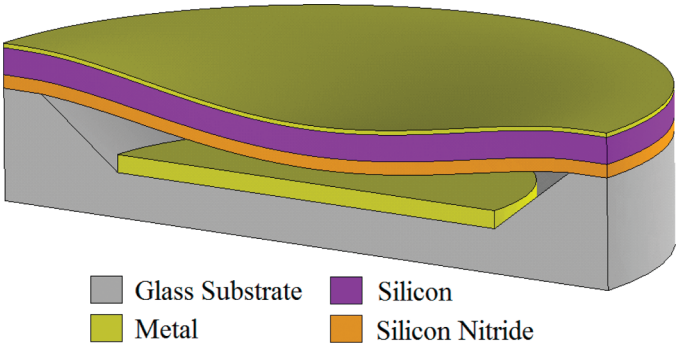


Fig. 1. 3-D illustration of the fabricated CMUT cell.

tance of the device is reduced and the dielectric reliability is improved as the post region in this approach does not experience any significant electric field. During the formation of bond pads to provide electrical access to bottom electrodes of individual transducer elements, a metal layer is also deposited on top of the silicon plate to further increase the conductivity of the top electrode and to provide a suitable layer for wire bonding.

As the starting substrate, we used a standard 0.7-mm-thick, 100-mm-diameter borosilicate glass wafer (Borofloat33, Schott AG, Jena, Germany) that has a high surface quality with an RMS roughness (Rq) of 0.7 nm and a good flatness with a warp that is less than 0.05%. The thermal expansion coefficient of the borosilicate glass substrate is 3.25 ppm/°C, close to that of silicon (3.2 ppm/°C) preventing stress in the silicon plate after anodic bonding. The SOI wafer that we used for fabrication has a 2 ± 0.5-μm-thick, n-type device layer with 0.001 to 0.005 Ω·cm resistivity, a 0.5-μm-thick BOX layer, and a 500-μm-thick handle wafer with 1 to 10 Ω·cm resistivity.

A. Forming Cavities and Bottom Electrodes

Before the process the borosilicate glass substrate was cleaned for 15 min in a heated mixture of concentrated sulfuric acid (H_2SO_4) and 30% hydrogen peroxide (H_2O_2; Piranha solution) for removal of organics and other gross particle contaminants from the surface. The cavity pattern was defined using 2-μm-thick negative photoresist (AZ-5214E IR, Clariant, Wiesbaden, Germany), which is suitable for lift-off [Fig. 2(a)]. The patterned wafer was hard-baked for 2 h at an elevated temperature of 125°C [Fig. 2(b)]. This step promotes the adhesion between the photoresist and the substrate and makes the photoresist a better mask for the etching. The cavities were created in 10:1 buffered oxide etch (BOE) solution [Fig. 2(c)]. Wet etching was preferred for a uniform etching and minimal surface roughness in the cavities. We measured the BOE lateral etch as 10 times faster than its vertical etch. It has been reported that a water-rich interface layer between the wafer and resist causes the etchant to penetrate very fast laterally [21]. As a result, faster lateral than vertical etching is often seen in isotropic etching. This lateral etch must be considered in the mask design to achieve the target cavity size after etching. 230-nm-deep cavities were etched in 15-min total time with 5 cycles of BOE etching of 3 min each. The photoresist was hard-baked for 10 min between each cycle to prevent peeling. After the cavity etching was completed, the wafer was transferred to the evaporation chamber without removing the resist. The gap height of the CMUTs was defined by the difference of the etch depth and the thickness of the metal deposited in the cavities. Thus a metal stack that consists of 20 nm of chromium as an adhesion layer and 90 nm of gold was deposited to obtain the 120-nm gap height [Fig. 3(d)]. The undercut that was formed during the wet etch helps to confine the metal electrode to the bottom surface of the cavity and also makes the lift-off process easier. The atomic force microscopy (AFM) imaging of the cavity (Fig. 3) demonstrated an RMS surface roughness of 2 nm on the metal surface in the cavity after lift-off.

B. Bonding

Prior to bonding, we deposited 200-nm silicon nitride on top of the device layer of the SOI wafer by using plasma-enhanced, chemical-vapor deposition (PECVD) at 1000-mTorr chamber pressure and 350°C temperature. This silicon nitride layer serves as an insulation layer between the conductive silicon plate (top electrode) and the metal in the cavity (bottom electrode) during device operation. The glass wafer and the SOI wafers were cleaned using solvents and Piranha solution, respectively. The borosilicate glass surface and the nitride surface were anodically bonded together at 350°C under 2.5-kN down force in vacuum (10^{-4} Torr) in a semi-automatic bonding system [model EVG510, EVG Group, St. Florian, Austria; Fig. 2(e)]. Typically, it is recommended to limit the current during the bonding [22]. The setup that we use does not have a current limited bonding option. Thus, the voltage was ramped up to its final value at a rate of 20 V/min not to cause breakdown in the silicon nitride layer and kept at the target value for 30 min. The metal is exposed to high electrical field during bonding, thus various bonding voltages were evaluated to maintain high bond yield without damaging the floating bottom electrode inside the cavities. The bonding was tested at 1000, 700, 600, and 500 V. A high bonding yield with no damage on the bottom electrodes was observed at 600 V for the presented process and wafer parameters. After bonding, the handle wafer was ground down to 100 μm. We used a heated tetramethylammonium hydroxide (TMAH) solution (10% TMAH at 80°C) to selectively remove the remaining handle wafer over the BOX layer, which was subsequently removed using 10:1 BOE solution [Fig. 2(f)].

C. Reaching Pads and Sealing

The borosilicate glass substrate is exposed to high electrostatic field, which causes outgassing during bonding [23]. Oxygen is the major component of the gas trapped in the cavities, making the process not suitable for appli-

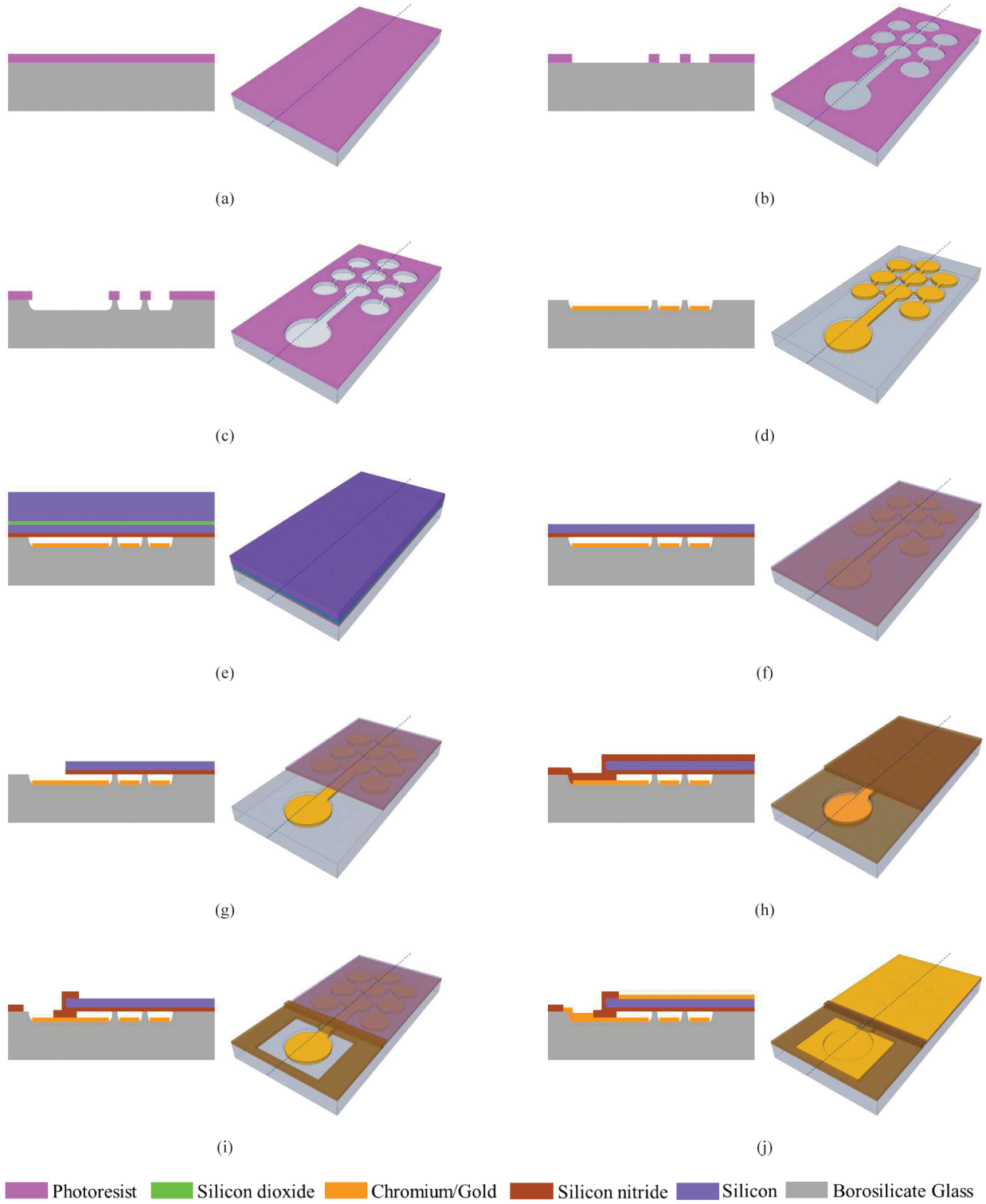


Fig. 2. Fabrication process flow. (a) Photoresist coated glass substrate; (b) lithography for cavity pattern using first mask; (c) BOE etch; (d) metal deposition and lift-off; (e) anodic bonding; (f) handle and BOX removal; (g) silicon etch for array separation and reaching pads using second mask; (h) silicon nitride deposition for sealing; (i) silicon nitride etch using third mask; (j) metal deposition and lift-off.

cations that require vacuum-sealed cavities. The problem can be solved using getter materials but the required getter thickness could be on the order of micrometers [24], which is much larger compared with the sub-micrometer cavity height we aim to achieve. Instead of using a getter material, we proposed to evacuate the gas inside the cavities and seal them in vacuum. To access the bottom electrode for forming bond pads, the plate at the pad location has to be etched. When the plate over the metal pad region is etched, the channel over the metal surface is exposed and allows the gas to escape [Fig. 2(g)]. We used reactive ion etching with SF_6 gas to etch silicon.

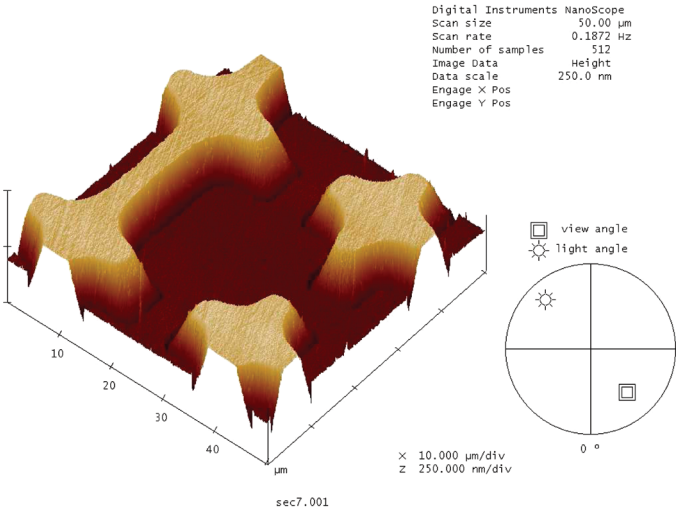


Fig. 3. AFM image of a cavity after metal bottom electrode deposition and lift-off.

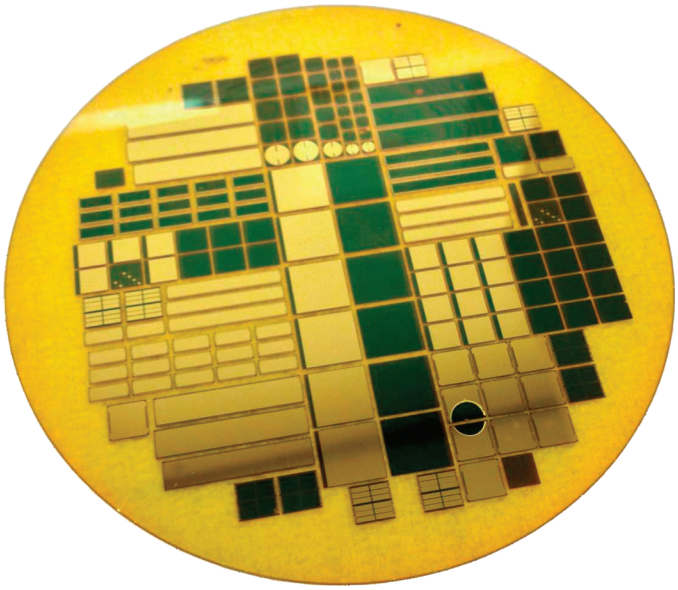


Fig. 4. Fabricated devices on the borosilicate glass wafer.

Different arrays implemented on the same wafer are also separated during this step by etching the conductive silicon between different arrays. After evacuating the trapped gas in the cavities, oxygen plasma is used to remove the photoresist. Because there is no wet cleaning at this step, no liquid reaches inside the cavities. Avoiding wet processing is important at this step as it can lead to stiction and consequently collapsed cells in the drying stage. To seal the cavities we deposited PECVD silicon nitride [Fig. 2(h)]. The thickness of the silicon nitride was chosen to be more than three times the cavity height for a proper sealing [10].

D. Forming Electrical Contacts

After the sealing step, the wafer surface is completely covered by silicon nitride. To create electrical contacts, the silicon nitride layer on the bond pads has to be removed. At this point, the silicon nitride deposited on the conductive silicon plate is also removed leaving the silicon nitride only on the locations where sealing is required. For etching the silicon nitride we used reactive ion etching where the AZ5214E IR photoresist was used as a mask. The photoresist was hardbaked for 5 min at 125°C before etching. After removing the nitride layer on the pads and on the silicon plates [Fig. 2(i)], 20-nm chromium and 130-nm gold were deposited. The chromium-gold metal stack was then lifted off in *N*-methyl-2-pyrrolidone (NMP) solvent [Fig. 2(j)]. At this step, the device fabrication is completed.

III. Characterization of Test Devices

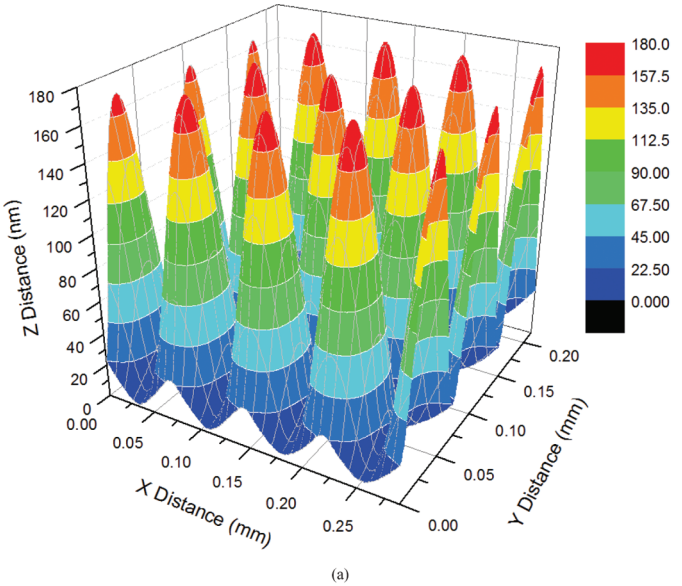
We demonstrated the presented fabrication process using a mask design including several single transducers, arrays, and test structures. The optical image of the wafer after fabrication is shown in Fig. 4. For verifying the design and fabrication process, we selected three CMUT designs with the physical parameters shown in Table I. These parameters are the target parameters considering the lateral etch due to wet etching described in the previous section.

A. Static Surface Deflection Characterization

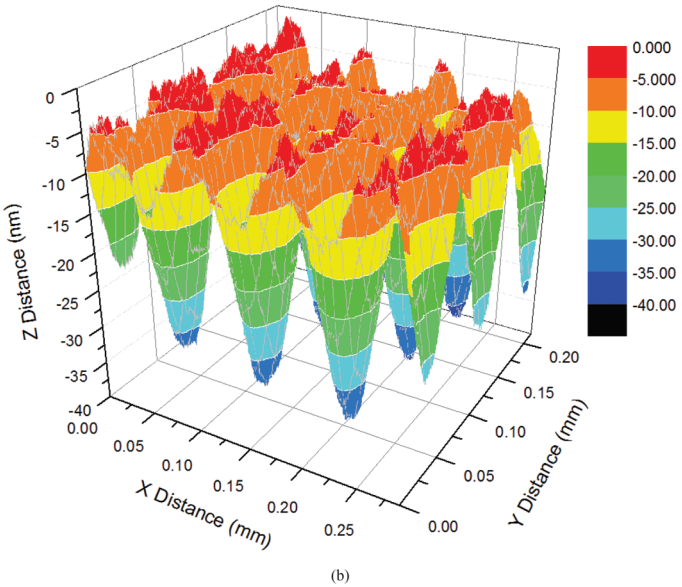
The success of the sealing process was confirmed by measuring the deflection profile of the plate after the completion of the entire process. The upward plate deflection due to gas trapped inside an array of cells of design #1 was measured using an optical surface profilometer [model NewView 5000, Zygo Corporation, Middlefield, CT, USA; Fig. 5(a)]. After evacuating the gas and sealing the channels, the deflection under atmospheric pressure was measured as 28 nm for the same design [Fig. 5(b)]. Finite element analysis (FEA; ANSYS v.14, ANSYS Inc., Canonsburg, PA, USA) for this cell predicts the atmospheric deflection as 26.8 nm, which also proves that there is no significant stress due to anodic bonding and the cavity is under vacuum.

TABLE I. Physical Parameters of the Fabricated CMUTs.

Design	#1	#2	#3
Shape of the cell		Square	
Cell width (µm)	77	71	53
Cell-to-cell distance (µm)		4	
Top metal thickness (µm)		0.15	
Silicon layer thickness in plate (µm)		1.8	
Insulating layer thickness in plate (µm)		0.2	
Gap height (µm)		0.12	
Bottom metal thickness (µm)		0.11	
Substrate thickness (µm)		700	
Number of cells per element	224	279	480
Length of an element (µm)	2258	2240	2270
Width of an element (µm)	638	665	674

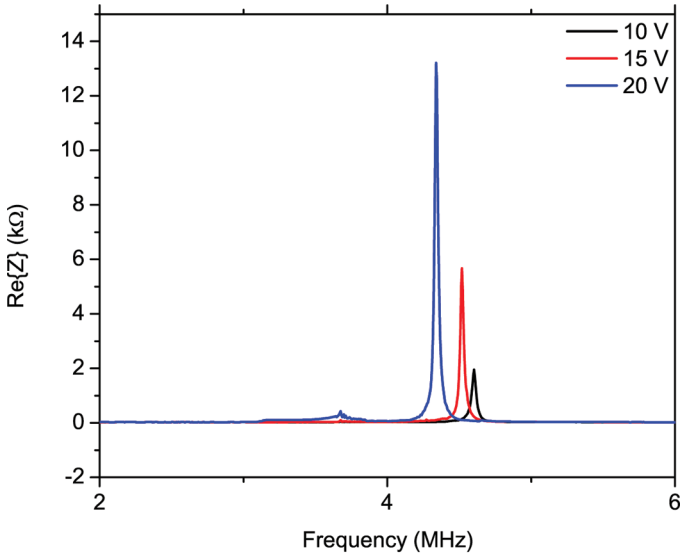


(a)

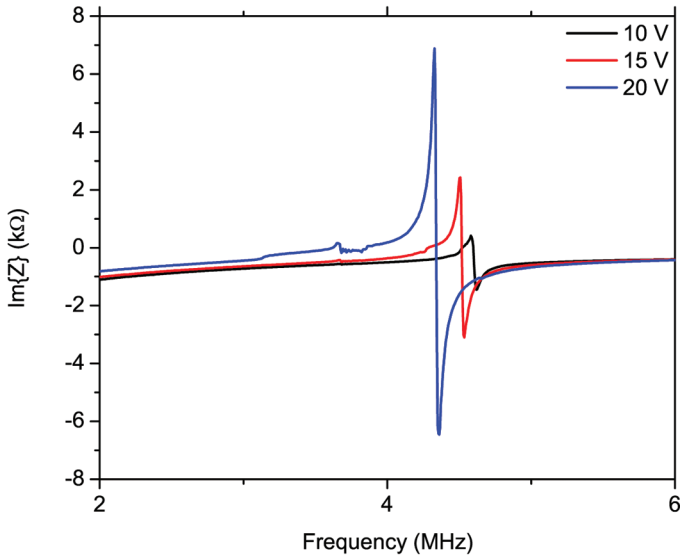


(b)

Fig. 5. Measured deflection profile of the plate over several cells: (a) after bonding and removal of handle wafer and BOX layer; (b) after gas evacuation and sealing in vacuum.



(a)



(b)

Fig. 6. Impedance measurements of design #2. (a) Real part of the electrical input impedance; (b) imaginary part of the electrical input impedance.

B. Electrical Input Impedance Characterization in Air

All three designs were tested in air using a network analyzer (model E5061B, Agilent Technologies Inc., Santa Clara, CA, USA) with an internal dc supply available up to 40 V. The measured real and imaginary parts of electrical input impedance in air for design #2 are shown for bias voltages of 10, 15, and 20 V in Fig. 6. The baseline in the real part corresponds to the series resistance of the device, which is measured as 21 Ω. To measure the collapse voltage, the resonant frequency is observed while increasing the bias voltage by 1-V steps. The collapse voltage is determined by the sudden resonant frequency jump at the collapse.

The collapse voltages and the resonant frequencies of these three designs were also simulated using FEA. TRANS 126, electromechanical transducer elements are used for the direct coupling of electrostatic and structural domains. The element is capable of handling the spring softening effect in the simulations. First, static analysis was performed to find the collapse voltages. Second, prestressed harmonic analysis was carried out to find the resonant frequency at the 70% of the collapse voltage. The material properties used in the simulations are listed in Table II. The simulations and the actual measurements are compared in Table III. The results show that the fabricated CMUTs operate as predicted by the finite element model.

We have measured the electromechanical coupling coefficient of design #2 (k_T^2) as 0.1 at 15-V dc bias (75% of the collapse voltage) and 0.3 at 20-V dc bias (90% of the collapse voltage), which are consistent with results report-

TABLE II. MATERIAL PROPERTIES USED IN SIMULATIONS.

	Silicon	Silicon nitride	Gold
Young modulus (GPa)	148	260	70
Density (kg/m^3)	2328	3100	3300
Poisson ratio	0.17	0.27	0.33
Relative permittivity		5.7	

ed earlier by Yaralioglu *et al.* [25]. The single cell capacitance of the same design under atmospheric pressure is calculated as 0.23 pF by using FEA, which corresponds to a total capacitance of 64.17 pF when multiplied with the total number of cells. We measured the total capacitance of design #2 as 67.84 pF, indicating that the external parasitic capacitance is less than 6%.

Design #2 was used for characterization in immersion.

C. Acoustic Pressure Characterization in Immersion

For immersion tests, vegetable oil was used because the transducer surface was not electrically insulated. A small tank was built over the transducer element that was wire-bonded to a chip carrier. A calibrated hydrophone (model HGL-0200, Onda Corporation, Sunnyvale, CA, USA) connected to a preamplifier (model AH-2010, Onda Corporation) was placed at 14-mm distance from the transducer surface on the central axis of the transducer. The element was operated in conventional, collapse-snapback, and collapse modes. A unipolar pulse with an amplitude of 20 V was superimposed on the dc bias voltage through a bias-T circuit. The conductive plate layer was grounded and the bottom electrode was used as the active electrode. First, a dc voltage of 12 V was applied and the element was driven with a 110-ns wide pulse. In that case, the element operates in conventional mode and the signal received by the hydrophone is shown in Fig. 7(a). For collapse-snapback operation, a nonlinear operating mode reported earlier [26], the transducer was biased at 21 V, on the brink of collapse, and the pulse width was increased to 150 ns to allow sufficient time for the plate to fully collapse and snap back. In this mode, the time that it takes for the plate to collapse and the time for a collapsed plate to snap back determines the dynamic response of the CMUT [27]. The measured hydrophone output waveform in collapse-snapback mode is shown in Fig. 7(c). Lastly, a dc voltage of 30 V, higher than the collapse voltage, was applied to operate the transducer in collapse mode. In this mode, the center of the plate is kept in constant contact with the bottom electrode; thus, only the region of the plate between the center and the clamped edge moves when the transducer is excited with an ac signal [28]. Consequently, the operating frequency shifts to higher frequencies, approximately twice of what is observed in conventional operation [29]. To operate the CMUT properly in the collapse mode, the applied pulse width was reduced to 60 ns. The measured hydrophone output for collapse mode is shown in Fig. 7(e).

TABLE III. SIMULATED VERSUS MEASURED VALUES OF RESONANT FREQUENCIES AND COLLAPSE VOLTAGES OF THE THREE DESIGNS.

	Collapse voltage (V)		Resonant frequency (MHz)	
Design	FEA	Measured	FEA	Measured
#1	18	17	3.94	3.9
#2	22	22	4.6	4.51
#3	41	39	7.75	7.6

The measurements were performed in air. For resonant frequency measurements, the bias voltage was set to 70% of the collapse voltage.

Fourier transforms of the waveforms presented in Figs. 7(a), 7(c), and 7(e) were calculated to analyze the frequency response in different operating modes. The normalized frequency spectrum at 14 mm and the normalized frequency spectrum after compensating for frequency-dependent attenuation and diffraction losses are shown in Figs. 7(b), 7(d), and 7(f) for different operating modes. The notches at 3.8 MHz and its higher harmonics correspond to the ringing in the substrate [30] as it was also evident in the time domain data as a tail following the main pulse. Substrate ringing can be pushed out of the frequency band of interest by choosing the substrate thickness accordingly. The results are summarized in Table IV.

The results are not corrected for pulse shape. t_p is the pulse width. f_c is the center frequency. FBW is the 3-dB fractional bandwidth. $P_{pp,surface}$ is the peak-to-peak pressure on the surface after compensating for diffraction and attenuation losses. S_{xmit} is the transmit sensitivity.

The presented CMUT structure with full electrode coverage over the entire cavity enables increased contact radius in collapse mode and hence can achieve high output pressure levels [31]. To test the transmit output pressure in collapse mode further, we set the dc bias voltage at 30 V and applied a 60-V_{pp}, 7-MHz, 3-cycle sinusoidal excitation signal using an RF power amplifier (model 325LA, Electronics & Innovation Ltd., Rochester, NY, USA). The pressure field on the xy-plane was measured at 14-mm distance from the transducer surface using a three-axis motorized stage (model PRO165, Aerotech Inc., Pittsburgh, PA, USA) with 100-μm step size (Fig. 8). By compensating for the diffraction and attenuation losses at the center

TABLE IV. SUMMARY OF HYDROPHONE MEASUREMENTS.

	V_{DC} (V)	t_p (ns)	$P_{pp,surface}$ (kPa)	S_{xmit} (kPa/V)	$f_{c,surface}$ (MHz)	FBW (surface), (%)
Conventional	12	110	226	11.3	2.76	107
Collapse-snapback	21	150	726	36.3	2.84	113
Collapse	30	60	568	28.4	7.15	126

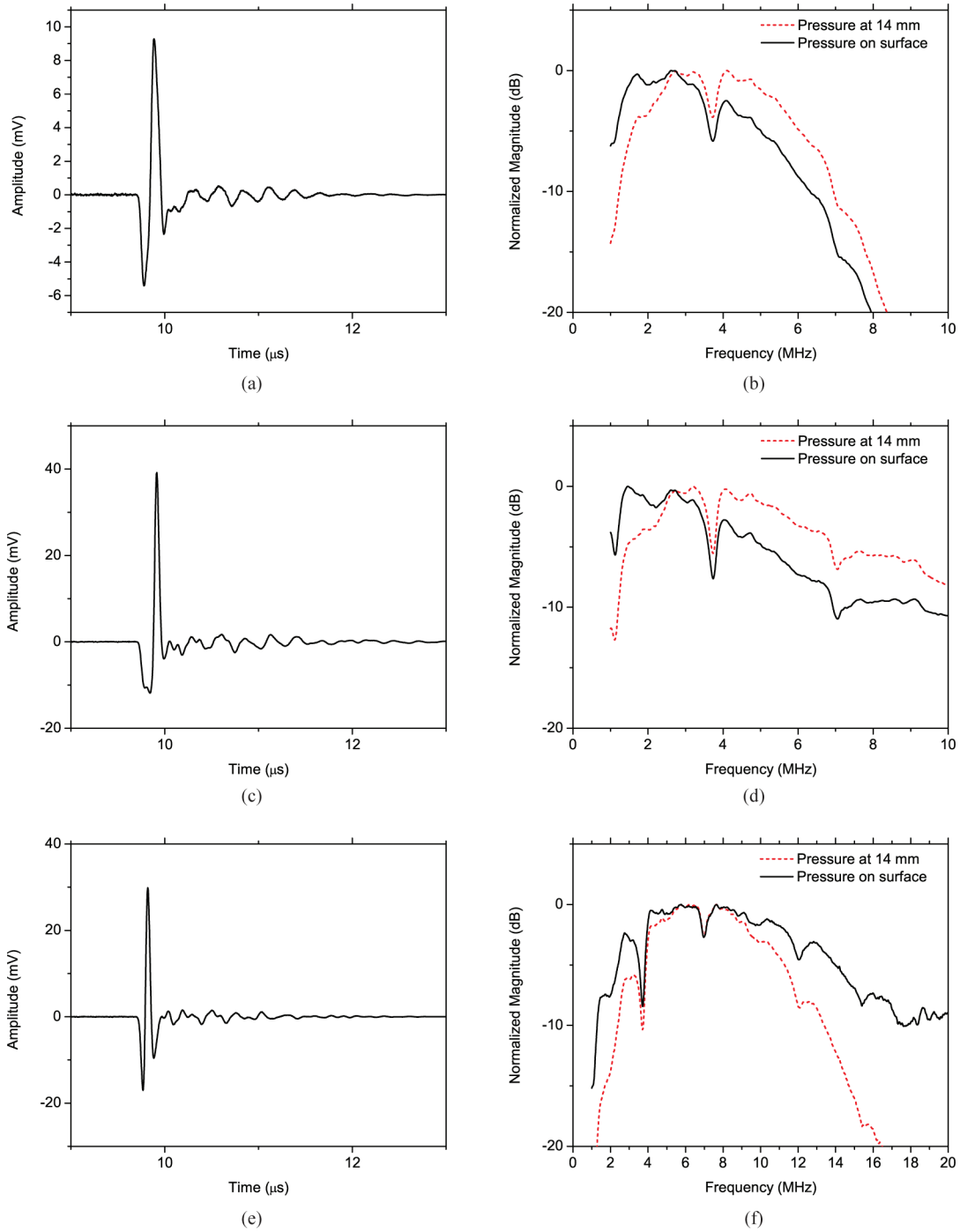


Fig. 7. Measured hydrophone output for design #2 in immersion at 14 mm from the transducer (time domain). (a) Conventional mode (V_{DC} = 12 V), (c) collapse-snapback mode (V_{DC} = 21 V), (e) collapse mode (V_{DC} = 30 V). Normalized output spectrum at the surface after compensating for frequency-dependent attenuation and diffraction losses. (b) Conventional mode (V_{DC} = 12 V), (d) collapse-snapback mode (V_{DC} = 21 V), (f) collapse mode (V_{DC} = 30 V).

frequency of 7 MHz, we calculated the peak-to-peak pressure as 1.67 MPa_{pp} on the transducer surface (Fig. 9).

IV. Discussion

The devices fabricated with the presented fabrication method demonstrated operation that is reliable and consistent with the theoretical designs. One of the main advantages of the presented fabrication approach is the reduced process complexity. 1-D arrays and single transducers have been fabricated with this process using only three photolithographic steps. Although anodic bonding has been used for CMUT fabrication before, different from previous demonstrations, we were able to realize vacuum-sealed, sub-micrometer cavities suitable for imaging arrays that can work in immersion or in contact with tissue. We achieved the vacuum sealing of the cavities by opening

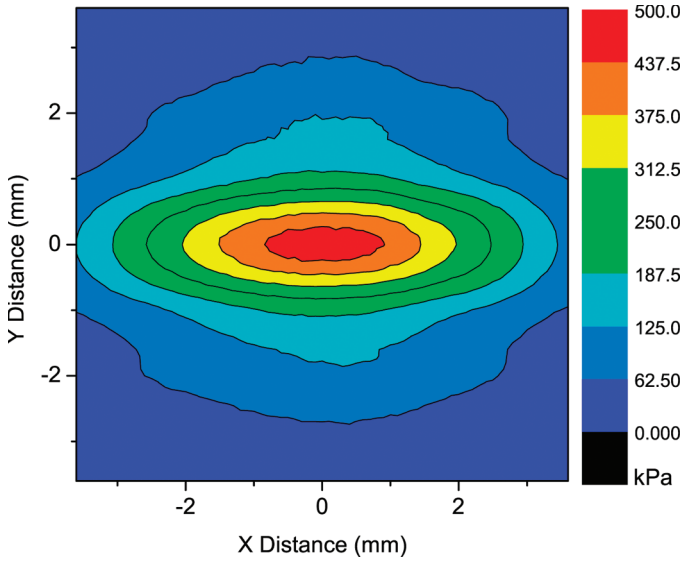


Fig. 8. Measured pressure field on a plane parallel to the transducer surface at a distance of 14 mm (V_{DC} = 30 V, collapse mode; V_{DC} = ±30-V, 7-MHz, 3-cycle sinusoidal).

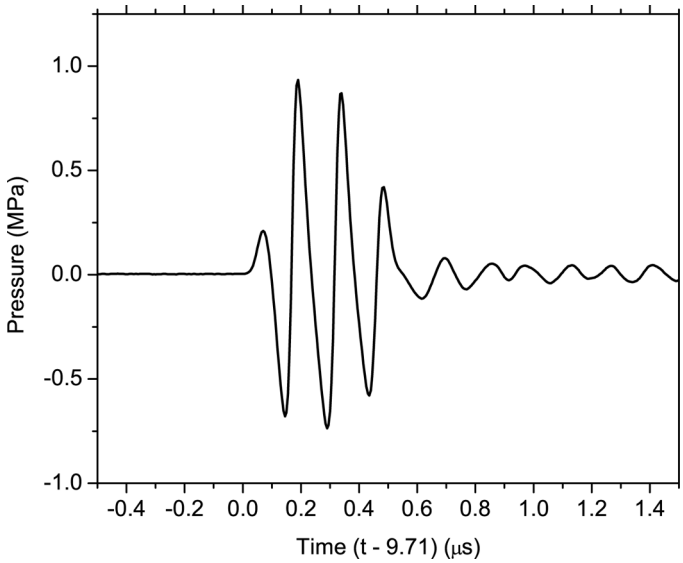


Fig. 9. Pressure on the surface calculated by compensating the on-axis pressure measurement at 14 mm for attenuation and diffraction losses (V_{DC} = ±30-V, 7-MHz, 3-cycle sinusoidal).

a vent in the plate to evacuate the trapped gas in the cavity, a byproduct of anodic bonding, and then depositing a silicon nitride layer in vacuum environment for sealing. Our sealing process is significantly different from the one used in sacrificial release process flow because the seal holes are not distributed across the element. The gas can be evacuated from a single point. Use of PECVD nitride deposition instead of low-pressure chemical vapor deposition (LPCVD) also helps because PECVD is more directional than LPCVD and can conformally coat the substrate, making the sealing more localized. Consequently, the sealing material is only deposited around the vent hole and does not get deposited inside the cavity. As a result, sealing-related problems observed in the sacrificial release process, such as gap height variations due to in-cavity deposition of sealing material [32], are not an issue in the presented approach.

Another difference in our process compared with previously demonstrated anodically bonded CMUT fabrication processes is the silicon nitride insulation layer we incorporated in the device structure, specifically under the conductive plate. This insulation layer enabled operation of these devices in collapse and collapse-snapback modes. Although we have not observed any failure in devices tested in collapse and collapse-snapback modes, further studies are required to investigate the long-term reliability of CMUTs operating in these contact modes. By choosing PECVD silicon nitride deposited at 350°C, the residual stress in the plate structure is minimized. The insulating layer could also be defined inside the cavity, instead of being part of the plate structure, at the expense of increased process complexity.

A key part of the presented process is using the same patterned photoresist layer both as a mask for wet etching of the glass substrate and also to lift off the evaporated metal film to define the bottom electrodes. As a result, in one photolithographic step the glass wafer becomes ready for bonding.

In the presented process, the gap height is determined by the difference of the etched cavity depth and evaporated bottom electrode thickness. Because the cavity etching is performed by a timed etch using 10:1 BOE, the etch rate should be well characterized to obtain repeatable cavity depth. We have consistently measured the vertical etch rate of 10:1 BOE in the borosilicate glass substrate as 15.3 nm/min. The lateral etch causing the aforementioned undercut progresses much faster at a rate of 155 nm/min, which should be accounted for during mask design. The evaporation rate also should be well characterized to control the final gap height. We used electron-beam evaporation, which offers precise rate control at very low deposition levels and were able to meet our target gap height of 120 nm. The variation of the gap height over the wafer was measured as less than 2%. We also measured less than 1% variation in resonant frequency and capacitance of 66 transducer elements in an area of 9.15 mm^2.

One of the processing steps that can be improved further is the silicon nitride etch by adding an etch-stop layer on top of the plate. Although highly selective, i.e., 100:1, dry etching of silicon nitride over silicon can be achieved with high flows of O_2 and N_2, and relatively small additions of CF_4 and NF_3 as a source of fluorine [33], an etch-stop layer on top of the silicon plate would allow use of standard etch recipes and would prevent pitting on the silicon plate due to overetching. The addition of an etch-stop on top of the silicon plate could be a significant addition to the presented process flow; slight overetching at this step is desired to ensure that there is no silicon nitride left on the exposed metal bottom electrode before the final metal deposition on the bond pad.

For the first demonstration of the presented fabrication scheme, we used a 0.7-mm-thick substrate that resulted

in substrate ringing at 3.8 MHz, which interferes with the signal spectrum for the presented designs. Considering that borosilicate glass wafers thinner than 0.1 mm are available, substrate ringing can be pushed beyond 25 MHz. Furthermore, using additional techniques such as using a lossy backing and roughening the backside of the substrate can further alleviate the substrate ringing [34].

The borosilicate glass substrate offers additional advantages for applications, in which ultrasound is either generated or detected by optical means, e.g., photoacoustic imaging [35] and interferometric displacement detection [36], as the borosilicate glass is optically transparent in the visible and near-infrared wavelength range.

V. Conclusion

We have presented a fabrication process for CMUTs based on anodic bonding. This process offers the well-known advantages of wafer bonding such as good control over the thickness and mechanical properties of the plate and overall reduced process complexity. In addition to these general advantages of wafer-bonding process, anodic bonding has the specific advantage of being more tolerant to roughness on the bonding surface. Furthermore, the narrower post structures are feasible with anodic bonding to maximize the fill factor, which is especially critical to achieve wide bandwidth at high frequencies. The maximum processing temperature in the presented approach is 350°C, which allows use of a patterned metal bottom electrode for improved series resistance. Use of the glass substrate helps reduce the parasitic capacitance and improves the dielectric reliability as the top plate and the bottom electrode mainly overlap on the active transducer area and not on the posts.

Through electrical measurements, we determined the characteristics of the fabricated devices and evaluated process uniformity. We found that the experimentally measured characteristics are as predicted by finite-element models and the demonstrated yield and uniformity are suitable for implementation of imaging arrays. The transmit pressure measurements showed that 1.67 MPa_{pp} is obtained at 7 MHz on the surface of the transducer for 60-V_{pp} excitation amplitude at 30-V dc bias in collapse mode, indicating a performance comparable to previously reported CMUT arrays, but achieved with a much simpler fabrication process.

Acknowledgments

The authors thank Marzana Mantasha Mahmud for the impedance measurements, Jeanne Lunsford for help with data acquisition setups, and Joe Matthews for dicing the wafer and wire bonding test devices on chip carriers.

The authors acknowledge the use of the Analytical Instrumentation Facility (AIF) at North Carolina State University, which is supported by the State of North Carolina and the National Science Foundation. Device fabrication was in large part performed at NCSU Nanofabrication Facility.

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