Wafer-Bonded 2-D CMUT Arrays Incorporating Through-Wafer Trench-Isolated Interconnects with a Supporting Frame

Xuefeng Zhuang, *Student Member, IEEE*, Ira O. Wygant, *Student Member, IEEE*, Der-Song Lin, Mario Kupnik, *Member, IEEE*, Ömer Oralkan, *Member, IEEE*, and Butrus T. Khuri-Yakub, *Fellow, IEEE*

***Abstract*—This paper reports on wafer-bonded, fully populated 2-D capacitive micromachined ultrasonic transducer (CMUT) arrays. To date, no successful through-wafer via fabrication technique has been demonstrated that is compatible with the wafer-bonding method of making CMUT arrays. As an alternative to through-wafer vias, trench isolation with a supporting frame is incorporated into the 2-D arrays to provide through-wafer electrical connections. The CMUT arrays are built on a silicon-on-insulator (SOI) wafer, and all electrical connections to the array elements are brought to the back side of the wafer through the highly conductive silicon substrate. Neighboring array elements are separated by trenches on both the device layer and the bulk silicon. A mesh frame structure, providing mechanical support, is embedded between silicon pillars, which electrically connect to individual elements.**

We successfully fabricated a 16 × 16-element 2-D CMUT array using wafer bonding with a yield of 100%. Across the array, the pulse-echo amplitude distribution is uniform (σ = 6.6% of the mean amplitude). In one design, we measured a center frequency of 7.6 MHz, a peak-to-peak output pressure of 2.9 MPa at the transducer surface, and a 3-dB fractional bandwidth of 95%. Volumetric ultrasound imaging was demonstrated by chip-to-chip bonding one of the fabricated 2-D arrays to a custom-designed integrated circuit (IC). This study shows that through-wafer trench-isolation with a supporting frame is a viable solution for providing electrical interconnects to CMUT elements and that 2-D arrays fabricated using wafer-bonding deliver good performance.

I. Introduction

Capacitive micromachined ultrasonic transducers (CMUTs) have attracted attention from both industry and academia as an ultrasound transducer technology to complement/replace piezoelectric transducers. On the application side, CMUTs have been shown to enhance existing medical ultrasound imaging probes [1], [2]. Furthermore, new applications that are considered challenging for piezoelectrics have been explored using CMUTs. In medical imaging, examples include annular ring-shaped arrays [3], [4], microlinear arrays [5], fully populated 2-D arrays [6], [7], flexible arrays [8], [9], and 2-D reconfigurable arrays [10]. In medical therapy, CMUTs can provide MR-compatible high-intensity focused ultrasound (HIFU) [11], [12]. On the device side, novel designs and fabrication methods have been proposed to improve the performance and reliability of CMUTs [13]–[17]. One of the milestones was the demonstration of CMUTs made by direct wafer-to-wafer fusion bonding by Huang *et al.* [13]. Wafer-bonding offers unparalleled fabrication flexibility as well as improved device performance and uniformity, when compared with the traditional surface micromachining technique [13]. Coupled with innovative designs, wafer-bonded CMUTs have delivered high output pressures, while retaining the expected wide fractional bandwidth [18].

It is highly desired to directly integrate CMUTs with front-end integrated circuits (ICs) (3-D integration) for medical ultrasound imaging applications [6]. One approach for 3-D integration is to build the CMUTs and the ICs on the same substrate (monolithic integration) [19]–[21]. The CMUT is directly built on the substrate with the IC using a post IC fabrication process. Thermal, material, and processing method choices of the CMUT are severely limited to be compatible with the IC on the same substrate. For example, the CMUT process temperature must be < 400°C to avoid severing the metal connections in the IC. Direct wafer-to-wafer fusion bonding becomes impossible due to the needed high-temperature (∼1000°C) postbonding annealing step. Moreover, monolithic integration of IC and CMUT generally reduces device yield, thus likely increasing the cost.

Another approach for 3-D integration is based on multiple chip modules (MCM) assembled through chip-to-chip bonding. This approach allows CMUTs and ICs to be fabricated on separate substrates in separate facilities. The respective fabrication processes can be individually optimized, expanding the thermal, material, and fabrication method choices for either module. The CMUT fabrication benefits the most from this decoupling. A variety of micro electromechanical systems (MEMS) fabrication techniques that are uncommon for ICs, such as through-wafer deep reactive ion etching (DRIE), and wafer-to-wafer fusion bonding (a powerful method of fabricating CMUTs with improved performance), can be used. Further, a defective CMUT or IC can be excluded from the later assembly step, hence reducing cost. However, the chip-to-chip bonding surface has to be located on the back of the CMUT substrate so that the CMUT can interface with the medium. Thus, in the MCM approach for 3-D

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The authors are with the Edward L. Ginzton Laboratory, Stanford University, Stanford, CA (e-mail: xzhuang@stanford.edu).

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integration, it is necessary to provide electrical contact to CMUT elements from the back side of the substrate. Therefore, developing proper through wafer interconnect methods is essential in this approach.

Researchers have reported on interconnect techniques both based on through-wafer vias [22]–[24] and through-wafer trench isolation [25]. In the through-wafer via implementation, a conductive material, usually doped polysilicon, is used to fill the vias through the several hundred micron thick silicon substrate. This material serves as the conductor between the front side of a silicon wafer, where the CMUT elements reside, and the back side of the wafer, where the chip-to-chip bond pads are located [22]–[24]. Integrating through-wafer vias with CMUTs is a complex process requiring many lithographic steps. After the deposition of the polysilicon, performing wafer-to-wafer fusion bonding is difficult. The complex through-wafer interconnect fabrication steps degrade wafer surface smoothness; therefore, an expensive chemical-mechanical polishing step is required to get bondable surface quality in terms of roughness [26]. Furthermore, these steps add stress to the wafer, which results in a reduced radius of curvature. To date, no successful through-wafer via fabrication technique has been demonstrated that is compatible with the wafer-bonding technique of making CMUTs. On the other hand, the fabrication process for CMUTs with frameless trench isolation, which we previously reported, is significantly simpler than through-wafer via process [25]. In that implementation, a carrier wafer is required during the deep reactive ion etching (DRIE) and the chip-to-chip bonding steps to provide mechanical support for the membranes. This particular requirement presents drawbacks in the fabrication process. Good adhesion between the carrier wafer and the membrane surface is required for adequate mechanical support for the membranes. However, it is then a challenge to separate the carrier wafer and the membrane after the chip-to-chip bonding. The adhesive material can swell in the solvent and, therefore, create stress that can break the CMUT membranes. Thus, it is highly desired to eliminate the need of the carrier wafer for the trench isolation process.

In this paper, we present the design, fabrication, and characterization of wafer-bonded 2-D CMUT arrays incorporating through-wafer trench-isolated interconnects with a supporting frame. The framed trench isolation method preserves the advantages of the frameless trench isolation process, such as small series resistance, low parasitic capacitance, and simple fabrication. More importantly, it solves the device yield issue. It is therefore an important enabling technology for the advancement of CMUTs, in particular for 2-D array realizations based on direct wafer bonding. In the following sections, we explain the design, fabrication, and test results of trench-isolated CMUT arrays with a supporting frame. We also demonstrate volumetric ultrasound imaging of a wire phantom using a 2-D CMUT array fabricated using the new technique and integrated with a custom-designed IC chip.

II. Design and Fabrication

Two-dimensional CMUT arrays with 16 × 16 elements were designed and fabricated based on the technique of trench isolation with a supporting frame. Two different element pitches were included in the design: 250 μm and 185 μm. The target center frequency is 5 MHz for the 250 μm device and 10 MHz for the 185 μm device. These arrays are intended to be integrated into prototype volumetric medical ultrasound imaging systems [6]. The following subsections explain in detail the design approach and the fabrication process.

A. Design

In a 2-D array featuring through-wafer trench-isolated interconnects, neighboring array elements, which are built on an silicon-on-insulator (SOI) wafer, are separated by trenches on both the device layer and the bulk silicon side. Electrical continuity between the CMUT device layer and the bulk silicon is provided by a small contact via at the center of each element. Back-side electrodes are made of highly conductive silicon. A silicon frame structure is embedded in the back-side isolation trenches to provide the required mechanical support; see Fig. 1(a). For comparison, through-wafer via and frameless trench isolation are illustrated in Figs. 1(b) and 1(c), respectively.

In general, the figures of merit for through-wafer interconnects include small series resistance, low parasitic capacitance, and compatibility with device fabrication. For CMUTs, the interconnect resistance should be sufficiently smaller than the CMUT element impedance for efficient power delivery and for improved noise performance on receive. The parasitic capacitance needs to be low compared with the CMUT device capacitance to minimize impact on device sensitivity. Another desired feature for through-wafer interconnects is that the fabrication should be compatible with the preferred method of making CMUTs, i.e., direct wafer bonding. These desired features are achievable in the through-wafer trench isolated interconnects with a supporting frame.

The series interconnect resistance can be reduced by using a highly doped silicon substrate. As an example, for a 250 μm by 250 μm 2-D array element that has a 40 μm wide frame structure with a 40 μm wide trench, the interconnect resistance as a function of the silicon wafer resistivity is calculated to be just a few ohms if the silicon wafer resistivity is below 0.05 Ω-cm; see Fig. 2(a). SOI wafers with these types of silicon bulk layers are readily available.

There are 2 contributors to the interconnect parasitic capacitance: the overlapping areas between the device layer (signal) and the frame (ground)—C_1 Fig. 1(a)—and the trench isolation between the back side electrode (signal) and the frame (ground)—C_2 Fig. 1(a). Because 1) the buried oxide (BOX) layer has a higher relative dielectric constant ($\varepsilon_{ox} = 3.97$ vs. $\varepsilon_{air} = 1$ [27]), and 2) the BOX layer is thinner than the isolation trenches (a few microns vs. tens

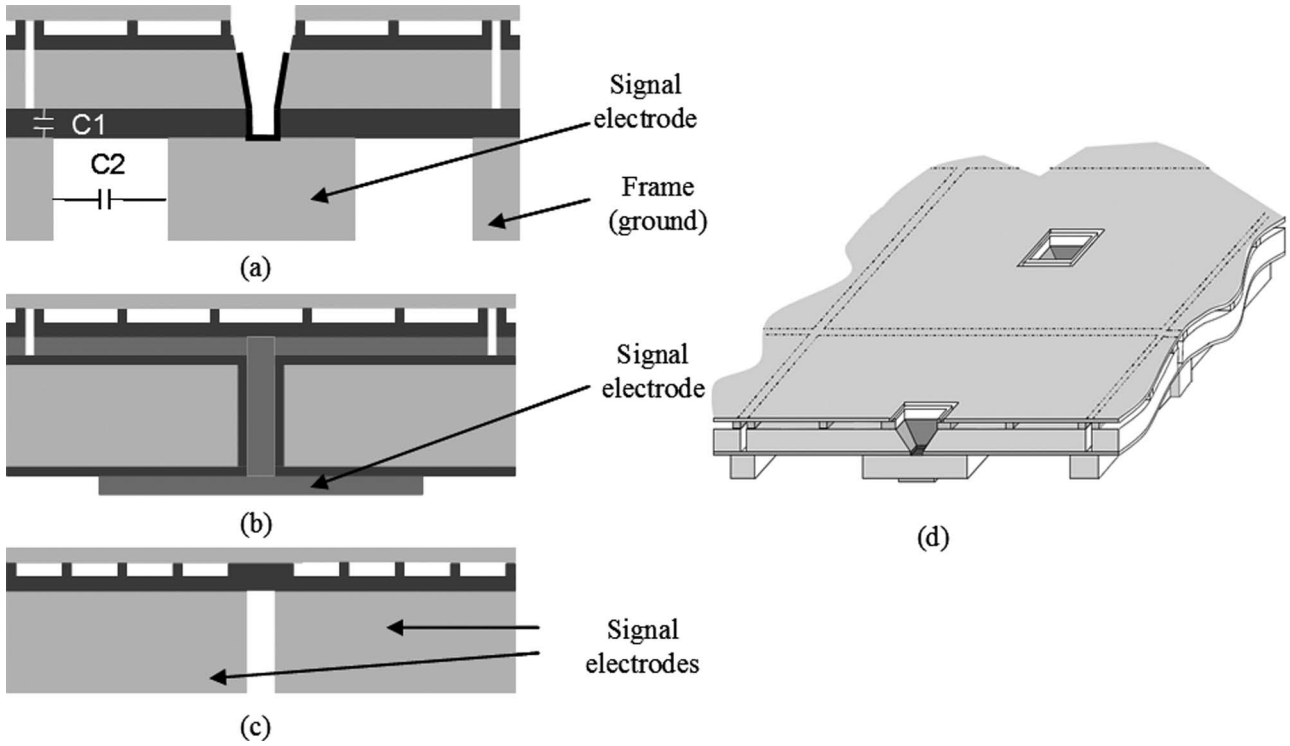


Fig. 1. Simplified cross-sectional diagrams illustrating (a) through-wafer trench-isolated interconnect with a supporting frame, (b) through-wafer via interconnect, (c) through-wafer trench-isolated interconnect without supporting frame, and (d) 3-D diagram of trench-isolated CMUT with a supporting frame. In (a), C_1 is due to the overlapping of the CMUT device layer and the silicon supporting frame; C_2 is due to the isolation trench. The membrane and the supporting frame are connected to ground (not shown in the figures).

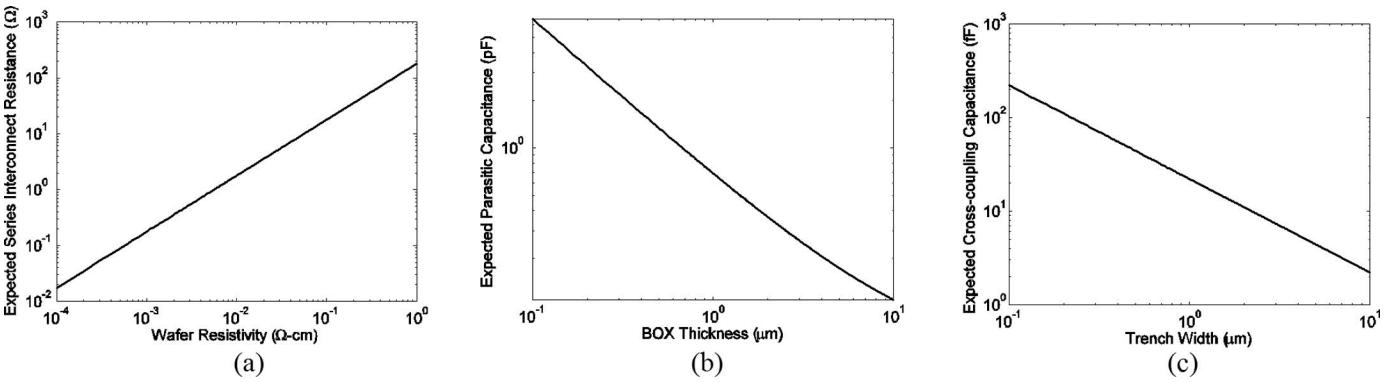


Fig. 2. (a) Expected series resistance, (b) expected parasitic capacitance, and (c) expected cross-coupling capacitance.

of microns), the overlapping areas are the dominant sources for parasitic capacitance. Therefore, an increased BOX layer thickness and a decreased frame width are desired for a reduced parasitic capacitance. There is a tradeoff in the frame width between parasitic capacitance and structural rigidity: the wider the frame, the better the supporting structural rigidity, but at the same time, the higher the parasitic capacitance. Another limitation of the frame width comes from fabrication considerations; a reasonably wide frame is required to account for the alignment inaccuracies. A frame as narrow as 40 μm was experimentally shown to provide sufficient mechanical support. At the same time, this frame is wide enough to accommodate all process uncertainties. Therefore, assuming a 40 μm wide frame, the total parasitic capacitance as a function of the BOX layer thickness is calculated for a 250 μm by 250 μm element; see Fig. 2(b). This calculation indicates that if a BOX layer of 2 μm, or thicker, is used; the parasitic capacitance can be reduced to be less than 0.4 pF. Compared with a typical device capacitance of ~2 pF for such an element, this is a good compromise (<20%).

The trench width is limited by fabrication considerations. The smallest trench width is limited by the aspect ratio achievable by the DRIE process used for the anisotropic etching of silicon. In the DRIE recipe used for this work, an aspect ratio of ~20 can be achieved. For a 300 μm thick silicon substrate, for example, the trench should be designed to be wider than 15 μm. It is desired to have a

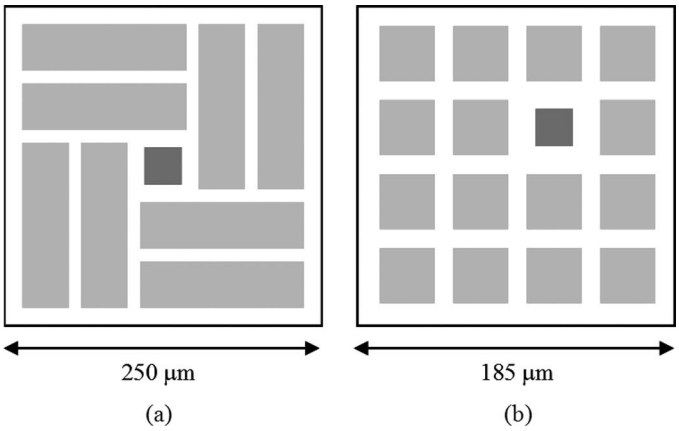


Fig. 3. CMUT cell layouts for (a) design 1 and (b) design 2. The light shade denotes membranes; the dark shade denotes contact vias.

TABLE I. DESIGN PARAMETERS.

	Design 1	Design 2
Number of elements	256 (16 × 16)	256 (16 × 16)
Element pitch (μm)	250	185
Number of membranes per element	8	15
Insulating layer thickness (μm)	0.3	0.3
Vacuum cavity height (μm)	0.15	0.15
Membrane width (μm)	40	28
Membrane length (μm)	133	28
Membrane thickness (μm)	1.4	1.0
Device layer thickness (μm)	10	10
Silicon substrate thickness (μm)	300	300
Front side trench width (μm)	4	4
Backside trench width (μm)	40	30
Frame width (μm)	40	40

wide trench for low parasitic capacitance, but the benefit of a wider trench will be marginal in terms of parasitic capacitance once it reaches a certain value. On the other hand, the trench width influences the interconnect impedance. This is because wider trenches mean narrower silicon pillars for the interconnects. Taking all the above tradeoffs into consideration, a reasonable trench width in the range 30 to 40 μm is recommended.

The front side isolation trenches contribute to the element-to-element electrical crosstalk and also influence the device fill factor; wider trenches suppress electrical crosstalk better, but also reduce the fill factor. A straightforward calculation, as shown in Fig. 2(c), suggests that the cross-coupling capacitance is negligible regardless of the trench width. Therefore, a narrow trench that is within the limit of the fabrication capability can be chosen. The photo masks used for the contact lithography (Image Technology, Inc., Palo Alto, CA) have a minimum resolution of 2 μm. Including a chosen safety margin, we decided that a reasonable front side trench width would be ∼5 μm.

Extensive literature exists on modeling CMUTs using both analytical [28], [29] and numerical methods [16], [30]–[36]. We used a MATLAB (MathWorks, Natick, MA) script [37] to aid the design of the CMUT arrays to have target center frequencies of 5 MHz and 10 MHz. This script is based on the equivalent circuit model [38], [39] that also includes the mass loading effect due to the liquid columns in front of the membranes [29]. The designs assumed a silicon membrane, and a silicon dioxide insulation layer in the cavity, both of which can be reliably made in our clean room facility using direct wafer bonding. Rectangular and square-shaped membranes are used over other membrane shapes to achieve high device fill factor. In the 250 μm pitch design, each element consists of 8 rectangular cells, as shown in Fig. 3(a); in the 185 μm pitch design, 15 square cells per element are used, as shown in Fig. 3(b). The electrical contact vias are located at the center of each element. In the square membrane designs, the via occupies the location of one membrane per element. Key design parameters are listed in Table I.

B. Fabrication

The CMUT elements are first fabricated on an SOI wafer with a 10 μm thick silicon device layer. Then, the electrical contact vias are formed in each element. In a subsequent fabrication step, the back-side isolation trenches and the embedded silicon supporting frame are fabricated simultaneously. The detailed fabrication steps are described below (Fig. 4).

CMUT cavities were first defined on the device layer of a double-side-polished SOI wafer using thermal oxidation and buffered oxide etching (BOE) techniques; see Fig. 4(a). The front electrical pads were then electrically divided in a DRIE step; see Fig. 4(b). Then another SOI wafer with a 1.0 μm or 1.4 μm thick device layer was fusion bonded to the device side of the first SOI wafer and annealed at 1000°C for 30 min; see Fig. 4(c). The handle wafer of the second SOI wafer was removed in a heated tetramethylammonium hydroxide (TMAH) solution; see Fig. 4(d) [40]. Contact vias were then opened in the middle of each element. Two etching techniques were used for forming the vias. The first technique was based on wet etching of silicon in heated potassium hydroxide (KOH) solution using the BOX layer of the second SOI wafer as the hard mask. It resulted in a 54.7° tapered slope on the side walls, a well-known characteristic of this wet etching technique for Si [41]. The second technique was based on DRIE using the Bosch process [42]. An inductively coupled plasma etcher (Multiplex ICP Etcher; Surface Technology Systems, Newport, UK) was used to achieve vertical side walls. Straight side walls result in smaller vias for the same contact area to the device silicon layer. Therefore, they are preferred in situations where small vias are critical due to device size constraints. In both cases, the BOX layer underneath the device layer acted as etch stop. A dry plasma etcher (AMT 8100 plasma etcher; Applied Materials, Santa Clara, CA) was used to remove the recessed BOX layer in the via region; see Fig. 4(e).

Then the contact vias were heavily doped by diffusion with phosphorus dopant to achieve doping levels required for Ohmic contact. This process was performed at atmospheric pressure at 1000°C for one hour in a furnace (Tylan; Tystar Corporation, Torrance, CA). Phosphorus oxy-

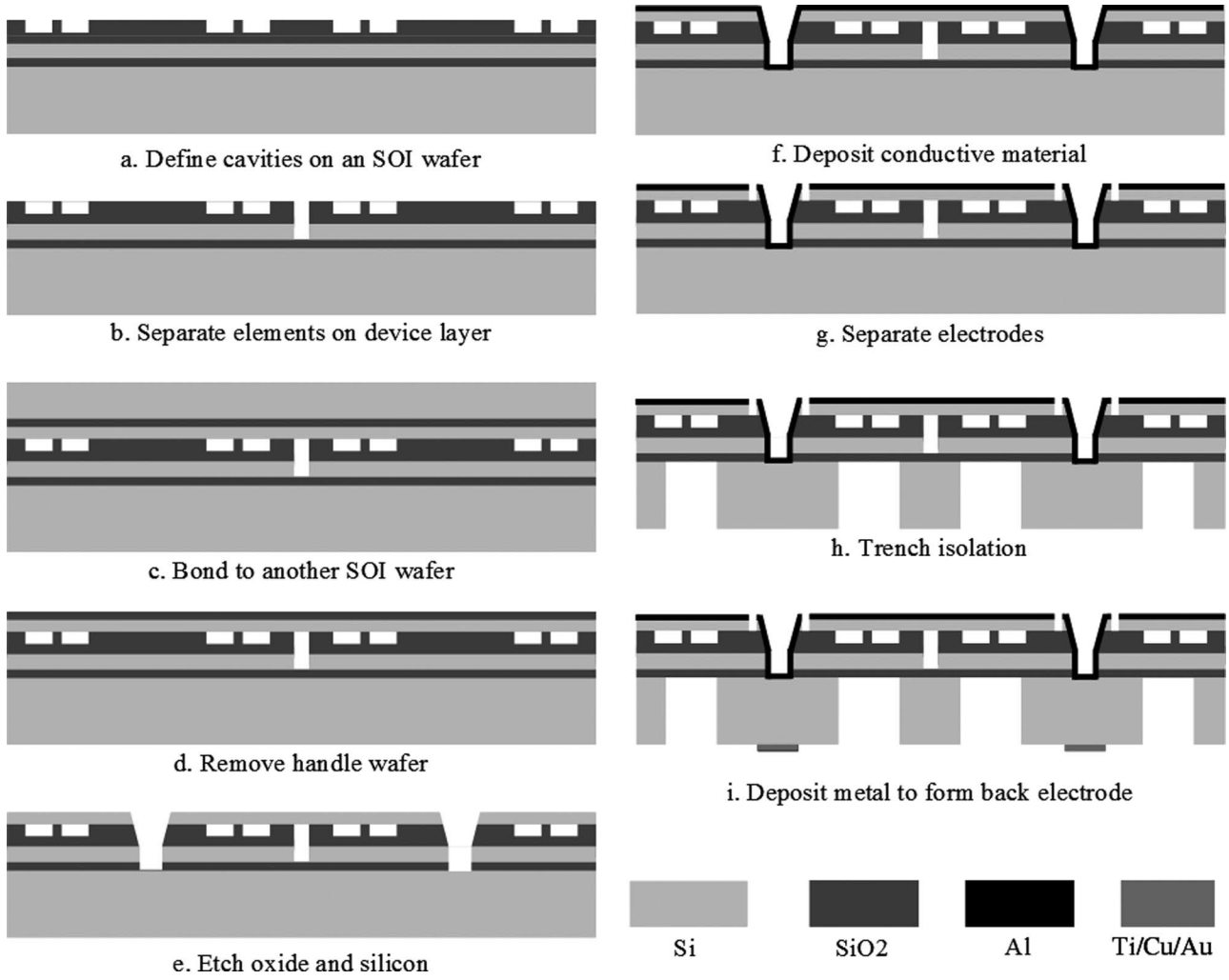
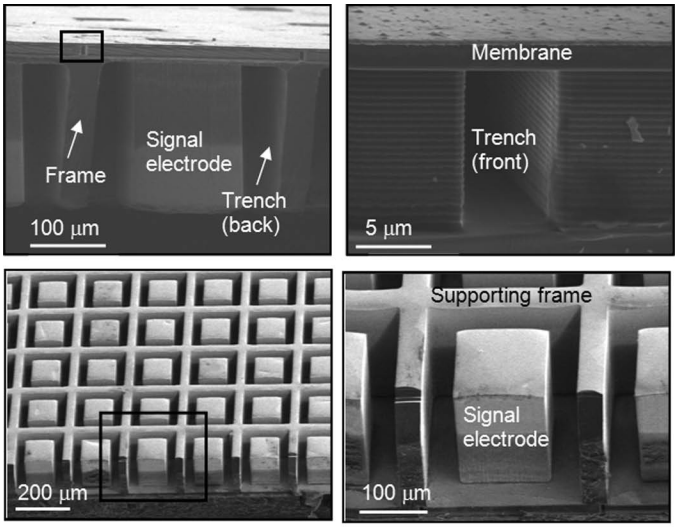


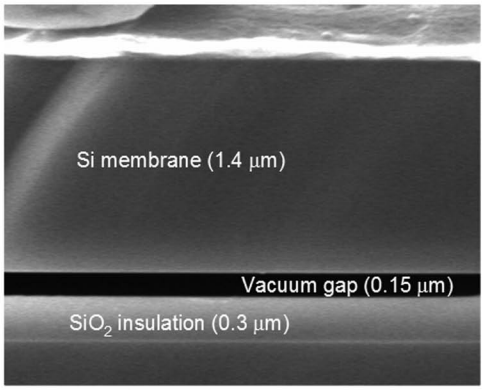
Fig. 4. Illustration of the fabrication process.

chloride gas ($POCl_3$) was used to provide the phosphorus atoms as dopants. After diffusion, the wafer was annealed at 1000°C in a nitrogen environment for one hour. The resulting dopant concentration was calculated to be $10^{20}/cm^3$ at the silicon surface using a semiconductor process simulator (TSUPREM4; Synopsis Inc., Mountain View, CA). A conformal deposition of a conductive material was needed in the contact via to provide electrical continuity between the CMUT device layer and the silicon substrate. We used sputtered aluminum as such a material for the wet-etched vias and highly doped polysilicon for the dry-etched vias; see Fig. 4(f). The aluminum sputtering was at 40°C, and no post annealing was performed. At a doping level of $10^{20}/cm^3$, Ohmic contact to aluminum is achieved through the carrier tunneling process [27]. The CMUT membranes were then remetallized with aluminum, and the vias were electrically separated from the membranes by etching away the silicon membranes surrounding the vias; see Fig. 4(g).

The silicon substrate was thinned down from the back side to 300 μm ± 10 μm (not shown in Fig. 4). For wafer thinning, first the wafer back side was lapped with aluminum oxide slurry. The aluminum oxide particle size is about 15 μm. A polishing step using colloidal silica slurry then followed to achieve a mirror finish. The particle size of the colloidal silica is ~20 nm. For 4-inch wafers, a thickness of >250 μm is recommended for wafer handling. Thinning down the silicon substrate reduced the series resistance and parasitic capacitance. Furthermore, this resulted in shortened back-side trench etching time. A 7-μm-thick photo resist layer (SPR 220–7; Shipley Company, L.L.C., Marlborough, MA) was spin-coated onto the back side of the SOI wafer and patterned. The signal electrodes and the supporting frames were then formed in a single DRIE etching step; see Fig. 4(h). The BOX layer of the SOI wafer acted as etch stop. A layer of Ti/Cu/Au was evaporated onto the electrodes to enhance the electrical contact to silicon and as an under bump metallurgy (UBM) layer for subsequent chip-to-chip bonding; see Fig. 4(i). During evaporation, the wafer was tilted 45° to prevent continuous metal coverage in the trenches that can electrically short neighboring elements. The CMUT arrays were then diced from the wafer and chip-to-chip bonded to a printed circuit board (PCB) or an IC. For chip-to-chip bonding, first, eutectic Sn/Pb solder balls with a diameter of 80 μm were jetted onto the bond pads on the IC chip



(a)



(b)

Fig. 5. (a) SEM pictures show the trench and frame structures. (b) Good control over the membrane thickness as well as vacuum gap height is achieved.

(Pac Tech USA Inc., Santa Clara, CA). The CMUT and IC were then aligned in a flip-chip bonder. The chip-to-chip assembly was then placed in an inert atmosphere furnace and the temperature was elevated to 220°C for solder reflow. The front and back side isolation trenches, as well as other features of the finished devices, are shown in the SEM photographs in Fig. 5.

III. Results and Discussion

A. Characterization in Air

Design 1 devices were characterized in air. The following parameters were measured: series resistance of the through-wafer interconnects, parasitic capacitance due to the frame structure, electrical crosstalk between the array elements, and electrical input impedance of the CMUT elements.

The series resistance of the contact vias was measured using a semiconductor parameter analyzer (Model 4145B; Hewlett-Packard Company, Palo Alto, CA). The resistance was measured on 6 dies. The average resistance is 6.6 Ω, with a maximum of 7.2 Ω, and a minimum resistance of 6.2 Ω. It is a smaller resistance compared with the 20 Ω resistance of a through-wafer via with doped polysilicon that the authors previously fabricated [6]. It is insignificant compared with the several kΩ device impedance of a 2-D array CMUT element.

The parasitic capacitance was measured on a dedicated test device identical to the regular device but without CMUT cells. Using a network analyzer (Model 8751; Hewlett-Packard Company, Palo Alto, CA), the parasitic capacitance was measured as 0.22 pF, slightly larger than the calculated value of 0.19 pF. For the calculation, the fringing capacitances were neglected. The parasitic capacitance is small compared with the ~2 pF CMUT device capacitance.

The electrical crosstalk was measured by exciting an array element with a 10 V, 10 ns unipolar pulse and detecting the received signal from neighboring elements at the same instant. Careful electrical shielding was provided between the excitation and receiving electrical traces to suppress the external electrical crosstalk. The received signal was 65 dB lower than the excitation signal. The silicon supporting frame that is embedded between the signal electrodes is electrically grounded. Therefore, it provides electrical shielding, which is the main reason for such excellent electrical crosstalk suppression.

The electrical input impedance in air was measured by probing (Model ACP40-W-GS-150; Cascade Microtech, Inc., Beaverton, OR) the electrodes on the back side of the wafer using an impedance analyzer (Model 8751; Hewlett-Packard Company, Palo Alto, CA). All 256 elements were functional (100% element yield). Across the array, the resonant frequency is uniform; see Fig. 6(a). The mean resonant frequency is 7.32 MHz and the standard deviation is 0.04 MHz. For comparison, after chip-to-chip bonding to a custom IC, the measured mean resonant frequency is 7.35 MHz with a standard deviation of 0.03 MHz; see Fig. 6(b). Therefore, chip-to-chip bonding had a small impact on device performance. Variability in die-to-die resonant frequency is small as measured in 12 arrays, with a mean of 7.33 MHz and a standard deviation of 0.04 MHz; see Fig. 6(c).

B. Characterization in Immersion

Both design 1 and design 2 devices were tested in soybean oil. Soybean oil is a nonconductive medium and was used because the CMUT surface was not electrically passivated in these experiments. Parylene and polydimethylsiloxane (PDMS) can be used to passivate the CMUT surface for testing in water [5], [43]. A reliable coating method of PDMS on CMUTs is currently under investigation to enable testing of CMUTs in water.

In immersion tests, first, pulse-echo experiments were performed on a design 1 device. In these experiments, the oil-air interface located 6 mm away from the transducer surface was used as a plane reflector. The received waveform and its Fourier transform, after correcting for dif-

fraction and attenuation losses, are shown in Fig. 7(a) and 7(b). The measurement showed a center frequency of 4.9 MHz, and a fractional bandwidth of 92%. Across the array, the pulse-echo amplitude varied slightly; see Fig. 7(c). The mean is 0.84 after normalizing to the highest pulse-echo amplitude, with a standard deviation of 6.6%. A significant portion of the nonuniformity comes from the edge elements. These elements have different boundary conditions and exhibit different characteristics than the inner elements. For this reason, dummy elements can be included in an ultrasound transducer array for medical imaging applications to improve uniformity [44]. If just the inner 14 × 14 elements are considered, the standard deviation of the pulse-echo amplitude further decreases to 4.4%. A comparable 2-D CMUT array fabricated with surface micromachining technique, reported previously [45], has a normalized mean of 0.35, and a standard deviation of 34%. It is evident from these measurements that wafer-bonded CMUTs feature improved device uniformity.

A design 2 device was measured in soybean oil with a hydrophone (model HNP-0400; Onda Corporation, Sunnyvale CA), calibrated in the frequency range from 1 to 20 MHz. The hydrophone was placed 4.5 mm away from the transducer surface. The hydrophone measurement showed a center frequency of 7.6 MHz and a fractional bandwidth of 95%; see Fig. 8(a) and (b). The expected band shape, calculated based on an equivalent circuit model [46], [47], is also shown in Fig. 8(b). The output pressure on the transducer surface was calculated by compensating the diffraction and attenuation losses due to the medium, which at 7.6 MHz were determined to be 30 dB [6]. The output pressure increased as the DC bias or the AC excitation voltage was increased; see Fig. 8(c). The maximum peak-to-peak output pressure was 2.9 MPa at the transducer surface, when biased at 80 V_{DC}, and excited by a 20 ns, 80 V unipolar pulse. Therefore, this device features both a wide fractional bandwidth and a high output pressure.

C. 3-D Ultrasound Imaging

Using a wire phantom, 3-D imaging experiments were performed. The wire phantom was constructed using 150 μm diameter fishing wires with a minimum spacing of 800 μm. A 2-D CMUT array (design 1) was chip-to-chip bonded to a custom designed IC; see Fig. 9(a). After chip-to-chip bonding, all 256 elements were functional. The CMUT was placed at the bottom of an oil tank with the wire phantom placed overhead; see Fig. 9(b). Details of the IC design and image reconstruction can be found in [45]. A single element transmits and receives at a time, and all 256 elements were sampled sequentially, controlled by a PC. A-scans were acquired using a digitizing oscilloscope (Model 54825; Agilent Technologies, Palo Alto, CA) at a sampling rate of 100 MS/s with a resolution of 8 bits. The RF data were stored in a hard drive. The image was reconstructed offline using classical synthetic aperture (CSA) beamforming on the RF data [6]. The 3-D rendered ultrasound image with a dynamic range of −25 dB was

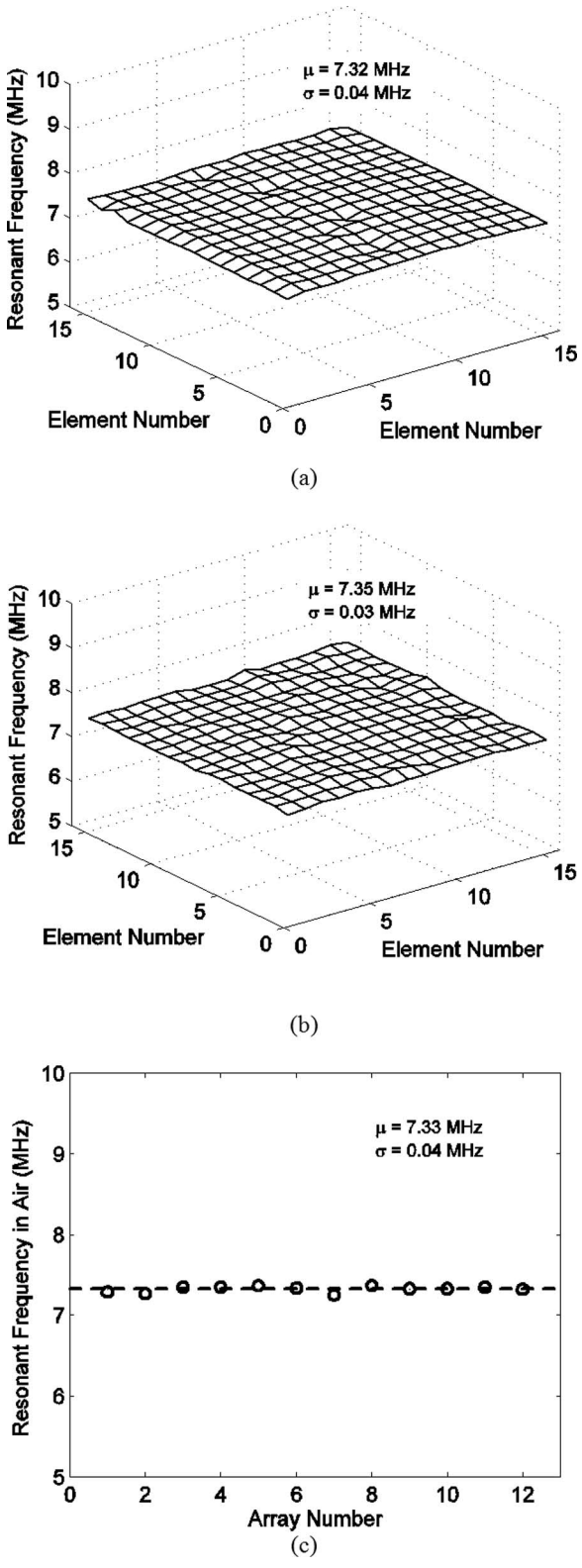


Fig. 6. Resonant frequency distribution across a 16 × 16-element 2-D array: (a) before chip-to-chip bonding, (b) after chip-to-chip bonding, and (c) across 12 arrays.

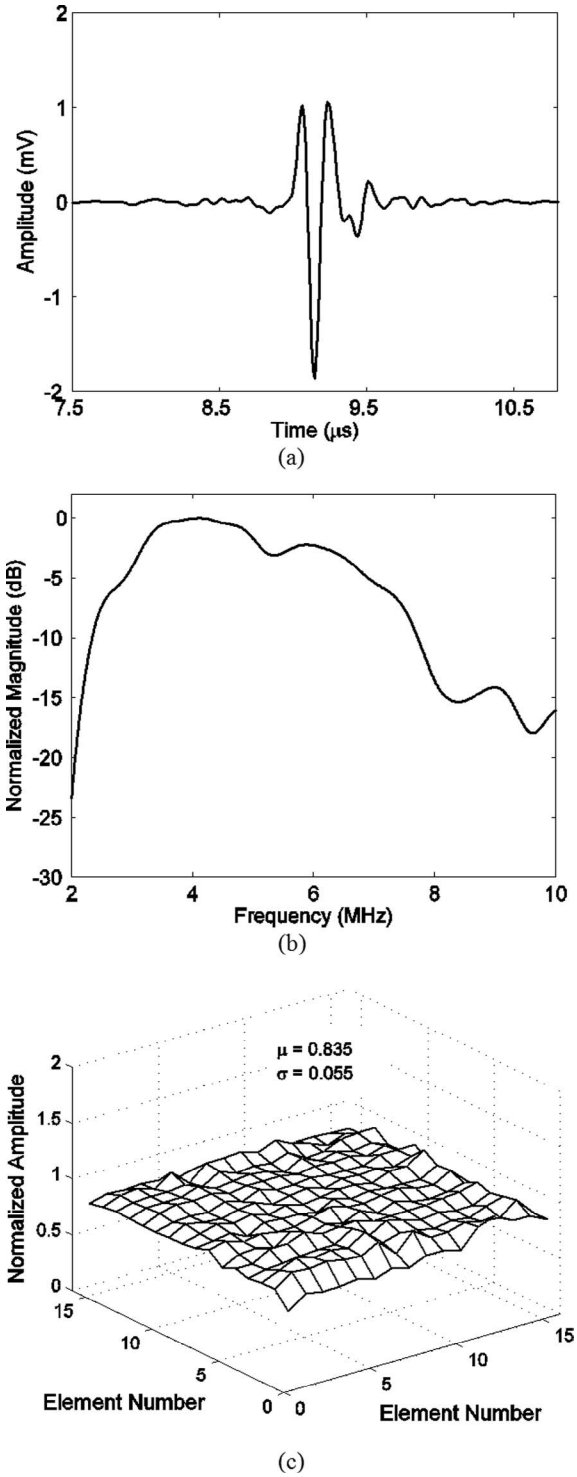


Fig. 7. (a) Received pulse-echo waveform, (b) pulse-echo spectrum, and (c) pulse-echo amplitude distribution across the array.

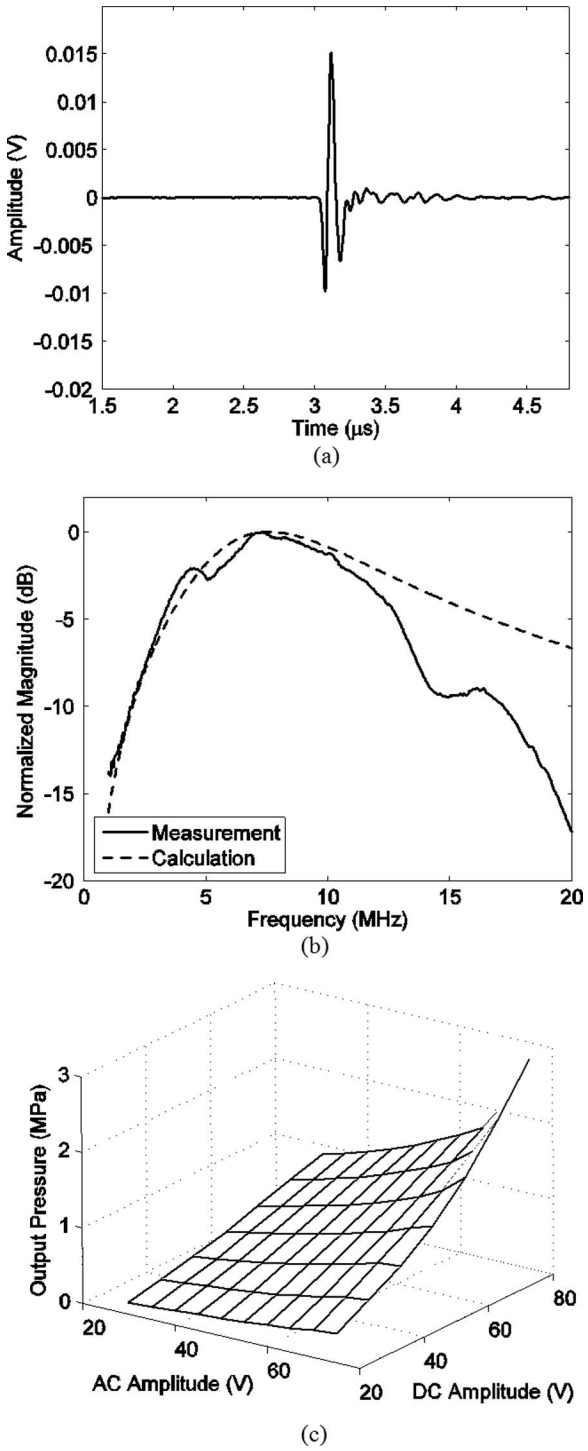


Fig. 8. (a) Waveform received by the hydrophone, (b) spectrum of the hydrophone reading, and (c) output pressure at the surface of the transducer for various DC bias and AC excitation voltages.

obtained using an open-source medical imaging software [48]; see Fig. 9(c).

IV. Conclusion

A new through-wafer interconnect technique for CMUT arrays is introduced. This technique is based on through-wafer trench isolation with a supporting frame. The embedded silicon frame provides the mechanical support; therefore, no carrier wafer is needed during the fabrication process. The interconnect fabrication is compatible with the direct wafer bonding process for CMUTs. The overall process is simple, and the fabricated interconnects showed a series resistance that is much smaller than the device impedance and a parasitic capacitance that is insignificant when compared with the device capacitance.

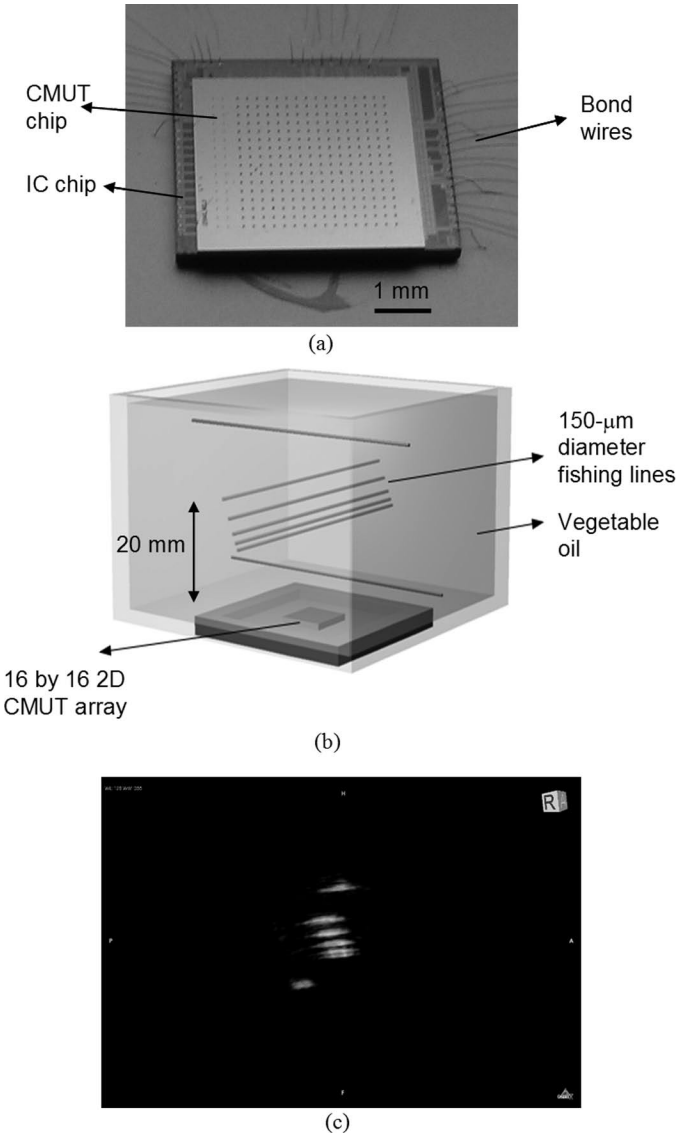


Fig. 9. (a) Photograph of 2-D array chip-to-chip bonded to an IC, (b) diagram of the wire phantom setup for the 3-D imaging experiment, and (c) 3-D ultrasound image of the wire phantom.

Electrical crosstalk between array elements is less than 65 dB, because the embedded silicon frame provides an electrical shielding between the silicon pillars. CMUT device performance is uniform, both in air (resonant frequency, $\sigma = 0.4\%$ of the mean), and in immersion (pulse-echo amplitude, $\sigma = 6.6\%$ of the mean). Wide fractional bandwidth of 95% and high peak-to-peak output pressure of 2.9 MPa were achieved on a 2-D array in immersion. After chip-to-chip bonding a 16×16 2-D CMUT array to an IC, all 256 elements were functional; 3-D ultrasound imaging of a wire phantom was demonstrated using a 2-D CMUT array chip-to-chip bonded to a custom-designed IC.

The presented interconnect technique can also be adopted for CMUT arrays with other configurations, e.g., 1-D arrays and annular ring arrays. Because the through-wafer trenches are fabricated after the formation of the CMUT membranes, this technique is also likely to be compatible with surface micromachining, which is a topic for our future work.

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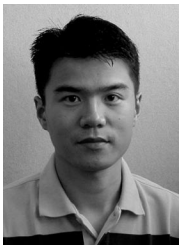


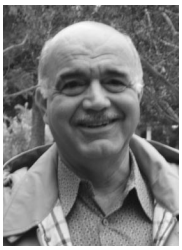
Xuefeng (Steve) Zhuang (S'02) received the B.S. degree from Louisiana State University (LSU), Baton Rouge, LA, in 2002, and the M.S. degree from Stanford University, Stanford, CA, in 2004, both in electrical engineering. He is currently pursuing a Ph.D. degree in electrical engineering at Stanford University. His research interests include micromachined sensors and actuators. His current research focuses on the new fabrication and packaging techniques for capacitive micromachined ultrasonic transducers. He won the LSU University Medal and the McLaughlin Dean's Medal (2002). He is a Stanford Graduate Fellow (2002). He is a student member of the IEEE and SPIE.

Ira O. Wygant received his B.S. degree in electrical engineering with a cross-college major in computer science from the University of Wyoming, Laramie, WY, in 1999. He received his M.S. degree in electrical engineering from Stanford University, Stanford, CA, in 2002. He is currently pursuing a Ph.D. degree in electrical engineering at Stanford University. Mr. Wygant has had internships with Oak Ridge National Laboratory, Oak Ridge, TN; Lucent Technologies, Reading, PA; and Agilent Laboratories, Palo Alto, CA. His research interests include integrated circuit design, ultrasound imaging, and MEMs fabrication as they relate to capacitive micromachined ultrasound transducers.

Der-Song Lin received the B.S. and M.S. degrees in civil engineering from National Taiwan University in 1995 and 1997, respectively, doing his master research on nondestructive evaluation. He also received an M.S. degree in mechanical engineering from Stanford University in 2006. He is currently working toward the Ph.D. degree in mechanical engineering at Stanford University, Stanford, CA. He worked as a consulting engineer at Sinotech Engineering Consultant Inc. from 1999 to 2001. He joined Redin International, Inc., as a special assistant to the CEO from 2001 to 2003. He is now working as a research assistant in E. L. Ginzton Laboratory, Stanford University. His research interests include MEMS technology, micromachined ultrasonic device, and medical device. Mr. Lin was a recipient of the National Ministry of Education Award, Taiwan, in 2004.

Mario Kupnik is currently a research associate in electrical engineering at Edward L. Ginzton Laboratory at Stanford University. He received his Ph.D. degree from the University of Leoben, Austria, in 2004, and the Diplom Ingenieur degree from Graz University of Technology, in 2000. From summer 1999 to October 2000, he worked as an analog design engineer for Infineon Technologies AG, Graz, on the design of ferroelectric memories and contactless smart card (RFID) systems. His present research interests include the design, modeling, fabrication, and application of micromachined sensors and actuators, with a main focus on capacitive micromachined ultrasonic transducers mainly for air-coupled applications, including high gas temperatures; for example, transit-time gas flowmeters for hot and pulsating gases, ultrasonic nondestructive evaluation using noncontact ultrasound, nonlinear acoustics, and biochemical gas-sensing applications (electronic nose). Dr. Kupnik has more than 5 years of teaching experience in the field of electrical engineering, and he is a member of the IEEE.

Ömer Oralkan received the B.S. degree from Bilkent University, Ankara, Turkey, in 1995, the M.S. degree from Clemson University, Clemson, SC, in 1997, and the Ph.D. degree from Stanford University, Stanford, CA, in 2004, all in electrical engineering. He joined the research staff at the E. L. Ginzton Laboratory of Stanford University in 2004 as an engineering research associate. He was promoted to the rank of senior research engineer in 2007. His past and present research interests include analog and digital circuit design, semiconductor device physics and fabrication, micromachined sensors and actuators, and medical imaging. His current research focuses on the design and implementation of integrated systems for catheter-based medical imaging applications, photoacoustic imaging, and chemical and biological sensor arrays. Dr. Oralkan has authored and co-authored more than 80 publications and received the 2002 Outstanding Paper Award of the IEEE Ultrasonics, Ferroelectrics, and Frequency Control Society. He is a member of the IEEE, SPIE, and AIUM.



Butrus (Pierre) T. Khuri-Yakub (S'70–S'73–M'76–SM'87–F'95) is a professor of electrical engineering at Stanford University. He received the B.S. degree in 1970 from the American University of Beirut, the M.S. degree in 1972 from Dartmouth College, and the Ph.D. degree in 1975 from Stanford University, all in electrical engineering. He was a research associate (1965–1978) and then senior research associate (1978–1982) at the E. L. Ginzton Laboratory of Stanford University and was promoted to the rank of professor of electrical engineering in 1982. His current research interests include medical ultrasound imaging and therapy, micromachined ultrasonic transducers, smart bio-fluidic channels, microphones, ultrasonic fluid ejectors, and ultrasonic nondestructive evaluation, imaging, and microscopy. He has authored more than 400 publications and has been principal inventor or co-inventor of 76 U.S. and international patents. He was awarded the Medal of the City of Bordeaux in 1983 for his contributions to nondestructive evaluation, the Distinguished Advisor Award of the School of Engineering at Stanford University in 1987, the Distinguished Lecturer Award of the IEEE UFFC Society in 1999, a Stanford University Outstanding Inventor Award in 2004, and a Distinguished Alumnus Award of the School of Engineering of the American University of Beirut in 2005.