# Integration of 2D CMUT Arrays with Front-End Electronics for Volumetric Ultrasound Imaging

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***Abstract*—For three-dimensional (3D) ultrasound imaging, connecting elements of a two-dimensional (2D) transducer array to the imaging system's front-end electronics is a challenge because of the large number of array elements and the small element size. To compactly connect the transducer array with electronics, we flip-chip bond a 2D 16 × 16-element capacitive micromachined ultrasonic transducer (CMUT) array to a custom-designed integrated circuit (IC). Through-wafer interconnects are used to connect the CMUT elements on the top side of the array with flip-chip bond pads on the back side. The IC provides a 25-V pulser and a transimpedance preamplifier to each element of the array. For each of three characterized devices, the element yield is excellent (99 to 100% of the elements are functional). Center frequencies range from 2.6 MHz to 5.1 MHz. For pulse-echo operation, the average −6-dB fractional bandwidth is as high as 125%. Transmit pressures normalized to the face of the transducer are as high as 339 kPa and input-referred receiver noise is typically 1.2 to 2.1 mPa/$\sqrt{\text{Hz}}$. The flip-chip bonded devices were used to acquire 3D synthetic aperture images of a wire-target phantom. Combining the transducer array and IC, as shown in this paper, allows for better utilization of large arrays, improves receive sensitivity, and may lead to new imaging techniques that depend on transducer arrays that are closely coupled to IC electronics.**

## I. Introduction

Three-dimensional (3D) ultrasound imaging provides important clinical benefits beyond those of traditional two-dimensional (2D) ultrasound imaging. With 3D ultrasound imaging, in addition to being able to acquire and display volumetric data, 2D cross-sectional scans can be obtained at arbitrary orientations relative to the transducer array, thus providing views of anatomy new to ultrasound imaging. Three-dimensional imaging also greatly increases the utility of analyzing images after the examination, potentially leading to less difficult and less expensive examinations [1].

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Three-dimensional ultrasound imaging is substantially more complex than 2D imaging. Fully populated, large-area 2D transducer arrays are desired for better signal-to-noise ratio (SNR) and improved image resolution. Spatial sampling of a 2D transducer aperture requires that the element pitch in both dimensions be less than about one-half the wavelength of ultrasound in tissue. The result is that 2D arrays can have a very large number of elements. For comparison, 1D arrays in current commercial systems commonly have 128 elements. A 128 × 128-element 2D array has 16,384 elements, which poses significant data processing and packaging challenges. Conventional 1D arrays can be connected to an external imaging system by matching to 50-Ω microcoaxial cables. However, even for a modestly sized 2D array, using cables and matching circuits would result in a bulky and complex system.

Because 2D array elements have limited size in both dimensions, they are usually much smaller than comparable 1D array elements. Their smaller size means they have a higher electrical impedance [2] and are thus more susceptible to parasitic capacitance. In a 1D array, the effects of parasitic cable capacitance can be avoided by electrically matching the transducer elements with the cables and terminating electronics [3]. However, because of the high equivalent impedance of the 2D array elements, broadband electrical matching is difficult.

A solution to interfacing electronics with 2D transducer arrays is to combine the transducer array with an integrated circuit (IC). A compact connection between an IC and a transducer array results in minimal parasitic capacitance and eliminates bulky cables. Implementing more of the system electronics with an IC can reduce the cost of 3D imaging systems. The functionality provided by the IC also enables a wealth of new imaging techniques that better utilize large arrays; examples include multiplexing the array over a limited number of cables or electronic channels [4], electronically reconfiguring the array for different element patterns [5], and implementing an analog-to-digital converter [6], [7] or beamformer [8] within the IC to reduce the number of connections with an external system.

With the IC presented here, we focus on preamplifiers and pulsers, as they are the basic circuit components of a pulse-echo imaging system. The IC preamplifiers are desired because they can be densely packed and located close to the transducer. Furthermore, they have low parasitic ca-

pacitance and can be custom-designed for a specific transducer design. The advantage of IC pulsers is that they can be provided to every element in the array without expensive external electronics or numerous cables. A drawback of IC pulsers is that they need to be implemented in a high-voltage process if their pulse voltages are to be comparable to those of external pulsers, which are routinely more than 100 V. The potentially lower voltage of IC pulsers can be compensated for by providing a greater number of them. By using more pulsers (with proper focusing delays), the goal of achieving a desired pressure at a given location in the tissue can be achieved with lower pulse voltages. Coded excitation [9] techniques can also be used to compensate for lower pulse voltages. An alternative to IC pulsers is to use high-voltage switches to route externally generated pulse voltages [10]. However, to switch very high voltages, a specialized IC process is needed which may not be ideal for implementation of the digital logic and preamplifiers. Externally provided pulses also require connecting cables.

Ultrasound transducer arrays closely coupled with ICs have been previously demonstrated; examples include a commercial 3D imaging system with electronics in the handle [11], micromachined transducers that are directly fabricated with electronics [10], [12]–[15], and a catheter-based system with CMOS ICs in the probe tip [16]. Additionally, a number of specially designed connectors have been shown [11], [17]–[22] for 2D arrays, which could lead to tighter integration of the transducer array with electronics. Studies focusing on front-end electronics for integration with micromachined transducer arrays include [23]–[25].

The approach to integration presented here is to flip-chip bond the IC directly to a capacitive micromachined ultrasonic transducer (CMUT) array. The CMUT array provides through-wafer interconnects that connect the transducer elements on the top side with flip-chip bond pads on the back side [26]. This approach provides a large number of densely packed connections and is relatively simple as it relies on industry-standard flip-chip bonding techniques and does not require a special interface connector. It also does not have the limitations imposed by fabricating the array on the IC, which include restrictions on the type of micromachining processes used to make the transducer array. For piezoelectric transducer arrays, directly flip-chip bonding to an IC is generally not an option as the dicing saw used to separate the elements would damage the IC. However, a piezoelectric array could be bonded to an intermediate connector, such as a flex circuit, which in turn could be flip-chip bonded to the IC. The simplicity of directly bonding to an IC is an advantage of using a CMUT array with through-wafer interconnects.

In this paper, we present the design and characterization of a $16 \times 16$-element 5-MHz CMUT array which is integrated with a custom-designed IC using flip-chip bonding (Fig. 1). With this device, we are targeting an intracavital ultrasound imaging application, although the design could be extended to different applications. Invasive 3D ultrasound imaging devices based on 2D piezoelectric transducer arrays are described in [27], [28]. In those works, the transducer arrays are connected with cables to a 3D imaging system with 512 transmitters and 256 receivers; real-time *in vivo* imaging results are presented that illustrate the utility of invasive 3D ultrasound imaging. Similarly designed probes would benefit from transducers integrated with electronics.

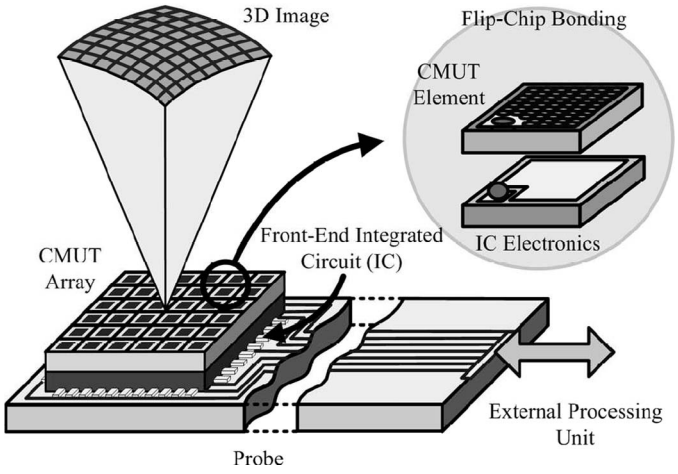


Fig. 1. Diagram of an imaging probe with a 2D CMUT array integrated with the front-end circuitry of an imaging system.

In the following sections, we present the fabrication of a $16 \times 16$-element CMUT array with through-wafer interconnects, techniques used to flip-chip bond the array to an IC, the IC design, characterization of the CMUT array and interconnects, and synthetic aperture imaging of a wire-target phantom.

## II. Design and Implementation

### A. CMUT Arrays

We designed and fabricated $16 \times 16$-element CMUT arrays with an element pitch of 250 $\mu$m to study combining a CMUT array with an IC and for application in intracavital ultrasound imaging.

For design of the CMUT membrane and cavity dimensions we used a combination of the CMUT equivalent circuit model [29], analytical calculations of membrane deflection [30], finite element modeling [31], and experimental data from past designs. Key parameters for the design are shown in Table I. Arrays with a range of membrane diameters and membrane thicknesses were fabricated to cover a range of frequencies and collapse voltages. The arrays were fabricated using a sacrificial layer etch process [32], [33], which is summarized in Fig. 2. Pictures of the fabricated arrays are shown in Fig. 3.

An element pitch of 250 $\mu$m was chosen to simplify the IC layout at the expense of increased grating lobes due to the greater than $\lambda/2$ element pitch. With a pitch of 250 $\mu$m, the circuitry and bond pad dedicated to an element fits into an area equal to the element area; thus, the bulk of the IC can consist of a $16 \times 16$ array of identical cells. In general, however, the IC does not restrict the

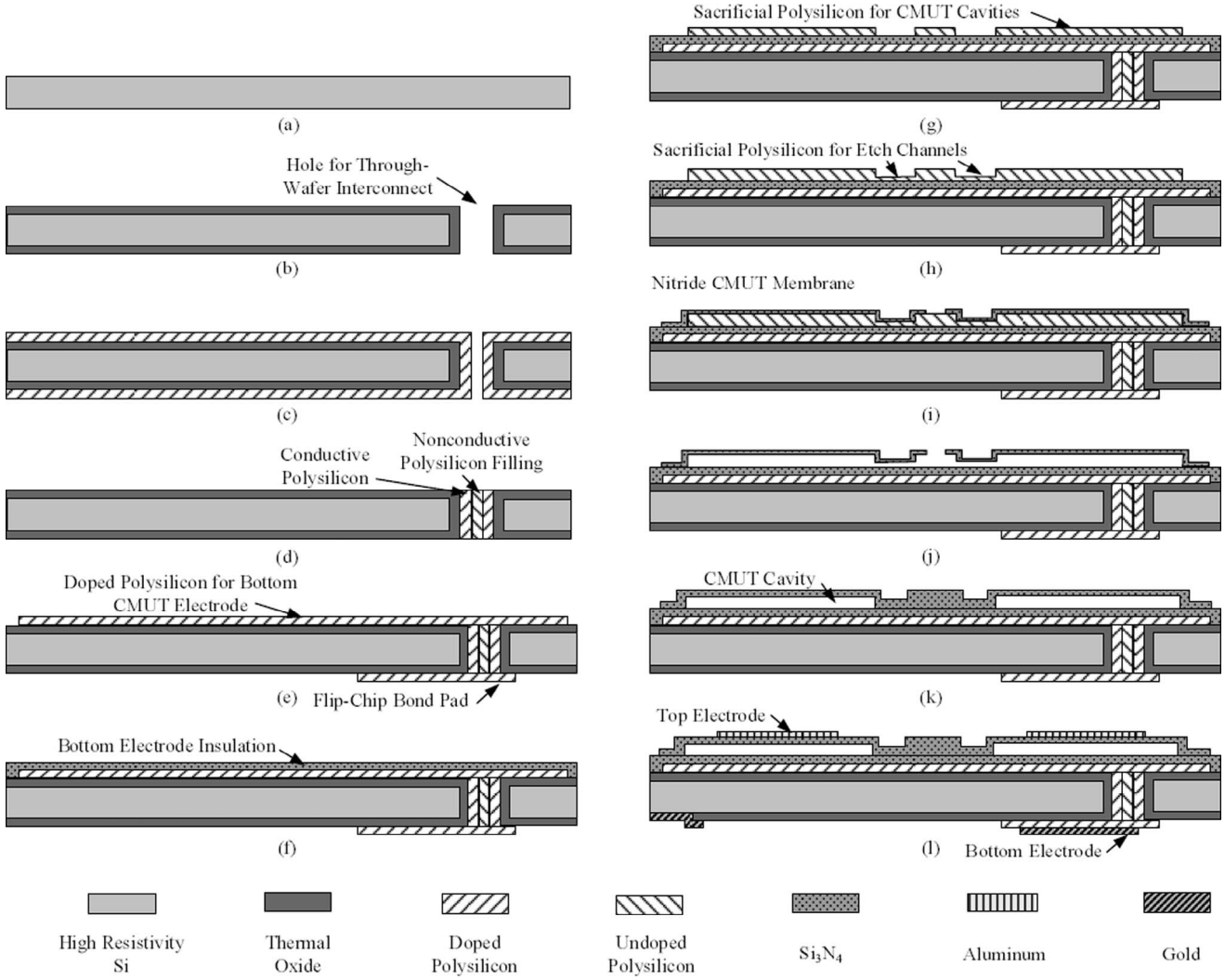


Fig. 2. Basic process flow used to fabricate the CMUTs. (a) The process starts with a high-resistivity silicon wafer. (b) To form the through-wafer interconnects, 20-$\mu$m diameter holes are etched through the wafer using deep reactive ion etching (DRIE). An oxide layer is grown to insulate the interconnects from the substrate. (c) Polysilicon is deposited and then doped to create the conductive parts of the through-wafer interconnects. (d) The vias are filled with undoped polysilicon. The polysilicon on the wafer surface is then etched back. (e) Polysilicon is redeposited, doped, and patterned to create the bottom electrode of the CMUTs and the flip-chip bond pad on the back side. (f) A nitride layer is deposited to insulate the bottom electrode. (g) CMUT cell cavity areas are defined. (h) Channels for the sacrificial etchant are defined. (i) A layer of nitride is deposited to form the membrane. Etch holes are opened. (j) The sacrificial layer is etched away to form the cavities. (k) The etch holes are sealed. (l) Gold is deposited and patterned for the top electrodes and flip-chip bond pads.

element pitch. The IC can be larger or smaller than the transducer array as long as the IC's flip-chip bond pads align with those of the transducer array.

Metal-insulator-semiconductor (MIS) through-wafer interconnects similar to those reported in [26] connect the CMUT elements on the top side of the wafer to flip-chip bond pads on the back side. The interconnects are fabricated in steps (a) through (e) of the process flow shown in Fig. 2. Cross sections of the interconnects are shown in Fig. 3(e) and (f). Interconnects based on pn-junctions have also been demonstrated for CMUTs [34]. Compared with pn-junction interconnects, MIS interconnects have slightly higher parasitic capacitance but can tolerate higher voltages and voltages of either polarity. To reduce the parasitic capacitance of the MIS interconnects, the arrays were fabricated using low-doped silicon wafers ($\rho > 10,000\ \Omega$-cm). As described in Section III-A, the capacitance of an interconnect is as low as 60 fF.

The dc bias voltage for the array is connected to flip-chip bond pads on the IC, which are connected to the top electrode of the array with through-wafer interconnects. The top electrode of the array is common to all of the elements and is used to bias the CMUTs. Fig. 4(b) shows how the bias voltage is applied. Resistor $R_b$ and capacitor $C_b$ are shared by all of the elements. Resistor $R_b$ is several hundred kilohms and serves to limit the current in case an element is shorted and to isolate the voltage supply. Capacitor $C_b$ is a large capacitor (hundreds of nanofarads or more) that filters out noise from the high-voltage supply and provides an ac ground for the transducer. On the back side of the array, the dc bias is connected to a grid of lines which connect to the silicon substrate [Fig. 3(c)]. As

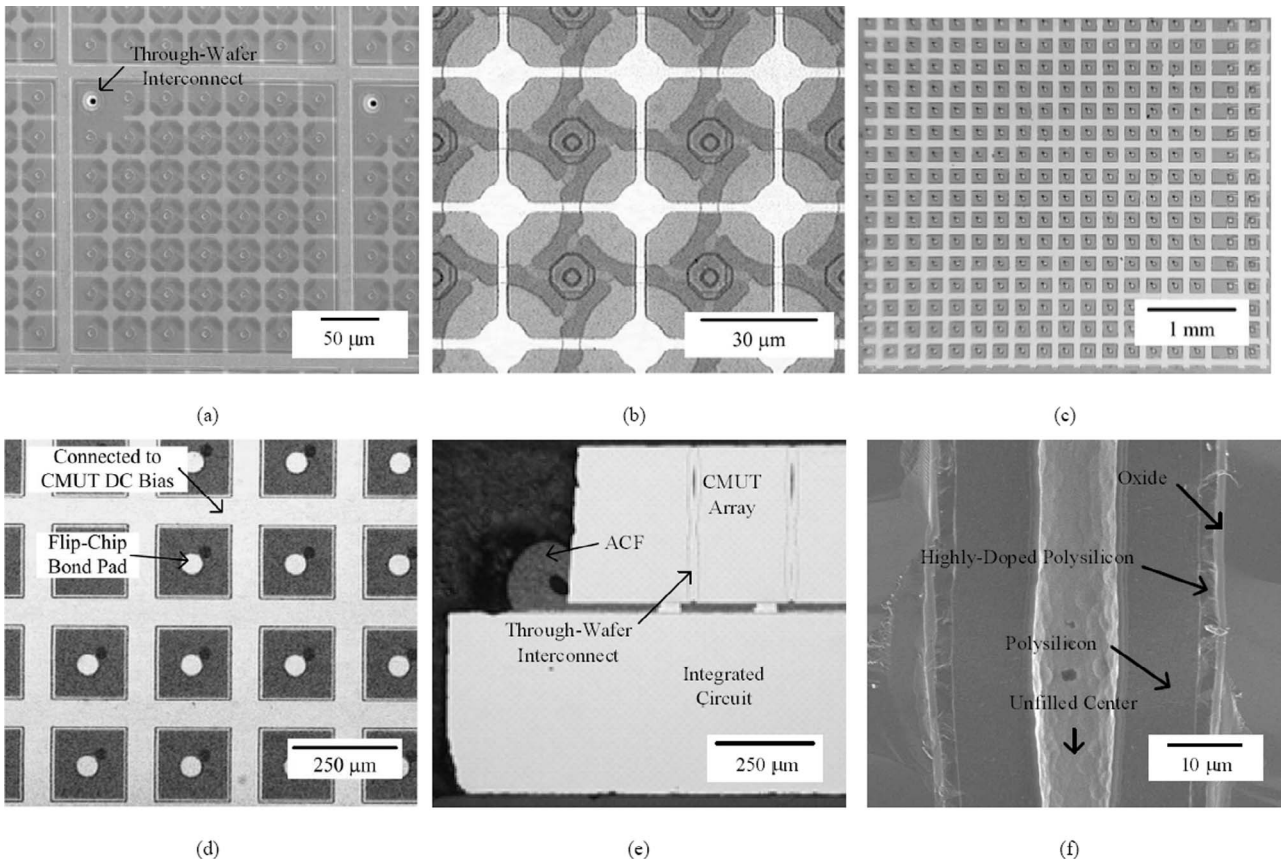


Fig. 3. Pictures and scanning electron micrographs (SEMs) of the CMUT array and through-wafer interconnects. (a) SEM of an individual 250-$\mu$m $\times$ 250-$\mu$m element. (b) Closeup of several 30-$\mu$m-diameter membranes. (c) Back side of the CMUT array. (d) Back side of several elements. (e) Cross section of a device flip-chip bonded using anisotropic conducting film (ACF). (f) SEM of the edge of a cleaved wafer showing a through-wafer via.

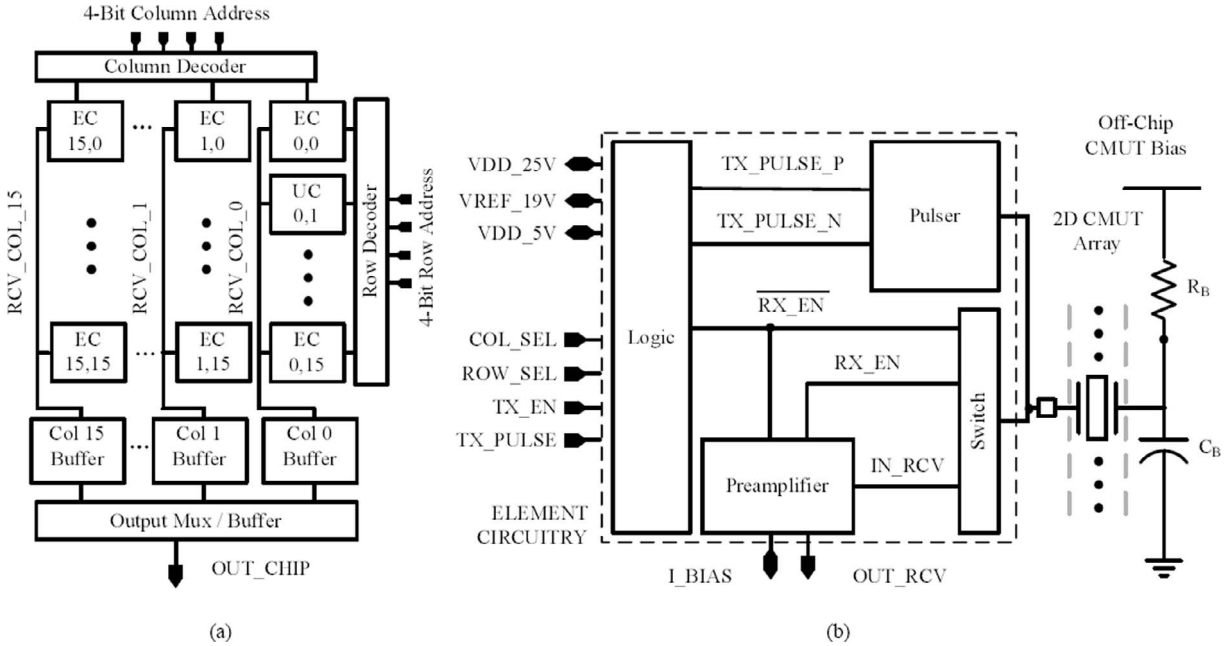


Fig. 4. Top-level circuit diagrams of the integrated circuit (IC). (a) Row and column decoders select a single element. All of the elements in a column share a single output buffer. (b) The IC provides each element with a pulser, preamplifier, high-voltage switch, and basic logic. The high-voltage switch protects the low voltage electronics of the amplifier during transmit. The logic controls the pulser state (high, low, or high impedance), switch, and amplifier power.

TABLE I
CMUT ARRAY PARAMETERS.

| | |
|---|---|
| Array size (elements) | $16 \times 16$ |
| Element pitch ($\mu$m) | 250 |
| CMUT membrane diameter ($\mu$m) | 24, 30, 36 |
| Number of membranes per element | 24, 35, 48 |
| Membrane thickness ($\mu$m) | 0.6, 0.5, 0.8 |
| Cavity thickness ($\mu$m) | 0.1 |
| Insulating layer thickness ($\mu$m) | 0.15 |
| Silicon substrate thickness ($\mu$m) | 400 |
| Flip-chip bond pad diameter ($\mu$m) | 50 |
| Through-wafer interconnect diameter ($\mu$m) | 20 |
| Silicon wafer resistivity ($\Omega$-cm) | $>10{,}000$ |

described in Section III-A, the silicon substrate is biased to reduce the parasitic capacitances of the through-wafer interconnect, the flip-chip bond pad, and the bottom electrode of the CMUT.

A drawback of applying dc bias voltage to the top electrode of the array is that it is applied to the side of the array which is exposed to the patient. Alternatively, the top electrode could be grounded and the voltage supplies for the IC shifted by the desired dc bias voltage.

### *B. Integrated Circuit with Pulsers and Preamplifiers*

The IC provides a transmit and receive circuit to every element of the array. This circuit consists of a pulser, a transimpedance amplifier, and a switch that protects the low-voltage amplifier electronics from the pulser's output. A circuit with the same basic topology was first implemented in a 2.5-V standard CMOS process [35]. For this work, we adapted those low-voltage circuits to a high-voltage process and made an array of circuits for imaging with a 2D array.

The circuitry dedicated to each transducer element is designed to occupy the same area as the element (250-$\mu$m $\times$ 250-$\mu$m). Each column of elements shares an output buffer which drives the load associated with the imaging system and connecting cables. The IC was designed for a high-voltage process (National Semiconductor, Santa Clara, CA). This process has two metal layers and a minimum feature size of 1.5 $\mu$m. Devices provided by the process include standard and high-voltage 1.5-$\mu$m CMOS devices, bipolar devices, and DMOS devices. For the pulser circuitry we use the high-voltage CMOS devices. For the remaining circuitry we use the standard CMOS devices.

To simplify the circuit design and data acquisition for this initial implementation of the electronics, the IC uses a single element at a time for transmit and receive. The active element is selected with four-bit row and column addresses. Although this design is simple compared to a multichannel system, the IC can be used for pulse-echo characterization of each element in the array and for real-time 3D synthetic-aperture imaging. The top-level design of the IC is illustrated in Fig. 4. Schematics of the pulser, preamplifier, and switch are shown in Fig. 5.

The timing of the transmit pulse and preamplifier startup is shown in Fig. 6. When the signal TX_EN [Fig. 5(d)] is high, the selected element is used to transmit: the preamplifier is turned off, the protection switch is opened, and the pulser output voltage is controlled by TX_PULSE. The duration of the TX_PULSE signal determines the duration of the output pulse. When TX_EN is low, then the selected element is used for receive: the preamplifier is turned on, the protection switch is closed, and the pulser output has a high impedance.

The receive circuitry uses a 5-V power supply and consumes 9 mW of power when an amplifier is enabled for receive. About 60% of the power is used by the enabled output buffer; the remainder is used by the enabled preamplifier. The power consumption was determined such that a 16-channel implementation of the IC would consume less than 150 mW, which is comparable to the 100-mW power limit given in [16] for an intravascular ultrasound IC.

To target low power or high channel count applications, the IC could be designed to consume less power per channel. Using the same IC process technology, the power consumption of the preamplifier could be reduced primarily at the expense of noise performance. Using a process with a lower supply voltage and finer features would reduce power consumption for both the preamplifier and buffer. Some buffer power could be saved by using a more efficient buffer circuit. More significantly, buffer power could be saved by reducing the total gain of the preamplifier and buffer. Ideally the gain of the preamplifier and buffer should be just large enough that the noise at the output of the buffer dominates the input-referred noise of the following stage. If the gain is any higher, the SNR for the system does not improve but the buffer consumes more power to swing larger voltages. In the IC presented, assuming the buffer drives the input of a typical ultrasound data acquisition system, the total preamplifier and buffer gain could be reduced without loss in SNR.

The pulser circuit [Fig. 5(a)] is based on the first stage of the pulser circuit described in [36]. High-voltage transistors MN1, MN1′, MP1, and MP1′ are used to increase the pulse voltage. The pulser's output is 25 V, 0 V, or high impedance, depending on the values of input signals IN_P and IN_N. The high impedance state is used during receive. The transistors of the pulser circuit are sized to provide pulses as short as 100 ns to a 2.5-pF load. The pulser occupies roughly one-third of the 250-$\mu$m $\times$ 250-$\mu$m IC area dedicated to each element.

The preamplifier circuit [Fig. 5(b)] is a transimpedance amplifier [37], [38] composed of a single-ended amplifier and a 430-k$\Omega$ feedback resistor. The single-ended amplifier consists of a common-source amplifier with a gain of $-100$ V/V followed by a source follower. A transimpedance amplifier acts as a current-to-voltage converter. It has a low input impedance which is well-suited for high-impedance sources [37]. The preamplifier was designed to have minimal noise, a bandwidth of 10 MHz, and a power consumption of 4 mW. For circuit simulations, the input to the amplifier was modeled with the CMUT equivalent circuit described in [29] with an additional parasitic capacitance of 1 pF.

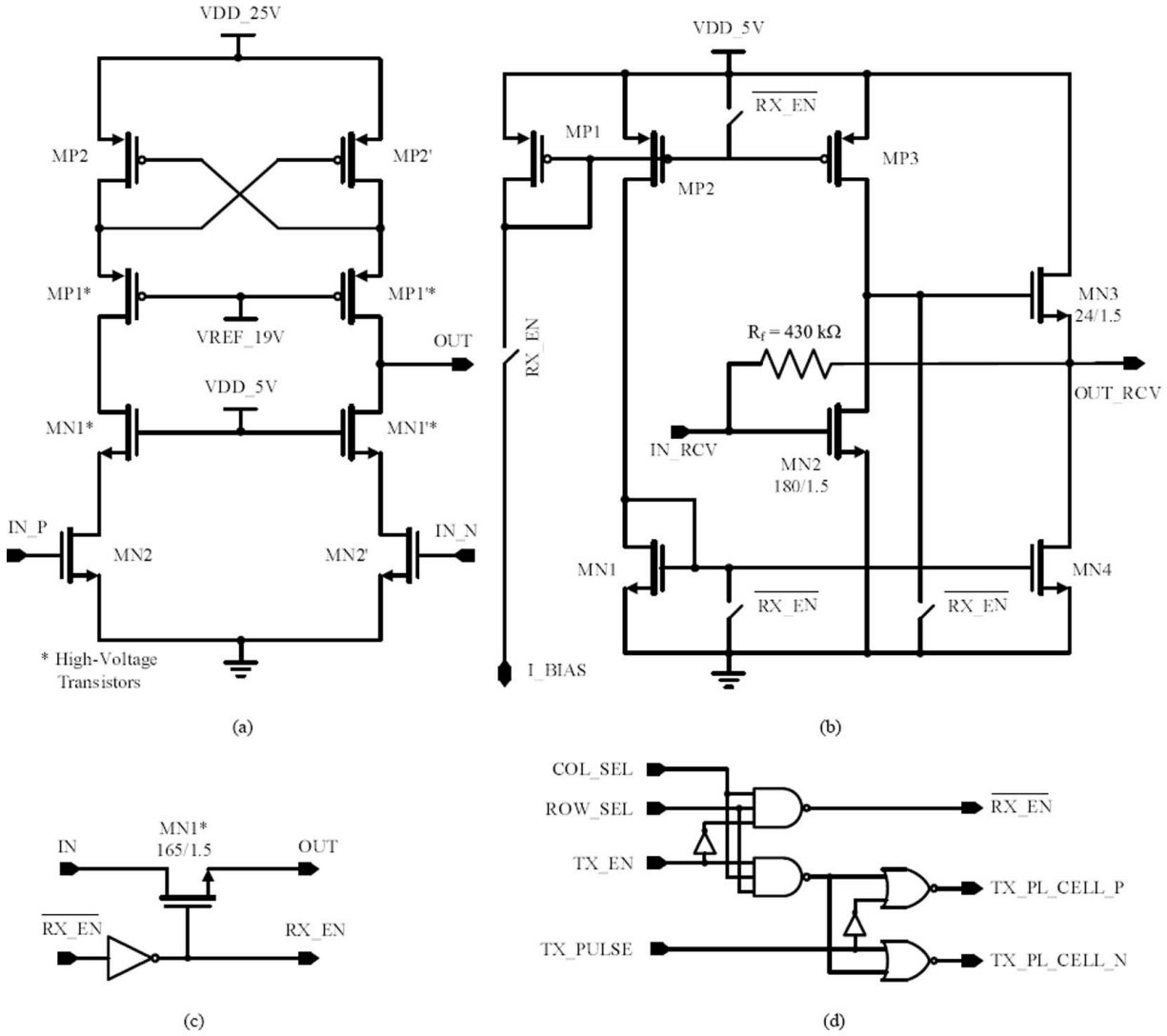


Fig. 5. Transmit and receive electronics provided to each element of the transducer array. (a) The pulser circuit provides up to 25-V unipolar pulses and is designed to provide pulses as short as 100 ns to a 2.5-pF load. Cross-coupled gates MP2 and MP2′ provide positive feedback that decrease the switching time, similar to a standard flip-flop. High-voltage devices MP1, MP1′, MN1, and MN1′ increase the maximum pulse voltage by limiting the voltage at the drains of the low-voltage transistors. (b) The transimpedance amplifier is composed of a common-source amplifier MN2, followed by a source follower buffer MN3, with feedback resistance $R_f$ connected between the input and output. The switches controlled by RX_EN allow the amplifier to be powered on and off. (c) The switch consists of a single high-voltage NMOS transistor. (d) If the ROW_SEL and COL_SEL signals are high, then the logic for an element opens the high-voltage switch during transmit; during receive, it closes the switch and powers on the amplifier.

The gain of the transimpedance amplifier is set by the feedback resistance $R_f$. At dc, the gain is equal to $-R_f$, which is $-430$ kΩ in our design. The input resistance is equal to the feedback resistor divided by the open-loop gain of the single-ended amplifier (430 kΩ/100 = 4.3 kΩ). When the feedback resistance is so large that the bandwidth is dominated by the capacitance in parallel with the feedback resistor, the bandwidth is approximated by

$$\omega_{\text{amp}} = \frac{1}{R_f C_f}, \tag{1}$$

where $C_f$ is the parasitic capacitance in parallel with the feedback resistor [37].

The primary noise sources of the transimpedance amplifier are the noise of the common-source amplifier and the feedback resistor. The equivalent current noise of the common-source amplifier is insignificant because of the large input impedance of the CMOS transistors. The equivalent voltage noise of the common-source amplifier is largely affected by device sizing and the circuit technology used. The feedback resistor value has the largest impact on noise performance. It contributes an input-referred noise current of $\sqrt{4kT/R_f}$. Because the input-referred noise is inversely proportional to the feedback resistance, a simple design approach is to make the feedback resistor as large as possible while still meeting the bandwidth requirements. Thus, the maximum value of the feedback resistor is set by (1), where $C_f$ is dominated by the gate-drain capacitance of transistor MN2 in Fig. 5(b).

The purpose of the output buffer is to drive the impedance of the connecting cable and input of the imag-

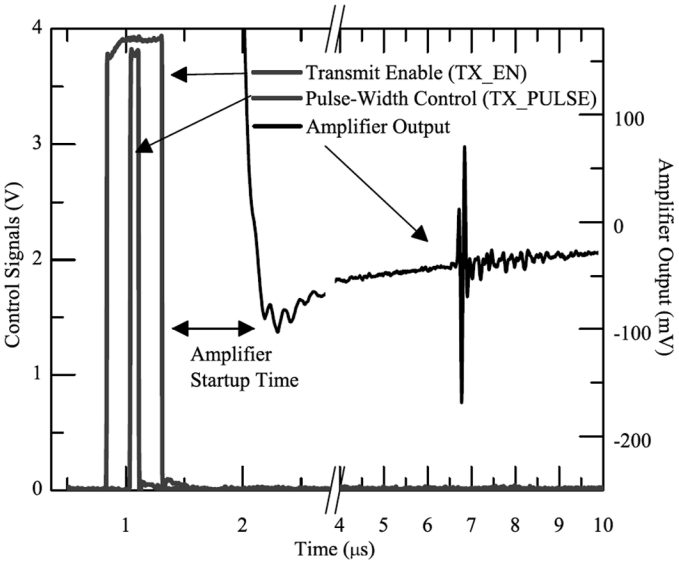


Fig. 6. Measurement showing the control signals and amplifier startup.

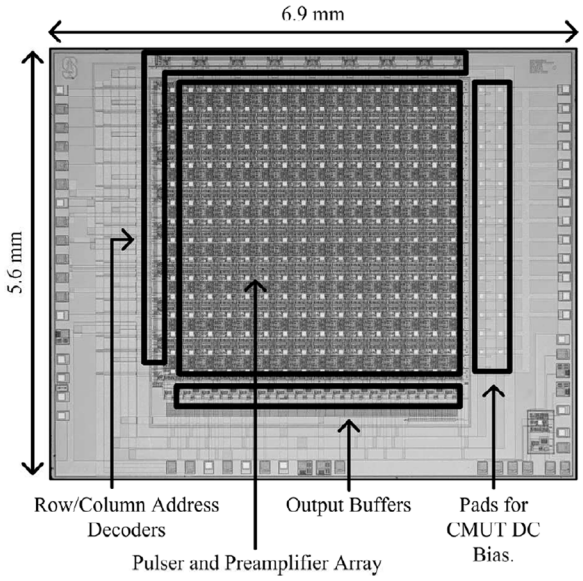


Fig. 7. Photo of the integrated circuit labeled to illustrate the general layout.

ing system. We use a source follower buffer because of its simple design and wide bandwidth. We designed the buffer to drive a 50-pF load with a 1-V peak-to-peak 5-MHz signal; with this specification, the buffer can drive a short cable with large signals. For large signals, the buffer must source a current of $2\pi f AC_{\text{load}}$. For our specifications, $f$ is 5 MHz, $C_{\text{load}}$ is 50 pF, and $A$ is 500 mV, which results in a current of 785 $\mu$A. We conservatively biased the buffer with 1 mA. The bandwidth of the source follower buffer is approximately $C_{\text{load}}/g_m$, where $g_m$ is the transconductance of the source follower transistor. The $g_m$ requirement determines the transistor size of the source follower; we sized the transistor so that the buffer would have negligible rolloff in gain at 10 MHz. The noise contribution of the buffer is negligible compared to the output noise of the preamplifier.

A photo of the IC illustrating the general layout of the fabricated chip is shown in Fig. 7. The IC measures 5.6 mm by 6.9 mm. For intravascular ultrasound imaging, the IC would need to be smaller, on the order of 2 mm by 2 mm or less. Flip-chip bonding technology would probably not impede decreasing the IC's size, as pad pitches as small as 50 $\mu$m can be bonded with current technology [39]. Using the existing circuitry, the IC could be made smaller by using a process with smaller feature sizes.

### *C. Flip-Chip Bonding*

A picture of a CMUT array flip-chip bonded to the IC is shown in Fig. 8. We used two flip-chip bonding techniques to connect the IC to the transducer array. For both techniques, a 20/20/300-nm Ti/Cu/Au metal stack was evaporated on the flip-chip bond pads of the transducer array. This metal stack enhances electrical contact and provides the under-bump metallurgy (UBM) required for flip-chip bonding.

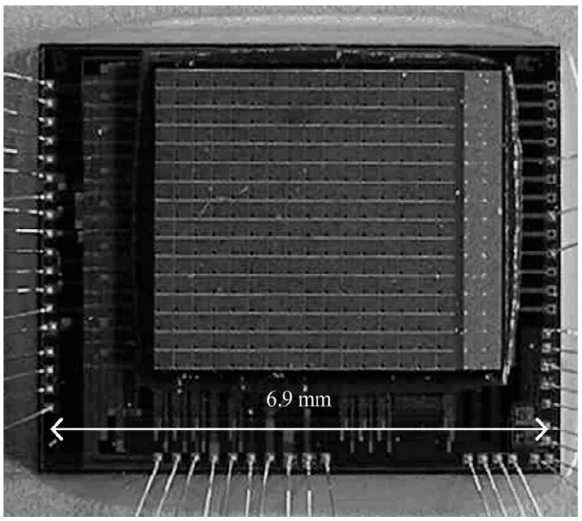


Fig. 8. A CMUT array flip-chip bonded to the integrated circuit.

The first flip-chip bonding technique is based on anisotropic conducting film (ACF). A wire bonder is used to form 25-$\mu$m-diameter, 25-$\mu$m-tall gold stud bumps on the 50-$\mu$m $\times$ 50-$\mu$m IC bond pads. A layer of ACF (FP1708E; Sony Chemicals, Tokyo, Japan) is then laminated on the stud-bumped IC. A flip-chip bonder (Model M8; Research Devices Inc., Piscataway, NJ) is used to align and bond the two parts by heating to a peak temperature of 190°C for 20 s and applying a pressure of 30 g/bump. The ACF is cured at this temperature. The ACF conducts at the points where it is squeezed between the CMUT pads and the gold bumps. Fig. 9(a) illustrates an ACF flip-chip bond. Fig. 10(a) shows the cross section of a flip-chip bonded device.

The second method used for flip-chip bonding is based on depositing eutectic Sn/Pb solder balls on the IC. For

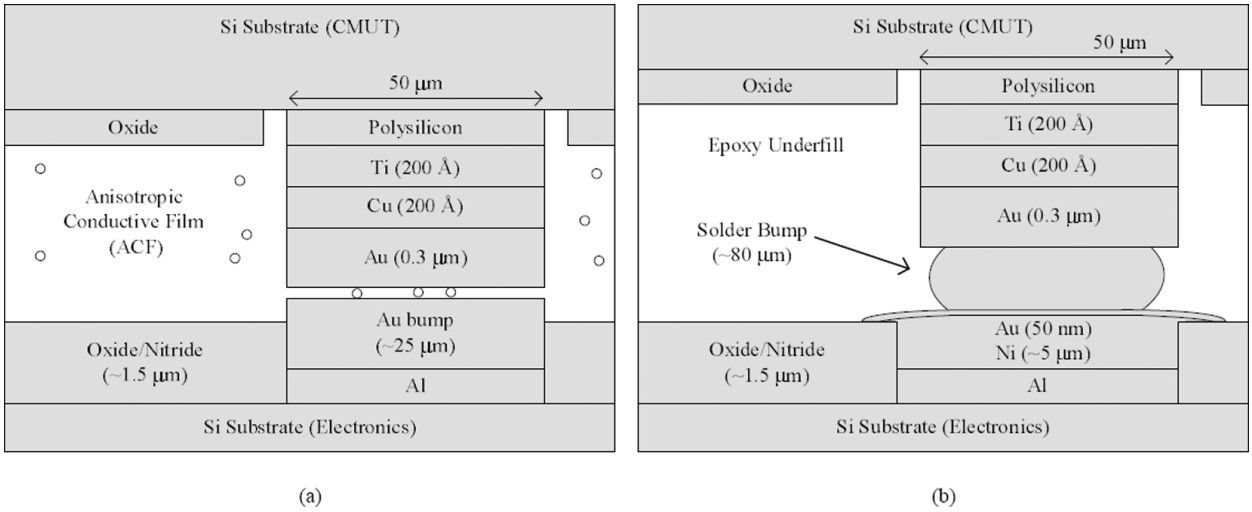


Fig. 9. Diagrams of flip-chip bonds made with (a) anisotropic conducting film (ACF) and (b) solder jetting.

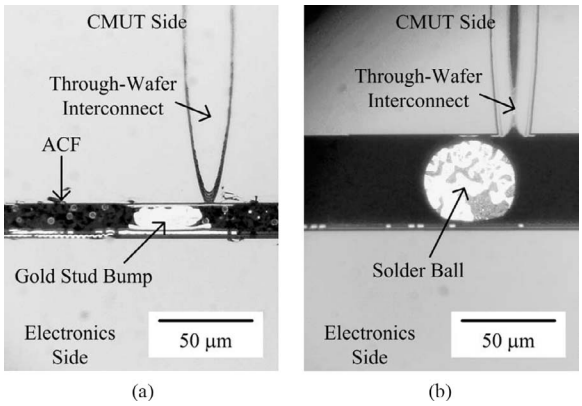


Fig. 10. Cross sections of devices bonded with (a) anisotropic conducting film (ACF) and (b) solder jetting.

this method, an electroless plating process (Pac Tech USA, Santa Clara, CA) is first used to coat the IC bond pads with a 5-$\mu$m-thick Ni/Au layer. Next, a solder jetting process (Pac Tech USA) is used to deposit 80-$\mu$m-diameter solder balls on the pads. For bonding, the IC and transducer array are aligned and then heated to 150°C with 4 g/bump of applied pressure. Solder reflow is done in an inert oven heated to 200°C at atmospheric pressure. Fig. 9(b) illustrates a flip-chip bond made using this process. The cross section of a bonded device is shown in Fig. 10(b).

## III. Characterization

### A. Through-Wafer Interconnects

We measured the equivalent parallel capacitance and series resistance of the through-wafer interconnects to estimate their effect on device performance. Because the through-wafer interconnects are fabricated before the CMUTs, they can be conveniently characterized on their own, prior to fabrication of the CMUTs on top of them. The total capacitance between the flip-chip bond pad and the silicon substrate (for this measurement, the silicon substrate was connected to ground) was measured (Fig. 11) with an LCR meter (4275A; Agilent Technologies, Palo Alto, CA). The flip-chip bond pad, through-wafer interconnect, and bottom electrode of the CMUT all form metal-insulator-semiconductor (MIS) structures with the silicon bulk. The total parasitic capacitance is the sum of these MIS capacitances. Because MIS capacitance is a function of voltage, the total parasitic capacitance depends on the applied voltage. Fig. 12 shows the measured capacitance as a function of dc voltage. The two regions of the capacitance curve, corresponding to accumulation and depletion in the bulk silicon, are typical for an MIS structure made with n-type silicon and operated at high frequencies [40]. As shown in Fig. 12, the capacitance varies between 100 fF and 500 fF, depending on the dc bias.

The measured capacitance shown in Fig. 12 is the total capacitance of the through-wafer interconnect, bottom CMUT electrode, and flip-chip bond pad. Because the sizes of the bottom electrode and flip-chip bond pad may vary between designs, it is useful to calculate the capacitance of the through-wafer interconnect alone, which is done by calculating the interconnect's area of contact with the silicon bulk relative to the bottom electrode and flip-chip bond pad areas. The calculated through-wafer interconnect capacitance in the accumulation region is about 250 fF. In the depletion region, the calculated interconnect capacitance is less than 60 fF. This depletion region capacitance is approximately eight times lower than the MIS through-wafer interconnect capacitance reported in [26]. This reduction in capacitance is largely due to the high resistivity ($\rho > 10,000$ Ω-cm) silicon wafers used. These measurements demonstrate the minimal parasitic capacitance that results from integrating the electronics with the transducer array. For comparison, coaxial cable used in ultrasound systems has parasitic capacitance on the order of 50 to 100 pF/m [41].

The MIS capacitance of the through-wafer interconnect depends on the polarity of the substrate voltage (Fig. 12).

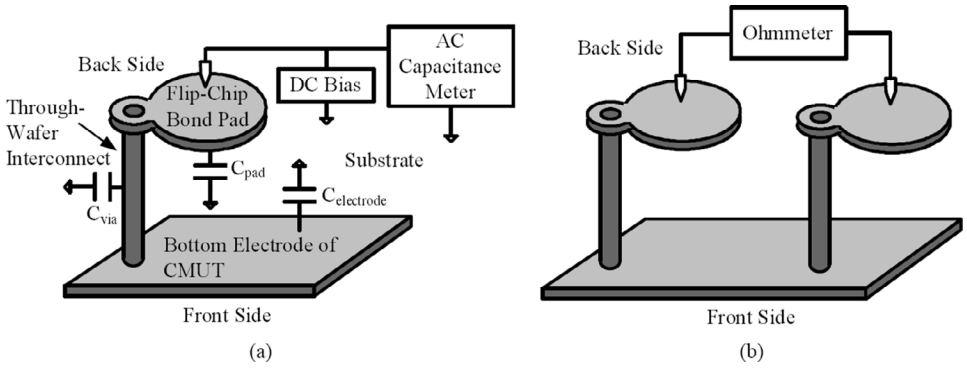


Fig. 11. Structures measured to determine (a) parasitic capacitance and (b) series resistance of the through-wafer interconnects.

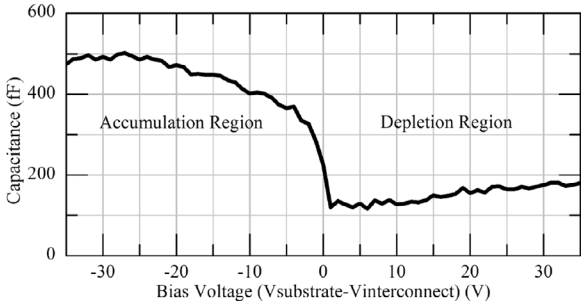


Fig. 12. Combined capacitance of the through-wafer interconnect, flip-chip bond pad, and bottom electrode as a function of DC voltage.

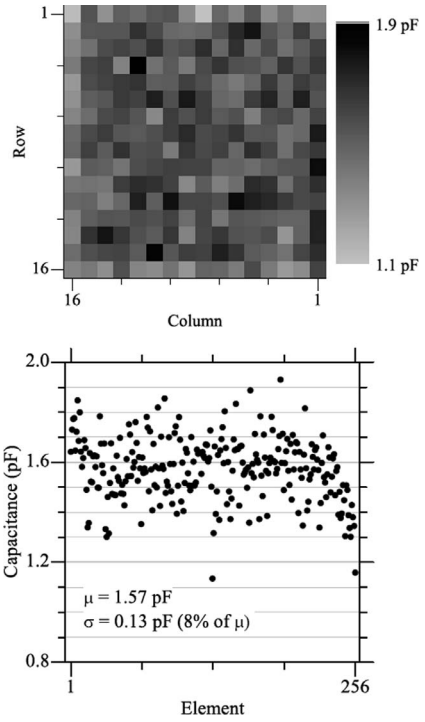


Fig. 13. 2D (top) and 1D (bottom) plots of transducer element capacitance.

Since the substrate is connected to the dc bias, the MIS capacitance depends on the polarity of the CMUT dc bias voltage. We use a negative dc bias voltage even though it results in slightly more parasitic capacitance. The reason is that for a positive pulse voltage (applied to the bottom electrode) a negative dc bias (applied to the top electrode) results in the highest total voltage across the CMUT. More net voltage across the CMUT, and a correspondingly higher electric field, translates to more output pressure for a given pulse voltage.

The series resistance of the via was measured using an ohmmeter as illustrated in Fig. 11(b). The series resistance is about 20 Ω, which is negligible compared to the equivalent series resistance of the CMUT elements (kilohms), pulser output impedance (tens of ohms), and preamplifier input resistance (kilohms).

### *B. Device Capacitance*

Before flip-chip bonding the finished array to the IC, the input impedance of each element of an array was measured with a network analyzer (8751; Agilent Technologies). This measurement was made by first calibrating the network analyzer with the measurement probe (ACP40-W-GS-150; Cascade Microtech, Inc., Beaverton, OR) and then contacting the back side of the transducer element to be tested. Element capacitance values extracted from the measured S11 parameters are shown in Fig. 13. The mean element capacitance was 1.57 pF with a standard deviation of 0.13 pF.

### *C. Amplifier Performance*

We measured the output-referred noise of the preamplifier and buffer in a flip-chip bonded device by connecting the buffer's output to a spectrum analyzer (Model 2712; Tektronix, Beaverton, OR) and recording the noise voltage as a function of frequency (Fig. 14). The recorded noise did not change as a function of the CMUT bias voltage, which indicates that the noise is dominated by the electrical noise of the preamplifier and buffer and not acoustical sources.

An input-referred pressure noise or noise equivalent pressure (NEP) [42] was determined by dividing the amplifier's output noise by the receive sensitivity values in Fig. 15(b). At 5 MHz, this conversion yields a typical NEP of 1.8 mPa/$\sqrt{\text{Hz}}$ or equivalently 65 dB relative to 1 $\mu$Pa/$\sqrt{\text{Hz}}$.

TABLE II
ULTRASOUND PROPERTIES OF MATERIALS USED FOR TESTING IMAGING ARRAYS.

| | Soybean oil [52] | Water [53] | Tissue [54] |
|---|---|---|---|
| Density (kg/m$^3$) | 913 | 1000 | 1050 |
| Sound velocity (m/s) | 1480 | 1497 | 1570 |
| Acoustic impedance (MRayls) | 1.35 | 1.49 | 1.65 |
| $\alpha$ (1/m-Hz$^k$) | $7.3 \times 10^{-12}$ | $2.2 \times 10^{-14}$ | $5.8 \times 10^{-6}$ |
| $k$ | 1.85 | 2 | 1 |

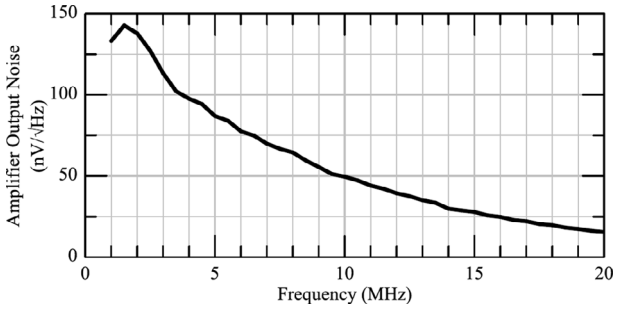


Fig. 14. Output noise of the preamplifier measured with a spectrum analyzer.

Comparing the frequency content of the one-way hydrophone measurements and the pulse-echo measurements indicates that the amplifier bandwidth does not limit the transducer's bandwidth. This is in agreement with the simulated bandwidth of 9.5 MHz for a 2-pF source capacitance. Measuring the amplifier's frequency response on its own is difficult because capacitance of more than a few picofarads at the input significantly reduces the amplifier's bandwidth. An on-chip test structure as used in [16] is one way of characterizing the amplifier without connecting it to a transducer.

### *D. Pulse-Echo Signal from a Plane Reflector*

For pulse-echo and imaging tests, a 5-cm × 5-cm × 4-cm acrylic tank was built. A rectangular hole was cut in the bottom of the tank to create an acoustic window for the array. The tank was then glued to a ceramic package that contained the flip-chip bonded device. For imaging and pulse-echo tests, the tank was filled with soybean oil.

We use soybean oil instead of water because it is nonconducting; thus, we can test the device in immersion without insulating the bond wires and electrodes of the CMUT and IC. Furthermore, the acoustic impedance and speed in soybean oil are similar to those for water and tissue (Table II). For *in vivo* testing, the device would need to be insulated. We have previously demonstrated CMUTs insulated with parylene for operation in water [43]. In general, insulating procedures used for piezoelectric arrays can also be used for CMUT arrays.

To measure the pulse-echo signal received from a plane reflector, we acquired the pulse-echo signal from the oil-air interface at 15 mm for each element of the array (Figs. 16, 17, and 18) with an oscilloscope (model 54825;

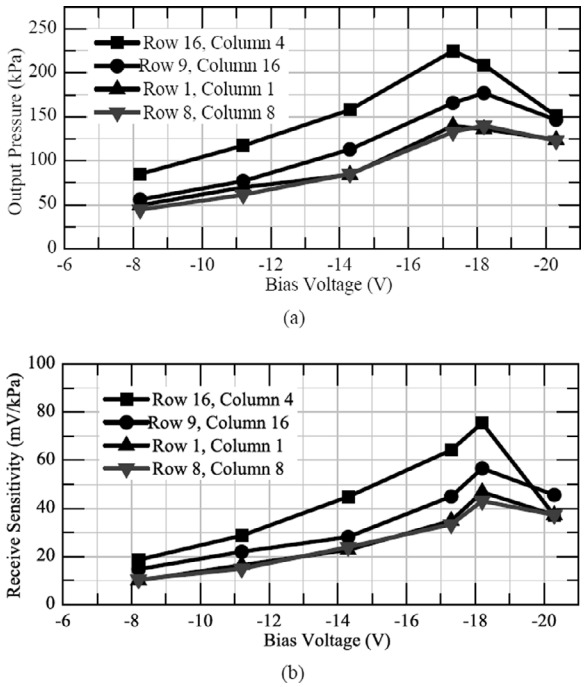


Fig. 15. Output pressure and receive sensitivity measurements based on hydrophone and pulse-echo measurements. (a) Transducer output pressure normalized to the face of the transducer. (b) Receive sensitivity at the output of the amplifier as a function of DC bias voltage.

Agilent Technologies). The frequency responses show wide bandwidth and good element-to-element uniformity. In the pulse-echo signals shown in Fig. 16(a) and (b), there are small signals following the main pulse. These signals might be due to crosstalk between the elements [2], particularly since they are more pronounced for elements in the center. A way of reducing this crosstalk could be to coat the array with a thin attenuating layer that would suppress laterally moving waves [44]; the insulating or matching layers used to coat the array could also serve this purpose. The characterization and suppression of crosstalk in CMUTs [45]–[48] is an ongoing topic of investigation.

The peak-to-peak transmitted pressure was measured for four elements of the array. These four elements included the one with the largest pulse-echo response and three with typical pulse-echo responses. The pressure was measured at a distance of 4 mm from the array using a calibrated hydrophone (model PZT-Z44-0400; Onda Corporation, Sunnyvale, CA). The pressure was then normalized to the face

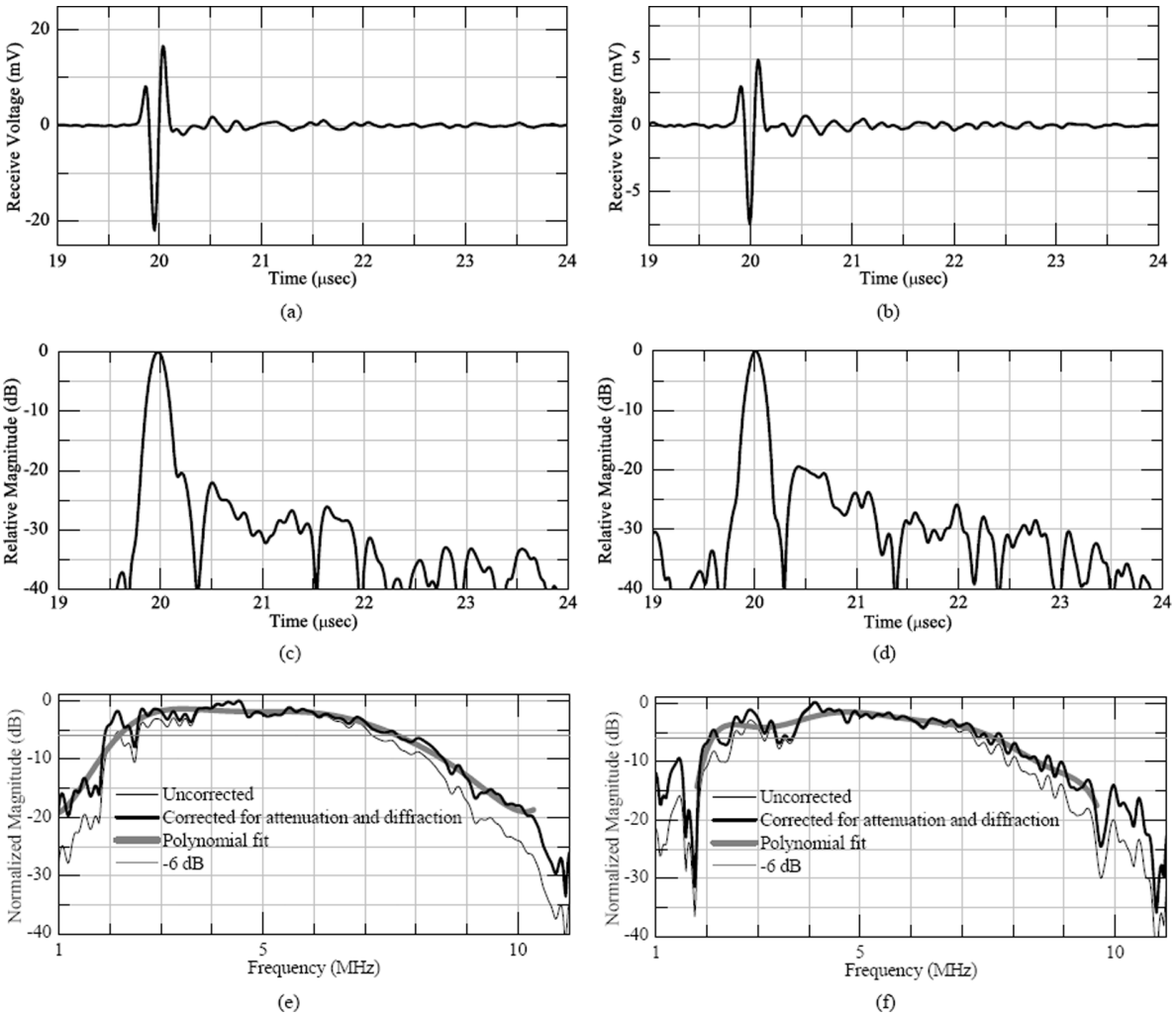


Fig. 16. Pulse-echo signals from a plane reflector at 15 mm. Results for the elements at row 16, column 4 and row 8, column 8 are chosen to represent the range of performance. The element at row 16, column 4 has the largest pulse-echo amplitude. The element at row 8, column 8 is a typical element from the center of the array. (a) Pulse-echo signal for the element at row 16, column 4. (b) Pulse-echo signal for the element at row 8, column 8. (c) Pulse-echo signal from Fig. 16(a) shown with envelope detection. The −6-dB width is 177 ns. (d) Pulse-echo signal from Fig. 16(b) shown with envelope detection. The −6-dB width is 190 ns. (e) Fourier transform of the pulse-echo signal shown in Fig. 16(a). A polynomial is fit to the Fourier transform to estimate the center frequency and bandwidth. (f) Fourier transform of the pulse-echo signal shown in Fig. 16(b).

of the transducer by compensating for the diffraction and attenuation losses. The frequency dependent attenuation of pressure is modeled using

$$P = P_0 e^{\alpha f^k z}, \tag{2}$$

where $P_0$ is the pressure at the face of the transducer, $f$ is frequency in Hz, $z$ is the propagation distance in meters, and constants $\alpha$ and $k$ are taken from Table II. At a distance of 4 mm and frequency of 5.1 MHz, these losses were calculated to be 26 dB. The normalized pressure as a function of bias voltage is shown in Fig. 15(a). The measured receive sensitivity for the same four elements is shown in Fig. 15(b).

The pulse-echo results discussed so far and the imaging results in the following section are for device 1 of Table III. The characterization results of two other devices are also summarized in Table III.

### *E. Imaging Results*

Because the IC uses a single element at a time, we use classic synthetic aperture (CSA) imaging. With CSA imaging, each element is used one at a time for both transmit and receive. Three-dimensional images are reconstructed from the acquired pulse-echo signals using a standard delay-and-sum algorithm. For an imaging depth of 30 mm, each pulse-echo signal is 40 $\mu$s long. Thus, acquiring all 256 pulse-echo signals requires about 10 ms, which corresponds to 100 frames per second. For the images presented here, data were acquired over several minutes using an oscilloscope. Data acquisition at a rate of 30 frames per second using an FPGA-based data acquisition system was demonstrated in [49].

We constructed a wire-target phantom using 150-$\mu$m (6-mil)-diameter fishing line. The basic geometry of the target is shown in Fig. 19. Acquired 2D images of the tar-

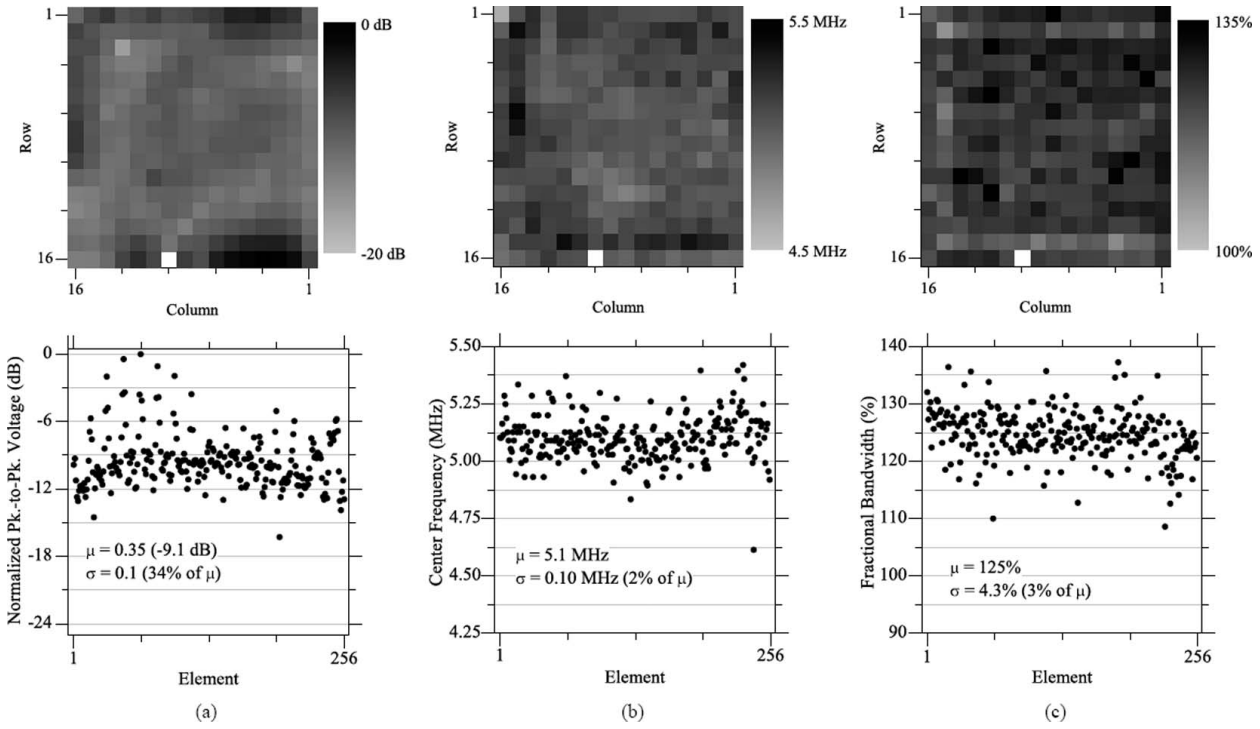


Fig. 17. 2D (top) and 1D (bottom) plots of element-to-element variation in the pulse-echo signal for a plane reflector at 15-mm. (a) Variation in peak-to-peak voltage. (b) Variation in center frequency. (c) Variation in −6-dB pulse-echo fractional bandwidth.

TABLE III
PERFORMANCE SUMMARY OF THREE DEVICES.

| Device parameter | 1 | 2 | 3 |
|---|---|---|---|
| Membrane diameter ($\mu$m) | 30 | 30 | 24 |
| Number of membranes per element | 35 | 35 | 48 |
| Element width ($\mu$m) | 200 | 200 | 204 |
| Membrane thickness ($\mu$m) | 0.6 | 0.5 | 0.6 |
| Flip-chip bonding technology | ACF | Solder-jetting | ACF |
| Center frequency, mean (MHz) | 5.1 | 2.3 | 5.7 |
| Center frequency, standard deviation (MHz) | 0.10 | 0.19 | 0.50 |
| Pulse-echo −6 dB fractional bandwidth, mean (%) | 125 | 65 | 105 |
| Pulse-echo −6 dB fractional bandwidth, standard deviation (%) | 4.3 | 17 | 13 |
| Pulse-echo voltage standard deviation (%) | 34 | 12 | 17 |
| Peak-to-peak output pressure [best, typical] (kPa) | 225, 139 | 330, 314 | 339, 275 |
| Receive sensitivity [best, typical] (mV/kPa) | 76, 47 | 73, 63 | 72, 67 |
| Input-referred noise [best, typical] (mPa/Hz) | 1.1, 1.8 | 1.8, 2.1 | 1.1, 1.2 |
| Bias voltage (V) | −17.3 | −30.3 | −45 |
| Number of working elements | 255 | 256 | 255 |

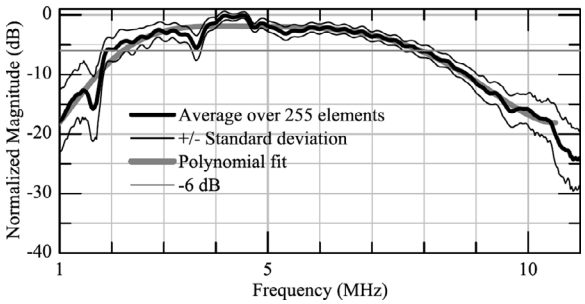


Fig. 18. The average of the Fourier transforms of the pulse-echo signals for all 255 working elements. The curve is corrected for frequency-dependent attenuation and diffraction losses for a two-way distance of 30 mm.

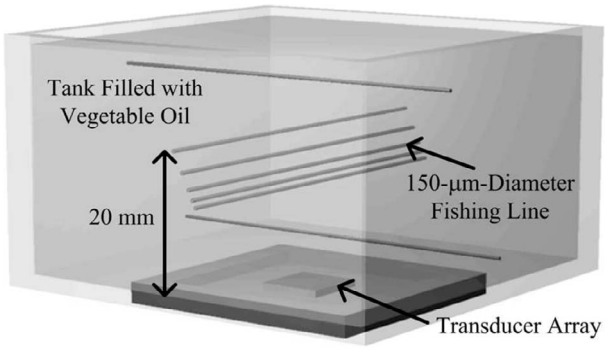


Fig. 19. Diagram of the wire-target phantom used for imaging. The minimum spacing between the lines is 800 $\mu$m.

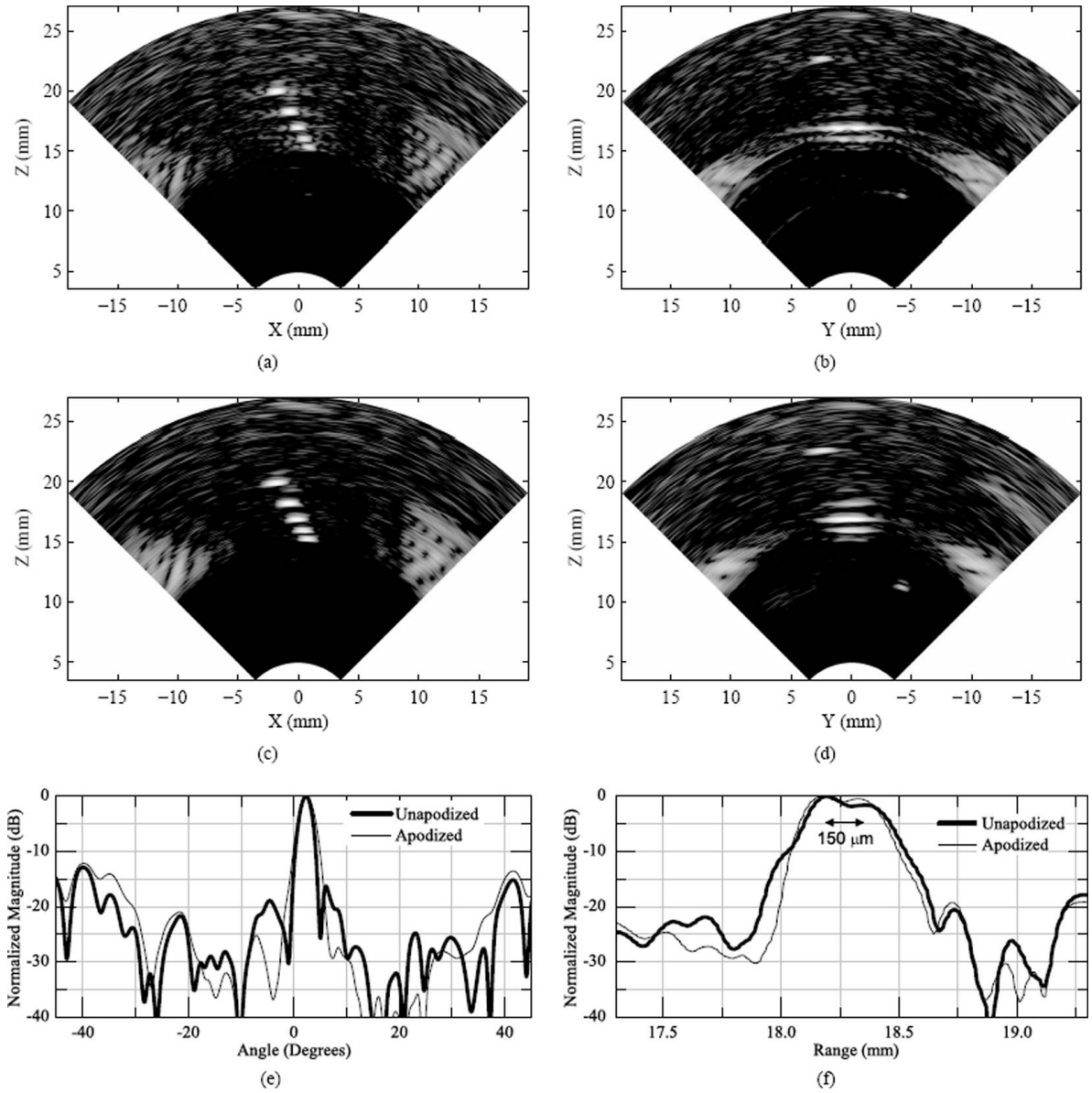


Fig. 20. Two-dimensional images obtained of the wire-target phantom illustrated in Fig. 19. Data for these images were averaged 16 times. The images are shown log-compressed with a dynamic range of 25 dB and a gamma correction of 1/0.8. For the images shown with apodization, the elements were weighted to compensate for variation in pulse-echo response and then weighted with a 2D Hamming function. (a) Unapodized X-Z cross section. (b) Unapodized Y-Z cross section. (c) Apodized X-Z cross section. (d) Apodized Y-Z cross section. (e) Lateral profile of the center wire seen in (a) and (b). The −6-dB width of the unapodized profile is 3.2°. (f) Axial profile of the center wire seen in (a) and (b). The two peaks of the profile correspond to the front and back sides of the 150-$\mu$m-diameter fishing line.

get are shown in Fig. 20. Medical image viewing software [50] was used to render the acquired volumetric image; the 3D rendering is shown in Fig. 21.

There are significant grating lobes in the images because of the CSA image acquisition and array pitch. Theoretically, the grating lobes should appear at an angle of $\arcsin(\lambda/(2d))$, where $\lambda$ is the wavelength and $d$ is the element pitch. For a 5-MHz center frequency and an element pitch of 250 $\mu$m, the grating lobes are expected to appear at $\pm 37°$, as observed in the images.

Significant improvements in image quality could be obtained with an IC that uses more than one element at a time for transmit and receive. The main drawbacks of CSA imaging compared with techniques that use more elements for transmit and receive are lower SNR, higher sidelobe levels, and grating lobes that appear at smaller off-axis angles. Several transmit and receive array designs, including CSA, are compared for a 5-MHz $16 \times 16$-element transducer array in [51].

## IV. Conclusion

In this paper we demonstrate that flip-chip bonding a 2D CMUT array to an IC is a compact means of providing electronics to a transducer array and results in minimal

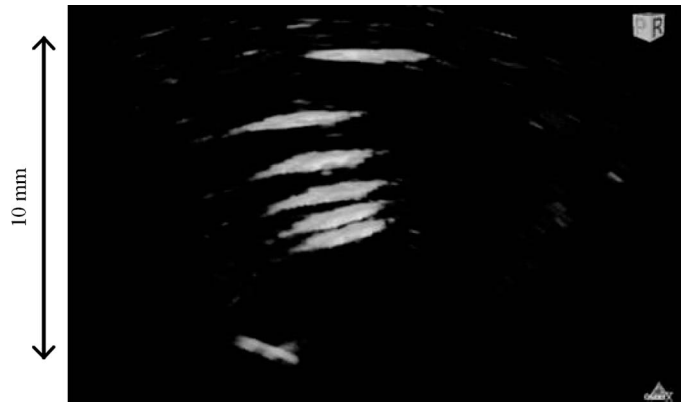


Fig. 21. 3D-rendered image obtained of the phantom shown in Fig. 19. Data for this image were averaged 16 times. The image is shown with log compression and a dynamic range of approximately 15 dB.

parasitics. Furthermore, with these results we demonstrate an ultrasound imaging device with wide bandwidth, excellent sensitivity, and high element yield.

The combination of a CMUT array with an IC benefits 3D ultrasound imaging by enabling systems that utilize large arrays and that are more sensitive, simpler, and less expensive. These benefits extend to other applications of ultrasound imaging as well.

## Acknowledgment

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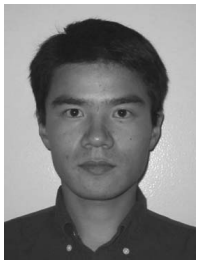

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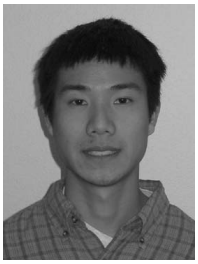

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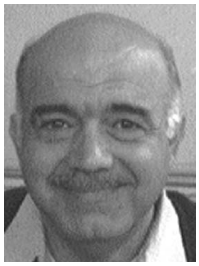

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