Fabrication of Flexible Transducer Arrays With Through-Wafer Electrical Interconnects Based on Trench Refilling With PDMS

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***Abstract*—Flexible transducer arrays are desired to wrap around catheter tips for side-looking intravascular ultrasound imaging. We present a technique for constructing flexible capacitive micromachined ultrasonic transducer (CMUT) arrays by forming polymer-filled deep trenches in a silicon substrate. First, we etch deep trenches between the bottom electrodes of CMUT elements on a prime silicon wafer using deep reactive ion etching. Second, we fusion-bond a silicon-on-insulator (SOI) wafer to the prime silicon wafer. Once the silicon handle and buried oxide layers are removed from the back side of the SOI wafer, the remaining thin silicon device layer acts as a movable membrane and top electrode. Third, we fill the deep trenches with polydimethylsiloxane, and thin the wafer down from the back side. The 16 by 16 flexible 2-D arrays presented in this paper have a trench width that varies between 6 and 20 μm; the trench depth is 150 μm; the membrane thickness is 1.83 μm; and the final substrate thickness is 150 μm. We demonstrate the flexibility of the substrate by wrapping it around a needle tip with a radius of 450 μm (less than catheter size of 3 French). Measurements in air validate the functionality of the arrays. The 250-μm by 250-μm transducer elements have a capacitance of 2.29 to 2.67 pF, and a resonant frequency of 5.0 to 4.3 MHz, for dc bias voltages ranging from 70 to 100 V. [2007-0078]**

***Index Terms*—Capacitive micromachined ultrasonic transducer (CMUT), fabrication, flexible arrays, intravascular ultrasound (IVUS), polydimethylsiloxane (PDMS), through-wafer interconnects, trench isolation.**

I. Introduction

INTRAVASCULAR ultrasound (IVUS) is an increasingly important imaging modality that provides new diagnostic and therapeutic capabilities for cardiovascular medicine. Using IVUS imaging, the degree of narrowing in blood vessels can be determined; plaque decomposition can be analyzed; and stent placements can be visually guided. Currently, commercially available IVUS catheters offer side-looking capabilities. A radial cross-sectional image of the vessel wall is formed by using an array of ultrasonic transducers wrapped around the tip of a catheter (Fig. 1) [1]. Piezoelectric transducer arrays are used in these catheters [2]. The manufacturing process for piezoelectric transducer arrays is based on meticulous steps such as mechanical lapping, polishing, and dicing. This labor-intensive process produces a low yield ratio, and therefore, is an expensive way of making transducer arrays. The fabrication of miniaturized devices is even more challenging, especially for IVUS, which requires the whole device to fit in 1–2 mm. Moreover, the piezoelectric transducer arrays need complex backing materials for acceptable acoustic performance, and suffer from large element-to-element nonuniformity. These drawbacks motivate the development of a flexible capacitive micromachined ultrasonic transducer (CMUT) array that can be wrapped around a catheter tip for IVUS applications. The authors and others demonstrated several experimental imaging devices that are based on CMUTs including 1-D and 2-D arrays, and forward-looking annular ring arrays [3]–[8]. These studies show that CMUTs are suitable for IVUS applications. CMUT arrays with different geometries can be easily fabricated on the same wafer. Potentially, using CMUT technology, forward-looking arrays can be combined with side-looking arrays on a single catheter to enable more advanced IVUS imaging systems that can simplify diagnostic and surgical procedures in the heart.

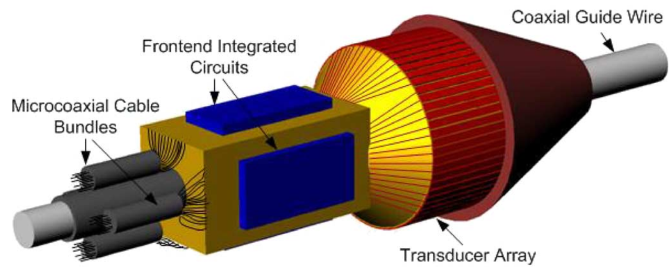

Fig. 1. Schematic of a catheter-based side-looking IVUS imaging probe (after [1]).

The basic structure of a CMUT can be described as a movable membrane over a shallow vacuum or air cavity [9], [10]. This structure can be built on a silicon substrate by using surface micromachining techniques [9]–[13] or by wafer bonding [14]. The most commonly used membrane material is either silicon or silicon nitride. Typically, the membrane thickness is on the order of 1–10 μm, and the cavity is less than 1 μm deep. Many membranes are connected in parallel to form a transducer element. When an electrical signal is applied

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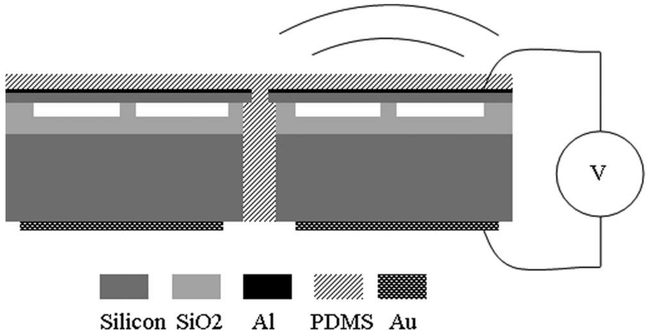


Fig. 2. Cross-sectional schematic of two flexible CMUT array elements. One of the elements is excited to transmit ultrasound waves into the surrounding medium.

between the electrodes of the transducer, the membrane is set into motion and sound waves are emitted in the surrounding medium (Fig. 2). Conversely, when the membrane vibrates as a result of the impinging waves, an electrical signal is generated between the two electrodes.

To implement a side-looking IVUS transducer array or a conformal external array, the silicon substrate, on which the CMUT array is made, should be flexible. In recent years, researchers have demonstrated flexible silicon structures based on polymer-coated trenches [15], [16]. Polymer-based structures have also been used as a flexible carrier for MEMS sensors by different research groups [17]–[20]. One method to achieve a flexible CMUT array is by aggressively thinning down the silicon substrate [21]. Thin silicon wafers (thickness $< 100\ \mu$m), although flexible, can easily break and impose practical handling difficulties [22]. Our approach to achieve flexible CMUTs is by etching through-wafer trenches to isolate array elements, and refilling the trenches with polydimethylsiloxane (PDMS).

In the following sections, we first explain the reasoning for the choice of PDMS as the trench-refilling and CMUT coating material. We then restate the key design criteria for CMUT arrays. Next, we demonstrate a flexible silicon substrate by trench-refilling with PDMS. We also present a method to incorporate CMUT elements onto a flexible silicon substrate, followed by test results on the CMUT arrays in air. Finally, fabrication challenges and future work are discussed.

II. Methods

A. Design

In our approach to fabricate flexible CMUT arrays with through-wafer electrical interconnects, CMUT array elements are fabricated on the front side of a highly conductive silicon wafer. Trenches are etched into the silicon substrate to electrically isolate the elements. PDMS is used to fill the trenches, and to coat the front surface of the CMUT. Highly conductive silicon pillars separated by PDMS-filled deep trenches are used to route electrical signals between the front and back sides of the wafer. The advantages of trench isolation as a method to make through-wafer electrical interconnections for CMUTs include low series resistance, negligible electrical crosstalk between elements, and ease of fabrication [23].

PDMS is a well-suited material to achieve a flexible array, and to serve as a coating layer for the CMUTs:

1) PDMS is mechanically flexible. When used to refill through-wafer trenches, it provides mechanical linkage between neighboring silicon pillars, and makes the array bendable.
2) PDMS is biocompatible. CMUTs coated with PDMS can be safely used for intravascular applications in close contact with tissue.
3) PDMS typically has high dielectric breakdown field strength ($\sim$20 kV/mm). Good insulation between the device and the tissue, as well as between the signal and ground electrodes, can be achieved.
4) The acoustic impedance of PDMS (1$\sim$1.9 MRayl [24]) is close to that of tissue (1.3 $\sim$ 1.7 MRayl [25]). As a result, little ultrasonic energy is reflected from the PDMS-tissue interface to cause undesired imaging artifacts.
5) PDMS is thermally stable at elevated temperatures ($> 200\ ^\circ$C). It is therefore compatible with the thermal reflow process in eutectic solder-based flip-chip bonding, a common process to integrate CMUT arrays with their supporting electronic circuits [5].

Because of these advantageous attributes, PDMS is already used to make acoustic lenses that cover transducer surfaces to focus ultrasound [26]. Recently, real-time *ex vivo* imaging results in an electrically conductive medium using a PDMS-coated CMUT array have been reported by Nikoozadeh *et al.* [27].

To demonstrate the flexibility of CMUTs in both x and y axes, we designed and fabricated 2-D arrays. Some of the important design criteria for CMUT arrays used in medical imaging are the center frequency, bandwidth, and the collapse (pull-in) voltage. The center frequency is determined according to the requirements for the image resolution and depth of penetration. Better resolution can be achieved at higher operating frequencies. However, depth of penetration is limited at higher frequencies due to higher attenuation. The image resolution in the axial direction depends on the fractional bandwidth (FBW), i.e., the ratio of the bandwidth to the center frequency. The efficiency of a CMUT is directly proportional to the product of the device capacitance and the electric field strength in the gap beneath the membrane [28]. Therefore, it is important to be able to sustain high electrical fields in the cavity without collapsing (pulling in) the membrane for improved transmission efficiency and reception sensitivity [29]. However, excessively high dc voltages should be avoided for patient safety, device reliability, and to relax design challenges for the supporting electronic systems.

The physical parameters of the CMUT designed in this paper are summarized in Table I. Rectangular membranes are used because they offer better FBW compared to other membrane shapes [30]. Single-crystal silicon membranes are used because they can be fabricated with the silicon-on-insulator (SOI) wafer-bonding technique, which offers better fill factor (ratio of the active membrane area to the total area of an array element) than the surface-micromachining technique. Higher fill factor is desired for improved FBW [31]. The collapse

TABLE I
PHYSICAL PARAMETERS OF THE CMUT

Membrane length (μm)	140
Membrane width (μm)	35
Membrane thickness (μm)	1.83
Vacuum cavity height (μm)	0.15
SiO_2 insulation layer thickness (μm)	0.3
Element pitch (μm)	250
Number of membrane / element	8
Metal coverage on membrane	100%
Number of elements in an array	256 (16 by 16)
Array dimension	4 mm by 4 mm
PDMS coating thickness (μm)	30

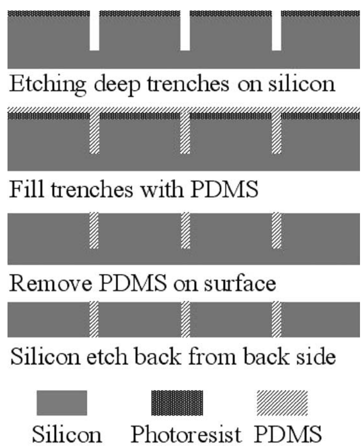


Fig. 3. Fabrication process to make a flexible silicon substrate by refilling through-wafer trenches with PDMS.

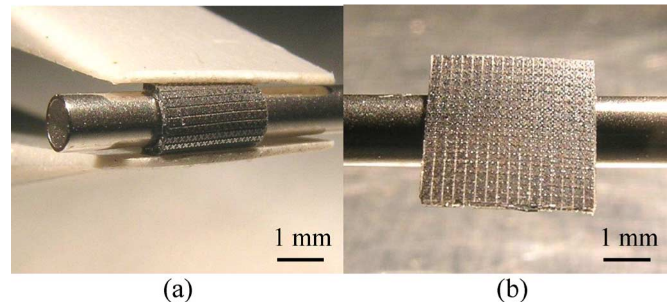


Fig. 4. Flexible silicon substrate realized by refilling through-wafer trenches with PDMS.

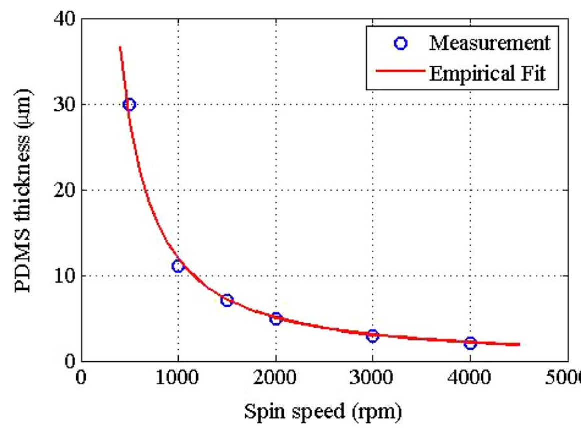


Fig. 5. PDMS thickness as a function of spin speed.

voltage is designed to be around 100 V. To prevent electrical leakage current between the conductive membrane and the silicon substrate, the oxide insulation is designed to be 0.3-μm thick (Fig. 2). The PDMS coating on the array surface is chosen to be 30 μm, which is a fraction of the acoustic wavelength, and can be easily achieved by a simple spin-coating step. Based on these parameters, an analytical model [32] predicts collapse voltages of 105 and 97 V, and resonant frequencies of 4.4 and 11.5 MHz in air, with and without PDMS coating, respectively.

B. Fabrication of a Flexible Silicon Substrate

Before making a flexible CMUT array, as an intermediate step, we built a flexible silicon substrate with PDMS-refilled deep trenches to prove the feasibility of our approach (Fig. 3). In these test samples, we used deep reactive ion etching (DRIE) to etch the silicon trenches with a 10-μm-thick photoresist layer as the mask; the width varies from 8 to 50 μm; the depth varies from 50 to 200 μm in different designs; and the pitch of silicon pillars is 250 μm. Each 2-D array consists of 16 by 16 elements, and measures 4 mm by 4 mm on the sides, in compliance with the dimensions of the intended 2-D CMUT array. The PDMS was dispensed on the wafer surface, followed by a spinning step at 5000 r/min. After curing the PDMS on a hot plate, excessive PDMS was removed from the wafer front side by a lift-off step. The wafer back side is etched back using DRIE so that the final silicon substrate thickness is equal to the trench depth (50 to 200 μm).

After finishing the process, the wafer can still be handled like a regular silicon wafer. To test the flexibility of the trench-isolated silicon pillars, a 4-mm by 4-mm 2-D array with a 200-μm substrate thickness was diced out from the wafer. We used tweezers to bend the substrate to conformally wrap around a needle tip, emulating a side-viewing IVUS catheter [Fig. 4(a)]. The silicon substrate returned to its original configuration after the bending force was removed [Fig. 4(b)]. The smallest needle tip we could successfully wrap the substrate around without fracturing the PDMS linkage between the silicon pillars had a diameter of 900 μm, which is smaller than a 3-French catheter tip.

The flexible substrates were heated up to 220 °C on a hot plate for 5 min, to emulate the thermal reflow process condition for Sn/Pb eutectic flip-chip bonding used to integrate CMUT arrays to a flexible printed circuit board (PCB) or a front-end IC. We were able to successfully repeat the stretching and wrapping tests after this thermal cycle.

Three different kinds of PDMS were used: two-part Dow Corning Sylgard 182, two-part Sylgard 184 and one-part 1-4105 (Dow Corning Corporation, Midland, MI). All substrates showed similar flexibility.

C. Fabrication of CMUTs on a Flexible Silicon Substrate

To build flexible CMUT arrays, we merged the fabrication process for conventional trench-isolated CMUTs [23] with the PDMS refilling process described in the previous section. We used the one-part Dow Corning 1-4105 PDMS in the presented

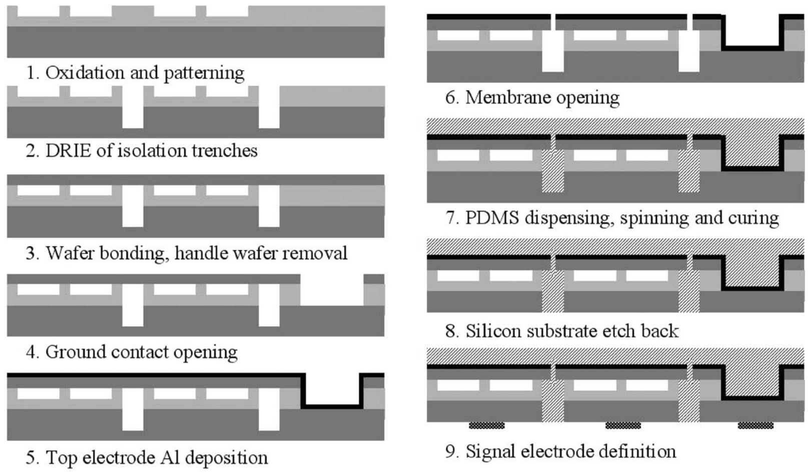


Fig. 6. Fabrication steps to incorporate CMUT elements onto a flexible silicon substrate.

experiments. The coating thickness for this particular PDMS as a function of spin rate was characterized first (Fig. 5). An empirical fitting to the data points was found to be

$$T = 58092 * S^{-1.23} \tag{1}$$

where T is the thickness of the PDMS film in micrometers, and S is the spin rate in revolutions per minute.

Fig. 6 shows the fabrication steps to incorporate CMUT elements onto a flexible silicon substrate. An n-type, highly conductive silicon wafer ($\rho < 0.025\ \Omega \cdot \mathrm{cm}$) was used to minimize the series resistance between the bottom electrode right underneath the cavity and the flip-chip bond pads on the back side of the wafer. First, cavities were defined on the front side of a prime silicon wafer by oxidation and etching (step 1). Deep trenches were then patterned and etched into the silicon substrate using DRIE (step 2). These trenches had widths varying between 6 and 20 μm, and a depth of about 150 μm. The wafer was then fusion bonded to an SOI wafer in vacuum and annealed at 1100 °C for 1 h. The silicon handle on the SOI wafer was dissolved in heated tetramethylammonium hydroxide solution, and the buried oxide was released in 6 : 1 buffered oxide etchant, leaving only the 1.83-μm-thick silicon device layer as the CMUT membrane (step 3). To connect the common top electrode to the back side of the wafer, the silicon membrane and oxide insulation layer on the dedicated common electrode area were opened up (step 4). The membrane was metallized by sputtering a 0.4-μm-thick aluminum layer (step 5). Holes with diameters of 4 to 10 μm were etched in the membrane overlapping the trench area to allow the PDMS to fill into the trenches (step 6). After this step, the top membrane was still continuous. After dispensing PDMS, the wafer was placed into a vacuum chamber for 2 min to allow air to be evacuated from the trenches. This step was repeated three times to ensure void-free PDMS filling in the trenches. The PDMS thickness on the array surface was controlled by the speed of the subsequent spinning step. Using the Dow Corning 1-4105 PDMS, a 30-μm thick layer was obtained by spinning at 500 r/min for 1 min. The PDMS was cured on a hot plate at 110 °C for 2 h (step 7). After etching the silicon substrate from the back side (step 8), the array elements were electrically isolated from one another, but mechanically linked by the PDMS in the trenches. Finally, a Ti/Cu/Au metal stack was deposited and patterned on the back side of the wafer to form the individual electrodes for each element (step 9).

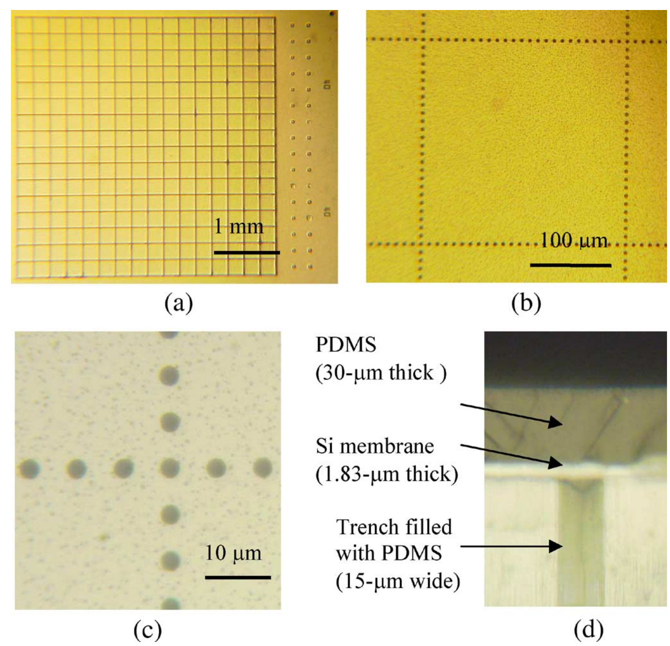


Fig. 7. Device photographs. (a) Front side view. (b) Magnified view of a single element. (c) Magnified view of through-wafer PDMS dispensing holes. (d) Cross-sectional view showing the trench, the membrane, and the PDMS coating and filling.

Fig. 7(a) shows the top view of the CMUT membranes corresponding to step 8 in Fig. 6. Magnified views of the holes on the membranes used to fill the trenches with PDMS are shown in Fig. 7(b) and (c). The PDMS completely filled the trenches without any voids, as seen in the device cross section [Fig. 7(d)].

III. Test Results and Discussions

The transducer arrays were characterized in air. The CMUT was biased at various dc voltages and a network analyzer (Model 8751, Hewlett-Packard Company, Palo Alto, CA) was

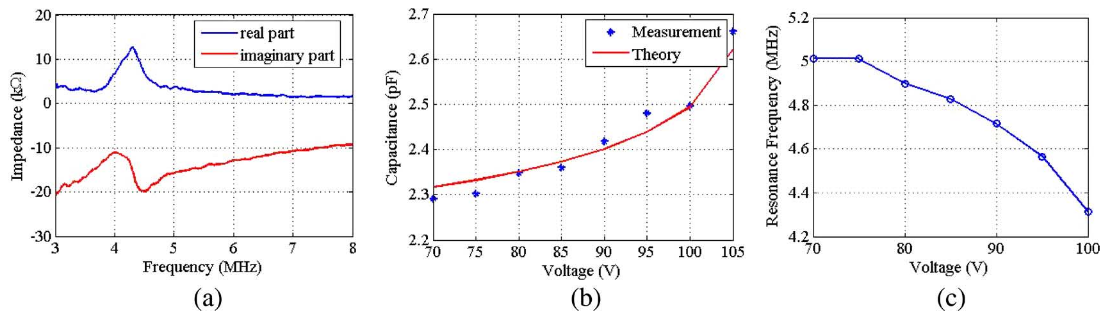


Fig. 8. Test results. (a) Electrical input impedance in air. (b) Device capacitance. (c) Resonant frequency.

TABLE II
CMUT CHARACTERISTICS

	With PDMS Coating		Without PDMS Coating	
	Measurement	Calculation	Measurement	Calculation
Collapse voltage (V)	120	105	98	97
Resonant frequency * (MHz)	4.5	4.4	10.4	11.5

* Measured at 80% of the collapse voltage.

used to measure the electrical input impedance. We used a microprobe (Model ACP40-W-GS-150, Cascade Microtech, Inc., Beaverton, OR) to make electrical contact on the back side of the CMUT array. Real and imaginary parts of the impedance are shown in Fig. 8(a). The low quality factor of the resonance in air compared to a similar CMUT without coating [23] is caused by the damping introduced by the PDMS film on the membrane.

The device capacitance was calculated using the impedance measurements. With increased dc bias, the capacitance increased due to the reduced cavity height as a result of the membrane deflection [Fig. 8(b)]. The measured capacitance was in good agreement with the values predicted by the analytical model. The resonant frequency in air was also extracted from the measurements made using the network analyzer. Fig. 8(c) shows the dependence of the open circuit resonant frequency on the dc bias voltage. The decreased resonant frequency is attributed to the spring softening effect of an electrostatically actuated system with increased dc bias voltage.

The collapse voltage of the CMUT membranes was measured as 120 V. At this voltage, the CMUT membrane contacts the bottom of the vacuum cavity, but no dc leakage current was observed from the signal electrodes to ground through the PDMS filling material.

The same measurements were also performed on CMUTs with the same physical parameters but without the PDMS coating. Table II summarizes the collapse voltage and resonant frequency for the CMUT, with and without the PDMS coating. The measurement results agree with the model within 13% of error. The differences can be explained by processing uncertainties, such as the gap and insulation layer thickness. Another possible cause for the discrepancies is the effects of the aluminum metallization [33], which is not considered in the model. The full effects of the PDMS coating on the CMUT performance are currently under investigation both by finite element simulation, and by experiments.

These arrays can bend when pushed in the center (Fig. 9). However, after bending, cracks form in the silicon membranes in the regions that overlap the trenches, and propagate to the active device areas [Fig. 10(a)]. This is because of the large-area, continuous single-crystal silicon membrane remaining on top of the trenches. A continuous silicon top membrane is needed to have an electrically continuous common top electrode. However, under large deformation, the large-area silicon membranes sustain stress intensities higher than the critical stress intensity of silicon, resulting in crack propagation [34]. Silicon ribbons (springs) have been used as interconnects for MEMS devices to provide better compliance without interrupting electrical continuity [35], [36]. Such ribbons will be incorporated into future designs to replace the continuous membranes in the trench area to reduce the probability of cracking [Fig. 10(b) and (c)]. This new design, however, is not necessary for side-looking catheters employing a 1-D array [2]. The connecting silicon on the front side of a 1-D array is not required because the top electrodes are readily accessible from the front side. Therefore, the silicon membrane linkage on the front side of a 1-D array can be completely eliminated.

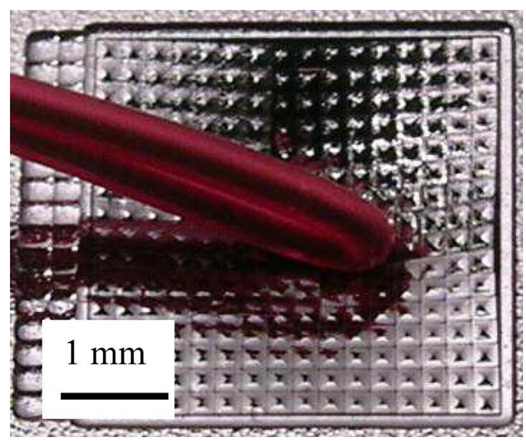
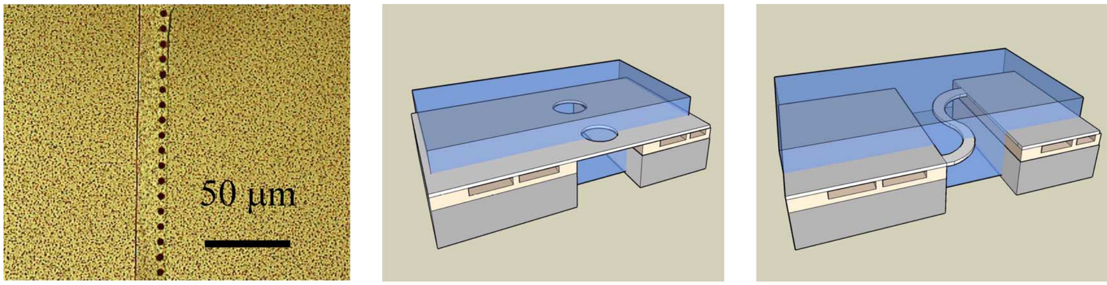


Fig. 9. Flexible 2-D CMUT array pushed by a wire on the back side.

IV. CONCLUSION

We demonstrated flexible silicon substrates based on PDMS-refilled through-wafer trenches. The finished device wafers can



(a) (b) (c)

Fig. 10. (a) Photograph of cracks on the membrane. (b) Schematic of current dispensing hole design. (c) Schematic of proposed design to eliminate cracking.

be handled the same way as regular wafers. These substrates can be stretched to conform to a curved surface, and be wrapped around catheter tips with a radius of 450 μm or less, and are potentially useful for IVUS applications. The technique presented in this paper can also be used to implement large flexible CMUT arrays to allow conformal coverage of an object in applications such as medical imaging, ultrasound therapy and nondestructive evaluation. The PDMS was shown to be able to withstand the high temperatures used in the flip-chip bonding process for integrating the CMUT to flexible PCBs or front-end ICs.

We also presented a fabrication process to incorporate CMUTs onto the flexible silicon substrate. Through-wafer electrical interconnections were also realized by this process. The CMUT device functionality was tested by capacitance and resonant frequency measurements. The PDMS provided sufficient electrical insulation between the array elements and ground.

In the current design, the flexibility of the CMUT array is limited by the large-area, continuous silicon membranes above the trenches. In future designs, narrow strips of silicon will be used to connect the neighboring elements to prevent cracking. Another topic of future study is the long-term reliability of the flexible silicon substrate based on trench refilling with PDMS.

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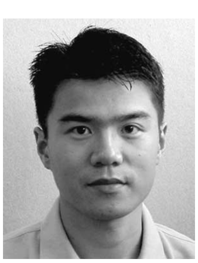

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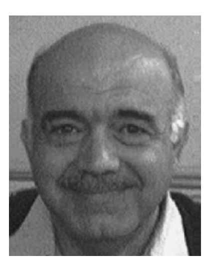

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