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Integration of trench-isolated through-wafer interconnects with 2d capacitive micromachined ultrasonic transducer arrays

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Abstract

This paper presents a method to provide electrical connection to a 2D capacitive micromachined ultrasonic transducer (CMUT) array. The interconnects are processed after the CMUTs are fabricated on the front side of a silicon wafer. Connections to array elements are made from the back side of the substrate via highly conductive silicon pillars that result from a deep reactive ion etching (DRIE) process. Flip-chip bonding is used to integrate the CMUT array with an integrated circuit (IC) that comprises the front-end circuits for the transducer and provides mechanical support for the trench-isolated array elements. Design, fabrication process and characterization results are presented. The advantages when compared to other through-wafer interconnect techniques are discussed.

Keywords: Capacitive micromachined ultrasonic transducer (CMUT); Trench isolation; Through-wafer interconnect; Post-processing; Flip-chip bonding

1. Introduction

Extensive research efforts have been carried out to develop large-area fully populated 2D ultrasonic transducer arrays [1–3]. These arrays are useful in applications such as real-time 3D ultrasound echocardiography and photo-acoustic tomography. It is difficult to route out electrical signals from the many array elements to the back-end hardware that performs signal processing. Traditional ultrasound transducers are based on the piezoelectric technology. Electrical interconnection to array elements can be realized by mechanically dicing array elements after the piezoelectric material is bonded to a printed circuit board (PCB), which is effectively a fanout structure [1,2]. Integration to IC is indirect, through the fanout structure, which adds parasitic capacitance that degrades signal integrity. It is challenging to scale down the kerf width as array element pitch decreases for high-frequency applications. Mechanical dicing becomes more difficult for irregular array geometries, such as annular ring-shaped geometries [4] and 2D arrays arranged in a non-Manhattan fashion.

The CMUT technology is a promising candidate for making 2D ultrasound transducer arrays because of the combination of the low-cost micromachining process and demonstrated performance advantages [3,5]. The lithographic fabrication process for making CMUTs can achieve arbitrary array geometries and is readily scalable in size. When incorporated with through-wafer interconnects, CMUT arrays can be directly integrated with front-end ICs. The integration of the front-end IC is important from a system-level perspective—it not only provides multiplexing to reduce the number of cables needed to communicate between the transducer and the signal-processing hardware, but also mitigates the undesirable effects of the parasitic capacitance from the lengthy cables. The existing interconnect scheme in 2D CMUT arrays, as well as many other types of MEMS transducer arrays, is based on through-wafer vias [6–13]. Through-wafer via holes are formed on the silicon substrate, and a conductive material such as doped polysilicon is deposited in the vias to bring electrical connection from the front side of the wafer to the back side. The through-wafer via process involves complex front and back side processes that include multiple

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thin film depositions, doping and etching before the wafer bonding step. These processes induce stress imbalance on the wafer and cause wafer warping. Consequently, it is difficult to fusion bond a silicon wafer with through-wafer via interconnects to an SOI wafer for making CMUTs [14]. The SOI wafer bonding technique is the preferred approach for making CMUTs because it offers higher fill factor (ratio between the active membrane area to the total element area) and better process control than the surface-micromachined CMUTs [15].

This paper presents a post-processed through-wafer electrical interconnect technique that is compatible with both the surface-micromachined and the SOI wafer-bonded CMUTs [16,17]. This technique differs from previously reported MEMS through-wafer via electrical interconnects in that it utilizes the silicon substrate itself as the conductive material and employs flip-chip bonding to provide mechanical support for the array elements (Fig. 1(c)). The trench-isolated interconnects reported in our work have a lower series resistance than comparable through-wafer via interconnects. Element-to-element cross-coupling capacitance is negligible. This technique enables thinning the silicon substrate down, which is not possible for pre-processed interconnects because of the difficulty in wafer handling. In our case, thinning the silicon substrate can enhance the transducer bandwidth by pushing the substrate reverberations out of the device operating frequency band. The design, fabrication and characterization of the interconnect as well as the CMUT performance are presented.

2. Design

The basic structure of a CMUT is a parallel plate capacitor with a rigid bottom electrode, and a top electrode that is located on a flexible membrane. Usually a number of membranes are connected in parallel to form a transducer element (Fig. 1(a)). In an array that consists of a number of elements, the top electrodes of the individual elements are connected together to form the common electrode. The previous approach for through-wafer interconnects is shown in Fig. 1(b) [3,7,8]. Micro-scale through-wafer vias filled with conductive material route the electrical signal from the front side to the back side of the wafer. The new approach reported in this paper is shown in Fig. 1(c). Instead of through-wafer vias, the highly conductive silicon substrate itself brings the electrical contact to the back side of the wafer. Through-wafer trenches separate the bottom electrodes from one another.

There are three major design criteria for the trench-isolated interconnects: (1) the cross-coupling capacitance between adjacent array elements should be small compared with the device capacitance; (2) the series resistance of the silicon interconnects should be insignificant relative to the device impedance; (3) the fill factor for the CMUT should be as large as possible for higher output power and broader fractional bandwidth [18]. Typically, for a 250 μm × 250 μm CMUT element, the device capacitance is 1–2 pF. For the electrical crosstalk to be negligible, the desired cross-coupling capacitance should be less than 0.1 pF. Fig. 2(a) shows the expected cross-coupling capacitance in air as a function of the substrate thickness and the trench width. Thinning the substrate down or increasing the trench width can readily achieve the desired negligible cross-coupling capacitance, with trenches of 10 μm sufficient for 400 μm thick wafers, and 5 μm for 200 μm thick wafers. Fig. 2(b) shows the expected series resistance as a function of the substrate resistivity for various thicknesses with an electrode size of 235 μm × 235 μm. When a highly conductive silicon wafer is used (∼0.01 Ω-cm), the theoretical series resistance is below 1 Ω, insignificant when compared to the CMUT impedance of many kilo Ohms. The upper limit of the device fill factor is determined by the width of the isolation trenches. Fig. 2(c) shows the dependency between the upper limit of device fill factor and trench width. Taking processing variations into consideration, four 48 μm wide, 220 μm

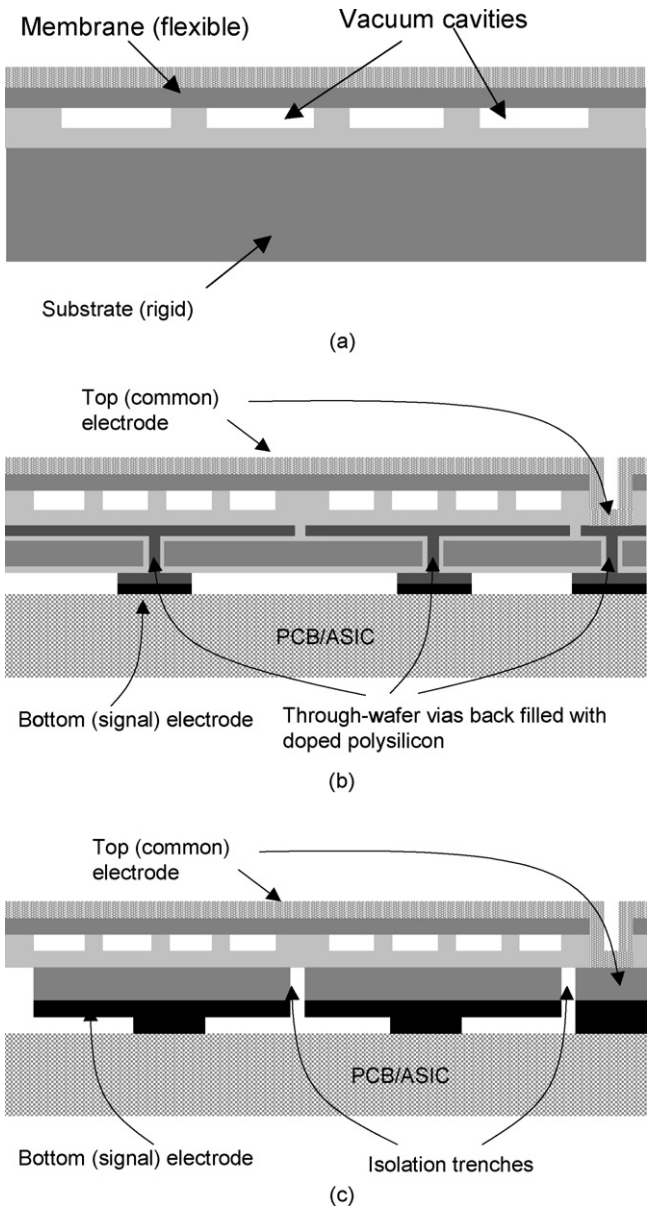

Fig. 1. (a) Cross-sectional schematic of a CMUT array element; (b) cross-sectional schematic of a CMUT array with through-wafer via interconnects flip-chip bonded to an IC chip; (c) cross-sectional schematic of a CMUT array with trench-isolated through-wafer interconnects flip-chip bonded to an IC chip.

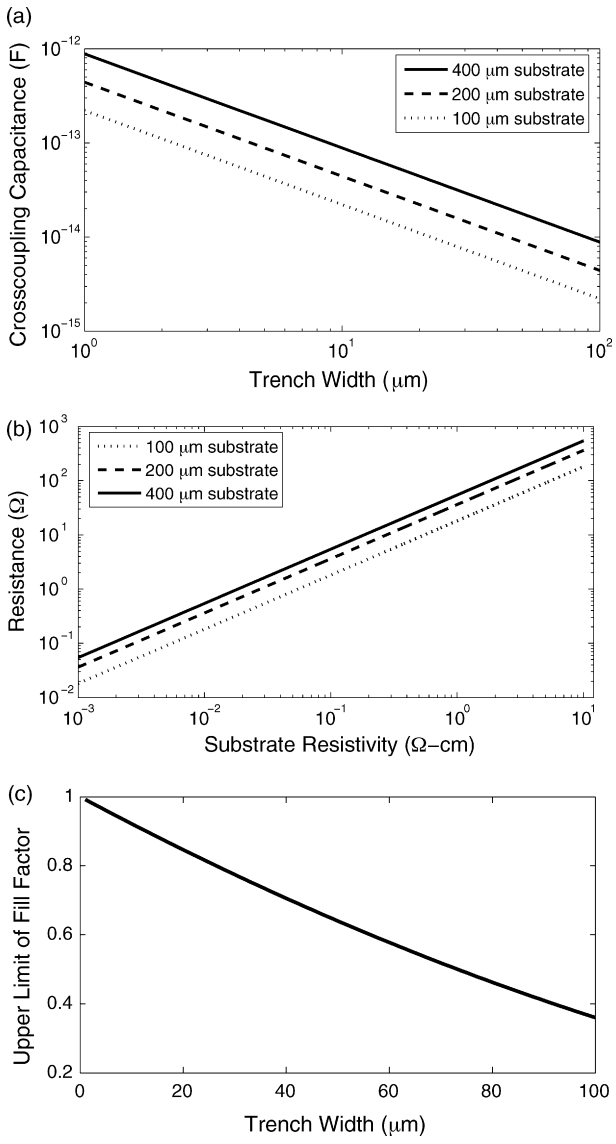

Fig. 2. (a) Theoretical element-to-element cross-coupling capacitance; (b) theoretical resistance; (c) upper limit of device fill factor.

long rectangular membranes are designed to form an element, with an isolation trench width of 15 μm, achieving a fill factor of 0.676. Table 1 summarizes the design parameters for the CMUT and interconnects.

Table 1
Device parameters of a trench-isolated CMUT array

Membrane width (μm)	48
Membrane length (μm)	220
Number of membranes/element	4
Membrane thickness (μm)	2.56
Cavity height (μm)	0.3
Substrate thickness (μm)	120–180
Trench width (μm)	15
Element pitch (μm)	250
Si wafer resistivity (Ω-cm)	<0.025
Riston film thickness (μm)	15
Fill factor (%)	67.6
Expected series resistance (Ω)	<1
Expected cross-coupling capacitance (pF)	<0.1

3. Fabrication process

The process sequence for CMUT arrays with through-wafer trench-isolated electrical interconnects is illustrated in Fig. 3. It consists of three major stages: the first is to form the CMUT cavities and membranes on the front side of the wafer (a–g); the second is the attachment to a carrier wafer and etching the through-wafer trenches (h–j); the last stage is flip-chip bonding the CMUT array to an IC chip and the releasing of the carrier wafer (k–m).

3.1. Fabrication of the CMUT cavity and membranes

The through-wafer trench-isolated CMUT fabrication starts with the formation of CMUT membranes on the front side of the wafer. Because SOI wafer bonding offers better process control than surface micromachining, it was selected as the method for making the CMUT membranes in this study. After growing a 0.22 μm thermal oxide layer, cavities are patterned and etched into the oxide. A second oxide layer with a thickness of 0.32 μm is grown to serve as the dielectric insulation layer between the conductive silicon membrane and the bottom electrode. During the second oxidation, the edge of the oxide side walls form a "hump" due to the diffusion growth nature of the thermal oxidation process—more oxide is grown on the edge than other areas. TSUPREM4 (Synopsys Inc., Mountain View, CA) simulation of such a hump is shown in Fig. 4. Because wafer-to-wafer fusion bonding requires smooth surfaces for good yield, these humps are removed in a plasma-etching step. Spin-coated photo resist is used as the etching mask. The mask layout is designed to accommodate any misalignment issue by utilizing self-alignment—this specific mask determined the final width of the rectangular cavities.

Next, an SOI wafer with a 2.56 μm device layer is fusion bonded to the oxide layer under vacuum and annealed at 1000 °C. The silicon handle wafer is removed by grinding and wet etching in heated tetramethylammonium hydroxide (TMAH) solution. The buried oxide (BOX) layer on the SOI wafer is removed in buffered oxide etchant (BOE). To bring electrical contact to the silicon substrate, the silicon membrane and the underlying oxide layer are patterned and etched in the ground contact area. An Al layer with a thickness of 0.3 μm is sputtered to cover the whole wafer front surface and patterned. At this point, the CMUT fabrication is finished, and the processing of electrical interconnect begins.

3.2. Carrier wafer attachment and through-wafer trench etching

The wafer front side is temporarily bonded to a quartz carrier wafer, which provides mechanical support and optical transparency for later processing steps. A 15 μm thick dry photoresist film (Riston CM206, Dupont, Wilmington, DE) is used as the bonding adhesive. The Riston resist film provides good adhesion, uniform thickness across the wafer, and reduces bubble formation and out-gassing during subsequent etching and met-

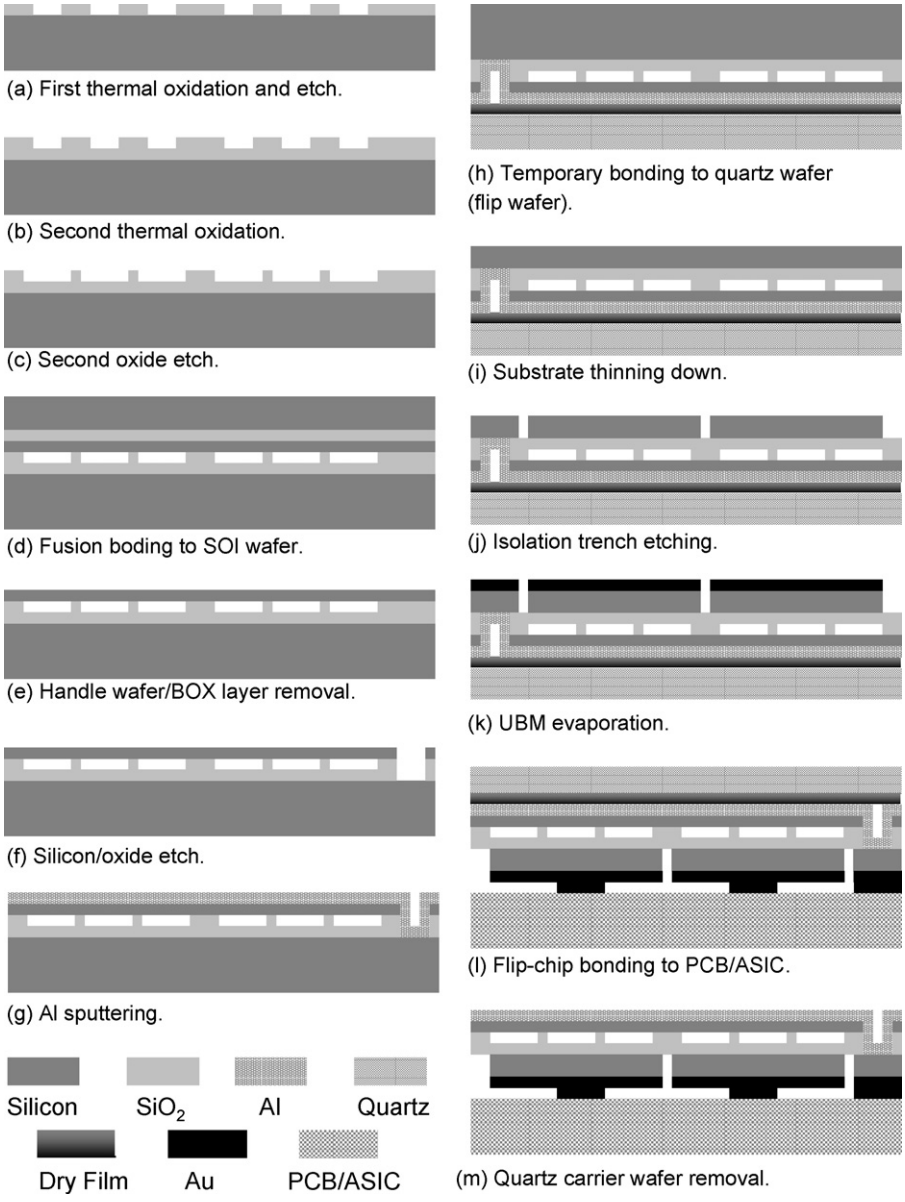

Fig. 3. Fabrication steps to integrate trench-isolated through-wafer interconnects with 2D CMUT arrays.

allization steps in high vacuum conditions. Regular photoresist (Shipley SPR 220-7, Rohm and Haas Electronic Materials, Phoenix, AZ) was also investigated for this temporary bonding purpose. However, the bonding quality is not satisfactory—some areas on the wafer demounted during the DRIE process due to the heat accumulation and solvent degassing from the photoresist.

The silicon substrate is thinned down to 120–180 μm using mechanical grinding and polishing. The ability for the post-processed through-wafer trenches to be thinned down has important implications. This step reduces the subsequent DRIE time and decreases the series electrical resistance and cross-coupling capacitance of the interconnects (Fig. 2(a and b)). For CMUTs, the adverse interference of substrate reverberation can be pushed out of the device operation frequency band by thinning down the substrate. Handling of the thinned-down wafers is like regular wafers, because the mechanical rigidity is now provided by the quartz carrier wafer.

Through-wafer trenches are etched into the substrate from the back side using DRIE in an inductively coupled plasma (ICP) etcher (Multiplex ICP Etcher, Surface Technology Systems, Newport, UK), with a 7 μm Shipley SPR220-7 photoresist as the etching mask. The photoresist is hard baked at a 110 °C oven for 1 h to prevent resist burning during the DRIE process. Although the selectivity between the silicon and oxide in the DRIE is excellent (>150:1), when the plasma etchant reaches the oxide layer, it will attack the silicon sideways, creating the "footing" problem [19]. The footing problem effectively reduces the active device area, and may even break through the vacuum cavities and hence change the device characteristics in an unpredictable manner. A solution to alleviate the footing problem is by modifying the etching recipe before the trench reaches the

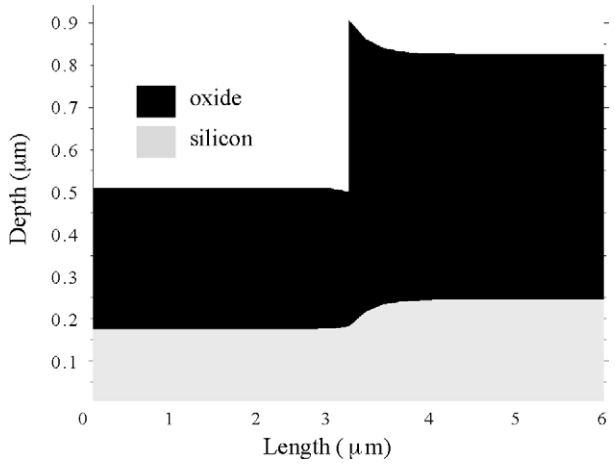

Fig. 4. TSUPREM4 simulation of the hump formation after the second oxidation step.

oxide layer to a reduced platen frequency for the plasma and an increased bias voltage. Micrographs illustrating severe footing problem occurring at the silicon-oxide interface as well as alleviated footing phenomenon in two fabrication runs are shown in Fig. 5(a and b), respectively. Table 2 summarizes the key differences in the process recipes.

3.3. Flip-chip bonding and carrier wafer releasing

After etching the trenches, a 200 Å/500 Å/2000 Å layer of Ti/Cu/Au is evaporated to form the metallization on the signal electrodes. This metal stack is needed to provide the under bump metallurgy (UBM) for the subsequent flip-chip bonding step. The evaporation is performed at a 45° angle relative to the metal source to prevent electrical shorting between neighboring pillars [20]. A guard ring structure is patterned around the array elements to prevent shorting in the edge elements. This evaporation technique eliminates the need for an additional lithography step to define the signal electrodes. Fig. 6(a) shows a back side view of 12 trench-isolated elements after the metallization step. Because the UBM evaporation was performed at an angle to the wafer surface, the device edge of the silicon wafer cast a metallization shadow on the carrier wafer. This shadow can be seen in Fig. 6(a).

Table 2
Key DRIE etching recipe parameters

	Regular etching recipe	Recipe to alleviate "footing" problem
Platen frequency (MHz)	13.56	0.38
RF bias voltage (V)	120	360
Passivation time/cycle (s)	7	7
Etching time/cycle (s)	12	12

Next, the wafer is diced to separate individual arrays for flip-chip bonding to IC chips with matching bond pad footprints. The IC chips that comprise the front-end circuits are custom designed, and fabricated by National Semiconductor Corporation, Santa Clara, CA. The aluminum flip-chip bond pads on the IC are coated with a 5 μm Ni/Au layer using an electroless plating process to provide the correct UBM for the solder bumps [21]. Sn/Pb eutectic solder balls with a diameter of 80 μm are placed on the bond pads using a solder jetting technique [22]. Pac Tech USA Inc., Santa Clara, CA, provided the electroless plating and solder jetting services. A picture of a part of an IC chip with solder balls in place is shown in Fig. 6(b). To flip-chip bond the chips, the CMUT and the IC are aligned and heated to 150 °C with 4 g/bump pressure. Following the alignment, the samples are placed into a nitrogen oven. The oven temperature is elevated to approximately 220 °C to allow for the solder reflow. Fig. 6(c) shows a 2D CMUT array bonded to an IC chip. The profile of solder joints between the CMUT signal electrodes and the IC bond pads after solder reflow is shown in Fig. 6(d).

After flip-chip bonding, mechanical support for the array elements is provided by the IC chip. The quartz carrier wafer can then be released. We experienced some difficulties in releasing the carrier wafer in the acetone solvent. The Riston film swells in the solvent, causing membrane detachment from the cavity at the center of the array. As an alternative releasing method, the quartz carrier can be mechanically polished away. Fig. 6(e) shows a section of a CMUT array surface with released quartz carrier wafer. Fig. 6(f) shows a corresponding surface profile of the CMUT surface, taken by a Zygo surface profiler (Model NewView 200, Zygo Corporation, Middlefield, CT), demonstrating a flat and smooth device surface.

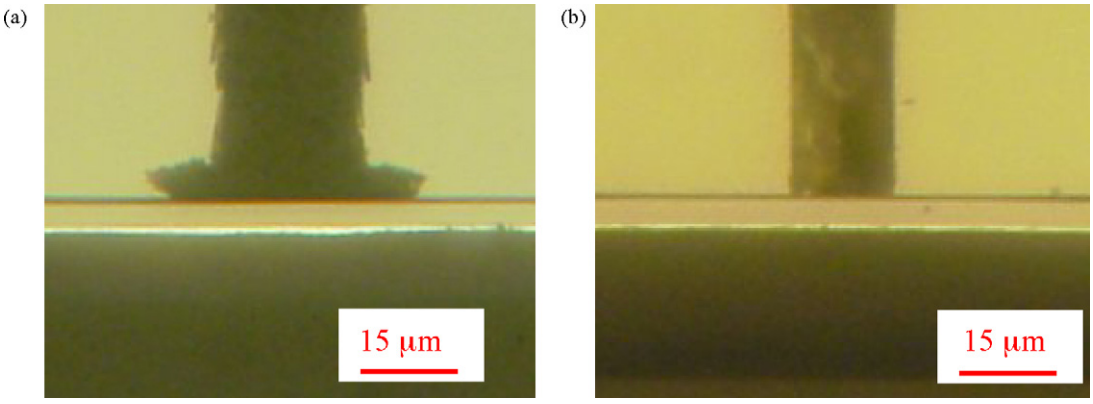

Fig. 5. (a) Through-wafer trench with footing; (b) footing is minimized.

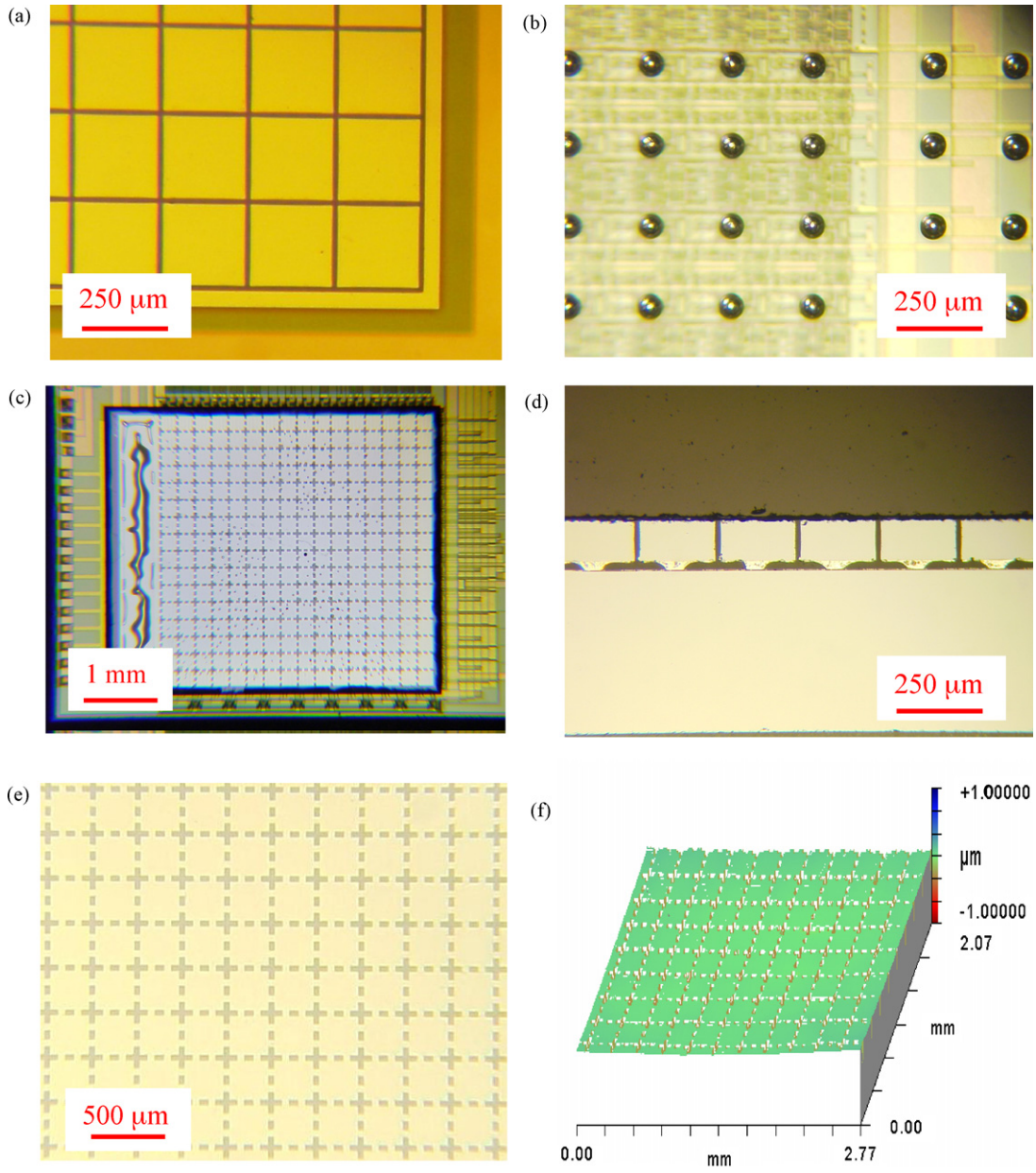

Fig. 6. (a) Back side electrodes; (b) a section of an IC chip with eutectic solder balls placed using solder jetting; (c) a trench-isolated 2D CMUT array flip-chip bonded to an IC chip; (d) isolation trench and solder joint profiles after reflow; (e) array surface after releasing quartz carrier wafer; (f) corresponding optical profile.

4. Characterization

Because a simple quartz fanout chip as shown in Fig. 7 offers more testing flexibility than a custom-designed IC, trench-isolated CMUTs flip-chip bonded to such a fanout chip were used for the characterization.

A network analyzer (Model 8751, Hewlett Packard Company, Palo Alto, CA) was used to measure the input impedance of the trench-isolated CMUT array elements in air. Simulations based on an equivalent circuit model in Ref. [23] were also performed. Fig. 8 shows a comparison and a good fit between the predicted and measured electrical input impedance of a CMUT element at a bias voltage of 110 V. When the DC bias voltage is high enough so that the electrostatic force overcomes the mechanical restoring force, the membrane will collapse to the bottom of the vacuum cavity. Using the same setup, the collapse voltage was determined by increasing the bias voltage until the fundamental resonant frequency changes abruptly, which was found to be 175 V (reasonably close to the predicted value of 180 V).

The real part of the input impedance at 20 MHz was extracted from the input impedance measurements performed with the network analyzer to determine the total series resistance. Since 20 MHz is a significantly higher frequency than the open circuit resonant frequency of around 8 MHz, and the CMUT is a high-Q device in air, the real part of the CMUT impedance at this frequency is negligible. The aluminum traces on the quartz fanout board have well defined geometries; resistance due to these traces was calculated and subtracted from the total measured resistance to find the resistance due to the trench-isolated

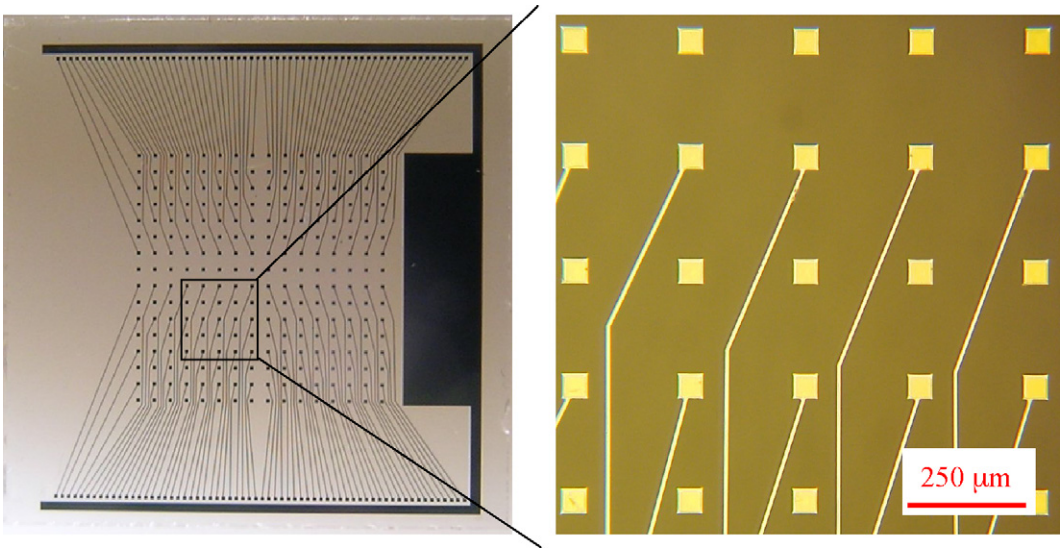

Fig. 7. Quartz fanout board.

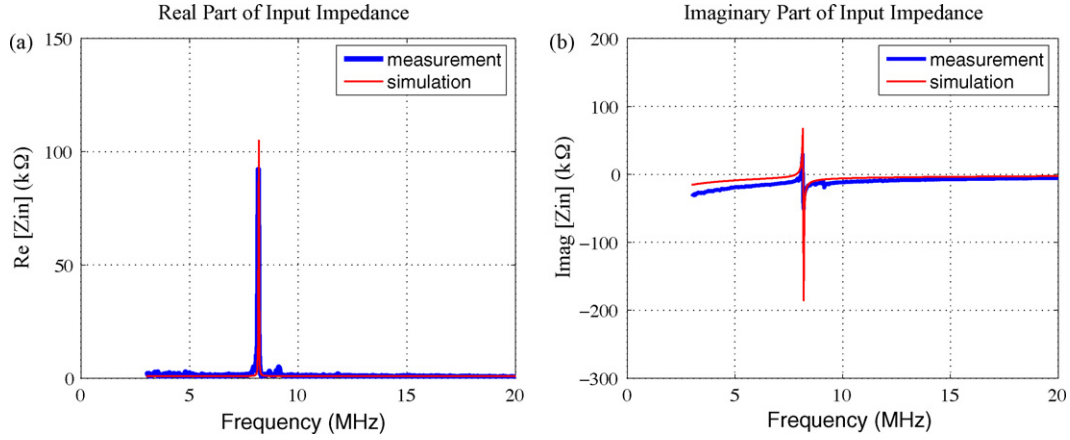

Fig. 8. Real and imaginary part of electrical input impedance in air.

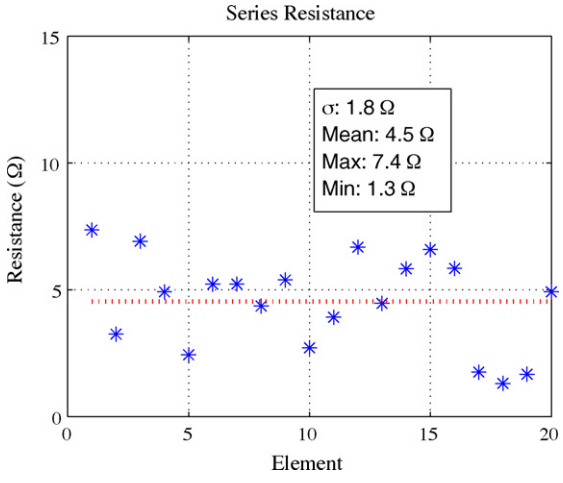

Fig. 9. Measured resistance values for 20 interconnects.

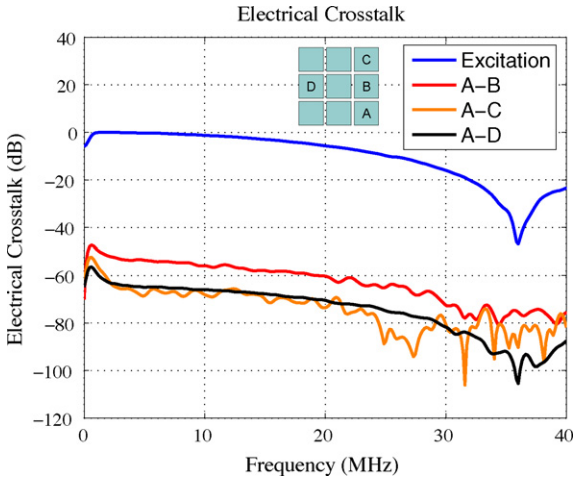

Fig. 10. Electrical crosstalk.

interconnect and the flip-chip bonds. Fig. 9 shows the resistance values for 20 interconnects. The average resistance is 4.5 Ω, and the standard deviation is 1.8 Ω. The series resistance is reduced when compared with the 20 Ω resistance associated with the previously reported through-wafer via interconnects for CMUTs [3,7,8].

Element-to-element electrical crosstalk was measured by exciting one element with a 32 V, 50 ns pulse, and detecting

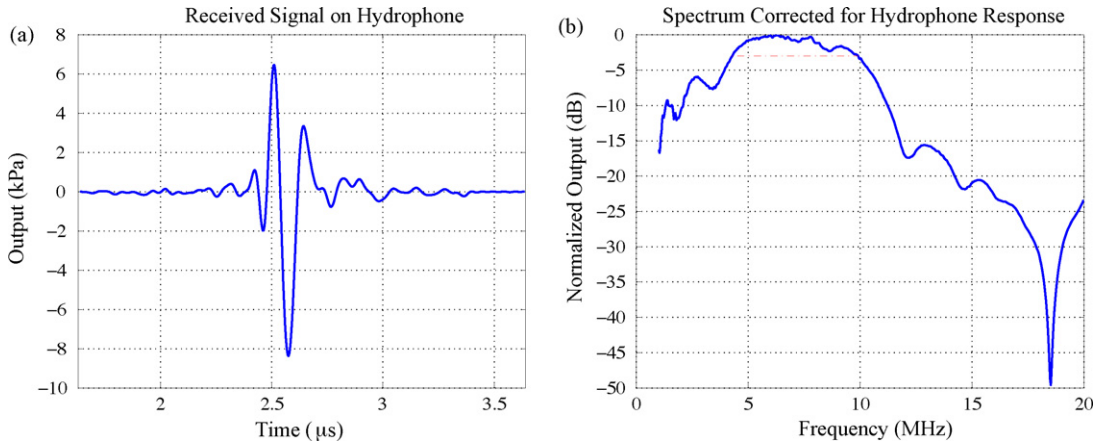

Fig. 11. Hydrophone measurement and corresponding spectrum.

the electrically coupled signal from neighboring elements. A pulse/function generator (Model HP 8116, Hewlett Packard Corp., Palo Alto, CA) was used as the AC source in the measurements. Fig. 10 shows the measurement results in the frequency domain. Both the excitation and received pulses were measured on a 1 MΩ load. In the worst case where two elements are next to one another (A and B), the electrical crosstalk is less than −53 dB at 5 MHz, corresponding to a coupling capacitance of about 29 fF. The electrical crosstalk was measured to be 10–20 dB lower when the receiver termination resistance is 50 Ω.

Finally, a trench-isolated CMUT array bonded to a fanout board was tested in immersion. A hydrophone (Model PZT-Z44-0400, ONDA Corp., Sunnyvale, CA) was used to measure the output pressure. The hydrophone was positioned at a distance of 3 mm from the transducer surface. A 17 dB, 10 kHz to 25 MHz, 50 Ω preamplifier was used to amplify the hydrophone signal before it was read into an oscilloscope. The device was biased at 80 V DC. A 30 V unipolar pulse with a pulse width of 100 ns was applied to the device, and the oscilloscope readings were recorded (Fig. 11(a)). The Fourier transform of the signal measured with the hydrophone, after correcting for the hydrophone frequency response, has a center frequency of 6 MHz, and a 3 dB fractional bandwidth of 80% (Fig. 11(b)).

5. Conclusion

Integration of trench-isolated through-wafer interconnects with 2D CMUT arrays has been demonstrated. CMUT devices with trench isolations were tested both in air and in immersion. Fabrication of these interconnects is compatible with both the surface micromaching process and the wafer bonding process for making CMUTs. When compared to the existing interconnects based on through-wafer vias, the trench isolation process is significantly simplified. The series resistance is reduced to 4.5 Ω from approximately 20 Ω, and the substrate thickness can be varied for optimized device performance. Element-to-element electrical cross coupling is less than −53 dB and is therefore negligible. Unlike the mechanical dicing technique used for the piezoelectric ultrasound transducer arrays, this technique is readily scalable with varying device sizes. It can also be applied to fabricate arrays with arbitrary array geometries.

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