The Search for Cathode and Anode Traps in High-Voltage Stressed Silicon Oxides

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ABSTRACT

When silicon oxide is stressed at high voltages, traps are generated inside the oxide and at the oxide's interfaces. The traps are negatively charged near the cathode and positively charged near the anode. The charge state of the traps can be easily changed by application of low voltages. Several models of trap generation have been proposed. These models involve either electron impact ionization processes or high field generation processes. We have attempted to determine the relative trap locations inside the oxides for oxides between 5 and 80 nm thick, in order to determine which processes are most likely. No evidence for a higher density of traps near the anode in any of these oxides was found, casting doubt on the efficiency of the impact ionization process in trap generation, even in thicker oxides. These data would support a trap generation model controlled by the high fields inside the oxides.

Introduction

It is well known that during high voltage stressing of thin oxides, traps are generated inside the oxides and at the oxides' interfaces. The traps are negatively charged near the cathode[1] and positively charged near the anode.[2] The charge state of the traps can easily be changed and repetitively cycled between positive and negative by the application of low voltages after the stress voltages have been removed.[3] These traps are responsible for the triggering of dielectric breakdown.[4-6] The statistical dependence of time dependent dielectric breakdown (TDDB) distributions on the trap generation has been calculated[4] and confirmed by coupling measured TDDB distributions with measured trap generation.[5] A recent modification of the statistical breakdown model has shown that the triggering mechanism for breakdown is the local generation of a high current leakage path from the cathode through the oxide to the anode,[6] resulting in a region of local heating, followed by thermal runaway.

It is not yet clear how or where the traps are generated in the oxide. One possible trap generation process involves hot electrons causing impact ionization near the anode, where the electron energy is maximum.[7] Impact ionization would not be a significant trap generation process in oxides thinner than about 20 nm, due to the limited amount of energy the electrons can gain from the oxide field of a thinner oxide.[7,8] It is not clear how impact ionization, a reversible process, can lead to trap generation, an irreversible process. Another possible trap generation process involves coupling the high oxide field to the lattice, causing the breaking of atomic bonds and the subsequent motion of the atoms to new sites.[9] An analysis of the energies involved in the trap generation processes has shown that a likely source of the trap generation is the formation and coalescence of vacancy defects in the oxide and is activated by the high electric fields present during the high voltage stresses.[10] Local asperities at the cathode have been correlated with low times-to-breakdown,[11] probably due to locally higher trap generation caused by locally higher fields. It is possible that the trap generation process is largely field dependent but could be catalyzed by the release of holes[8] or hydrogen[12] near the anode.

One model of trap generation that predicts a spatial distribution to the traps is the impact ionization model, in which more traps are generated near the anode, where the electron energy is the highest. Several attempts have been made to clarify the positions of the traps inside the oxides, however, the interpretation of data concerning actual trap positions, rather than just centroids of the traps, is most difficult.[13] Measurements of the drop of the tunneling currents, caused by the negatively charged traps near the measurement cathode in 10 nm thick oxides, following both positive and negative stressings, have shown that the traps are relatively uniformly distributed throughout 10 nm thick oxides.[14] However, this data, being taken on oxides less than 20 nm thick, did not rule out the possibility that more traps were generated near the anode in thicker oxides, where the electron energies were higher. In the work to be described below, an attempt was made to measure different trap densities near the anodes and cathodes of thicker oxides, up to oxides as thick as 80 nm. No evidence was found to indicate that there were more traps near the anode than near the cathode.

Experimental

Oxides with nominal thicknesses of 5, 10, 20, 40, and 80 nm were fabricated using highly reliable localized oxidation of silicon (LOCOS) processes at four different semiconductor manufacturing facilities using both p-type and n-type substrates. The oxides were representative of the high quality, state-of-the-art oxides that are presently being manufactured. The oxide areas varied from manufacturer to manufacturer, but were in the range between 10^{-6} and 10^{-3} cm^2. In none of the oxides were either extrinsic early breakdowns or LOCOS edge effects observed. The measurements described below were performed in the dark if the silicon surface was in accumulation and with light shining on the periphery of the oxide if the silicon surface was in inversion or depletion, to avoid deep depletion effects.

Prior to any stress measurements, two of each of the different thicknesses of oxides were sacrificed to obtain current-voltage (J-V) characteristics to breakdown. The J-V measurements were normalized to the oxide areas. The sweep rate for the J-V measurements was approximately 1 MV/s, for all of the different thicknesses of oxides. Both positive and negative gate voltages were used for the J-V measurements. A set of J-V characteristics to breakdown

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have been shown in Fig. 1 for a set of oxides fabricated on n-type silicon using positive gate voltages. All of the oxides studied here were characterized by low pretunneling leakage currents, typically less than 10^{-14} A prior to the onset of tunneling, and Fowler-Nordheim (F-N) tunneling currents in the tunneling regime. The J-V characteristics were used to determine the breakdown fields, the magnitude of the low level, pretunneling leakage currents, the voltages at which the oxides were stressed, and the voltages at which the trap densities were characterized. The breakdown fields dropped as the oxide thicknesses increased, in agreement with previously reported data.[1]

After the J-V characteristics had been measured, new oxides were used for the trap location experiments. The traps were generated inside the oxides by the application of high stress voltages. Both positive and negative stress voltages were used in order to generate different densities of traps near the stress anodes and stress cathodes. Two techniques were used to determine the trap locations inside the oxides. In one technique, the tunneling currents were measured as a function of time and measurement voltage polarity before and after the traps had been generated. The voltages used to measure the tunneling currents, in this technique, were low enough to be below the threshold at which significant traps were generated, and were generally 2 to 3 MV/cm less than the stress voltages. In the second technique, J-V characteristics were swept to relatively low, nonstressing, tunneling voltages and the stress induced leakage currents (SILCs) were measured. The SILCs were used as a measure of the trap densities near the electron injecting interface. In both techniques, both positive and negative measurement voltages were used to sample the traps generated near the stress anode and stress cathode. In this paper the term "stress anode" or "stress cathode" is used to specify which interface was the anode or cathode during the stress. In the case of positive stress voltages, the stress cathode and electron injecting interface was the substrate. In the case of negative stress voltages, this interface was the gate. Since there were no stress polarity effects measured using either of the trap detection techniques described above, it is not necessary to explicitly describe whether positive or negative gate voltages were used to stress the oxides, except for illustrative examples. Implicit in both of these measurements was the assumption that the traps, once generated, did not move throughout the oxide, and the charge state of the traps could be changed by the application of low voltages after the stresses had been removed.[3] Typical trap densities measured after either positive or negative gate voltage stressing at 10 MV/cm for 100 s, during which a fluence of 1-2 C/cm^2 had passed through the oxide, were approximately $10^{19}/cm^3$.

Dependence of Tunneling Currents on Trap Location

When a constant high voltage was applied to an oxide, the tunneling current initially rose due to the anomalous positive charge and then decayed due to the negatively charged traps generated near the cathode.[1] This correlation of the decay of the tunneling current with trap generation has been used to calculate the coulombic cross section of the charged traps as 3×10^{-13} cm^2.[15] The charge state of both types of traps was easily changed by the application of low, nontunneling voltages of opposite polarity to the stress polarity.[3] Since the traps were charged and discharged by the tunneling of electrons into and out of the traps, it often took thousands of seconds to complete the charge-state reversal process.[16] The trap charging/discharging took place faster at higher voltages. The symmetries of the trap generation and the charging/discharging processes to either stress polarity or charging/discharging polarity suggested that the charge state of the traps was being changed, but that the traps were remaining fixed in their positions inside the oxide.

The oxides described above were stressed at both positive and negative gate voltages. The tunneling currents were measured before and after the stresses using both positive and negative tunneling voltages. The measurement voltages were chosen to be about 2 to 3 MV/cm less than the stress voltages to ensure that the measurement voltages only sampled the traps near the cathodes and did not generate any new traps. Whenever the polarity of the measurement voltage was opposite to the stress voltage polarity, sufficient time was allowed to completely change the charge state of the traps, before the tunneling currents that were used to detect the traps were measured.

The tunneling currents, measured at relatively low tunneling voltages, on 10 nm thick oxides have been shown in Fig. 2 for oxides stressed with negative gate voltages and in Fig. 3 for oxides stressed with positive gate voltages. During positive gate voltage stressings the stress cathode was the substrate and the stress anode was the gate, with the opposite nomenclature applying during negative gate voltage stressings. Both polarities of low tunneling voltages were used to sample the traps near the stress cathode and stress anode. Positive measurement voltages sampled the trap densities near the substrate and negative measurement voltages sampled the trap densities near the gate, regardless of stress polarity. The tunneling currents were measured for 100 s and, at the low tunneling voltages at which these measurements were made, the tunneling currents were constant, indicating no additional trap generation at the low tunneling measurement voltages. The low

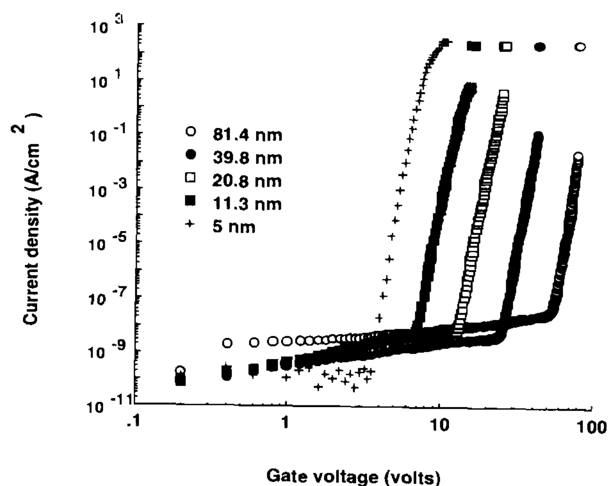

Fig. 1. Current-voltage characteristics of the 5 to 80 nm thick oxides showing the low pretunneling leakage currents and the Fowler-Nordheim tunneling currents. All oxides were 5×10^{-5} cm^2. Notice that the breakdown electric field dropped as the oxide thickness increased.

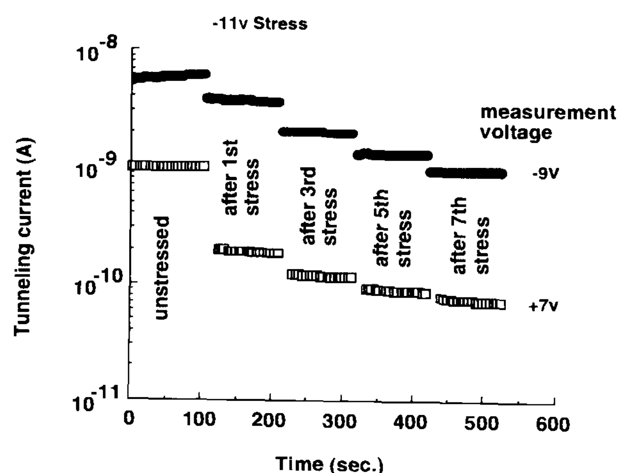

Fig. 2. Tunneling currents measured at low tunneling voltages following negative gate voltage stressings. All oxides were 1×10^{-4} cm^2.

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tunneling currents were smaller after each stress cycle due to the increase in the trap densities with increased numbers of stress cycles.[1] The stresses were performed at the voltages shown in Fig. 2 and 3 for 100 s per stress cycle. The trap densities were calculated from the decay of the transient current following removal of each stress voltage pulse using the tunneling front model.[17] It was found that the drops in the tunneling currents shown in Fig. 2 and 3 were: (*i*) independent of measurement polarity indicating that the densities of traps near the stress anodes were similar to the densities of traps near the stress cathodes for both stress polarities; (*ii*) independent of stress polarity indicating that both positive and negative gate voltage stresses were equally effective in generating traps inside the oxides; and (*iii*) were proportional to the trap densities measured after the stress voltages had been removed. The similarity of the decays in the low voltage tunneling currents for the two different stress polarities and the two different measurement polarities indicated that the traps in these 10 nm thick oxides were relatively uniformly distributed throughout the oxides.

Similar measurements were taken on the 5 and 20 nm thick oxides with similar results. The magnitude of the decays in the low tunneling currents decreased as the oxide thicknesses decreased, due to screening of the fields in the thinner oxides.[18,19] Attempts to repeat these measurements on the 40 and 80 nm thick oxides were not conclusive due to the lower breakdown fields measured on these thicker oxides, as shown in Fig. 1. It was difficult to stress the oxides at high enough fields, using a constant stress voltage, to generate a significant number of traps in the thicker oxides before dielectric breakdown occurred, and also to measure the low tunneling currents. The second technique described below was used to sample the traps in the thicker oxides. This second technique was also used to sample the traps in the thinner oxides.

Dependence of Stress Induced Leakage Currents on Trap Location

Since it proved difficult to use the decay of the low-voltage tunneling current to sample the traps in the thicker oxides, it was decided to use the increase in the SILCs as a measure of trap distributions in the oxides. It is well known that SILCs are related to trap-assistance tunneling processes in thin oxides.[12,17-23] It has been shown that the SILCs are proportional to the stress-induced trap densities.[17] Recent measurements have shown that the SILCs are composed of a dc component and a transient, 1/time, component.[18] Both components of the SILCs are proportional to the trap density, with the dc component becoming significant in oxides thinner than 7 nm.[18]

The low level pretunneling currents were measured in all the oxides. The oxides were then stressed at high voltages, and the SILCs were measured. Both positive and negative stress voltages were used and both positive and negative SILC measurement voltages were used. The positive measurement voltages sampled the traps near the substrate and the negative measurement voltages sampled the traps near the gate. The magnitudes of the SILCs were used as a measure of the trap densities near the electron injecting interface.

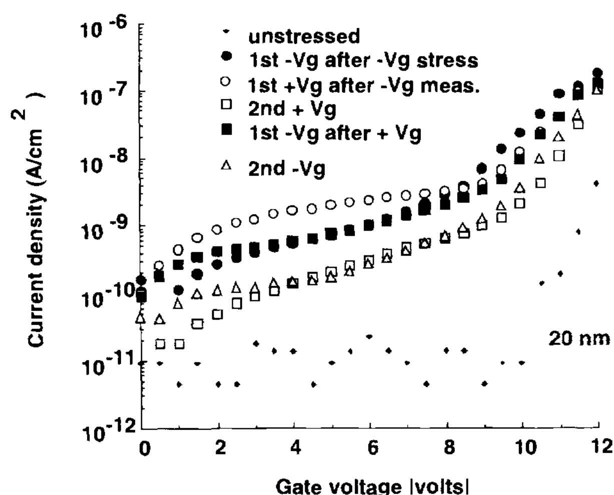

Fig. 4. SILCs and OTOLCs measured on a 20 nm thick oxide after negative gate voltage stressing. All oxides were 2.5 × 10^{-4} cm^2.

A note of caution is in order concerning the SILC measurement, whenever the measurement polarity is changed. Whenever the stress polarity and measurement polarity were different, or whenever the measurement polarity was changed, it was necessary to exercise care to ensure that the SILCs that were being measured did not contain the one-time-only-leakage-current (OTOLC) caused by the transient tunneling charging/discharging of the traps.[17,24] An example of the SILCs that were measured on a 20 nm thick oxide fabricated on p-type silicon after negative gate voltage stressing at −20 V has been shown in Fig. 4. The data shown in this figure show that the SILCs measured on an oxide depended on the sequence in which the SILCs are measured. The measurement sequence was as follows: (*i*) measure the unstressed low-level leakage current (curve 1); (*ii*) stress the oxide at −20 V for 100 s and gen-

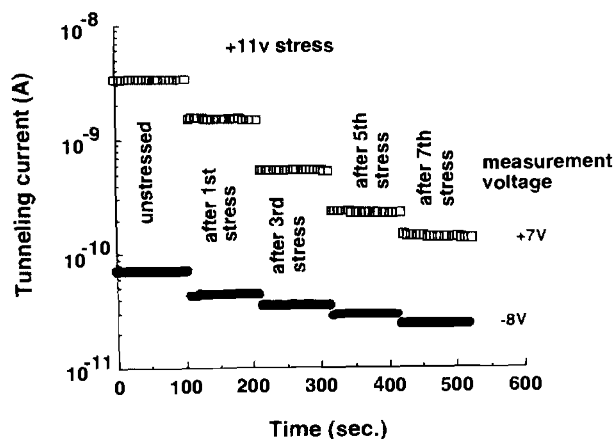

Fig. 3. Tunneling currents measured at low tunneling voltages following positive gate voltage stressings. All oxides were 1 × 10^{-4} cm^2.

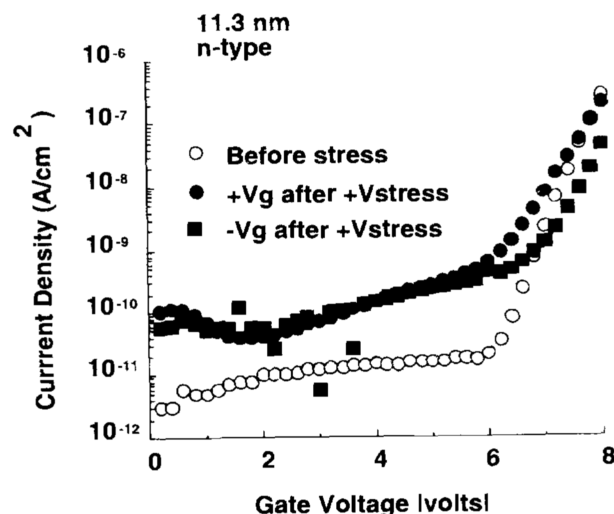

Fig. 5. Polarity dependence of SILCs measured on 11.3 nm thick oxides showing no dependence on the measurement polarity. All oxides were 5 × 10^{-5} cm^2.

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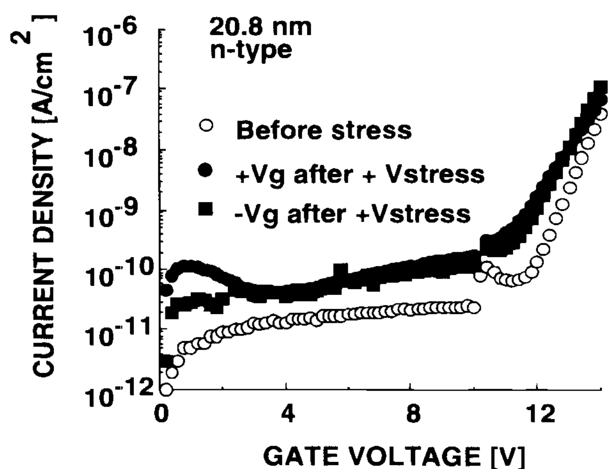

Fig. 6. Polarity dependence of SILCs measured on 20.8 nm thick oxides showing no dependence on the measurement polarity. All oxides were 5×10^{-5} cm^2.

erate traps inside the oxide; (*iii*) measure the SILC at negative gate voltages (curve 2); (*iv*) measure the SILC at positive gate voltages (curve 3); (*v*) remeasure the SILC at positive gate voltages (curve 4); (*vi*) remeasure the SILC at negative gate voltages (curve 5); (*vii*) remeasure the SiLC at negative gate voltages (curve 6).

The first SILC measured after a high-voltage stress showed a higher SILC than subsequent SILCs; compare curve 1 with curve 6. The SILC showed a OTOLC whenever the measurement polarity was changed; compare curve 3 with curve 6 or compare curve 5 with curve 4. This OTOLC was caused by the transient tunnel charging/discharging of the traps near the interfaces.[17,24] The first SILC measured after the stress was higher than subsequently measured SILCs; compare curve 2 with curve 6. It should be noted that once a SILC as shown in curve 4 or curve 6 had been measured, all subsequent SILCs measured with the same polarity were identical. Similar results to those shown in Fig. 4 were obtained on all of the oxides following either positive or negative gate voltage stresses. Thus, the SILCs reported below, for the different thicknesses of oxides, will all be the second SILCs measured at the same measurement polarity to avoid the complications of the OTOLCs.

The SILCs measured on an 11.3 nm thick oxide fabricated on n-type silicon after positive gate voltage stressing have been shown in Fig. 5. The SILCs measured with pos-

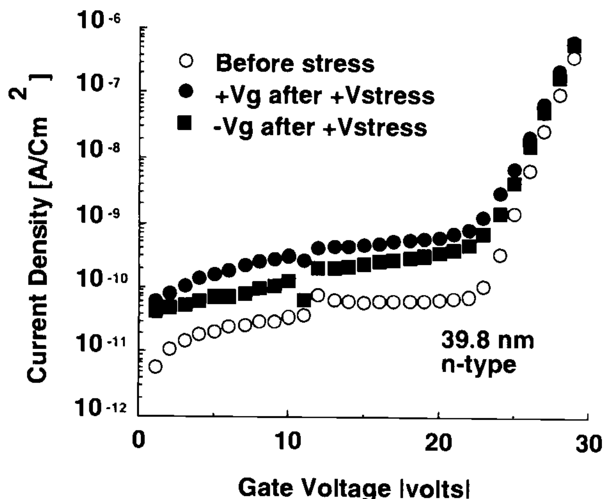

Fig. 7. Polarity dependence of SILCs measured on 39.8 nm thick oxides showing no dependence on the measurement polarity. All oxides were 5×10^{-5} cm^2.

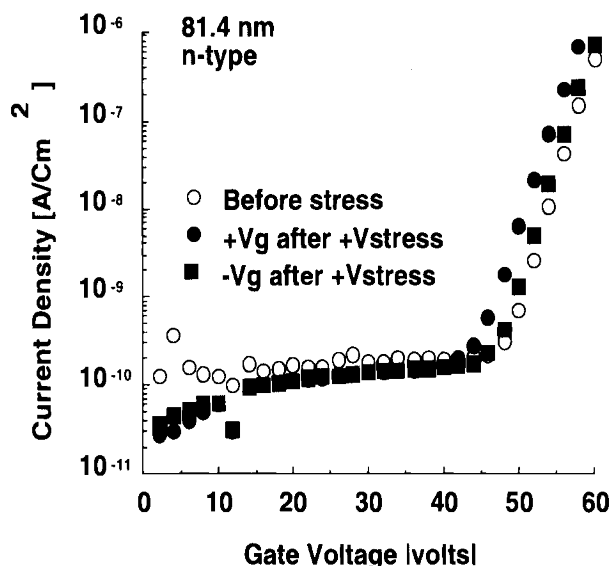

Fig. 8. Polarity dependence of SILCs measured on 81.4 nm thick oxides showing no dependence on the measurement polarity. All oxides were 5×10^{-5} cm^2.

itive and negative gate voltages were nearly identical indicating that the trap densities were nearly the same near the stress cathode and stress anode. Similar measurements made on 20.8 nm thick oxides, 39.8 nm thick oxides, and 81.4 nm thick oxides have been shown in Fig. 6, 7, and 8, respectively. In no case was it possible to detect higher SILCs, and hence, more traps, near the stress anode than near the stress cathode, indicating that the trap densities near each interface were nearly identical. There was no evidence for more traps near the stress anode, where the electron energies were higher, even for the thicker oxides. The small SILCs measured in the 81.4 nm thick oxide were due to the lower trap densities generated in these oxides. The thicker oxides had lower trap densities because it was not possible to stress these oxides at the high fields used for the thinner oxides due to the lower breakdown fields, as shown in Fig. 1.

Discussion of Results

The changes in the low voltage tunnel currents shown in Fig. 2 and 3 gave no indication that there was a higher density of traps generated near the stress anode than near the stress cathode. The tunneling currents dropped after each stress cycle, indicating that more traps had been generated during each of the stress cycles. The low voltage tunneling currents dropped by about the same percentages, whether the measurement voltages were sampling the traps generated near the stress anode or near the stress cathode, after either polarity of stress voltages had generated the traps. Trap generation was relatively independent of stress polarity. Thus, there was no evidence for higher trap densities near the stress anode. It should be noted that the differences that have been measured in the time to breakdown when the stress polarity was changed[11] were due to asperities at the electron injecting interface, leading to high local densities of traps, and not due to intrinsic polarity dependences of trap generation.

The SILCs were used as a measure of the traps generated inside the oxides, particularly in the thicker oxides where the low voltage tunneling currents were not useful for trap measurements. These data, shown in Fig. 5 through 8, also did not show any evidence that there were more traps generated near the stress anode than near the stress cathode. Thus, there was no evidence that impact ionization near the stress anode was a dominant mechanism causing trap generation inside the oxides. When using SILCs to characterize traps inside oxides it was necessary to account for the OTOLC.

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Conclusions

Two techniques were used to attempt to find differences in trap densities near the stress anodes and stress cathodes in silicon oxides. Even in thick oxides, where more traps were expected to be found near the stress anode, there was no evidence of higher trap densities near the anode. Thus, it appears that impact ionization is not the dominant cause of trap generation inside silicon oxide, and trap generation caused by the high electric fields may be the dominant source of the stress-generated traps.

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