Capacitive Micromachined Ultrasonic Transducer Technology for Medical Ultrasound Imaging

A. S. Ergun, X. Zhuang, Y. Huang, O. Oralkan, G. G. Yaralioglu and B.T. Khuri-Yakub

E. L. Ginzton Laboratory, Stanford University, Stanford, CA, 94305, USA;

ABSTRACT

Capacitive micromachined ultrasonic transducer (cMUT) technology has been recognized as an attractive alternative to the more traditional piezoelectric transducer technology in medical ultrasound imaging for several years now. There are mainly two reasons for the interest in this technology: Micromachining is derived from the integrated circuit technology and therefore shares the well-known advantages and experience of it. Also, capacitive transduction using thin membranes has fundamental superiorities over the piezoelectric transduction mechanism such as wide frequency bandwidth.

Capacitive micromachined ultrasonic transducers are essentially capacitor cells where the two plates of the capacitor, the membrane and the substrate, are separated with a vacuum sealed cavity. Typically, a cMUT is made of many micro-scale capacitor cells operating in parallel. This paper describes a new fabrication technique for building cMUTs which is called the wafer-bonding method. In this method, the cavity and the membrane are defined on separate wafers and brought together by wafer-bonding in vacuum. The wafer-bonding method has several advantages over the traditional sacrificial release method of cMUT fabrication. It allows greater flexibility in the cMUT design which means better device performance. It reduces the number of process steps, device turn-around time, and increases the overall uniformity, reliability. and repeatability. Device examples of one-dimensional and two-dimensional arrays designed to work in the 1 to 50 MHz range with 100 % fractional bandwidth highlight the advantages of this method, and show that cMUT technology is indeed the better candidate for next generation ultrasonic imaging arrays.

Keywords: Capacitive Micromachined Ultrasonic Transducer, Two-dimensional array, Ultrasonic imaging, wafer bonding

1. INTRODUCTION

Capacitive transduction is based on the electrostatic attractive (Coulomb) force on the plates of a charged capacitor. If one of the plates is movable with respect to the other, then the electrostatic force will displace the plate. The movable plate can be thought of as clamped with a spring that opposes the electrostatic attraction force. When an alternating voltage is applied, the movable plate will vibrate generating acoustical wave in the medium in contract with the movable plate. On the other hand, an incoming acoustic wave puts the movable plate into vibration, which modulates the capacitance between the plates. The incoming acoustic signal is detected by measuring the charge flow in and out of the capacitor under constant bias voltage. Condenser microphones are well known examples for capacitive transducers.

In the field of ultrasound, piezoelectricity has been the choice of transduction mechanism, although capacitive transduction is at least as old as piezoelectricity. The main reason for the use of piezoelectric materials is that the large coupling coefficient that heretofore was difficult to match in capacitive devices. The requirement for capacitors to compete with piezoelectric materials is a very high electric field in the gap of the capacitor as initially predicted by Langevin.[1] Given that breakdown in air occurs at an electric field strength of 10^6 V/m, very small gaps are required to enable high electric fields with no breakdown (Paschen law). Today, micro-electromechanical systems (MEMS) technologies enable the manufacture of capacitors with such small gaps, which initiated the interest in capacitive transducers once again. Early versions of micromachined electrostatic transducers were first reported in the late 1980s,[2] and the early 1990s.[3] The performance of these devices were not at a level to compete with the piezoelectric transducers, mainly because of poor control over the gap height and membrane size and shape. A later version that used more advanced micromachining techniques allowed the

Further author information: (Send correspondence to A. S. Ergun)
A. S. Ergun: E-mail: sanli@stanford.edu, Telephone: 1 650 723 8447

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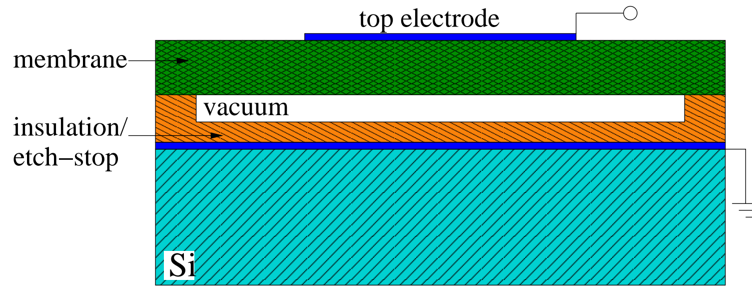


Figure 1. Schematic cross section of a basic capacitor cell.

realization of submicron gaps, and well-defined membrane sizes and shapes, which improved the performance of capacitive ultrasonic transducers[4] to a comparable level with piezoelectric transducers. These micromachined transducers were later abbreviated as cMUT standing for capacitive micromachined ultrasonic transducer.

There are two basic methods for fabricating cMUTs: the sacrificial release process, and the recently developed wafer bonding method. The sacrificial release process has been the traditional method for fabricating cMUTs. There are numerous versions of the sacrificial release process, all sharing the same basic principle. The cavity underneath the membrane is created by depositing or growing a sacrificial layer on the carrier substrate, which is selectively removed after the membrane deposition. Selective removal of the sacrificial layer is often referred as the release process, and can be done either by wet etch or dry etch. Wafer-bonding, which has been used for fabricating pressure sensors and accelerometers for some time, refers to the permanent bonding of two similar or different substrates. The fabrication of cMUTs using the wafer-bonding method, a recent development, offers many technological and performance benefits, and is expected to replace the sacrificial release process. This paper is focused on cMUT fabrication technologies, and is organized as follows: Section II briefly describes cMUT operation principles. Section III describes the fabrication techniques focusing on the wafer-bonding method. Device examples are shown in Section IV, which is followed by a discussion on electronic integration.

2. BASIC PRINCIPLES OF OPERATION

A basic capacitor cell made of a thin membrane is shown in Figure 1. The electrostatic force generated on the membrane of the capacitor cell is proportional to the square of the applied voltage, the area of the capacitor and the permittivity of the material between the plates, and inversely proportional to the square of the separation between the plates:

$$F_{elec} = \frac{\epsilon_0 A V^2}{2d^2} \tag{1}$$

where A is the area of the capacitor, V is the applied voltage, ϵ_0 is the permittivity of free space, and d is the separation between the plates. Because the electrostatic force is proportional to the square of the bias voltage, linear cMUT operation requires DC bias voltage together with the AC excitation. Then the electrostatic force can be written as

$$F_{elec} = \frac{\epsilon_0 A}{2d^2}(V_{DC}^2 + 2V_{DC}V_{AC} + V_{AC}^2) \tag{2}$$

The first term in the parenthesis represents the static force, the second term represents the excitation force proportional to the applied AC voltage, and the last term represents the harmonic contribution of the AC voltage. When the DC bias voltage is much larger than the AC excitation, the harmonic contribution can be ignored.

The membrane can be thought of as a mass clamped with a spring that opposes the electrostatic attraction force. The static force on the membrane is balanced by the mechanical restoring force. An important design parameter of a CMUT membrane is the collapse voltage, above which the attractive force can no longer be balanced by the restoring force of the membrane. This collapse voltage determines the operating point of the device. Therefore, it is crucial to calculate the collapse voltage accurately. Approximate and accurate collapse voltage calculations can be found in[5] and,[6] respectively.

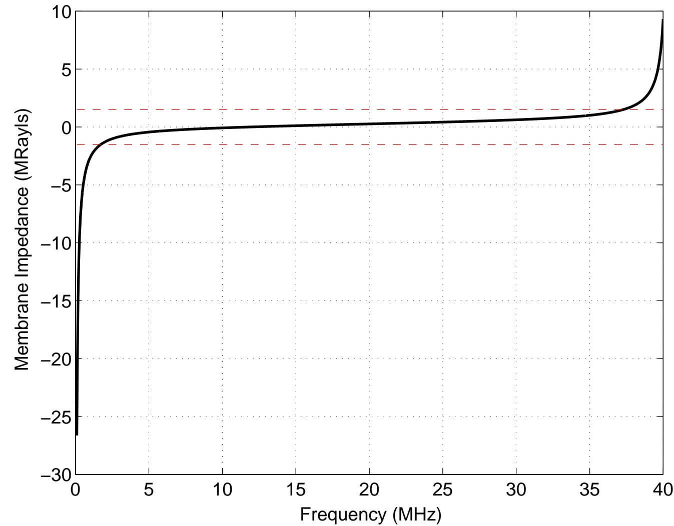


Figure 2. The mechanical impedance of a typical CMUT element designed for operation in the 5-35 MHz range in fluids

Traditionally, the DC bias voltage is set below the collapse voltage, which is referred to as conventional mode of operation. However, there are two other modes of operation: in-collapse and in-and-out of collapse mode of operations. In the in-collapse mode of operation, the center of the membrane is pinned to the substrate at all times, and a ring around the contact region vibrates. In the in-and-out of collapse mode of operation, the membrane goes into collapse and releases back in the transmit mode, to generate very high sound pressures. Detailed work on these modes of operation can be found in.[7]

The AC excitation force on the membrane results in the generation of acoustic waves in the medium in compliance with the mechanical impedance of the membrane and the medium. The mechanical membrane impedance predicts the linear membrane dynamics, and is derived by solving the equation of motion.[8, 9] The analysis of CMUT transducers is greatly simplified with the use of electrical equivalent circuit modelling introduced by Mason for electro-acoustic devices,[10] and improved to accurately include the effect of acoustical loading of the medium.[11]

For operation into fluids, the transducer's membrane impedance is below that of fluids over a large frequency range, resulting in very broad bandwidth operation. As an example, Figure 2 shows the mechanical membrane impedance of a cMUT made of 52 membranes, each with 36 μm diameter and 1 μm thick membranes. The red dashed lines (corresponding to ± 1.5 MRayls) show the frequency range where the mechanical membrane impedance is lower than the mechanical impedance of the medium. In reality, the impedance of the medium is not purely real as implied here. Because of the finite size of the transducer and the fill factor, the impedance of the medium has a complex part as well.[11] Although this changes the frequency response and lowers the bandwidth, Figure 2, as a first cut, shows the inherent advantage of cMUTs with respect to piezoelectric transducers in terms of frequency bandwidth. Another advantage of the low-impedance nature of cMUTs is that, the output pressure and receive sensitivity are matters of electrical impedance matching into the proper transmitter and receiver electronics.

3. FABRICATION TECHNOLOGIES

3.1. Sacrificial Release Process

The sacrificial release process starts with a conductive silicon wafer. The silicon surface is doped with the appropriate dopant to achieve high conduction at the surface, which is the back electrode in cMUT operation. A thin layer of low-stress silicon nitride is then deposited using the appropriate gas composition (dichlorosilane (DCS) to ammonia (NH_3) ratio of 14:1). The thickness of this layer – also called the etch-stop layer – must be sufficiently thick to protect the silicon wafer from the etchant during the long wet sacrificial layer etch. Because the capacitance of this layer comes in series with the active gap capacitance it should not be arbitrarily thick . In principle, only a few hundred Angstroms of silicon nitride

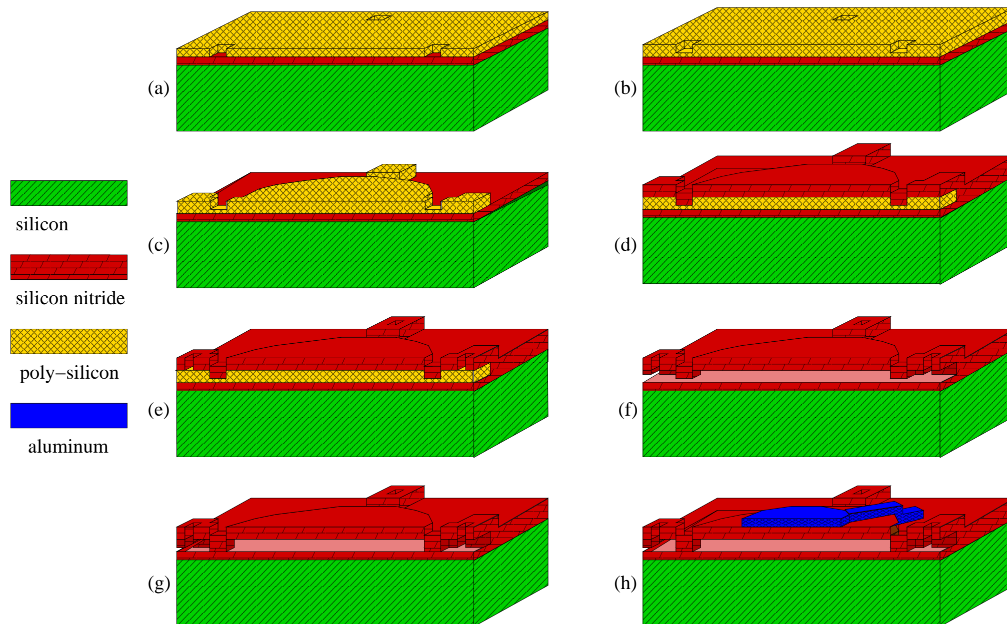


Figure 3. Process flow for the sacrificial release process.

is sufficient: but typically a > 1000 Å thick etch-stop layer is used to avoid problems with possible pin holes in very thin silicon nitride layers.

Sacrificial layer deposition and patterning is done in two steps so that the channels that KOH uses to remove the sacrificial layer are thinner than the cavity thickness (Fig. 3 (a), and (b)). The thickness of the second poly-silicon layer determines the thickness of the channels, and the total poly-silicon thickness from the first and second depositions determines the initial cavity height.

Another photolithography and dry etch step follows the second poly-silicon deposition, defining the cavity and the membrane shape, together with the etch channels (Fig. 3 (c)). In general, the membrane can be any shape, but circles and hexagons are easier to model and used most often, and rectangular membranes are harder to release. Especially high aspect ratio rectangular membranes are almost impossible to realize without sacrificing active area, which is one of the major deficiencies of the sacrificial release process.

The next step is the critical membrane deposition (Fig. 3 (d)). The membrane is made of low-stress silicon nitride deposited by LPCVD at 785 ^{o}C, just like the etch-stop layer. Because there will be another layer of silicon nitride added during the sealing step, the silicon nitride thickness at this time is not the final membrane thickness. This step is critical because the mechanical properties of the resulting silicon nitride film determines the mechanical properties of the membrane. Therefore, uniformity, repeatability, and good control over the thickness is of crucial importance, which is an issue with low-stress silicon nitride depositions.

Next, a lithography and dry etch steps open small holes through the silicon nitride layer (Fig. 3 (e)). The etch holes are located on the etch channels, so that when the wafer is immersed in KOH solution, KOH etches its way to the cavity and releases the membrane (Fig. 3 (f)). At room temperature, the etch may take several days depending on the membrane size. During the long KOH etch, the etch-stop layer protects the silicon wafer. Next step in the process seals the holes with another layer of LPCVD silicon nitride deposition (Fig. 3 (g)). Low pressure deposition condition of the LPCVD is considered vacuum for practical purposes, and ensures that the cavity is vacuum sealed. After the sealing step, a dry etch step finalizes the membrane thickness. The final membrane thickness is determined by the initial silicon nitride

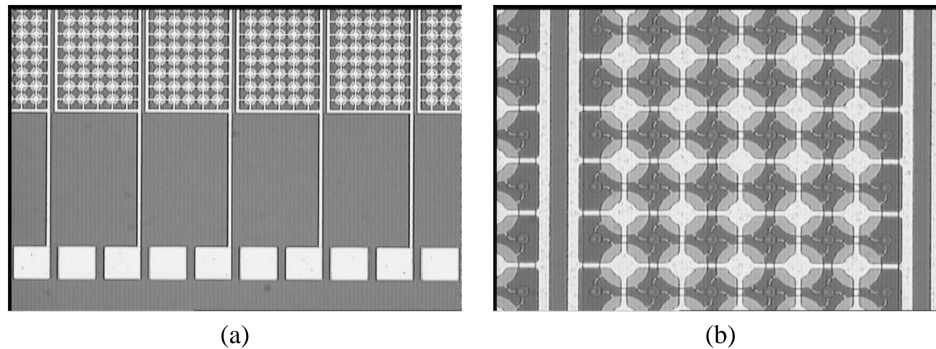


Figure 4. Optical pictures of a one-dimensional array fabricated using the sacrificial release process: (a) showing bond pads and elements, and (b) a closer look at an array element with 5 circular membranes across the width.

deposition, plus the final silicon nitride deposition, plus the amount of silicon nitride that gets deposited inside the cavity during sealing, and minus the amount of etch-back. On the other hand, the gap height is determined the by the initial sacrificial layer thickness, minus the amount of silicon nitride that gets deposited inside the cavity. These, together with the uncertainty in the mechanical properties of the silicon nitride film, make up the major deficiencies of the sacrificial release process. Even in different variations of the sacrificial release process where different membrane and sacrificial layer combinations are used, the problem remains the same: low thickness and quality control.

The rest of the process involves getting the electrical connections from the bond pads to the top and bottom electrodes. A lithography and etch step opens a connection to the ground plane through the silicon nitride layers. Subsequently, aluminum is sputtered over the whole wafer, and patterned with lithography and wet etch (Fig. 3 (h)). After putting the metal, wafers are annealed in forming gas to obtain ohmic contact to ground.

3.2. Wafer-bonding Method

Wafer-bonding, considered as a bulk process, is widely used in micromachining, and older than surface micromachining techniques. There are three basic wafer bonding techniques: anodic bonding, fusion bonding and adhesive bonding. While the physics behind each of these is different, the purpose and the outcome is the same: the permanent bonding of two similar or different substrates.

Silicon fusion bonding, the method used in cMUT fabrication, is a direct bond between two silicon surfaces. It takes place at high temperatures, forming strong covalent bonds between the silicon wafers. The bond is hermetic, and exceptionally stable both mechanically and electrically.[12] Measurements and observations indicate that the yield strength of the bond is close to the yield strength of single-crystal silicon.[13] This level of stability is crucial for extreme applications such as high-pressure and high-temperature sensing environments. The bond is equally stable even when one of the wafers is thermally oxidized.

Silicon fusion bonding has shown to have many important advantages over surface micromachining techniques in making pressure sensors.[12] Along with stability, wafer-bonding allows easier fabrication of complex structures (e.g., membranes) out of single crystal silicon. Single-crystal silicon as a mechanical material has been extensively studied, and is very well characterized.[14] Its mechanical and electrical properties are consistent on a wafer, from wafer to wafer, and from time to time; important characteristics which surface micromachining does not exhibit at that level. Being very similar in nature, cMUTs made with the silicon fusion bonding share these excellent properties.

The fabrication of cMUTs using the wafer-bonding technique begins with two wafers: a prime quality silicon wafer and a silicon-on-insulator (SOI) wafer. The prime quality silicon wafer is thermally oxidized to a pre-determined thickness, followed by a photolithography step to define the cavity shape. The thermally-grown silicon dioxide layer is etched in hydrofluoric acid solution (can be dry etched too) through the photoresist pattern all the way to the silicon as shown in Fig. 5 (a). After the etch, another layer of silicon dioxide is thermally grown (Fig. 5 (b)). Because the membrane is silicon, which is not an insulator, the second oxidation isolates the conductive silicon substrate from the top electrode to avoid shorting.

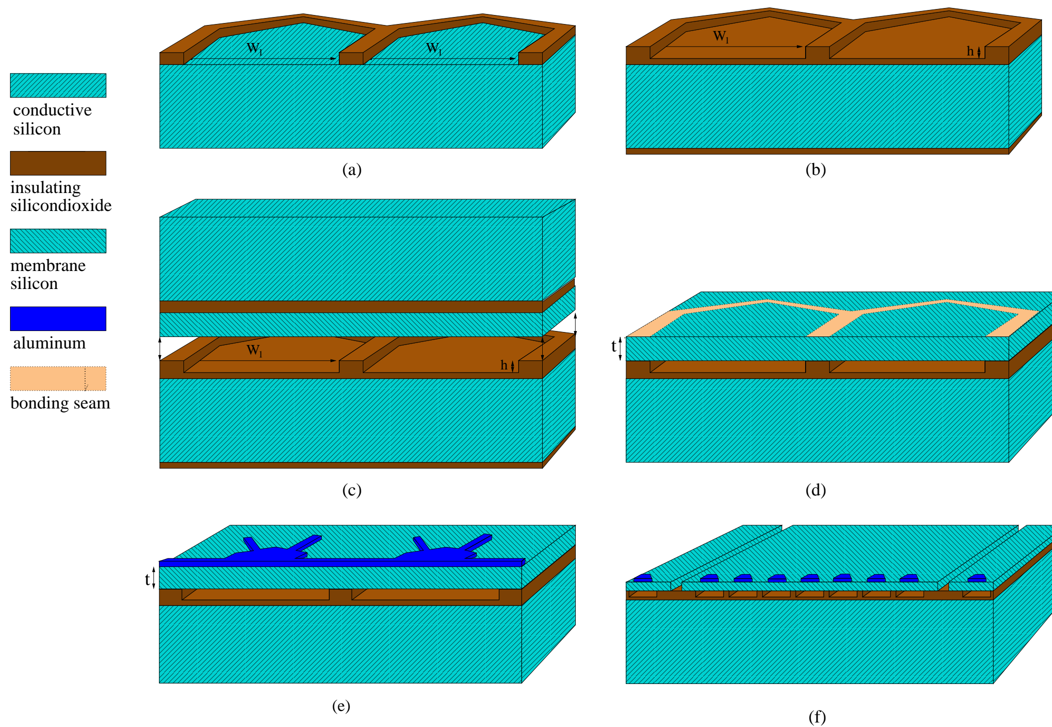


Figure 5. Process flow for the wafer bonding method.

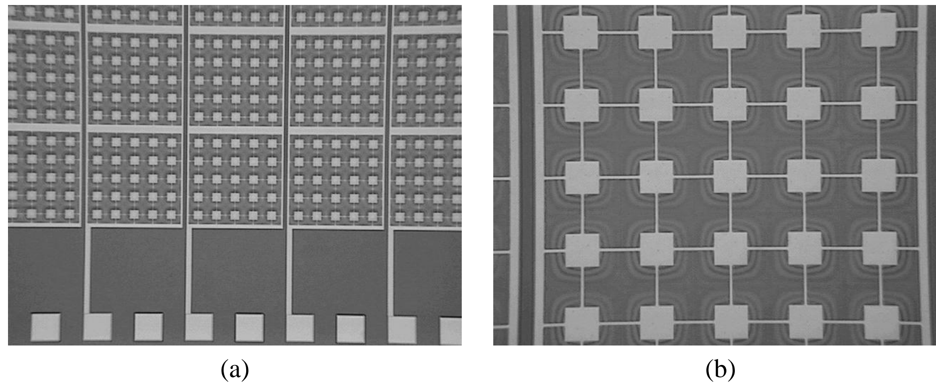
Following the second oxidation, the SOI wafer and the prime wafer (after being RCA-cleaned and surface-activated) are brought together in vacuum as shown in Fig. 5 (c). As soon as the two wafers come in close contact, short-range van der Waals forces attract the two wafers to each other, and weak hydrogen bonds are formed. The wafers are immediately annealed/oxidized at 1100 ^{o}C to form strong covalent bonds.

After bonding and annealing, the handle part of the SOI wafer (including the buried oxide layer) is removed to release the membranes (Fig. 5 (d), either by wet etching or dry etching. Wet etching of silicon, a well-known process, can be done with a solution of either KOH or tetra-methyl-ammonium-hydroxide (TMAH). Because both KOH and TMAH have very slow etch rates for silicon dioxide, when the silicon etch is complete, the wet etch process will slow down considerably at the buried oxide (BOX) layer. The buried oxide layer can then be removed with hydrofluoric acid, which stops at the silicon membrane.

The remaining steps of the wafer-bonded cMUT process are very similar to methods for surface micromachined cMUT process,with the exception of element definition. In order to access to the bottom silicon and make the ground connection, openings through the silicon and silicon dioxide layers are defined with photolithography and dry-etch steps. The top electrode is sputtered and then patterned by another photolithography and wet etch step (Fig. 5 (e)). Finally, the elements are defined by etching isolating trenches as shown in Fig. 5 (f). Because the active silicon layer is not a good insulator, it must be etched all the way to the oxide layer to isolate the elements from each other electrically. The trenches are defined with photolithography, and dry etched into the silicon.

3.3. Comparison of sacrificial release and wafer-bonding methods

The wafer-bonded cMUT process (as evident from the above description) substantially reduces the complexity of cMUT fabrication. The number of essential masks reduces from 6 to 4, and the processing time is reduced proportionally compared to sacrificial release processes. The wafer-bonding technique also adds many design flexibilities that improve device efficiency. Because the cavity and the membrane are defined on separate wafers, it is possible to optimize them both at the same time. There are no wet release processes to limit the size of the membranes that can be fabricated, virtually eliminating the limit on the low frequency end. The cavity height and the insulation layer thickness are determined by



(a) (b)

Figure 6. Optical pictures of a one-dimensional array fabricated using the wafer bonding method: (a) showing bond pads and elements, and (b) a closer look at an array element with 5 square membranes across the width.

thermal oxidation steps, which is a well-controlled process used extensively in VLSI processes. The thickness of the thermally grown silicon dioxide is precise as is the on-wafer and wafer-to-wafer thickness uniformity. This accuracy allows excellent control over the cavity height, and the insulation layer thickness. Typical on-wafer and wafer-to-wafer thickness uniformities are better than 1%, where uniformity is defined as the ratio of the standard deviation to the mean of the thickness measurements.[15] Similarly, because the membranes are made of the active silicon layer of the SOI wafer, the membrane thickness and thickness uniformity are determined by the SOI wafer. For SMART-CUT thin SOI wafers ($< 1.5\ \mu$m active silicon thickness), the thickness variation is less than 10 nm for 100-mm wafers.[16] In addition, the membrane is single crystal silicon, which has well-known mechanical and electrical properties with no residual stress. Consequently, the control over the membrane thickness and its mechanical properties, as well as the on-wafer and wafer-to-wafer thickness uniformity, are excellent in comparison to any of the deposited membranes.

The direct bonding of the prime wafer (on which the cavity is defined) and the SOI wafer is the most critical step. Both wafers must be ultra-clean, free from particles, and ultra-smooth. The number of bonds - and therefore the strength of the bond - depends on the smoothness (inverse of surface roughness) of the wafers. Although this seems like a stringent requirement, it is readily achieved by prime quality silicon and SOI wafers. Successful SOI manufacturing companies and pressure sensor companies,[12, 13, 16] proves the reliability of this process.

In all of cMUT fabrication processes, the membrane is either an insulating material, such as silicon nitride, or a conductive material, such as doped poly-silicon. In the wafer-bonding method, the membrane is composed of single crystal silicon, which is really a semiconductor. Unless heavily doped, it is neither an insulator nor a conductor. Therefore, its electronic properties has to be accounted while making designs,[15] which complicates the analysis process compared to other cMUT structure.

In wafer-bonded cMUTs, the membrane and the substrate are separated with thermally grown silicon dioxide which isolates the top electrode from the bottom electrode electrically. Both the thickness of the post that supports the membranes and the thickness of the insulation layer in the cavity must accommodate the highest voltage of operation. Although silicon nitride has slightly lower breakdown field, wafer-bonded cMUTs are more vulnerable to dielectric breakdown. Because the membrane is not insulating, the electric field share of the insulation layer is larger, which promotes failures and charging in the silicon dioxide layer. The insulation layer thickness has to be designed accordingly thick to lower the field in the insulation layer.

In contrast to sacrificial release processes, the wafer-bonding method does not have any wet release process. The absence of stress in the silicon membrane together with the absence of a wet release process, gives the wafer-bonding method the unique capability of fabricating large membranes with a sealed cavity. The frequency range of cMUTs is thereby extended to 10 kHz on the low frequency side.[17] Wafer-bonded cMUTs have a distinctive advantage on the higher side of the frequency range as well.[18] Because they do not require etch holes and channels, the active area can be utilized very efficiently by leaving only two microns (or less) of post region between membranes. The active area utilization, also referred to as the fill factor, has significant implications on cMUT performance: it directly scales the output pressure

and receive sensitivity, affects the acoustical load seen by the transducer (low fill factor implies narrower bandwidth), and determines the acoustical reflection coefficient of the cMUT on receive. The parasitic capacitance of a cMUT refers to the capacitance that does not contribute to the acoustical output. Although parasitic capacitance is usually not a problem on transmit, it adversely affects the signal-to-noise ratio on receive. By definition, increasing the fill factor, reduces the parasitic capacitance, while increasing the active capacitance. In summary, the fill factor has a three-fold effect on the overall device efficiency: increased output pressure and receive sensitivity because of area gain, and increased singal to noise ratio (SNR) because of reduced parasitic capacitance.

Wafer-bonded cMUTs have other features that contribute to the fill factor, including the ability to fabricate high aspect ratio rectangular membranes. Using rectangular membranes increases both the fill factor, and the average displacement over the membrane compared to circular or hexagonal membranes. Recent work[19] revealed that rectangular membranes are better than square membranes in both transmit efficiency and receive sensitivity, by 46% and 43%, respectively.

4. DEVICE EXAMPLES

Figure 7 shows the frequency response of the separate device examples. The first example ((a) and (b))shows the response of four elements transmitting and receiving together in an 86 element one-dimensional array. Array elements are 585 μm wide, and 4.8 mm long, and are made of 200 96 μm wide and 1 μm thick square membranes. The experiment is done with 90 V bias and 10 V amplitude single cycle tone burst. An aluminum block, 11.5 mm away, is used as a reflector. The received pulse-echo frequency response shows the exceptional wide bandwidth that can be achieved with cMUTs. The second example is a high frequency design made of 19 μm diameter (inscribed) and 1 μm thick hexagonal membranes. In this case, the frequency response (d) is centered at 7 MHz with 100% fractional bandwidth. The small dip that is seen in the frequency response around 8 MHz is because of the substrate ringing mode, which is normally eliminated by using a backing. In this example, the response is measured using a hydrophone which is located 1 cm away. The response is not corrected for the hydrophone response and attenuation. Therefore, the roll-off at the high end does not reflect the actual high frequency response of the device. However, this example, like the low frequency one, shows the exceptional wide bandwidth of cMUTs. Also, note that these results are obtained without any matching layers, which is required for piezoelectric transducers to achieve wide bandwidth.

The improved depth resolution is an immediate consequence of wide frequency bandwidth.[20–23] It also enables imaging modalities which are difficult to achieve with narrow band systems, such as harmonic imaging.

5. ELECTRONIC INTEGRATION

An important handicap of cMUTs is the lower device capacitance as compared to similar size piezoelectric transducers, and higher parasitic capacitance. Although, it is not a big issue in transmit mode, cMUTs suffer from the parasitic capacitance in receive mode, which lowers the signal to noise ratio. Also, the existing imaging instruments are all designed and optimized for piezoelectric arrays, and therefore are not suitable for cMUTs. In these respects, to get the best out of the potential performance of cMUTs, a dedicated and integrated electronic design is required, especially for 2D and high-frequency arrays. There are basically two approaches to electronic integration for cMUT arrays. The first one is the monolithic integration in which cMUT arrays are post-processed on to the electronics chip.[24–26] Because cMUTs are build on an existing electronic chip, the highest temperature of the cMUT process is limited to 400 ^{o}C. The other integration method is the hybrid integration of the electronics with the cMUT array using flip-chip bonding. In this approach, the electronics and cMUTs (with electrical through-wafer interconnects[27]) are manufactured separately. Both approaches have advantages and disadvantages, but certainly are promising for the future of volumetric ultrasound imaging using 2D arrays. Because the electronics and the transducers are manufactured separately, the hybrid integration is a relatively simpler, faster (quick turn-around), and higher yield method when compared to post-processing, and allows more flexibility in the design and fabrication of the cMUT arrays. More detail and data on electronic integration can be found in.[28–30]

6. CONCLUSION

Capacitive micromachined ultrasonic transducers have been an attractive alternative to piezoelectric transducers for some time, showing performance benefits both in air and immersion applications,[22] and higher coupling efficiency than piezoelectric transducers.[31] A major handicap has been low output pressure capability of cMUTs in their normal mode of

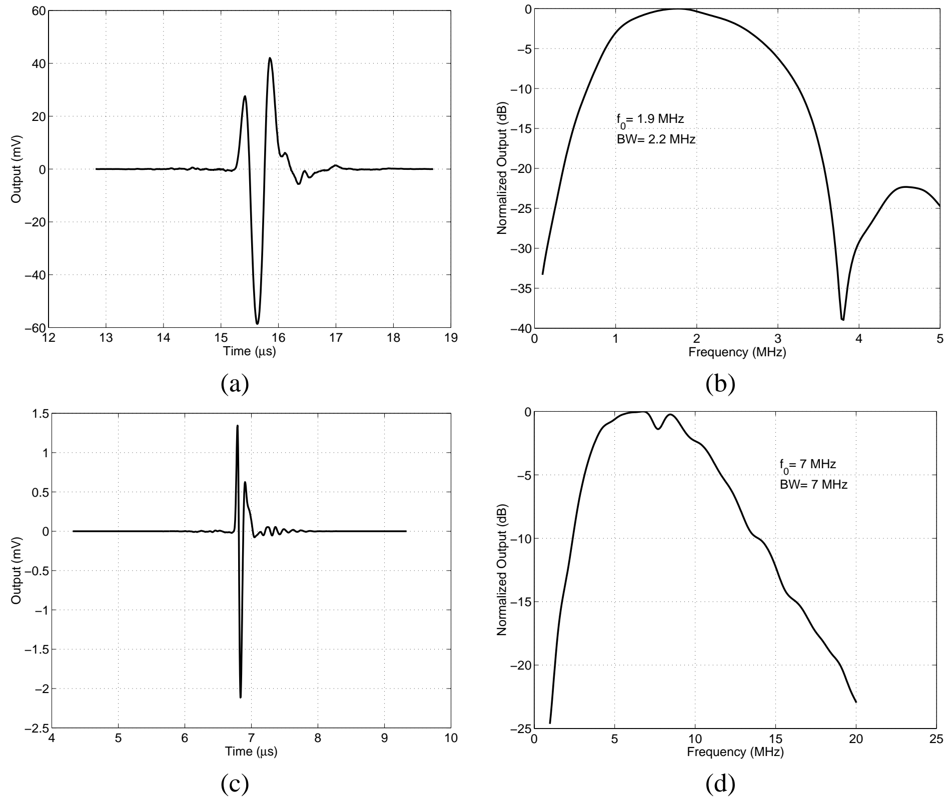


Figure 7. Frequency response of one-dimensional cMUT array elements fabricated using the wafer-bonding method: (a) and (b) respectively show the pulse-echo time and frequency response of the low frequency device. (c) and (d) respectively show the pitch-catch time and frequency response of the high frequency device, as measured by a calibrated hydrophone 1 cm away.

operation in immersion applications. Recent attempts show that the output pressure capability can be improved by operating the cMUT in different modes.[32] CMUTs also offer significant technological benefits: by using micromachining techniques, derived from integrated circuit technologies, cMUTs benefit from batch fabrication capability and scalability, the two factors that had driven down the cost of IC fabrication.

The most important feature of CMUTs is that it is not just a replacement technology. It also enables many different imaging applications and modalities. Volumetric imaging using 2D arrays, and miniature arrays integrated with the electronics are just two examples. Although, the cMUT technology has some problems with output pressure, parasitic capacitance and etc., it should be considered as a mature technology. The impact of the cMUT technology on the medical ultrasound imaging is expected to be biggest when the electronic integration methods are matured enough as well.

In this paper, we also reviewed and qualitatively compared the two cMUT fabrication techniques: the sacrificial release process, and the wafer-bonding technique. Both processes have similar outcomes, and delivers wide-band and easily manufacturable one-dimensional and two-dimensional cMUT arrays. However, it is seen that the wafer-bonding method offers easier, faster, more repeatable and more reliable manufacture for cMUTs.

REFERENCES

1. F. V. Hunt, *Electroacoustics; the analysis of transduction, and its historical background*, Cambridge, Harvard University Press, 2nd ed., 1982.
2. K. Suzuki, K. Higuchi, and H. Tanigawa, "A silicon electrostatic ultrasonic transducer," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control* **36**(6), pp. 620–627, 1989.

3. M. Rafiq and C. Wykes, “The performance of capacitive ultrasonic transducers using v-grooved backplates,” *Meas. Sci. Technol.* **2**, pp. 168–174, 1991.
4. M. I. Haller and B. T. Khuri-Yakub, “A surface micromachined electrostatic ultrasonic air transducer,” in *Ultrasonics Symposium Proceedings*, pp. 1241–1244, IEEE, 1994.
5. I. Ladabaum, X. C. Jin, H. T. Soh, A. Atalar, and B. T. Khuri-Yakub, “Surface micromachined capacitive ultrasonic transducers,” *IEEE Trans. on Ultrasonics, Ferrolectrics and Frequency Control* **45**, pp. 678–690, 1998.
6. A. Nikoozadeh, B. Bayram, G. G. Yaralioglu, and B. T. Khuri-Yakub, “Analytical calculation of collapse voltage of cmut membrane,” in *presented at the IEEE Intl. Ultrason. Symp., Montreal, Canada*, IEEE, 2004.
7. B. Bayram, Ö. Oralkan, A. S. Ergun, E. Hæggström, G. G. Yaralioglu, and B. T. Khuri-Yakub
8. O. Ahrens, A. Buhrdorf, D. Hohlfeld, L. Tebje, and J. Binder, “Fabrication of gap-optimized cmut,” *IEEE Trans. on Ultrasonics, Ferrolectrics and Frequency Control* **49**, pp. 1321–1329, Sep. 2002.
9. A. S. Ergun, G. G. Yaralioglu, and B. T. Khuri-Yakub, “Capacitive micromachined ultrasonic transducers : Theory and technology,” *Journal of Aerospace Engineering* **16**, pp. 76–84, 2003.
10. W. Mason, *Electromechanical Transducers and Wave Filters*, Van Nostrand, New York, 1948.
11. A. Lohfink, P. C. Eccardt, W. Benecke, and H. Meixner, “Derivation of a 1d cmut model from fem results for linear and nonlinear equivalent circuit simulation,” in *Ultrasonic Symposium Proceedings*, pp. 465–468, IEEE, 2003.
12. K. Petersen, J. Brown, T. Vermuelen, P. Barth, J. Mallon, Jr., and J. Bryzek, “Ultra-stable, high-temperature pressure sensors using silicon fusion bonding,” *Sensors and Actuators A* **A21-A23**, pp. 96–101, 1990.
13. P. W. Barth, “Silicon fusion bonding for fabrication of sensors, actuators and microstructures,” *Sensors and Actuators A* **A21-A23**, pp. 919–926, 1990.
14. K. E. Petersen, “Silicon as a mechanical material,” *Proceedings of the IEEE* **70**, pp. 58–95, May 1982.
15. A. S. Ergun, G. G. Yaralioglu, Ö. Oralkan, and B. T. Khuri-Yakub, *MEMS/NEMS Techniques and Applications*, ch. Techniques and Applications of Capacitive Micromachined Ultrasonic Transducers. Kluwer, 2005.
16. S. S. Iyer and A. J. Auberton Hervé, eds., *Silicon Wafer Bonding Technology for VLSI and MEMS applications*, INSPEC¡ The Institution of Electrical Engineers, London, 2002.
17. A. S. Ergun, Y. Huang, C.-H. Cheng, Ö. Oralkan, J. Johnson, H. Jagannathan, U. Demirci, G. G. Yaralıoğlu, M. Karaman, and B. T. Khuri-Yakub, “Broadband capacitive micromachined ultrasonic transducers ranging from 10 khz to 60 mhz for imaging applications and more,” in *Ultrasonic Symposium Proceedings*, pp. 1039–1043, IEEE, 2002.
18. D. T. Yeh, O. Oralkan, A. S. Ergun, X. Zhuang, I. O. Wygant, and B. T. Khuri-Yakub, “High frequnency cmut arrays for high-resolution medical imaging,” in *presented at the SPIE Medical Imaging, San Diego, CA*, SPIE, 2005.
19. Y. Huang, E. Hægström, X. Zhuang, A. S. Ergun, and B. T. Khuri-Yakub, “Optimized membrane configuration improves cmut performance,” in *Ultrasonic Symposium Proceedings*, IEEE, 2004.
20. D. M. Mills and S. W. Smith, “Real-time in-vivo imaging with capacitive micromachined ultrasound transducer (cmut) linear arrays,” in *Ultrasonic Symposium Proceedings*, pp. 568–571, IEEE, 2003.
21. D. M. Mills, “Medical imaging with capacitive micromachined ultrasound transducer (cmut) arrays,” in *Ultrasonic Symposium Proceedings*, IEEE, 2004.
22. Ö. Oralkan, A. S. Ergun, J. A. Johnson, M. Karaman, U. Demirci, K. Kaviani, T. H. Lee, and B. T. Khuri-Yakub, “Capacitive micromachined ultrasonic immersion transducers: Next-generation arrays for acoustic imaging?,” *IEEE Trans. on Ultrasonics, Ferrolectrics and Frequency Control* **49**, pp. 1596–1610, November 2002.
23. Ö. Oralkan, A. S. Ergun, C.-H. Cheng, J. A. Johnson, M. Karaman, T. H. Lee, and B. T. Khuri-Yakub, “Volumetric ultrasound imaging using 2-d cmut arrays,” *IEEE Trans. on Ultrasonics, Ferrolectrics and Frequency Control* **50**, pp. 1581–1594, November 2003.
24. R. A. Noble, R. R. Davies, M. M. Day, L. Koker, D. O. King, K. M. Brunson, A.R.D. Jones, J.S. McIntosh, D.A. Hutchins, T. J. Robertson, and P. Saul, “Cost-effective and manufacturable route to the fabrication of high-density 2d micromachined ultrasonic transducer arrays and (cmos) signal conditioning electronics on the same silicon substrate,” in *Ultrasonic Symposium Proceedings*, pp. 941–944, IEEE, 2001.
25. R. A. Noble, A. D. R. Jones, T. J. Robertson, D. A. Hutchins, and D. R. Billson, “Novel, wide bandwidth, micromachined ultrasonic transducers,” *IEEE Trans. on Ultrasonics, Ferrolectrics and Frequency Control* **48**, pp. 1495–1507, Nov. 2001.

26. R. A. Noble, R. R. Davies, D. O. King, M. M. Day, A.R.D. Jones, J.S. McIntosh, D.A. Hutchins, and P. Saul, "Low-temperature micromachined cmuts with fully-integrated analogue front-end electronics," in *Ultrasonic Symposium Proceedings*, pp. 1045–1050, IEEE, 2002.
27. X. Zhuang, I. O. Wygant, O. Oralkan, A. S. Ergun, C.-H. Cheng, Y. Huang, and B. T. Khuri-Yakub, "Two-dimensional capacitive micromachined ultrasonic transducer (cmut) arrays for miniature integrated ultrasonic imaging systems," in *presented at the SPIE Medical Imaging, San Diego, CA*, SPIE, 2005.
28. I. O. Wygant, X. Zhuang, D. T. Yeh, A. Nikoozadeh, Ö. Oralkan, A. S. Ergun, M. Karaman, and B. T. Khuri-Yakub, "Integrated ultrasonic imaging systems based on cmut arrays: recent progress," in *presented at the IEEE Intl. Ultrason. Symp., Montreal, Canada*, IEEE, 2004.
29. Ö. Oralkan, S. T. Hansen, B. Bayram, G. G. Yaralioglu, A. S. Ergun, and B. T. Khuri-Yakub, "High-frequency cmut arrays for high-resolution medical imaging," in *presented at the IEEE Intl. Ultrason. Symp., Montreal, Canada*, IEEE, 2004.
30. Ö. Oralkan, S. T. Hansen, B. Bayram, G. G. Yaralioglu, A. S. Ergun, and B. T. Khuri-Yakub, "Cmut ring arrays for forward-looking intravascular imaging," in *presented at the IEEE Intl. Ultrason. Symp., Montreal, Canada*, IEEE, 2004.
31. G. G. Yaralıoğlu, A. S. Ergun, B. Bayram, E. Hægström, and B. T. Khuri-Yakub, "Calculation and measurement of electromechanical coupling coefficient of capacitive micromachined ultrasonic transducers," *IEEE Trans. on Ultrasonics, Ferrolectrics and Frequency Control* **50**, pp. 449–456, April 2003.
32. B. Bayram, E. Hægström, G. G. Yaralıoğlu, and B. T. Khuri-Yakub, "A new regime for operating capacitive micromachined ultrasonic transducers," *IEEE Trans. on Ultrasonics, Ferrolectrics and Frequency Control* **50**, pp. 1184–1190, September 2003.