RECENT PROGRESS IN CAPACITIVE MICROMACHINED ULTRASONIC IMMERSION TRANSDUCER ARRAY

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Abstract

Capacitive micromachined ultrasonic immersion transducers are attractive alternatives to piezoelectric transducers due to their ease of array fabrication. Possibility of localized electronics integration is another advantage for transducer array manufacturing to eliminate massive cable connections between transducers and their peripheral electronics. Among various approaches, transducer electronics co-fabrication and transducer electronics flip chip bonding are two of the most attractive ways to realize the integration. Various process alternatives for both transducer fabrication and electronics integration are reviewed in this paper. Flip chip bonding is the chosen approach to optimize both transducer and electronics design without process compatibility constraints. Latest experimental results in both 1-D and 2-D capacitive micromachined ultrasonic immersion transducer arrays are reported.

I. Introduction

Capacitive micromachined ultrasonic transducers (cMUTs) are attractive alternatives to piezoelectric transducers [1], especially for array operation due to its ease of electronics integration. In the past few years, research work has been emphasized on the fabrication process [2], [3] and theoretical modeling of single cMUT devices [4], [5]. Many applications, especially immersion array imaging, demand improvements of cMUTs both in terms of individual device performance and array behavior. In addition, massive interconnects between array devices and signal conditioning and processing electronics is of concern.

In this paper, various process alternatives for both transducer fabrication and electronics integration are analyzed. Flip chip bonding is the chosen approach to optimize both transducer and electronics design without compromise of performance. Encouraging results on both 1-D and 2-D immersion transducer array are presented.

II. Transducer Fabrication

An immersion cMUT consists of metalized membrane (top electrode) suspended above heavily doped silicon bulk (bottom electrode) as shown in Fig. 1. where typically the upper electrode is loaded with fluid ambient. A single transducer consists of many such elements in parallel connection. When a DC voltage is applied between the two electrodes, Coulomb forces attract them together. At the same time, the residual stress within the membrane resists the attraction. If the membrane is driven by an AC voltage, significant ultrasound generation results, which is the case for the transmitter device. Conversely, significant detection currents are generated when the membrane is biased appropriately and subjected to ultrasonic waves, which is the case for the receiver device.

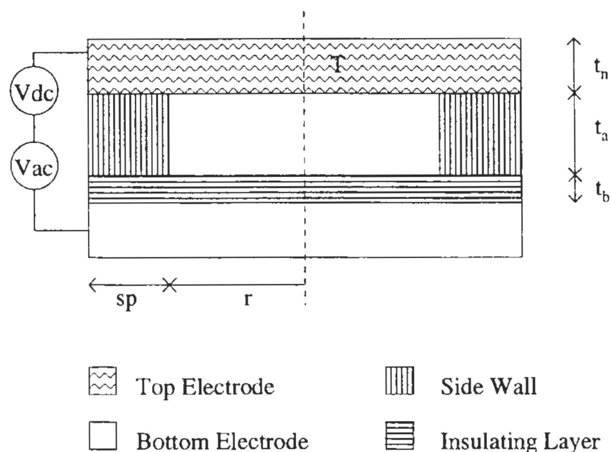

Fig. 1. An immersion cMUT cell.

There are mainly three kinds of membrane formation schemes reported. The properties in surface profile, stress control and sacrificial etching selectivity are summarized in Table I. Option A used silicon nitride as membrane material and silicon dioxide as sacrificial layer with timed sacrificial etching [6], [7]. Option B used silicon nitride as membrane material and polysilicon as sacrificial layer with lithographically defined active region [2], [8]. Option C used polysilicon as membrane material and low temperature oxide as sacrificial layer with on-chip CMOS circuits [9]. Process C is the only option for transducer electronics co-fabrication on the same wafer due to its low thermal budget and readily available material selection in standard CMOS process. Process A and B are also possible for the same integration only if the nitride membrane is taken care of with low temperature PECVD deposition.

Table I. Comparison of membrane formation process.

Option	Surface	Stress	Etch Selectivity
A	Planner	Good control	Poor
B	Non-Planner	Good control	Excellent
C	Planner	Poor control	Acceptable

There are three kinds of cavity sealing schemes reported as summarized in Table II. Option A used sub-micron lithography to define the vias and sealed with direct redeposition [10], [9]. Option B used low cost lithography to define the vias and the vias were subsequently sealed with species sticking coefficient control [2], [8]. Option C used low cost lithography to define the vias and subsequently

sealed with buffered channel region [11], [12]. For transducer electronics co-fabrication, sub-micron lithography is automatically available for stanford CMOS process. So the selection is really dependent on the budget and process capability.

Table II. Comparison of cavity sealing process.

Option	Sealing Profile	Cost	Fill Factor
A	Excellent control	High	High
B	Poor control	Low	High
C	Excellent control	Low	Low

III. Transducer Interconnects

There are two distinct ways reported to create massive interconnects between transducer arrays and signal conditioning and processing electronics without going through bulky cables as summarized in Table III. Transducer electronics co-fabrication is a natural choice for a fully CMOS compatible transducer fabrication schemes [9]. But when the transducer takes majority of the die area, the total cost will be increased dramatically.

Flip chip solder bonding of transducer die and electronics die is an alternative [12]. For transducers with much larger area than electronics, flip chip bonding is, in fact, a better choice since transducer fabrication process is normally much simpler and cheaper. In addition, separate processes for transducer and electronics fabrication provide non-compromised parameter space for separate performance optimization for both transducer and electronics design and fabrication.

Table III. Comparison of Interconnection Scheme.

Option	Advantage	Disadvantage	Best Fit
A	One process	Compromise	Small area
B	Optimization	Two processes	Large area

Flip chip bonding is the chosen approach in this paper. A complete process flow for double sided transducer fabrication process is shown in Fig. 2.

We start with a 500 um thick double-sided polished p-type < 100 > silicon wafer which is thermally oxidized and coated with 1 um of polysilicon (Fig. 2-1). The polysilicon is removed from the back side of the wafer by a plasma dry back-etch. Vias 100 um in diameter are etched from the back side of the wafer using a silicon deep trench etcher (STS Limited, UK), stopping on the thermal oxide. This oxide then is removed by an anisotropic dry etch (Fig. 2-2). A 2 um polysilicon layer is deposited, coating the via walls and wafer surfaces. The polysilicon is then doped using gas phase phosphorus drive-in at 1000°C, yielding a conductive path through the wafer.

The cMUTs are built on the front side polysilicon, which is patterned into individual islands (Fig. 2-3). First a thin layer of LPCVD nitride is deposited at 800°C as an insulator and an etch stop for the sacrificial etch to be performed later. An amorphous silicon sacrificial layer is subsequently deposited and dry-etch patterned into octagonally shaped islands to define the active transducer cavity

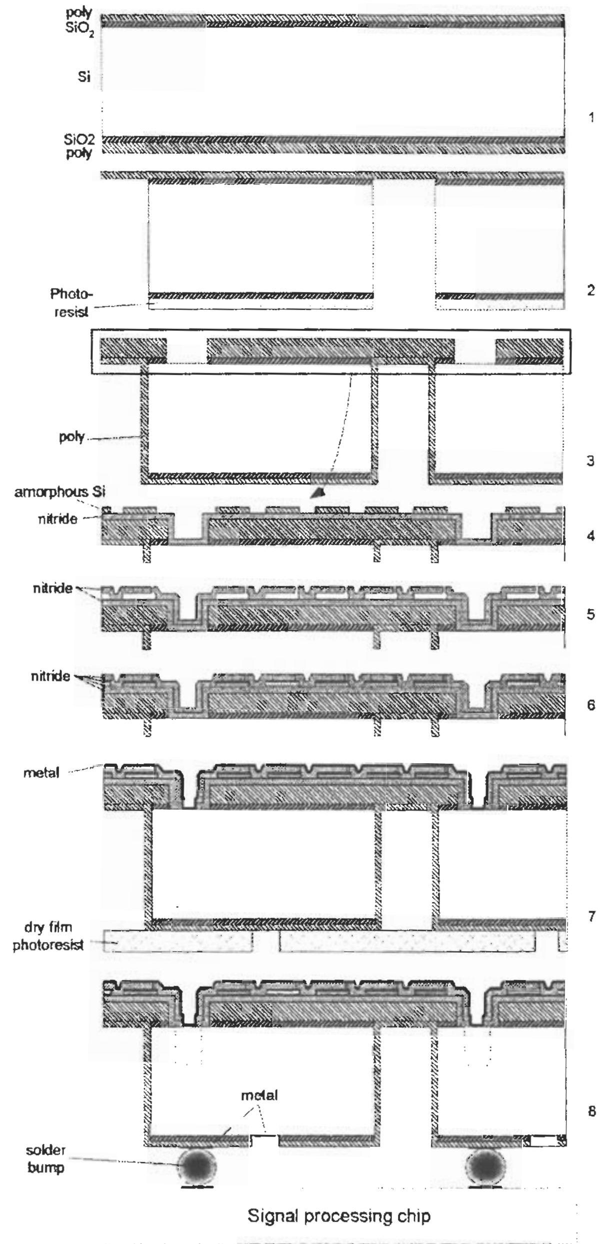

Fig. 2. Process flow for double sided fabrication.

regions (Fig. 2-4). The nitride membrane is then deposited by LPCVD, after which vias are dry-etched to allow an access path for the sacrificial etchant. After the cavities have been formed by KOH etching (Fig. 2-5), they are vacuum sealed by LPCVD nitride, which is subsequently selectively back-etched to achieve the desired membrane thickness (Fig. 2-6). Aluminum is then sputtered and wet-etch patterned to act as the top (ground) electrode.

The back-end processing consists of two special lithography steps on the back side of the wafer, in order to yield the individual contact pads. The presence of the deep vias makes it impossible to deposit photoresist homogeneously on the back side through spin-coating. We use a 30 um

thick dry film photoresist (Riston by Dupont) that is laminated over the back side, and that covers ('tents') the via holes, planarizing the surface and allowing a standard photolithography on the back side of the wafer (Fig. 2-7). The backside pads are then defined by polysilicon and oxide dry etch using Riston as a mask. In a final lithographic step, the metal solder bump pads and metal ground strip lines are defined by a Riston lift-off. The chip can now be flip-chipped to a signal processing chip (Fig. 2-8).

IV. Experimental Results

Both 64 element 1-D array and 16 x 16 element 2-D array cMUTs are fabricated in this paper. Fig. 3 shows the top view of a few 64 element 1-D arrays, and each of the element has 8 x 160 cells of 30um in diameter. Fig. 4 shows the front side view of 16 x 16 element 2-D array, and each of the element has 72 cells of 36um in diameter. Fig. 5 shows the back side view of the same 2D array indicating through-wafer interconnects for flip chip solder bonding.

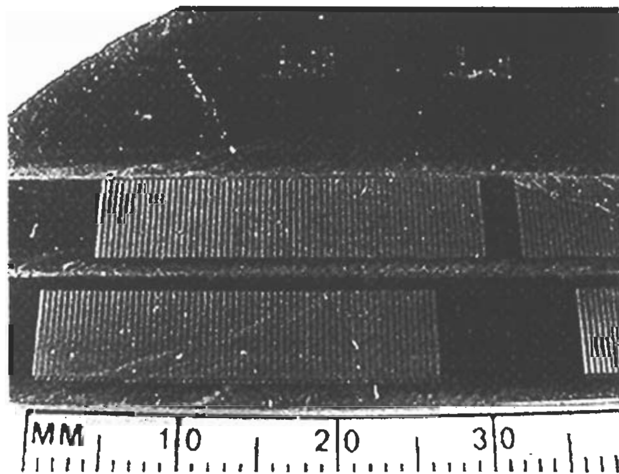

Fig. 3. Top view of 1-D immersion cMUT array.

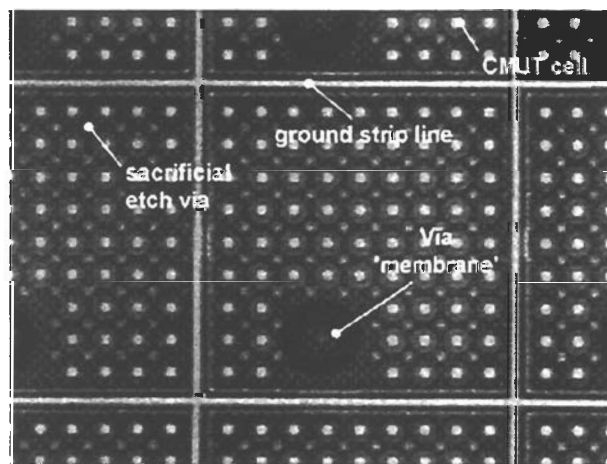

Fig. 4. Front side view of 2-D Immersion cMUT array.

Fig. 6 shows the Fourier transform of radiation pattern of the 1-D array element biased at 40 V and its neighbors biased at 80 V. Better than 45 degree of -6dB acceptance angle and better than 100% bandwidth are evident from the spectrum-angle plot.

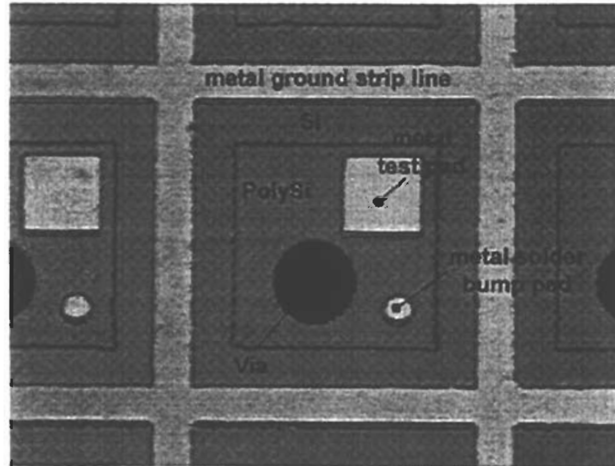

Fig. 5. Back side view of 2-D Immersion cMUT array.

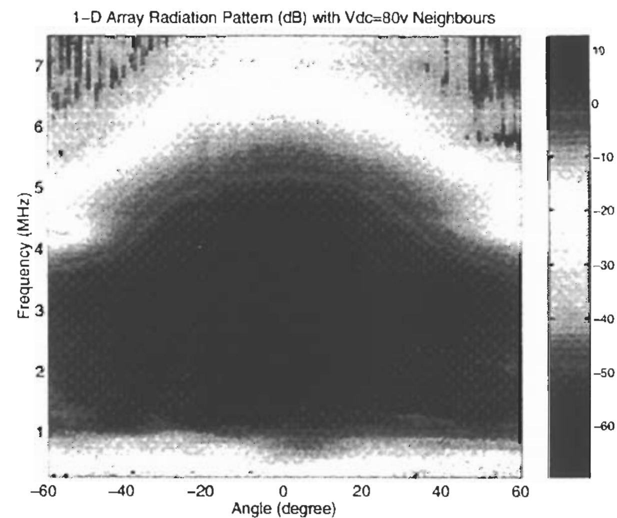

Fig. 6. 1-D Array element radiation pattern.

An 275um square active cMUT source is imaged with a 64 element 1-D array. Better 25dB signal to noise is achieved in the reconstructed image as shown in Fig. 7.

As a measure of the total tolerable loss in pulse-echo operation, one can define a dynamic range (DR) for the transducer as the ratio of the pressure output of the transducer to the minimum detectable pressure. A 2-D array element achieved a total dynamic range of 150 dB/Hz for 10 V input voltage at 3 MHz. The measured and simulated dynamic range are shown in Fig. 8 for 1 V input voltage. The simulation result using a different amplifier and reduced parasitics shows that a 160 dB/Hz dynamic range for 10 V input voltage is achievable at 3 MHz.

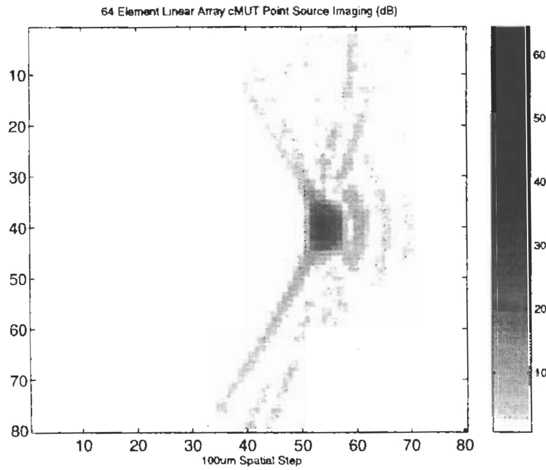

Fig. 7. Point source image reconstruction.

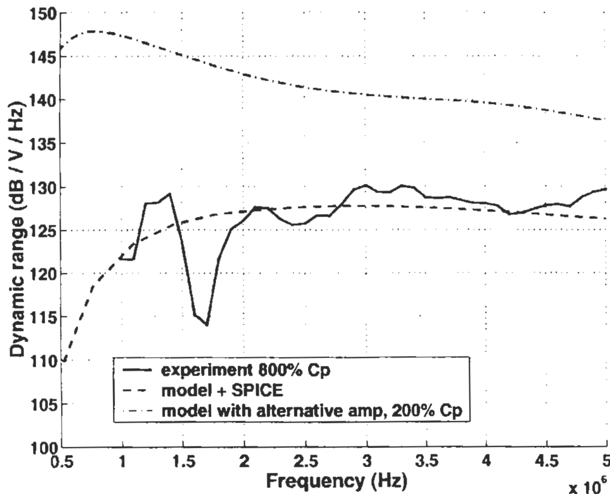

Fig. 8. .2-D Array element experimental results.

V. Conclusion

This paper presents a systematic analysis on design and fabrication of capacitive ultrasonic immersion transducer arrays. Various process options and alternatives are summarized based on membrane formation schemes and cavity sealing methods. Transducer electronics co-fabrication and flip chip bonding technology makes it possible to eliminate massive cable interconnects between transducer arrays and their peripheral electronics.

64 element 1-D arrays and 16 x 16 element 2-D arrays are designed and fabricated in this paper. The bandwidth, acceptance angle and transducer dynamic range measurements show the excellent performance of cMUT array elements which are suitable for array operation. A preliminary imaging results from 64 element 1-D array transducers are also presented. The experiments in this paper show that micromachined ultrasonic capacitive immersion transducer arrays are competitive alternatives to conventional piezoelectronic ultrasonic transducer arrays.

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References

[1] Eccardt, P., Niederer, K., and Fischer, B., "Micromachined transducers for ultrasound applications," in *Ultrasonics Symposium*, Toronto, Canada, October 1997, IEEE Ultrasonics, Ferroelectrics, and Frequency Control Society, vol. 2, pp. 1609–1618.

[2] Jin, X. C., Ladabaum, I., and Khuri-Yakub, B. T., "The microfabrication of capacitive ultrasonic transducers," in *International Conference on Solid-State Sensors and Actuators*, Chicago, USA, June 1997, IEEE Electron Device Society, pp. 437–440.

[3] Jin, X. C., Ladabaum, I., and Khuri-Yakub, B. T., "The microfabrication of capacitive ultrasonic transducers," *IEEE/ASME Journal of Microelectromechanical Systems*, vol. 7, no. 3, pp. 295–302, September 1998.

[4] Haller, M. I. and Khuri-Yakub, B. T., "A surface micromachined electrostatic ultrasonic air transducer," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 43, no. 1, pp. 1–6, January 1996.

[5] Ladabaum, I., Jin, X. C., Soh, H. T., Atalar, A., and Khuri-Yakub, B. T., "Surface micromachined capacitive ultrasonic transducers," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 45, no. 3, pp. 678–690, May 1998.

[6] Haller, M. I.and Khuri-Yakub, B. T., "A surface micromachined electrostatic ultrasonic air transducer," in *Ultrasonics Symposium*, Cannes, France, 1994, IEEE Ultrasonics, Ferroelectrics, and Frequency Control Society, pp. 1241–1244.

[7] Ladabaum, I., Jin, X. C., Soh, H. T., Pierre, F., Atalar, A., and Khuri-Yakub, B. T., "Micromachined ultrasonic transducers: towards robust models and immersion devices," in *Ultrasonics Symposium*, San Antonio, Texas, November 1996, IEEE Ultrasonics, Ferroelectrics, and Frequency Control Society, pp. 335–338.

[8] Jin, X. C., Ladabaum, I., and Khuri-Yakub, B. T., "Surface micromachined capacitive ultrasonic immersion transducers," in *IEEE Workshop on Microelectromechanical Systems*, Heidelberg, Germany, January 1998, pp. 649–654.

[9] Eccardt, P., Niederer, K., Scheiter, T., and Hierold, C., "Surface micromachined ultrasound transducers in CMOS technology," in *Ultrasonics Symposium*, San Antonio, Texas, November 1996, IEEE Ultrasonics, Ferroelectrics, and Frequency Control Society, pp. 959–962.

[10] Soh, H. T., Ladabaum, I., Atalar, A., Quate, C. F., and Khuri-Yakub, B. T., "Silicon micromachined ultrasonic immersion transducers," *Applied Physics Letters*, vol. 69, no. 24, pp. 3674–3676, 1996.

[11] Jin, X. C., Ladabaum, I., Degertekin, F. L, Calmes, S., and Khuri-Yakub, B. T., "Fabrication and characterization of surface micromachined capacitive ultrasonic immersion transducers," *IEEE/ASME Journal of Microelectromechanical Systems*, vol. 8, no. 1, pp. 100–114, March 1999.

[12] Jin, X. C., Calmes, S., Cheng, C. H., Degertekin, F. L., and Khuri-Yakub, B. T., "Micromachined capacitive ultrasonic immersion transducer array," in *International Conference on Solid-State Sensors and Actuators*, Sendai, Japan, June 1999, IEEE Electron Device Society, pp. 1500–1503.