A Multichannel, Pipeline Analog-to-Digital Converter for an Integrated 3-D Ultrasound Imaging System

Kambiz Kaviani

Center for Integrated Systems
Stanford University
kambiz@stanford.edu

Ömer Oralkan

Center for Integrated Systems
Stanford University
ooralkan@stanford.edu

Butrus T. Khuri-Yakub

E. L. Ginzton Laboratory
Stanford University
khuri-yakub@stanford.edu

Bruce A. Wooley

Center for Integrated Systems
Stanford University
wooley@ee.stanford.edu

Abstract

An 8-channel, 10-bit pipeline analog-to-digital converter (ADC) designed for use in an integrated 3-dimensional ultrasound imaging system, has been implemented in a 0.25-μm CMOS technology. Two parallel sample-and-hold stages are employed to multiplex a total of 8 adjacent ultrasound channels, each sampled at 20 MHz. The sampled and multiplexed signals are fed into two parallel pipelines, each operating at 80 MHz. These two pipelines are subsequently multiplexed into a single pipeline operating at 160 MHz to conserve area. An experimental prototype of the proposed architecture occupies less than 4 mm^2 of silicon area and achieves a peak SNDR more than 54 dB for a 2.1-MHz input signal, while dissipating only 20 mW per each analog input channel from a 2.5-V power supply.

1. Introduction

Real-time three dimensional (3-D) ultrasound imaging for medical and underwater applications is an area of expanding research interest. The realization of a real-time 3-D ultrasound imaging system depends on the fabrication of two dimensional transducer arrays with individually addressable elements together with supporting control and data acquisition circuits.

Capacitive micromachined ultrasonic transducers (CMUTs) can be fabricated using standard silicon integrated circuit fabrication technology and provide both wide bandwidth and high sensitivity, as well as the potential for integration with supporting circuitry [1]. Consequently, CMUTs are an attractive transducer choice for 2-D phased imaging arrays. Each element in a 2-D CMUT array is addressable through a through-wafer via interconnect [2], and such an array can be integrated with peripheral circuits using a flip-chip bonding technology to realize an imaging probe of the type shown in Fig. 1.

The proposed image reconstruction algorithm for the system depicted in Fig. 1 employs a low-cost front-end architecture, yet provides high quality imaging through phased sub-array processing of the echo signals acquired by a small active phased sub-array multiplexed over a large transducer array [3]. The front-end interface circuits required include low-noise pre-amplifiers together with analog multiplexers that route the transmit and receive signals to and from the selected sub-arrays, respectively.

The received signals in an ultrasound imager have a very large dynamic range as a consequence of variations in echo amplitude at fixed distances and the attenuation of echoes that increases with distance. Time gain control (TGC) amplifiers can be used to compensate for attenuation, thus reducing the dynamic range required in the subsequent digitization of the signals [4]. The implementation of the analog-to-digital (A/D) conversion as an integral part of the system decreases the sensitivity of the system to the analog circuit imperfections and eliminates the need for an unmanageable number of interconnects between the ultrasonic probe and the processing unit. On the other hand, constraints on the power dissipation and

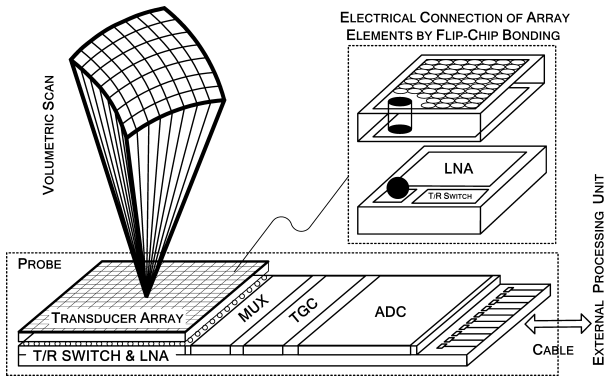

Fig. 1 Schematic of the integrated ultrasound probe

the area of the A/D converter are complicated by the need to process many channels in parallel. The area and power constraints become especially severe for ultrasound probes designed to fit in an endoscope [5].

In recent years switched-capacitor pipeline architectures have emerged as an attractive approach for the implementation of Nyquist-rate, medium-to-high resolution A/D conversion in wideband applications [6]-[8]. Pipeline A/D converters offer power and area advantages over the flash and multistep approaches at the cost of latency. In particular, the pipeline stages can be scaled to reduce the power and the area of the overall converter [7], [8]. Moreover, as illustrated by this work, later stages in the pipeline can be multiplexed.

This paper describes the architecture and circuit implementation for a multichannel, pipeline A/D converter. An experimental prototype integrated in a 0.25-µm CMOS technology is capable of digitizing eight parallel channels, each with a 10 MHz signal bandwidth, with 10 bits of resolution. The prototype chip occupies less than 4 mm^2 of silicon area and dissipates a total of 330 mW from a 2.5-V supply.

2. ADC Architecture

Fig. 2 shows a block diagram of the proposed A/D converter architecture. The outputs from four adjacent ultrasound channels are multiplexed through the front-end sample-and-hold (SAH) circuits into each of the paths comprising the first section of the parallel, pipeline converter. Since the design for 10-bit resolution is limited by *kT/C* noise, the area can be reduced by increasing the number of multiplexed channels by each front-end SAH circuit and also per each parallel section of the architecture. This is due to the fact that the *kT/C* noise does not depend on how many channels are multiplexed but rather on how large the sampling capacitors are. To increase the number of multiplexed input channels, a 1.5 bit-per-stage architecture has been chosen to realize the pipeline stages since it has the highest conversion speed and also the least area compared to higher bits-per-stage architectures [9]. Since the resolution required for the later stages in the pipeline is relaxed [9], the two parallel paths of the converter can be merged into a single path operating at twice the sampling frequency of the first section of the converter. This multiplexing becomes possible when the settling time needed to achieve the resolution required for the remaining stages in the pipeline is half that required in the first section. In this design, the multiplexing of the pipeline paths can be implemented once the 5 most significant bits of the conversion have been resolved. A single pipeline can then be used to resolve the 5 least significant bits for both paths. In this second section of the pipeline, the resolution is no longer noise limited, and the capacitors can therefore be scaled aggressively. This scaling not only reduces the area and power required but also ensures adequate settling of the interstage residue amplifiers in the multiplexed stages due to smaller output load capacitances.

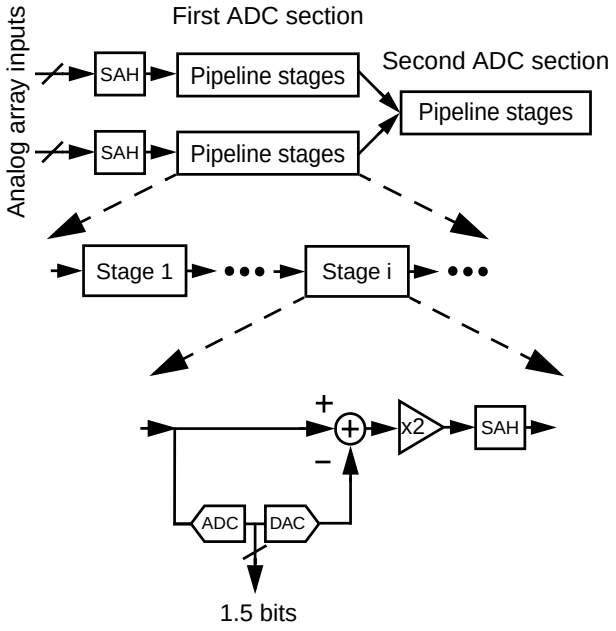

Fig. 2 Proposed ADC architecture

3. Circuit Implementation

Fig. 3 is a simplified schematic of the front-end SAH circuit. Each of the SAH circuits samples four input channels in sequence, as illustrated in the timing diagram, with an overall sampling frequency of 80 MHz. This provides Nyquist-rate sampling for each 10-MHz bandwidth analog input channel. In addition, the two SAH circuits are time interleaved so that while one is in the sampling, or tracking mode, the other is holding the sampled signal. This time-interleaved operation is needed to allow for the subsequent multiplexing of the two parallel pipeline paths, as demonstrated later in this section. Each SAH stage has been implemented as a fully

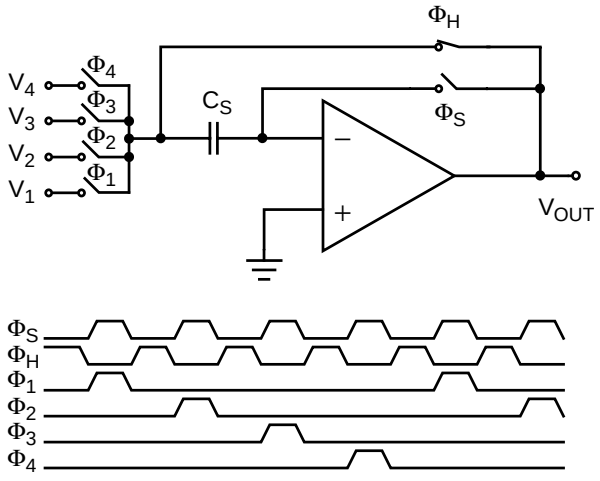

Fig. 3 SAH circuit and input multiplexing timing diagram

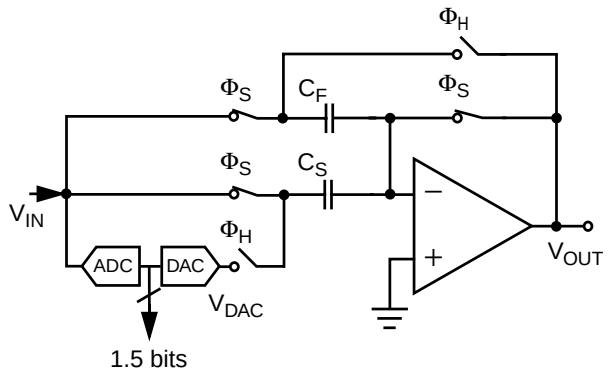

Fig. 4 Pipeline stage schematic

differential switched-capacitor circuit with the unity gain feedback to suppress the supply and common-mode disturbances due to the mixed-mode nature of the circuit. To reduce the area of the SAH stage, the sampling capacitor is also used as the holding capacitor around the operational amplifier [10], as shown in Fig. 3.

Similarly, the pipeline stages have been implemented differentially, with holding capacitors again employed in the sampling mode to increase the conversion rate and lower the area of the stage, as shown in Fig. 4 by a single-ended circuit schematic for the sake of simplicity.

Fig. 5 shows how the two parallel pipeline paths are merged later in the pipeline into a single pipeline path operating at 160 MHz. As can be inferred from the timing diagram, the multiplexing is only possible when the two multiplexed stages and therefore the two parallel paths are operating in a time-interleaved manner. To ensure adequate settling of the two multiplexed pipeline stages, the clocking scheme shown in Fig. 5 is employed so that the 80 MHz clocks Φ_{11} and Φ_{12} will fall after the 160 MHz Φ_{21} clock falls.

Telescopic gain-boosted operational amplifiers are used in all pipeline stages, as well as the SAH circuits. The cascode topology provides a high-speed, single stage

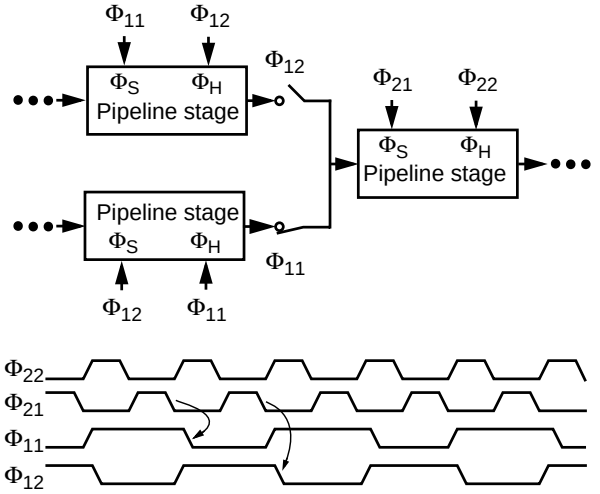

Fig. 5 Stage multiplexing clock scheme

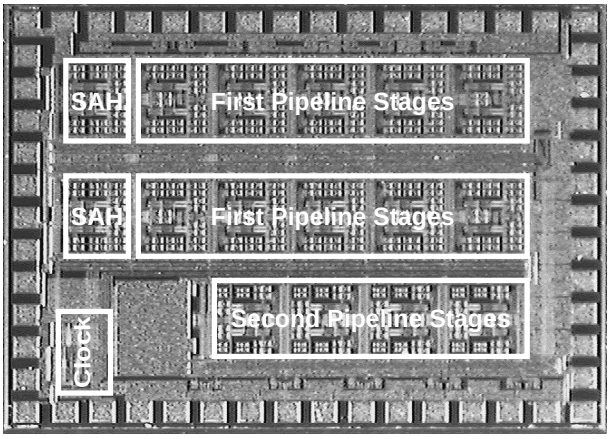

Fig. 6 ADC die photo

design with minimal power dissipation. Switched-capacitor common-mode feedback is used to bias the differential amplifiers.

The clock input to the prototype chip is a low-swing differential clock at 320 MHz and is used to generate the non-overlapping clock phases Φ_{11}, Φ_{12}, Φ_{21} and Φ_{22} and their delayed replicas, which are used to minimize signal-dependent charge injection. Also, the rising edge of each clock and its delayed version are aligned to allow more time for the settling of the interstage residue amplifiers while in the hold mode.

4. Experimental Results

An experimental prototype has been fabricated in a 0.25-μm, 5-metal, CMOS technology and occupies 4 mm^2 of silicon area, including the pads, while only using metal-to-metal capacitors. A die photo of the pad-limited chip is shown in Fig. 6. The measured SNR and SNDR vs. input level and input frequency are presented in Fig. 7 and Fig. 8, respectively. An FFT plot of the spectrum of a digital output is shown in Fig. 9, illustrating that the crosstalk from an adjacent 2.1-MHz signal is suppressed by more than 70 dB. The performance of the experimental prototype is summarized in Table I.

5. Conclusion

A multichannel, pipeline analog to digital converter has been designed and implemented for an integrated 3-D ultrasound imaging system. Multiplexing has been used to reduce the area of the converter. The modular architecture offers a practical choice for array processing and allows the integration of larger transducer arrays as the technology shrinks to smaller feature sizes. Although the architecture was originally designed for an ultrasound imaging system, it can be used to implement A/D converters for other multichannel applications, such as general purpose data acquisition, multichannel communication systems, and other multi-sensor systems.

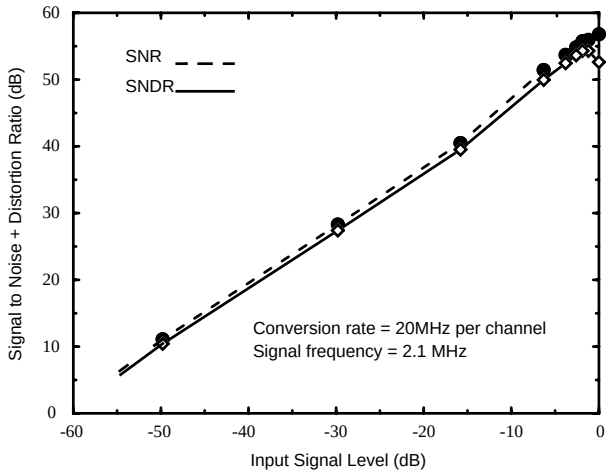

Fig. 7 Measured SNR and SNDR vs. input signal level

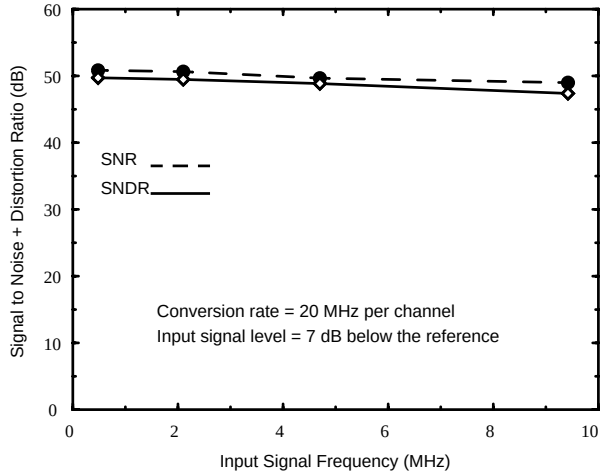

Fig. 8 SNDR vs. input signal frequency

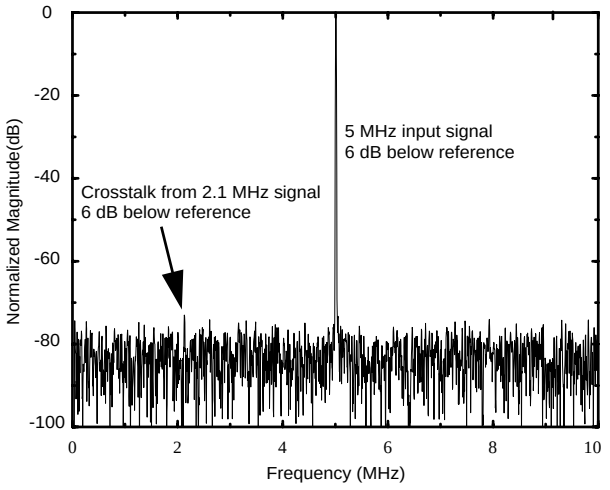

Fig. 9 FFT spectrum of a digital output channel

Table I. Measured ADC performance

Supply voltage	2.5 V
Number of input channels	8
Sampling rate per channel	20 MHz
Peak SNDR(@2.1MHz)	54.3dB
Peak SNR(@2.1MHz)	56.8dB
Power Dissipation	
Digital including output drivers	170 mW
Analog per each channel	20 mW
Total	330 mW
Die area including the pads	4 mm^2
Technology	CMOS 0.25µm

6. Acknowledgments

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7. References

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