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Fabrication of Anodically Bonded Capacitive Micromachined Ultrasonic Transducers with Vacuum-Sealed Cavities

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Abstract*—Capacitive micromachined ultrasonic transducers (CMUTs) have demonstrated great promise for next-generation ultrasound technology. Wafer-bonding technology particularly simplifies the fabrication of CMUTs by eliminating the requirement for a sacrificial layer and increases control over device parameters. Anodic bonding has many advantages over other bonding methods such as low temperature compatibility, high bond strength, high tolerance to particle contamination and surface roughness, and cost savings. Furthermore, the glass substrates lower the parasitic capacitance and improve reliability. The major drawback is the trapped gas inside the cavities, which occurs during bonding. Earlier CMUT fabrication efforts using anodic bonding failed to demonstrate a vacuum-sealed cavity. In this study, we developed a fabrication scheme to overcome this issue and demonstrated vacuum-backed CMUTs using anodic bonding. This new approach also simplifies the overall fabrication process for CMUTs. We demonstrated a CMUT fabrication process with three lithography steps. A vibrating plate is formed by bonding the device layer of a silicon-on-insulator (SOI) wafer on top of submicron cavities defined on a borosilicate glass wafer. The cavities and the bottom electrodes are created on the borosilicate glass wafer with a single lithography step. The recessed bottom metal layer over the glass surface allows bonding the plate directly on glass posts and therefore helps reduce the parasitic capacitance and improve the breakdown reliability. A surface roughness of 0.8 nm is achieved in the cavity using wet chemical etching. A 200-nm PECVD silicon nitride layer deposited on the 2 μm device layer of the SOI wafer prior to bonding serves as the insulation layer to prevent shorting after pull-in. The trapped gas inside the cavities is evacuated after anodic bonding by reactive ion etching. The 120-nm cavities are then sealed with PECVD silicon nitride. We measured the atmospheric deflection of the plates after fabrication, which proves the vacuum inside the cavities. Impedance and hydrophone measurements were performed both in conventional (2.8 MHz) and collapse (7.2 MHz) modes. Bonding on posts with widths as small as 2 μm was successfully demonstrated using anodic bonding which is difficult to achieve with other wafer bonding methods.

I. Introduction

The fabrication of CMUTs has made a significant progress since they were first introduced. The advances in the microfabrication technology has enabled fabrication of more efficient CMUTs with high electrical field strength maintained in a submicron vacuum gap. First demonstrated CMUTs were fabricated using the sacrificial release method, in which the cavities are formed by selectively removing the sacrificial layer under the plate. The plate is created by deposition of an additional layer on the sacrificial layer, thus the thickness is limited and requires well control over the deposition parameters. On the other hand, the removal of sacrificial layer leads to stiction of the plate due to the capillary forces, especially when the gap height is low. The etching holes also occupy some space over the transducer surface and reduces the fill factor.

Wafer bonding methods simplify the CMUT fabrication and provide a flexible environment to chose the mechanical properties and the thickness of the vibrating plate [1]. In this method, cavities are created on a substrate before the bonding. The required plate is then bonded over the cavities in a vacuum environment to form the CMUT structure. Most common wafer bonding technique that is used for CMUT fabrication is fusion bonding. Typically, a thermal oxide layer is grown on a conductive silicon substrate and cavities are formed by etching this oxide layer leaving oxide posts around the cavities. A second oxidation creates the insulating layer required for a proper CMUT operation. The oxide posts are bonded to the device layer of an SOI wafer at a high temperature, usually over 1100°C. The handle and the BOX layers are removed to leave the plate which serves as the vibrating structure and the top electrode of the device. The distance between the cavities can be reduced and thus the fill factor can be increased but sufficient bonding surface should be left. However, fusion bonding requires flat surfaces with a surface roughness less than 1 nm and can not tolerate contamination. The breakdown voltage is limited with the post thickness and the devices suffer from high parasitic capacitance. An improved version of this process uses local oxidation of silicon (LOCOS) to further extend the oxide thickness in the post region at the cost of increased fabrication complexity [3], [4].

Anodic bonding, on the other hand, combines the advantages of wafer bonding and a dielectric substrate which makes it potentially an ideal candidate for CMUT fabrication. This bonding technique is a well-know process, which is extensively used by industry for packaging. It is a simple, well characterized, and low cost method as compared to other bonding techniques. Its tolerance to surface roughness and contamination is considerably high. It has been demonstrated that metal electrodes can be buried into the glass substrate and the glass wafer can be anodically bonded with an SOI wafer to fabricate CMUTs [5], [6]. The major drawback is the

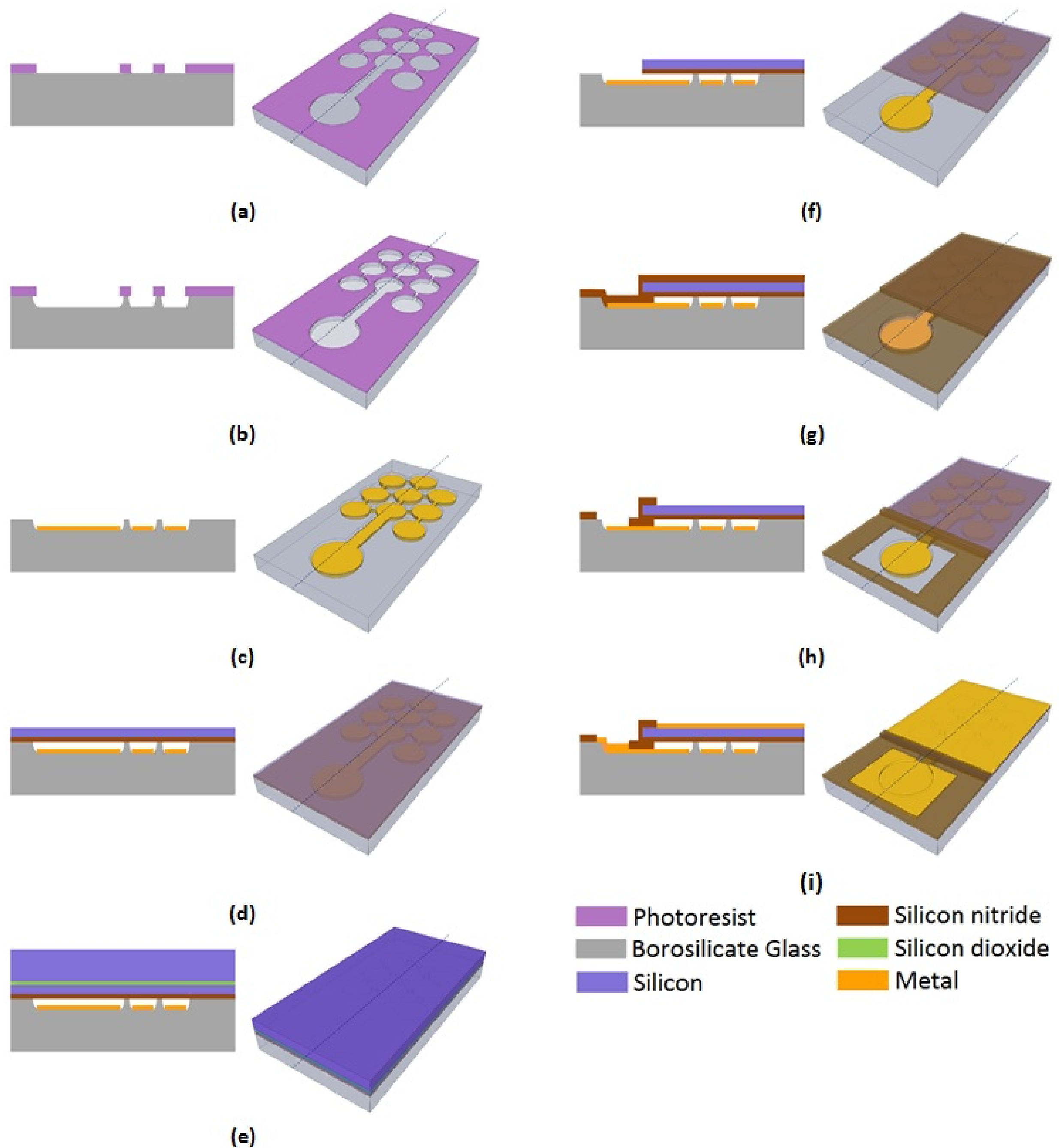

Fig. 1. Fabrication process flow. (a) Photoresist coated glass substrate; (b) Lithography for cavity pattern; (c) BOE etch; (d) Metal deposition and lift-off; (e) Anodic bonding; (f) Handle and BOX removal; (g) Silicon etch for array separation and reaching pads; (h) Silicon nitride deposition for sealing; (i) Silicon nitride etch; (j) Metal deposition and lift-off.

outgassing during bonding and consequently trapped gas in the cavities. The devices fabricated with this method lack vacuum cavity. In this paper, we overcame this issue and fabricated vacuum-sealed CMUTs using anodic bonding with only three photolithography masks.

II. Fabrication Process

The fabrication process flow is given in Fig. 1. The fabrication starts by forming the cavities on the borosilicate glass substrate. The glass substrate was first cleaned using Piranha solution. We used AZ5214E-IR photoresist and patterned it using the first photolithography mask. The cavities can be formed either by wet chemical etching or reactive ion etching. We preferred wet chemical etching and used buffered oxide etch (BOE) (10:1) to etch the borosilicate substrate. Before etching, the photoresist was hard-baked for 1 hour in order to improve the adhesion between the photoresist and the

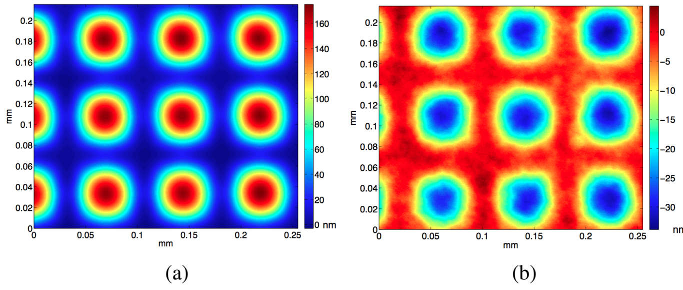

Fig. 2. The deflection of the plate after handle and BOX removal (a) and the atmospheric deflection after sealing (b)

substrate. The lateral etch rate was measured 20 times higher than vertical etch rate. In order to prevent the peeling of resist during BOE etch, the total etch time is divided into 3-min slots and the resist is hard baked for 10 mins between each slot. We targeted an etch depth of 230 nm. We achieved a surface roughness of 0.8 nm at this depth. After etching the cavities, photoresist was not removed and the wafer was directly placed into the evaporation chamber for metal depositon. We deposited 20 nm chromium and 90 nm metal. The undercut due to the lateral etch eases the lift-off. The gap height is determined by the difference between the deposited metal thickness and the etch depth of the cavity. Next step is to deposit silicon nitride on the device layer of the SOI. This layer serves as an intermediate bonding layer, as well as an insulating layer to prevent the electrical shorting in collapse mode. We deposited 200-nm PECVD silicon nitride on the SOI wafer. We tested bonding at various voltages. As the bottom electrode floats, the high electrical field applied during the bonding can damage it. We started from a higher voltage and tried bonding at a lower voltage each time until we get no damage on the gold and still achieve high bonding yield. It turned out that the required voltage is 700 V for this case. After bonding the handle wafer was ground down to 100 μm and the rest was removed using heated tetramethylammonium hydroxide solution (10% TMAH at 80°C). BOX layer was removed using 10:1 BOE solution. The deflection profile is measured with an opticle surface profiler (Fig. 2a). An upward deflection was observed due to the pressured gas inside the cavities. We did a second lithography and etched the silicon over the bottom electrode pad in order to evacuate the gas. The photoresist was then removed by oxygen plasma. The wafer was placed back again into the PECVD chamber to seal the cavities at the bottom pad locations. For a proper sealing, 800-nm conformal silicon nitride was deposited which was at least three times higher than the cavity depth [7]. To create electrical contact pads, the silicon nitride over the plate and the pad is removed by masking the sealing location. This third and last patterned photoresist layer is also used for lift-off purpose to deposit metal over the bottom pad and over the silicon plate to get better conductivity. The deflection profile measurement was repeated over the same region and the observed profile was shown in Fig. 2b.

TABLE I
PHYSICAL PARAMETERS OF THE TESTED CMUT

Shape of the cell	Square
Cell width, μm	71
Cell-to-cell distance, μm	4
Top metal thickness, μm	0.15
Silicon layer thickness in plate, μm	1.8
Insulating layer thickness in plate, μm	0.2
Gap height, μm	0.12
Bottom metal thickness, μm	0.11
Substrate thickness, μm	700
Number of cells per element	270
Length of an element, μm	2240
Width of an element, μm	665

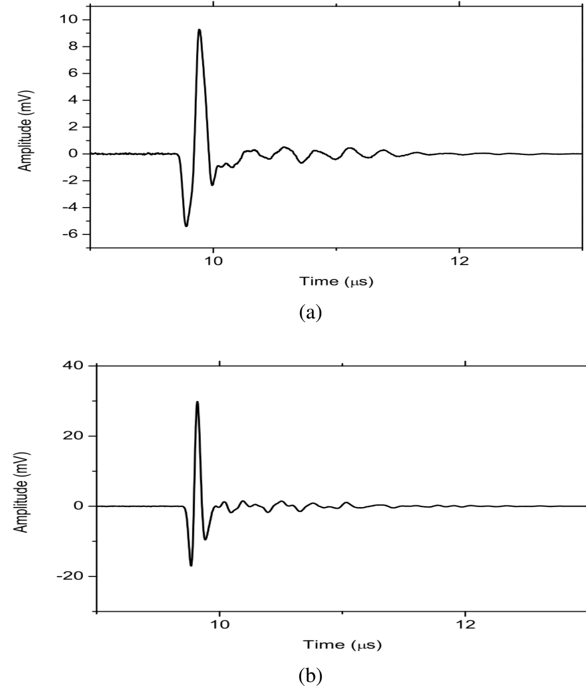

Fig. 3. Measured hydrophone output for fabricated device in immersion at 14-mm from the transducer (time domain). (a) Conventional mode (V_{DC} = 12 V), (b) Collapse mode (V_{DC} = 30 V).

III. CHARACTERIZATION

We selected one of the test elements and characterized it. The physical properties of the selected CMUT element is given in Table I. Impedance measurements were done using an impedance analyzer. The collapse voltage was measured as 22 V. The same element was used for characterization in immersion. The immersion experiments were done in vegetable oil. The hydrophone was placed 14 mm away from the transducer surface. The conductive plate layer was grounded and the bottom electrode was used as the active electrode. First, a 110-ns unipolar pulse with an amplitude of 20 V was superimposed on a DC bias of 12 V and applied to CMUT through a bias-T circuit. In that case, the CMUT operates in the conventional mode. The measured hydrophone output, after correcting for attenuation and diffraction losses, shows that the CMUT has a center frequency of 2.8 MHz (Fig. 4a). The

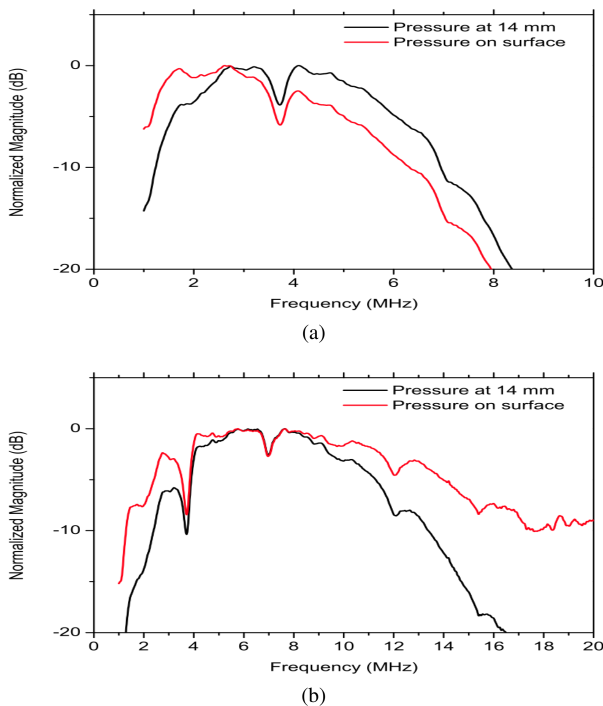

Fig. 4. Fourier transform of the measured hydrophone output for fabricated device in immersion at 14-mm from the transducer. (a) Conventional mode (V_{DC} = 12 V); (b) Collapse mode (V_{DC} = 30 V).

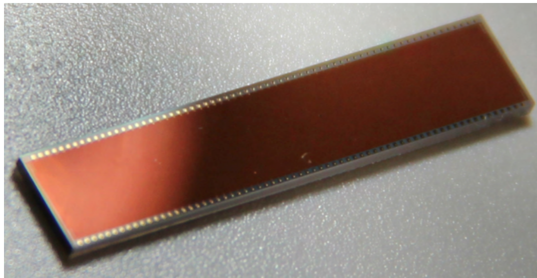

Fig. 5. Fabricated 1D CMUT array

transmit sensitivity is 11 kPa/V and the fractional bandwidth is 107% for this operation mode. We further increased the DC voltage up to 30 V to operate the CMUT in collapse mode. The pulse amplitude was kept constant but the pulse with is reduced to 60 ns. The center frequency of the device shifted to 7.2 MHz (Fig. 4b) due to collapse and the transmit sensitivity is increased to 28 kPa/V. And we observed a fractional bandwidth of 126% for the collapse mode. The presented frequency spectrum is not corrected for the pulse shape. Lastly, we checked the resonant frequency of each individual element in an imaging array that we fabricated (Fig. 6). The results show that the standard deviation is 0.11 MHz with a mean value of 12.5 MHz in resonant frequency for a 66-element array.

IV. Conclusion

We have presented a simple fabrication process for CMUTs using anodic bonding. Besides the known advantages of wafer bonding, the process is low-cost and tolerates higher surface roughness. Furthermore, maximizing the fill factor is possible because anodic bonding can be performed on smaller contact area. We have demonstrated bonded posts with a width as low as 2 μm, which is difficult to achieve with other bonding methods. The bonding temperature is 350°C, which allows use of a patterned metal bottom electrode for improved series resistance. The usage of an insulating substrate reduces the parasitic capacitance. The experimentally measured characteristics and uniformity show that this fabrication process is suitable for implementation of CMUT imaging arrays.

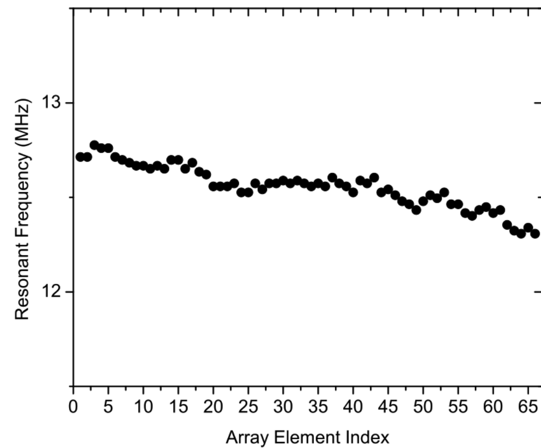

Fig. 6. Distribution of resonant frequency over the array elements

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