22.9 3D Volumetric Ultrasound Imaging with a 32×32 CMUT Array Integrated with Front-End ICs Using Flip-Chip Bonding Technology

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3D ultrasound imaging is becoming increasingly prevalent in the medical field. Compared to conventional 2D imaging systems, 3D imaging can provide a detailed view of tissue structures that makes diagnosis easier for the physicians. In addition, 2D image slices can be formed at various orientations to the transducer, making the examination less dependent on the skill of the sonographer. However, various challenges exist in developing a 3D imaging system, such as integration of a large number of elements, as well as post-processing of datasets received from a large number of channels. 2D transducer arrays are typically integrated with custom ICs in the probe handle to perform some intermediate beamforming and to reduce the number of cable connections to the imaging system. Capacitive micromachined ultrasonic transducers (CMUTs) have emerged as an alternative to piezoelectric transducers. Being a MEMS device, they greatly benefit from flexibility and ease of fabrication, and can be seamlessly integrated with electronics. Previous work [1] demonstrates 3D stacking of CMUTs and dummy ICs with an intermediate interposer layer. However, that represents more of a mechanical demonstration of 3D integration. In this paper, we present a fully functional 3D ultrasound imaging system comprising a 32×32 2D CMUT array, 3D-stacked with front-end ICs using flip-chip bonding technology. The imaging system is capable of capturing real-time volumetric ultrasound data, and displaying 2D and 3D ultrasound images.

Compared to piezoelectric transducers, CMUTs typically have wider bandwidth, which translates to better axial resolution, and benefit from MEMS fabrication processes allowing for direct integration with ICs. CMUT technology also allows for batch processing, thereby reducing the overall cost of manufacturing. The 2D CMUT arrays of this work (Fig. 22.9.1) are fabricated in-house using a process described in [2]. They are designed to have a center frequency of 5MHz, a pull-in voltage of 36V, and an element-to-element pitch of 250µm. They also incorporate through-silicon vias (TSVs) to enable flip-chip bonding.

Figure 22.9.2 depicts a partial block diagram of the IC. This is a slightly modified version of the IC presented in [3]. The IC is fabricated in a 1.5µm high-voltage process. Each IC consists of 256 elements, capable of interfacing a 16×16 array of CMUT elements for transmit and receive. The transmit circuitry is capable of generating a focused ultrasound beam, and consists of an 8b shift register, a comparator, a one-shot circuit, and a 25V pulser (adapted from [4]) in each element. On the receive end, each element consists of a transimpedance amplifier and an output buffer. The amplifier has a bandwidth of 25MHz and consists of a common-source amplifier, a source-follower buffer, and a 215kΩ feedback resistor. The output buffer is designed to drive capacitive loads of up to 50 pF, and has an 800mV peak-to-peak output swing for frequencies up to 10MHz. A high-voltage switch protects the low-voltage receiver from the pulser in each IC element.

The IC can be used in two modes: pulse-echo or photo-acoustic. However, for the scope of this paper, we limit our discussion to the pulse-echo mode of operation. To improve the frame rate of the displayed image and minimize the front-end hardware complexity, we use only the 64 diagonal elements for receive mode. As mentioned in [5], the image quality obtained using only diagonal elements in receive mode is very comparable to that obtained using all elements. However, we gain a great deal in achievable frame rate, as well as the ability to limit the number of cables that would be needed to interface the back-end system. The power consumption varies depending on the strategy used in transmit beamforming, and on the imaging method. We used the classical phased-array imaging method, and the measured power consumption by the entire CMUT-Interposer-IC assembly is 600mW, corresponding to a power density of 2.5mW/mm^2.

Tight integration of the CMUT array and the IC is key to improving noise performance and receive sensitivity, leading to better image quality. Therefore, the CMUT array and the front-end ICs are 3D stacked with the help of an intermediate interposer layer using flip-chip bonding technology. In some cases, the CMUT array can be directly flip-chip bonded to the IC. However, having an interposer layer enables tiling several CMUT arrays to the front-end ICs to create a large-area, integrated 2D array, which would not be otherwise feasible to implement in a single chip. For our device assembly presented in this paper, a 32×32 CMUT array is formed by tiling four 16×16 CMUT arrays. Polishing of two edges of each CMUT die is necessary to achieve compact tiling. The four CMUTs are flip-chip bonded side-by-side on a 2×2 grid on the front side of the interposer (Fig. 22.9.3). Since 1024 CMUT array elements need to be addressed, four ICs are flip-chip bonded to the backside of the interposer. Figure 22.9.3 shows the cross-section of the CMUT-Interposer-IC stack. The interposer is a 6-layer substrate with a minimum trace width of 100µm and a spacing of 50µm. The flip-chip bonding integration is accomplished using 80µm-diameter solder interconnects, resulting in a final gap of approximately 50µm between the CMUT or IC dies and the interposer.

The back-end system consists of an interface board and a PC-based imaging system (Verasonics data acquisition system, Verasonics, Redmond, WA). The CMUT-Interposer-IC assembly is placed and wirebonded onto a PCB substrate, acting as a custom package that "plugs" into the interface board (Fig. 22.9.4). The interface board provides the necessary biasing to the IC, off-chip buffers for the RF channels, and level-shifters for the digital I/O signals. An FPGA board (Virtex-6 FPGA ML605, Xilinx, San Jose, CA) is used to transfer delay sets and necessary control signals to the ICs to enable real-time transmit beamforming. The RF data are received by the Verasonics system and then transferred to a PC for image reconstruction using custom GPU-based software employing classical phased array imaging method.

Figure 22.9.5 depicts the experimental setup. A tank was built to test the assembly in immersion using vegetable oil as the medium. Wire and spring phantoms are used to demonstrate real-time volumetric imaging. Volumetric data are acquired at a rate of 5.4 volumes per second, limited by the 1.2GB/s data transfer rate between the Verasonics system and the PC. A B-mode image of the wire phantom acquired in real-time and a volume-rendered image of the spring phantom are shown in Fig. 22.9.6. These images are obtained with the CMUT array biased at 50% of the pull-in voltage. Currently, volume rendering is done offline and work is in progress to enable real-time rendering. Development of a new IC capable of simultaneous multi-beam transmit scheme is ongoing as well.

Acknowledgments:
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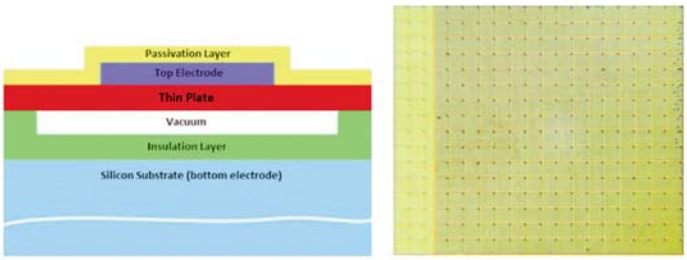

Figure 22.9.1: Basic CMUT cross-section (left) and 2-D 16×16 CMUT array (right).

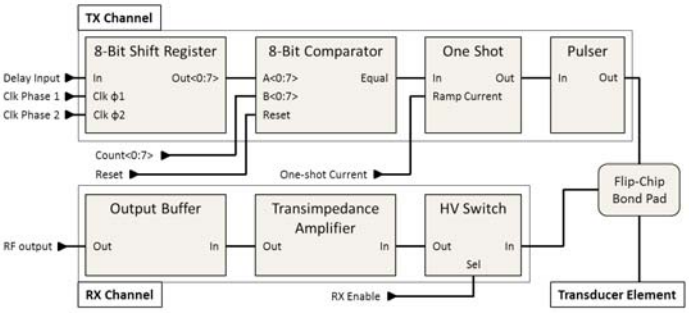

Figure 22.9.2: Block diagram of a single element of the IC.

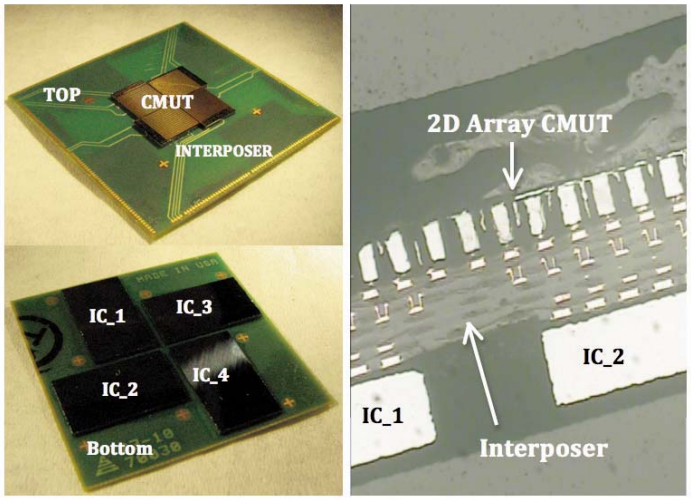

Figure 22.9.3: 3D stack (left) and cross-section (right) of CMUT-Interposer-IC assembly integrated using flip-chip bonding technology.

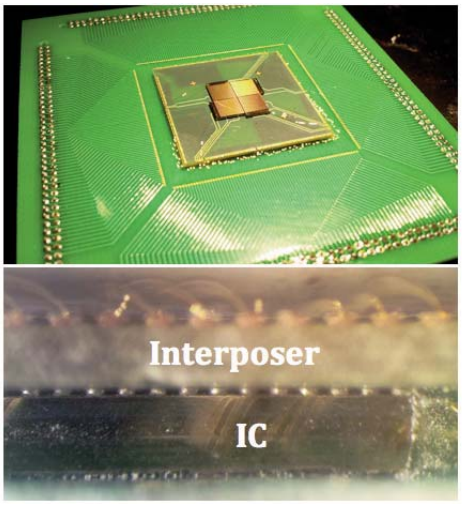

Figure 22.9.4: CMUT-Interposer-IC assembly wirebonded to a custom package (top). Side-view of the assembly showing the IC flip-chip bonded to the interposer (bottom).

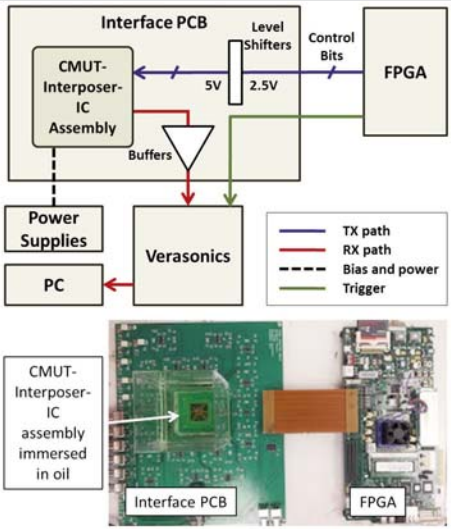

Figure 22.9.5: Block diagram of the experimental setup (top) and photograph of the interface PCB and the FPGA board (bottom).

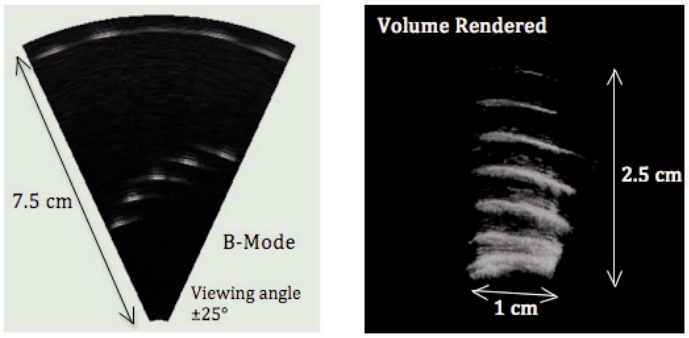

Figure 22.9.6: B-mode image of wire phantom (left) and volume-rendered 3D image of spring phantom (right).

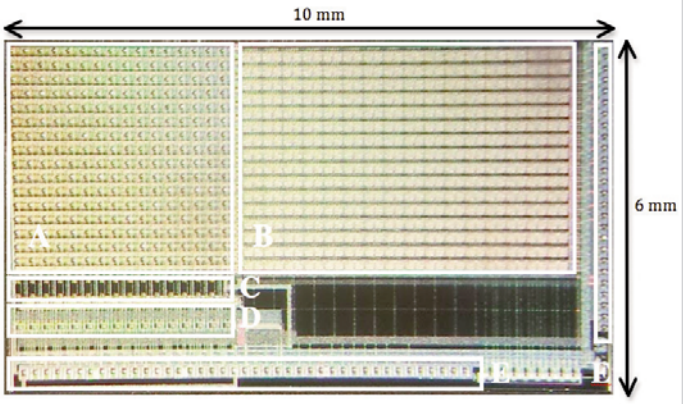

Figure 22.9.7: Die photo of IC. (A) Flip-chip pads, 256 pulsers and receivers. (B) Shift register and comparator array. (C) CMUT DC-bias pads. (D) 16 output buffers. (E) I/O and power pads.

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