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Fabrication of Capacitive Micromachined Ultrasonic Transducers with Through-Glass-Via Interconnects

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***Abstract*—This paper introduces a novel fabrication method for capacitive micromachined ultrasonic transducer (CMUT) arrays amenable to 3D integration. The work demonstrates that MEMS structures can be directly built on a through-glass-via (TGV) substrate. The key feature of this new approach is the combination of TGV interconnects with a vibrating silicon-plate structure formed by anodic bonding. This method simplifies the overall fabrication process for CMUTs with through-wafer interconnects by eliminating the need for an insulating lining for vias or isolation trenches. Fabrication of CMUTs on a glass substrate and use of copper-filled vias as interconnects can help reduce the parasitic interconnect capacitance and resistance, improving device performance and reliability. This work is especially important for fabricating 2D CMUT arrays and integrating them closely with supporting electronic circuits.**

***Index Terms*—CMUT; TGV; Anodic bonding; 3D integration; Glass.**

I. Introduction

Three-dimensional (3D) ultrasound has important medical and underwater applications over the traditional two-dimensional (2D) ultrasound. However, building such a system is significantly more complicated due to the difficulties in the fabrication of 2D transducer arrays and their integration with the front-end integrated circuits (IC). The traditional ultrasound transducers are based on piezoelectric technology. The CMUT technology is an alternative to piezoelectric technology to make 2D ultrasound transducer arrays using the standard IC fabrication processes. When combined with through-wafer-interconnections, CMUT arrays can be directly integrated with the front-end IC by flip-chip bonding, which is critical for the overall CMUT-based system efficiency and also a compact form factor. The primary application of interest in this project is patterned neural stimulation [1]. The developed technology also directly benefits other imaging and therapeutic applications. The current strategies to develop CMUT arrays amenable to hybrid integration are based on through-silicon-via (TSV) interconnects [2], which require an MIS or PN junction isolation to reduce the parasitic capacitance since silicon is a semiconductor. This approach results in an increased process complexity. Also, use of polysilicon as bottom electrode and via material causes roughness in the cavities and induces additional stress, degrading the CMUT performance. The TSV process is limited mainly to surface micromachining CMUT process because the filling of TSV vias creates stress and contaminates the wafer surface, making the scheme unsuitable for fusion bonding [3]. An alternative interconnection method used for CMUTs is to create deep isolation trenches in a highly conducting silicon substrate, where resulting pillars underneath each element serve as the interconnect from the front to the backside of the wafer [3]. This process is still complicated and creates reliability problems due to the exposed gap between top and bottom electrodes of the CMUT on the top surface. Additionally, stress control is critical during this process.

In recent years, TGVs and anodic bonding have been widely used in the interposer technology for both wafer and die-level packaging, especially for radio-frequency (RF) applications [4]. However, MEMS structures have not been built directly on TGV substrates. We have recently reported a process for fabricating vacuum-sealed CMUTs on a glass substrate using anodic bonding [5]. This process benefits from all the advantages of wafer bonding. Additionally, it reduces the parasitic capacitance and series resistance by using an insulating substrate and a metal bottom electrode. It is also lower cost and can tolerate higher surface roughness compared to fusion bonding.

In this paper, we demonstrate that this process could be adapted to 2D CMUT array fabrication by incorporating a TGV substrate. In the following section, we first present the detailed description of the fabrication process flow. In Section III, the via resistance is characterized. Then the electrical input impedance of a fabricated CMUT element is presented.

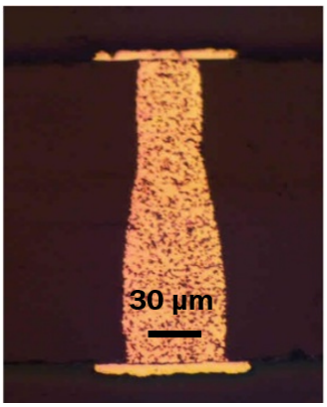


Fig. 1. Optical image of a TGV cross section. (Image courtesy of Tim Mobley, Triton Microtechnologies, Carlsbad, CA)

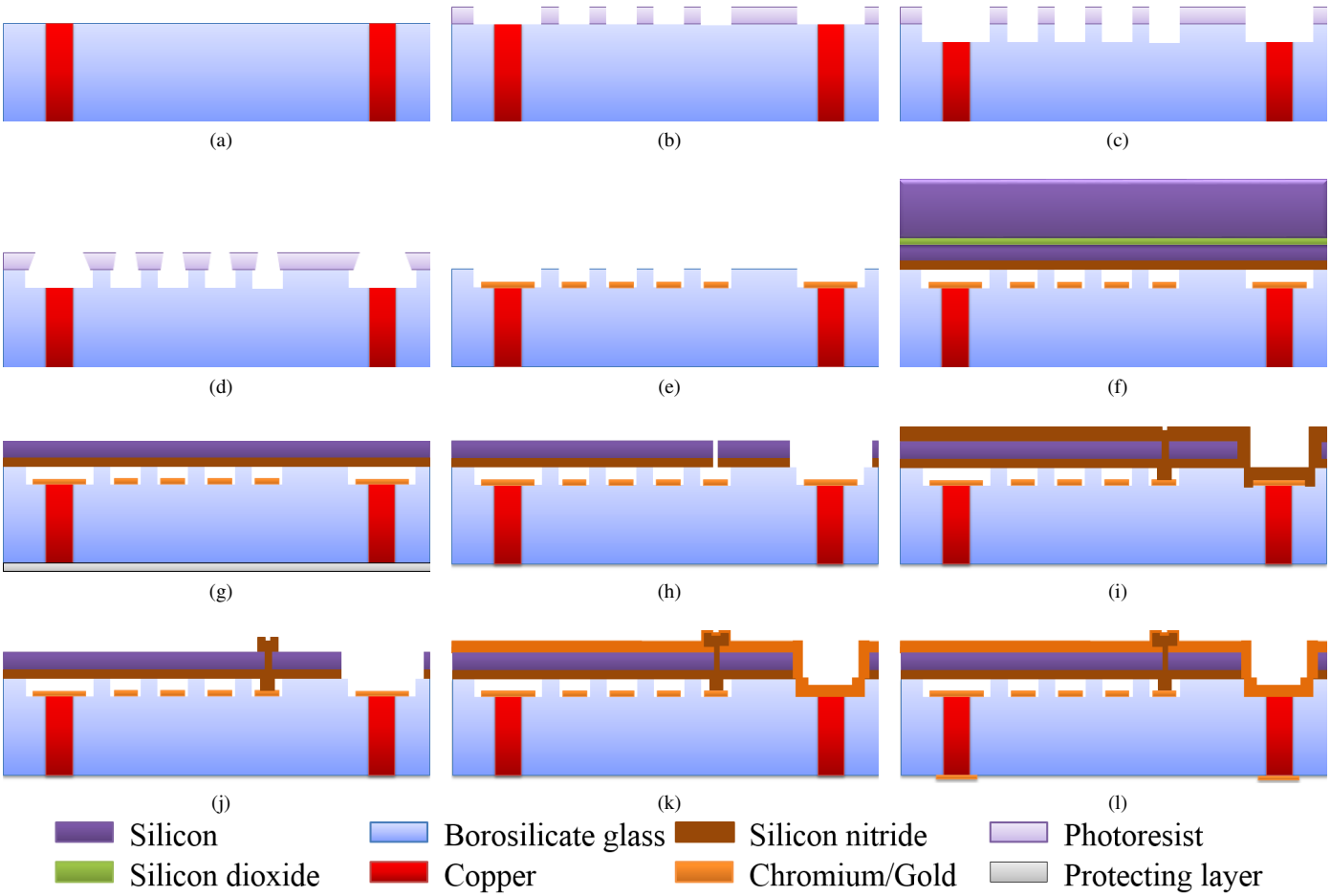
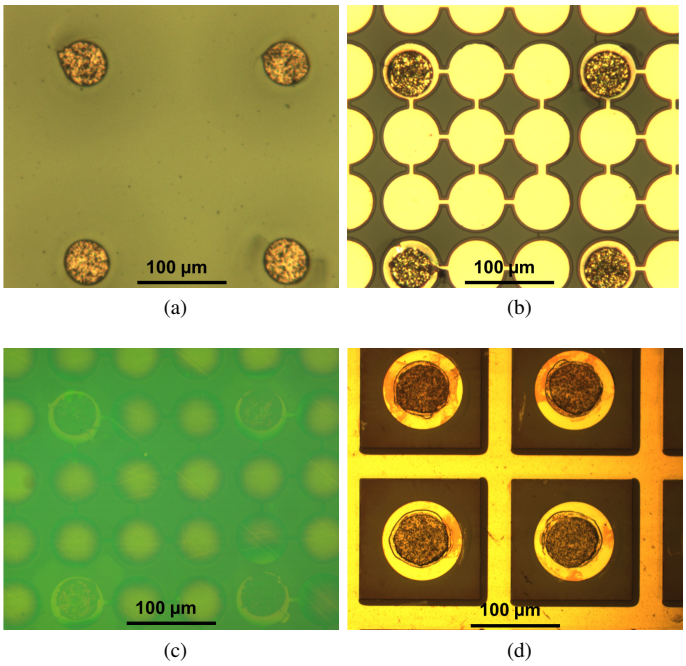


Fig. 2. Fabrication process flow: (a) Initial TGV substrate; (b) Photolithography for cavity patterning; (c) DRIE etch; (d) Photolithography to pattern bottom electrode; (e) Metal deposition and lift-off; (f) Insulation layer deposition on the SOI and anodic bonding; (g) Handle and BOX removal with backside protection; (h) ProTEK removal; Silicon/silicon nitride etch for gas evacuation, array separation, and reaching top electrode connection; (i) Silicon nitride deposition for sealing; (j) Silicon nitride etch; (k) Top electrode deposition; (l) Backside metallization.

II. Fabrication Process

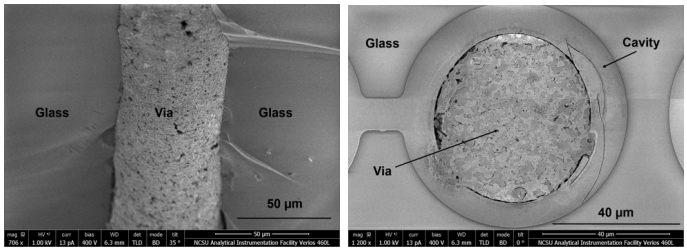
The TGV substrate is fabricated with customized via locations. Through-wafer channels are first created in a 0.7-mm borosilicate glass wafer by laser drilling at the locations where CMUT elements would be connected [6]. The through channels are then filled with thermal coefficient of expansion (TCE) matched copper paste. The wafer is then sintered and polished until a smooth glass surface and a good copper-to-glass surface co-planarity are obtained. Fig. 1 shows the cross section of a single via in a glass substrate. The diameter of the via is 50 µm at the laser exit side and 70 µm at the laser entry side. We build the CMUTs on the laser exit side and use the laser entry side for the backside pad formation. The fabrication process flow is shown in Fig. 2. The TGV substrate was first cleaned using heated N-Methyl-2-pyrrolidone (NMP@70°C) solution for removal of organics and contaminants from the surface. Fig. 3a shows the surface of four vias. The cavities were patterned using negative photoresist aligning to the dedicated through-wafer-via. We performed reactive ion etching to define a cavity depth of 300 nm. The photoresist was then removed and the bottom electrode pattern was defined by a second photolithography step using a 2-µm-thick negative photoresist which is suitable for lift-off. At this step, the copper vias were wet etched to the same depth as cavities to create a planar bottom surface for the electrode. A stacked metal that consists of 20-nm chromium as an adhesion layer and 130-nm gold was deposited to obtain the bottom electrode and define the gap height. The metal thickness was chosen so that it is enough to cover the transition gap from the glass to the via for electrical connection and define a gap height of 150 nm. Fig. 3b shows the top view of the 300-nm cavity with 150-nm bottom metal. An RMS roughness of 0.8 nm and 2.2 nm was measured on the glass post surface and the bottom metal surface, respectively. Next, we deposited 200-nm PECVD silicon nitride insulation layer on the device layer of the SOI wafer. The processed glass surface and an SOI device layer with the insulation layer were brought together and anodically bonded in vacuum at 350°C under 700-V bias voltage. The handle layer of the SOI wafer was ground down to 100 µm.



(a) (b)

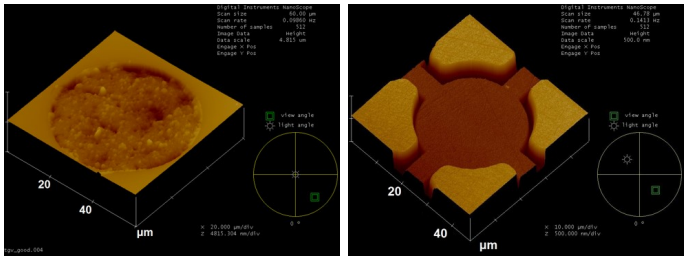
(c) (d)

Fig. 3. (a) Starting TGV substrate; (b) After etching, bottom electrode deposition, and lift-off; (c) After anodic bonding and handle/BOX removal; (d) Backside pad formation.



(a) (b)

Fig. 4. (a) SEM cross-sectional image of a TGV. (b) SEM top-view image of a cavity with a via.



(a) (b)

Fig. 5. (a) AFM image of the initial via surface. (b) AFM image of a circular cell cavity with bottom electrode.

At this step, a protection layer (ProTEK B3 alkaline protective coating, Brewer Science, Rolla, MO) was coated and cured on the backside to protect the vias from tetramethylammonium hydroxide (TMAH) process. A heated TMAH solution (10% TMAH@85°C) was used to selectively etch the remaining handle layer over the BOX layer. The silicon plate was released after removing the BOX layer in 10:1 buffered oxide etch (BOE) solution. The released membrane is shown in Fig. 3c. Then we removed the ProTEK layer on the backside. The third photolithography step was performed to etch the silicon plate with silicon nitride insulation layer in order to access the cavity to evacuate the trapped gas and to reach the vias for top electrode access. The dicing lines to separate arrays were defined at the same step. The wafer was then sealed under vacuum with 800-nm conformal PECVD silicon nitride. In order to connect the plate to vias for top electrode access, the silicon nitride over the plate and on the top connection vias were removed, leaving the PECVD silicon nitride only at the place where sealing was needed. After removing photoresist using oxygen plasma, 20-nm chromium and 300-nm gold were deposited by DC sputtering over the entire wafer. At this step, the process on the front side was completed. The fifth photolithography was done on the backside to define the pads. Fig. 3d shows the backside electrode. Fig. 4 and Fig. 5 show the via and the cavity profiles.

III. Characterization

We measured the resistance of test structures, which include two vias connected with a metal line, by accessing from the backside of the wafer. The via test structures are shown in Fig. 6a and the experimental setup is shown in Fig. 6b. The average resistance of 130-µm, 190-µm and 250-µm long metal lines are 6.81 Ω, 9.69 Ω and 13.13 Ω, respectively. The resistance distribution is shown in Fig. 6c. As a result, the resistance of a single via including the contact resistance is approximately 2 Ω, which is lower compared to the TSV or trench-isolated CMUT implementations [2], [3]. The bottom gold sheet resistance is therefore approximately 1 Ω/sq, which matches the reported sheet resistance of gold [7].

We performed preliminary impedance measurements on a fabricated 2D CMUT element accessed from the backside of the wafer. The physical parameters of the element are summarized in Table I. The measurement result in Fig. 7 shows the functionality of the fabricated device. The open-

TABLE I
Physical parameters of the tested CMUT

Shape of the cell	Circular
Cell width, µm	77
Cell-to-cell distance, µm	5
Top metal thickness, µm	0.3
Silicon layer thickness in plate, µm	2
Insulating layer thickness in plate, µm	0.2
Gap height, µm	0.15
Bottom metal thickness, µm	0.15
Substrate thickness, µm	700
Number of cells per element	9
Length of an element, µm	243
Width of an element, µm	243
Element pitch, µm	250

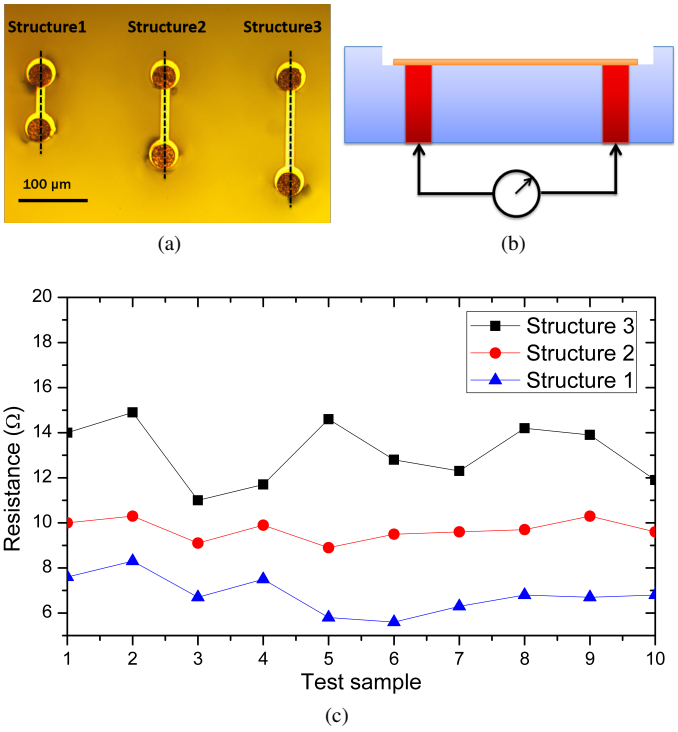


Fig. 6. (a) Via conductivity test structures. (b) Setup of the via conductivity test. (c) Resistance distribution for different test structures.

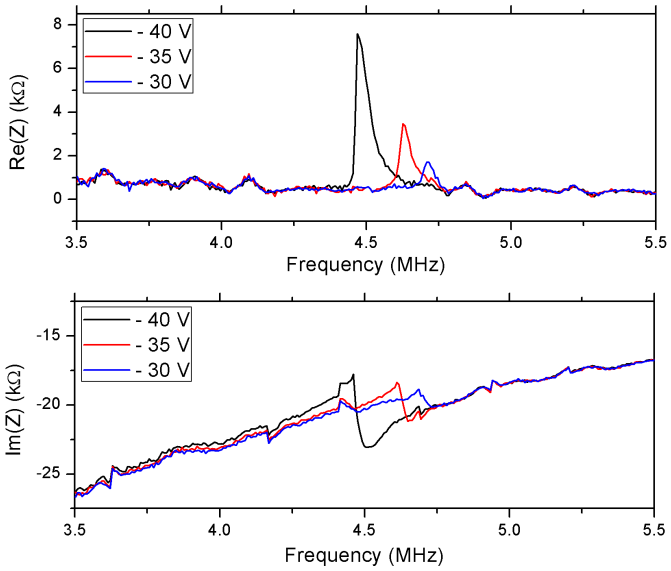


Fig. 7. Real and imaginary parts of the measured electrical input impedance for a 2D CMUT array element with 3 × 3 cells.

circuit resonant frequency of the CMUT element is 4.47 MHz at -40-V DC voltage. Spring softening effect is observed in the impedance measurement.

IV. Conclusion

We presented a simple CMUT fabrication process that integrates TGV interconnects and anodic bonding. The process eliminates the need for insulating lining for the vias or isolation trenches and is suitable for 2D CMUT array fabrication. The use of an insulating substrate and metal vias can reduce the parasitic capacitance and the series resistance of the CMUTs. The resistance of a single via is measured as 2 Ω. The initial impedance measurements demonstrate the basic functionality of the fabricated device.

Acknowledgment

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