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Design of High-Frequency Broadband CMUT Arrays

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***Abstract*—In this work we demonstrate a high-frequency (29-MHz) broadband (100% FBW) CMUT 1D array. The devices are fabricated using anodic bonding with only three photolithography steps. We also discuss the design guidelines for high-frequency broadband CMUTs using the simulations. A high fill factor and a thin plate are important for the broadband design. Small cell size is required for the increased center frequency. To improve the transducer sensitivity and to keep the collapse voltage low, the gap height should be small and a high-k dielectric insulation layer should be employed. The fabrication steps we report in this paper have good potential to meet the high-frequency broadband CMUT design requirements. So far we have demonstrated that we can define a 50-nm gap, bond to a post as narrow as 2 μm, and pattern a high-k dielectric layer on the bottom electrode.**

***Index Terms*—High frequency transducer array; Broadband; CMUT; Anodic bonding; Glass.**

I. Introduction

High-frequency (>20 MHz) ultrasound has been subject to extensive research in recent decades. In a broad range of applications in which deep penetration is not required, including dermatology, ophthalmology, intravascular imaging, and small animal studies, high-frequency ultrasound can meet the high-resolution requirement at a safe acoustic power level. The major technology hurdle for making high-frequency arrays is associated with the conventional piezoelectric transducer fabrication techniques [1], [2]. The thickness of the piezoelectric crystal and the pitch of the array typically need to be tens of microns which is difficult to achieve using conventional fabrication techniques, such as lapping, polishing, and dicing. Also, increased cross coupling could be observed between elements depending on how the kerfs are filled. Furthermore, achieving wide bandwidth is difficult in these arrays.

Capacitive micromachined ultrasonic transducer (CMUT) technology has demonstrated great promise for the implementation of high-frequency arrays [3]. The small device dimensions can be achieved by precisely controlled microlithography and thin-film technologies. Also, batch processing allows the reduction of the manufacturing cost. CMUTs for high-frequency applications have been investigated before [4], [5]. However, the fractional bandwidth (FBW) of the early high-frequency CMUT designs (30 MHz) was limited (<80%) mainly because of the low fill factors [5].

We have reported a three-mask process to fabricate CMUTs by anodic bonding [6]. Anodic bonding provides the possibility of bonding to a small area. In this work, we successfully demonstrated that we can fabricate high-frequency broadband CMUTs on a glass substrate using a similar fabrication process.

In the following section, we first report the design and fabrication of a high-frequency broadband 1D array. The immersion measurement results are presented in Section III. Section IV presents the guidelines for high-frequency broadband CMUT design.

II. Design and Fabrication

We designed, fabricated, and characterized a 256-element, 65-μm-pitch, 1D linear array. The cells are densely packed to achieve a relatively high fill factor (60%). The gap of the device is defined by buffered oxide etch (BOE) and metal deposition. A shallow gap is desired for high-frequency designs to reduce the collapse voltage and improve the efficiency. We choose the gap height to be 50 nm so that the silicon nitride breakdown voltage at the sealing location is higher than the device pull-in voltage.

The high-frequency CMUTs are fabricated in a similar way as the three-mask process we reported. The difference is that for this work we do not remove the PECVD silicon nitride on the device active area. Instead, the sealing silicon nitride serves as part of the vibrating plate as well as for surface passivation. The simplified process flow is shown in Fig. 1.

The fabrication starts with a 0.7-mm-thick, 100-mm-diameter borosilicate glass wafer. The cavities are patterned and then etched down to 210 nm in 10:1 BOE solution. Hard-bake and interval bake are performed to enhance the adhesion. Bottom electrodes are defined by e-beam evaporation and lift-off. To set the exact gap height, we performed test runs before depositing metal on the actual wafer. The AFM image in Fig. 2a shows the gap height is 50 nm before bonding. Anodic bonding is performed after depositing a 200-nm-thick layer of silicon nitride on the device layer of the SOI wafer as the insulation layer. After anodic bonding, the handle wafer is first ground down to 100 μm and then removed by TMAH solution. The BOX layer is removed by BOE solution. The bottom electrode pads are opened and then resealed by 600-nm conformal PECVD silicon nitride. We remove the sealing silicon nitride on the bottom pads and define a metal line in contact with the silicon plate for top electrode access. The silicon nitride on the active area is kept as part of the plate. The SEM image shown in Fig. 2b confirmed that we achieved

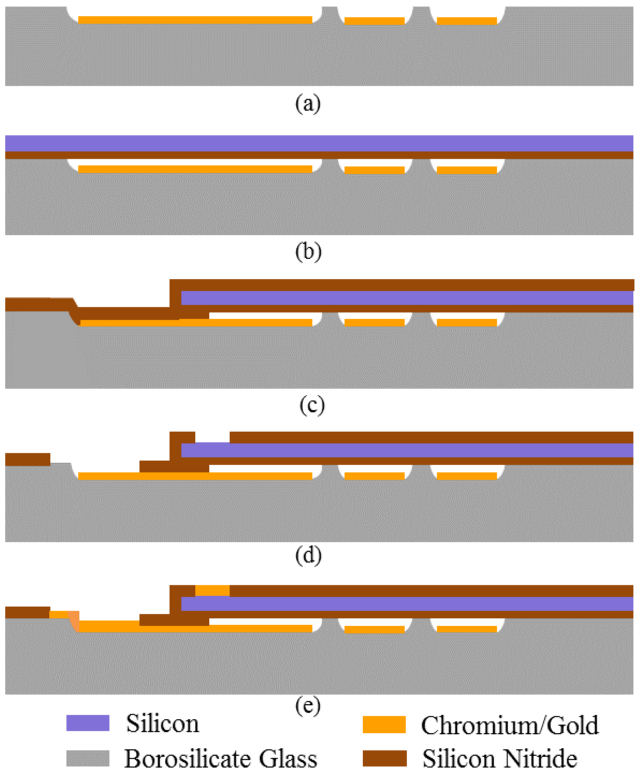
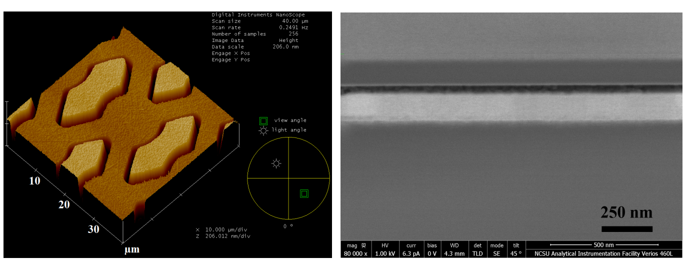


Fig. 1. Fabrication process flow: (a) Cavity and bottom electrode formation; (b) Handle and BOX layer removal after anodic bonding; (c) Pads opened and the cavities are sealed by PECVD silicon nitride; (d) Silicon nitride etch to expose the pads; (e) Metal deposition and lift-off.



(a) (b)

Fig. 2. (a) AFM image shows the gap height before bonding, and (b) SEM image shows the gap height of the fabricated CMUTs.

the 50-nm gap height for the final device. The fabricated 1D high-frequency CMUT array is shown in Fig. 3. Table. I shows the physical parameters of the final device.

III. Characterization

The immersion test was performed in a tank filled with vegetable oil. A 1D array was diced and wirebonded to a chip carrier. The frequency response of the element in transmit was measured using a hydrophone (Model HGL-0200, Onda Corporation, Sunnyvale, CA) at a distance of 1.8 mm. The element was biased at 50-V DC and excited using a pulser/receiver (Model 5073PR, Olympus Corporation,

TABLE I
Physical parameters of the fabricated CMUT 1-D array

Shape of the cell	Circular
Cell width, µm	21
Cell-to-cell distance, µm	5.5
Top silicon nitride thickness, µm	0.6
Silicon layer thickness in plate, µm	1.5
Insulating layer thickness in plate, µm	0.2
Gap height, µm	0.05
Bottom metal thickness, µm	0.16
Substrate thickness, µm	700
Number of cells per element	219
Length of an element, µm	1826
Width of an element, µm	58.3
Array pitch, µm	65

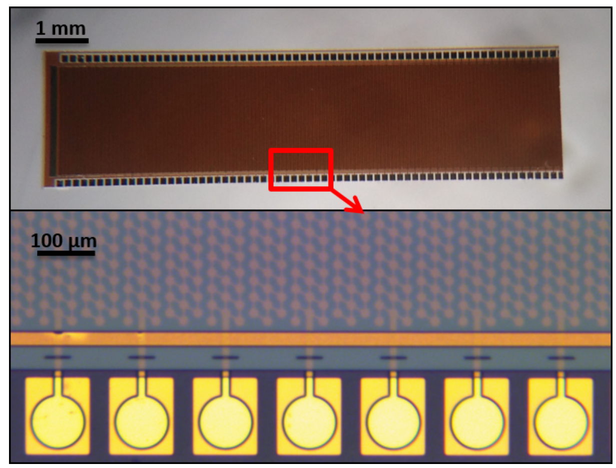


Fig. 3. Fabricated 1D high-frequency CMUT array

Waltham, MA. Pulse repetition frequency (PRF): 200 Hz; Energy level: 2; Damping level: 1).

The signal received by the hydrophone is shown in Fig. 4a in time domain. The corresponding frequency spectrum is shown in Fig. 4b. The frequency spectrum shows the transducer center frequency is 29 MHz and the 3-dB FBW is 100% after correcting for the pulse spectrum. The hydrophone calibration is available up to 40 MHz at the time. Therefore the spectrum is not corrected for the hydrophone response.

IV. Design Guidelines for High Frequency Broadband CMUTs

We have demonstrated a high-frequency broadband 1D CMUT array working at a center frequency of 30 MHz. In this section, we will analyze the design guidelines to extend this result to higher frequencies.

A. Plate dimensions

Different plate thickness and width combinations can be used to obtain the same frequency of operation. Fig. 5a shows the different designs all operating at the same center frequency. For the high-frequency broadband CMUT design, the cell size is required to be small to increase the center frequency. The plate thickness is required to be thin in order to reduce the stiffness, which will increase the bandwidth and reduce

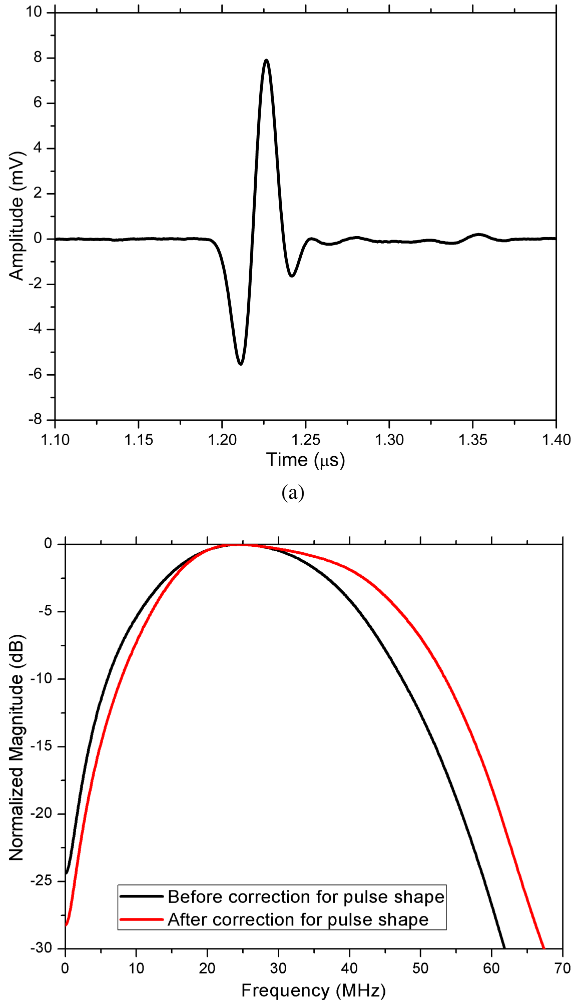


Fig. 4. (a) Experimental received signal by the hydrophone, and (b) Corresponding frequency spectrum

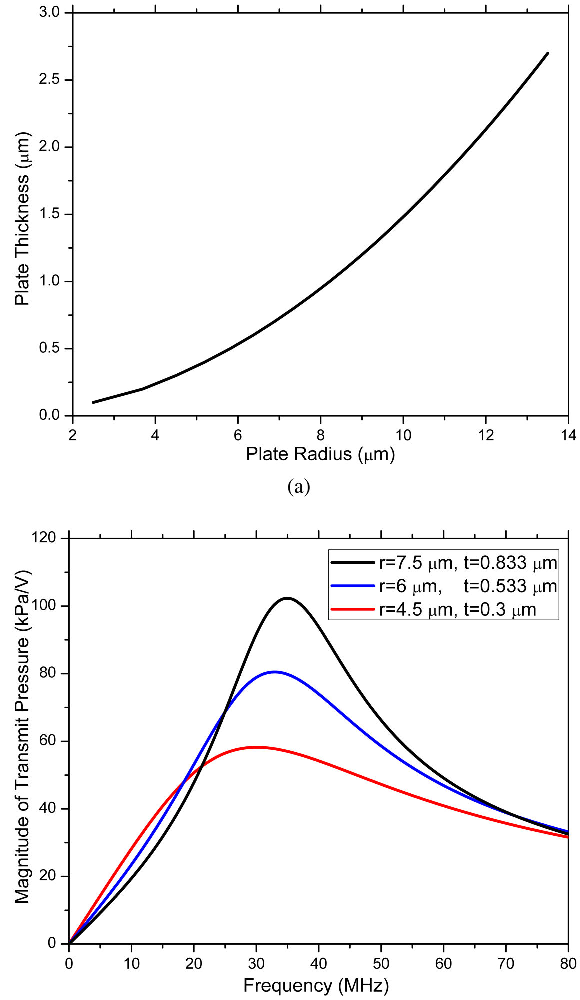


Fig. 5. (a) Simulation results of different combinations of plate thickness and radius to achieve the same mechanical resonant frequency; (b) Bandwidth is broadened with decreasing plate thickness.

the pull-in voltage. The output pressure of three different combinations are plotted in Fig. 5b when the bias voltage was 80% of the collapse voltage. The fill factor is fixed as 60% for each case. The similar simulation for the CMUTs operating at lower frequency was reported in [7].

B. Fill factor

Early demonstrations of high-frequency CMUTs were limited by the narrow fractional bandwidth compared to the desired wideband response (>100%). This is mainly because of the low fill factor [5]. When the fill factor is low, each individual cell push the fluid sideways as well as in the normal direction. As a result, the hydrodynamic mass of the fluid for each cell increases and therefore degrades the center frequency and bandwidth [5].

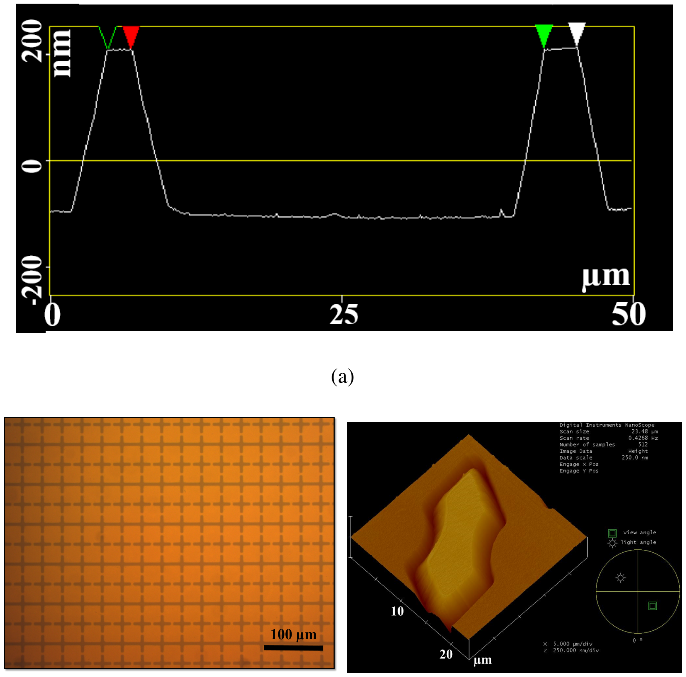
The early high-frequency CMUTs were fabricated using sacrificial release process that requires etch holes between the cells, which results in a low fill factor [5]. Use of fusion bonding yields a higher fill factor. Typically a 5-μm post width is used in the process. However, when the cell size decreases, the required bonding area becomes comparable to the active area. We have demonstrated that anodic bonding is successful with a post width as narrow as 2 μm. The AFM image in Fig. 6a shows the cross section of the 2-μm wide post before anodic bonding. The micrograph in Fig. 6b shows the bonded plate on the post. This process will significantly improve the fill factor even for small cell sizes and hence increase the bandwidth.

C. Thin gap

The gap height for the high-frequency CMUTs should be small to reduce the collapse voltage. For high-frequency CMUTs, the output pressure will not be limited by the available gap as 5-nm displacement can generate 2-MPa pressure at 40 MHz.

D. Insulation layer

The dielectric insulation layer is important for CMUT transmit and receive sensitivity and for the pull-in voltage [8].



(a)

(b) (c)

Fig. 6. (a) AFM cross-section showing the 2-μm post width (b) Optical image shows the bonded plate, and (c) AFM image shows the HfO_2 defined on the bottom metal suface.

For high-frequency CMUTs, the pull-in voltage can be reduced by using a high-k dielectric material as the insulation layer. Fig. 7 shows the electric field in the vacuum gap and in the insulation layer. By using high-k dielectric such as HfO_2 one can reduce the electric field in the insulation film and hence improve the device sensitivity. We have recently developed an atomic layer deposition (ALD) based process to form an HfO_2 layer on the top of bottom electrode. Fig. 6c shows the HfO_2 defined on the bottom electrode surface in the cavity.

V. Conclusion

We demonstrated a high-frequency broadband 1D CMUT array using only three photolithography steps in the fabrication. The fabricated CMUT was characterized in immersion. The CMUT shows 29-MHz center frequency and 100% FBW after correcting for pulse shape. We further discussed the important aspects of high-frequency broadband CMUT design. The simulation results show that a high-fill factor, and a thin plate are required to broaden the fractional bandwidth. A small cell is required to achieve a high center frequency. A shallow gap and a high-k dielectric material as an insulation layer enhance the transducer sensitivity and help reduce the operating voltage. We have demonstrated that we can bond to a post as narrow as 2 μm, which will significantly improve the fill factor. Also, we showed that the gap height can be well controlled to 50 nm using BOE etch and e-beam evaporation. We have successfully deposited and patterned the HfO_2 insulation layer on the bottom electrode. The thin plate can be implemented with a single crystal SOI device layer that can be thinner than what is achievable using sacrificial release process in general.

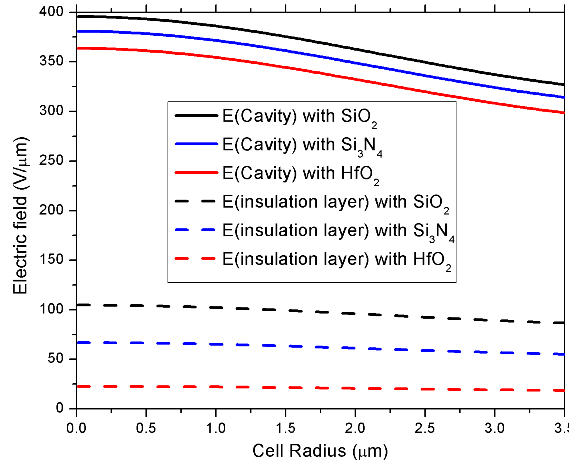


Fig. 7. Electric field in the vacuum gap and insulation layer implemented with different materials.

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