Trench-Isolated CMUT Arrays with a Supporting Frame: Characterization and Imaging Results

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***Abstract* – We report on the characterization and imaging results of trench-isolated CMUT arrays with a supporting frame. The CMUT arrays are built on a silicon-on-insulator (SOI) wafer using direct wafer-to-wafer fusion bonding technique. Electrical contacts to individual elements are brought to the back side of the wafer by highly conductive silicon pillars. Mechanical support for array elements is provided by a silicon frame structure. 1D and 2D arrays with 250-μm element pitch were fabricated and tested in air and in immersion. Rectangular membranes are used, which feature two distinctive pull-in (collapse) points in both air and immersion tests. The double collapsing membranes enable an operating frequency ranging from 1.9 MHz in conventional mode to 58 MHz in second collapse mode on the same device. After flip-chip bonding the 2D arrays to custom-designed integrated circuits (IC), volumetric imaging was demonstrated.**

***Key words* – CMUT; through-wafer trench-isolated interconnect; supporting frame; volumetric imaging**

I. INTRODUCTION

We recently reported on a through-wafer interconnect technique for CMUT arrays [1]. In this approach, the array elements are built on the device layer of an SOI wafer, and are separated from one another by trenches on both the device layer and the bulk silicon wafer. Mechanical support for the array elements are provided by a built-in frame structure in the bulk silicon. Electrical connections to the elements are made through the silicon pillars corralled by the supporting frame (Fig. 1).

The trench-isolated through-wafer interconnect with a supporting frame is compatible with both wafer-to-wafer direct fusion bonding and sacrificial layer releasing technologies for CMUT fabrication. Other advantages include low series resistance, parasitic capacitance and electrical crosstalk, and variable substrate thickness, as well as significantly simplified process flow when compared to the through-wafer via interconnect technique [1].

In this paper, we report on the air and immersion test results of the trench-isolated CMUTs with a supporting frame. We also demonstrate volumetric imaging results obtained from a 16-by-16 2D array with a 250-μm element pitch, flip-chip bonded to a custom-designed IC.

II. DESIGN AND FABRICATION

Trench isolated 1D and 2D CMUT arrays with mechanical supporting frames were fabricated using direct wafer-to- wafer fusion bonding technique. Details of the fabrication process can be found in [1]. The finished devices have highly conductive, single crystal silicon membranes. The 1D arrays have 38 elements, each 250 μm by 2.4 mm in size. The 2D arrays have 16x16 elements with a 250-μm pitch. In both arrays, 40-μm wide rectangular membranes are used. These arrays are designed to operate at a center frequency of 5 MHz in immersion (conventional mode). The supporting frames and isolation trenches are both 40 μm wide. The substrate thickness ranges from 200 μm to 400 μm. In this paper, we report on characterization results based on devices with 300-μm-thick substrates. The key device parameters are summarized in Table I.

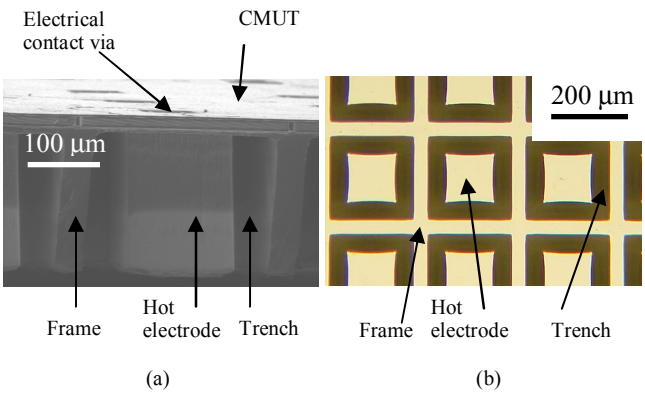

Figure 1: (a) SEM photograph (cross-section) of trench isolation with a supporting frame, and (b) photograph of the back side electrodes and the supporting frame.

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TABLE I: DEVICE PARAMETERS FOR TRENCH-ISOLATED CMUT ARRAYS WITH A SUPPORTING FRAME.

Membrane width (μm)	40
Membrane length, 2D element (μm)	133
Membrane length, 1D element (μm)	220
Number of membranes / 2D element	8
Number of membranes / 1D element	48
Element pitch (μm)	250
Membrane thickness (μm)	1. 4
Cavity height (μm)	0.15
SiO_2 insulation thickness (μm)	0.3
Substrate thickness (μm)	300
Device layer thickness (μm)	10
BOX layer thickness (μm)	2
Trench width (μm)	40
Frame width (μm)	40
Silicon wafer resistivity (Ω-cm)	< 0.025

III. CHARACTERIZATION RESULTS AND DISCUSSION

The following measurements for air operation were performed: electrical input impedance of the CMUT elements, series resistance of the through-wafer interconnects, parasitic capacitance of the frame structure, electrical crosstalk between the array elements, and membrane static deflection as a function of the DC bias voltage.

Electrical input impedance in air was measured by probing (Model ACP40-W-GS-150, Cascade Microtech, Inc., Beaverton, OR) the signal electrodes on the back side of the wafer using a network analyzer (Model 8751, Hewlett-Packard Company, Palo Alto, CA). The network analyzer was calibrated with the measurement probe. Across a 256-element 2D array, a uniform open-circuit resonant frequency was observed (Fig. 2).

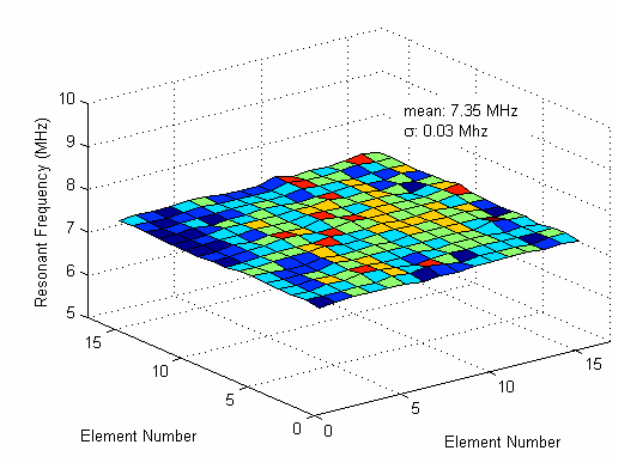


Figure 2: Open circuit resonant frequency distribution in air at 30 Vdc.

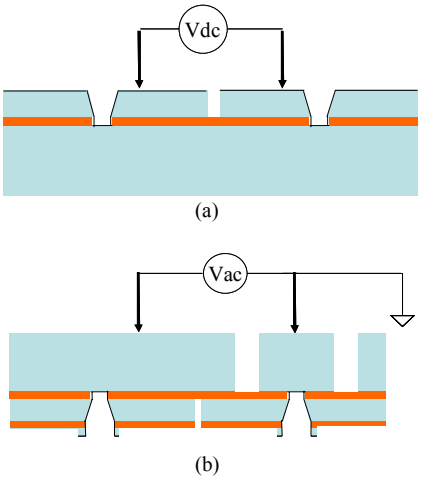


Figure 3: Schematics illustrating the series resistance measurement setup (a), and the parasitic capacitance measurement setup (b).

The series resistance of the contact vias was measured using a semiconductor parameter analyzer (Model 4145B Hewlett-Packard Company, Palo Alto, CA) [Fig. 3(a)]. The resistance was measured to be 7 Ω. The parasitic capacitance due to the supporting frame was measured using a network analyzer (Model 8751, Hewlett-Packard Company, Palo Alto, CA) [Fig. 3(b)]. A small parasitic capacitance of 0.22 pF was measured, close to the predicted value of 0.19 pF. Compared to the device capacitance of about 2 pF, the parasitic capacitance is insignificant.

The electrical crosstalk was measured by exciting an array element with a 10-V, 30-ns pulse, and detecting the instantaneously received signal from neighboring elements. Careful electrical shielding was provided between the excitation and receiving electrical traces to suppress external crosstalk. The received signal was 65 dB down compared with the excitation signal. This low electrical crosstalk is a result of the inherent electrical shielding provided by the silicon supporting frame that is embedded between the electrodes.

An interesting double collapse phenomenon is observed on the devices [2]. The electrical input impedance measurements in air show a resonant frequency of about 7.5 MHz in conventional operation. Upon the collapse of the membrane to the bottom of the cavity, the resonant frequency abruptly shifts to 30 MHz. Upon further increase of the bias voltage, a second abrupt jump of the resonant frequency to around 55 MHz is observed. The imaginary part of the electrical input impedance of a 2D array element was used to calculate the CMUT capacitance. The calculation was performed at 100 MHz so that it is far away from the acoustic resonant frequencies at all bias conditions. The device capacitance is about 2.6 pF in the conventional mode, 3.5 pF in the first collapse mode, and 3.9 pF in the second collapse mode (Fig. 4).

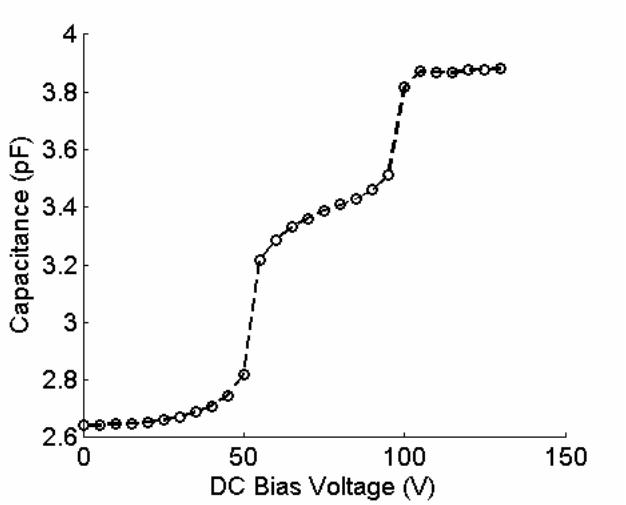


Figure 4: Device capacitance of a 2D array element as a function of DC bias voltage. Two abrupt increases in device capacitance can be clearly seen.

The double collapse phenomenon is confirmed by measuring the static displacement of the CMUT membranes using a white light interferometer (Model NewView 200, Zygo Corporation, Middlefield, CT) at various DC bias voltages. Two distinctive membrane pull-in points are observed at the first collapse voltage (~50 V) and second collapse voltage (~100 V), respectively. Before first collapse, the membrane deflects less than the vacuum gap height of 0.15 µm. In the first collapse mode, the membrane contacts the insulation layer at the bottom of the vacuum cavity. Throughout the first collapse mode, the contact area progressively increases in the long direction with increasing DC bias, but remains largely unchanged in the short direction. When the bias voltage is increased past the second collapse voltage, the contact area in the short direction substantially increases in an abrupt fashion, indicating a second collapse. The schematics shown in Fig. 5 illustrate the size of the contact area for each bias condition.

A 1D array element was used to perform hydrophone and pulse-echo measurements in vegetable oil. A hydrophone (Model HNV-0400, Onda Corporation, Sunnyvale, CA) was used to measure the output spectrum for the device operating in conventional mode. This is because in the pulse-echo measurements, we did not use an amplifier, and thus pulse-echo measurements in the conventional mode were not possible on the device we measured. The transmitted signal from the CMUT as measured by the hydrophone has a center frequency of 3.5 MHz with a 90% bandwidth at 52 V (Fig. 5). In both the first and second collapse mode, pulse-echo measurements were successfully performed using the oil-air interface as the plane reflector. At a bias voltage of 90 V (first collapse mode), the center frequency is 21.6 MHz, with a 6-dB fractional bandwidth of 100%. At 150 V (second collapse mode), the center frequency increases to 33 MHz, with the 6-dB higher cut-off at 58 MHz, and the lower cut-off at 8 MHz. Thus, in the second collapse mode the device provides a wide fractional bandwidth of 150% (Fig. 6).

Existing analytical and finite element analysis models can accurately predict the first collapse behavior for CMUTs possessing different kind of membrane shapes (e.g., circular shapes or rectangular shapes) [3, 4]. However, the second collapse behavior observed in these electrical, acoustical and optical experiments can not be adequately explained by the existing models. Further modeling is needed to explain the mechanism behind the double collapse behavior. In particular, investigations need to be carried out to understand whether it is related to the rectangular membrane geometry. These studies are required to understand the potential tradeoffs in device performance.

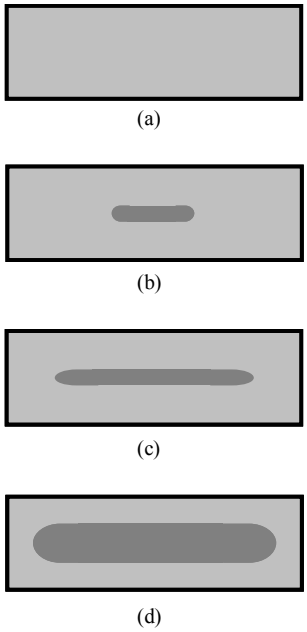


Figure 5: Schematics, derived from membrane static deflection measurements, illustrating contact area under different DC bias conditions: (a) conventional mode, (b) first collapse mode, (c) right before second collapse, and (d) second collapse mode.

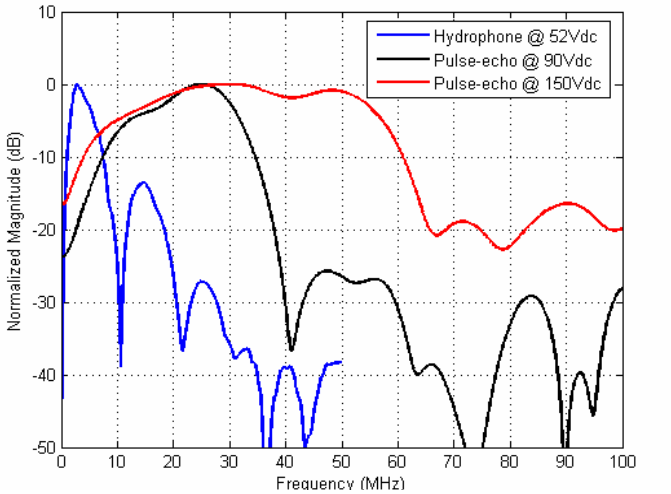
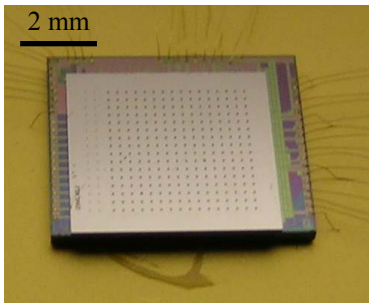
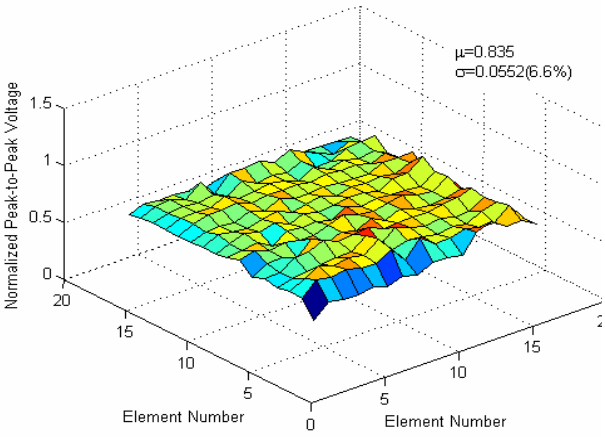


Figure 6: Spectra of a 1D array element measured at three operation modes.

A 2D array was flip-chip bonded to a custom-designed IC [Fig. 7(a)]. Details of the IC design and beamforming algorithm are explained in [5]. For flip-chip bonding, eutectic Sn/Pb solder balls were first jetted onto the bond pads on the IC chip. The CMUT and IC were then aligned in a flip-chip bonder. The flip-chip assembly was then placed in an inert atmosphere furnace for solder reflow. After flip-chip bonding, all 256 elements in a 2D array are tested to be functional [Fig. 7(b)]. 3D imaging of wire phantoms is demonstrated [Fig. 8].



(a)

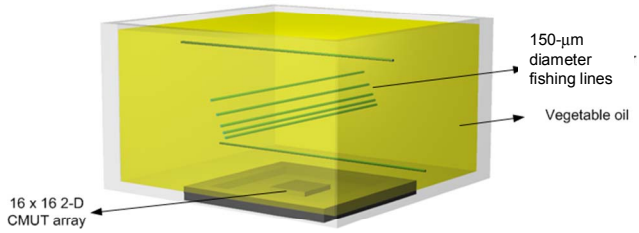


(b)

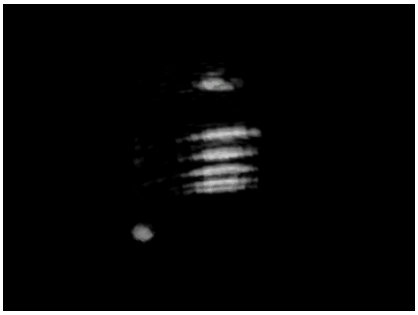
Figure 7: (a) Photograph of a trench-isolated 2D CMUT array with a supporting frame flip-chip bonded to an IC. (b) Variation, across the array, of pulse-echo amplitude from a plane reflector. All array elements are tested to be functional.

IV. CONCLUSION

Through-wafer trench isolation with a supporting frame enables fabrication of CMUT arrays with through-wafer interconnects by direct wafer-to-wafer fusion bonding. CMUT arrays fabricated using this technology are characterized in air and in immersion. Low series resistance, parasitic capacitance and element-to-element electrical crosstalk can be achieved using this interconnect scheme. The CMUTs fabricated in this study show a double collapsing behavior. Further study is needed to guide future designs to take advantage of this phenomenon. Volumetric imaging using a trench-isolated 2D CMUT array with a supporting frame flip-chip bonded to a custom IC is demonstrated.



(a)



(b)

Figure 8: (a) Illustration of the wire phantom used for the imaging experiment. The minimum separation between the wires is 0.8 mm. (b) 3D rendered imaging of the wire phantom.

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