Zero-Bias Resonant Sensor with an Oxide-Nitride Layer as Charge Trap

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Abstract — **We report on a capacitive resonant sensor with an oxide-nitride (ON) layer used as charge trap. The main idea is that we intentionally inject charges into the ON layer by biasing the device for 30 s with 160% of the pull-in voltage. We use a capacitive micromachined ultrasonic transducer (CMUT) to demonstrate this idea. The CMUT is fabricated via high temperature assisted direct wafer bonding after a local oxidation of silicon (LOCOS) to form evacuated cavities (vacuum gaps), and, thus, the device inherently has the ON layer beneath single-crystal silicon plates and vacuum gaps. Therefore, this device is ideal for this work. It allows us to test an elegant charge injection mechanism. By simply pulling in the plate a high electric field strength (~ 8.9 MV/cm) is created in the ON layer for a designated time, which results in charge injection. These charges stay trapped in the ON layer and create an intrinsic electric field in the vacuum gaps, which would otherwise require an external dc bias voltage of 44% of the pull-in voltage. We successfully implemented a 5.3-MHz oscillator with this zero-bias resonator and achieved excellent noise performance of 0.06 Hz of Allan deviation.**

I. Introduction

Dielectric charging is typically an unwanted phenomenon in MEMS devices, because it is known to degrade the stability and the reliability [1]. These unwanted charging effects come into play, when the dielectric layer is located between two electrodes and traps charges. On the other hand, there are controllable charging methods actively investigated. One example is Corona injection method [2], in which the ions are injected into the dielectric layer during the fabrication step. There are also post-fabrication charging methods such as the contact charging [3]. Charges are transferred when a charged material comes into direct contact with the dielectric layer. The conductive structure with a high electric potential contacts the dielectric film, and then it transfers the charges on to the film.

Capacitive micromachined ultrasonic transducers (CMUTs) were originally developed for airborne ultrasound applications [4] and later for medical imaging applications, that is, in immersion. Recently, they have been investigated for chemical sensor applications [5]. Typical CMUTs have a dielectric film in the gap, *i.e.* between the moving plate and the substrate. The dielectric film is typically 100-nm to 3-μm thermal oxide in the conventional CMUT fabrication process. In a recent fabrication process development, we utilized the local oxidation of silicon (LOCOS) with high temperature assisted direct wafer bonding [6]. In this process an oxide-nitride layer (ON layer) has a dual functionality. First, it is used as a LOCOS mask during the fabrication, and, second, it remains inside the bottom of the vacuum gaps as an electrical insulation layer.

An ON layer is typically known for its ability to trapped electrical charges. In case one manages to store the electrical charges into the ON layer in a well-defined and reproducible way, the requirement for an external *dc* bias voltage can be eliminated. Most of the time, the charge layer build-up in the insulation layer of an electrostatic device is considered parasitic. This is because the electrical charges reduce the electric field strength in the vacuum gap, *i.e.* they counteract the electric field induced by the external *dc* bias. As a result, the performance of the charged device is lowered and in worst case the likelihood of an intrinsic electric breakdown is increased due to charging. In this work, we demonstrate a technique of how we manage to get the electrical charges into the ON layer. We show that this can be done in a well-controlled manner for CMUTs, because they inherently allow increasing the electric field strength in the ON layer significantly by simply applying a *dc* bias voltage larger than the pull-in voltage. Then, the injected and trapped charges generate an intrinsic electric field inside the vacuum gap, large enough to *dc* bias the device without an external *dc* voltage source connected to it.

II. Characterization of the Charged Device

A. Device description and charge injection due to pull-in

The CMUT used for this work consists of 169 circular cells, all electrically connected in parallel (Fig. 1). Each cell consists of a single crystal silicon plate, attached to the pre-patterned (by LOCOS, [6]) thermally grown silicon dioxide by high temperature assisted direct wafer bonding (Fig. 2). The silicon plate acts as the moving part and is actuated by electrostatic force, *i.e.* by applying a potential difference between the plate and the substrate. The radii of the cells are

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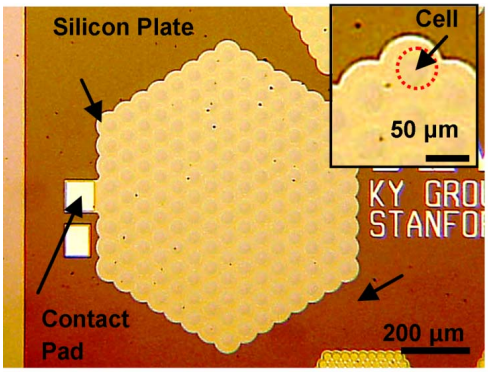

Figure 1. Photograph of the CMUT consisting of 169 cells, electrically connected in parallel. The vacuum cavities under the 500-nm-thick silicon plates are visible.

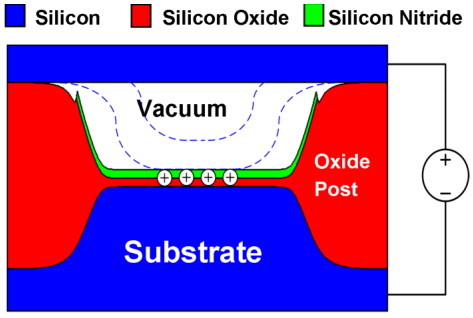

Figure 2. Cross-sectional schematic of one cell (not in scale). The thick oxide post layer ensures increased reliability with low parasitic capacitance during regular operation with external bias voltage, as well as during charge injection cycle. Blue dashed lines represent the plate during charging injection cycle.

25 µm and the thickness of the electrically conductive silicon plate is 500 nm. The cavity is vacuum-sealed to avoid squeeze film damping effects and to minimize the internal loss mechanism with the goal of large quality factor (good noise performance). As explained before, the unique structure of this CMUT is the result from the LOCOS-based fabrication process. Because in this process [6] we intentionally leave the LOCOS mask inside the vacuum gaps, there is a thin layer (55 nm) of stoichiometric silicon nitride on top of a thin (35 nm) silicon dioxide layer. Therefore, this ON layer not only is used during the fabrication for LOCOS, it also is an essential part of the final device in terms of functionality and reliability. It prevents from stiction and electrical shortage when the conductive silicon plate contacts the conductive bottom substrate. Contact can happen due to a large swing during operation, *dc* bias voltages beyond the pull-in voltage, or other reasons such as an increased ambient pressure.

In addition, we can use the ON layer as a charge trap, when the plate contacts the dielectric layer due to a *dc* bias voltage larger than the pull-in voltage. The *dc* bias voltage, in addition to the ambient pressure, deflects the plate downwards due to the electrostatic and mechanical force, respectively. In

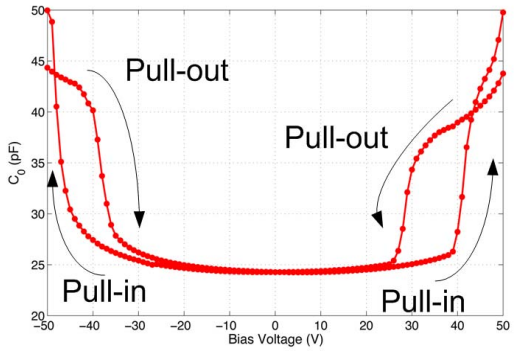

Figure 3. Exemplary C-V plot of a typical CMUT.

case the *dc* voltage is larger than the pull-in voltage, the equilibrium between the electrostatic and mechanical restoring force is not present anymore and the plate rapidly moves down to the ON layer, as indicated in Fig. 2 (dashed line). In a simplified parallel-plate-spring model [7], this pull-in takes place when the plate deflection is 1/3 of the effective gap height (effective distance between the plate and the substrate including the effect of the insulation layer). Because the applied *dc* bias voltage stays applied to the device after the pull-in event, the plate is in intimate contact with the ON layer and the electric field strength inside the ON layer is drastically increased. This large electric field (~ **8.9 MV/cm**) results in an injection of charges into the ON layer. After reducing the *dc* bias voltage, the silicon plate pulls-out and the charges remain in the ON layer, and, thus, create an electric field that penetrates the vacuum gap.

B. Characterization of charging

The amount of charging can be characterized by capacitance-voltage measurements (C-V curves). The electrical impedance of the CMUT is measured by an impedance analyzer (Model 4294A, Agilent Technologies, Palo Alto, CA) at various *dc* bias voltages. Based on these measurements, a total device capacitance, C_0, is calculated from the low-frequency and high-frequency impedance values, *i.e.* away from the resonance of the device. Fig. 3 shows the typical C-V plot of a CMUT. In the range of the *dc* bias voltage less than the pull-in voltage, the C-V curve shows a parabolic shape for both polarities. The parabolic shape is caused by the gradual increase of static deflection of the plate as a function of the *dc* bias voltage. At the pull-in point, a sudden increase in capacitance C_0 occurs, which is an evidence of contact between silicon plate and ON layer. However, due to cell-to-cell non-uniformity not all plates pull in at the exact same *dc* bias voltage. Thus, only a limited slope around an average pull-in voltage can be observed. Even after all silicon plates are in contact with the ON layer, the capacitance continues to increase, although with a reduced slope. This is due to the increase of the contact area between the silicon plate and the ON layer.

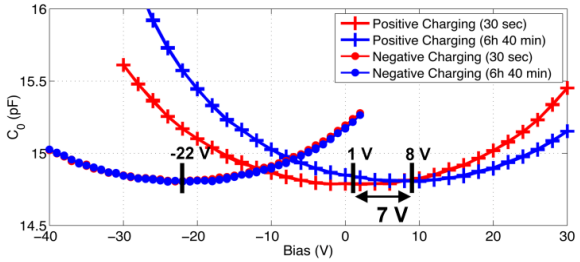

Figure 4. C-V measurement without pull-in cycle before and after the charging. The point of symmetry of each parabolic curve corresponds to the amount of built-in bias due to the charging in the insulation layers.

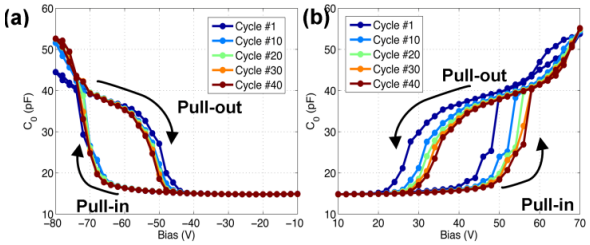

Figure 5. C-V measurement for complete pull-in/pull-out cycles with (a) negative and (b) positive bias voltages. Before the measurement, a 30-s pre-charging is applied by external bias voltages of (a) -80 V and (b) 70 V.

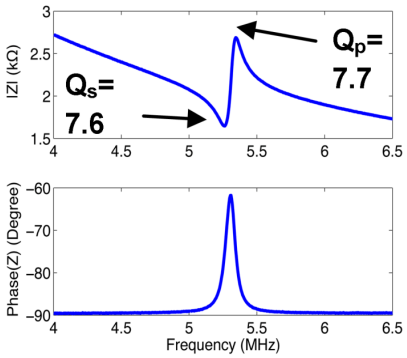

Figure 6. Measured input impedance characteristic of the zero-bias resonator after charge injection cycle, *i.e.* without external bias voltage. Quality factors, Q_p and Q_s are calculated based on the magnitude of impedance and admittance, respectively.

There are two methods to quantify the amount of charges injected into the ON layer from the C-V plot. First, after the silicon plate was pulled-in and charges were injected, one can expect a shift of pull-in voltage, which can be used as a measure of injected charges inside the ON layer. Due to the simple detection of the pull-in point in a C-V plot, this is commonly used to characterize the charging of a single capacitive device, such as a MEMS switch. Second, in a similar way one can look at the symmetry line of the parabolic region of the C-V plot, because after the charge injection this line will be shifted to the right or left, depending on the polarity of the applied *dc* bias voltage during the charge injection step. The advantage of this second approach is that the device only needs to be pulled-in during the actual charge injection step, which ensures that the amount of injected charges is not altered. Thus, for this work we used this second approach to quantify the amount of injected charges in the ON layer.

C. Charging results

The amount of charging is characterized for both positive and negative *dc* bias voltages (Fig. 4). First, a positive 70-V pull-in bias voltage is applied to the device for 30 s (pre-charging). Then the C-V curve is obtained by sweeping the voltage from only -30 V to 30 V so that pull-in point is not reached. Afterwards, the same pull-in bias voltage is applied again for 6 hours 40 min (long-term-charging) to reach an equilibrium condition. For the negative bias voltage, the pull-in bias voltage is -80 V and the C-V characterization is performed for a *dc* bias voltage ranging from -40 V to 2 V.

Charge injection due to the positive and negative bias voltage is different in terms of both the amount and the time constant (Fig. 4). With the negative bias voltages, the amount of injected charges is equivalent to -22 V external *dc* bias voltage and this amount of charge injection happens during the first 30 s of the pull-in condition. On the other hand, the charge injection with positive bias is observed to be significantly slower and the additional charging during 6 hours 40 min is only equivalent to 7 V external *dc* bias voltage. Therefore, the device features a large asymmetry in terms of pull-in induced charge injection.

The larger time constant of charging with a positive bias voltage can be well observed in the C-V measurement during the long-term-charging step. During this long-term-charging, the C-V curves were obtained every 10 min (Fig. 5). With the negative bias voltage, the pull-in voltage does not change during this time period (left graph in Fig. 5), *i.e.* the charge injection happens during the first 30-s pre-charging. On the contrary, the pull-in voltage continues to increase with the positive bias voltage during this time period (right graph in Fig. 5).

The amount of the trapped charges inside the ON layer can be calculated from the C-V plot and the device dimensions. The amount of charges trapped with negative bias voltage is equivalent to an external *dc* bias voltage of -22 V. This equivalent bias voltage can be converted to the average trapped charge of 9.8 x 10^{-8} C/cm^2, which generates an intrinsic electric field strength of ~0.55 MV/cm inside the vacuum gap.

In order to utilize this intrinsic electric field as a *dc* bias, it is crucial that the trapped charge has a good temporal stability, *i.e.* remain trapped inside the ON layer for as long as possible. Thus, in this work, we focus on the charges injected via a negative *dc* bias voltage. After performing the charge injection as described (equivalent *dc* bias voltage of -22V), the device was monitored for full 7 days at room temperature. During this 7-day measurement, we did not observe any charge degradation inside the ON layer. At an elevated temperature (160°C), however, we observed a decrease of 8.7% of trapped charges during a time period of ~17 hours.

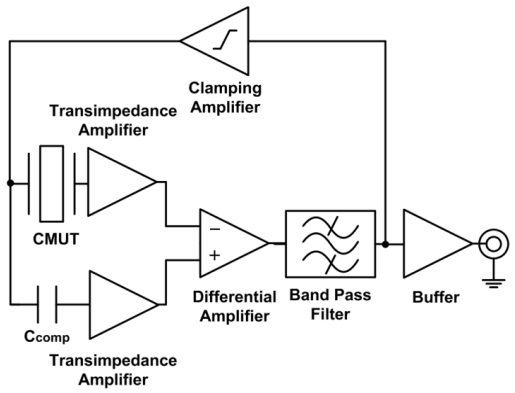

Figure 7. Circuit diagram of oscillator circuit. C_{comp} is selected to be same as device capacitance (C_0). The topology of this circuit is based on a Pierce oscillator. An additional transimpedance amplifier with C_{comp} and a differential amplifier effectively compensate the effect of parasitic capacitance of the CMUT.

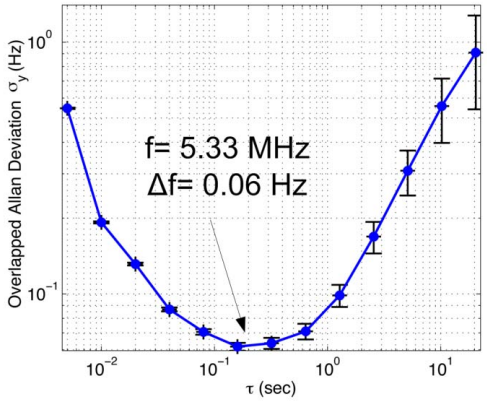

Figure 8. Overlapped Allan deviation calculated from the frequency counter with a gate time of 5 ms. The error bars indicate the 1-sigma confidence level.

III. Application of the Charged Device

In order to demonstrate the advantage and the applicability of the CMUT after charge injection, we developed an oscillator circuit, which utilizes the charged CMUT as the frequency selective device. The charge injected via the negative *dc* bias voltage is equivalent to a bias voltage of -22 V, which is equivalent to 44% of the pull-in voltage (before charge injection). This intrinsic electric field is sufficient to *dc* bias the device, and, thus, to detect a pronounced series and parallel resonance in the electrical impedance measurement result, as shown in Fig. 6. In addition, this measured impedance (Z) is identical to the impedance of the same device before charge injection, *i.e.* without trapped charges in the ON layer, and biased with an external *dc* bias voltage of -22 V.

Based on this charged device, we design the oscillator circuit to track the resonant frequency without any external *dc* bias voltage (Fig. 7). The working principle of the circuit is similar to the circuit for MEMS resonators. The device is connected to a transimpedance amplifier, which forms a closed-loop together with a band-pass filter and a clamping amplifier. The loop gain is maximum at the series resonance (*i.e.* where the |Z| becomes minimum), and, thus, the frequency of the output signal follows the series resonant frequency of the CMUT.

In addition to the basic closed-loop system, we add parasitic capacitance cancellation path. Due to the unwanted parasitic capacitance, the measured quality factor of the device (Fig. 6) is 7.6. In order to remove this parasitic loading effect, we populate an additional transimpedance amplifier, connected to a static compensation capacitance (C_{comp}), in parallel to the transimpedance amplifier connected to the charged CMUT. In case the frequency of the signal is far from the resonant frequency of the CMUT, the gain of two transimpedance amplifiers are identical and those signals are cancelled out in a differential amplifier. As a result, only the signal from the resonance of the device is amplified in a differential amplifier. By utilizing this capacitance cancellation technique, the quality factor of the resonance inside the loop gain is improved by a factor of 10.

To evaluate this CMUT-based oscillator, the short-term frequency stability is characterized in time domain based on Allan deviation measurements. The output signal from this zero-bias oscillator is measured by a frequency counter (Stanford Research System, Model SRS620, Sunnyvale, CA) with a gate time of 5 ms. Allan deviation from this measurement (Fig. 7) shows an excellent short-term frequency stability of 0.06 Hz ($\sigma_y = 1.1 \times 10^{-8}$).

IV. Discussion

The elegance of this charge injection method is its reversibility. If the ON layer is charged with a negative bias voltage, the trapped charges can later be removed by another pull-in at a positive bias voltage and vice versa. Thus, this method opens the possibility of tuning the amount of the trapped charges inside the ON layer to adjust the intrinsic bias voltage for an optimal operation point. In addition, our results show a strong asymmetric behavior based on the polarity of the applied *dc* bias voltage. These results require a future work to clarify the charging mechanism of the ON layer.

We also demonstrated the capacitance cancellation method in the CMUT oscillator circuit for the first time. Although this method requires additional amplifiers, this technique is essential for devices that have a significant degradation of quality factor due to the parasitic capacitance. By removing the effect of the parasitic capacitance, the in-circuit quality factor without bias voltage is 75, which is close to the mechanical quality factor of the resonator (80~90). In general, this method will increase the device design flexibility, in which there is a trade-off between the parasitic capacitance and the fabrication feasibility.

The benefit of the intrinsic bias voltage is a simplification of the circuit. In order to supply an external bias voltage, it requires more components, which introduce an additional

noise, parasitic capacitance as well as circuit complexity. However, the amount of the intrinsic bias voltage in our work is not enough to operate the device without the additional circuit components, *i.e.* the capacitance cancellation circuit. It is due to the larger parasitic capacitance of the prototype, which can be reduced with a design modification.

V. CONCLUSION

We presented a zero-bias resonator based on the CMUT with an excellent stability. With a charge injection into the embedded ON layer by pull-in, we presented the CMUT with an intrinsic bias voltage of 44% of the pull-in voltage. This charge injection mechanism is reversible by applying *dc* bias voltage with opposite polarity. Additionally, the trapped charges are stable for 7 days in room temperature. Based on the charged device, we presented a CMUT-based resonant system without and external *dc* bias voltage. This low-quality-factor resonator system shows a good short-term frequency stability of 0.06 Hz (σ_y = 1.1x10^{-8}). This charging method opens the possibility of MEMS-based resonator systems without external bias voltage for various applications including mass-loading sensing applications. To expand the possibility, a future work of the contact charging of the ON layer should address the charging mechanism as well as new techniques to maximize the intrinsic bias voltage.

REFERENCES

[1] S. Melle, D. De Conto, D. Dubuc, K. Grenier, O. Vendier, J. Muraro, J. Cazaux, and R. Plana, "Reliability modeling of capacitive RF MEMS," *IEEE Trans. Microwave Theory and Techniques,* vol. 53, pp. 3482-3488, 2005.

[2] Gunther, "Mechanism of charge storage in electron-beam or corona-charged silicon-dioxide electrets," *IEEE Trans. Electrical Insulation,* vol. 26, pp. 42-48, 1991.

[3] W. Greason, "Analysis of charge injection processes including ESD in MEMS*," J. Electrostatics*, vol. 66, pp. 602-608, 2008.

[4] I. Ladabaum, X. Jin, H. Soh, A. Atalar, and B. Khuri-Yakub, "Surface micromachined capacitive ultrasonic transducers," *IEEE Tran. Ultrasonics, Ferroelectrics and Frequency Control,* vol. 45, pp. 678-690, 1998.

[5] K.K. Park, H.J. Lee, M. Kupnik, O. Oralkan, and B.T. Khuri-Yakub, "Capacitive micromachined ultrasonic transducer as a chemical sensor," *2008 IEEE Sensors Conference*, pp. 5-8, 2008.

[6] K.K. Park, H.J. Lee, M. Kupnik, O. Oralkan, and B.T. Khuri-Yakub, "Fabricating capacitive micromachined ultrasonic transducers with direct wafer-bonding and LOCOS technology," 2008 *IEEE 21st International Conference on Micro Electro Mechanical Systems*, pp. 339-342, 2008.

[7] A.S. Ergun, G.G. Yaralioglu, and B.T. Khuri-Yakub, "Capacitive Micromachined Ultrasonic Transducers: Theory and Technology*," J. Aerospace Engineering*, vol. 16, pp. 76-84, 2003.