Trench-Isolated CMUT Arrays with a Supporting Frame

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***Abstract* – We present a trench-isolated CMUT process with a supporting mesh frame for a fully populated 2D array. In this process, the CMUT array is built on a silicon-on-insulator (SOI) wafer. Electrical interconnections to array elements are provided through the highly conductive silicon substrate. Neighboring array elements are separated from one another by trenches on both the device layer and the bulk silicon. A mechanically supporting frame is designed as a mesh structure between the silicon pillars providing electrical connections to the individual elements. Like the frameless trench isolation process, the framed trench isolation is compatible with both wafer-bonded and surface-micromachined CMUTs. In addition, this process eliminates the need for attaching the device wafer to a carrier wafer for the required mechanical support during the deep trench etching and flip-chip bonding steps, which presents difficulties during the release of the carrier wafer.**

***Key words* – CMUT; through-wafer trench-isolated interconnect; supporting frame**

I. INTRODUCTION

In large, fully populated 2D transducer arrays, providing connection to each array element is a challenge. In the case of 2D CMUT arrays, researchers have reported on interconnect techniques both based on through-wafer vias and through-wafer trench isolation. In the through-wafer via implementation, a conductive material, usually doped polysilicon, is used to fill the vias and serves as the conductor between the front and back sides of the array elements [1]. It was found that after the deposition of the polysilicon, performing wafer-to-wafer fusion bonding is difficult [2]. Therefore, the through-wafer via approach is limited to only surface micromachining CMUT processes. The through-wafer trench-isolation process is compatible with both the surface micromachining and the wafer-to-wafer fusion bonding techniques [3, 4]. This is because the isolation trenches are formed after the CMUT membranes have been fabricated on the front side of the wafer. In our previously reported trench isolation process, a carrier wafer is required during the deep reactive ion etching (DRIE) and the flip-chip bonding steps to provide the mechanical support for the membranes. This particular requirement presents certain drawbacks in processing. Good adhesion between the carrier wafer and the membrane surface is required for adequate mechanical support for the membranes. However, it is difficult to separate the carrier wafer and the membrane after the flip-chip bonding. The adhesive material may also swell in the solvent, creating stress that can break the CMUT membranes. It is highly desired to eliminate the need of the carrier wafer for the trench isolation process. Using a supporting frame with the trench-isolated CMUT arrays preserves the advantages of the frameless trench isolation process, such as the compatibility with both wafer-bonding and surface micromachining processes, and eliminates the need of a carrier wafer. It is therefore an important enabling technology for the advancement of 2D CMUT arrays.

This paper explains the design concept, process details as well as test results of the trench-isolated CMUT arrays with a supporting frame.

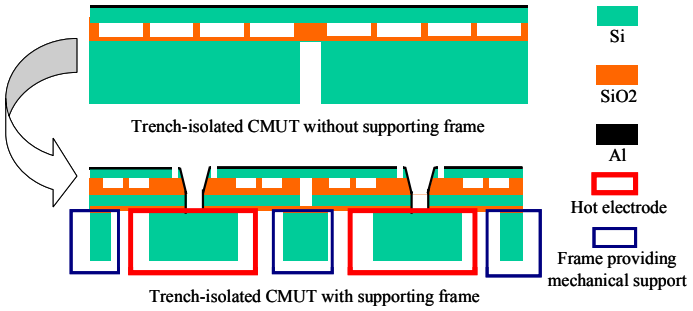

Figure 1: Cross sectional cartoons of a frameless trench-isolated CMUT array (top) and a trench-isolated CMUT array with a supporting frame (bottom).

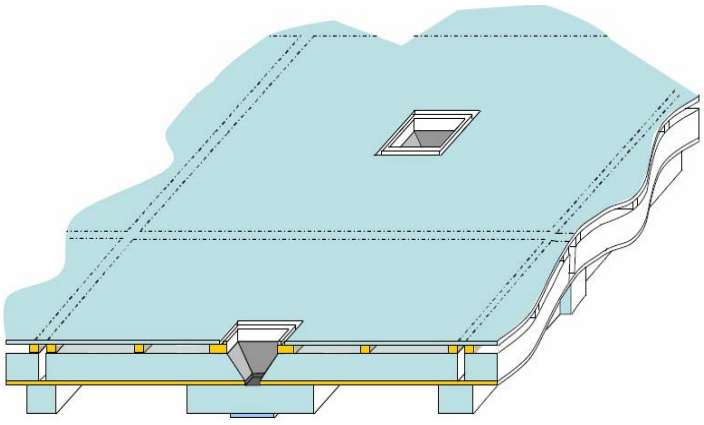

Figure 2: 3D diagram of trench-isolated CMUT with a supporting frame.

II. DESIGN CONCEPTS

In frameless trench-isolated CMUT arrays, only a few microns of silicon and silicon dioxide remain between array elements after the DRIE process. These thin-films are fragile and present handling difficulties. A carrier wafer is therefore needed for additional mechanical support during DRIE and flip-chip bonding steps. Instead of the carrier wafer, the trench-isolated CMUT arrays with a supporting frame have a built-in silicon mesh structure in between array elements to provide the needed mechanical support. A cross-sectional view and a 3D diagram of the supporting frame concept are illustrated in Fig. 1 and Fig. 2. Both the supporting frame and the signal electrodes are built into the substrate of a highly conductive SOI wafer. Deep through-wafer trenches are etched from the back side of the SOI wafer to separate the frame and the signal electrodes. The front electrical pads are electrically divided by trenches etched on the device layer of the same SOI wafer. A via is etched on the device silicon and the buried oxide (BOX) layers so that aluminum can be sputtered into the via to bring electrical continuity for the signal electrodes.

In the trench-isolated CMUT arrays with supporting frames, the parasitic capacitance is largely determined by the overlapping areas between the device and bulk layers of the SOI wafer. Therefore, the parasitic capacitance can be reduced by increasing the BOX layer thickness and reducing the width of the mesh frames. In our test runs, SOI sample pieces with frames as narrow as 10 µm were fabricated. These pieces could be handled like regular pieces of silicon. The BOX layer thickness can be easily made to 4 – 5 µm thick in a wet oxidation environment at 1100 ^{o}C for 48 hours. Fig. 3 shows the calculated parasitic capacitance as a function of BOX layer thickness for a 200-µm thick SOI wafer with a frame width of 30 µm. As seen in the figure the parasitic capacitance can be reduced to an insignificant level by design, assuming the device capacitance of an array element is in the order of 1 pF.

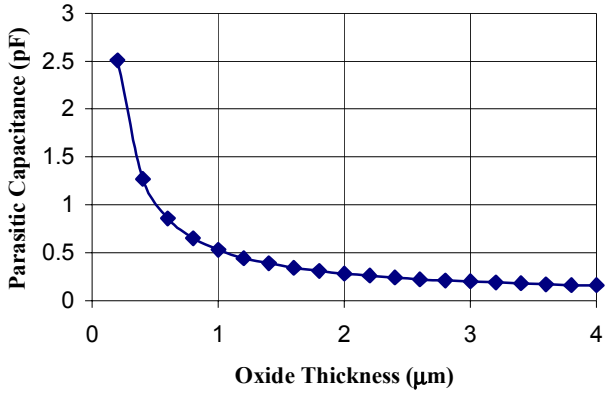

Figure 3: Calculated parasitic capacitance as a function of BOX thickness. Frame width: 30 µm, trench width: 40 µm, substrate thickness: 200 µm.

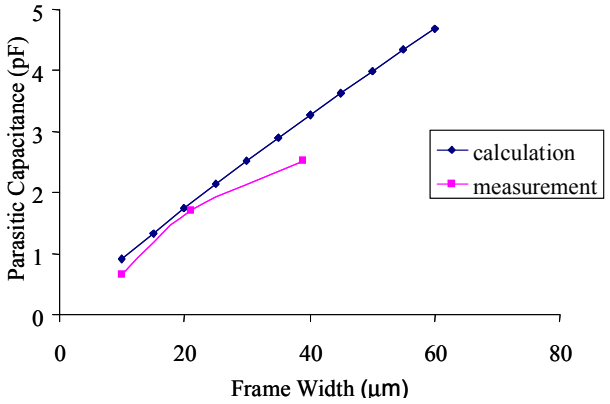

Figure 4: Calculated and measured parasitic capacitance on a test device.

To confirm the calculation of the parasitic capacitance, test dummy devices consisting of mesh frames and front side electrical pads were fabricated on an SOI wafer with an 8-µm device layer and 0.2-µm BOX layer. Fig. 4 shows the measured and calculated capacitance values. One possible explanation for the smaller measured capacitance than the calculated capacitance is the footing phenomenon of the DRIE when the etching is terminated on oxide [5]. Tooting reduces the effective overlapping areas between the signal and ground electrodes and thus results lower parasitic capacitance.

Series resistance is a function of the size of the signal electrode and the resistivity of the silicon substrate. To reduce the series resistance, a highly conductive substrate is desired. Fig. 5 shows the expected resistance values of an electrode for varies substrate resistivities. When a highly conductive substrate is used, the series resistance can be ignored.

Because a contact via is needed in the device layer to make electrical continuity for the interconnects, the fill factor of the CMUT is affected. This is analogous to the reduction of fill factor in CMUTs with through-wafer via interconnects. This impact of fill factor is compensated by the fact that the isolation trench on the front side of the device layer can be narrow (a few microns) because this layer is relatively thin and definition of narrow trenches is possible using DRIE. In our design, a fill factor of 0.72 is achieved.

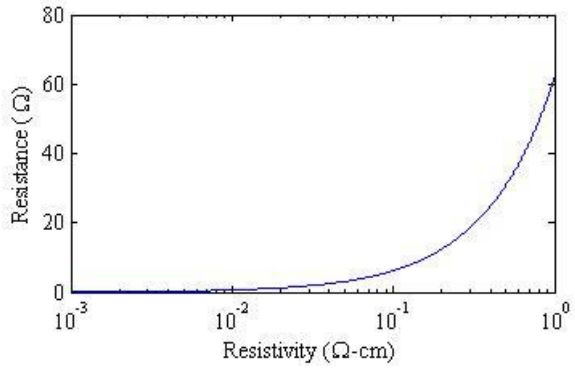

Figure 5: Expected series resistance as a function of substrate resistivity. Electrode size: 180 µm x 180 µm x 200 µm.

III. Process Details

We fabricated trench-isolated, 2D, 16-element x 16-element, CMUT arrays with supporting frames to demonstrate the feasibility of this technique. A summary of the device parameters is shown in Table I.

TABLE I: DEVICE PARAMETERS FOR TRENCH-ISOLATED CMUT ARRAY WITH A SUPPORTING FRAME.

Membrane Width (μm)	40
Membrane Length (μm)	140
Number of Membranes / Element	8
Element Pitch (μm)	250
Membrane Thickness (μm)	1.84
Cavity Height (μm)	0.15
Substrate Thickness (μm)	200
Device Layer Thickness (μm)	10
BOX Layer Thickness (μm)	1.95
Trench Width (μm)	50
Frame Width (μm)	30
Silicon Wafer Resistivity (Ω-cm)	0.025

Fig. 6 illustrates the detailed fabrication steps. CMUT cavities are first defined on the device layer of a double-side-polished SOI wafer using oxidation and buffered oxide etching (BOE) techniques. The front electrical pads are then electrically divided in a DRIE step. Following that, another SOI wafer with a membrane silicon layer is fusion bonded to the device side of the first SOI wafer and annealed at 1000 °C for 30 minutes. The handle wafer of the second SOI wafer is removed in a heated tetramethylammonium hydroxide solution. A contact via on each array element is defined by photo lithography and wet etching of silicon in heated potassium hydroxide (KOH) solution using the BOX layer of the second SOI wafer as the hard mask. This etching step stops automatically at the BOX layer underneath the device layer. A dry plasma etcher (AMT 8100 plasma etcher, Applied Materials, Santa Clara, CA) is used to remove the recessed BOX layer in the via region. In this step, the exposed silicon resulting from the KOH etching step serves as the hard mask. An aluminum layer is sputtered on the silicon membrane to form the top electrode, as well as on the contact via to establish electrical continuity for the signal electrodes. The silicon substrate is thinned down to 200 μm by mechanical grinding and polishing. A 7-μm-thick photo resist layer is spin-coated onto the back side of the SOI wafer and patterned. The signal electrodes and the supporting frames are formed in the subsequent DRIE etching step. A layer of Ti/Cu/Au is evaporated onto the electrodes to enhance the electrical contact to the silicon. During evaporation, the wafer is tilted for 45° to prevent electrical shorting between neighboring elements. Fig. 7 and Fig. 8 show the finished devices with contact vias, supporting frames and signal electrodes.

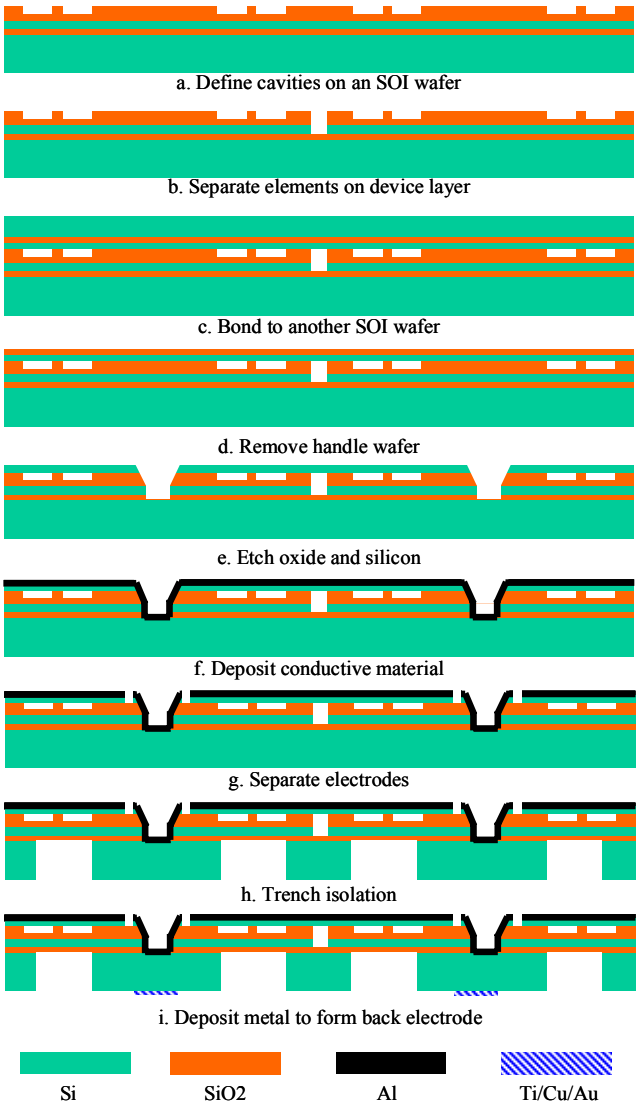

Figure 6: Process steps.

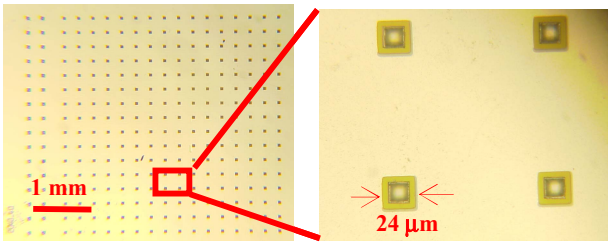

Figure 7: Optical pictures of the front side of the CMUT array. The zoomed-in picture shows the contact vias.

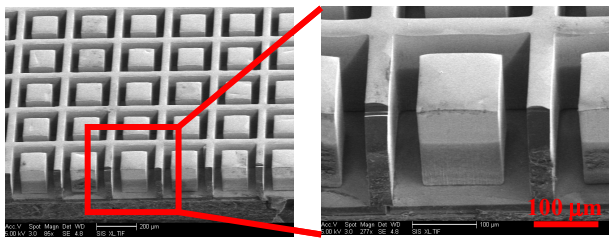

Figure 8: SEM pictures of signal electrodes and supporting frame.

IV. TEST RESULTS

Electrical input impedance in air was measured by probing the signal electrodes on the finished devices using a network analyzer (Model 8751, Hewlett-Packard Company, Palo Alto, CA). Fig. 9 shows the typical real and imaginary parts of the input impedance. The resonant frequency as a function of DC bias voltage is shown in Fig. 10. The collapse voltage is found to be 80 volts, reasonably close to the predicted value of 82 volts. Across the array, the resonant frequency is uniform. The standard deviation is 0.02 MHz (0.23%). In the first fabricated array, 6 elements out of a total of 256 elements in an array do not show resonance due to lithographic defects during processing.

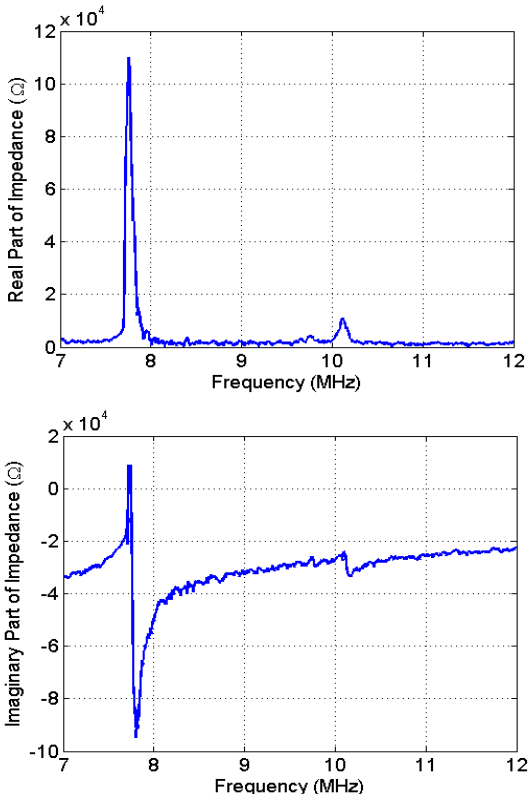

Figure 9: Electrical input impedance in air.

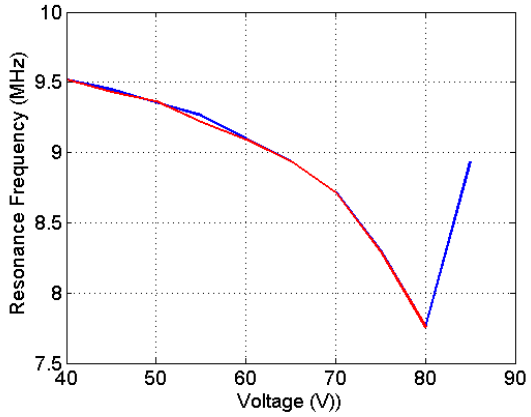

Figure 10: Resonance frequency as a function of DC bias voltage.

The total device capacitance is measured to be 1.9 pF. Based on the design parameters, the predicted device capacitance is calculated to be 1.66 pF, and the parasitic capacitance is calculated to be 0.29 pF. Therefore, the total measured capacitance agrees with the theoretical prediction.

V. FUTURE WORK

In our future work, the trench-isolated CMUT arrays with supporting frames will be flip-chip bonded to a custom-designed integrated circuit (IC) to perform volumetric imaging.

VI. CONCLUSIONS

2D CMUT arrays with a supporting frame have been demonstrated. Through-wafer trench-isolated interconnects are implemented on theses arrays. The finished wafers can be handled like regular wafers. The fabrication process is compatible with both the surface micromachining and the wafer bonding processes developed for CMUTs because the trenches are fabricated after the formation of the CMUT membranes. The overall process is simple, and results in good device uniformity. These CMUT devices have a parasitic capacitance that is negligible when compared to the device capacitance. In air testing, the predicted resonant frequency and collapse voltage are reasonably close to the predicted values.

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