INTERCONNECTION AND PACKAGING FOR 2D CAPACITIVE MICROMACHINED ULTRASONIC TRANSDUCER ARRAYS BASED ON THROUGH-WAFER TRENCH ISOLATION

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ABSTRACT

A new process for connecting elements of a 2D capacitive micromachined ultrasonic transducer (CMUT) array to flip-chip bond pads on the back side of the transducer array is presented. Array elements are isolated from one another by trenches etched into the highly conductive silicon substrate using deep reactive ion etching (DRIE). Gold is deposited on the back side of the array to create the flip-chip bond pads. The array is then flip-chip bonded to an integrated circuit that comprises the front-end circuitry for the transducer and provides mechanical support for the isolated array elements. Because the interconnects are fabricated after the CMUT membranes, this technique is suitable for CMUT arrays regardless of the fabrication techniques used to form the membranes.

1. INTRODUCTION

In recent years, researchers have demonstrated through-wafer electrical interconnects for silicon-based micromachined sensors and actuators [1-4]. These interconnects are particularly important in MEMS systems where densely populated 2D transducer elements are desired. In these systems, there is little room to spare for interconnect routing. One existing through-wafer interconnect implementation is based on through-wafer vias [2]. Vias are etched from both sides of a highly resistive silicon wafer and are insulated from the substrate by a layer of oxide. A conductive material such as doped polysilicon is then deposited to fill the vias and to provide an electrical path from the front side of the wafer to the back side. The process of filling the vias creates stress across the silicon wafer and contaminates the wafer surface, making this scheme unsuitable for silicon-on-insulator (SOI) wafer bonding later on. The SOI wafer bonding technique is a powerful tool used to fabricate the CMUT and a wide range of other MEMS devices [5, 6].

One way to overcome the shortcomings of the through-wafer via scheme is to avoid the stress inducing process steps before the SOI wafer bonding. Through-wafer trench isolation is based on this concept. Instead of etching the through-wafer vias, through-wafer trenches are etched using the same DRIE process after the membranes are formed. The silicon substrate itself then acts as the electrical connection from the wafer front side to the wafer back side. This paper presents the fabrication steps for this technique, as well as methods to flip-chip bond a trench isolated CMUT to an integrated circuit (IC) or fan-out board. The fabrication for trench isolation is simple yet trench isolated arrays have lower series resistance and improved substrate flexibility compared with the existing through-wafer via implementation.

2. CMUT AND TRENCH DESIGN

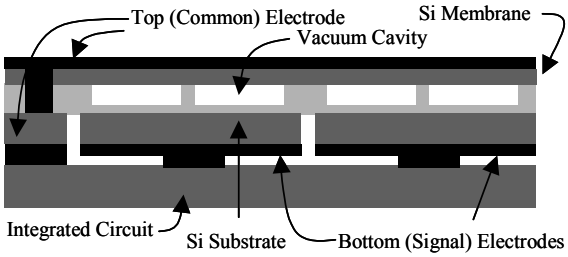


Figure 1: Cross-sectional schematic of a trench-isolated CMUT array that is flip-chip bonded to a custom-designed IC.

Fig. 1 shows a schematic of a trench-isolated CMUT array that is flip-chip bonded to a custom-designed IC. The CMUT is formed on the front side of the wafer. The CMUT is composed of a thin membrane supported by oxide sidewalls over a shallow vacuum cavity. These membranes are coated with a layer of metal to form the top (common) electrode of the device. The conductive Si substrate and gold metal on the back side of the array form the bottom (signal) electrode. The resulting structure is essentially a vacuum gap capacitor. The common electrode and the signal electrodes are separated by the through-wafer trenches. The IC provides a DC bias to the membranes through the common electrode and applies AC voltage through the signal electrodes to actuate the membranes and generate ultrasonic waves. Reflected ultrasound is detected by the same array. Low noise amplifiers on the IC amplify the transducers' signals due to the impinging ultrasound.

An increasingly popular application for 2D CMUT arrays is medical imaging. This paper reports on 16 element by 16 element 2D CMUT arrays designed and fabricated for endoscopic ultrasonic imaging applications. The CMUT has a 250-μm element pitch. The 2.56-μm thick rectangular membranes (rectangular membranes are preferred for higher active area coverage) are 48 μm wide and 220 μm long. The membrane geometry was chosen such that the center frequency is around 5 MHz when loaded with water. The cavity height was designed to be 0.3 μm thick according to the operating voltage requirements.

The isolation trenches were designed to be 10 μm wide. Wider trenches are preferred for reduced electrical crosstalk between elements. However, wide trenches reduce the active area and fill factor for each element, thus sacrificing transducer performance in areas such as fractional bandwidth.

3. FABRICATION

The fabrication process is shown in Fig. 2. It consists of three major stages: the first is the formation of the CMUT cavities on the front side of the wafer, the second is etching the through-wafer trenches, and the last stage is flip-chip bonding the CMUT array to a fan-out board or an IC chip.

Fabrication of CMUT

Two predominant fabrication methods exist for CMUT fabrication: surface micromachining and SOI wafer bonding. The SOI wafer bonding technique was used to fabricate the membranes in this study. Cavities are defined by growing and patterning thermal oxide on a highly conductive prime silicon wafer (0.025 Ω-cm). An SOI wafer is bonded to the prime wafer by fusion bonding. Membranes are formed after the handle wafer and the buried oxide layer are removed by wet etching.

A layer of aluminum is sputtered onto the membrane to form the common electrode. The silicon membrane and the oxide layer underneath are selectively opened to establish a connection to the common electrode from the back side of the wafer by the sputtered aluminum.

Substrate Thinning and Trench Isolation

After the CMUT membranes are formed, the membrane side of the wafer is temporarily bonded to a carrier wafer for mechanical support. This is necessary because after the trench etching, the array elements are only attached by the thin membrane on the front side. A 15-μm thick dry photoresist film (Riston CM206, Dupont, Wilmington, DE) is used to assist the bonding. A 250-μm thick quartz wafer is used as the carrier wafer. The quartz carrier wafer thickness is chosen to be thick enough for the needed mechanical support, yet thin enough for reduced thermal resistance during the subsequent DRIE process.

The silicon substrate of the device wafer is then grinded and polished down to 120 μm. The reduced substrate thickness offers a number of advantages such as less cross-coupling capacitance between array elements and smaller series resistance for the interconnects. For ultrasonic transducers, it is also important to be able to thin the substrate to push interference due to substrate reverberations out of the operation frequency band.

The dry photoresist film and the quartz are both optically transparent, enabling front-to-back alignment when defining the trenches by photolithography. During the DRIE process, the dry photoresist film shows no sign of deformation or outgassing, and bonding strength is sufficient to hold the 250-μm by 250-μm silicon pillars in place. The DRIE is timed such that the silicon pillars are completely isolated from each other. Over etching is avoided to minimize the sideway etching when the DRIE is terminated on the oxide layer.

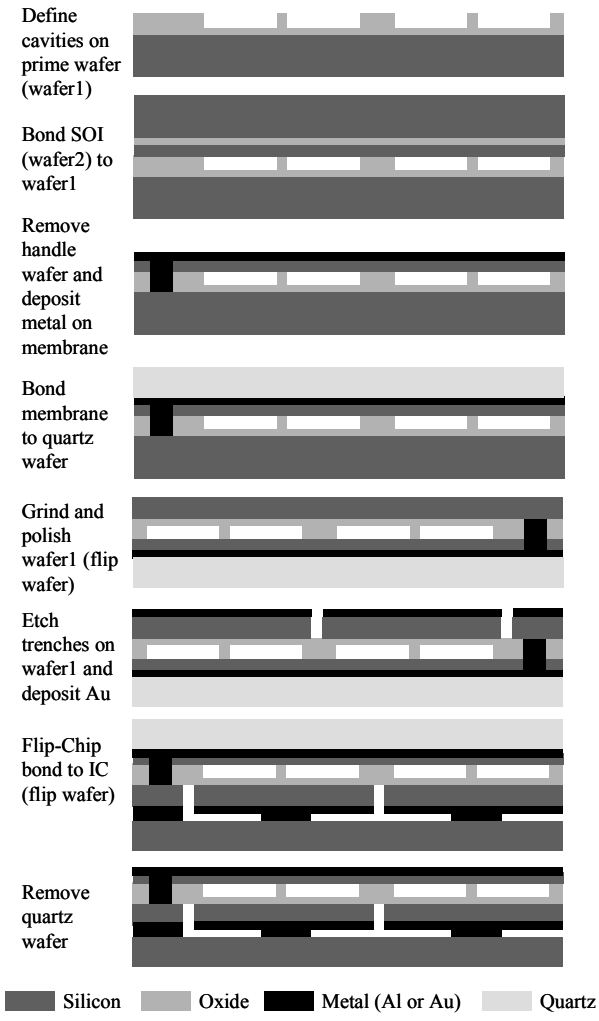
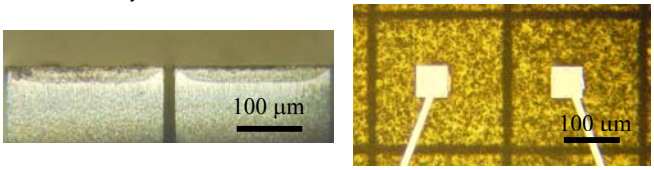


Figure 2: Fabrication steps for through-wafer trench-isolated CMUT arrays.



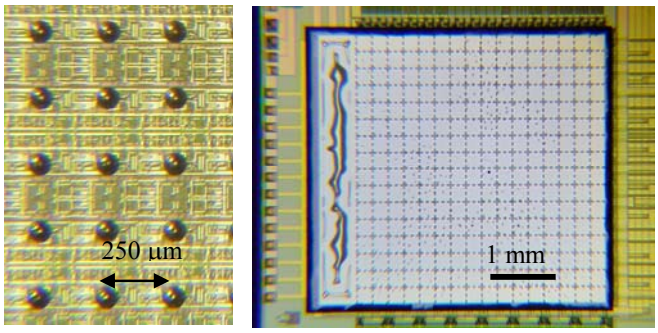
(a) (b)

Figure 3: (a) A trench profile. (b) Back side view of ACF-based flip-chip bonded trench-isolated electrodes seen through a quartz fan-out board.

Flip-Chip Bonding

A Ti/Cu/Au metal stack is evaporated onto back side pads to enhance electrical contact and to establish the needed under bump metallurgy (UBM) for flip-chip bonding. Two flip-chip bonding techniques have been investigated. The first is based on anisotropic conducting film (ACF). For this technique, a wire bonder is used to place 25-μm diameter, 25-μm tall gold bumps on the 50-μm by 50-μm bond pads on a matching chip, which can be an IC or a fan-out board. ACF (FP1708E, Sony Chemicals, Tokyo, Japan) is then laminated on the matching chip. A flip-chip bonder (Model M8, Research Devices Inc., Piscataway, NJ) is used to align and bond the two parts by applying a pressure of 30 g/bump and a peak temperature of 190 ^{o}C for 20 seconds. The ACF film is cured at the elevated temperature. It conducts at the points where it is squeezed between the CMUT pads and the gold bumps. Fig. 3 (b) shows a back side view of ACF-based flip-chip bonded trench-isolated electrodes seen through a quartz fan-out board.

For the second flip-chip bonding technique, solder bumps are deposited on the bond pads of the matching chip. These pads are first coated with 5 μm of Ni/Au with an electroless plating process to provide the correct UBM for the solder bumps. Solder balls with diameters of 80 μm are placed onto these bond pads using a solder jetting process [7]. A picture illustrating an IC chip with solder balls in place is shown in Fig. 4 (a). The CMUT and IC are aligned and heated to 150 ^{o}C with 4 g/bump pressure. Following the alignment, the samples are placed into an inert atmosphere oven and a reflow at 200 ^{o}C is performed. A trench-isolated CMUT array flip-chip bonded to an IC using solder bumping is shown in Fig. 4 (b).



(a) (b)

Figure 4: (a) A section of an IC with solder balls placed using solder jetting and (b) a trench-isolated 2D CMUT array flip-chip bonded to an IC chip using solder bumps.

After the flip-chip bonding, mechanical support is provided by the IC or fan-out board. The quartz carrier wafer can be removed by a wet releasing process in acetone. Fig. 5 shows the membrane side of a CMUT array after releasing.

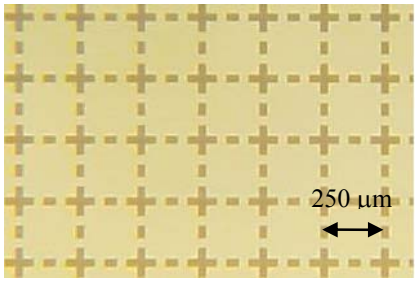


Figure 5: 24 CMUT membranes after releasing of quartz carrier.

4. TEST RESULTS

The theoretical series resistance of the interconnect is given by

$$R = \rho \cdot \frac{L}{A}, \qquad (1)$$

where ρ is the resistivity of the silicon substrate, L is the thickness of the substrate and A is the area of the pillars. The calculated resistance is 0.57 Ω based on this formula. The measured series resistance is 4.5 Ω. The measurement was performed with a network analyzer on array elements flip-chip bonded to a fan-out board [Fig. 3(b)]. Therefore this series resistance includes the ACF-based flip-chip bond resistance, which accounts for the difference between the calculated and the measured resistance values. The series resistance is reduced when compared to that of the existing through-wafer vias, which can be as high as 65 Ω [2].

Fig. 6 shows the electrical cross coupling measurement results between two closest elements in an array. Both the excitation and received pulses were terminated with a 1-MΩ load. The electrical crosstalk between two neighboring elements is less than -53 dB, corresponding to a coupling capacitance of about 29 fF. Since the device capacitance is about 1 pF, the cross coupling capacitance can be safely neglected for practical purposes.

Fig. 7 shows the electrical input impedance of a trench-isolated CMUT array element connected to a fan-out board. The array element is operated with 110 V applied bias. The acoustical resonance behavior fits the prediction based on an equivalent circuit model [8] closely. The bias voltage was increased until the fundamental resonant frequency disappeared. This point corresponds to the membrane touching the bottom of the cavity, collapsing. The collapse voltage was found to be 175 volts, close to the predicted value of 180 volts.

An added benefit of the trench-isolated interconnect technique is that it has the potential to enable flexible arrays. In medical ultrasound, flexible 1D and 2D arrays are needed to cover a curved surface for applications such as side-looking catheters and large area conformal arrays for lesion detection

deep in the body. Preliminary results from this work show it is possible to fold trench-isolated CMUT arrays [Fig. 8].

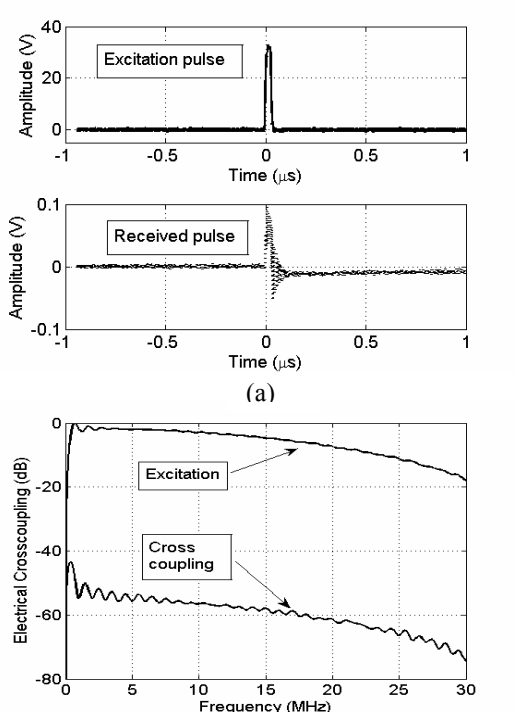


Figure 6: Electrical cross coupling measurements. (a) Time domain waveform. (b) Frequency domain.

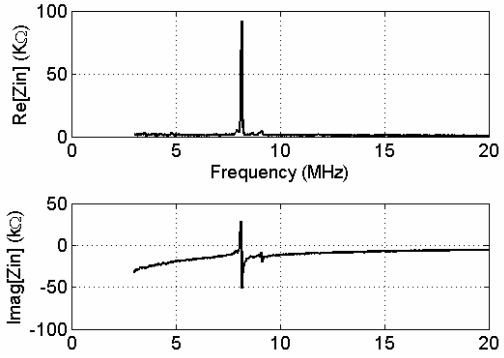


Figure 7: Real and imaginary parts of the input impedance of a trench-isolated CMUT array element.

Figure 8: Trench-isolated 2D CMUT arrays with a curvature.

5. CONCLUSIONS

Interconnection and packaging for 2D CMUT arrays based on through-wafer trench isolation and flip-chip bonding have been demonstrated. Fabrication of these interconnects is compatible with both the surface micromaching process and the wafer bonding process for CMUTs. The process is simplified when compared to the existing through-wafer via scheme, while the series resistance is reduced to 4.5 Ω. Electrical cross coupling between elements is less than –53 dB and is therefore negligible.

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