FABRICATING CAPACITIVE MICROMACHINED ULTRASONIC TRANSDUCERS WITH DIRECT WAFER-BONDING AND LOCOS TECHNOLOGY

K. K. Park, H. J. Lee, M. Kupnik, Ö. Oralkan, and B. T. Khuri-Yakub

Edward L. Ginzton Laboratory, Stanford University, Stanford, California, USA

ABSTRACT

We present an improved fabrication method for capacitive micromachined ultrasonic transducers (CMUTs). Recently, a process was developed to fabricate CMUTs using direct wafer-bonding instead of the traditional sacrificial release method. This paper presents a method based on local oxidation of silicon (LOCOS) and direct wafer-bonding to improve the controllability of gap heights and the parasitic capacitance. Critical vertical dimensions are determined by a thermal oxidation process, which allows tight vertical tolerances (< 10 nm) with unmatched uniformity over the entire wafer. Using this process we successfully fabricated CMUTs with gap heights as small as 40 nm with a uniformity of ± 2 nm over the entire wafer.

1. INTRODUCTION

CMUTs are gaining increasing attention in the field of medical and underwater imaging, not only as a replacement for piezoelectric transducers, but also as an enabling component for new applications [1]. In addition, CMUT technology has recently been used to make devices for applications such as high intensity focused ultrasound (HIFU) therapy [2] and resonating chemical sensors [3]. The basic structure of a CMUT consists of a movable thin membrane and a supporting substrate separated by a vacuum cavity. Typically, a doped silicon substrate makes up the bottom electrode of the capacitor and a conducting membrane acts as the top electrode. The membrane vibrates harmonically when excited with an electrical AC signal. Conversely, an electrical signal is generated when the membrane vibrates due to impinging ultrasound waves.

The first CMUT was fabricated using a sacrificial release process [4]. In this process, a silicon nitride membrane layer is deposited on a patterned sacrificial polysilicon layer; the polysilicon is subsequently removed via small channels; and then the resulting gap is vacuum sealed by a second silicon nitride layer deposited on top of the membrane; the final membrane thickness is set by etching back the nitride layer. There are several inevitable drawbacks of this CMUT fabrication method: It might not be possible to release the membrane because of the possible stiction problems [5]; intrinsic stress in the nitride membrane is very sensitive to deposition conditions; the membrane thickness can not be tightly controlled because of the successive deposition and etching steps used to form the membrane; the gap height can not be well controlled because of the unwanted nonuniform nitride deposition in the cavity during the sealing step [6].

As a promising alternative to the sacrificial release process, a CMUT process utilizing the well-known direct wafer-bonding technique (fusion bonding) was developed [7]. In this process, the vacuum cavities are formed by etching an oxide layer before the wafer is bonded to a silicon-on-insulator (SOI) wafer in a vacuum chamber. After removing the handle wafer and the buried oxide (BOX) layer of the SOI wafer, a single crystal silicon layer remains as the CMUT membrane with good uniformity and without significant residual stress. However, this process controls the vacuum gap height through an etching process (dry or wet), making precise gap control difficult. In addition, the minimum gap height is limited by the thickness of the initial oxide layer. This requires a design compromise in terms of the breakdown voltage and the parasitic capacitance in the area between the cells of the CMUT. However, an extended insulation layer structure (post) for CMUTs can be used to address these issues [8].

In this paper, we introduce a CMUT fabrication process based on LOCOS and wafer-bonding. This process overcomes the two main issues associated with the conventional wafer-bonding process for CMUT fabrication: low breakdown voltage and high parasitic capacitance. Furthermore, we demonstrate that this process features an excellent gap height control, which is achieved by patterning the silicon substrate inside the cavity via thermal oxidation, and then forming the oxide posts by a selective thermal oxidation step using the conventional LOCOS process.

2. PROCESS FLOW

The fabrication process (Fig. 1) starts with a 2-μm thick thermal oxidation (1050°C, Wet O_2) on a highly doped silicon substrate. The silicon dioxide (SiO_2) layer is then patterned and etched down to the silicon substrate [Fig. 1(a)], leaving SiO_2 only on the regions that will be used to form the bottom electrodes. The etching process is performed in two steps to minimize an etch undercut. 80% of the grown oxide thickness is first etched by plasma etching. This process has a poor selectivity between SiO_2 and Si, and also increases the surface roughness. Thus, to maintain the surface smoothness, the remaining 20% of the SiO_2 layer is wet-etched in a 20:1 buffered oxide etch (BOE) solution with minimum over-etching time. Over-etching in BOE increases the surface roughness [9]. Therefore, the durations of all BOE etchings are set based on the calculations using the measured oxide thickness.

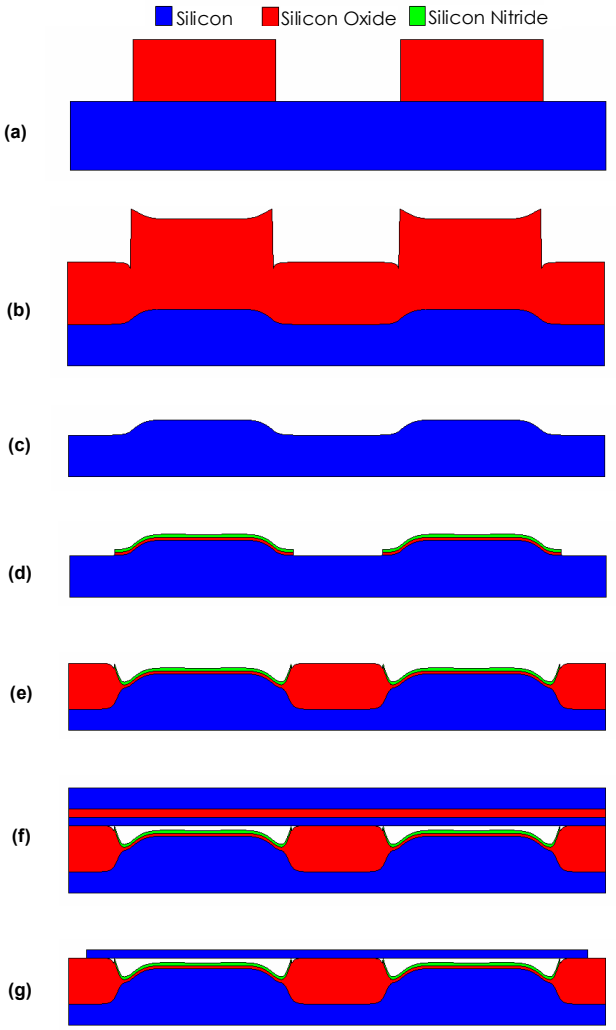

Figure 1: Main process flow of fabrication.

After patterning the oxide layer, an additional thermal oxidation (1050°C, Wet O_2) is performed [Fig. 1(b)]. Taking advantage of different oxide growth rates for SiO_2 on SiO_2 and SiO_2 on Si, a pattern of protrusion can be created in the silicon substrate below the initially grown SiO_2 layer by removing all thermally grown SiO_2 by 6:1 BOE [Fig. 1(c)], again with minimum over-etch time. The next step is the thermal growth of a 40-nm thick base oxide layer (1000°C, Dry O_2), which is followed by low-pressure chemical vapor deposition (LPCVD) of a low-stress 80-nm silicon nitride (Si_3N_4) layer. After patterning, the thin nitride film and oxide films (nitride-oxide layer) are etched with plasma etching and 20:1 BOE, respectively [Fig. 1(d)]. The base oxide layer acts as a protective layer when etching the nitride film in two ways. First, it acts as an etch stop for the plasma etching of silicon nitride. Second, it protects the surface smoothness at the oxide to silicon interface. After patterning the nitride with plasma etching, the oxide is patterned with 20:1 BOE with minimum over-etching time. A 700-nm thick oxide layer is then grown (1050°C, Wet O_2) [Fig. 1(e)]. With the Si_3N_4 masking oxygen from diffusing into the bottom electrode, local oxidation of silicon (LOCOS) is performed. The locally grown SiO_2 becomes

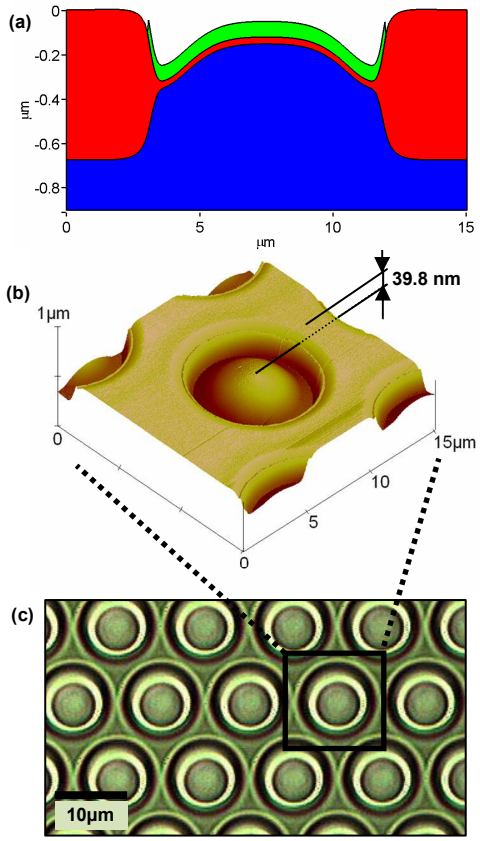

Figure 2: (a) TSUPREME-4 simulation of LOCOS process. Color code is the same as Fig. 1. (b) AFM measurement. Measured step height is 39.8 nm. Edge of the LOCOS mask is visible. (c) Optical picture of the corresponding step.

the post structure, which will be the wafer-bonding surface and support the membrane. All previous process steps are designed and monitored to maintain a minimal roughness on the post surface. An SOI wafer with a 500-nm thick and highly doped silicon device layer is then fusion bonded in vacuum to the processed wafer [Fig. 1(f)]. The vacuum cavities of the CMUT are enclosed by the oxide post, nitride-oxide layer and the SOI wafer. This vacuum seal is maintained by the good quality of the wafer bonding process. To further enhance the strength of the wafer-to-wafer bond, the bonded wafers are annealed in N_2 at 1050°C for 5 hours. The handle wafer of the bonded SOI wafer is then removed using Tetramethylammonium Hydroxide (TMAH) and the BOX layer is removed in 6:1 BOE. After this step, the front side of the wafer surface is covered by a 500-nm conductive silicon membrane.

The silicon membrane is then patterned to define the elements of the CMUT array [Fig. 1(g)]. The next step is to deposit aluminum, which is later patterned to form electrical contact pads for each element. One contact pad is placed on top of the bonded silicon membrane. The other contact pad is placed directly on the silicon substrate providing a common ground contact for all the elements, *i.e.* the silicon dioxide layer had to be patterned before the aluminum deposition step. As a last step, through-wafer trenches are

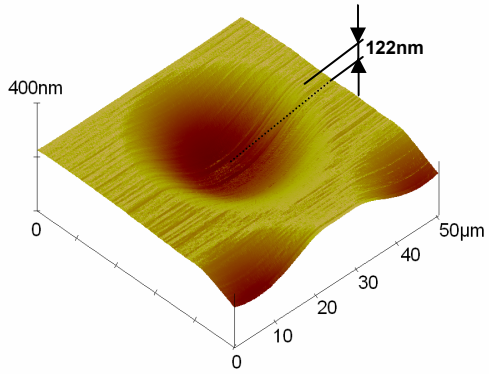

Figure 3: AFM measurement of the bonded membrane. Diameter of this membrane is 40 µm and the thickness is 0.5 µm. Deflection due to the atmospheric pressure is 122 nm.

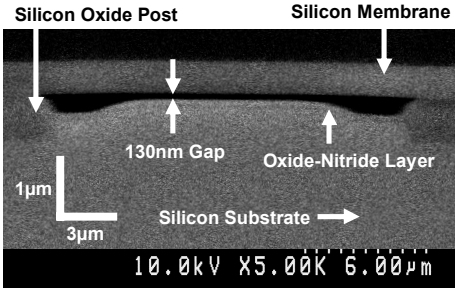

Figure 4: SEM photograph of the cross section of a single CMUT cell. The photograph is stretched 3.2 times in vertical direction for better visibility.

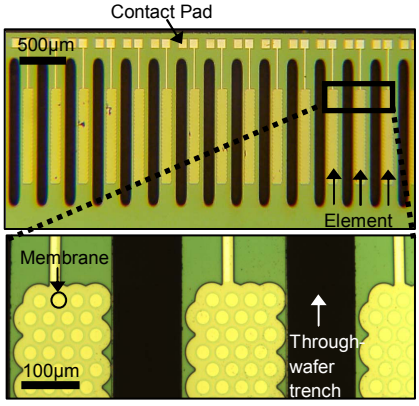

Figure 5: Optical picture of the fabricated device.

formed using deep reactive ion etching (DRIE) to reduce the element-to-element crosstalk through the substrate (Fig. 5).

3. RESULTS

Wafer-bonding process

The success of the wafer-bonding process [Fig. 1(f)] is determined by the bond strength. Besides the well–known requirement of low surface roughness for a successful direct wafer bonding, two further criteria are essential for good bond strength. First, the geometrical flatness of the two bonding surfaces should be low enough [10]. The grown oxide, the post [Fig. 1(e)], needs to provide a sufficiently flat bonding area. Second, the edge of the LOCOS mask must be lower than the level of bonding surface. These

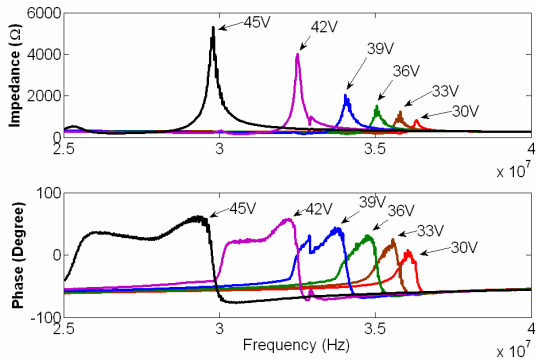

Figure 6: Measured electrical input impedance of 40 nm gap device at several different bias voltages (Silicon membrane, diameter: 12 µm, thickness: 0.5 µm, 2240 membranes per array).

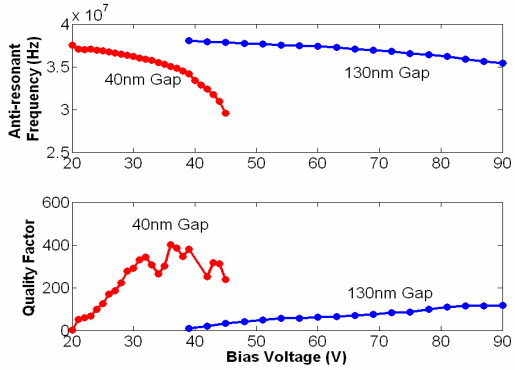

Figure 7: Comparison between two devices with different gap heights. Anti-resonant frequency and the quality factor are calculated from the electrical input impedance.

criteria were verified through TSUPREME-4 simulations [Fig. 2(a)] in the design step and through atomic-force-microscope (AFM) measurements during the fabrication run [Fig. 2(b)]. The surface roughness of the bonding area was monitored for each pre-bonding fabrication step. We were able to keep the surface roughness as low as ~2.4 $Å_{RMS}$ prior to bonding, although there were two short over-etching in BOE before the final oxide posts (bonding area) were grown. The surface roughness of the substrate before fabrication was ~1.5 $Å_{RMS}$.

As mentioned before, the wafer-bonding process was performed at a pressure smaller than 0.5 x 10^{-5} mTorr. Already at the stage of Fig. 1(g), we verified that our CMUT cells were vacuum sealed by performing atomic force microscope measurements (Fig. 3).

Fabrication

We successfully fabricated several CMUT arrays. One example is shown in Fig. 4; the array has 32 elements; each element consists of 100 to 3200 membranes connected in parallel; elements are separated from each other by through-wafer trenches. Most of the device area is covered by silicon dioxide, grown by the LOCOS process [Fig. 1(e)]. The area of highly conductive silicon is minimized to reduce the parasitic capacitance of the device.

Because the bonded silicon membrane is highly conductive, metal electrodes on the membranes are not required. This is a great advantage for the chemical sensor applications [3] for two reasons. First, the smaller mass of each membrane results in better mass sensitivity. Second, the absence of the metal electrodes reduces the thermally induced stress effects that might occur during the metal deposition step due to the thermal expansion coefficient mismatch between the Si membrane and the metal electrode [11].

The dimensions of the cavity and the thickness of the silicon membrane determine the mechanical resonant frequency of the CMUT. In the presented process flow, the thickness of the silicon membrane was precisely determined by the specifications of the SOI wafer and measured before the fabrication process. Also dimensions of the cavity were measured during the fabrication run using an AFM [Fig. 2(b)].

For further verification of the fabrication process, we cleaved one wafer (Fig. 4.) and used a scanning electron microscope (SEM) to image the device cross section. The locally grown SiO_2 posts and the bird's beak structure are visible in Fig. 4, which corresponds to Fig. 1(g) (both figures are vertically exaggerated). The device in Fig. 4 has a 130-nm vacuum gap height, which is only 14% of the SiO_2 post thickness. We also successfully fabricated the same structure with a 40-nm gap and 720-nm oxide posts.

Characterization

Electrical input impedance measurements are widely used to characterize CMUTs as well as MEMS resonators [1,3,7,12]. We used an impedance analyzer (Model 4294A, Agilent Technologies, Palo Alto, CA), and a variable DC bias voltage connected via a bias-T to measure the electrical input impedance of the device (Fig. 6). The magnitude of the input impedance has a minimum value at its mechanical resonant frequency (*i.e.* series resonant frequency). The maximum impedance at the anti-resonant frequency (*i.e.* parallel resonant frequency) is determined by the mechanical properties of the membrane and the parasitic capacitance. Due to the spring softening effect [13], both resonant frequencies decrease with increasing bias voltage. In general, our devices show similar characteristics to other CMUTs fabricated with conventional wafer bonding process or sacrificial nitride process [1,3,7]. The CMUT can be modeled with an equivalent circuit and the model parameters can be derived from input impedance measurements in the frequency domain using simple curve fitting. This allows determining performance parameters, such as resonant frequency, quality factor and parasitic capacitance, etc. Since the gap height is now independent to the SiO_2 post, we were able to successfully fabricate 40-nm gap devices. Fig. 7 shows the comparison of the 40-nm to 130-nm gap devices. The thin gap devices exhibit a higher quality factor (~300-400) at lower bias voltages.

4. CONCLUSIONS

We introduced a CMUT fabrication process that is based on wafer-bonding and LOCOS. The process allows an independent control between the gap height and the oxide post thickness. This is advantageous in terms of reliability (electrical breakdown) and device performance (parasitic capacitance). Based on well developed thermal oxidation methods, this process enables to fabricate devices with precise dimensions. This process also yields superior uniformity and reproducibility compared to previous process flows.

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REFERENCES

[1] A. S. Ergun *et al*., "Capacitive Micromachined Ultrasonic Transducers: Theory and Technology", *J. Aerosp. Eng*., vol. 16, pp. 76-84 , 2003.

[2] S. H. Wong *et al*., "Design of HIFU CMUT Arrays for Treatment of Liver and Renal Cancer" in *Proc. 6th International Symposium on Therapeutic Ultrasound*, vol. 911, pp. 54-60, 2007.

[3] K. K. Park *et al*., "Capacitive Micromachined Ultrasonic Transducers for Chemical Detection in Nitrogen", *Appl. Phys. Lett.*, vol. 91, pp. 094102, 2007.

[4] M.I. Haller *et al*., "Micromachined 1-3 Composites for Ultrasonic Air Transducers", *Rev. Sci. Instrum*., vol.65, p.2095-2098, 1994.

[5] N. Tas *et al*., "Stiction in Surface Micromachining", *J. Micromech. Microeng*., vol. 6, pp. 385–397, 1996.

[6] D.-S. Lin *et al*., "Characterization of Fabrication Related Gap-Height Variation in Capacitive Micromachined Ultrasonic Transducers", accepted for *Proc. IEEE Ultrason. Symp.,* 2007.

[7] Y. Huang *et al*., "Fabricating Capacitive Micromachined Ultrasonic Transducers with Wafer-bonding Technology", *J. Microelectromech. Syst*., vol. 12, pp. 128- 137, 2003.

[8] M. Kupnik *et al*., "Extended Insulation Layer Structure for Capacitive Micromachined Ultrasonic Transducers," accepted for *Proc. IEEE Ultrason. Symp*., 2007.

[9] N. Miki *et al*,. "Effect of Nanoscale Surface Roughness on the Bonding Energy of Direct-bonded Silicon Wafers", *J. Appl. Phys.*, vol. 94, pp. 6800-6806, 2003.

[10] K. T. Turner, "Wafer Bonding: Mechanics-Based Models and Experiments", *Ph.D. dissertation*, MIT, 2004.

[11] M. Kupnik *et al*., "Finite Element Analysis of Fabrication Related Thermal Effects in Capacitive Micromachined Ultrasonic Transducers," in *Proc. IEEE Ultrason. Symp.*, pp. 938–941, 2006.

[12] C. T.-C. Nguyen et al., "An Integrated CMOS Micromechanical Resonator High-Q Oscillator", *J. Solid-State Circuits,* vol. 34, pp. 440-455, 1999.

[13] G. G. Yaralioglu et al., "Finite-Element Analysis of Capacitive Micromachined Ultrasonic Transducers", *IEEE Trans. Ultrason., Ferroelect., Freq. Contr.,* vol. 52, no. 12, pp. 2185- 2198, 2005.