DESIGN OF ALL-POLE LOW-PASS LADDER FILTERS USING CURRENT-MODE DAMPED INTEGRATORS

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ABSTRACT

A method for operational simulation of all-pole low-pass LC ladders filters by using current-mode damped integrators is introduced. The circuits obtained by this method need only current mirrors and capacitors and are convenient for realization in CMOS technology as well as can be used in other technologies.

1. INTRODUCTION

LC two-ports have played an important role in the design of filters [1] because of their very low passband sensitivities to element tolerances. Therefore, in recent years a considerable amount of effort have been devoted to the design of filters based on the operational simulation of LC ladder prototypes [2]. The basic building block in a filter is an integrator with multiple input or multiple output, which ideally should have infinite DC gain. The distinguishing characteristic of the method introduced in this paper is that damped integrators are used instead of ideal integrators. The advantage of using damped integrators is that they are more realistic and easier to implement since any integrator is damped in reality due to finite DC gain. In addition, the integrator constructed from a current mirror as explained in this work has finite input conductance and capacitance, therefore can absorb the shunt parasitics, such that the most of the parasitics effectively create pole or zero shift instead of new parasitic poles or zeros.

In synthesis of the ladder filters, we use current-mode blocks, which provide a high linearity with wide dynamic range operating at high frequencies and low supply voltages. Furthermore, addition and multiplication by a scalar can be performed in a simpler manner using current-mode blocks.

In the following section, the basic design procedure to generate the current-mode active circuit simulating the operation of an LC ladder prototype is introduced. Section III presents the simulation results for the current-mode ladder filter in comparison with the characteristics of the LC ladder prototype.

2. DESIGN PROCEDURE

Although the approach introduced here can be applied to any LC ladder circuit, for the sake of simplicity, it is explained by considering a third-order maximally flat low-pass minimum inductance LC ladder prototype. The ladder is terminated from both ends by 1-ohm resistors as shown in Fig. 1. By writing the node voltages in terms of mesh currents, and conversely the mesh currents in terms of the node voltages in s-domain, the signal flow-graph (SFG) corresponding to the LC ladder prototype in Fig. 1 is easily obtained as shown in Fig 2. Note that the integrator blocks

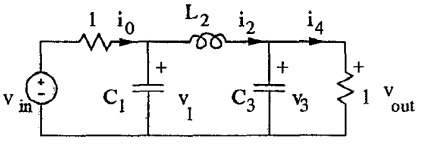

Figure 1. LC ladder prototype

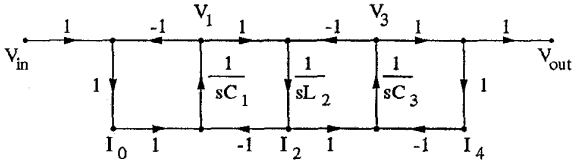

Figure 2. Signal-Flow Graph of the LC ladder prototype

in the signal-flow graph are lossless integrators. However, the integrators considered in this work are damped. Therefore, we must device an approach to convert this signal-flow graph to an equivalent one which is built by using damped integrators.

This approach basically propagates the source termination resistor toward the other end of the ladder by leaving resistors in parallel with the capacitors and in series with the inductors as will be explained in the following.

The first step is to convert the 1-ohm source termination resistor into two 2-ohm resistors in parallel as in Fig. 3(a). Then we use the i_s-shift property [3] to convert one of the 2-ohm resistors into the equivalent combination of vertical resistors and voltage controlled current sources (VCCS) as shown in Fig. 3(b), which are parallel to the input voltage source v_{in} and the capacitor C_1. Here, the resistor and the VCCS which are parallel to v_{in} can be ignored since they only effect the current of v_{in} without changing the internal node equations. Next, the 2-ohm resistor which is parallel to C_1 is replaced by two 4-ohm resistors in parallel as shown in Fig. 3(c). Then, the current source and the 4-ohm resistor parallel to it are converted to a voltage controlled voltage source (VCVS) in series with two 2-ohm resistors as in Fig. 3(d). As the next step, we use the v_s-shift property [3] to convert one of the last created 2-ohm resistors into equivalent combination of two current controlled voltage sources (CCVS) and resistors connected series to them at both sides of the node designated by "v_{12}", as shown in Fig. 3(e). Finally, we convert the voltage controlled voltage source connected series with a 2-ohm resistor, which are vertically connected to node designated by "v_{12}" to a

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current source controlled by v_{in} in parallel with a 2-ohm resistor as shown in Fig 3(f). This step completes the circuit transformation that we need. All the steps explained above are depicted in Fig. 3.

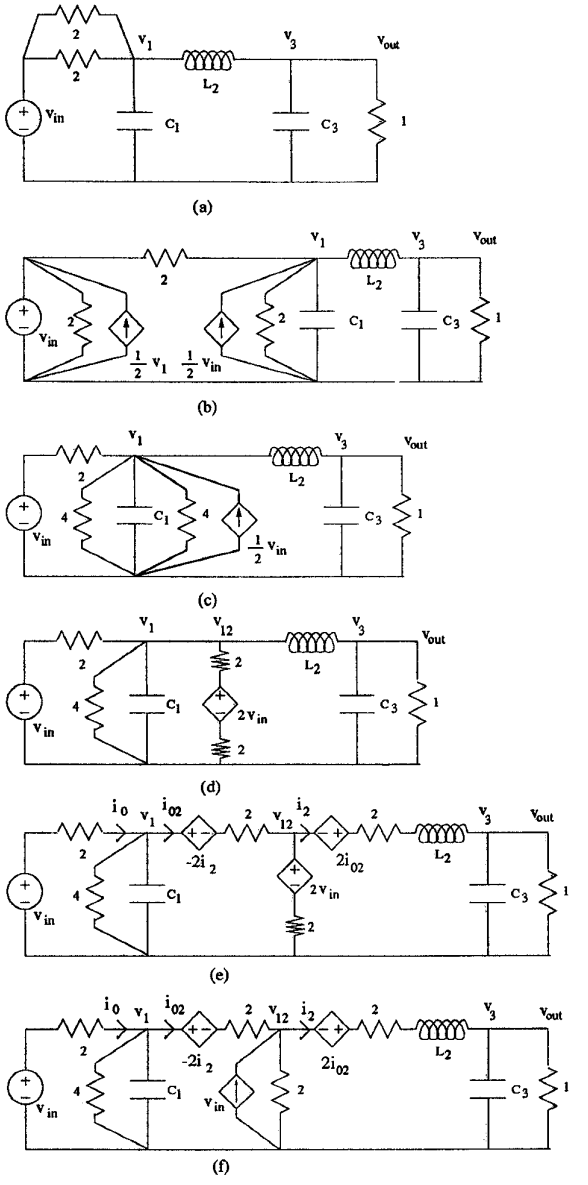

Figure 3. Transformation of the LC ladder prototype.

Now we can draw the signal-flow graph of the transformed circuit as shown in Fig. 4 by writing mesh and node equations in terms of the Laplace transforms of the variables v_{in}, i_0, v_1, i_{02}, v_{12}, i_2 and v_3. One can easily verify that the signal-flow graphs shown in Fig. 2 and Fig. 4 both realize the same transfer function, that is

$$T(s)=\frac{1}{s^3C_1L_2C_3+s^2L_2(C_1+C_3)+s(C_1+L_2+C_3)+2} \qquad (1)$$

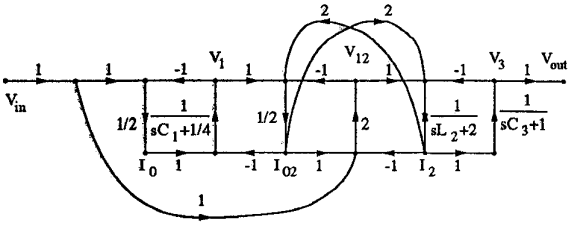

Figure 4. Signal-Flow Graph of the transformed circuit.

Although the process of transforming an LC ladder prototype into a new LC ladder circuit that contains damped integrators is explained here on a third-order LC ladder filter prototype, it can be easily realized that the same process can be continued further, in order to apply the same procedure to higher order, that is longer, all-pole low-pass LC ladder prototypes.

It is interesting to note that the signal-flow graph in Fig. 4 is composed of the subgraphs that are special cases of the generic signal-flow graph shown in Fig. 5(a). For instance, the subgraph at the input of the SFG in Fig. 4 has a constant incoming branch and constant outgoing branches. To obtain such a signal flow graph, C is chosen zero and $g_{mi} = 1$, and $g_{mp1} = g_{mp2} = 1$. The subgraph shown in Fig. 5(a) can be implemented by the linear circuit shown in Fig. 5(b). Let us just ignore the parasitic components C_i, g_{op} and g_{on} for the moment. For the most part, these parasitics are absorbed in the entire circuit by the intended shunt components. For instance g_{op} and g_{on} are absorbed by the the input conductance g_{mi} of the following stage which is the same type of subcircuit and C_i becomes shunt and increases the value of the actual capacitance of the integrator that may be following the subcircuit under consideration. The linear circuit shown in Fig. 5(b) can be implemented by the current-mode building blocks as the CMOS current-mode low-voltage damped integrator [4] shown in Fig. 6. Since the capacitors C in both rails of the fully balanced circuit shown in Fig. 6 are connected in series, they are replaced an equivalent capacitor $C/2$. The transistors whose gates are connected to V_{cp} and V_{cn} are the ones used for tuning the integrators, or in other words for tuning the transconductances of the current mirrors. The transistor sizes are computed from the necessary transconductance values, that are g_{mi}, g_{mp}, and g_{mn}. Note that the branch

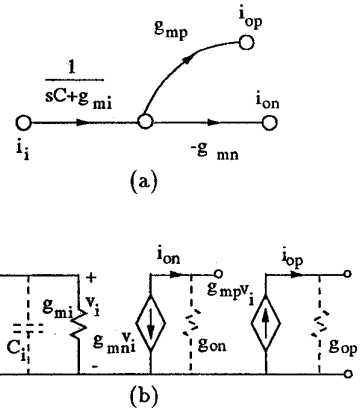

Figure 5. Basic signal-flow subgraph and the basic linear circuit realization.

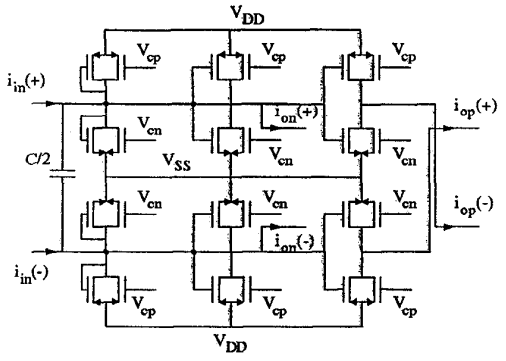

Figure 6. Fully balanced CMOS tunable current-mode low-voltage damped integrator.

transmittances in the signal-flow graph shown in Fig. 4 are normalized values with respect to 1rad/s and 1Ω. The transconductance corresponding to the unit branch transmittance should be computed by $C/(2\pi f_0)$, where C is the integrator capacitance and f_0 is the denormalization frequency.

3. SIMULATION RESULTS

The signal-flow graph of the transformed circuit shown in Fig. 4 is constructed by using the circuit blocks described in Fig. 5 in order to examine the performance of the equivalent active network. The active implementation of the building blocks is realized using MOS transistors and capacitors by means of CADENCE and considering a 2-μ double-metal double-poly CMOS technology. The active implementation basic building block integrator block is depicted in Fig. 6.

The simulation of the active network is performed for different cutoff frequencies which means for different capacitor values. The performance of the active equivalent circuit is listed for different LC ladder prototypes in table 1. The magnitude characteristics of LC ladder prototypes and the corresponding active implementations are depicted together for comparison in Fig. 7.

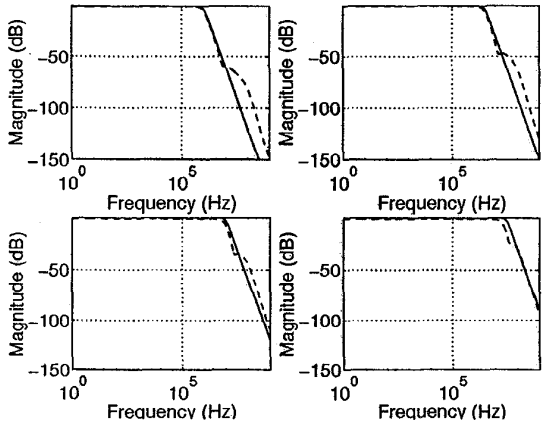

Figure 7. Transfer characteristics of the prototype and active filters for various cutoff frequencies.

The simulation results demonstrate that the performance of the active circuit is very close to the performance of the prototype circuit for low frequencies, but there is a slight

Prototype	Simulated	Cutoff (pr) f_{cpr}	Cutoff (sim) f_{csim}
$C_1 = 0.16\mu F$ $L_2 = 0.32\mu H$ $C_3 = 0.16\mu F$	$C_{C1} = 20.8pF$ $C_{L2} = 41.6pF$ $C_{C1} = 82.2pF$	$995kHz$	$938kHz$
$C_1 = 0.05\mu F$ $L_2 = 0.10\mu H$ $C_3 = 0.05\mu F$	$C_{C1} = 6.5pF$ $C_{L2} = 13.0pF$ $C_{C3} = 26.0pF$	$3.18MHz$	$2.84MHz$
$C_1 = 0.016\mu F$ $L_2 = 0.032\mu H$ $C_3 = 0.016\mu F$	$C_{C1} = 2.08pF$ $C_{L2} = 4.16pF$ $C_{C3} = 8.32pF$	$9.96MHz$	$7.68MHz$
$C_1 = 0.005\mu F$ $L_2 = 0.01\mu H$ $C_3 = 0.005\mu F$	$C_{C1} = 650fF$ $C_{L2} = 1.3pF$ $C_{C3} = 2.6pF$	$31.8MHz$	$17.3MHz$

Table 1. Simulation results for active filters filters with various cutoff frequencies.

hump at higher frequencies. It is verified by simulation that the reason for this hump is the parasitic capacitances in the active circuit. The effect of the parasitic capacitances prevents an exact pole-zero cancelation and results in the hump. But the hump does not cause a significant problem, for example for the filter with cutoff frequency at nearly 1MHz, the signal is suppressed nearly by 60dB where the hump occurs. For filters with higher cutoff frequencies, we have observed that the filter characteristic slightly shifts toward the lower frequencies. However, the tuning capability of the blocks used in the active implementation enables us to correct the deviations from the expected performance. In Fig. 8, it is shown how the performance of the circuit with cutoff frequency at approximately 32 MHz is corrected by tuning. Although it may not be important since it is a filter, the DC gain of the filter is less than what is expected. This occurs due to the input conductance of the mirrors are decreased and the absorbed output conductances become significant. This deviation can be corrected also simply by tuning the transconductance of the input or the output stage. Here, one should also note that the sim-

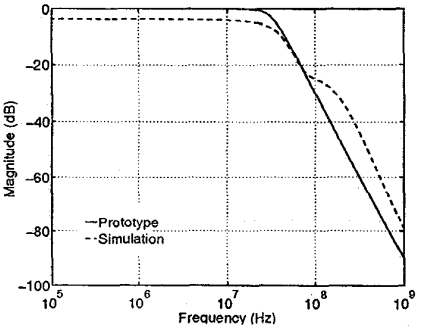

Figure 8. Correction of the cutoff frequency for the filter with cutoff frequency nearly 32MHz

ulations are performed with transistors with gate width of 2μ. Even better results can be obtained by using CMOS technologies with smaller feature sizes.

4. CONCLUSIONS

This work presents an approach for realization of the internal operation of an LC ladder filter by a current-mode active circuit using current mirrors and capacitors only. It is verified by simulation, considering CMOS 2–μ technology and by a full-custom design using CADENCE design tools, that the implementation of the proposed method yields good results. The tunability of the building blocks makes it possible to correct the performance of the filter for higher frequencies. Although the approach is presented by a third-order example, it can be easily applied to higher order LC ladder prototypes by induction. The presented approach is discussed for all-pole low-pass LC ladder prototype. However, it can be extended easily to arbitrary configurations in order to include also the elliptic, band-pass and high-pass LC ladder prototypes. Since the approach is independent of how the current mirrors are implemented. It can be applied by employing other current-mirrors such as cascode and improved Wilson current mirrors and other technologies such as Bipolar, BiCMOS or GaAs. The same approach can be easily applied by using also voltage mode circuits, switched-capacitor and transconductance-C circuits since the approach finds a signal-flow graph build by damped integrators.

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