Fabrication of Vacuum-Sealed Capacitive Micromachined Ultrasonic Transducers With Through-Glass-Via Interconnects Using Anodic Bonding

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***Abstract*— This paper presents a novel fabrication method for vacuum-sealed capacitive micromachined ultrasonic transducer (CMUT) arrays that are amenable to 3D integration. This paper demonstrates that MEMS structures can be directly built on a glass substrate with preformed through-glass-via (TGV) interconnects. The key feature of this new approach is the combination of copper through-glass interconnects with a vibrating silicon-plate structure suspended over a vacuum-sealed cavity by using anodic bonding. This method simplifies the overall fabrication process for CMUTs with through-wafer interconnects by eliminating the need for an insulating lining for vias or isolation trenches that are often employed for implementing through-wafer interconnects in silicon. Anodic bonding is a low-temperature bonding technique that tolerates high surface roughness. Fabrication of CMUTs on a glass substrate and use of copper-filled vias as interconnects reduce the parasitic interconnect capacitance and resistance, and improve device performance and reliability. A 16×16-element 2D CMUT array has been successfully fabricated. The fabricated device performs as the finite-element and equivalent circuit models predict. A TGV interconnect shows a 2-Ω parasitic resistance and a 20-fF shunt parasitic capacitance for 250-μm via pitch. A critical achievement presented in this paper is the sealing of the CMUT cavities in vacuum using a PECVD silicon nitride layer. By mechanically isolating the via structure from the active cells, vacuum sealing can be ensured even when hermetic sealing of the via is compromised. Vacuum sealing is confirmed by measuring the deflection of the edge-clamped thin plate of a CMUT cell under atmospheric pressure. The resonance frequency of an 8-cell 2D array element with 78-μm diameter circular cells and a 1.5-μm plate thickness is measured as 3.32 MHz at 15-V dc voltage (80% $V_{pull\text{-}in}$). [2016-0200]**

***Index Terms*— Capacitive micromachined ultrasonic transducer (CMUT), Through-glass-via (TGV), anodic bonding, 3D integration, glass.**

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I. Introduction

CLOSE integration of ultrasonic transducer arrays and front-end integrated circuits is critical for the overall ultrasound system efficiency and also a compact form factor. For 2D arrays and arrays used in ultrasound imaging catheters where the element area is small, the receiver electronics must be closely integrated with the transducer array to avoid additional parasitic capacitance introduced by the cables to preserve signal quality. The capacitive micromachined ultrasonic transducer (CMUT) technology has attracted a great deal of attention because of advantages such as ease of fabricating arrays and integrating them with supporting electronics, as well as wide bandwidth [1]. Two main methods have been developed for integrating CMUTs with supporting circuits: monolithic integration and hybrid integration [2]. For monolithic integration, one method is to co-process the CMUTs and the electronics side by side [3]. In this method, not only the substrate area is shared by CMUTs and electronic circuits, but also the properties and vertical dimensions of the layers used in the CMUT structure are limited by the CMOS process materials and film thicknesses. The other method is to fabricate the electronic circuit first and then build the CMUTs on top by post-processing [4]–[7]. This method has a good area utilization and more dimensional control, but the CMUT process is still limited because of the temperature constraints set by the existing metal lines. The complexity of the overall process also increases.

Hybrid integration allows the optimization of CMUTs and electronics independently. In hybrid integration, through-wafer interconnects are established as part of CMUT arrays to enable a close connection with supporting electronics by chip-to-chip bonding or through an intermediate layer such as an interposer or a flex circuit [8], [9]. The current implementation of this hybrid integration approach is based on using through-silicon-vias [10]. Since silicon is a semiconductor, a reverse biased PN junction or a metal-insulator-semiconductor (MIS) structure has to be used to isolate individual connections to each element in an array and to reduce the parasitic capacitance [11]. The implementation of an isolation structure complicates the fabrication process. Using polysilicon as a via and electrode material degrades the surface quality and wafer flatness, affecting subsequent processing steps. Last, the

fabricated devices could suffer from a leakage current and reverse junction breakdown. An alternative interconnection method used for CMUTs is to create deep isolation trenches in a highly conducting silicon substrate, where the resulting pillar underneath each element serves as the interconnect from the front to the backside of the wafer [12]. This process is also complicated and creates reliability problems due to the exposed gaps between top and bottom electrodes of the CMUT array elements on the top surface.

Through-glass-vias (TGVs) have been used for advanced electronic packaging, especially for RF applications where parasitics are critical [13]. Anodic bonding is widely used for wafer-level hermetic MEMS packaging [14]. In recent years, fabrication of CMUTs on a glass substrate has aroused significant interest [15]–[17]. We have recently reported a process for fabricating vacuum-sealed CMUTs on a borosilicate glass substrate using anodic bonding [18]. This process benefits from all the advantages of wafer bonding, including process simplicity, control over plate thickness and properties, high fill factor, and ability to implement large vibrating cells. Additionally, it reduces the parasitic capacitance and series resistance benefiting from an insulating substrate and a metal bottom electrode, respectively. In this work, we extend this process by incorporating TGV interconnects. Our first attempt to incorporate TGVs in our anodic bonding based process fell short of yielding vacuum-sealed devices [19]. Here in this paper we present improvements in our design and process flow to achieve vacuum sealing. We also present further characterization results regarding TGV performance.

In the next section, we first present the fabrication process flow. In Section III, the measured and simulated results of static surface deflection and measured TGV resistance and capacitance are presented. Also, the electrical input impedance characterization is performed demonstrating the devices are vacuum-sealed and the measured performance agrees well with the equivalent circuit model (ECM) and also the finite-element model (FEM). Section IV discusses some important aspects of the fabrication process and proposes further improvements.

II. Fabrication Process

The targeted implementation is illustrated in Fig. 1, where the CMUTs are fabricated on a TGV substrate and directly flip-chip bonded to an integrated circuit (IC). The vibrating plate consists of a thin single-crystal silicon layer embedded between a silicon nitride insulation layer at the bottom and a metal electrode on top. The bottom electrodes are formed in the etched glass cavities and connected to the dedicated TGV interconnects giving each element electrical access from the backside. The metal layer deposited on top of the silicon plate is common to all elements in an array and is connected to a TGV for backside access. A stacked metal layer is deposited and patterned on the backside to form the bondpads.

The starting substrate is a standard 0.7-mm thick, 100-mm diameter borosilicate glass wafer (Borofloat 33, Schott AG, Jena, Germany) that has a high surface quality with an RMS roughness of 0.7 nm and a good flatness (warp < 10 μm and bow < 58 μm) (Fig. 2a). The thermal expansion coefficient of the borosilicate glass substrate is 3.25 $ppm/°C$, close to

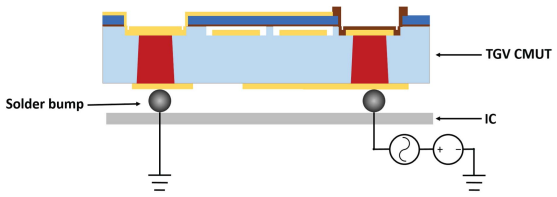


Fig. 1. A schematic cross-section of a completed CMUT element with TGV interconnects flip-chip bonded on an IC.

that of silicon (3.2 $ppm/°C$). The SOI wafer that we used for implementing the thin plate has a 2 ± 0.5-μm-thick, n-type device layer with 0.001-0.005 Ω·cm resistivity, a 0.5-μm-thick BOX layer, and a 500-μm-thick handle wafer with 1-10 Ω·cm resistivity. A total of five masks are used for the fabrication process presented in Fig. 2. The via on the left in the cross-sectional drawings and the via in the back in the 3D drawings are for the top electrode connection. The via on the right in the cross-sectional drawings and the via on the front in the 3D drawings are for the bottom electrode connection.

A. Design and Formation of the TGVs

The vias are designed on the 100-mm wafer area for both bottom and top electrode connections for different array geometries. The alignment marks are also formed by TGVs for aligning the subsequent layers to the via pattern.

Through-wafer channels are created first in the 0.7-mm borosilicate glass substrate at the designed via locations by laser drilling (Fig. 2b). The through channels are then metallized by using the conductive copper paste technology (Triton Microtechnologies, Oro Valley, AZ) [20] (Fig. 2c). A benefit of this approach is that the paste has a thermal coefficient of expansion (TCE) matched to that of the glass substrate. Therefore, potential mechanical stress that can be caused by further heating steps and possible cracks around the vias can be minimized. Then, the wafer is sintered and polished. By selecting the appropriate coating material on the substrate before polishing and using a slurry loaded with composite particles as abrasive during the chemical-mechanical polishing (CMP) process, a smooth glass surface and a good copper-to-glass surface coplanarity are obtained [21], [22]. For a completed TGV wafer, the via location is in the range of ±5 μm from the designed location in both X and Y directions, which is the accuracy of the laser drilling. The diameter of the via is 70 μm at the laser entry side and 50 μm at the laser exit side. We build the CMUTs on the laser exit side and use the laser entry side for the backside pad formation. With 33207 vias formed on the 100-mm wafer area, the average wafer warp increased from $\sim$10 μm to $\sim$50 μm. Fig. 3 shows the optical image of the finished TGV substrate and a closeup view of the vias. Fig. 4a shows the scanning electron microscope (SEM) cross-sectional image of a TGV embedded in the glass substrate. Fig. 4b shows the atomic force microscope (AFM) image of the via surface on the laser exit side. At the via-glass boundary on the surface, copper and glass are at the same level in most regions around each via, which makes a reliable electrical connection between the CMUT electrodes and the TGVs possible.

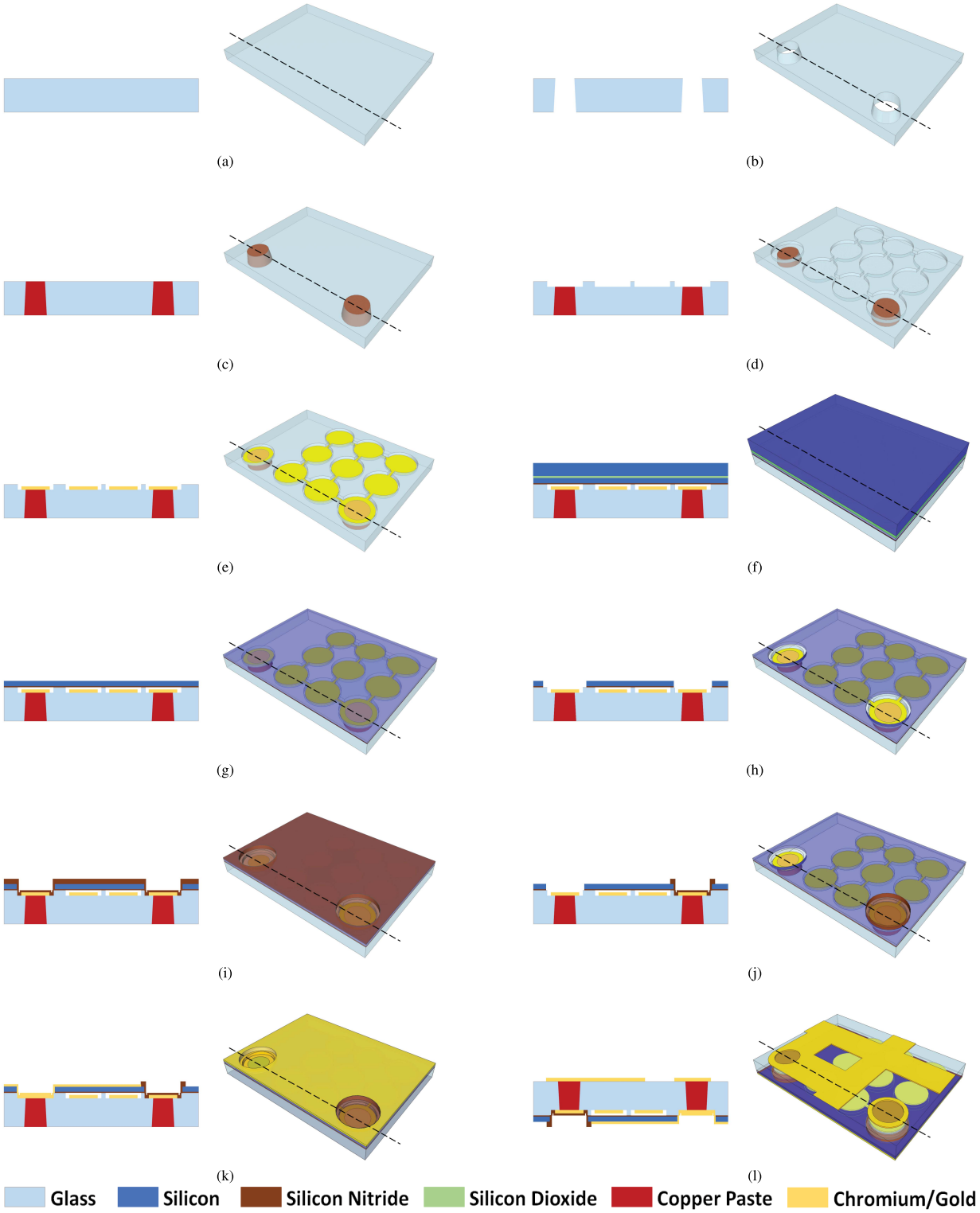


Fig. 2. Fabrication process flow: (a) Initial glass substrate; (b) Laser drilling; (c) Metalization of the vias; (d) Glass etch; (e) Metal deposition and lift-off; (f) Insulation layer deposition on the SOI and anodic bonding; (g) Handle and BOX removal; (h) Silicon/silicon nitride etch for gas evacuation, array separation, and reaching top electrode connection; (i) PECVD silicon nitride deposition for sealing; (j) Silicon nitride etch; (k) Top electrode deposition and metal etch; (l) Backside metalization by lift-off.

B. Forming Cavities and Bottom Electrodes Connected to the TGV

The TGV substrate was cleaned using a heated N-Methyl-2-pyrrolidone (NMP@70°C) solution to remove organics and contaminants from the surface. Acid based cleaning solutions cannot be used because of the copper in the via. After cleaning, the cavities were patterned using a negative photoresist with the alignment of each element to the dedicated TGV. We used reactive ion etching (RIE) to etch glass instead of buffered oxide etchant (BOE) in order to avoid peeling of the

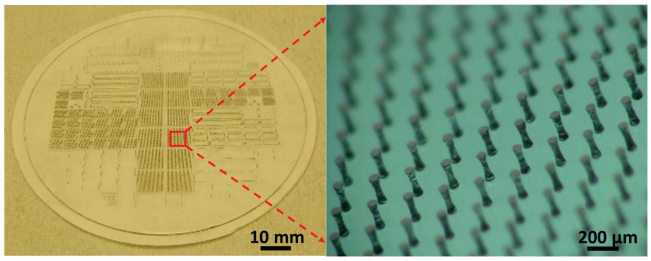
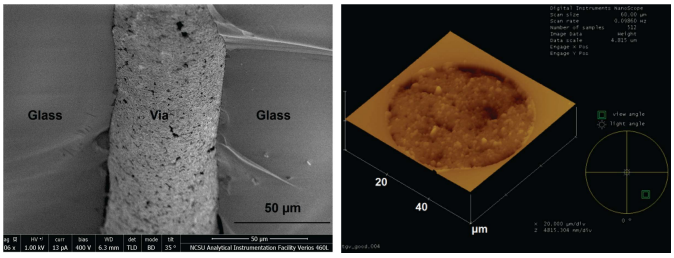


Fig. 3. Optical image of a 100-mm borosilicate glass wafer with completed TGVs (left). A closeup view of the vias embedded in the glass substrate (right).



(a) (b)

Fig. 4. (a) SEM cross-sectional image of a TGV. (b) AFM top-view image of a via surface.

photoresist and not to damage copper vias. Dry etching also helps achieve a deeper cavity, which is desired for a thicker bottom electrode to build a reliable connection to the TGV. We performed RIE with SF_6 gas to realize a glass cavity depth of 320 nm (Fig. 2d). After removing the photoresist, the bottom electrode was patterned by a second photolithography step using a 2-μm-thick negative photoresist (AZ-5214E IR, Clariant, Wiesbaden, Germany), which is suitable for lift-off. Prior to the bottom metal deposition, we wet etched the copper vias also 320 nm using a copper etchant (Copper Etchant 49-1, Transene Company, Inc., Danvers, MA) in order to keep the glass surface at the bottom of the cavity level with the copper via surface. This selective wet etchant does not attack the photoresist and helps remove the copper oxide on the via surface and consequently improve the electrical connectivity between the bottom electrode and the TGV. Then a stacked metal that consists of 20-nm chromium as an adhesion layer and 130-nm gold was deposited into the cavity by evaporation and defined by lift-off as bottom electrode to obtain a 170-nm gap height and to build the electrical connection from the TGV to the bottom electrode (Fig. 2e). The AFM image of the cavity (Fig. 5) demonstrates an RMS surface roughness of 3.3 nm on the bottom metal surface after lift-off. The RMS surface roughness on the glass post remains 0.7 nm. Fig. 6 shows the top view of the processed substrate that is ready for anodic bonding.

C. Anodic Bonding

A 200-nm low-stress silicon nitride insulation layer was deposited on the device layer of the SOI wafer by plasma-enhanced chemical vapor deposition (PECVD) prior to bonding. The TGV wafer was cleaned with a solvent-based solution and the SOI wafer was cleaned using Piranha solution. The borosilicate glass surface and the nitride insulation layer

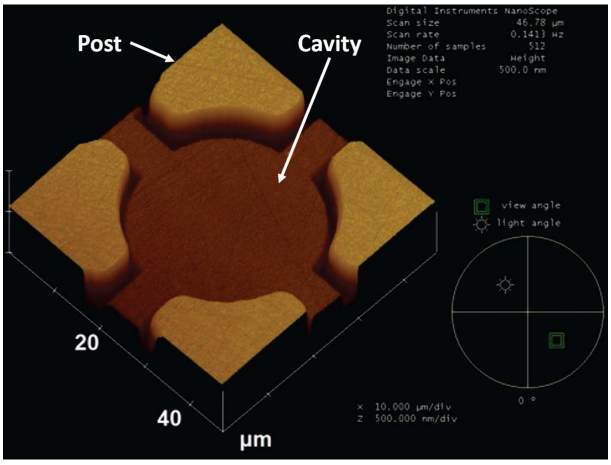


Fig. 5. AFM image of the bottom metal defined in a glass cavity.

surface were brought together in vacuum (10^{-4} Torr) and then bonded at 350°C under 2.5-kN down force in a semi-automatic bonding system (Model EVG510, EVG Group, St. Florian, Austria) (Fig. 2f). It is important to keep the wafer in vacuum before increasing the temperature to prevent copper oxidation. The handle layer of the SOI wafer was then ground down to 100 μm. At this step, a protection layer (ProTEK B3 alkaline protective coating, Brewer Science, Rolla, MO) was coated and cured on the backside in order to protect the vias during the handle wafer removal process. This protection layer also prevents any liquid from flowing into the bonded cavities through the via locations in case there is a leakage. A heated tetramethylammonium hydroxide (TMAH) solution (10% TMAH@85°C) was used to selectively etch the remaining handle layer over the BOX layer. The silicon plate was released after removing the BOX layer in 10:1 BOE solution (Fig. 2g).

D. Reaching Vias and Sealing

We performed a third photolithography step in order to evacuate the gas generated during anodic bonding, and also to reach the vias for top electrode connection. The lines to guide the final dicing of the arrays were defined at the same time. For the gas evacuation we chose to open the plate over the TGV for bottom metal connection (Fig. 2h). In this way we could later seal this location so that the via is mechanically isolated from the active area but electrically connected to the bottom electrode. This improves the reliability of the process because CMUT operation will be independent of the TGV condition in case of failure of hermetic sealing around the via, which would break the CMUT vacuum and degrade the CMUT performance. This was observed in our first-generation devices, mainly because of some microcracking around the via boundary [19].

Prior to sealing, the photoresist on the frontside was removed by oxygen plasma and the protection layer on the backside was removed by RIE using CF_4 gas. The wafer was then sealed under vacuum with 1-μm conformal PECVD silicon nitride at 1000-mTorr chamber pressure and 350°C temperature (Fig. 2i). In order to avoid copper oxidation,

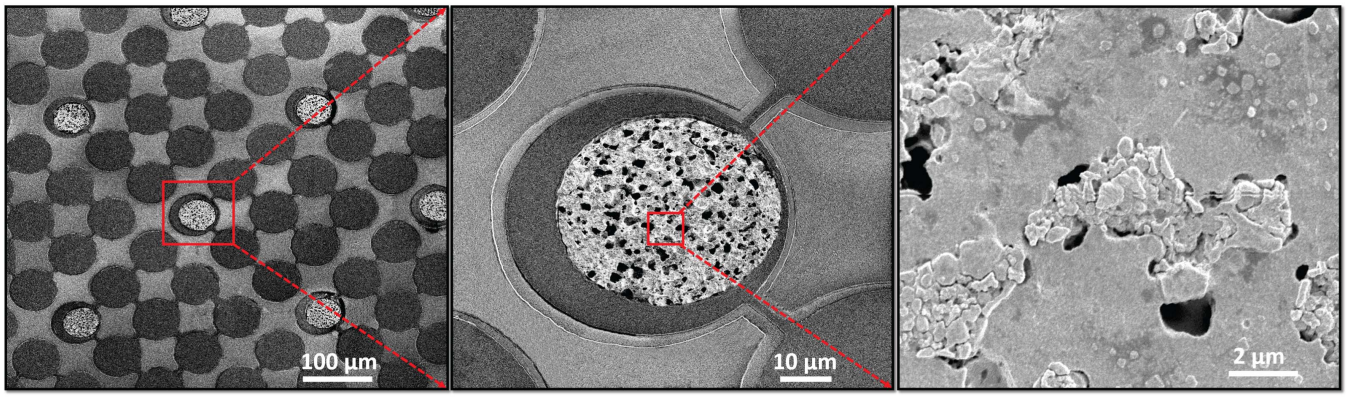


Fig. 6. SEM images of the completed glass substrate with TGVs that is ready for anodic bonding. The left image shows the elements defined on the glass substrate. Each element is composed of 9 cells including the one for TGV connection. In the middle is a zoomed image of a cell with a TGV. The right image shows a closeup view of the TGV surface.

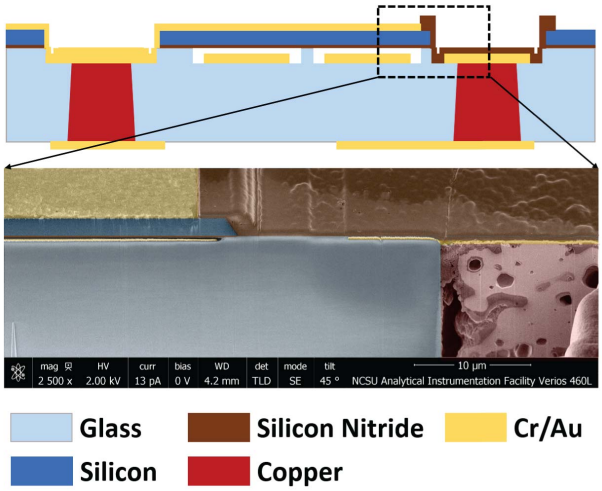


Fig. 7. SEM cross-section of a finished CMUT cell next to the TGV interconnect for an element. (Pseudocolor added to show different layers matching to the corresponding cross-sectional drawing).

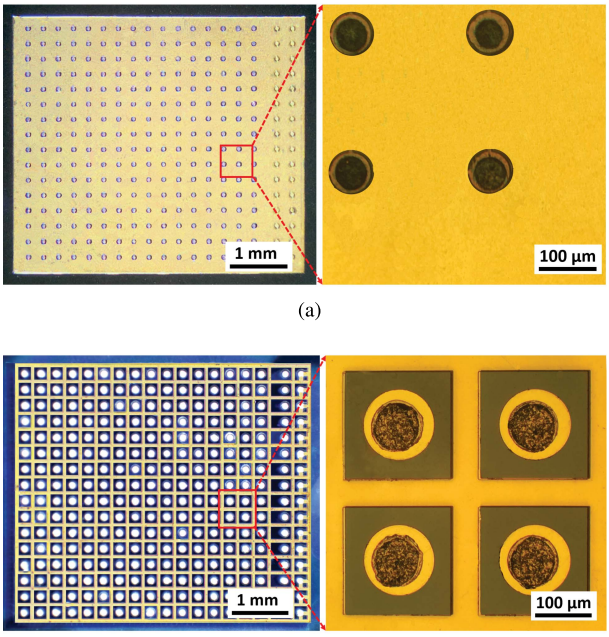


Fig. 8. (a) Front side view of the completed 16×16-element 2D CMUT array. (b) Backside view of the completed 16×16-element 2D CMUT array.

the wafer needs to stay in vacuum when chamber temperature is above 100°C.

E. Forming Electrical Contacts

To create the top electrode connections, the silicon nitride layer on the top electrode connection vias had to be removed. At this point, the silicon nitride deposited on the conductive silicon plate was also removed and the sealing layer was only left covering the cell that encloses bottom electrode TGV (Fig. 2j). After removing the negative photoresist using oxygen plasma, 20-nm chromium and 180-nm gold were deposited by dc sputtering over the entire wafer. The silicon nitride etching mask was used again, this time with positive photoresist to remove the metal on the sealing region in order to eliminate the parasitic capacitance at this location (Fig. 2k).

The last photolithography was done on the backside to define the bottom electrode pads and a rectangular grid of top electrode connections to facilitate probing of elements. 20-nm chromium and 180-nm gold were deposited and then lifted off on the backside (Fig. 2l). At this step the device fabrication was completed. The SEM image in Fig. 7 shows the cross-section of a completed CMUT cell with the dedicated TGV for bottom electrode connection. Fig. 8a is the optical image of the front side of the fabricated 16×16-element 2D CMUT array. Fig. 8b shows the array backside that has bondpads and lines distributing the top electrode connection to facilitate testing using a probe station. The physical parameters of the fabricated transducer elements are shown in Table I.

III. Characterization of the Fabricated Devices

A. Characterization of the Deflection of the Thin Plate Under Atmospheric Pressure

Compared to our work reported in [19], the major improvement of this study is that a reliable vacuum sealing of the active CMUT cells could be achieved by mechanically isolating the through-glass via from the active CMUT cells. The achievement of vacuum sealing can be confirmed by

TABLE I
PHYSICAL PARAMETERS OF THE FABRICATED CMUT ARRAY

Shape of the cell	Circular
Cell diameter, μm	78
Cell-to-cell distance, μm	4
Top metal thickness, μm	0.2
Silicon layer thickness in plate, μm	1.5
Insulating layer thickness in plate, μm	0.2
Gap height, μm	0.17
Bottom metal thickness, μm	0.15
Substrate thickness, μm	700
Number of cells per element	8
Length of an element, μm	243
Width of an element, μm	243
Element pitch, μm	250

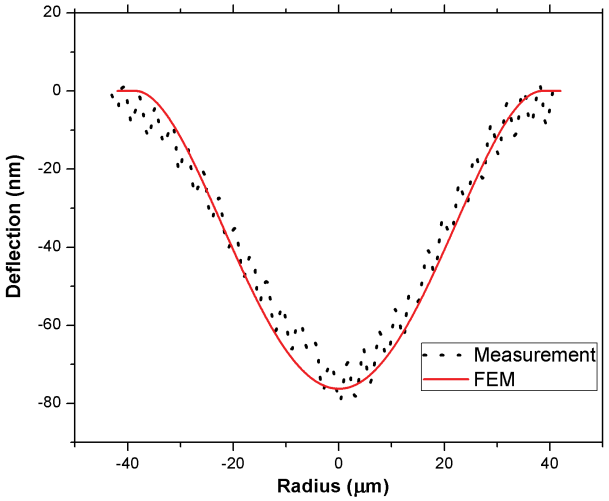


Fig. 9. Measured and simulated deflection profile of the plate after the device fabrication was completed.

measuring the plate deflection under atmospheric pressure. We used a stylus surface profilometer (Dektak 150, Veeco Instruments Inc, Plainview, NY) and measured a maximum deflection of 80 nm in the center of a circular CMUT cell (Fig. 9). The finite element model (ANSYS v.15, ANSYS, Inc., Canonsburg, PA) predicts that the atmospheric deflection is 78 nm, confirms the sealing, and also proves that there is no significant stress generated on the plate during the fabrication.

B. Characterization of the TGV Parasitic Resistance and Capacitance

One of the main motivations for using copper through-glass vias for interconnection is the reduced parasitic resistance and parasitic capacitance. We designed via test structures with different pitch (125 μm, 190 μm, and 250 μm) to characterize the via resistance and via-to-via capacitance as shown in the left panel of Fig. 10a. Both resistance and capacitance measurements were performed by accessing the vias from the backside of the wafer after the backside metal pad formation. The resistance test vias are connected on the front side by a metal layer that is formed at the step of bottom metal deposition. The measurement setups are shown in the right panel of Fig. 10a.

The via resistance test structures include two vias connected with a metal line. Therefore the resistance includes two TGV

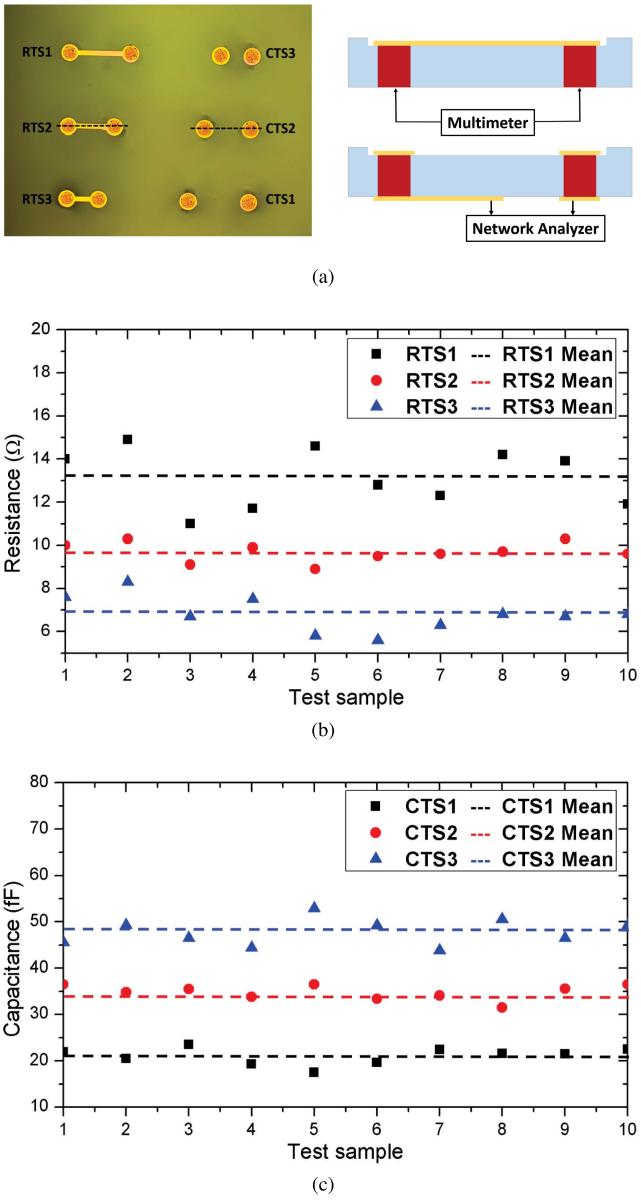


Fig. 10. (a) Via test structures (left panel), via resistance measurement setup (right panel top), and via-to-via capacitance measurement setup (right panel bottom). (b) Measured results for resistance test structures. (c) Measured results for capacitance test structures.

resistances in series with the resistance of the 20-μm-wide metal line between the vias. We measured 10 test structures for each pitch using a multimeter (U1272A Handheld Digital Multimeter, Agilent, Santa Clara, CA) connected to two needle probes in a probe station. The resistance distribution is shown in Fig. 10b and the average resistance of structures with 125-μm, 190-μm, and 250-μm pitch are 6.8 Ω, 9.7 Ω, and 13.1 Ω, respectively. As a result, the resistance of a single via including the contact resistance is calculated as approximately 2 Ω. The bottom gold sheet resistance is approximately 1 Ω/sq, which matches the sheet resistance of 130-nm-thick gold that has been reported in the literature [23].

The via-to-via capacitance is mainly contributed by the two vias as electrodes with the glass as a dielectric between them. The metal pads on the via will only contribute a negligible

TABLE II

AVERAGE VIA-TO-VIA CAPACITANCE: MEASUREMENT AND SIMULATION RESULTS

Via-to-via distance	Measured	FEM	Analytical
125-μm	47.8 fF	51.7 fF	54.1 fF
190-μm	34.8 fF	37.9 fF	38.6 fF
250-μm	21 fF	30.5 fF	32.8 fF

amount of capacitance. The capacitance measurement is performed by using a 125-μm pitch coplanar microwave probe (Model ACP40-GSG-125, Cascade Microtech, Beaverton, OR) connected to a network analyzer (Model E5061B, Agilent Technologies, Inc., Santa Clara, CA). The calibration was carefully done in a tight frequency range from 10 MHz to 10.000005 MHz in order to measure the femtofarad-level capacitance. The measured capacitance distribution is shown in Fig. 10c and the average capacitance of structures with 125-μm, 190-μm, and 250-μm pitch are 47.8 fF, 34.8 fF, and 21.0 fF, respectively. The measured values are confirmed by the finite element model and analytical calculation using Eq.1. In the equation, $2d$ is the center-to-center pitch of two vias; R is the via radius; l is the substrate thickness, i.e, via length. Some variance between the model and the measurement could be due to the fact that the actual via is tapered while the model assumes the via to be cylindrical. The comparison of the measurements and models is summarized in Table II. One should also note that the parasitic capacitance is between the signal electrode (bottom electrode) and ground (top electrode) for each element. Hence the measured via parasitic capacitance represents the worst case. To that end, the measured via-to-via capacitance is a more accurate representation for element-to-element electrical coupling. In any case, given the CMUT device capacitance is usually in the order of picofarads, the parasitic capacitance introduced by the TGV interconnects is negligible

$$C = \frac{\pi \varepsilon_0 \varepsilon_r l}{ln[\frac{d}{R} + \sqrt{[\frac{d}{R}]^2 - 1}]}. \quad (1)$$

C. Characterization of Electrical Input Impedance in Air

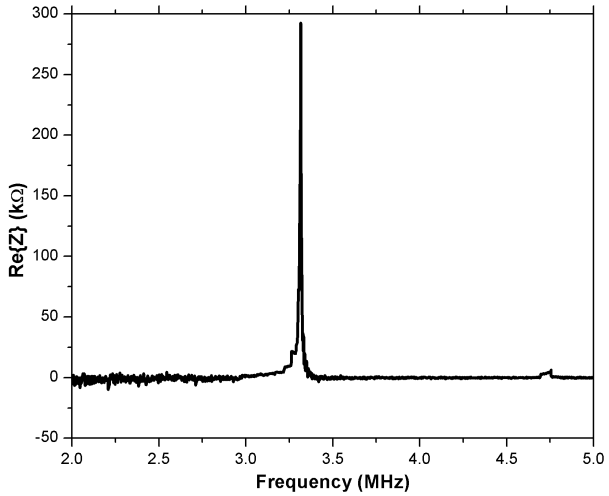
We tested the fabricated elements in air using a network analyzer (Model E5061B, Agilent Technologies, Inc., Santa Clara, CA) with an internal dc voltage source available up to 40 V. We probed the elements from the backside of the wafer. The real and imaginary parts of the electrical input impedance are measured in air (Fig. 11). The open-circuit resonance frequency of a 2D CMUT array element was measured as 3.32 MHz at 15-V dc voltage, which is approximately 80% of the pull-in voltage. The baseline in the real part corresponds to the series resistance of the device that includes via resistance as well as the resistance of the bottom electrode, which is measured as 21 Ω at 5 MHz from Fig. 11a. The device capacitance is calculated as 2274 fF at 5 MHz from Fig. 11b.

The resonance frequency, collapse voltage, and device capacitance were simulated using the equivalent circuit model [24] and by finite element model using TRANS 126 electromechanical transducer elements for direct coupling of electrostatic and structural domains. The material properties used in the simulations are listed in Table III. The simulations and the measurements are compared in Table IV. The results show that the fabricated CMUTs with TGV interconnects have a small parasitic capacitance (approximately 200 fF) and operate as predicted by the models.

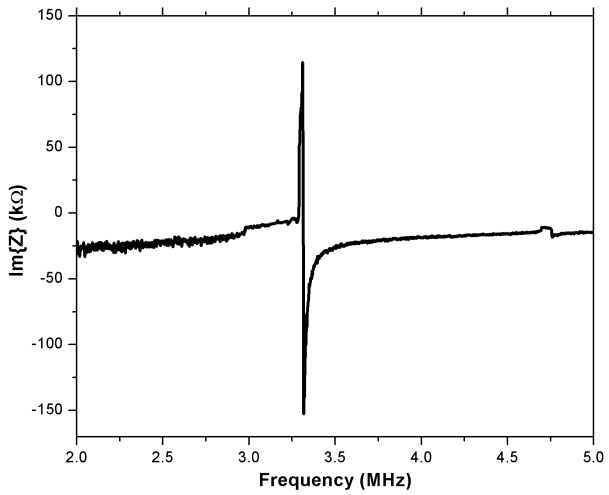
TABLE III

MATERIAL PROPERTIES USED IN SIMULATIONS

	Glass	Silicon	Silicon Nitride	Gold
Young modulus, GPa		148	260	70
Density, kg/m^3		2328	3100	3300
Poisson ratio		0.17	0.27	0.33
Relative permittivity	4.6	11.7	5.7	



(a)



(b)

Fig. 11. Impedance measurements (V_{dc} = 15 V) (a) Real part of the electrical input impedance; (b) Imaginary part of the electrical input impedance.

IV. DISCUSSION

The selection of the sealing location is critical for reliable vacuum sealing of the CMUTs. In the presented fabrication method, we choose to open the plate over the bottom electrode TGV. On one side this approach evacuates the gas inside the cavity if the via is hermetically sealed; On the other

TABLE IV
SIMULATED VERSUS MEASURED DEVICE PERFORMANCE IN AIR

	Measured	ECM	FEM
Resonance Frequency	3.32 MHz	3.47 MHz	3.34 MHz
Collapse Voltage	17.5 V	15.4 V	17 V
Device Capacitance	2274 fF	2001 fF	2054 fF

side, the sealing silicon nitride deposition step isolates the CMUT cavities in case of a leaking via. Therefore, a reliable sealing could be achieved regardless of the hermetic property of the TGV.

In the presented approach, by decreasing the substrate thickness, a smaller via diameter could be realized and thus more space and flexibility in array design can be achieved. 40-μm vias with 80-μm pitch have already been demonstrated in a 0.65-mm-thick borosilicate glass wafer [22]. 20-μm vias are possible in 0.3-mm-thick borosilicate glass. Several aspects of the process flow could be further improved. First, the insulation silicon nitride could be replaced by an ALD HfO_2 layer defined in the CMUT cavities by lift-off process. We demonstrated the feasibility of this approach in [25]. Also, for a better plate thickness control an etch-stop could be added after the handle removal process to avoid the silicon plate overetch in sealing nitride etching step.

First and foremost, this paper demonstrates the process feasibility for incorporating TGVs in 2D CMUT array fabrication using anodic bonding. The fabricated arrays need to be flip-chip bonded to the electronics for immersion measurements, which is outside the scope of the presented work but will be investigated in the future.

V. CONCLUSION

In this paper we presented a CMUT fabrication process that integrates TGV interconnects and anodic bonding. The process is low-temperature and eliminates the need for an insulating lining for making through-wafer interconnects. Anodic bonding has the specific advantage of being more tolerant to roughness on the bonding surface compared to commonly used fusion bonding technique. By opening the plate over the bottom electrode TGV and then re-sealing, a reliable vacuum seal can be achieved for all the elements.

The use of glass as substrate and metal for interconnects and electrodes reduce the parasitic capacitance and the series resistance of the CMUTs. The resistance of a single via is measured as 2 Ω. The via-to-via capacitance of a 250 μm-pitch via pair is measured as 21 fF. The impedance measurements demonstrate the fabricated device has low parasitics and operates as the models predict.

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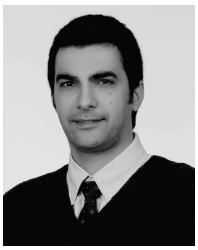

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