

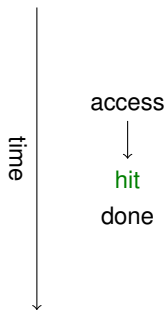
THE ENTANGLING INSTRUCTION PREFETCHER

Alberto Ros Alexandra Jimborean

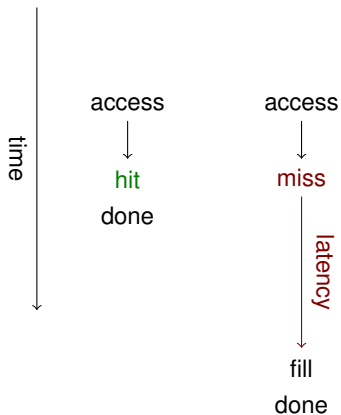
University of Murcia, Spain

May 31, 2020

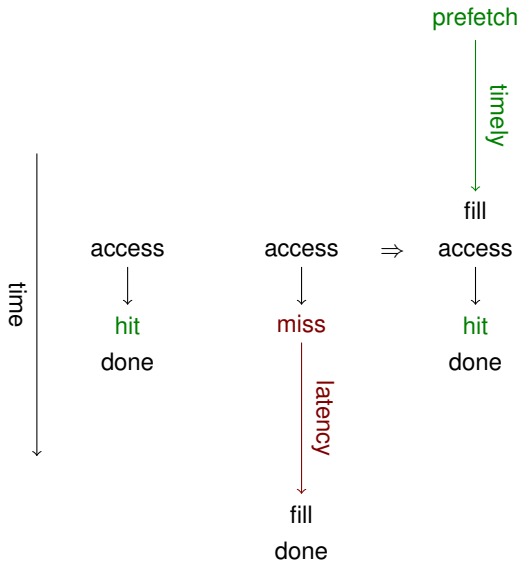
MOTIVATION: TIMELINESS



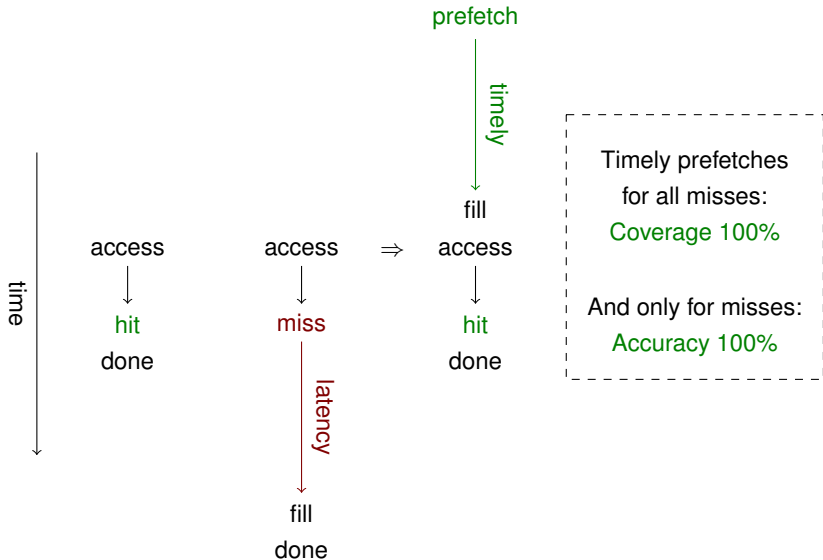
MOTIVATION: TIMELINESS



MOTIVATION: TIMELINESS



MOTIVATION: TIMELINESS



CONCEPT OF ENTANGLED ACCESSSES



CONCEPT OF ENTANGLED ACCESSSES

prefetch 1



access 1



miss



fill
done

CONCEPT OF ENTANGLED ACCESSSES



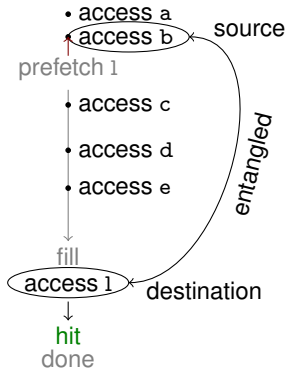
CONCEPT OF ENTANGLED ACCESSSES



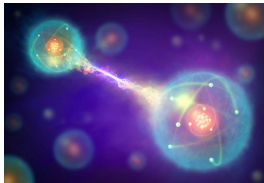
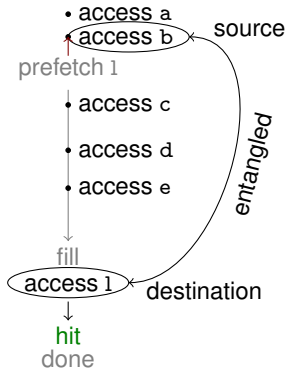
CONCEPT OF ENTANGLED ACCESSSES



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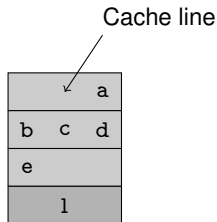
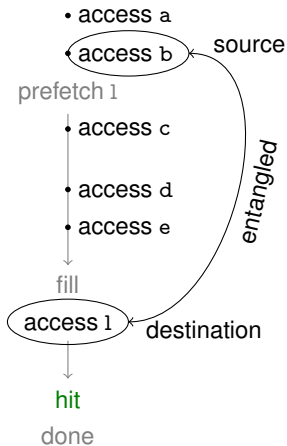
Quantum entanglement

(Image: © MARK GARLICK/SCIENCE

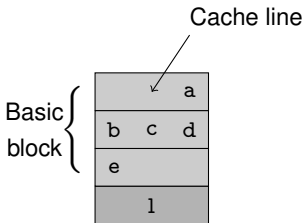
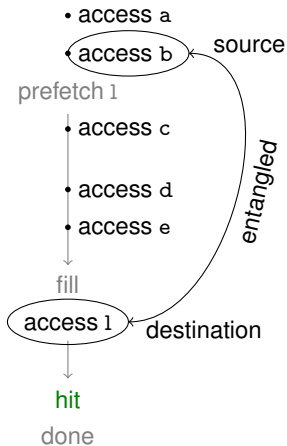
PHOTO LIBRARY/Getty)

THE ENTAGLING PREFETCHER FOR INSTRUCTIONS —EPI—

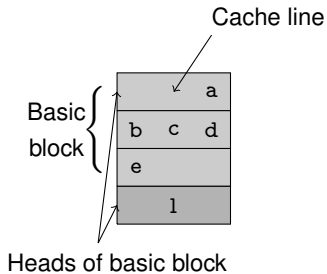
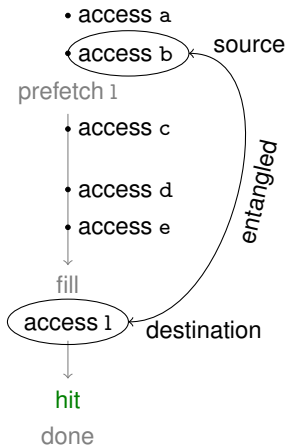
ENTANGLING CACHE LINES HEAD OF BASIC BLOCKS



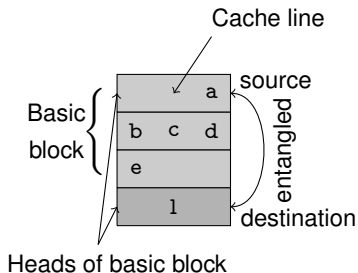
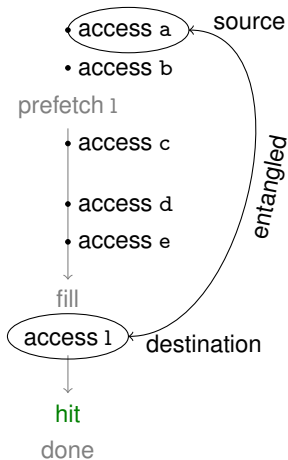
ENTANGLING CACHE LINES HEAD OF BASIC BLOCKS



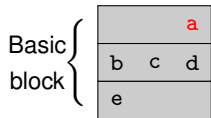
ENTANGLING CACHE LINES HEAD OF BASIC BLOCKS



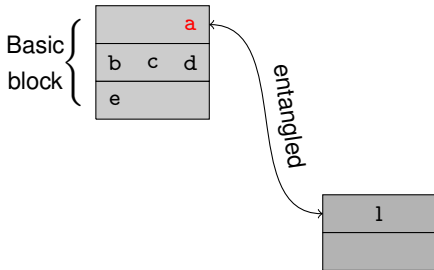
ENTANGLING CACHE LINES HEAD OF BASIC BLOCKS



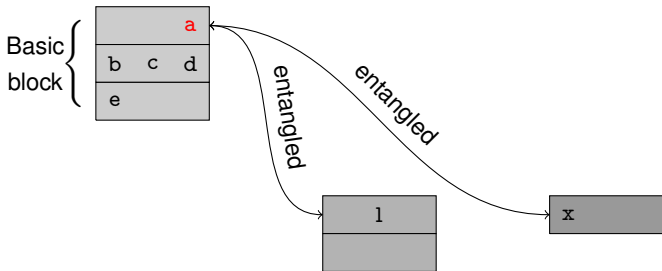
WHAT TO PREFETCH ON AN ACCESS TO a?



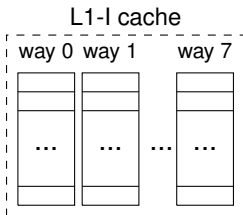
WHAT TO PREFETCH ON AN ACCESS TO a?



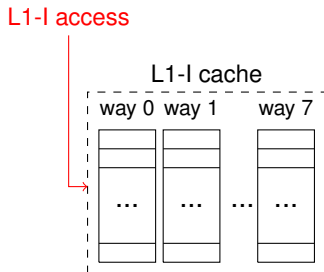
WHAT TO PREFETCH ON AN ACCESS TO a?



DESIGN OF EPI



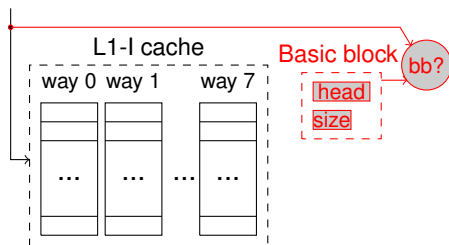
DESIGN OF EPI



DESIGN OF EPI - FINDING BASIC BLOCKS

0	a
1	b c d
2	e
0	1

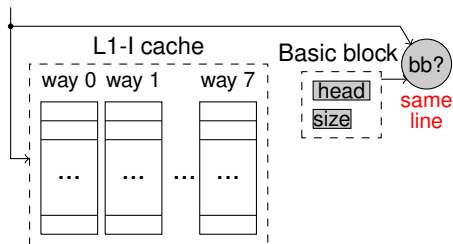
L1-I access



DESIGN OF EPI - FINDING BASIC BLOCKS

0	a
1	b c d
2	e
0	1

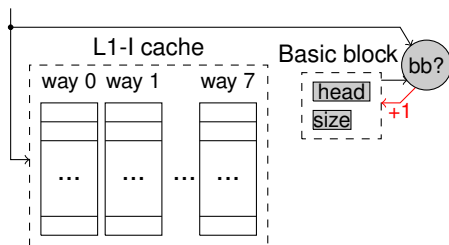
L1-I access



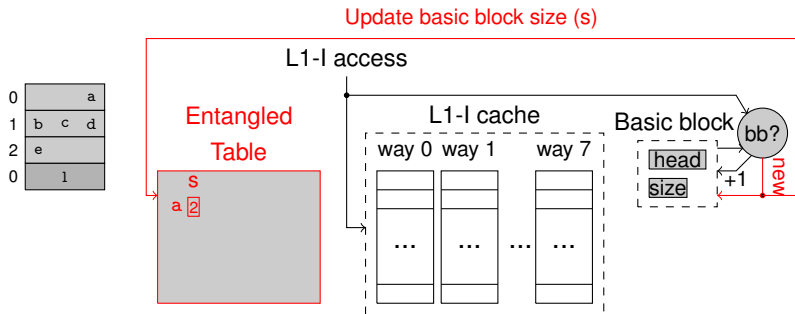
DESIGN OF EPI - FINDING BASIC BLOCKS

0	a
1	b c d
2	e
0	1

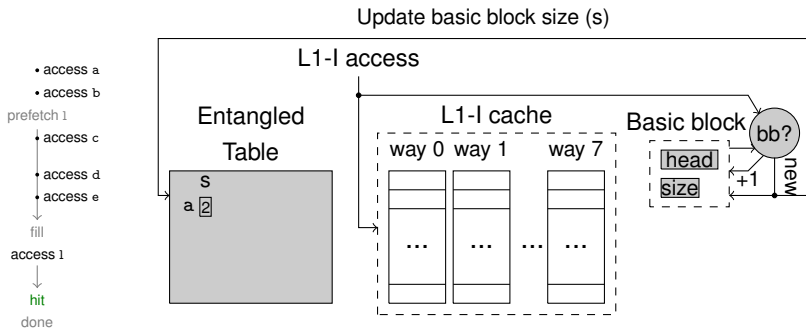
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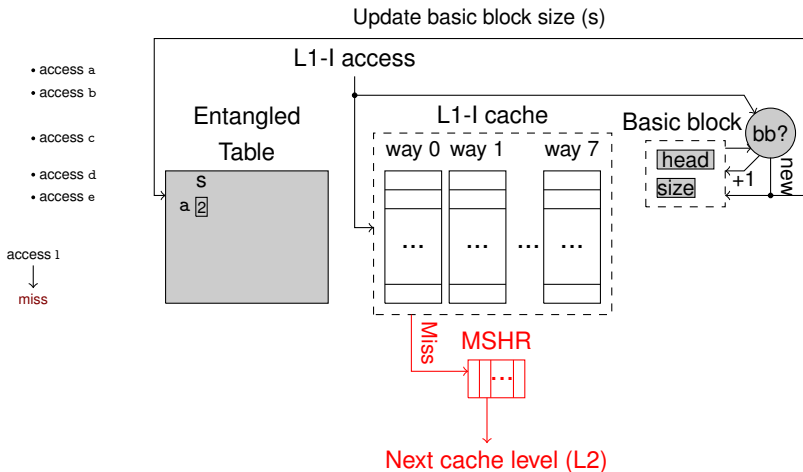
DESIGN OF EPI - FINDING BASIC BLOCKS



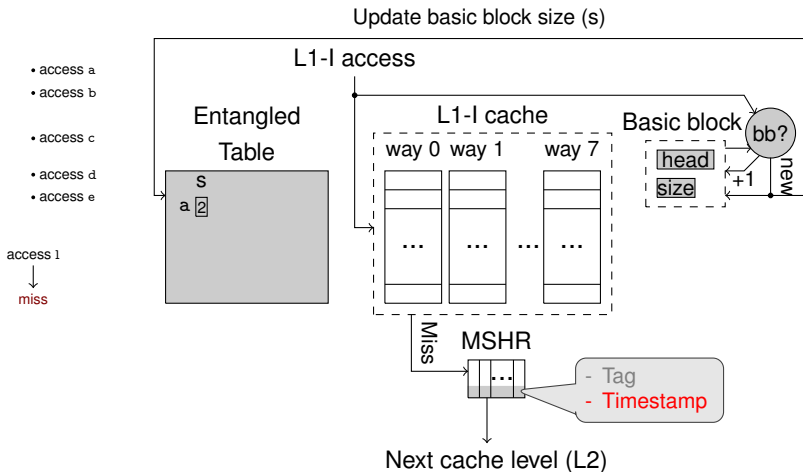
DESIGN OF EPI - ENTANGLING CACHE LINES



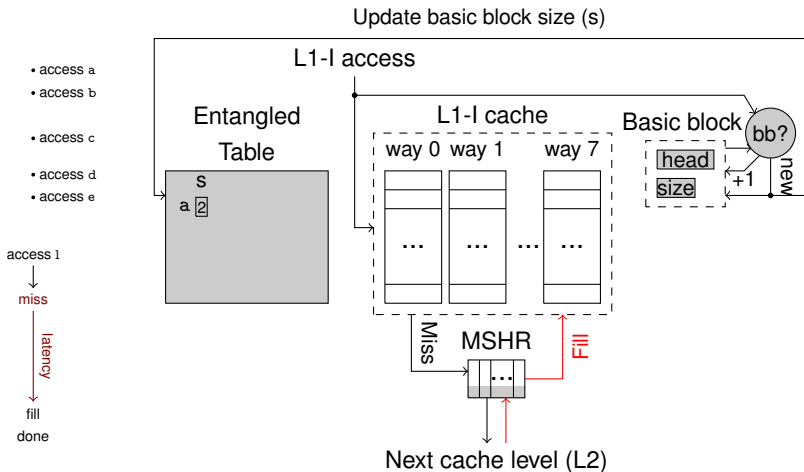
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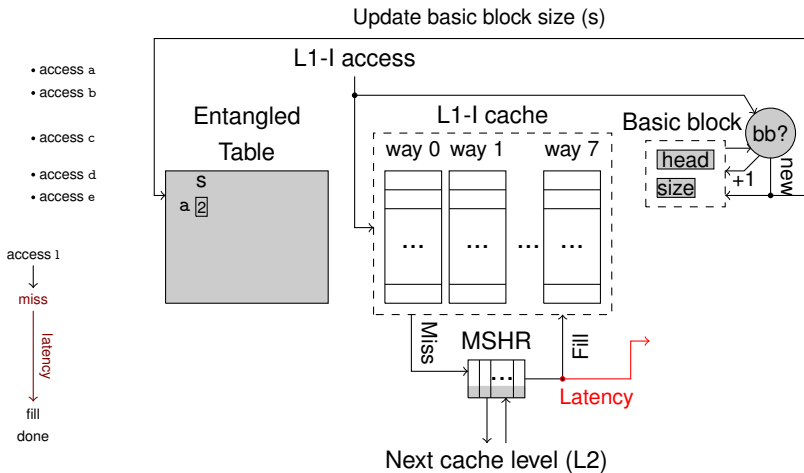
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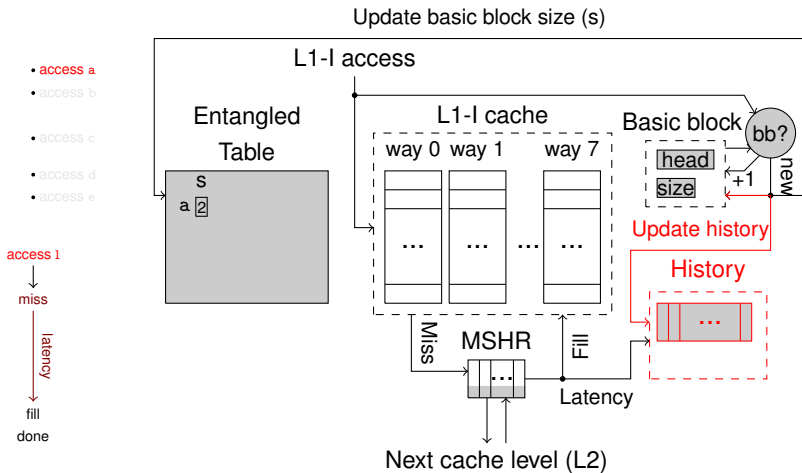
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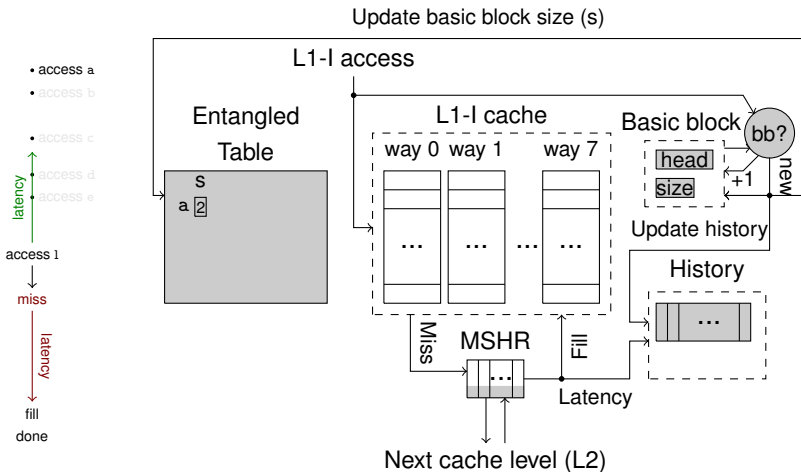
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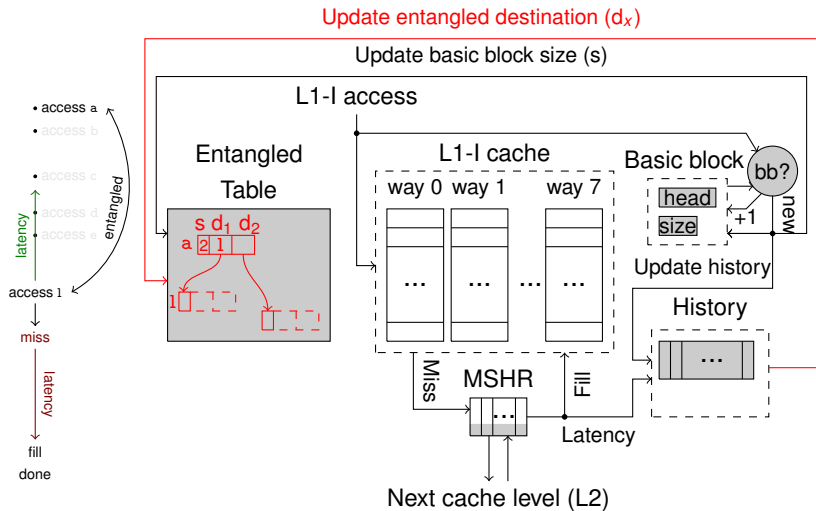
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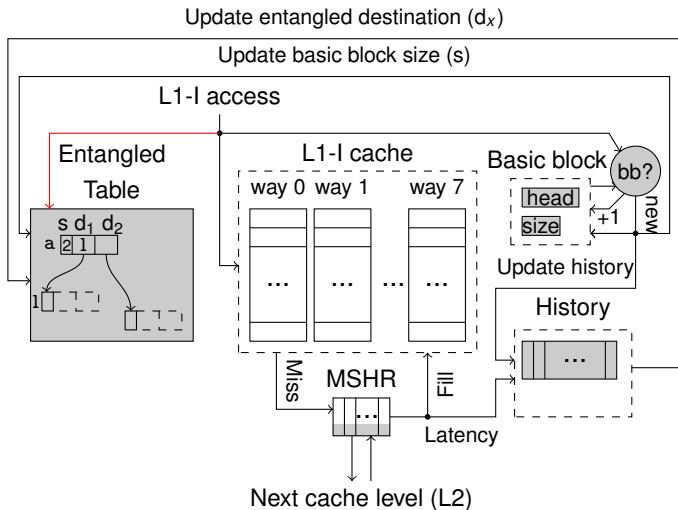
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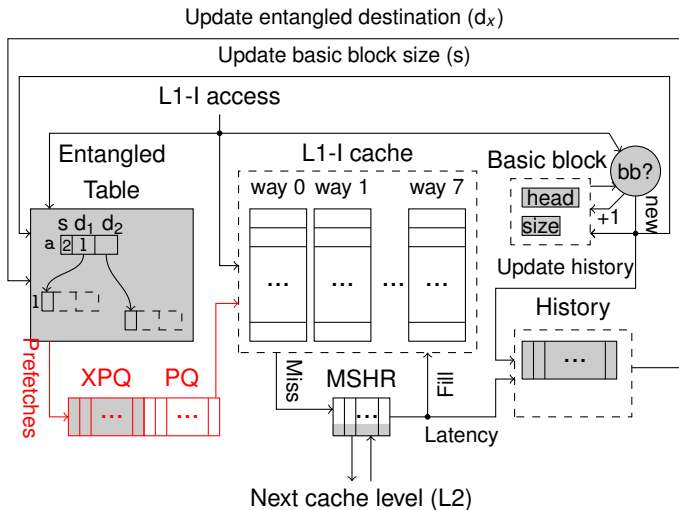
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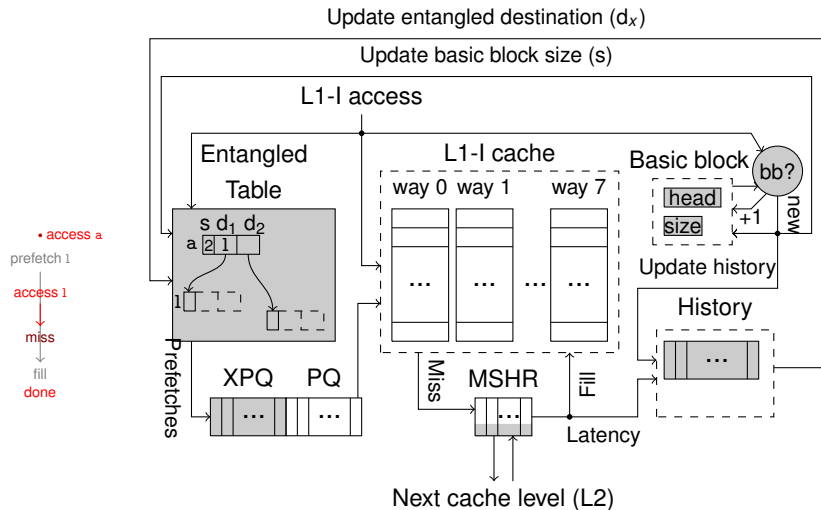
DESIGN OF EPI - ISSUING PREFETCHES



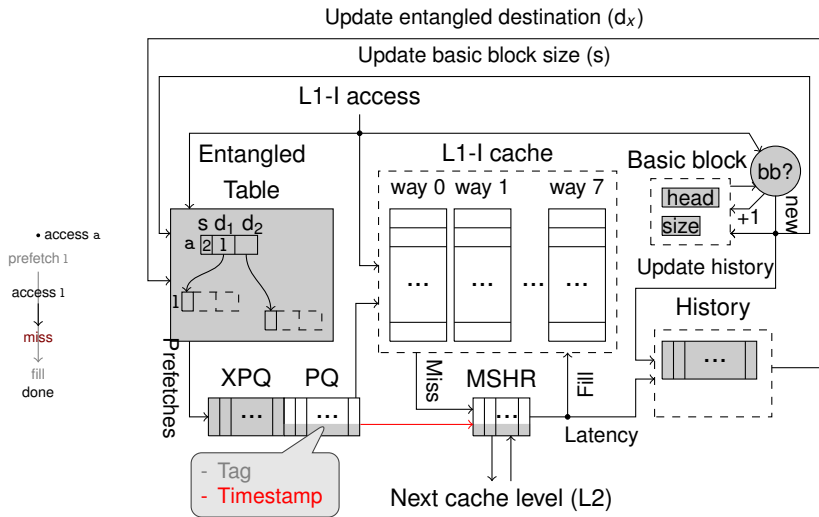
DESIGN OF EPI - ISSUING PREFETCHES



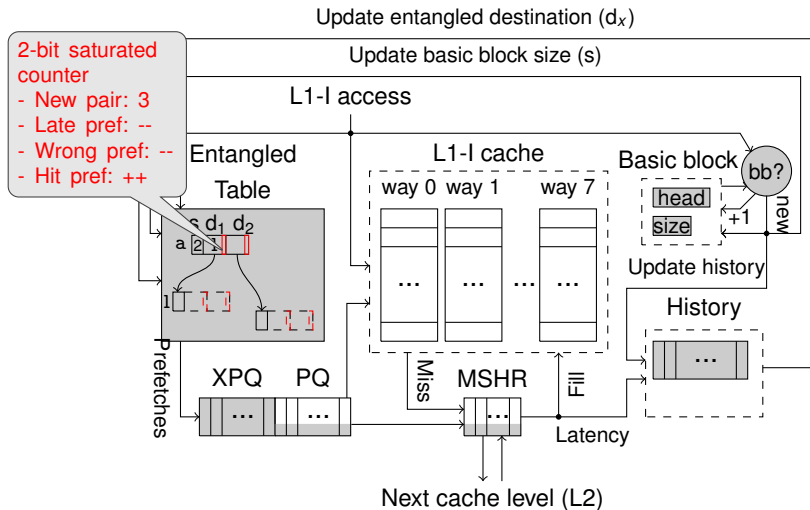
DESIGN OF EPI - FIXING LATE PREFETCHES



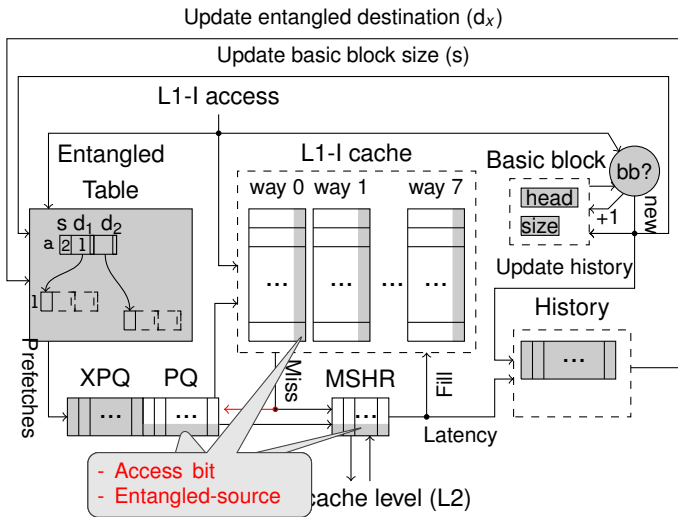
DESIGN OF EPI - FIXING LATE PREFETCHES



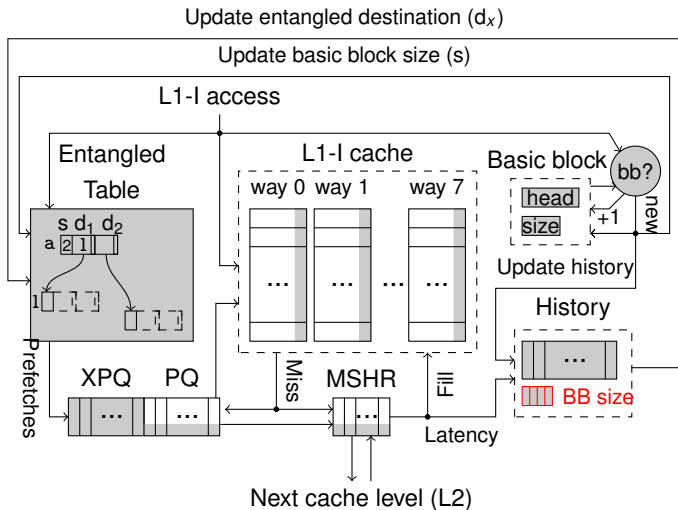
DESIGN OF EPI - CONFIDENCE FOR ENTANGLED PAIRS



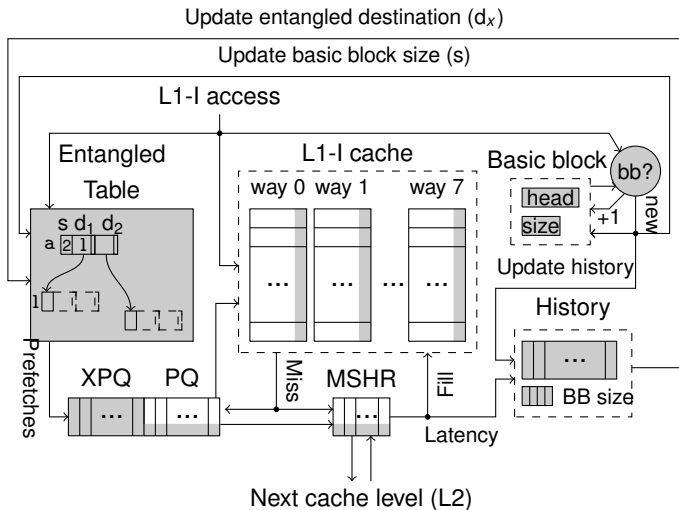
DESIGN OF EPI - CONFIDENCE FOR ENTANGLED PAIRS



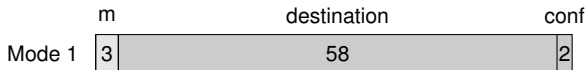
DESIGN OF EPI - MERGING BASIC BLOCKS



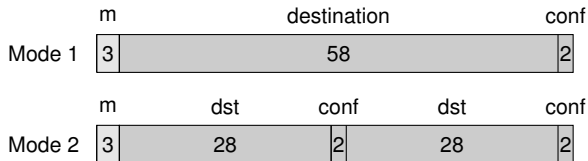
DESIGN OF EPI



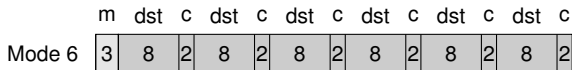
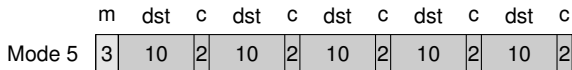
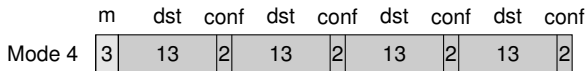
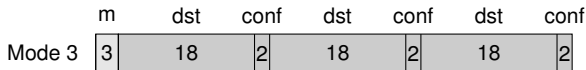
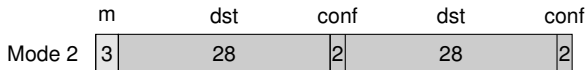
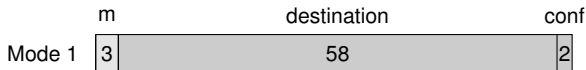
COMPRESSING DESTINATIONS



COMPRESSING DESTINATIONS



COMPRESSING DESTINATIONS



RESULTS

Prefetcher	Size (KB)	Norm. IPC	Coverage	Accuracy	Misses (%)
No-IPref	0.00	1.000	0.000	0.000	23.055

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NextLine	0.00	1.085	0.244	0.307	17.754

RESULTS

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No-IPref	0.00	1.000	0.000	0.000	23.055
NextLine	0.00	1.085	0.244	0.307	17.754
EPI-4w	14.15	1.155	0.639	0.736	8.575
EPI-8w	27.25	1.253	0.850	0.764	2.540
EPI-12w	40.36	1.281	0.921	0.773	1.084

RESULTS

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EPI-12w	40.36	1.281	0.921	0.773	1.084
EPI-16w	53.36	1.288	0.941	0.774	0.805
EPI-20w	66.46	1.290	0.946	0.774	0.736
EPI-24w	79.46	1.291	0.947	0.774	0.717
EPI-28w	92.46	1.292	0.949	0.774	0.705
EPI-32w	105.56	1.293	0.949	0.774	0.697
EPI	127.98	1.295	0.956	0.770	0.623

CONCLUDING REMARKS

- **Timeliness** as a key property
- **Entangles** heads of basic blocks to trigger timely prefetches
- Good performance/area trade-off

THE ENTANGLING INSTRUCTION PREFETCHER

Alberto Ros Alexandra Jimborean

University of Murcia, Spain

May 31, 2020



ECHO, ERC Consolidator Grant (No 819134)